A Fully-Integrated Shift-Register DLDO Using Pull-Up and Pull-Down Devices

by

Junyi Shen
B.S. , University of Shanghai for Science and Technology, 2019

Submitted to the Graduate Faculty of the

Swanson School of Engineering in partial fulfillment

of the requirements for the degree of

Master of Science in Electrical and Computer Engineering

University of Pittsburgh

2021

UNIVERSITY OF PITTSBURGH

SWANSON SCHOOL OF ENGINEERING

This thesis was presented

by

Junyi Shen

It was defended on

March 5, 2021

and approved by

Samuel Dickerson, PhD, Assistant Professor, Department of Electrical and Computer Engineering

Rajkumar Kubendran, PhD, Assistant Professor, Department of Electrical and Computer Engineering

Thesis Advisor: In Hee Lee, PhD, Assistant Professor, Department of Electrical and Computer Engineering

A Fully-Integrated Shift-Register DLDO Using Pull-Up and Pull-Down Devices

Junyi Shen, M.S.

University of Pittsburgh, 2021

The digital low-drop-out regulator (DLDO) regulates its output voltage and provides a fast transient response during a load change. DLDO is an essential part for managing power consumption of multiple supply voltage domains in modern system-on-chip (SOC) designs. One of the conventional DLDO designs uses a shift register (SR) to regulate the output voltage by controlling shift directions of the output bits. The shift register changes the output bits sequentially, hence providing high accuracy in steady state. However, due to this characteristic, the SR-based DLDO cannot provide a fast transient response during a load change. Higher clock frequency during the load transient can solve the problem, but it results in higher power consumption. To overcome this disadvantage, this paper offers a fully-integrated SR-based DLDO with pull-up and pull-down switches. It discusses optimization of the pull-up and pull-down switch size in detail.

Table of Contents

List of Tables

List of Figures

1.0 Introduction

In modern system-on-chip (SOC) designs, multiple power domains are used to enhance the performance while keeping power consumption low. For example, in a microprocessor with multiple power domains, a cache could remain activated for data retention while a main core is power gated [1]. A low-dropout regulator (LDO) is an essential building block to manage the supply voltage of the different power domains [2]. With improvement of process technology, the minimum supply voltage has become near- or sub-threshold voltage of transistors, making conventional analog LDOs difficult to achieve a high gain and bandwidth [3]. A digital LDO (DLDO) is challenging the analog LDO with a wider range of operation voltage, fast transient response and process scalability [4]. Recent studies has provided a variety of controller designs on DLDOs [5]–[11]. DLDOs with shift register [5] (SR) and barrel shifter [6] demonstrated a small steady state error. However, SR-based DLDO suffers from a large voltage droop at load transition since SR changes output bits linearly. Also, the SR-based design heavily depends on clock speed so that it suffers from high power consumption even with adaptive frequency control technique [6]. A large output capacitor reduces the voltage droop, but it cannot be integrated and requires extra pins and areas. This paper provides a SR-based DLDO only with fully-integrated 800pF output capacitor while achieving fast output regulation using pull-up and pull-down transistors.

2.0 Research Background

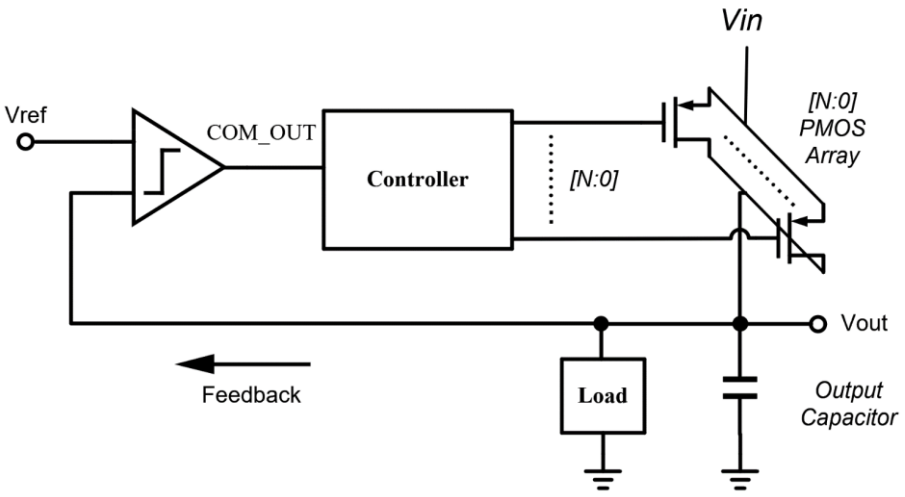

Figure 1 Block diagram of conventional DLDO.

Figure 1 shows a conventional DLDO that consists of 5 parts such as a comparator, a controller, power transistors, an output capacitor and a load circuit. The comparator generates a feedback signal by comparing output voltage (Vout) with reference voltage (Vref). Most DLDOs use clocked comparators [4]–[7], [9], [12] due to low power consumption, high speed, high precision, and low operating voltage. Especially, it dissipates ultra-low power by updating its output with a clock signal [13]. The controller is one of the most important parts in DLDOs and divided into two classes (time-driven and event-driven) in recent studies. The time-driven controller forms a synchronous design by using clock signals and continuously evaluate the output voltage and eliminate the error. It includes DLDOs with a shift register [5], a barrel shifter [6] and a successive approximation register [7],[9]. On the other hand, the event-driven controller only works when Vout is lower than Vref. It monitors Vout with multiple comparators to create dead-zone for event triggering. The controller enters hibernation mode when a steady state is detected, consuming

lower power than the time-driven design. The both types of controllers typically generate an one-hot or thermometer code and control the following power transistors, usually PMOS array. It adjusts the number of turned-on power transistors and regulates Vout around Vref. It controls the power transistors by estimating the load current (Iload) given a load condition. A DLDO employs an output capacitor for fast transient response by handling conditions with fast Iload change. In general, an output capacitance of <1nF can be integrated on chip, saving an off-chip component. The output capacitance which cannot be integrated requires extra pins and PCB areas, increasing the overall cost. As a result, restricting the output capacitance is important in DLDO designs. Thus, it is critical to achieve fast response, low voltage droop, a wide dynamic load range while integrating the output capacitance on chip. In addition to the conventional DLDOs, different DLDO designs have been proposed, including switched-capacitor-based design [14].

3.0 Proposed DLDO Design

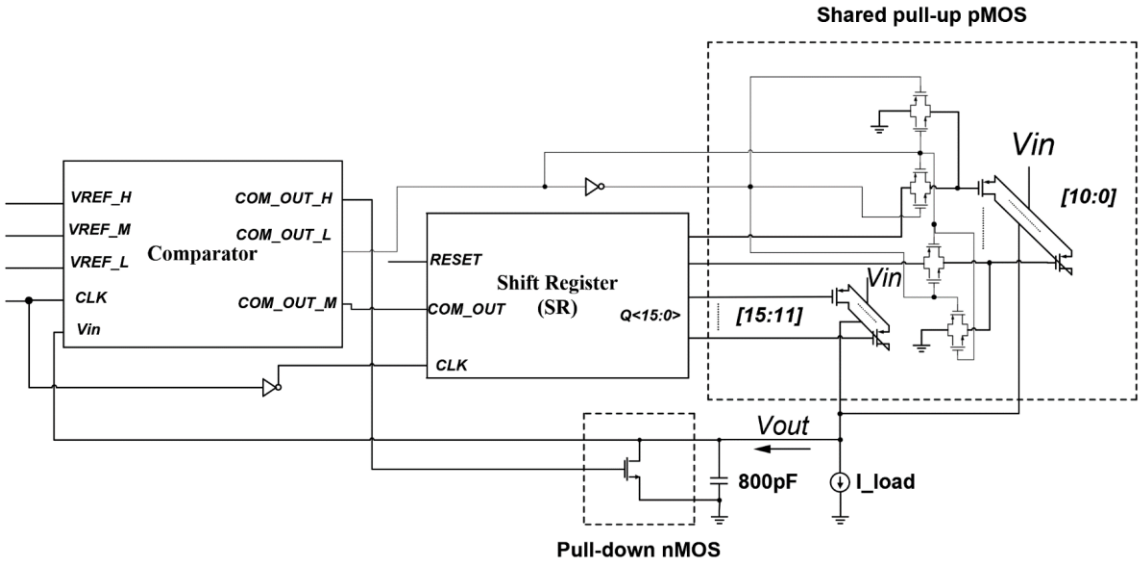

Figure 2 Proposed DLDO block diagram.

Figure 2 shows the proposed DLDO with 6 parts such as a comparator, a 16-bit SR, power transistors, logic circuits and 800pF output capacitor. Vin is the varying input supply voltage and Vout is the output voltage regulated by the power transistors.

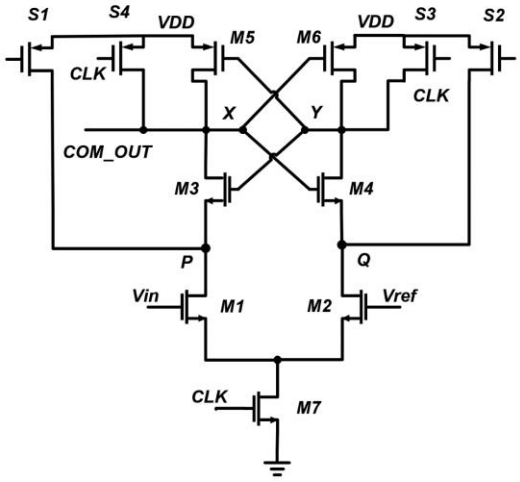

Figure 3. Comparator for proposed DLDO.

Figure 3 shows the dynamic comparators of the proposed design with low power consumption, rail-to-rail output and fast speed [15]. This structure consists of a clocked differential pair (M1 & M2), two cross-coupled pairs (M3 & M4 and M5 & M6), and four pre-charge switches (S1, S2, S3 and S4). It operates in three phases: reset, amplification and regeneration. During the reset phase (CLK = 0), the turned-on pre-charge switches (S1 – S4) pre-charges the nodes P, Q, X and Y high. In amplification phase (CLK = 1), the pre-charged nodes P, Q, X and Y are discharged through transistors M7. Constant common-mode voltage turns on M1 and M2 always. Differential voltage creates a slight difference between the current flowing through M1 and M2, discharging nodes P and Q at different speeds. As voltages of the node P and Q reach 'VDD (supply voltage) – Vthn (threshold voltage of NFET)', M3 and M4 is turned on. Then, the nodes X and Y starts to be discharged at different rates. Regeneration phase starts soon after voltage at either X or Y drops to 'VDD-Vthn', turning either M5 or M6 on. By the cross-coupled configuration, the final voltage reaches VDD at either node X or node Y, and the other node becomes zero, depending on the polarity of the differential input signal. The node X is the output of the comparator (COM_OUT).

Ideally, the comparator changes the output when one input level crosses the other input level. However, device mismatches in V_{th} and $\beta(=\mu C_{ox}W/L)$ [16] and transistor noise, such as thermal and flicker noise[17], makes their left and right parts asymmetry and change the output when the two input voltages are slightly different. The device mismatches cause a DC offset voltage to the input of the comparator, and the noise randomly changes the input voltage that changes the comparator output. In Figure 3, M3 – M6 are turned off in the pre-charge phase using S1-S4, reducing their offset contribution [18]. The mismatch between M1 and M2 and their nose are the dominant contributor to the entire offset of the comparator [19]. The mismatch and noise create non-zero differential output current even when the input voltages are the same, which affects the output transition speed and thus the final value of the comparator. Figure 3 show one example that mitigates the input-referred offset by adding additional capacitors to pre-charge node P and Q [15].

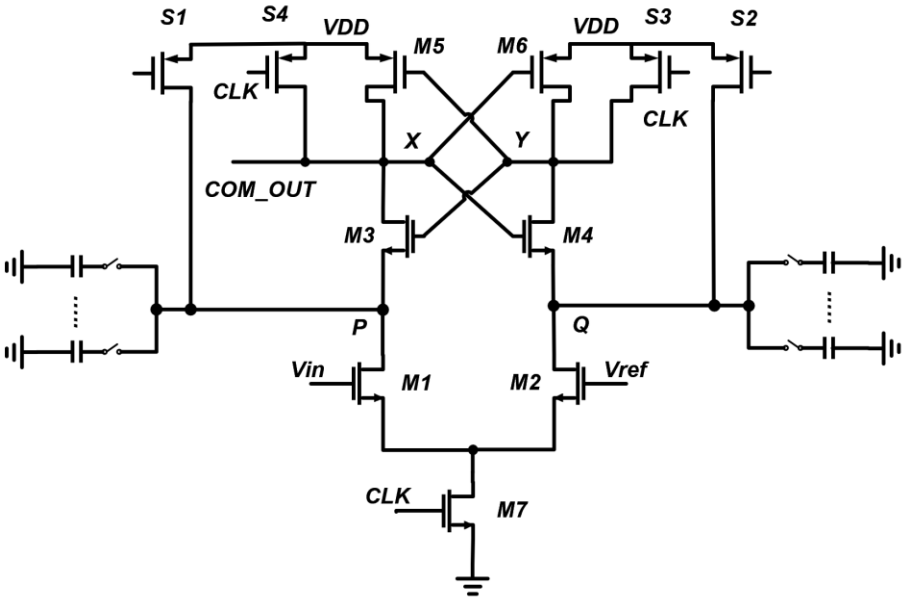

Figure 4. Offset cancellation using programmable capacitors

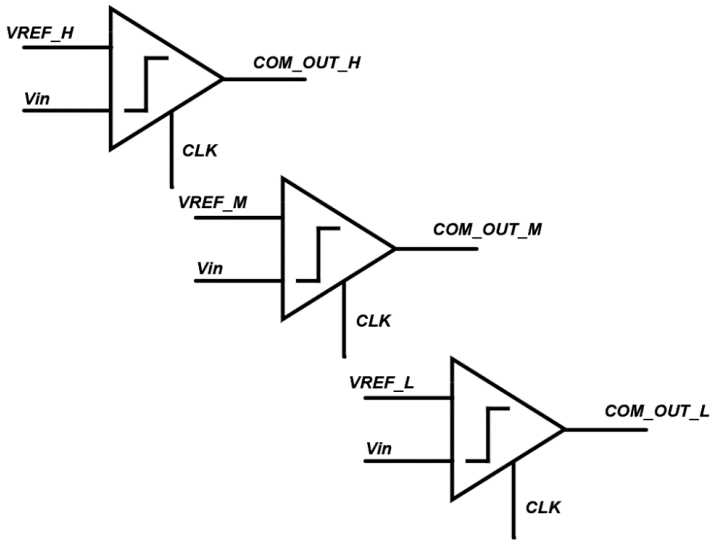

Figure 5. Multi-voltage-level comparators.

To control the pull-up pMOS and pull-down nMOS transistors in Figure 2, the proposed design adds another two comparators with two additional threshold voltages to generate COM_OUT_H and COM_OUT_L, as shown in Figure 5.

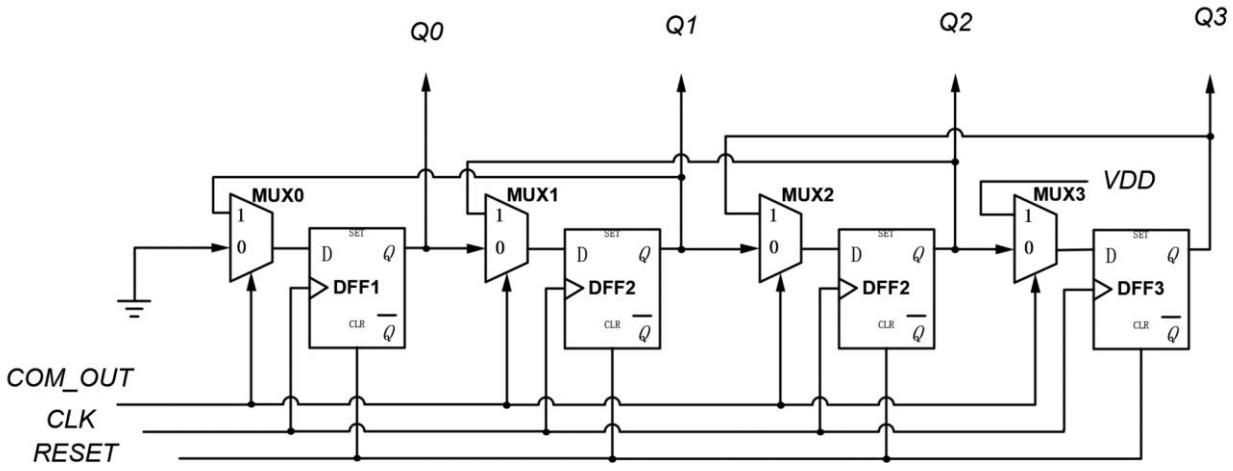

Figure 6. SR in proposed DLDO.

Figure 6 depicts a simplified version of SR with flip-flops and multiplexers [5], implemented in 16 bits in this work. The comparator output (COM_OUT) changes its shifting direction from MSB to LSB. In a reset state (RESET = 1), all the output bits are reset to 0. When 'RESET = 0' & 'COM_OUT = 0', the output bits stay as 0. When 'RESET = 0' and 'COM_OUT = 1', MUX3 sets the output to 1 (D of DFF3). At the next clock edge, MSB (Q3) is set to 1, and DFF3 stores the value for MUX2 for Q2. Hence, as shown in Figure 7, SR performs a left shift operation when COM_OUT = 1 and a right shift operation for the opposite condition.

The propose design selects the number of bits of the SR as 16 accepting output ripple of 5mV, balancing accuracy in steady state and settling time during load transition. A SR with higher number of bits provides smaller output ripple but suffer from slow response, resulting in a longer settling time, based on $T_S = N/f$, where TS is settling time, N is the number of bits of the SR, and *f* is the operating frequency. For example, DLDOs with a 128-bit SR suppresses its output ripple less than 1mV (5mV for one with a 16-bit SR. However, it experiences 8× longer setting time (1.6μs versus 0.2 μs) than the counterpart.

In the proposed design, the maximum load current is set to 2.7mA. VDD is 500mV, and Vout is 450mV. As the power transistors are turned on, their source-drain voltage (V_{SD}) is 50mV, and the source-gate voltage (V_{SG}) is 500mV. The threshold voltage (V_T) of the pMOS power transistor in the process is -384.2mV. Since $V_{SD} \leq V_{SG} - |V_T|$, the pMOS transistor operates in triode region, and the drain current can be expressed as $I_{SD} = \mu_p C_{ox} \frac{W}{L}\{(V_{SG} - |V_T|)V_{SD} - \frac{1}{2}{V_{SD}}^2\}$. Based on this equation, each power transistor is required to have width of 3.39μm for the minimum length of 50nm, to support the target maximum load current (2.7mA) with all the 16 power transistors.

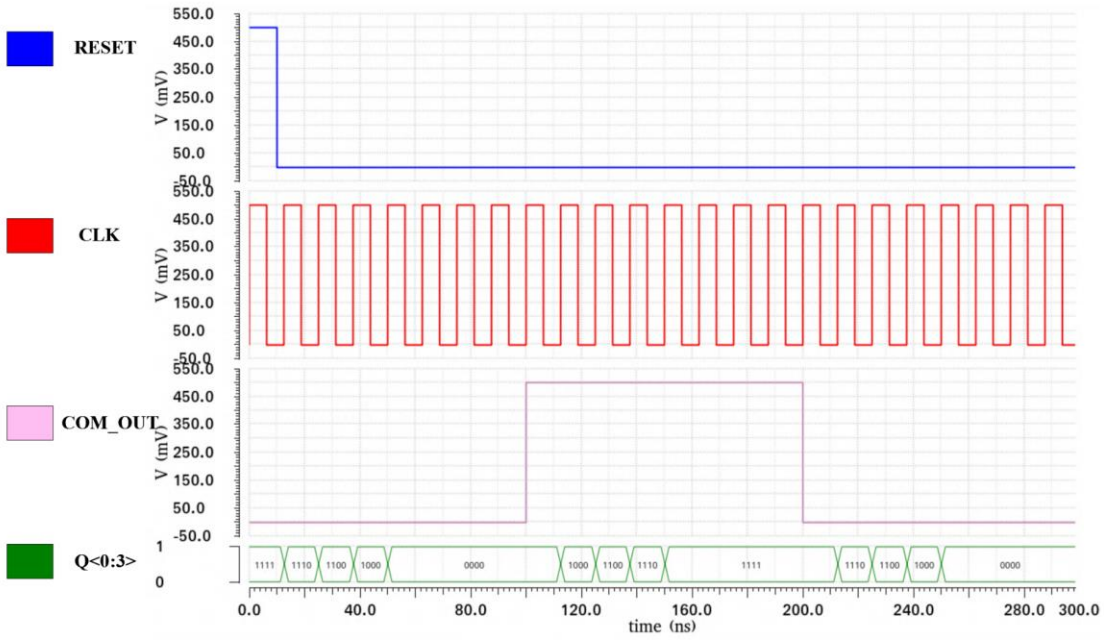

Figure 7. Simulation waveform of 4-bit SR.

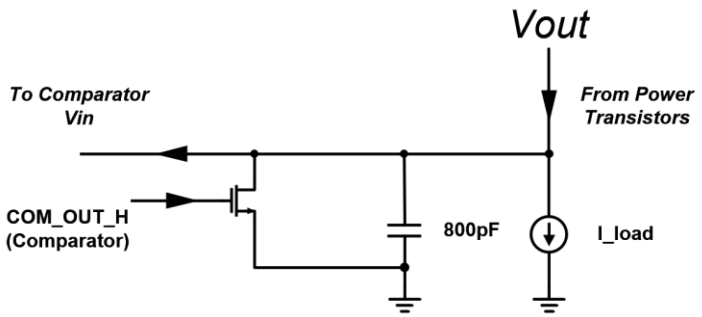

Figure 8. Pull-down nMOS design in proposed DLDO.

An output capacitor reduces voltage droop when load current increases significantly. However, when the load current changes rapidly from heavy to light levels, Vout experiences larger overshoot with the capacitor. It holds Vout much higher than Vref and discharges it slowly, resulting in long settling time. To solve this problem, the proposed DLDO introduce a pull-down nMOS switch in a similar approach proposed in [9]. Figure 8 shows the pull-down nMOS transistor, controlled by COM_OUT_H from a comparator. When Vout exceeds the high threshold voltage (Vref_H in Figure 5), COM_OUT_H becomes 1, and the nMOS switch is turned on, creating a

discharge current path in addition to the small load current. When Vout is lower than Vref_H, the nMOS switch is turned off.

Figure 9 and Table 1 shows simulation results with pull-down nMOS sizes from 1µm to 20µm. The overshoot is the voltage difference between Vref_M and maximum output voltage at the load current drop. The settling time is the period from the beginning of the load current transition to the point when Vout is regulated within 2% error referenced to Vref_M (450mV± 9mV). For the nMOS transistor sizes smaller than 10µm, the overshoot and settling gradually decreases. However, the transistor size larger than 9µm, it becomes too strong and results in unstable operation. For the minimum overshoot and stable operation, the size of the pull-down nMOS transistor is chosen to 9µm.

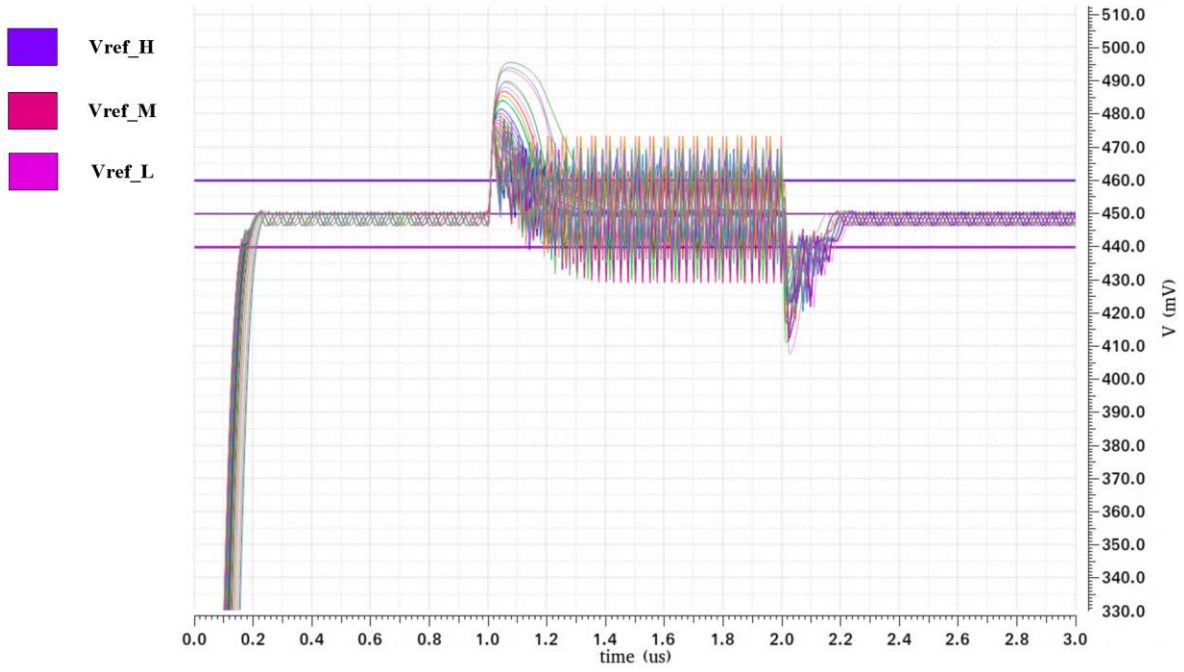

Figure 9. Simulated DLDO with different size of pull-dwon nMOS transistors.

Table 1. Statistics during load drop using different size of pull-down nMOS

nMOS size (um)	Overshoot (mV)	Settling Time (ns) (2%)	Stability (Y/N)
1	45.6	319.5	Y
2	43.3	245.01	Y
3	39.6	199.18	Y
4	36.8	182.45	Y
5	34.1	182.33	Y
6	31.5	171.38	Y
7	29.3	160.66	Y
8	27.3	168.07	Y
9	26.7	159.03	Y
10	25.1	N/A	N
11	28.9	N/A	N
12	28.1	N/A	N
13	26.7	N/A	N
14	26.7	N/A	N
15	26.3	N/A	N
16	28	N/A	N
17	26.8	N/A	N
18	26.5	N/A	N
19	26.7	N/A	N
20	27.8	N/A	N

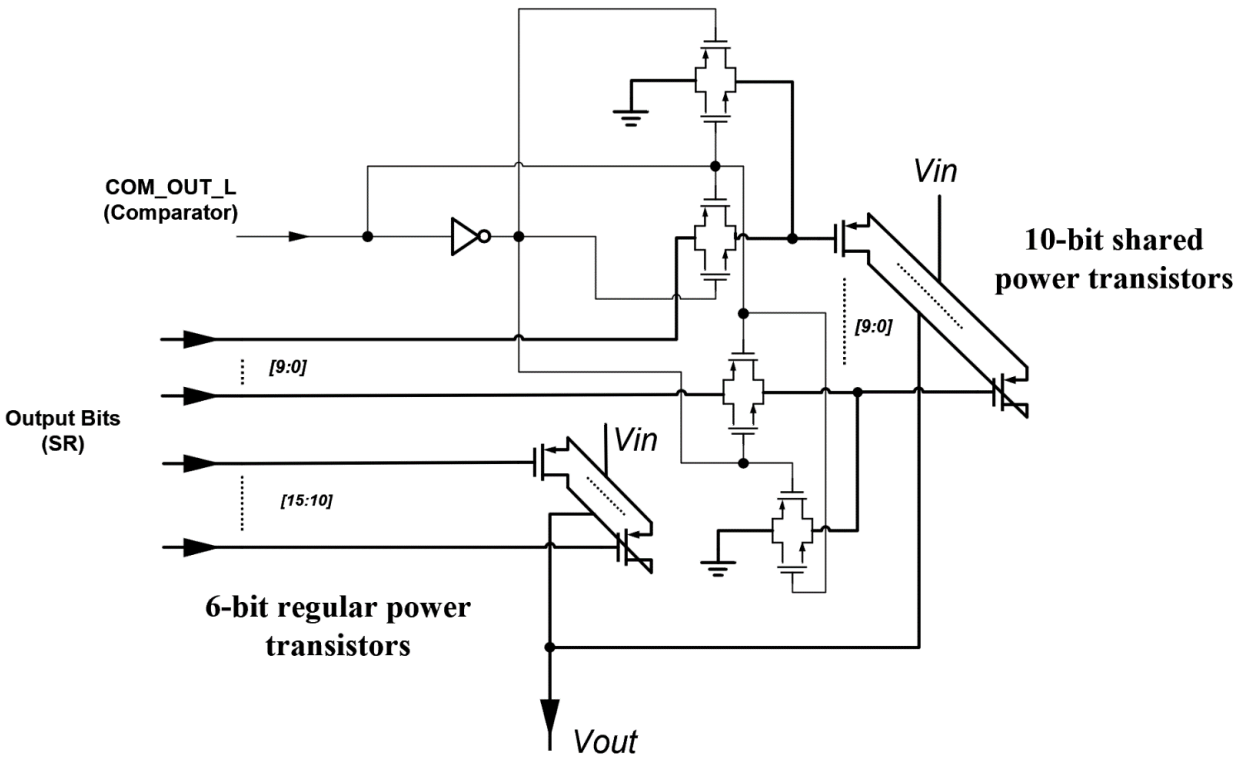

Figure 10. Pull-up pMOS design in proposed DLDO.

As previously mentioned, despite the precise output during the steady state, the conventional SR-DLDO suffers from a large voltage droop during load current increase due to its linearly-shifting characteristic. To solve this issue, some part of the SR output bits is used as pull-up pMOS switches during the event, as shown in Figure 10. It uses 10 bits of the SR output bits, starting from LSB, as pull-up pMOS switches. The gate of each switches is connected to the output of two transmission gates, which takes corresponding SR output bits or ground as inputs. These two transmission gates are controlled by two complementary signals from COM_OUT_L. When Vout < Vref_L (shown in Figure 5), COM_OUT_L is set to 1 and sets the output voltage of the transmission gates to ground, making the 10 pMOS transistors to operate as the pull-up pMOS switches. On the other hand, the transistors operate as normal power transistors. Instead of including separate pMOS transistors for the pull-up switches, the proposed design saves areas by sharing the pMOS transistors both for the power transistors and pull-up switches.

A portion of the power transistors is used as pull-up pMOS transistors when Vout < Vref_L. Table 2 shows simulated Vout when the load current is the maximum (I_max), with different number of the pull-up pMOS transistors, assuming all the power transistors controlled by the SR is turned off. The pull-up pMOS transistors should regulate Vout higher than Vref_L (440mV) but not to create overshoot higher than Vref_M (450mV). The 14 turned-on pull-up transistors generates Vout of 442.53mV higher than Vref_L, satisfying the requirement. The 15 pull-up transistors also meet the requirement, but it provides a smaller margin before SR decreases its output value. Here, all the 16 power transistors are not required for I_max since it targets Vout to be just higher than Vref_L rather than Vref_M at this fast load change. However, after this event, all the 16 power transistors are eventually turned to maintain Vout near Vref_M.

In addition to the pull-up transistors, the number of transistors controlled by SR should be considered since they can be additionally turned on as Vout reach Vref_L from a lower value. They are turned on from MSB to LSB sequentially as shown in Figure 11. Thus, for Vout < Vref_L, the total number of turned-on power transistors is the sum of the number of pull-up pMOS transistors and the number of power transistors turned on by the SR. The turned-on power transistors controlled by the SR can be calculated based on the output settling time and clock speed as T_S/T_{CLK}. For the total number turned-on transistor of 14, only 10 pull-up pMOS transistors are necessary in addition to 4 turned-on power transistors controlled by the SR.

Table 2. Simulated DLDO with different number of turned-on power transistors at load current increase.

Number of turned-on pull-up pMOS transistors without using SR control	Output voltage (mV) after I_load changes from I_min to I_max	Settling time (ns)	Calculated number of turned-on power transistor only by SR control	Required pull-up pMOS transistors considering the power transistors turned on by SR control
1	-1337.2	2410.92	200.91	-199.91
2	-984.74	2200.77	183.3975	-181.3975
3	-652.13	1990.78	165.8983333	-162.8983333
4	-312.45	1567.67	130.6391667	-126.6391667
5	-58.82	1181.51	98.45916667	-93.45916667
6	124	710.25	59.1875	-53.1875
7	254.21	323.98	26.99833333	-19.99833333
8	336.7	123.74	10.31166667	-2.311666667
9	379.76	77.9	6.491666667	2.508333333
10	403.07	50.6	4.216666667	5.783333333
11	417.94	47.98	3.998333333	7.001666667
12	427.37	45.43	3.785833333	8.214166667
13	436.28	40.27	3.355833333	9.644166667
14	442.53	39.28	3.273333333	10.72666667
15	447.61	36.17	3.014166667	11.98583333
16	450.54	35.97	2.9975	13.0025

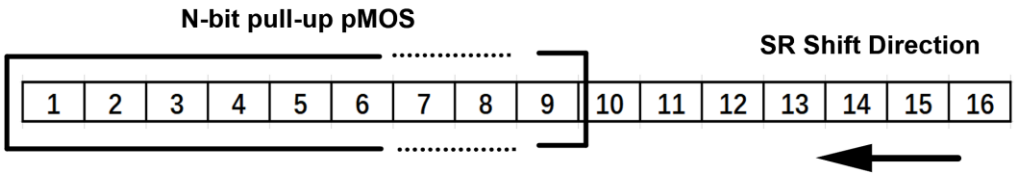

Figure 11. Shared pull-up pMOS at load current increase.

4.0 Simulation Results

The proposed DLDO is designed in a CMOS 45nm process and evaluated in transistor-level simulations. The supply voltage is 500mV, and the output capacitance is 800pF. Figure 12 shows the transient analysis result of the comparator for the proposed DLDO. VOL_IN is the input voltage which increases linearly from 400mV to 600mV. The three horizontal lines from up to down are Vref_H (460mV), Vref (450mV), and Vref_L (440mV). The three vertical lines from left to right are COM_OUT_L, COM_OUT_M, and COM_OUT_H. At the point where VOL_IN intersects COM_OUT, COM_OUT flips its value. The comparator shows only maximum error of 28µV and the maximum delay of 632ps at a clock frequency of 80MHz, providing precise comparison for the proposed DLDO.

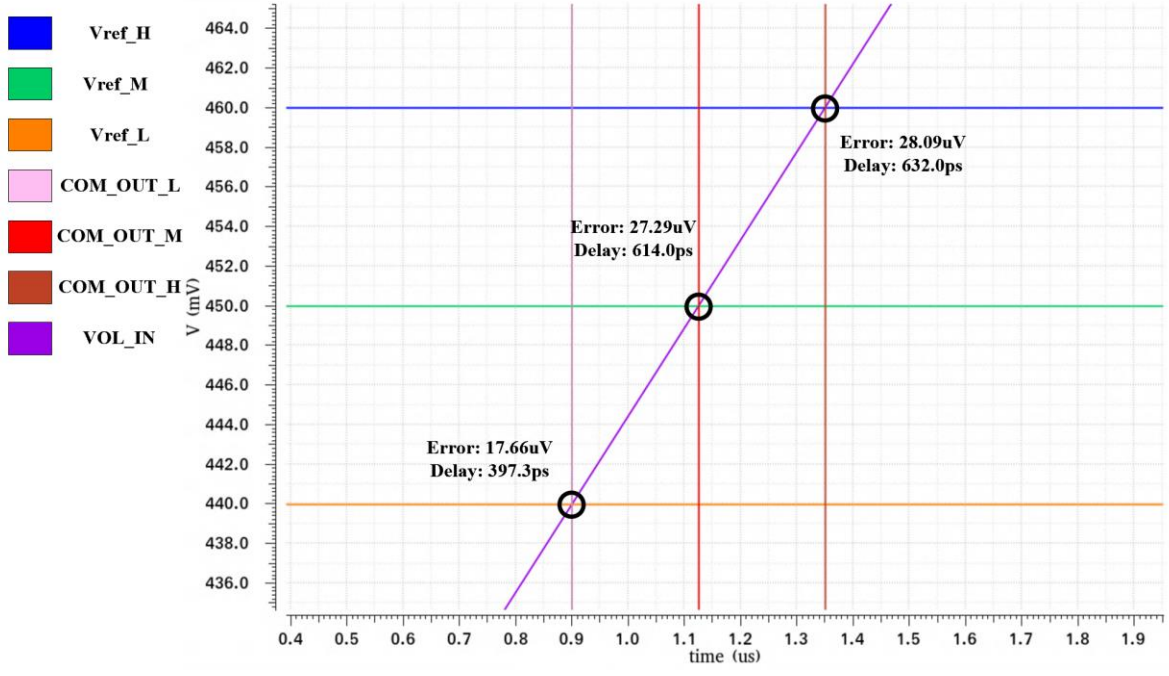

Figure 12. Simulation result of the comparator in proposed DLDO.

Figure 13 shows a DC simulation result of the power transistors. Each power transistors have length of 50nm and width of 3.39µm. It shows that the 16 power transistors can support 2.7mA with V_{SG} = 500mV & V_{DS} = 50mV when they are all turned on.

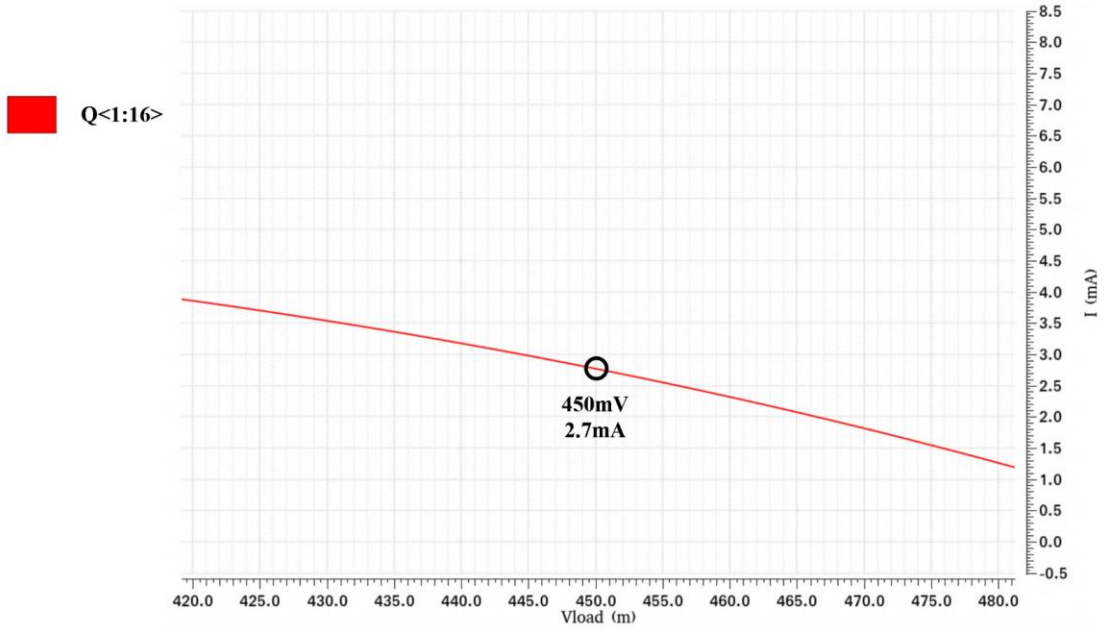

Figure 13. Simulation result of the power transistors for SR.

Figure 14 shows the transient simulation result of the proposed DLDO with pull-up pMOS and pull-down nMOS transistors. The input supply voltage of the DLDO is 500mV. The reference voltage Vref_L, Vref, and Vref_H are 440mV, 450mV, and 460mV, respectively. The clock speed is 80MHz. A current source is used to simulate the load change. In the beginning, the load current is set to 2.7mA (the maximum load current). At 1µs, the load current is dropped from 2.7mA to 20µA (the minimum load current) in 10ns. At 2µs, the load current is increased back to 2.7mA in 10ns.

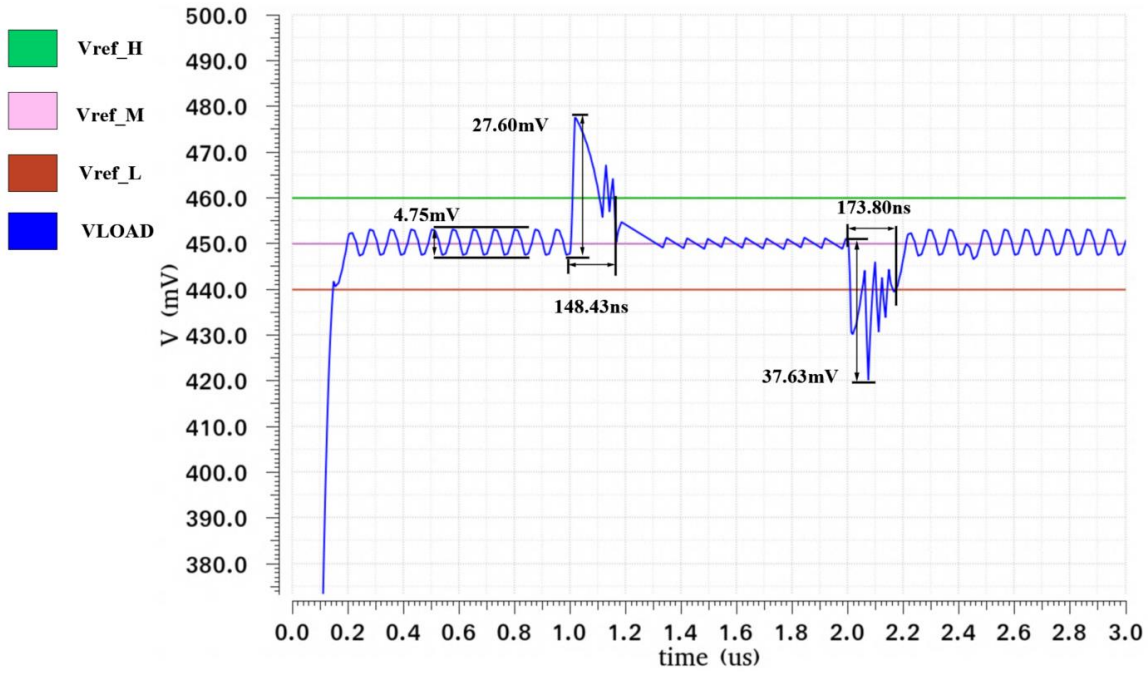

Figure 14. Transient analysis result of proposed DLDO with pull-up pMOS and pull-down nMOS.

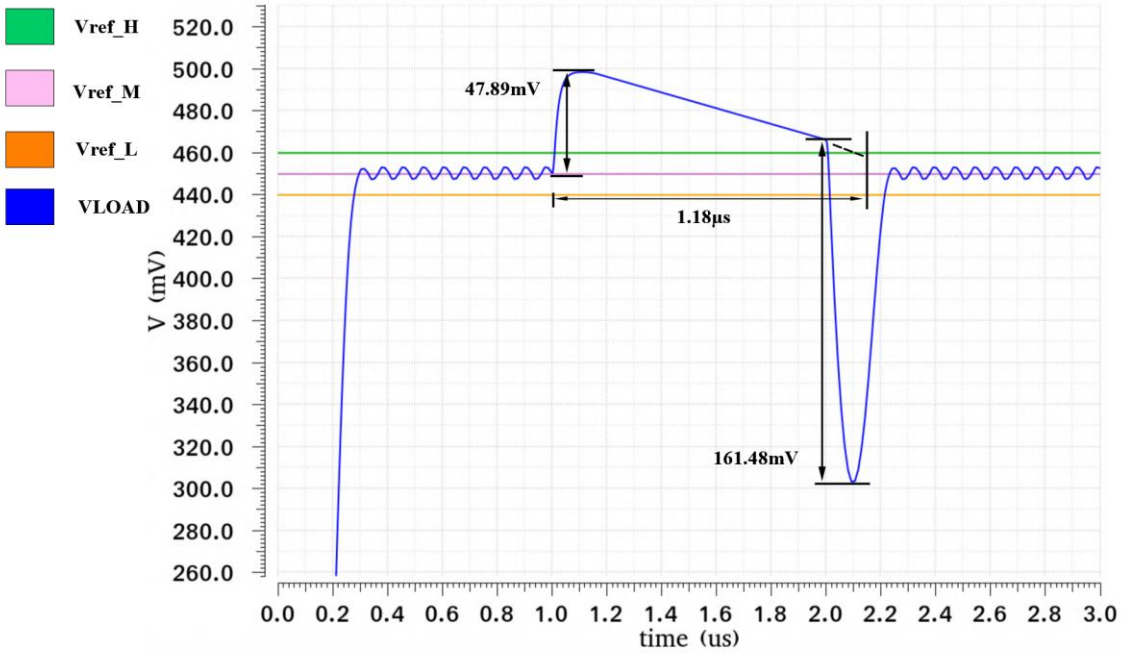

Figure 15. Transient analysis result of proposed DLDO without pull-up pMOS and pull-down nMOS.

The maximum output ripple is 4.75mV during the steady state while showing a 27.6mV overshoot at 1μs at a dynamic load event. As Vout exceeds Vref_H, the pull-down nMOS transistors are turned on, create a discharge path for the output capacitor, and immediately regulate the output voltage back to Vref_M. At 2μs, it achieves output voltage drop of 37.63mV, where the pull-up pMOS transistors are turned on when the output voltage is lower than Vref_L. Oscillation occurs at the load transient condition mainly because the pull-up pMOS transistors are turned off right after Vout becomes higher than Vref_L. At this point, driving strength of the linearly-increased output bits of the SR (number of turned-on power transistors) does not match with the load current. After this oscillation period, Vout is stabilized to the final value when the turned-on power transistors and provides drive strength matched to the load current.

For comparison, Figure 15 shows the simulated DLDO without pull-up pMOS and pull-down nMOS transistors. Compared with the DLDO with the pull-up and pull-down transistors, it shows 73% larger overshoot of 47.89mV by discharging the output capacitor slowly. Also, it shows 330% larger undershoot of 161.48mV from slow response of the SR.

Table 3 compares the proposed DLDO with pull-up pMOS and pull-down nMOS transistors to one without them. The figure of merit (FOM) indicates the performance of DLDOs that takes both quiescent current and response time into account [20]. The DLDO with the transistors achieves a 42% smaller overshoot than the one without the transistors at the load current drop. Also, the settling time is reduced by 87% with a help of the pull-down nMOS transistor (1.18μs without the pull-down transistor and 148.43ns with it). At the load current increase, the voltage droop is reduced by 77% with a help of the pull-up pMOS transistors. From these advantages, the DLDO with the transistors achieves 77% better FOM, compared with one without the transistors.

Table 3. Comparison of the proposed DLDO with and without pull-up and pull-down switch.

	w/o pull-up and pull-down switch	w/ pull-up and pull-down switch
Process	45nm	45nm
Load Range [I_load_max/I_load_min]	24μA~2.7mA (113x)	24μA~2.7mA (113x)
Vin[V]	0.5	0.5
Vout[V]	0.45	0.45
IQ.MIN [A]	1.20E-05	1.20E-05
COUT [F]	8.00E-10	8.00E-10
ΔVOUT [V]	1.61E-01	3.76E-02
△ I_Load [A]	2.47E-03	2.47E-03
Ts @ I_load_max to I_load_min [ns]	1180	148.43
Ts @ I_load_min to I_load_max [ns]	204.02	173.80
FOM*	2.55E-10	5.94E-11
FOM(ps)	254.5184612	59.36027799
* FoM = COUT · (ΔVOUT / △ I_Load) · (IQ /△ I_Load); The smaller is better		

To analyze how the offset voltage from comparator affects the performance of the proposed DLDO, a constant voltage source of ±5V is applied to the input of the comparator as examples to emulate the offset as well as the noise at decision time. Figure 16 shows an example of +5mV offset voltage added to the comparator for VREF_H.

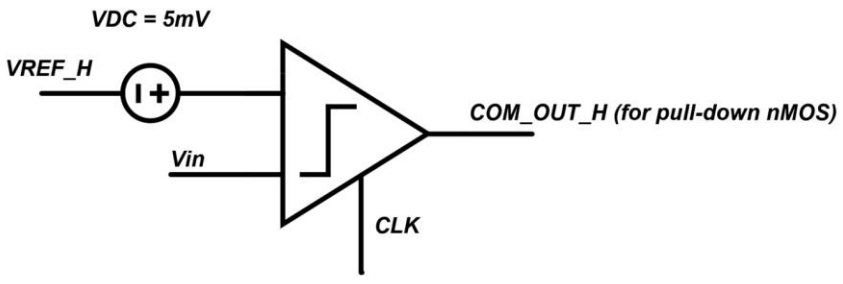

Figure 16. 5mV offset voltage added to the comparator for VREF_H.

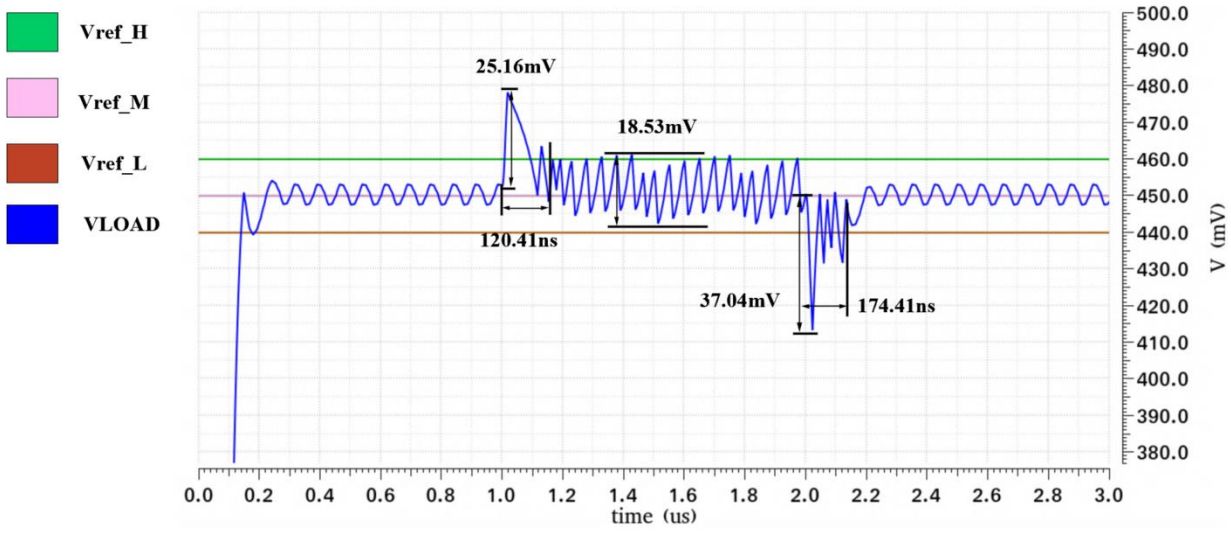

Figure 17. Transient analysis result of proposed DLDO with -5mV offset at Vref_H.

Figure 17 shows the transient simulation result of the proposed DLDO with -5mV offset voltage at Vref_H. Due to the -5mV offset, the reference voltage of the comparator for pull-down nMOS transistor is Vref_H − 5mV. The overshoot and undershoot is changed by -8% and -1%, respectively. The settling times are changed by -19% and 0.35% at the overshoot and undershoot events, respectively. Also, the 338% larger maximum ripple is observed between the overshoot and undershoot. The -5mV offset voltage draws Vref_H closer to Vref_M. Thus, the pull-down nMOS transistor is turned on earlier than the DLDO without offset voltage when the load current drops from maximum to minimum value. As a result, the overshoot and settling time at DLDO with -5mV offset at Vref_H are smaller than the one without offset. However, the pull-down nMOS transistor is too strong when its reference voltage is closer to Vref_M, resulting in oscillations with large output ripple after the load transient at 1µs. The undershoot and its settling time do not change significantly since the offset at Vref_H does not affect Vref_L.

Figure 18 demonstrates the simulation result with +5mV offset at Vref_H. The reference voltage of the comparator for pull-down nMOS becomes $\mathrm{Vref\_H} + 5\mathrm{mV}$. The overshoot and undershoot is changed by 12% and -0.02%, respectively. The settling times are changed by 24% and -0.07% at the overshoot and undershoot events, respectively. Also, the maximum ripple is changed by -2% before the overshoot, respectively. With +5mV offset at Vref_H, the voltage difference between Vref_H and Vref_M is larger. Hence, the pull-down nMOS transistor is turned on later than the DLDO without offset voltage, resulting in large overshoot and long settling time. There are no significant changes at undershoot and its settling time since the offset at Vref_H does not affect Vref_M and Vref_L.

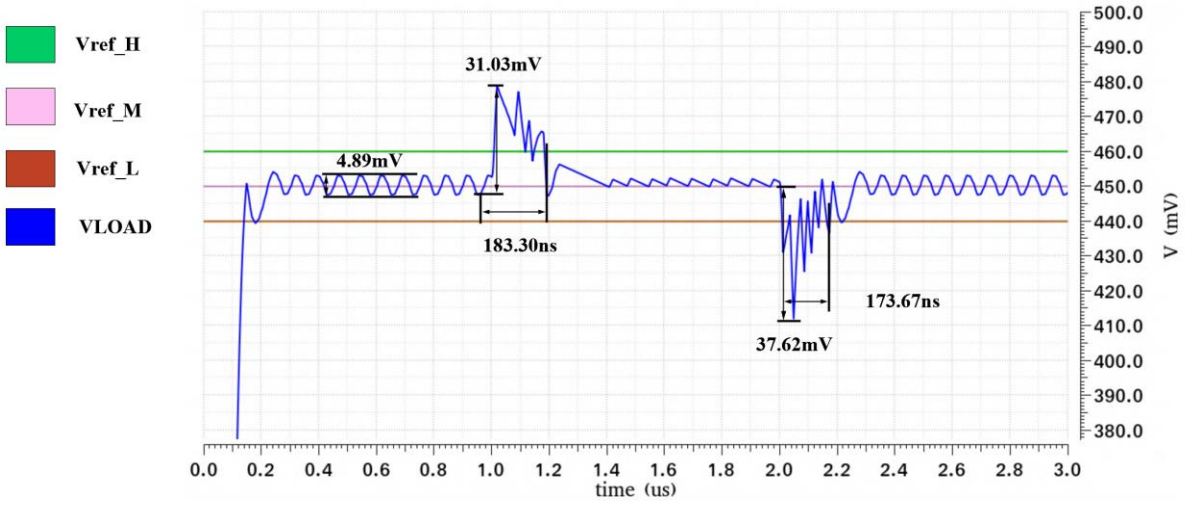

Figure 18. Transient analysis result of proposed DLDO with +5mV offset at Vref_H.

Figure 19 depicts the simulated result of proposed DLDO with -5mV offset at Vref_M. The -5mV offset changes the reference voltage of the comparator for SR to '$\mathrm{Vref\_M} - 5\mathrm{mV}$'. The overshoot and undershoot is changed by 5% and -26%, respectively. The settling times are changed by -6% and -30% at the overshoot and undershoot events, respectively. Also, the 246% larger maximum ripple is observed after the undershoot. The -5mV offset at Vref_M regulates VLOAD

around 445mV, which is closer to Vref_L. Thus, when the load current increases from minimum to maximum value, the pull-up pMOS transistors is turned on earlier compared with the DLDO without offset, resulting in a smaller undershoot and shorter settling time. However, similar to the problem in Figure 17, the pull-up pMOS transistors are too strong for 445mV VLOAD, which creates large output ripple after the load transient at 2µs.

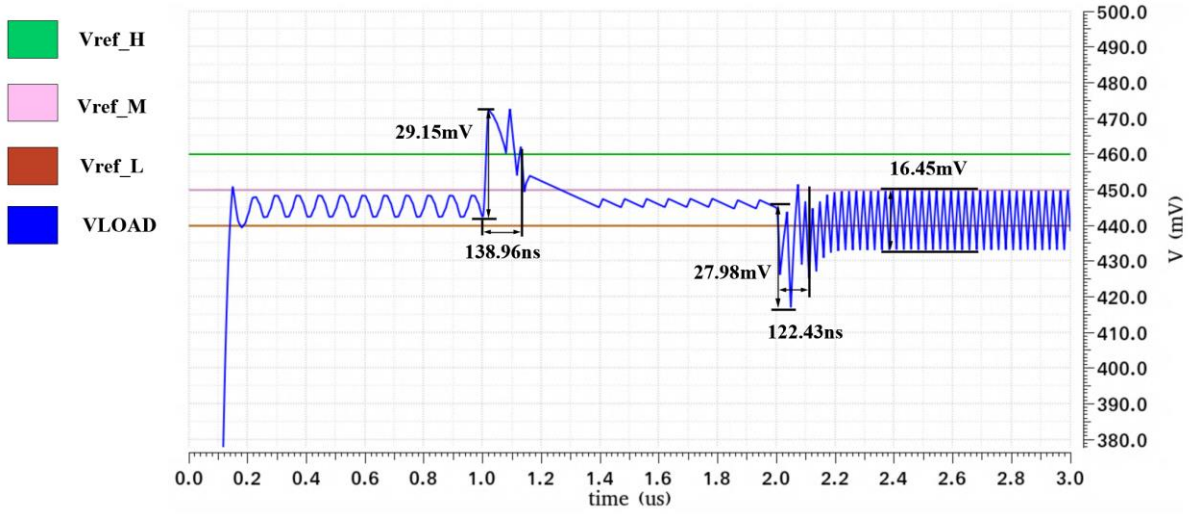

Figure 19. Transient analysis result of proposed DLDO with -5mV offset at Vref_M.

Figure 20 shows the transient analysis of DLDO with +5mV offset on Vref_M. Due to the +5 offset, the reference voltage of the comparator for SR becomes $\mathrm{Vref\_M} + 5\mathrm{mV}$. The overshoot and undershoot is changed by 2% and 10%, respectively. The settling times are changed by 40% and -14% at the overshoot and undershoot events, respectively. Also, the 214% larger maximum ripple is observed between the overshoot and undershoot. With +5mV offset at Vref_M, VLOAD is regulated around 455mV, which is too close to Vref_H. It results in a larger overshoot and longer settling time since the pull-down nMOS transistor is too weak with higher VLOAD. Also, the smaller voltage difference between VREF_H and VREF_M with higher VLOAD makes the comparators for SR and pull-down nMOS transistor flip more frequently, creating large output

ripple after the load transient at 1µs. With higher VLOAD, the SR also turns on more power transistors between 1µs and 2µs. Despite the larger undershoot due to the larger voltage difference between VLOAD and Vref_L, the settling time of load transient at 2µs becomes smaller.

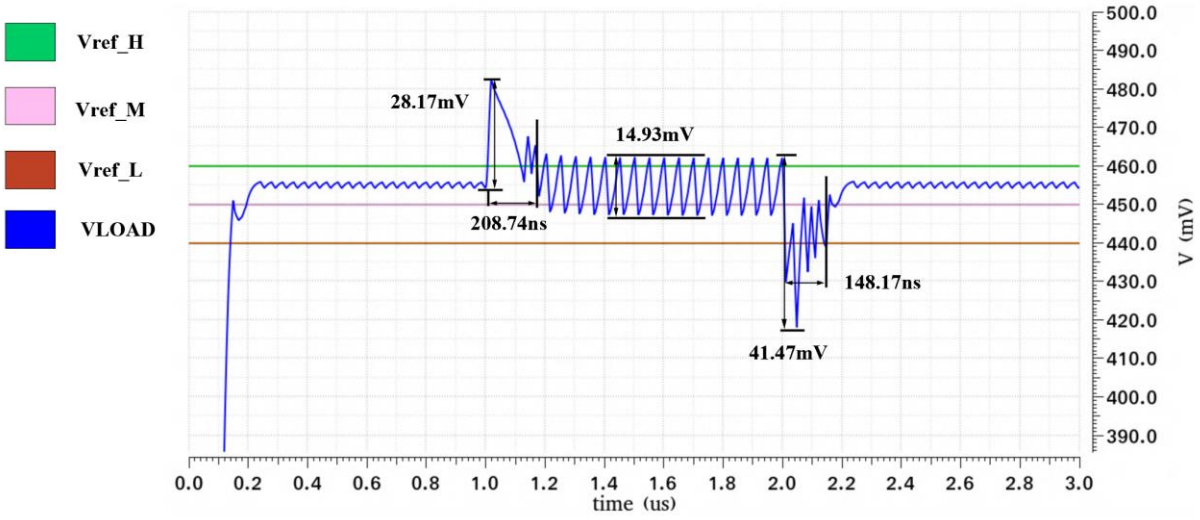

Figure 20. Transient analysis result of proposed DLDO with +5mV offset at Vref_M.

Figure 21 demonstrates the simulation result with -5mV offset at Vref_L. The reference voltage of the comparator for shared pull-up pMOS transistors becomes $\mathrm{Vref\_L} - 5\mathrm{mV}$. The overshoot and undershoot is changed by 1% and 30%, respectively. The settling times are changed by -2% and 4% at the overshoot and undershoot events, respectively. Also, the 38% larger maximum ripple is observed after the undershoot. With -5mV offset at Vref_L, the pull-up pMOS transistors is turned on later than the DLDO without offset when the load current increases from minimum to maximum value. This results in a larger undershoot and longer settling time. With the longer settling time, the SR turns on more power transistors (1 or 2 more bits) so at 2.2µs there is a small overshoot, creating larger output ripple. The offset at Vref_L does not affect the overshoot and settling time of the load transient at 1µs.

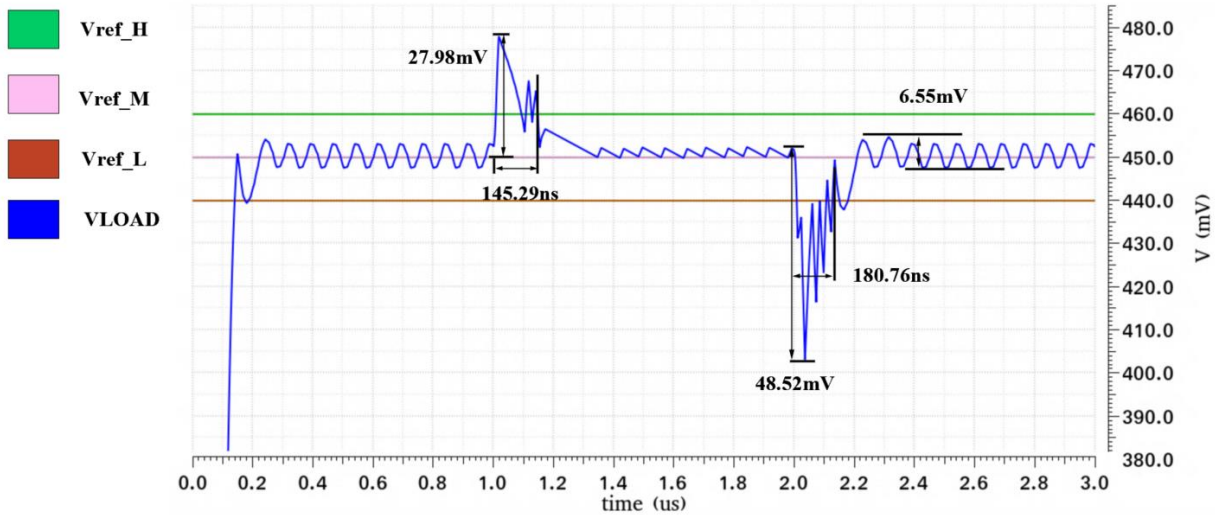

Figure 21. Transient analysis result of proposed DLDO with -5mV offset at Vref_L.

As shown in Figure 22, with +5mV offset at Vref_L, the reference voltage of the comparator for shared pull-up pMOS transistors becomes $\mathrm{Vref\_L} + 5\mathrm{mV}$. The overshoot and undershoot is changed by 0.69% and 17%, respectively. The settling times are changed by 5% and -15% at the overshoot and undershoot events, respectively. Also, the maximum ripple is change by 55% before the overshoot, respectively. The higher Vref_L due to the offset does not affect the overshoot and settling time of the load transient at 1µs. The pull-up pMOS transistors are turned on earlier than the DLDO without offset. Thus, the undershoot and settling time when the load current increases from minimum to maximum is smaller. However, the pull-up pMOS is too strong with +5mV offset at Vref_L, creating small oscillations after entering the steady state. Hence, the maximum output ripple becomes larger.

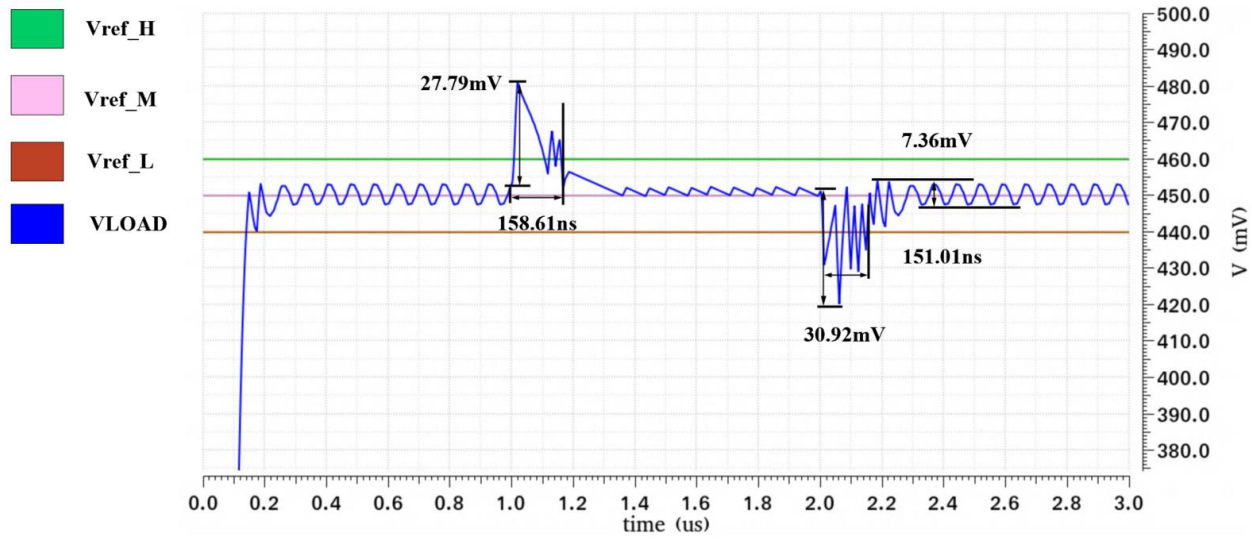

Figure 22. Transient analysis result of proposed DLDO with +5mV offset at Vref_L.

Table 4. Comparison of proposed DLDO with different offset voltages

	w/o offset	-5mV Offset @ Vref_H	+5mV Offset @ Vref_H	-5mV Offset @ Vref_M	+5mV Offset @ Vref_M	-5mV Offset @ Vref_L	+5mV Offset @ Vref_L
IQ.MIN [A]	1.20E-05	1.22E-05	1.21E-05	1.21E-05	9.12E-06	1.21E-05	1.21E-05
COUT [F]	8.00E-10	8.00E-10	8.00E-10	8.00E-10	8.00E-10	8.00E-10	8.00E-10
Undershoot [V]	3.76E-02	3.70E-02	3.76E-02	2.80E-02	4.15E-02	4.85E-02	3.09E-02
Overshoot [V]	2.76E-02	2.52E-02	3.10E-02	2.92E-02	2.82E-02	2.80E-02	2.78E-02
△ I_Load [A]	2.47E-03	2.47E-03	2.47E-03	2.47E-03	2.47E-03	2.47E-03	2.47E-03
Ts @ I_load_max to I_load_min [ns]	148.43	120.41	183.3	138.96	208.74	145.29	158.61
Ts @ I_load_min to I_load_max [ns]	173.8	174.41	173.67	122.43	148.17	180.76	151.01
Maximum output ripple [mV]	4.75	18.53	4.89	16.45	14.93	6.55	7.36
FOM*	5.94E-11	5.91E-11	5.99E-11	4.43E-11	4.96E-11	7.70E-11	4.92E-11
FOM(ps)	59.36	59.11	59.89	44.32	49.59	77.05	49.18
* FoM = COUT · (Undershoot / △ I_Load) · (IQ /△ I_Load); The smaller is better							

Table 4 compares the proposed DLDO with different offset voltages based on the simulation results shown from Figure 17 to Figure 22. Considering ±5mV, the overshoot, undershoot, and maximum output ripple are degraded by 5%, 30%, and 290% as the worst case, respectively. The FOMs is maintained in the most cases, but it is degraded by 30% when -5mV offset voltage is applied to Vref_L since the undershoot for FOM calculation becomes larger. If the degraded performance is not acceptable for the target application, the offset should be

suppressed by using the offset cancellation technique in Fig. 4 or increasing device size, especially the input transistors, to suppress their device mismatches and noise. However, this comes with higher power consumption or response time increase.

5.0 Scaling Effect on Proposed DLDO

The proposed DLDO is designed in CMOS 45nm process technology. Figure 23 [21] shows the trend of transistor supply voltage (VDD) and threshold voltage (Vth) with the improvement of process technology. Both VDD and Vth decrease as technology generation advances, but VDD decreases at a faster rate compared with Vth. Hence, the overdrive voltage (VDD – Vth) becomes smaller.

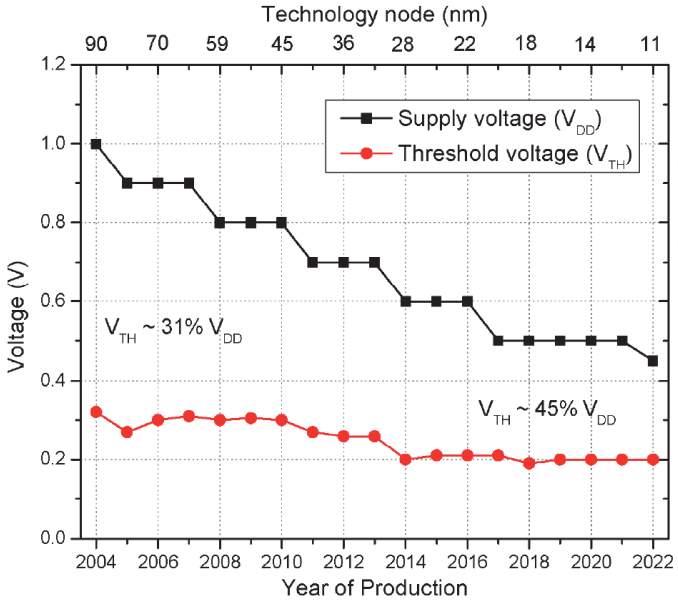

Figure 23. Trend of supply voltage and threshold voltage in process scaling [21].

Figure 24 shows how the scaling changes the load current and number of output bits in the proposed DLDO. Assuming Vin = VDD, the overdrive voltage of the power pMOS transistors becomes smaller as the process scales down. The supply voltage of the load circuit (Vout) can be reduced by the amount of Vth reduction while maintaining the overdrive voltage of transistors in the load circuit. However, Vin decreases more than Vout, V_{SD} of the pMOS power transistors

become smaller. This reduces the drain current of the power transistors. If the load current is reduced by smaller parasitic capacitance in an advanced process, the power transistors can be large enough to support the load circuit so that the original aspect ratio (W/L) can be maintained or reduced. Otherwise, the width or the number of power transistors should be increased. In a similar way, the size of pull-down nMOS transistor should be adjusted as shown in Figure 25.

In a scaled process, the transistors of the comparator become weaker due to lower overdrive voltage, but the reduced internal parasitic and load capacitance can compensate it, or the width of transistors should be increased additionally. Typically, the performance of SR is not a limiting factor in the DLDO, so its design does not need to be updated.

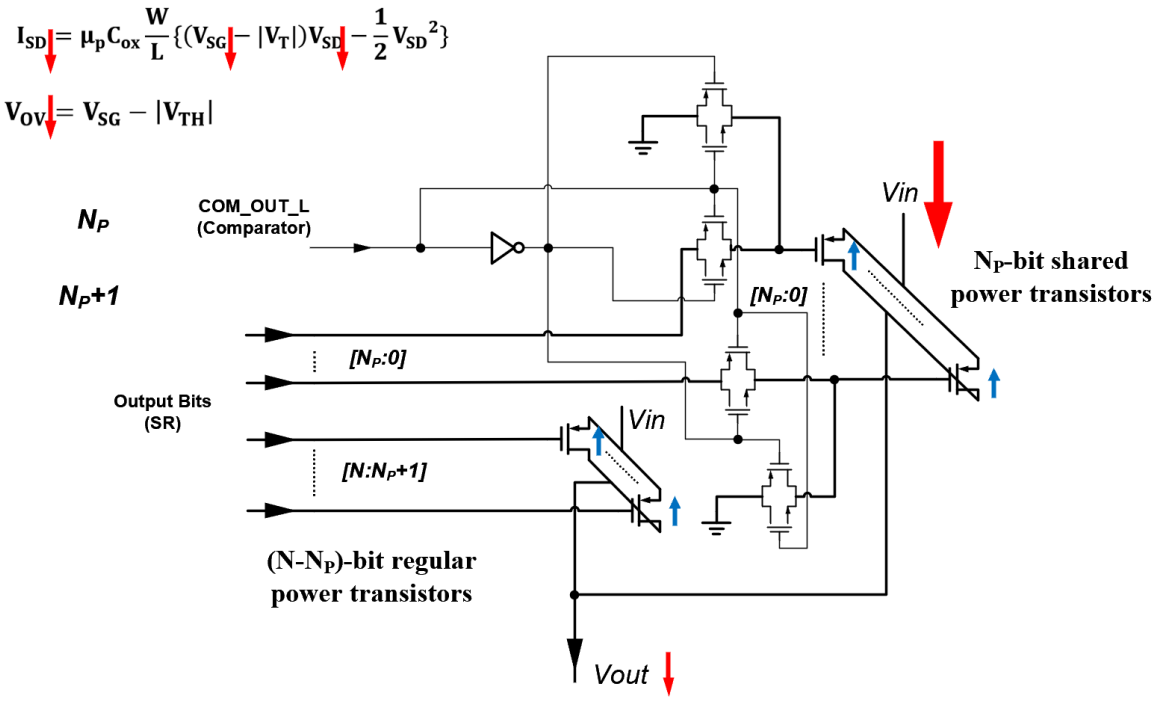

Figure 24. Trend of the output bits in proposed DLDO with process scaling.

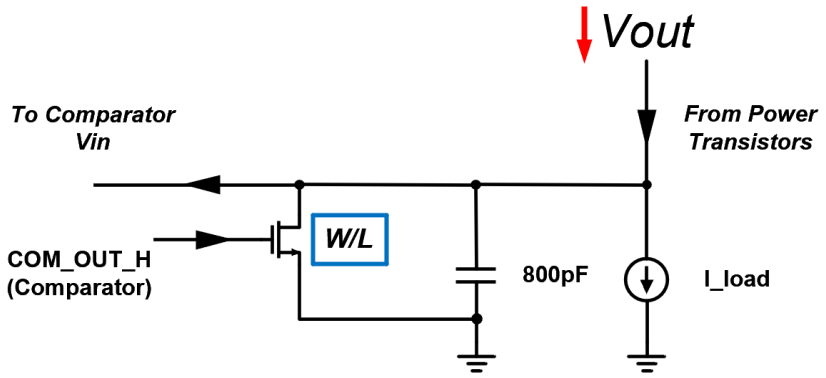

Figure 25. Trend of pull-down nMOS in proposed DLDO with process scaling.

Figure 26 shows how the comparator design should be updated in an advanced process. In the pre-charge phase (CLK = 0), the driving strength of S1 – S4 becomes weaker due to limited overdrive voltage. However, the speed performance of the comparator is mainly limited by the delay from when CLK rises to when either X or Y is decreased so that S1 – S4 do not need to be adjusted from the minimum size. In the evaluation phase (CLK = 1), the reduced overdrive voltage reduces the driving strength of M3, M4, and M7, which can be the main bottleneck of the delay of the comparator. It results in increasing transient response of the DLDO and thus higher overshoot and undershoot. Thus, the aspect ratio of the transistors should be increased to meet the delay requirement in the advanced process.

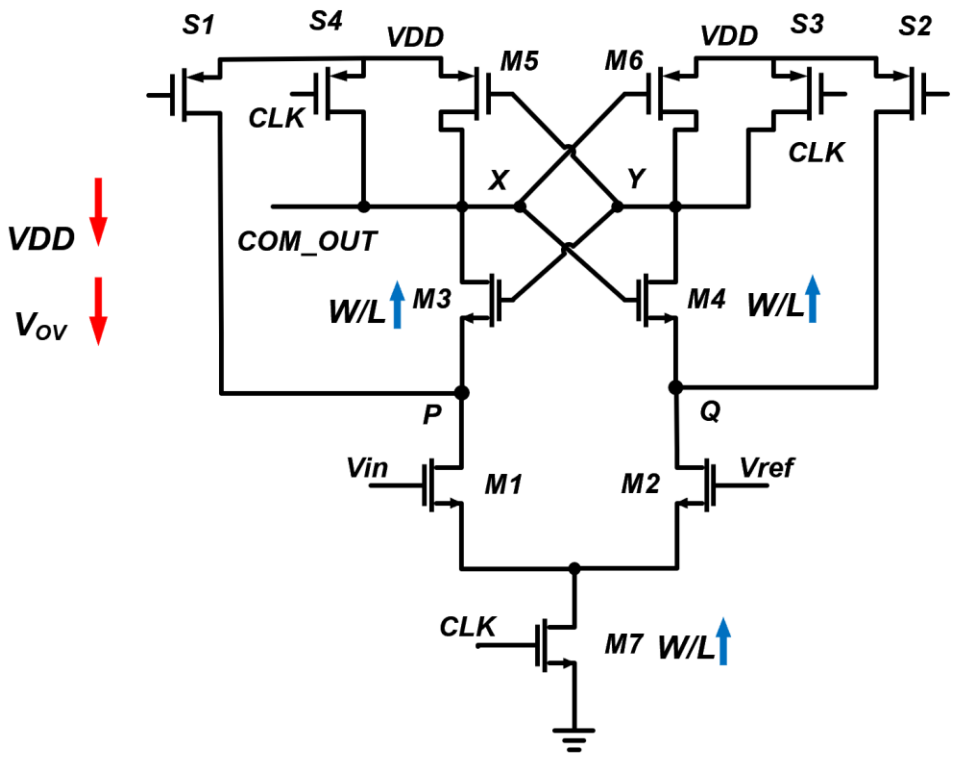

Figure 26. Trend of comparator in proposed DLDO with process scaling.

6.0 Conclusion

This paper investigated circuit design of a fully-integrated SR-based DLDO with pull-up pMOS and pull-down nMOS transistors. With optimal pull-up and pull-down device size, the proposed design improves overshoot, undershoot, and setting time by 42%, 77%, and 87%, respectively, compared with one without the transistors. It compensates the main disadvantages of the SR-based DLDO at the cost of additional simple circuits.

Bibliography

[1] Z. Toprak-Deniz *et al.*, "Distributed system of digitally controlled microregulators enabling per-core DVFS for the POWER8TM microprocessor," *Dig. Tech. Pap. - IEEE Int. Solid-State Circuits Conf.*, vol. 57, pp. 98–99, 2014, doi: 10.1109/ISSCC.2014.6757354.

[2] D. Kim, S. Kim, H. Ham, J. Kim, M. Seok, and S. K. Hynix, "0 . 5V-V IN , 165-mA / mm 2 Fully-Integrated Digital LDO based on Event-Driven Self-Triggering Control," *2018 IEEE Symp. VLSI Circuits*, no. Table I, pp. 109–110, 2018.

[3] F. Yang and P. K. T. Mok, "A 0.6-1V input capacitor-less asynchronous digital LDO with fast transient response achieving 9.5b over 500mA loading range in 65-nm CMOS," *Eur. Solid-State Circuits Conf.*, vol. 2015-Octob, pp. 180–183, 2015, doi: 10.1109/ESSCIRC.2015.7313858.

[4] Y. Lu, F. Chen, and P. K. T. Mok, "A Single-Controller-Four-Output Analog-Assisted Digital LDO with Adaptive-Time-Multiplexing Control in 65-nm CMOS," *ESSCIRC 2019 - IEEE 45th Eur. Solid State Circuits Conf.*, pp. 289–292, 2019, doi: 10.1109/ESSCIRC.2019.8902511.

[5] Y. Okuma *et al.*, "0.5-V input digital LDO with 98.7% current efficiency and 2.7-μA quiescent current in 65nm CMOS," *Proc. Cust. Integr. Circuits Conf.*, pp. 98–101, 2010, doi: 10.1109/CICC.2010.5617586.

[6] S. Bin Nasir, S. Gangopadhyay, and A. Raychowdhury, "A 0.13μm fully digital low-dropout regulator with adaptive control and reduced dynamic stability for ultra-wide dynamic range," *Dig. Tech. Pap. - IEEE Int. Solid-State Circuits Conf.*, vol. 58, pp. 98–99, 2015, doi: 10.1109/ISSCC.2015.7062944.

[7] M. Huang, Y. Lu, U. Seng-Pan, and R. P. Martins, "An output-capacitor-free analog-assisted digital low-dropout regulator with tri-loop control," *Dig. Tech. Pap. - IEEE Int. Solid-State Circuits Conf.*, vol. 60, pp. 342–343, 2017, doi: 10.1109/ISSCC.2017.7870401.

[8] Y. J. Lee *et al.*, "A 200-mA Digital Low Drop-Out Regulator With Coarse-Fine Dual Loop in Mobile Application Processor," *IEEE J. Solid-State Circuits*, vol. 52, no. 1, pp. 64–76, 2017, doi: 10.1109/JSSC.2016.2614308.

[9] S. Li and B. H. Calhoun, "A 745pA Hybrid Asynchronous Binary-Searching and Synchronous Linear-Searching Digital LDO with 3.8×105 Dynamic Load Range, 99.99% Current Efficiency, and 2mV Output Voltage Ripple," *2019 IEEE Int. Solid- State Circuits Conf. -*, pp. 232–234, 2019.

[10] L. G. Salem, J. Warchall, and P. P. Mercier, “ISSCC 2017 / SESSION 20 / DIGITAL VOLTAGE REGULATORS AND LOW-POWER TECHNIQUES / 20 . 3 A 100nA-to-2mA Successive-Approximation Digital LDO with PD Compensation and Sub-LSB Duty Control,” pp. 340–342, 2017.

[11] D. Kim and M. Seok, “Fully integrated low-drop-out regulator based on event-driven PI control,” *Dig. Tech. Pap. - IEEE Int. Solid-State Circuits Conf.*, vol. 59, pp. 148–149, 2016, doi: 10.1109/ISSCC.2016.7417950.

[12] J. Tang, C. Zhan, G. Wang, and Y. Liu, “A 0.7V Fully-on-Chip Pseudo-Digital LDO Regulator with 6.3μA Quiescent Current and 100mV Dropout Voltage in 0.18-μm CMOS,” *ESSCIRC 2018 - IEEE 44th Eur. Solid State Circuits Conf.*, vol. 2, pp. 306–309, 2018, doi: 10.1109/ESSCIRC.2018.8494307.

[13] R. Sangeetha, A. Vidhyashri, M. Reena, R. B. Sudharshan, S. Govindan, and J. Ajayan, “An Overview of Dynamic CMOS Comparators,” *2019 5th Int. Conf. Adv. Comput. Commun. Syst. ICACCS 2019*, pp. 1001–1004, 2019, doi: 10.1109/ICACCS.2019.8728470.

[14] L. G. Salem and P. P. Mercier, “A Sub-1.55mV-Accuracy 36.9ps-FOM Digital-Low-Dropout Regulator Employing Switched-Capacitor Resistance,” *2018 IEEE Int. Solid-State Circuits Conf.*, pp. 304–306, 2018.

[15] B. Razavi, “The StrongARM latch [A Circuit for All Seasons],” *IEEE Solid-State Circuits Mag.*, vol. 7, no. 2, pp. 12–17, 2015, doi: 10.1109/MSSC.2015.2418155.

[16] A. Almansouri, A. Alturki, A. Alshehri, T. Al-Attar, and H. Fariborzi, “Improved StrongARM latch comparator: Design, analysis and performance evaluation,” *PRIME 2017 - 13th Conf. PhD Res. Microelectron. Electron. Proc.*, pp. 89–92, 2017, doi: 10.1109/PRIME.2017.7974114.

[17] B. Razavi, *Design of Analog CMOS Integrated Circuits*. 2005.

[18] G. Campardo, R. Micheloni, and D. Novosel, *VLSI-Design of Non-Volatile Memories*. Springer Berlin Heidelberg, 2005.

[19] H. Xu and A. A. Abidi, “Analysis and Design of Regenerative Comparators for Low Offset and Noise,” *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 66, no. 8, pp. 2817–2830, 2019, doi: 10.1109/TCSI.2019.2909032.

[20] P. Hazucha *et al.*, “A linear regulator with fast digital control for biasing integrated DC-DC converters,” *Dig. Tech. Pap. - IEEE Int. Solid-State Circuits Conf.*, vol. 42, no. 1, pp. 66–73, 2006, doi: 10.1109/isscc.2006.1696279.

[21] V. S. Daniel Arbet, Lukas Nagy, “Ultra-Low-Voltage IC Design Methods,” *Intech*, vol. 32, pp. 137–144, 2019, [Online]. Available: http://www.intechopen.com/books/trends-in-telecommunications-technologies/gps-total-electron-content-tec- prediction-at-ionosphere-layer-over-the-equatorial-region%0AInTec.