FPGA IMPLEMENTATION OF A MULTIHOP WAVELENGTH DIVISION MULTIPLEXING (WDM) RING ROUTER ALGORITHM

by

NURUL HAZLINA BINTI NOORDIN

Thesis submitted in fulfillment of the requirements for the degree of Master of Science

NOVEMBER 2004

ACKNOWLEDGEMENTS

In the name of Allah, the Gracious and Merciful, Syukur Alhamdullilah, thank you to Allah for the strength and opportunity in completing this project.

The thesis would not be successfully completed without several people and they deserve credits. I would like to extend my gratitude to my mentor and supervisor, Prof Madya Dr. Othman Bin Sidek for the guidance and knowledge throughout this research. Also, thank you to Dr. R.Badlishah as a helpful and informative co-supervisor for this project. Their consistent supports and advices have immensely contributed to the completion of this work.

Special appreciations are as well dedicated to both of my parents for their splendid courage and support. Meanwhile, momentous thanks are also in order for all my friends who have helped me in providing information and tools to complete this project.

Last of all, my thanks go to all those who have helped towards the completion of this project in any way.

ii

TABLE OF CONTENTS

	Page
ACKNOWLEDGEMENTS	ii
TABLE OF CONTENTS	iii
LIST OF TABLES	vi
LIST OF FIGURES	v
LIST OF ABBREVIATION	ix
LIST OF APPENDICES	x
LIST OF PUBLICATIONS & SEMINARS	x
ABSTRAK	xi
ABSTRACT	xii

CHAPTER ONE : INTRODUCTION

1.0	Introduction	1
1.1	Wavelength Division Multiplexing Architecture	2
	1.1.1 WDM Routing Algorithm for Multi-hop Network	3
1.2	WDM Physical Switches and Routers	4
1.3	Project Objective	5
1.4	Project Methodology	6
1.4	Thesis Organization	6

CHAPTER TWO : LITERATURE REVIEW

2.0	Background	
2.1	Basic Computer Network	8
	2.1.1 Network Layers	9
	2.1.2 TCP/IP Reference Model	10
	2.1.3 Elements of a Computer Network	11
	2.1.4 Network Topology	13
2.2	Wavelength Division Multiplexing	15
	2.2.1 Wavelength Division Multiplexing Functionality	15

	2.2.2 Classes of WDM Optical Network	16
	2.2.3 Multi-Hop and Single Hop Architectures in Broadcast and	17
	Select Network	
	2.2.4 Requirements for Protocol Support	19
	2.2.5 Physical Elements in WDM	20
2.3	Various Network Processor Architecture	21
2.4	FPGA as Design Tools for CNDR Router	25

CHAPTER THREE : ROUTING ALGORITHM FOR WDM RING NETWORK

3.0	Background	27
3.1	Components of the WDM Ring Network	28
	3.1.1 Physical Structure of WDM Ring Network	28
	3.1.2 Virtual Links and Virtual Rings of WDM Ring Network	29
3.2	3.2 Routing Algorithms for WDM Ring Network	30
	3.2.1 Wavelength Ordered Routing (WOR)	30
	3.2.2 Comparing Dimensional Number Routing (CDNR)	32
3.3	Node Address Assignment of CDNR Algorithm for 15-node Ring Network	34
3.4	CDNR Router Operation and Algorithm	36

.

CHAPTER FOUR : DESIGN APPROACH AND METHODOLOGY

•

4.0	Comparing Dimensional Number Routing (CDNR) Router Design	39
4.1	Logic Structure of a Node	39
4.2	FIFO Xilinx Design	41
4.3	Top Level of CDNR Router Design	42
4.4	Structure of CDNR Algorithm	
	4.4.1 Packets Structure	45
	4.4.2 Top Level Design of CDNR Router	46
	4.4.3 Path Controller of CDNR Router	50
	4.4.3.1 Path Controller Logic Design	52
	4.4.4 RAM Module	54
	4.4.4.1 RAM Address Generator	56

4.4.5 Output Coder	58
4.4.6 Pulse Generator Unit	59
4.4.7 Switching Unit	60
4.4.8 Testbench Module for CDNR Router Verification	61

CHAPTER FIVE : SIMULATION AND IMPLEMENTATION

5.0	Backg	jround	64
5.1	Simula	ation Results	64
	5.1.1	Top Level Design Of CDNR Router Simulation	65
	5.1.2	Path Controller Unit Simulation	67
	5.1.3	Path Process Unit Simulation	66
	5.1.4	Path Coder Unit Simulation	69
	5.1.5	Pulse Generator Unit Simulations	68
	5.1.6	The Simulations of Serial to Parallel Component	71
	5.1.7	The Simulations of Parallel to Serial Converter Unit	72
	5.1.8	Testbench Output Waveform	73
	5.1.9	Analysis of the simulation	74
5.2	Implementation		74
	5.2.1	Implementing Procedure	77
	5.2.2	Implementation Results	78
	5.2.3	Conclusion	79

CHAPTER SIX : CONCLUSION AND DISCUSSION

6.0	Conclusion	80
6.2	Future Work	81
BIBLI	OGRAPHY	82
APPE	NDICES	
Apper	ndix A : Router designs (Xilinx – ISE tools)	84
Apper	ndix B : Implementation reports	105
Apper	ndix C : Publication	120

LIST OF TABLES

2.2	Usage of optical communication components in optical networks	16
3.1	Dimensional number representative of the nodes for CDNR ring network	35
3.2	Virtual rings formed in CDNR ring network and the connecting nodes	35
4.1	Xilinx chip specification used to implement CDNR Algorithm	44
4.2	The mode and function of each signal	46
4.3	Active output of path controller responding to dimensional address	51
4.4	Truth table of CDNR path processing unit	53
4.5	The function of RAMB4_S16_S16 input and output pins	55
4.6	Codes representing the active output	58
4.7	The state and function of the testbench data	61
5.1	The output result responding to the incoming packets	68
5.2	5 samples packets generated by the testbench unit	74
5.3	Input and output ports of CDNR router on FPGA chip	78
5.4	Output observed from logic analyzer	79

LIST OF FIGURES

Page

2.1	Diagram of a node terminal in a computer network	11
2.2	Network Topologies	13
2.3	Levels of functionality incorporated in WDM	16
2.4	Node structure of multihop network ; Physical topology, Logical topology	19
2.5	The anatomy of a switch or router	20
2.6	Block diagram of a generic network processor	21
2.7	Architecture Overview of Motorola C-5 Network Processor	22
2.8	An overview of Agere network processor architecture	23
2.9	Block diagram of Coresma 6001 router architecture	24
2.10	Block diagram of Transport Triggered Architecture (TTA) in an ATM configuration	25
3.1	The logical structure of WDM ring utilizes 15 nodes	29
3.2	Block diagram of a node	31
3.3	Logical structure of the path controller for WOR algorithm as proposed by Xiaoshe Dong	32
3.4	Logical structure of the path controller for CDNR algorithm	33
3.5	A complete diagram of 15 nodes connection that employs CDNR Algorithm that consist the virtual links, virtual rings and its dimensional number	36
3.6	Structure of a node for WDM networks	37
4.1	Block Diagram of a node in WDM network	40
4.2	An In Sight View of a CDNR Router Processing Unit	40
4.3	Block diagram of a synchronous FIFO	41
4.4	FPGA Design Flow Using Xilinx ISE Series 5.1i Suite	43
4.5	Flow chart of a router that employs CDNR Algorithm	45
4.6	Structure of a packet for CDNR router	45
4.7	Top Level Block Diagram of CDNR Router	47
4.8	Top level design flow chart of Comparing Dimensional Number Routing (CDNR) router	49
4.9	Path controller module for 15 nodes ring network	50
4.10	Dimensional number bit of a packet header	50
4.11	CDNR path processing flow chart	52
4.12	Truth table of CDNR path processing unit	53
4.13	RAM module in Xilinx Spartan II E family	54
4.14	Flow chart of Spartan II E RAMB4_S16_S16	56

4.15	Logic block of RAMB4_S16_S16 address generator	56
4.16	Structure of the packet after being buffered in RAM unit	57
4.17	The design of counter unit for address input	57
4.18	Structure of the router output section	58
4.19	PULSE unit to generate reset signals for coder unit	59
4.20	Switch module that combines data bits and code bits	60
4.21	Flow chart of testbench for CDNR router verification	63
5.1	Timing diagram of Top Level execution	66
5.2	Timing diagram of Path Controller Unit execution	67
5.3	Timing diagram of Path Process Unit execution	69
5.4	Timing diagram of Path Coder Unit execution	70
5.5	Timing diagram of Pulse Generator Unit execution	71
5.6	Timing diagram of Serial to Parallel Component execution	72
5.7	Simulation waveform of Parallel to Serial Converter Unit	72
5.8	Timing diagram of the testbench execution	73
5.9	Test bed diagram for CDNR algorithm	75
5.10	BurchED FPGA Demo Board that that occupies 300K gate XC2S300E FPGA	76
5.11	Hardware setup of FPGA Demo Board connection to Network Analyzer and functional generator.	76
5.12	Implementation constraint (.ucf) file	77

LIST OF ABBREVIATION

- ASIC Application-Specific Integrated Circuit
- ATM Asynchronous Transfer Mode
- CDNR Comparing Dimensional Number Routing
- CPU Central Processing Unit
- CRC Cyclic Redundancy Check
- DES Data Encryption Standard
- DOD Department Of Defense
- DSP Digital Signal Processing
- E/O Electrical To Optical
- FIFO First In First Out
- FPGA Field Programmable Gate Array
- ISP Internet Service Provider
- ITU-T International Telecommunication Union, Standardization Sector
- LAN Local Area Network
- MAC Medium Access Control
- MSN Manhattan State Network
- O/E Optical To Electrical
- OMS Optical Multiplex Section
- OTS Optical Transmission Section
- RAM Random Access Memory
- RISC Reduced Instruction Set Computer
- SRAM Static Random Access Memory
- TCP Transmission Control Protocol
- TCP/IP Transmission Control Protocol/Internet Protocol
- VHDL VHSIC Hardware Description Language
- VHSIC Very High Speed Integrated Circuit
- WDM Wavelength Division Multiplexing
- WOR Wavelength Ordered Routing

LIST OF APPENDICES

		Page
1.1	Top level design	85
1.2	Path process design	86
1.3	Path control design	87
1.4	Buffer design	88
1.5	Switch design	90
1.6	Pulse unit design	91
1.7	Multiplexer design	94
1.8	Counter design	96
1.9	Coder design	97
1.10	Testbench design	98
2.1	Synthesis report	106
2.2	Mapping report	109
2.3	Place & Route report	112
2.4	Pad report	115
2.5	Programming file report	119

PUBLICATION

Page

 1.1
 THE AMERICAN INTERNATIONAL UNIVERSITY –
 121

 BANGLADESH (AIUB) Journal of Science and Engineering
 121

 Title - Fpga Implementation Of A Multihop Wavelength Division
 121

 Multiplexing (WDM) Ring Router Algorithm
 121

IMPLEMENTASI SISTEM PENGHALA RANGKAIAN CINCIN MULTIHOP PEMULTIPLEKSAN PEMBAHAGIAN PANJANG GELOMBANG (WDM) KE ATAS FPGA

ABSTRAK

Satu sistem penghalaan yang teratur dan cepat adalah penting untuk memastikan gentian optik digunakan secara optimum. Pemultipleksan pembahagian panjang gelombang (Wavelength Division Multiplexing - WDM) merupakan satu teknik yang digunakan untuk memastikan penggunaan sepenuhnya lebar jalur dalam gentian optik dan untuk mengelakkan masalah bottleneck. WDM terbahagi kepada 2 bahagian iaitu, satu lompatan (singlehop) dan pelbagai lompatan (multihop). Dalam sistem pelbagai lompatan, paket-paket yang akan dihantar ke sesuatu destinasi perlu melalui beberapa Iompatan. Algoritma Perbandingan Nombor Dimensi (Comparing Dimensional Number Routing - CDNR) telah dicadangkan untuk memaksimakan penggunaan lebar jalur gentian optik. Projek ini menerangkan satu rekabentuk rangkaian multihop yang mengaplikasikan algotirma (CDNR) tersebut dan implementasinya ke atas FPGA. Rekabentuk penghala ini terbahagi kepada 3 bahagian iaitu; bahagian masukan, bahagian kawalan laluan dan bahagian keluaran. Proses rekabentuk ini dilaksanakan menggunakan perisian Xilinx ISE dan kadar pemprosesan datanya (throughput) 5GHz. Rekabentuk ini telah berjaya diterjemah, dipeta dan diimplementasikan ke atas BurchED FPGA Demo Board yang mengandungi 300K get XC2S300E Xilinx FPGA. Dalam prototaip ini, penyambungan optik digantikan dengan penyambungan elektrik. Rekabentuk ini turut memuatkan jadual rujukan yang menjana data masukan untuk set penghala. Data keluaran dianalisa menggunakan pengalanisa logik.

FPGA IMPLEMENTATION OF A MULTIHOP WAVELENGTH DIVISION MULTIPLEXING (WDM) RING ROUTER ALGORITHM

ABSTRACT

In order to make the optimum use of a large capacity of optical fibers, a quick routing algorithm is essential. Wavelength Division Multiplexing (WDM) is a technology that is widely employed to fully the huge bandwidth provided by optical fibers and to alleviate electronic bottleneck. WDM network is broadly divided into two categories; single-hop and multi-hop. For multi-hop network, a packet from a source to a destination may have to hop through one or more intermediate nodes. A routing algorithm, Comparing Dimensional Number Routing has been proposed to fully exploit the bandwidth of fiber optics. This project describes the design of a multihop WDM router for ring network that employs Comparing Dimensional Routing Algorithm. In order to evaluate the complexities of the algorithm in hardware, the design has been implemented on Field Programmable Gate Array (FPGA). It is implemented on FPGA to evaluate the complexities of the algorithm on hardware. The design is divided into 3 main blocks; input module, path controller module and output switching module. Using Xilinx ISE software, the designs are successfully translated, mapped, routed and placed onto BurchED FPGA Demo Board. Based on timing simulation results, the throughput of the router is 5GHz. A test bed for evaluating the design is constructed on B5-X300 Board that occupies 300K gate XC2S300E FPGA which is supported by Xilinx Webpack tools. In the prototype, optical interconnecting is replaced with an electrical interconnect. The FPGA chip is equipped with a lookup table that generates input data to supply data vectors. The outputs are subsequently observed for the corresponding data signal using a logic analyzer.

xii

CHAPTER 1 INTRODUCTION

1.0 Introduction

Optical network offers high speed data bit rate with a very low bit error rate, which is needed in many applications. Due to these flexibilities, optical fibers are used for all types of communication including audio, video, and data applications in real and non-real time (Werner Bux et al, 2001). The basic element in the optical network is the wavelength. One of the benefits of optical networks is that different network architecture can be designed based on a single wavelength. As many wavelengths of signals are transported across the network, it becomes important to manage and switch each one individually. The efficiency of an optical network can be optimized by applying wavelength division multiplexing (WDM) technique.

Before the advent of WDM (Wavelength Division Multiplexing), increasing the transmission capacity of a link could only be achieved by multiplying the number of lines and accumulating repeaters-regenerators. With WDM, a single optic fiber is sufficient for transmitting several signals of different wavelengths at the same time.

By implementing WDM technique, signals are transmitted in many different colors (wavelengths) of laser light down the same optical fiber. Early WDM systems used two wavelengths: 1310 nm and 1550 nm which have zero dispersion point for traditional single-mode fiber and the lowest attenuation point for silica-based single mode fiber, respectively (Juha Itkonen, 1998). However, the wavelengths vary according to the specified band as defined by International Telecommunication Union (ITU). The bands are; the O-Band (1,260nm to 1,310nm), the E-Band (1,360nm to 1,460nm), the S-Band (1,460nm to 1,530nm), the C-Band (1,530nm to 1,565nm), the L-Band (1,565nm to 1,625nm) and the U-Band (1,625nm to 1,675).

A WDM system is characterized by its capacity, which is the product of the number of channels carried by a fiber multiplied by the transmission throughput of each channel, and by its range, or the distance between the transmitters and receivers.

A wavelength-routed network provides end-to-end permanent or switched connections, known as light paths. In today's high-end long-distance communication, each optical signal (often referred to as a channel or a wavelength) can operate at up to 2.5 Gbps or 10 Gbps. Currently, available systems can support up to 64 channels and vendors are promising to commercialize up to 160 channel systems in the near future. This enables a single fiber to carry more then 1 terabit/s of information (Cisco, 2000).

WDM has been one of the technologies used for long-distance carrier networks in the last ten years, due to an ever-decreasing cost per km transmitted and everincreasing ranges. This explains the WDM hegemony over backbone networks of major operators, which is taking advantage of WDM to optimize their architecture and enrich their service.

1.1 Wavelength Division Multiplexing Architecture

Wavelength Division Multiplexing architecture can be broadly divided into multihop and single-hop networks. Single hop network requires the nodes to communicate with each other in a single hop. This requires a significant amount of dynamic coordination between the nodes, since, for packet transmission duration, one of the transmitters of the sending node and one of the receivers of the destinations node must be tuned to the same wavelength channels. To assure the network efficiency, the transmitters and receivers must be very rapidly tunable. However, there is a limitation in single hop network where it may incur significant overhead due to high tuning times

of tunable components (Jason P. Jue et al, 2000). This situation requires the transmitters and receivers of single hop network to be dynamic. Alternatively, in multihop network system, the channel to which a node's tuning transmitter or receiver is relatively static. This means that there will be no direct path among the nodes. Due to this scenario, a packet from a source node to a destination node may have to hop through several intermediate nodes.

Transceiver's tuning time plays a vital role in determining the performances and characteristics of a network system. However, its impact on multihop network is little compared to the single-hop network since the multihop virtual topology is essentially static.

1.1.1 WDM Routing Algorithm for Multi-hop Network

In 1997, Xiaoshe Dong had proposed Wavelength Ordered Routing (WOR) algorithm to manage the routing system of a multi-hop ring network (Xiaoshe Dong et al, 1997). Two years later, another routing algorithm for WDM multi-hop ring network, Comparing Dimensional Number Routing (CDNR), was introduced by Tomohoro Kudoh from Keio University, Japan (Tomohoro Kudoh et al, 1999).

When a node receives a packet in Wavelength Ordered Routing (WOR) system, it will compare the destination identifier bits, *d*, from the header of a packet with the node's own identifier, *i*. If they are the same, the packet is transferred to the connected node as it indicates that the packet has arrived at its destination. Otherwise, it will select another alternative path and sends the packet through the intermediate virtual ring.

However, in Comparing Dimensional Number Routing (CDNR), each node is assigned with a unique dimensional number. Routing is done based on the comparison

between these dimensional number bits and the destination identifier bits, *d*, from the header of a packet.

Between these two algorithms, the implementation of Wavelength Ordered (WOR) algorithm is much more complicated compare to the implementation of Comparing Dimensional Number Routing (CDNR) (Tomohoro Kudoh et al, 1999). Due to this complexity, WOR requires larger circuit to implement the routing process. Both of WOR and CDNR algorithm is further discussed in Chapter 3.

1.2 WDM Physical Switches and Routers

The proliferation of WDM transmission system has given rise to the question of scale that is whether the switches and routers can deal with the multiplication of fiber transmission capacity by a corresponding of port increase. Building bigger system implies two issues; having to distribute packets over more processing units and making switches with many more input and output ports (Werner Bux et al, 2001). Apart from that, the port's switching and routing speeds inevitably have to follow the increasing speed of serial transmission over fibers.

The challenge in developing WDM router and switches is to achieve a fast processing hardware. This was made possible by advances in Application-Specific Integrated Circuit (ASIC) technology, combined with design optimization in packet processing and switching hardware. ASIC technologies offer a faster processing time compare to CPU (central processing unit) in developing a router or switch unit. This is because CPU has problems with real time processing due to the interrupt handling commands, cache hierarchy and operating system. These operations require the packets to be buffered several times.

Even though CPU's programmability is important, their floating-point units go unused. Besides that, ASIC's design are capable in delivering 'wire speed' processing for Gigabit Ethernet and fast optical connections such as OC-12 (622 Mbps) and OC-48 (2.488 Gbps) (Linley Gwennap, 2001). ASICs also consolidates the work of many chips into a single, smaller, faster package, reducing manufacturing and support costs while boosting the speed of the device built with them. However, ASICs offer little or no reconfigurability besides the expensive development cost; the cost of the tools alone makes them unaffordable for many companies (Mark Kohler, 2001).

An alternative technology, known as Field Programmable Gate Array (FPGA), has emerged that combines the high performance of custom silicon and ASICs with the dynamic reprogrammability of the microprocessor or network processor (John W. Lockwood et al, 2001). The FPGA contains an array of combinational logic circuits, Flip/Flops, and on-chip memory that can be programmed to implement thousands parallel logic circuits and/or finite state machines to process packets at high speed. Every logic element on the device can be reprogrammed. This approach adds flexibility when compared to an ASIC solution and reduces control overhead when compared to a general purpose CPU. Reducing the control overhead leads to less power consumption and higher performance (Tomas Henriksson, 2001).

1.3 Project Objective

The main objective of this project is to develop an FPGA based prototype of a router for multihop WDM ring network that implements the Comparing Dimensional Number Routing (CDNR) algorithm. FPGA is chosen as the medium to develop the prototype as it is cost effective compare to ASICs' design due to its reprogramability advantage. Besides that, this project is also aimed to develop a trainer kit using FPGA as a learning tool due to its reconfigurable capabilities and portability.

In this project, the prototype is designed based on a 15 nodes ring topology with 9 wavelengths. Each node is assigned with a different dimensional number. The router is developed in VHDL and schematic environment using Xilinx ISE software. The design is later downloaded onto a B5-X300 BurchED FPGA demo board. The board houses a 300K-gates XC2S300E FPGA. The throughput of the designed system is 2.285Gbps and it can operate up to 5GHz of data input. The FPGA chip is equipped with a lookup table that generates input data pattern to supply data vectors. The outputs are subsequently observed for the corresponding data signal using a logic analyzer to verify the functionality of the router.

1.4 Project Methodology

In the beginning phase of this project, the network performances of Comparing Dimensional Number Routing Algorithm (CDNR) were observed with OMNett software. The module consists 15-nodes ring network. Every node is equipped by a Medium Access Control (MAC), a packet generator and a receiver.

The router controller unit is designed using XIIinx ISE software. There are two modes of design entry used in this project, which are VHDL and schematic. After the design is successfully drawn, it is then synthesized. The verification of the design is done with both functional and timing simulation. Upon the success of the simulated results, the designs are implemented on FPGA chip. Later, the hardware output of the designed router is observed using Logic Analyzer.

1.5 Thesis Organization

Chapter 2 discusses the Wavelength Division Multiplexing (WDM) technologies and its protocols. It covers the basic understanding of single-hop and multihop architecture. This chapter also outlines the physical elements of WDM, specifically the architecture of network processor and classes of WDM optical network.

Chapter 3 elaborates the two algorithms of WDM multihop ring network, which are Wavelength Ordered Routing (WOR) and Comparing Dimensional Number Routing (CDNR). It also focuses on the implementation of CDNR algorithm for a ring network which consists of 15 nodes. The calculation of each node's dimensional number is also shown here.

Chapter 4 describes the design of the router. The designs are divided into three segments, which are the input part, the controlling part and the output part. The designs are done in both schematic and VHDL environment. This chapter also expands the design's characteristics.

Chapter 5 presents the simulation results of the router. The timing simulations were performed using ModelSim Tools Software. This chapter also explains the FPGA board-level implementation procedures and the aspect of hardware setup. The hardware output of the designed router is observed using Logic Analyzer.

Chapter 6 concludes the whole project. Some conclusive remarks are presented in this chapter as well. Apart from that, future work and suggestion for improvements are also indicated at the end of this chapter.

CHAPTER 2 LITERATURE REVIEW

2.0 Background

Computer network usage has increased enormously over the last decades. When Internet gained popularity in the middle of the 1990's, computer network became everyone's concern and the network capacity was far less than the demand. In the last five years, the data traffic has actually more than doubled every year (L. Geppert, 2001). In the second half of the 1990's, optical transmission equipments and optical fibers have been developed in order to cope with the throughput increment of each physical link. With the introduction of wavelength division multiplexing (WDM), the throughput increased further by more than one order of magnitude (Tomas Henriksson, 2001).

The electronic equipments that process the information sent over these optical links has not kept up with the increase in transmission speeds. This in combination with the need for more advanced network features, such as Quality of Service (QoS), traffic shaping and network security which has recently led to the development of many new hardware architectures for network equipments (Tomas Henriksson, 2001).

2.1 Basic Computer Network

Computer networks are used to connect small groups of computers. These computers are located closed to each other. It is known as local area network (LAN). Network function can be described through its protocols. The reference model used is ISO/OSI (Industry Standard Organization/Open System Interconnection).

2.1.1 Network Layers

There are two protocols which are widely referred to in networking. They are OSI Reference Model and Transmission Control Protocol/Internet Protocol (TCP/IP). OSI Reference Model consists of 7 layers as shown in Table 2.1. It was developed in 1984 and describes how the protocols should be implemented.

Layers	Main Functions				
Application	Provides different services to the applications				
Presentation	Converts the information				
Session	Handles problems which are not communication issues				
Transport	Provides end to end communication control				
Network	Routes the information in the network				
Data Link	Provides error control between adjacent nodes				
Physical	Connects the entity to the transmission media				

Table 2.1: The 7 layers of ISO/OSI reference model

The physical layers describe the physical characteristics of the communication, such as conventions about the nature of the medium used for communication (such as wires, fiber optic links or radio links), and all related details such as the connectors, channel codes and modulation, signal strengths, wavelengths and timing issues. The data link layer specifies how packets are transported over the physical layer, including the *framing* signal. *Framing* signal is the special bit patterns that mark the start and end of packets. Examples of Data-link layer protocols are ethernet, wireless ethernet, SLIP, token ring and Asynchronous Transfer Mode.

The third layer, network layer, solved the problem of getting packets across a single network. Examples of such protocols are XX.25 and the ARPANET's Initial Connection Protocols. With the advent concept of internetworking, additional functionality was added to this layer, namely getting data from the source network to the destination network. This generally involves routing the packet across a network of networks, known as internet. The protocols at the transport layer solve problems of

reliability of sending information to intended destination and ensure that data arrives in the correct order.

The session layer uses transport layer to establish a connection between processes on different hosts. It handles security and creation of a session. The presentation layer performs functions such as text compression, code or format conversion to try to smooth out differences between hosts. It allows incompatible processes in the application layer to communicate via the session layer. The application layer handles issues like network transparency, resource allocation and problem partitioning. The application layer is concerned with the user's view of the network (e.g. formatting electronic mail messages).

2.1.2 TCP/IP Reference Model

Transmission Control Protocol (TCP) is a connection-oriented transport protocol that sends data as an unstructured stream of bytes. TCP and IP were developed by a Department of Defense (DOD) research project to connect a number of different networks designed by different vendors into a network of networks known as the Internet. It was initially successful because it delivers a few basic services that everyone needs such as file transfer, electronic mail and remote login across the large number of client and server systems.

The layers of TCP/IP are simplified to 5 main layers which are application layer, transport layer, network layer, link layer and physical layer.

TCP is responsible for verifying the correct delivery of data from client to server. Data can sometimes lost in the intermediate network; therefore, TCP adds support to detect errors or lost data and to trigger retransmission until the data is correctly and completely received. Meanwhile, IP is responsible for moving packet of data from node to node. IP forwards each packet based on a four byte destination address, known as IP address. The Internet authorities assign ranges of numbers to different organizations. The organizations assign groups of their numbers to departments. IP operates on gateway machines that move data from department to organization to region and then around the world.

2.1.3 Elements of a Computer Network

The different types of elements in a computer network can roughly be categorized into two main classes; terminals and routers (Tomas Henriksson, 2001). Network terminals are presented in many different environments such as desktops, computers, printers, IP phones and web cameras. Figure 2.1 shows a basic block diagram of a terminal in a computer network.

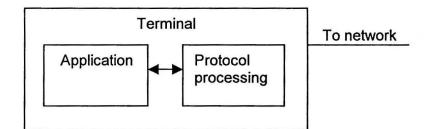


Figure 2.1 Diagram of a node terminal in a computer network

The terminals have to handle all layers of protocols in the ISO/OSI reference model. The transport layer protocols deal with end-to-end communication, which are connection oriented. A connection-oriented protocol must build up a connection before any data can be transported and it tears down the connection when the data transfer is completed.

However, routers are fundamentally different from terminals, since their main operation is not to take active part in any communication, but rather to forward data to the correct destination. Routers can operate at many different layers in the ISO/OSI reference model, traditionally they only manage protocols up to layer 3 (Tomas Henriksson, 2001).

A router that only works on layer 1, the physical layer, is called a repeater. A repeater simply amplifies the signal carrying the data so that it can travel longer distances. A router that works on layer 2 is normally called a switch. A complete router works on layer 3 and interconnects two or more layer 2 links of different type, which are nowadays normally point-to-point links. The Internet Protocol (IP) is the network protocol that has become dominant in the world and it is not likely that any other network protocol will take over in the foreseeable future, except from the next generation IP, IPv6.

Generally router functionalities can be split into two planes, the data plane and the control or management plane. The data plane consists of the performance demanding and simple task of forwarding packets to the correct link. The control plane consists of all other activities, that are more complex, but does not require fast handling, although routing table updates may be as frequent as several hundred per second.

Routers are becoming more complex as they can be used for traffic shaping which deals with the task of balancing the traffic. The traffic must pass a single point in the network on two or more links that eventually all will lead to that point. The routers are also used for policing purposes which are concerned with limiting the traffic, from or to a certain terminal or group of terminals, e.g. if a company has only paid for a certain bandwidth, the Internet service provider (ISP) routers will limit their usage to this bandwidth. Besides that, routers are also used to gather statistic. The statistics are needed in traffic shaping and policing. They are also used by the operator in order to analyze the network performance and resolve possible bottlenecks. The routers are

also used for security purposes. It does simple firewall tasks, such as not allowing packets from a specific source to enter a special part of a network, to advanced virus scanning and denial of service attack detection and prevention.

All of these tasks require the router to process layer 4 information of the packet header and sometimes even layer 7's information of the OSI model. These processes require the router to scan through all data in the packet.

2.1.4 Network topology

A network may be represented as a collection of nodes, some of which are connected by links. A given node may have links to many other nodes as seen in Figure 2.2. Network topology is determined only by the configuration of connections between nodes.

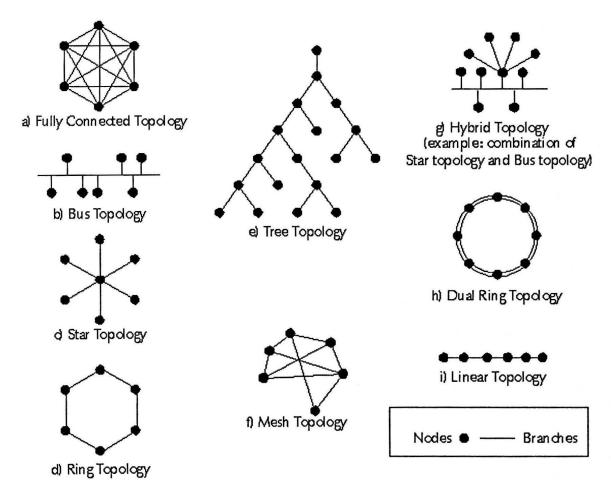


Figure 2.2 : Network Topologies

A fully connected topology is a network topology in which there is a direct link between all pairs of nodes. In a fully connected network with N nodes, there are N(N-1)/2 direct links. It is also known as mesh network. While a bus topology is a network topology in which there is a single line to which all nodes are connected, and the nodes connect only to this bus.

A star topology is a network in which peripheral nodes are connected to a central node, which rebroadcasts all transmissions received from any peripheral node to all peripheral nodes on the network, including the originating node. All peripheral nodes may thus communicate with all others by transmitting to, and receiving from, the central node only. Ring topology network exactly two branches connected to it. These nodes and branches form a ring. If one of the nodes on the ring fails than the ring is broken and cannot work. A dual ring topology has four branches connected to it, and is more resistant to failures.

A tree topology network resembles an interconnection of star networks in that individual peripheral nodes which are required to transmit to and receive from one other node only and are not required to act as repeaters or regenerators. Unlike the star network, the function of the central node may be distributed. Meanwhile, in mesh topology, there are at least two nodes with two or more paths between them. A hybrid topology is a combination of any two or more network topologies in such a way that the resulting network does not have one of the standard forms. A hybrid topology is always produced when two different basic network topologies are connected.

Among all the topologies, ring topologies have been widely used in wavelength division multiplexing WDM networks. This is because of the high percentage of packet survival capabilities in ring topology and the fact that their capacity can be shared by all the connecting nodes (Georgios Ellinas et al, 1998).

2.2 Wavelength Division Multiplexing

Wavelength-Division Multiplexing (WDM) is a transmission technology, which enables transmitting multiple channels on multiple wavelengths of light along a single optical fiber. WDM takes optical signals (each carrying information at a certain bit rate), gives them a color (a wavelength or specific frequency), and then sends them down the same fiber. Each piece of equipment sending an optical signal has the illusion of having its own fiber. WDM gets more information (wavelength) to travel, not by increasing their speed but by getting them to travel in parallel in their own dedicated lanes. WDM is widely applied in Synchronous Optical Network (SONET) protocol as SONET over WDM network provides scalability and cost-effectiveness.

2.2.1 Wavelength Division Multiplexing Functionality

There are three levels of functionality distinguished for WDM, based on the classification for the different types of functions as defined by The International Telecommunication Union, Standardization Sector (ITU-T) (Roue-Peden, 1998).

The Optical Transmission Section (OTS) Layer is concerned with the final transmission of bits over optical fibers (B.D Theleen et al, 2002). To this purpose, functions are included for optically empowering the data signals regarding all wavelength channels simultaneously. To provide independent wavelength channels, the Optical Multiplex Section (OMS) Layer includes functions that represent the actual utilization of the WDM technique. Besides that, it also includes functions for the optional use of wavelength conversion in the optical domain. The Optical Channel Section (OCS) Layer specifies functions for offering the separated wavelength channels to function of higher –layer protocols, which are implemented in the electrical domain.

To provide services to users, WDM is merely concerned with transmitting bits over fibers. With respect to the OSI reference model, WDM includes only functionality regarding the physical layer. The three levels of functionality distinguished in Figure 2.3 are therefore seen as sub layers of the physical layer.

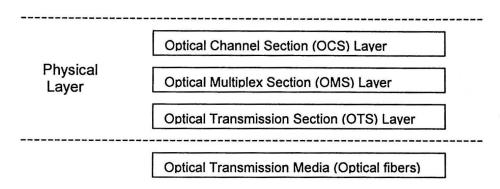


Figure 2.3 Levels of functionality incorporated in WDM

2.2.2 Classes of WDM Optical Network

Optical network can be defined by four broad classes, based on the types of optical communications components used (Malathi Veeraraghavan et al, 2001). Table 2.1 shows the usage of optical communication components in optical networks.

Optical communication	Classes of optical network				
components	Optical link networks	Broadcast- and-select networks	Wavelength- routed networks	Photonic packet- switched networks	
Non switching optical components	Yes	Yes	Yes	Yes	
Tunable transmitters /receivers	No	Yes	May or may not present	May or may not present	
Optical circuit switches (OADM&OXC)	No	No	Yes	May or may not present	
Optical packet switches	No	No	No	Yes	

Table 2.1: Usage of optical communication components in optical networks

Optical link networks consists of all electronic switches interconnected by optical links which can be a single-channel or a multi-channel point-to-point links, or shared-medium broadcast links. Point-to-point multi-channel links are created by placing WDM multiplexers/demultiplexers at the end of the fiber while shared-medium broadcast links are created through the use of WDM passive star couplers.

Meanwhile, in broadcast-and-select (B&S) networks, the components used in this network are tunable transmitter and receivers. Data is broadcast on all the links and receivers are programmed to select the channels they should receive. These networks are classified as either single-hop or multihop. These terms indicate whether user data only traverses optical switching components on the end-to-end path (singlehop) or whether it traverses a combination of optical and electronic switching components (multihop).

Wavelength-routed networks include optical circuit switches (OADMs/OXCs), and optionally tunable transmitters and receivers. This network can also be classified as single-hop or multihop. Single-hop wavelength routed networks use only optical switching components such as photonic switches and optical WDM XCs while multihop wavelength routed networks consists of optical circuit switches, electronic switches and optionally tunable transmitters and receivers.

Photonic packet-switched networks contain optical packet switches, optionally tunable transmitters and receivers. The optical circuit switching could be in the form of OADMs/OXCs or tunable transmitters and receivers that tuned on call-by-call basis.

2.2.3 Multi-Hop and Single Hop Architectures in Broadcast and Select Network

Basic goal of a protocol is to provide a certain degree of connectivity among the nodes. Broadcast and select network works by having the inputs from various nodes,

which are combined in a WDM star coupler, and later the mixed optical information is broadcast to all outputs (Biswanath Mukherjee, 1992). Generally, there are 2 classes of architectures that can be constructed for both WDM local and metropolitan area network which are single-hop and multihop (Biswanath Mukherjee, 1992).

Single hop network provides direct connection between the source and destination of a packet during packet transfer duration. It requires some amount of coordination between the nodes that involve tuning of the transmitter or receivers at each node (Malathi Veeraraghavan et al, 2001). A single hop protocol achieves connectivity through the use of tunable components. Each node communicates directly with every node. However, there is a limitation in single hop network where it may incur significant overhead due to high tuning times of tunable components (Jason P. Jue et al, 2000).

A multihop network achieve its connectivity through the use of additional transmitters and receivers at each node and requires no tuning, instead relying on a static logical topology. It does not incur the potentially high tuning overhead of a single-hop network. The disadvantage of this kind of network is that its reliance on multiple transmitters and receivers, which often result in low connectivity in the network, and consequently higher average hop distances (Jason P. Jue et al, 2000). Figure 2.4 shows the physical and logical topology of a multihop network.

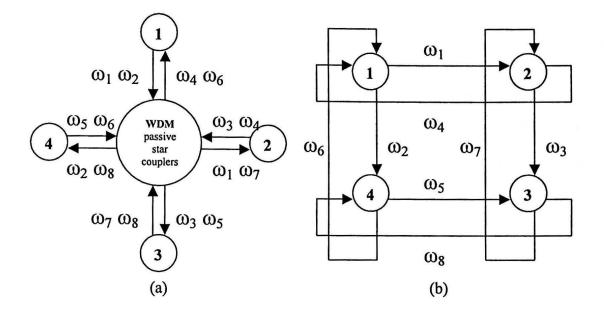


Figure 2.4: Node structure of multihop network (a) Physical topology (b) Logical topology

There are several isues which must be considered in designing a good multihop system. The structure's average hop distance between nodes must be small. Then, the average packet delay must be minimal, apart from that, the nodal processing complexities must also be small in order to achieve a high speed environment (Biswanath Mukherjee, 1992). Consequently, simple routing mechanism must be employed.

2.2.4 Requirements for Protocol Support

To comply with the prescription of the OSI reference model, protocols for directly supporting WDM must include functionality of the data link layer (B.D Theleen et al, 2002). The functions of data link protocols are concerned with supplying an errorfree transfer of data over the physical wavelength channels of an optical fiber. Generally, there are 3 main strategies for reserving wavelength channels (B.D Theleen et al, 2002), which are;

- Single Protocols Support concerns of reserving all wavelength channels of a fiber for a single supporting protocol. In this case, all wavelength channels transmit distinct data signals that have a similar intrinsic structure.
- Static multi-protocol support concerns of having different kinds of higher-layer protocols. In this case, it is possible to implement and identify exactly which wavelength channels are reserved for what supporting at any time during the exploitation of the communication network.
- Dynamic multi-protocol support the reservation of a wavelength channel for a specific supporting protocol can change during operation of the communication network.

2.2.5 Physical elements in WDM

Basically, WDM routers and switches are built from a couple of elements, which are;

- 1. Line interface; which physically attach multiple transmission system and provide framing functionality.
- Network processors; provide the intelligence to analyze packet headers and lookup routing tables besides classify packets based on their destinations and provide queuing and policing of packets.
- Switch fabric; which provides high-speed interconnection of the node's packet processing unit.
- System processor; which performs control point functions such route computations and network management.

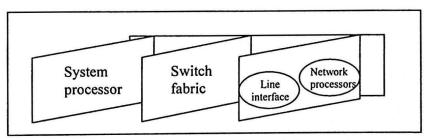


Figure 2.5: The anatomy of a switch or router

Figure 2.5 illustrates the general operation principles of a network processor (Werner Bux et al, 2001). The bitstream receives the serial stream of packet data and extract the information needed, such as IP source/destination address, for further process. The packet is later written into the packet buffer memory. While the extracted control information is fed to the processor complex, which constitute the programmable unit of this network processor unit. The search engine unit looks up the medium access control (MAC) or IP address classifies the packets and also search for virtual path identification properties. A generic network processor is shown in Figure 2.6.

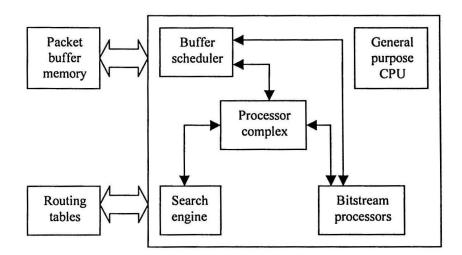


Figure 2.6: Block diagram of a generic network processor

2.3 Various Network Processor Architecture

The basic architectures used for packet processing are traditional general purpose CPU's (central processing unit) and fixed function ASICs (application specific integrated circuits) (Tomas Henriksson, 2001). In this section, several network processor architectures and designs are discussed.

The first architecture is Motorola C-5 Network Processors. Motorola C-5 Network Processors can handle cell and packet processing, table lookup processing, and queue management functions, which makes it suitable for routers. It has 16

Channel Processors (CP) and 5 supporting units for table lookup, queue management, buffer management, switching interface and control as illustrated in Figure 2.7. The supporting processors are most likely of ASIC type. The channel processors consist three parts, which are an internal control and two serial data processors, each for transmission and reception of packets. Motorola C-5 network processor architecture is illustrated in Figure 2.7.

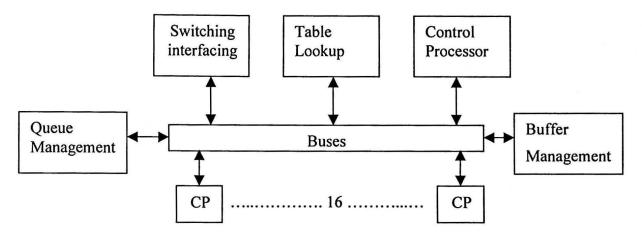


Figure 2.7: Architecture Overview of Motorola C-5 Network Processor

The Agere Fast Pattern Processors is aimed for line card and big routers. It performs packet classification, traffic managements, quality of services and packet modification functions. This fast pattern processor is built up of several blocks, which work in parallel. The input framer of fast pattern processor splits the data stream into 64 byte blocks. These blocks are then sent to routing switch processors for further process. Figure 2.8 shows the block diagram of Agere network processor architecture.

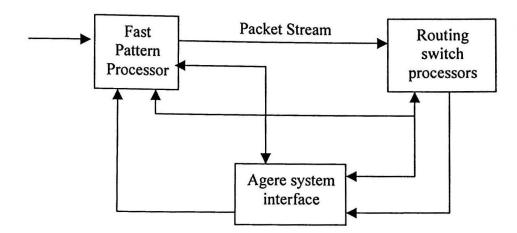


Figure 2.8: An overview of Agere network processor architecture

Coresma 6001 is another network processor architecture. It is a host based universal protocol processor. It can handle many protocols on layer 2 and layer 3. It is intended for desktop computers and supports a PCI interface in order to be able to connect to the main computer bus. The Coresma 6001 consists of a 4 RISC processors; two of them work in the transmitting path while the other two in the receiving path. Apart from that, there are also fixed function units that support CRC (cyclic redundancy check) and DES (data encryption standard) operations. The first-infirst-out unit classifies the packets according to the arrival time. The first data will be given the priority to be first processed in the next stage. Figure 2.9 shows the block diagram of Coresma 6001 router architecture.

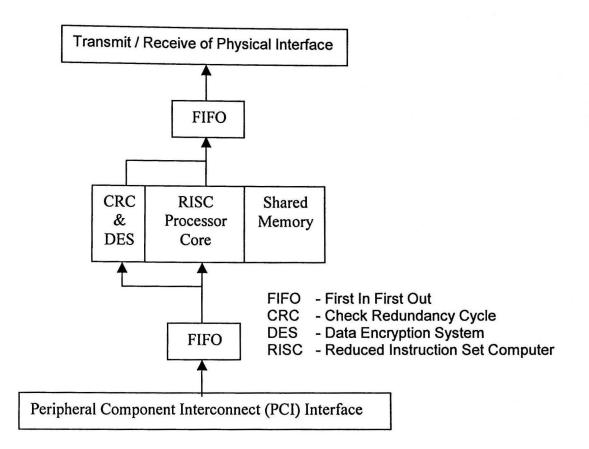


Figure 2.9: Block diagram of Coresma 6001 router architecture

The last network processor architecture is known as Transport Triggered Architecture (TTA). It was developed for network processing application. The main concept is to have only one instruction, which is move. The data can then be transported to the Functional Units (FU) of the processors and as soon as input data is available at an FU, it will process the data and produce an output. In this way, the program controls data movements rather than data processing. Figure 2.10 shows the block diagram of TTA in an Asynchronous Transfer Mode (ATM) configuration.