DESIGN OF AN ULTRA-WIDEBAND FREQUENCY-MODULATED CONTINUOUS WAVE

SHORT RANGE RADAR SYSTEM FOR EXTENDING INDEPENDENT LIVING

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ABSTRACT

Design of an Ultra-Wideband Frequency Modulated Continuous Wave Short Range Radar System for

Extending Independent Living

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Falls in the disabled and elderly people have been a cause of concern as they can be immobilized by the fall and have no way to contact others and seek assistance. The proposed frequency modulated continuous wave (FMCW) short range radar (SRR) system, which uses ultra-wideband (UWB) signals can provide immediate assistance by monitoring and detecting fall events. The unique characteristics of this system allow for a frequency-based modulation system to carry out triangulation and sense the location of the fall through the usage of a continuous chirp signal that linearly sweeps frequency. This project focuses on the development, design and simulation of a ring oscillator that exhibits the frequency modulated signal on a single integrated circuit chip. The ring oscillator is controlled by a voltage ramp signal generator and a voltage to current (V-I) converter. The circuit is designed in Cadence using TSMC 180nm process technology and operates in the frequency range of 3.409 GHz to 5.349 GHz with a spectral bandwidth of 1.94 GHz, which meets the Federal Communications Commission's standards for unlicensed ultra-wideband transmissions.

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Chapter 1

INTRODUCTION

The need for research and solutions towards extending independent living for the elderly and disabled population has been increasing throughout the years. The number of elderly Americans is projected to nearly double from 52 million in 2018 to 95 million by 2060 and many of them have many pre-existing conditions and risk factors that can contribute to a high chance of falling [1]. These factors include lower body weakness, vitamin D deficiency, vision problems, usage of medicines that affect balance, and home hazards such as loose carpet or broken steps. A leading cause of injury-related visits to emergency departments for adults aged 65 or older in the United States, falling can lead to head injuries and broken bones as well as the increased likelihood of falling again [2]. Many of those who fall are immobilized and risk the danger of being unable to contact for help and seek assistance. Although the elderly or disabled can live in a care facility or hire full-time caretaker to reduce this risk, the option to live independently in the comfort of their own home with privacy is much more enticing if they have access to assisted living systems that can monitor and protect them. Therefore, such real-time monitoring systems like fall detectors can significantly extend independent living for the elderly and disabled by gathering detailed health data of the user and allowing for quick response to events.

Video surveillance is one way to monitor subjects and can easily notify for immediate assistance in case of emergencies [3]. However, multiple cameras are required to cover all lines of sight and blind spots or when the user is obstructed by an object or wall; this leads to a large amount of hardware and more costs. Additionally, this monitoring system is obtrusive as it does not allow privacy for the user.

Wearable medical devices are another type of devices that can detect if a fall has occurred by using sensors such as accelerometers or gyroscopes [4]. However, these wearable sensors tend to be invasive and only provide useful information if the user remembers to put the device on daily. This

can be a huge problem in the elderly population, many of whom suffer from Alzheimer's and memory loss.

LifeAlert is a commercial product that allows users to contact for help when they have fallen. The user wears a pendant with a button in which if it pressed, proper authorities and emergency services will be directly contacted and notified. The issue with this solution is that, like wearable medical devices, it is obtrusive and requires the user to remember to wear the device at all times. The user must also be capable of operating and using the pendant, which is not likely if they are unconscious after they have fallen. Additionally, the LifeAlert service requires a monthly fee in addition to activation costs [5].

Radar is alternative method that can help with the limitations that these current systems have. Electromagnetic waves in radar system can be used to detect and identify objects, or in this case, persons. The signals propagate throughout the air until it reaches the object; once reached, part of the signals is reflected back towards the radar system which can be used to determine characteristics of the person such as location, size, and shape [6]. Due to the fact that electromagnetic waves are used for detection, this system is unobtrusive and provides full privacy for the user. A single radar unit system can also be used to monitor multiple rooms, which means the complexity and cost of eldercare monitoring are reduced. The accuracy and efficiency of these systems can greatly improve healthcare quality for independently living.

The proposed system in this paper offers an efficient and unobtrusive method of in-home monitoring and fall detection without compromising the user's privacy by using ultra-wide-band (UWB) frequency modulated continuous wave (FMCW) short-range radar (SRR) technology. The unique characteristics of this radar system allow for boundary and fall location detection through multiple rooms, walls, and obstructive objects in an entire floor; therefore, less hardware is required which leads to reduced production and maintenance costs. UWB also allows for low power transmission and robustness against multipath interference [7]. The small-sized package of this system

which contains the transmitter, receiver, and other hardware components will minimize invasiveness and obtrusiveness in the user's home and space.

The key feature of FMCW is that it continuously transmits a linear, frequency swept chirp signal over a period of time to find object distance and therefore the location of the fall. This thesis focuses on the development, design, and simulation of the chirp signal through a current-starved ring oscillator controlled by a voltage ramp signal generator and a voltage to current (V-I) converter using the TSMC 180nm process technology. The chirp signal operates at a frequency range of 3.409 GHz to 5.349 GHz with a spectral bandwidth of 1.94 GHz. In Chapter 2, brief backgrounds regarding the characteristics of UWB, FMCW and ring oscillators are discussed. In Chapter 3, the development and design of the schematic and layout of the circuit are discussed. Chapter 4 describes the testing and simulation setup to verify the correct operation of the circuit. Chapter 5 contains the analysis and discussion of the results from the testing and overall design of the circuit. Chapter 6 provides concluding remarks and explores future potential work for this system.

Chapter 2

BACKGROUND

2.1 UWB Background

UWB is a radio technology, used in short-range radiocommunication, that transmits low radio-frequency energy over a large frequency range. In location and imaging devices, UWB is very precise and less sensitive to noise as it is able to retrieve more information from a single transmission due to its large frequency bandwidth. Low power transmission allows it to be usable alongside with other sensitive devices such as medical sensors and devices [7].
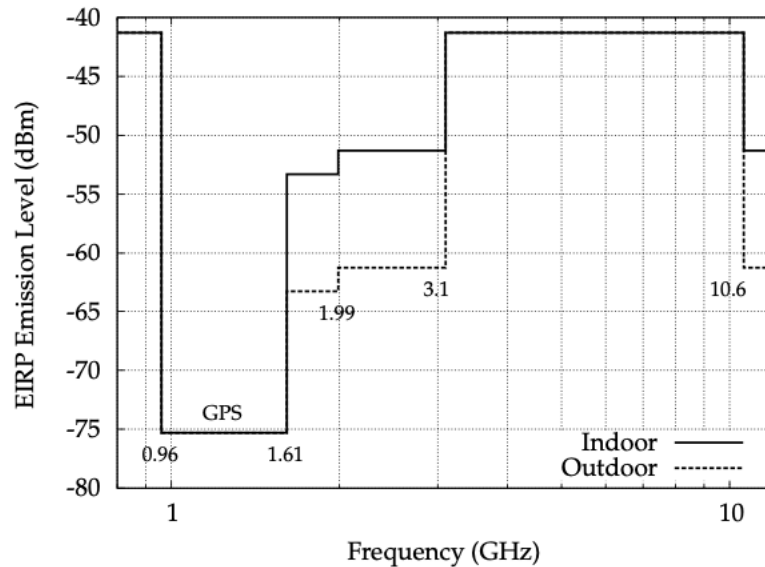
Figure 2-1: FCC mask for power limits on UWB transmissions.

The Federal Communications Commissions (FCC) allows for unlicensed ultra-wideband transmissions in the frequency range from 3.1 to 10.6 GHz and regulates the legal definition of an ultra-wideband signal. According to Title 47, Part 15 of the Code of Federal Regulations, devices using UWB technology are required to have a spectral bandwidth of at least 500 MHz measured at 10 dB below the peak power. These devices are also limited to a power spectral density emission of -41.3 dBm/MHz in the required frequency range, as shown in Figure 2-1. Additionally, there is a peak power limit of 0 dBm EIRP on the emissions contained within a 50 MHz bandwidth centered on the

frequency at which the highest radiated emission occurs. Eq. 2-1 shows that the equivalent isotropic radiated power (EIRP) is defined as the product of the power supplied to the antenna and antenna gain [8].

$$EIRP_{max}(dBm) = P_A(dBm) + G_{A(max)}(dB) \qquad (2\text{-}1)$$

2.2 FMCW Background

FMCW radar is a radar system that continuously transmits a linear, frequency-swept chirp signal. As shown in Figure 2-2, its frequency output increases linearly with time set by a sweep rate, k_f. This chirp signal propagates waves from the transmitter out to objects and back; the time it takes to return back to the receiver, proportional to the frequency difference between the transmitter and receiver signals, is used to find the object distance and location [9].
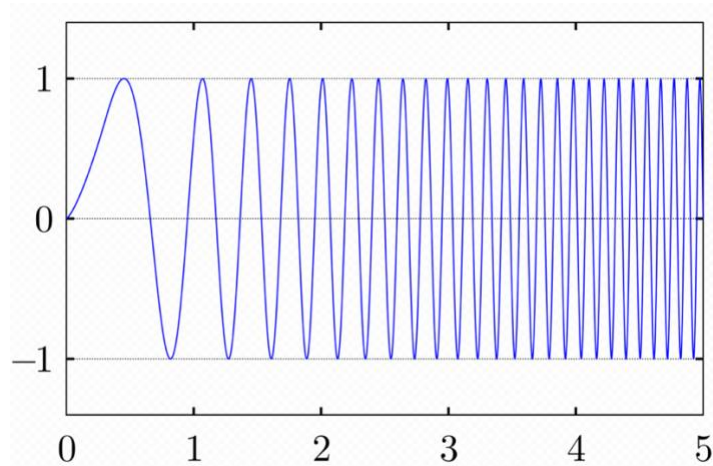
Figure 2-2: Time Domain Output of the Transmitted Chirp Signal.
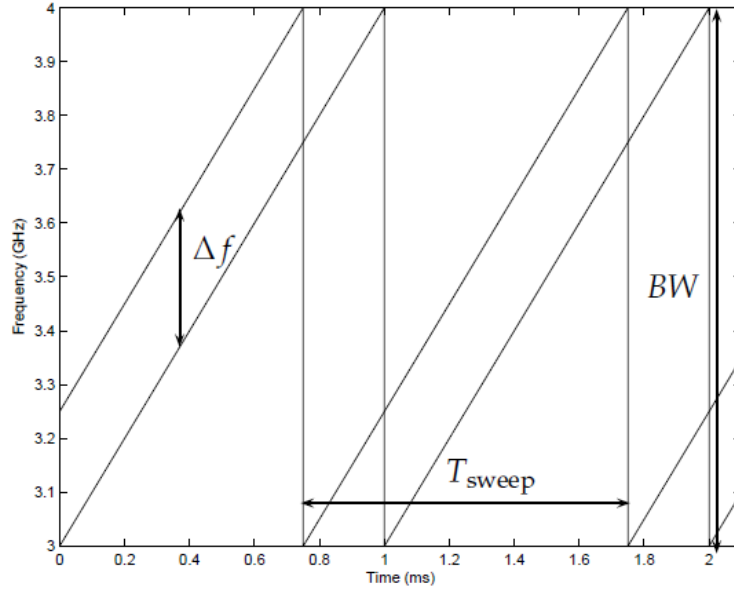
Figure 2-3: FMCW Radar Frequency Sweep Over Time.

Figure 2-3 shows the frequency sweep of the transmitted signal (left) and received signal (right) in a FMCW radar system. In a single sweep period, the transmitted chirp signal can be represented by [9]:

$$s_T(t) = \cos\left[2\pi(f_o + k_f t)t\right] = \cos\left[2\pi(f_o t + k_f t^2)\right] \qquad (2\text{-}1)$$

where f_o is the start frequency of the chirp signal. The received signal is then simply a time delayed version of the transmitted signal:

$$s_R(t) = \cos\left[2\pi(f_o + k_f(t - \Delta t)(t - \Delta t)\right] = \cos\left[2\pi(f_o t - f_o \Delta t + k_f t^2 - 2k_f t\Delta t + k_f \Delta t^2)\right] \quad (2\text{-}2)$$

where Δt is the amount of time it takes for the signal to travel from the transmitter to the object and back to the receiver. The sweep rate k_f can be defined as how much the frequency ranges per unit of time:

$$k_f = \frac{BW}{T_{Sweep}} \qquad (2\text{-}3)$$

where BW is the frequency sweep bandwidth and T_{Sweep} is the time period of the sweep. K_f, which is the slope of the sweep, can then be used along with the frequency difference Δf to find the amount of time Δt the signal has travelled:

$$\Delta t = \frac{\Delta f}{k_f} \qquad (2\text{-}4)$$

The instantaneous frequency difference Δf between the transmitted and received signal is constant for all points in time and is calculated through the usage of a mixer that subtracts and adds the received and transmitted signal frequencies. The received signal can be passed through a low pass filter to remove the higher unwanted frequencies and extract only the difference between the frequencies of the signals. The resulting frequency difference Δf is also known as the beat frequency. The time Δt the signal has travelled can then be used to calculate the distance d the object is from the receiver:

$$d = \frac{\Delta t \cdot c}{2} = \frac{\Delta f \cdot c}{2 \cdot k_f} \qquad (2\text{-}5)$$

Where a factor of 2 is used to account for the round-trip path of the signal and c is the speed of light.

2.3 Overall System

Figure 2-4 shows an overall block diagram of how the design of this chirp signal integrated circuit chip could be used for. The FMCW source signal is at the transmitter side where its signal would be received by 3 antennas in order to perform triangulation and obtain the distance and location of an object through 3 axes. Additional circuits will need to be designed in order to perform amplifying, power division, mixing, filtering, and ADC conversion.
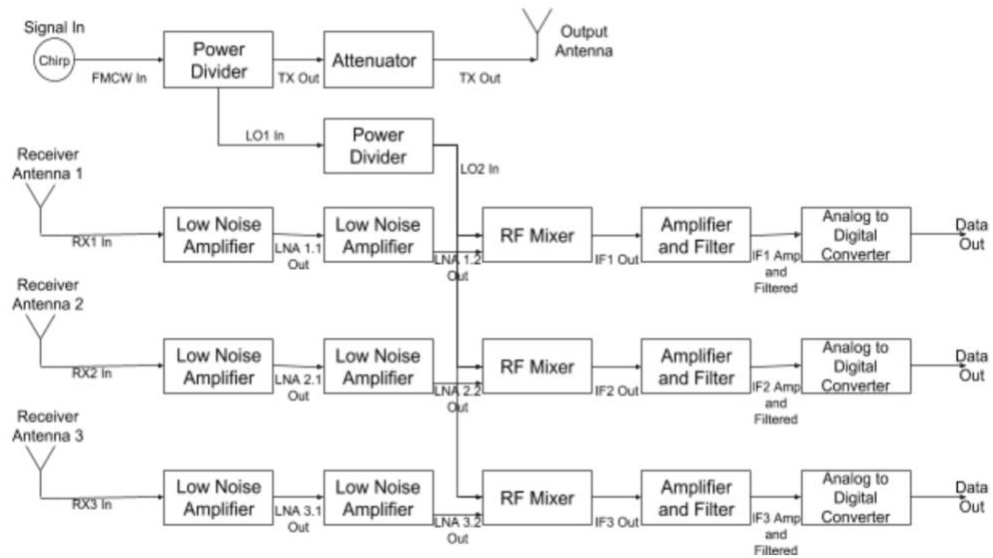
Figure 2-4: Overall System Block Diagram.

Chapter 3

DESIGN

3.1 Design Specifications

The proposed system, shown in Figure 3-1, uses a combination of a voltage ramp signal generator, voltage to current (V-I) converter, and current starved ring oscillator to output a continuous, frequency swept signal at a supply voltage of 1.8V. In addition, the output signal needs to be linearly swept at a time T_{Sweep}, which needs to be more than the size of the room that the signal is transmitting in divided by the speed of light:

$$T_{Sweep} > \frac{Room\ Size}{c} \qquad (3\text{-}1)$$

For this thesis, a room size of 30m is chosen; using Eq. 3-1, a sweep time greater than 100 ns must be used. In practical use, the sweep time must be greater than how long it takes for the signal to travel round trip to the far side of the room and back in order to account for the signal discontinuities occurring at 100ns. There must also be enough time for the transmitted signal to be returned before the chirp signal begins a new sweep; if there is not enough time, the FMCW source frequency becomes invalid, and distance cannot be measured. Therefore, the chosen sweep period is 10 μs. Additionally, as mentioned in Chapter 2, the output signal must be in the allowable FCC frequency range for UWB devices, which is 3.1 to 10.6 GHz, and have a bandwidth of at least 500 MHz. Linearity of the frequency sweep is also important as how much the frequencies of the actual output signal differs from a truly linear line affects the accuracy of the distance measurement. Eq. 2-5 can then be used to determine the accuracy of the distance measurement.
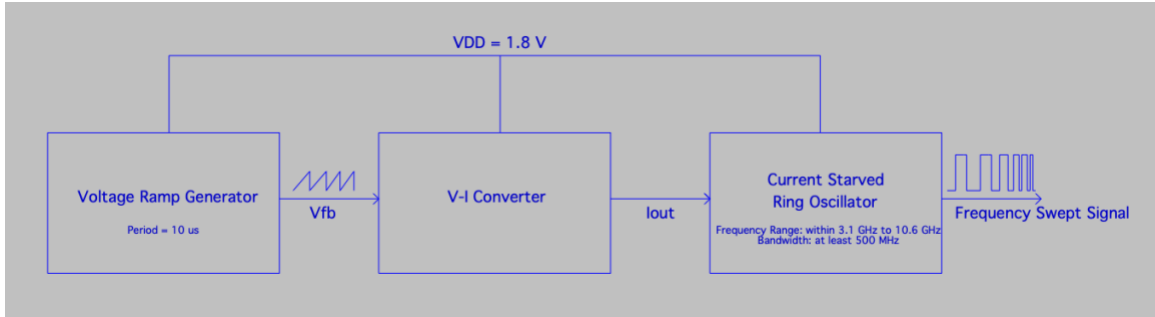
Figure 3-1: FMCW Radar System Block Diagram.

Shown in Figure 3-1, the first stage uses a configuration that repeatedly outputs a ramp control voltage. The second stage takes this control voltage and converts it into a linear increasing output current. This current will be used as an input in the current-starved ring oscillator and allow for a linear, frequency swept square wave signal at the output of the system. The following sections will further explain in-depth the design and configuration of each stages and the overall circuit.

3.2 Voltage Ramp Signal Generator

3.2.1 Theory

The first stage of the proposed system uses a hysteric comparator configuration with a SR latch and feedback network, similar to that of a 555 timer. The basic purpose of this topology is to repeatedly slowly charge and quickly discharge a capacitor every period to generate a linear voltage ramp signal V_{fb}. Figure 3-2 shows the circuit schematic.
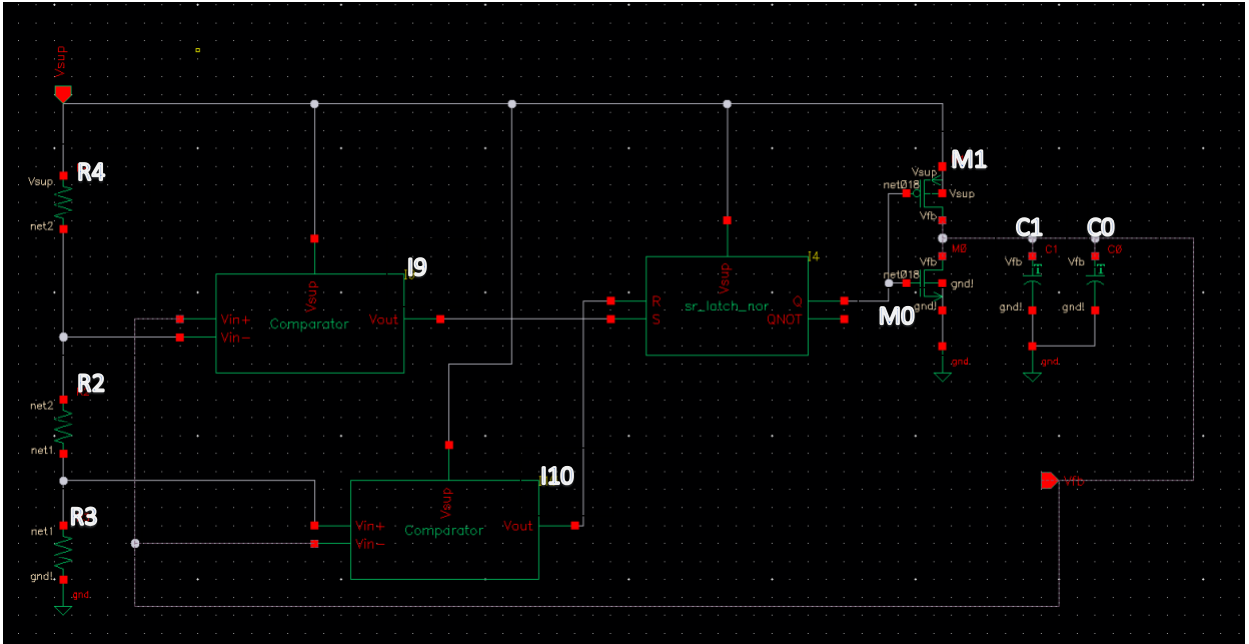
Figure 3-2: Voltage Ramp Signal Generator Circuit.

Shown in Figure 3-2, the NMOS M0 and PMOS M1 forms a constant current source for slowly charging and quickly discharging the capacitor. Figure 3-3 shows the timing diagram of the circuit and the operation is as follows: when the voltage across the capacitor, or V_{fb}, goes below the reference voltage created by R3, reset goes HIGH which causes the output Q of the SR Latch to go LOW; this turns off the NMOS M0 and the node at V_{fb} goes HIGH and charges the capacitor. When the capacitor voltage charges above the R3 reference voltage, both set and reset are LOW, meaning the output Q will hold its previous value (in this case, $Q = 0$); thus, the capacitor will continue to charge. When the voltage across the capacitor goes above the reference voltage created by R2, set goes HIGH which causes the output Q to go HIGH; this turns on the NMOS M0 and the node at V_{fb} goes LOW and discharges the capacitor until it goes back down below the R3 reference voltage, where this process repeats. Therefore, it can be seen that the voltage on the capacitor V_{fb} charges between the R3 and R2 reference voltages for every period.
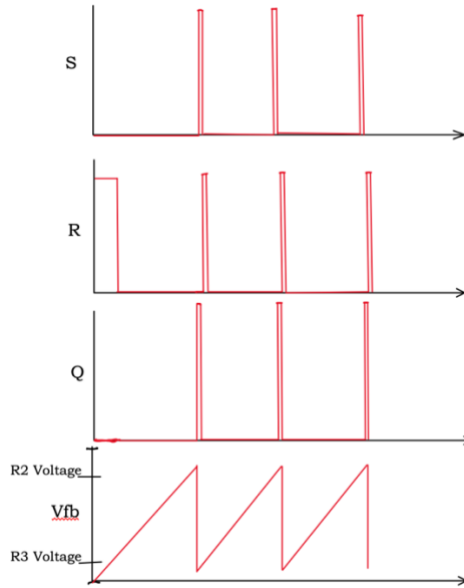
Figure 3-3: Timing Diagram of Ramp Generator Circuit

The circuit begins with a voltage divider network that composes of 3 resistors R2, R3, and R4 to create two reference voltages based off of the supply voltage V_{Sup} of 1.8V. The values of these resistors are important as the reference voltages they create determine the range of voltage on the capacitor node and, therefore, the sweep period; additionally, they also affect the start and stop frequency of the frequency range in the ring oscillator.

The R3 reference voltage is held at the positive (non-inverting) terminal V_{in} + of the I10 comparator while the R2 reference voltage is held at the negative (inverting) terminal V_{in} – of the I9 comparator. These comparators produce a digital voltage that is dependent on the voltages at their input terminals. If $V_{in}+$ is greater than V_{in} -, the comparator's output voltage will be a HIGH or '1'; if V_{in} – is greater than V_{in} +, the comparator's output voltage will be a LOW or '0'. In this circuit, $V_{in}+$ of the I9 comparator and $V_{in}-$ of the I10 comparator are tied together and connected to the feedback voltage V_{fb}. The purpose of the two comparators is to create a hysteresis voltage range, established by the R2 and R3 reference voltages, so that the V_{fb} will repeatedly charge and discharge within the bounds of this range. Figure 3-4 shows the internal schematic of the comparator.

Figure 3-4: Internal Schematic of Comparator.

The outputs of these comparators are then fed to the inputs of the SR Latch which is a data storage device dependent on its Set and Reset inputs. Table 3-1 shows the truth table and operation of the SR Latch. The SR latch circuit was designed using NOR gates and minimum transistor sizes. Q is used as the input for the feedback network whereas Q' is not used. Figure 3-5 shows the schematic design for the SR Latch.

Table 3-1: SR Latch Truth Table.

S	R	Q	Q'
0	0	No Change	No Change
0	1	'0' or LOW	'1' or HIGH
1	0	'1' or HIGH	'0' or LOW
1	1	Invalid Condition	Invalid Condition

Figure 3-5: Internal Schematic of SR Latch using NOR implementation.

Figure 3-6 shows the feedback network portion of the schematic which consists of the PMOS

M1 and NMOS M0 in a CMOS inverter configuration along with capacitors C1 and C0.
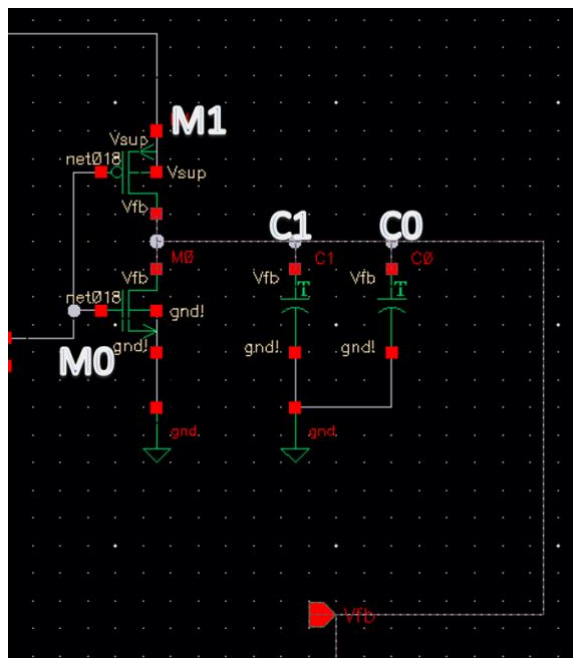
Figure 3-6: Feedback Network Portion of Ramp Generator Circuit.

This configuration allows for fine tuning of the period, charging/discharging time of the capacitor, and linearity of the ramp output voltage. The switching behavior of a CMOS inverter is depicted in Figure 3-7. When the input of the inverter network is LOW, the NMOS is off and the PMOS is on and charges the capacitor at the V_{fb} node. When the input is HIGH, the PMOS turns off and the NMOS turns on and discharges the capacitor. As seen in Figure 3-7, R_n and R_p are the on resistances of the NMOS and PMOS, respectively and the arrows are the current through those transistors [10].
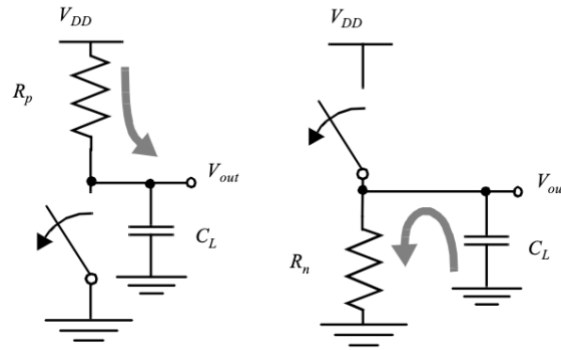
Figure 3-7: CMOS Inverter Switch Model when (left) pMOS charges the capacitor and when (right) nMOS discharges capacitor.

To achieve a repeated ramp signal for every sweep period T_{Sweep} of 10 µs, a slow charging time and fast discharging time are desired; for this project, a discharge time of 1 ns was the target. The current through a capacitor can be defined as [10]

$$i_c = C\frac{\Delta v}{\Delta t} \qquad (3\text{-}2)$$

Where C is the capacitance, Δv is the change of voltage on the output node on the capacitor, and Δt is the change of time for charging or discharging. The time it takes to charge to the capacitor Δt_{charge} and the time it takes to discharge the capacitor $\Delta t_{discharge}$ can then be defined as

$$\Delta t_{charge} = C\frac{\Delta v}{I_{SD}} \qquad (3\text{-}3)$$

$$\Delta t_{discharge} = C\frac{\Delta v}{I_{DS}} \qquad (3\text{-}4)$$

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Where I_{SD} is the source-drain current through the PMOS and I_{DS} is the drain-source current through the NMOS. From these equations, it can be observed that for a long charge time, I_{SD} needs to be small-valued and that for a short discharge time, I_{DS} needs to be large-valued.

3.2.2 Component Values and Transistor Sizing

The starting point is to choose the start and end voltage of the sweep, which is determined by the reference voltages created by the resistor divider network. If R2 = 2.5 kΩ, R3 = 13.3 kΩ, and R4 = 20 kΩ, this produces 0.6687 V at V_{in} + of the I10 comparator and 0.7944 V at V_{in} – at the I9 comparator. Therefore, V_{fb} should theoretically charge from 0.6687 V to 0.7944 V for every period. In reality, due to process variations and delays caused by the capacitances of transistors, resistors, and wires, some errors will be introduced so these values will not be exact. The following calculations will use theoretical values, but further tuning of the transistor sizing will need to be done after simulation to achieve target specifications.

Using Eq. 3-4, for a target discharge time of 1 ns, change of voltage Δv of 0.1257 V (0.7944 V – 0.6687 V), and a 39.8 pF load capacitance, the drain-source current of the nMOS is

$$I_{DS} = C \frac{\Delta v}{\Delta t_{discharge}} = (39.8pF) \frac{0.1257\ V}{1\ ns} = 5\ \text{mA.} \quad (3\text{-}5)$$

Similarly, using Eq. 3-3, for a charge time of 9.999 μs, the source-drain current of the pMOS is

$$I_{SD} = C \frac{\Delta v}{\Delta t_{charge}} = (39.8pF) \frac{0.1257\ V}{9.999\mu s} = 500\ \text{nA.} \quad (3\text{-}6)$$

Although intrinsic capacitances are present in M0 and M1, these are relatively small, in orders of 10^{-15} F, compared to the load capacitance of 39.8 pF. The total capacitance is largely dominated by the load, so calculations can be estimated with the 39.8 pF which will give ballpark estimate value for the transistor sizes.

It can be seen that to require a current of 5 mA through the PMOS is quite large for the process used as this can lead to frying and malfunction of the chip if manufactured. One method to

solve this issue is by adding several PMOS transistors in parallel with M1 so that the current through each transistor is smaller but the total effective current for a required of 5 mA is still met.

By printing the DC Operating Points in the Cadence ADE Simulator Tool, device and model parameters in the TSMC 180nm library can be determined to calculate the needed transistor sizes. Table 3-2 lists the relevant process parameters for the TSMC 180nm.

Table 3-2: NMOS and PMOS Device Parameters in TSMC 180nm Technology.

NMOS M0 parameters	Value	PMOS parameters	Value
μ_n	405.36 cm^2/V*s	μ_p	85.73 cm^2/V*s
C_{ox}	8.42 * 10^{-3} F/m^2	C_{ox}	8.42 * 10^{-3} F/m^2
$k'_n = \mu_n\, C_{ox}$	$390 * 10^{-6}$	$k'_p = \mu_p\, C_{ox}$	$72 * 10^{-6}$
V_{TN}	354.505 mV	V_{TP}	-412.06 mV

Table 3-3: Terminal Voltage Analysis for Operating Regions of NMOS and PMOS.

Region	NMOS	PMOS
Cut Off	$V_{GS} \leq V_{TN}$	$V_{SG} \leq |V_{TP}|$
Linear	$V_{GS} > V_{TN}$, $V_{DS} \leq V_{GS} - V_{TN}$	$V_{SG} > |V_{TP}|$, $V_{SD} \leq V_{SG} - |V_{TP}|$
Saturation	$V_{GS} > V_{TN}$, $V_{DS} > V_{GS} - V_{TN}$	$V_{SG} > |V_{TP}|$, $V_{SD} > V_{SG} - |V_{TP}|$
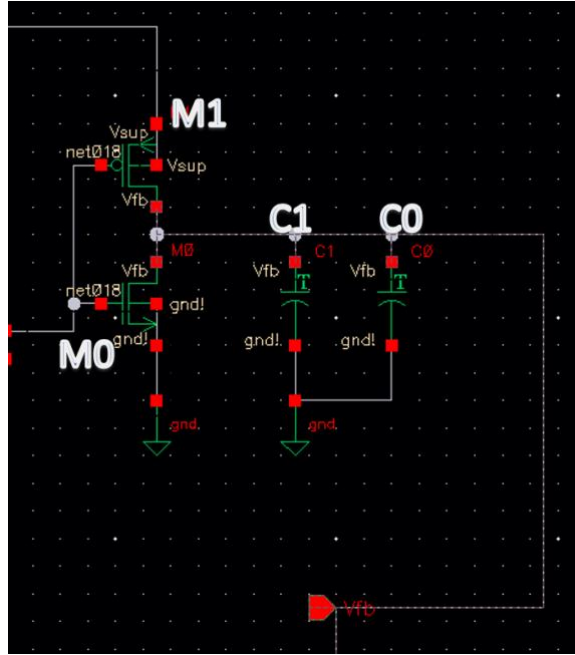
Figure 3-8: Feedback Network Portion of Ramp Generator.

When the capacitor starts to discharge, the NMOS is turned on with a 1.8 V at its gate

terminal. Therefore, the V_{GS} should be 1.8 V with the V_{DS} starts to decrease from 0.7944 V to 0.6687

V. Since $V_{GS} - V_{TN} > V_{DS}$, Table 3-3 shows that M0 is in the linear region. The current equation for

an NMOS in the linear region is defined as [11]

$$I_{DS} = k'_n (W/L)_n [(V_{GS} - V_{TN})V_{DS} - \frac{V_{DS}^2}{2}](1 + \lambda V_{DS}) \qquad (3\text{-}7)$$

Where k'_n, k'_p are the process transconductance parameters, W/L are the width-length channel aspect

ratio, V_{GS}/V_{SG} are the gate-source and source-gate voltages, V_{TN}/V_{TP} are the threshold voltages,

V_{DS}/V_{SD} are the drain-source and source-drain voltages, and λ is the channel length modulation

parameter. Using Eq. 3-7, where the channel length parameter λ is ignored, its channel width-length

ratio is determined to be

$$(W/L)_n = \frac{I_{DS}}{k'_n[(V_{GS} - V_{TN})V_{DS} - \frac{V_{DS}^2}{2}](1 + \lambda V_{DS})} = \frac{5 \text{ mA}}{390 * 10^{-6}[1.8 \, V - 354.505 \, mV)(0.7944 \, V) - \frac{0.7944^2 \, V}{2}](1 + 0V_{DS})} = 15.4$$

$$(3\text{-}8)$$

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Similarly, when the capacitor starts to charge, the PMOS is turned on with a 0 V at its gate terminal. The V_{SG} is then 1.8 V with its V_{DS} starts to increase from 0.6687 V to 0.7944 V. Table 3-3 shows that the M1 PMOS transistor is also in the linear region. The current equation for a PMOS in the linear region defined as [11]

$$I_{SD} = k'_p (W/L)_p [(V_{SG} - |V_{TP}|)V_{SD} - \frac{V_{SD}^2}{2}](1 + \lambda V_{SD}). \qquad (3-9)$$

Using Eq 3-8, its channel width-length ratio is determined to be

$$\left(\frac{W}{L}\right)_p = \frac{I_{SD}}{k'_p[(V_{SG} - |V_{TP}|)V_{SD} - \frac{V_{SD}^2}{2}](1 + \lambda V_{SD})} = \frac{500 \text{ nA}}{72 * 10^{-6}[1.8\,V - 412\ mV)(0.6687\,V) - \frac{0.6687^2\,V}{2}](1 + 0V_{DS})} = 0.01 \quad (3-10)$$

In the final design, M0 has transistor sizes of W = 15.2u and L = 1u while M1 has W = 220n and L = 19.995u. Note that these transistor sizes are not exact as analytical and mathematical determined values as these equations do not accurately represent real life operation and modern CMOS technology devices due to short channel effects and process variations in the models as well as intrinsic and parasitic capacitances in the transistors. M0's $(W/L)_n$ of 15.2 gave better results in simulation as the discharge time was sufficient.

The length of M1 was increased in order to reduce channel length modulation of the capacitor output voltage and exhibit a more linear voltage waveform. Depicted in Figure 3-9, channel length modulation occurs when the channel length decreases by ΔL and the reverse bias depletion region widens for an increase in V_{DS}. Increases in V_{DS} causes the channel pinch-off point to extend away from the drain and move towards the source [12]. Thus, the channel length is thinner at the drain end and is reduced. The channel length modulation parameter in the current equations can also be defined as

$$\frac{\Delta L}{L} = \lambda V_{DS} \qquad (3-11)$$

Channel length modulation shortens the channel and leads to a reduced output resistance and, therefore, an increase in current with drain bias. This effect introduces non-linearity in the current

through the PMOS and, therefore, the voltage sweep. By making L large-valued, the channel length

modulation effect can be reduced as ΔL relatively small to achieve a linear voltage sweep.
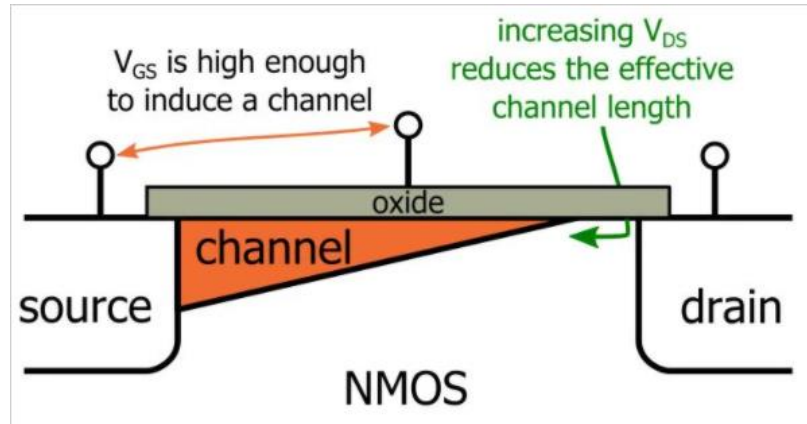
Figure 3-9: Channel Length Modulation Effect.

The load capacitance is 39.8 pF. However, due to sizing limitation for the capacitor cell used,

the maximum capacitance per cell allowed is 1.7919 pF; therefore, C1 is 1.7919 pF with a multiplier

of 20 and C0 is 378.186 fF. Table 3-4 shows the final values and sizes of each component in the

schematic.

Table 3-4: Component Values and Transistor Sizes for Sawtooth Ramp Generator.

Designator	Width W (m)	Length L (m)	Resistance (Ω)	Capacitance (F)
R2	1 μ	6.66 μ	2.50147 k	N/A
R3	1 μ	37.9 μ	13.3034 k	N/A
R4	1 μ	58.1 μ	20.0048 k	N/A
C0	13.365 μ	13.365 μ	N/A	378.86 f
C1	30 μ x 20	30 μ x 20	N/A	1.7919 x 20 = 36.838 p
M0	15.2 μ	1 μ	N/A	N/A
M1	220 n	19.995 μ	N/A	N/A

Figure 3-10 shows the resulting V_{fb} output signal, where it sweeps from 0.6397 V to 0.7842 V. These values will be used in calculations in the following section.
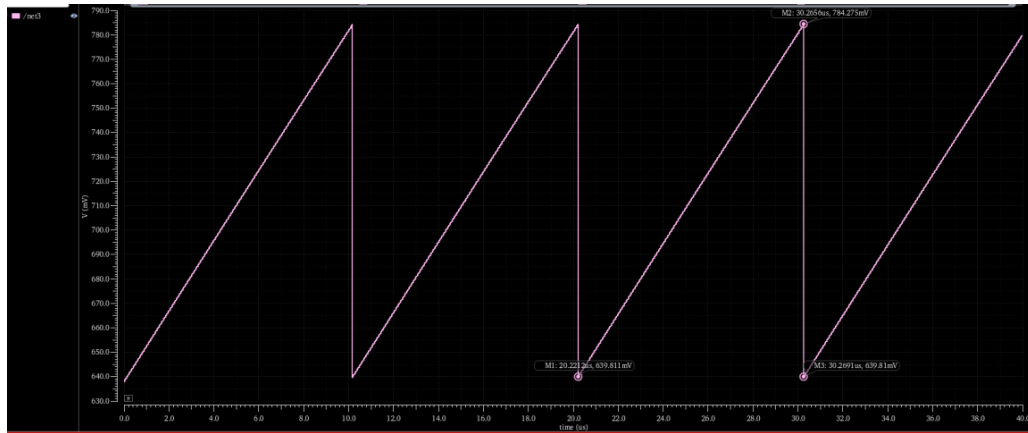
Figure 3-10: Output Voltage of Ramp Generator

3.3 Voltage to Current (V-I) Converter

3.3.1 Theory

The second stage of the system is the V-I converter, shown in Figure 3-11. The basic working principle of this circuit is to hold an NMOS in the linear region where it will convert its V_{GS} to current linearly. This is done by using a high gain op-amp configuration formed from a Common-Gate (CG), Common-Source (CS), and PMOS current mirror to create a constant V_{DS} across the NMOS. A transistor in the linear region with a constant V_{DS} will linearly convert its V_{GS} to a proportional current. The input to this stage is the ramp sweep voltage created by the circuit described in Chapter 3.2 and converts that voltage into a linear current I_{OutN}.
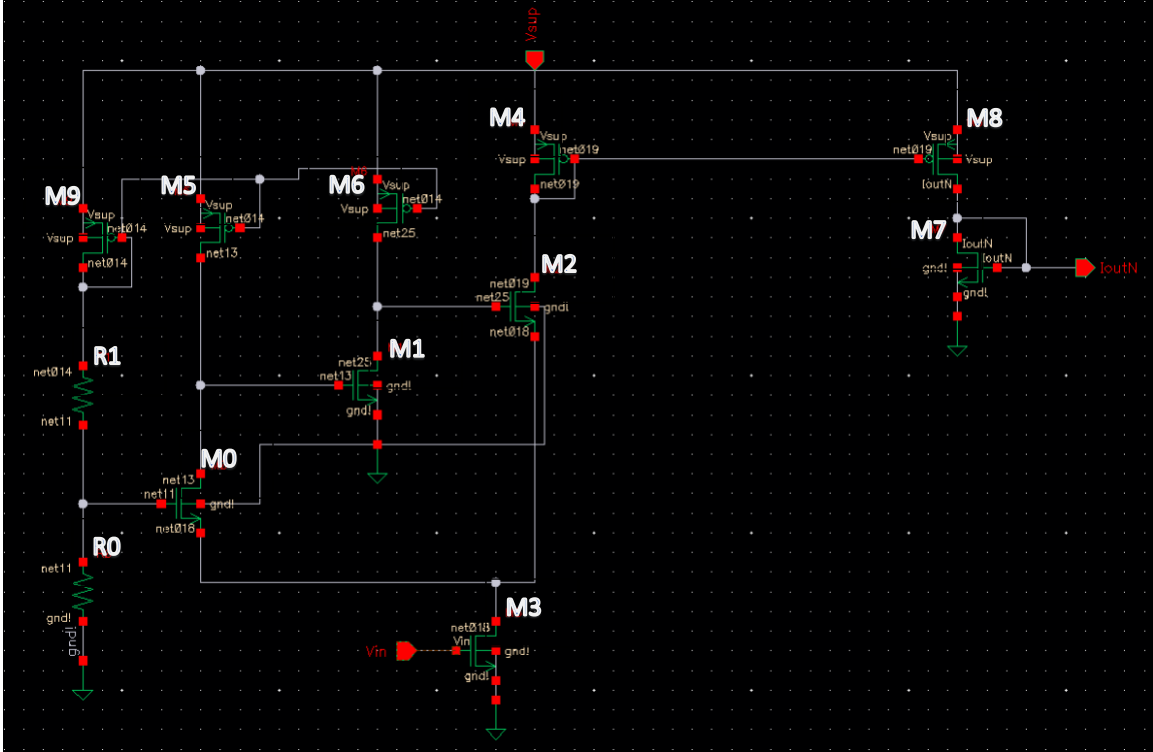
Figure 3-11: Schematic of V-I Converter.

By keeping M3 in the linear region, the V_{GS}, which is a linear ramp voltage signal from the previous stage, can be used to obtain a linear current through M3. A NMOS is defined to be in the saturation region as [11]

$$V_{DS} > V_{DSAT} \text{ where } V_{DSAT} = V_{GS} - V_{TN} \text{ (3-12)}$$

For a NMOS and a PMOS in the saturation region, their respect current equations are [11]

$$I_{DS} = \frac{1}{2}k'_n(W/L)_n(V_{GS} - V_{TN})^2(1 + \lambda V_{DS}) \qquad \text{(3-13)}$$

$$I_{SD} = \frac{1}{2}k'_p(W/L)_p(V_{SG} - |V_{TP}|)^2(1 + \lambda V_{SD}) \qquad \text{(3-14)}$$

Where V_{DS} is the drain-source voltage, V_{GS} is the gate-source voltage, and V_T is the threshold voltage. Therefore, in order to guarantee that the transistor stays in the linear region, the V_{DSAT} must be made large enough so that the V_{DS} is never greater than the V_{DSAT}. Solving for V_{DSAT} from Eq. 3-13, ignoring the channel length modulation parameter,

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$$V_{DSAT} = V_{GS} - V_T = \sqrt{\frac{2 \cdot I_{DS} \cdot L}{k'_n \cdot W}}. \quad (3\text{-}15)$$

Therefore, increasing the channel length L will give a large valued V_{DSAT} and keep the transistor in the linear region. There is very little change on the drain voltage of M3 so it can be assumed that it is held constant theoretically. Figure 3-12a shows the relationship between the V_{GS} and I_{DS} of a NMOS transistor for a constant V_{DS} [13]. For this circuit, since the V_{GS} is a linear increasing voltage signal, the V_{DS} will be less than $V_{GS} - V_T$, which produces a linear I_{DS} current.
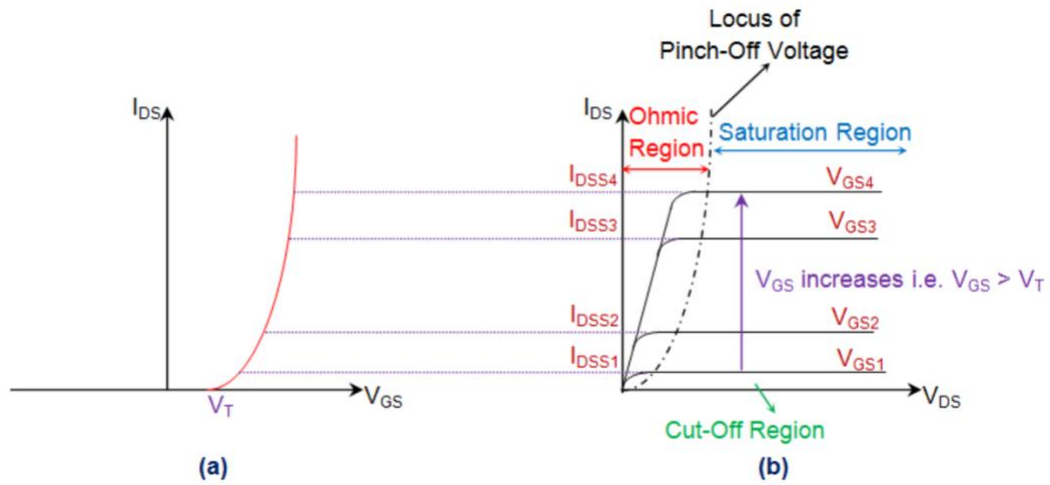
Figure 3-12: (a) Transfer Characteristics and (b) Output Characteristics Curve of a NMOS.

Another functionality of this circuit is to mirror and output that current to the next stage. M0 and M1 form a Common-Gate (CG) and Common-Source (CS) amplifier where they are actively loaded by M5 and M6 in order to produce a high output resistance and gain. The currents through the active loads are mirrored from the M9 transistor. M0 is biased at a fixed voltage set by the R1 and R2 voltage divider network. If V_{IN} linearly increases, more current will be provided through the M3 transistor; this means that the V_{GS} of M0 will also increase by decreasing its source voltage V_s due to the fact that V_G is at a constant voltage. In a CG amplifier, the source terminal of the transistor serves as the input voltage, the drain terminal is output voltage, and the resulting open-circuit voltage gain is large and non-inverting. Therefore, since the change of voltage at the source terminal of M0 is decreasing in the negative direction, the output of M0 will also be negative and large. CS amplifiers take the input at the gate terminal, the output at the drain terminal, and the open-circuit voltage gain is

also be large but inverting. Since the input voltage is negative, M1 will invert it and output a large and positive voltage gain. The voltage change across the V_{GS} of M2 is then a factor of the gain of the CG and CS amplifier more than the change of V_{GS} across M0. This allows most of the current through M3 to go through M2 instead of through M0.

M4, M8, and M7 form a current mirror configuration where the current through M4, which is the current through M2, is mirrored to M8. M7 is then used to take this current I_{OUTN} to feed it to the next stage of the ring oscillator.

3.3.2 Component Values and Transistor Sizing

M0, M1, and M2 is set at minimum size whereas active loads M5 and M6 have W = 13 μm in order to exhibit the large gain that these amplifiers need to have. M9 acts as current mirror to bias each of the active load transistors. R0 and R1 form a resistor divider each with a resistance of 2.41 kΩ to bias the M0 transistor.

In order to size M3 to be in the linear region, its V_{DS} must be determined. Using Eq. 3-12, the V_{GS} of M0 can be reworked as

$$V_{GS,M0} = V_{DSAT,M0} + V_{TN,M0} \qquad (3\text{-}16)$$

The source voltage $V_{S,\,M0}$ of M0 is defined as

$$V_{S,M0} = V_{G,M0} - V_{GS,M0} = V_{Bias} - V_{GS,M0} \qquad (3\text{-}17)$$

Where its gate voltage V_G is biased voltage V_{Bias} set by the R0 and R1 resistors. Eq. 3-16 can then be substituted into 3-17 where

$$V_{S,M0} = V_{Bias} - V_{DSAT,M0} - V_{TN,M0} = V_{Bias} - V_{TN,M0} \,. \qquad (3\text{-}18)$$

Theoretically, the most of the current through M3 should flow through the right branch where M2 is and none should go through M0. If there isn't any current flowing through M0, its $V_{DSAT,\,M0}$ should also be zero so its source voltage $V_{S,M0}$ is then a constant voltage set by V_{Bias} and its threshold voltage V_{TN}. Additionally, the source voltage of M0 is also the V_{DS} of M3. Therefore,

$$V_{DS,M3} = V_{Bias} - V_{TN,M0} \ . \qquad (3\text{-}19)$$

Since V_{Bias} is set at 0.56 V, then using Eq. 3-19, the V_{DS} of M3 is 0.206 V. From here, the linear

current equation of an NMOS from Eq. 3-7 can then be used to find the channel width-length ratio of

M3. If the chosen starting current of the sweep is 2 μA, then

$$(W/L)_{n,M3} = \frac{I_{DS}}{k'_n[(V_{GS}-V_{TN})V_{DS}-\frac{V_{DS}^2}{2}](1+\lambda V_{DS})} = \frac{2 \ \mu A}{390*10^{-6}[0.639 \ V-354.505 \ mV)(0.206 \ V)-\frac{0.206^2 \ V}{2}](1+0V_{DS})} = 0.5 \qquad (3\text{-}20)$$

This aligns with the theory that L needs to be larger than the W of the transistor to force its operation

in the linear region. M3 with W = 1 μm and L = 2 μm allows the transistor to stay in the linear region

as the V_{GS} is swept from 0.6397 V to 0.7842 V. To verify that M3 was indeed in the linear region, DC

operating point analysis was done by comparing the minimum and maximum V_{GS} points with the

corresponding V_{DS}. Figure 3-13 shows I_{DS}, $V_{GS,}$ and the V_{DS} of M3. At the minimum,

$$V_{GS} = 639.7 \ mV, V_{DS} = 206.15 \ mV$$

$$V_{DS} = 206.15 \ mV < \ V_{GS} - V_{TN} = \ 639.7 \ mV - 354.5 \ mV = 285.2 \ mV \quad (3\text{-}21)$$

At the maximum,

$$V_{GS} = 784.2 \ mV, V_{DS} = 173.7 \ mV$$

$$V_{DS} = 173.7 \ mV < \ V_{GS} - V_{TN} = \ 784.2 \ mV - 354.5 \ mV = 429.7 \ mV \quad (3\text{-}22)$$

At both points, the V_{DS} is less than the V_{DSAT} so it can be confirmed that M3 is in the linear region.
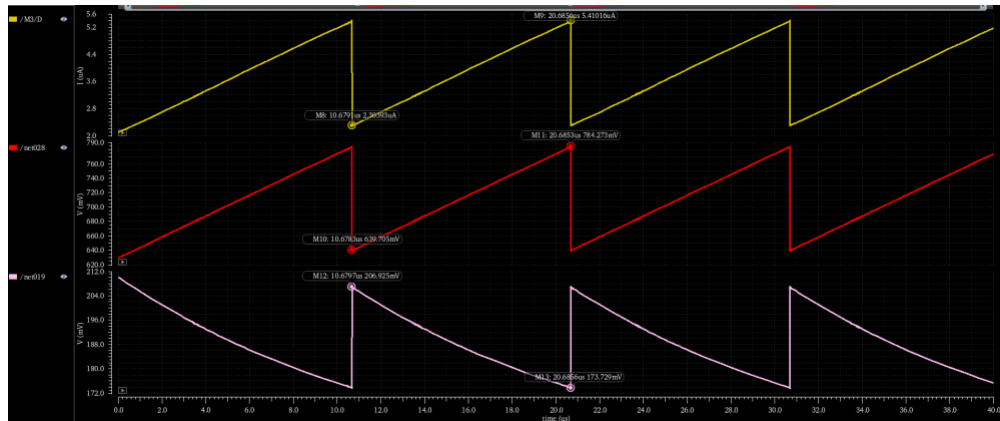
Figure 3-13: IDS (yellow), VGS (red), and VDS (purple) of M3.

Shown in Figure 3-14, M4 and M8 form the current mirror where their widths are doubled relative to the width the M2 transistor to match the ratio of their mobilities and to equate the propagation delays. M7 is set at minimum sized. Table 3-5 shows the final transistor sizes.
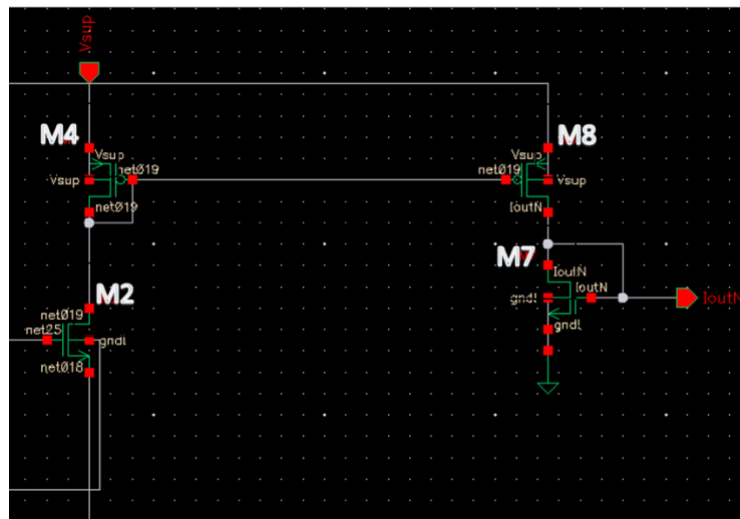
Figure 3-14: Current Mirror Portion of V-I Converter.

Table 3-5: Component Values and Transistor Sizes for V-I Converter.

Designator	Width W (m)	Length L (m)	Resistance (Ω)
R0	1 μ	6.64 μ	2.41522 k
R1	1 μ	6.64 μ	2.41522 k
M0	2 μ	180 n	N/A
M1	2 μ	180 n	N/A
M2	2 μ	180 n	N/A
M3	1 μ	2 μ	N/A
M4	4 μ	180 n	N/A
M5	13 μ	180 n	N/A
M6	13 μ	180 n	N/A
M7	2 μ	180 n	N/A
M8	4 μ	180 n	N/A
M9	2 μ	180 n	N/A

Figure 3-15 shows that the output current I_{OUT} increases from 3.34 μA to 7.288 μA. These values will be needed for calculations in the next section.

Figure 3-15: Output Current IOUT (red) and Vfb (blue) from the Ramp Generator.

3.4 Current Starved Ring Oscillator

Voltage controlled oscillators (VCO) are electronic devices that are able to generate a repeating signal at specific oscillation frequency and can be designed to transmit the FMCW chirp signal [14]. This particular frequency is controlled and varied by a voltage input. VCOs a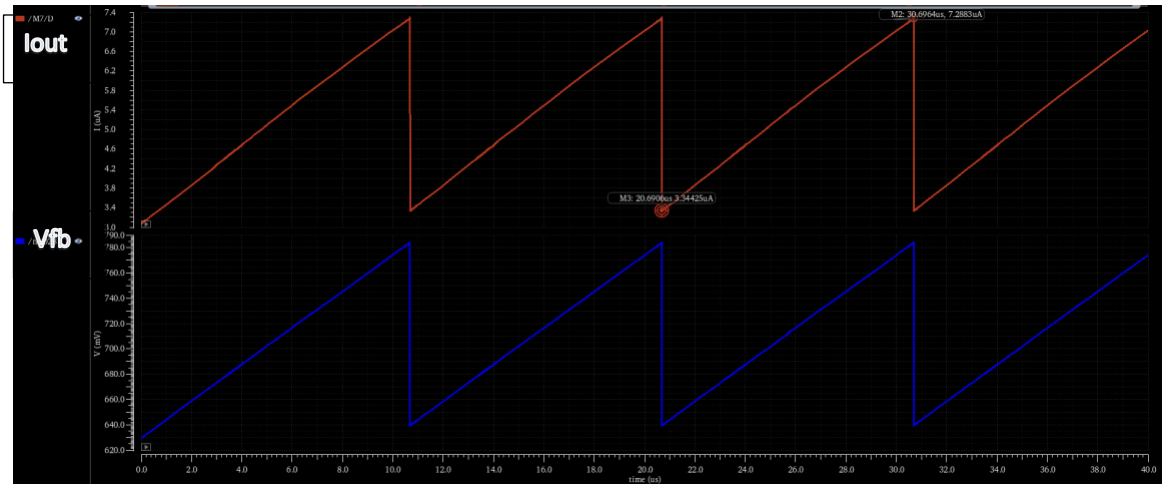re key components in wireless communication systems as they have low power consumption, high frequency applications, good phase and frequency stability, and linearity of frequency vs. control voltage. The ring oscillator, a type of VCO, uses an odd number N of inverters connected in series where the output of the Nth stage inverter is feedback to the first stage inverter; its output oscillates between two voltages levels of either one or zero. Figure 3-16 shows a 3-stage ring oscillator where N is 3.
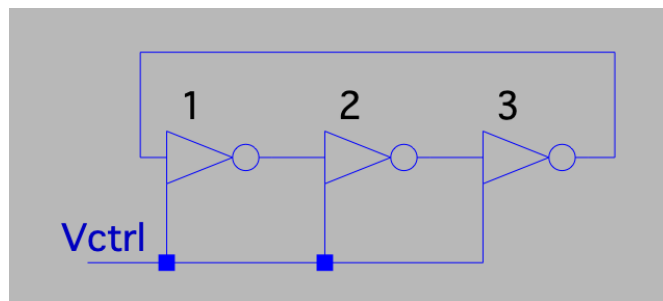

Figure 3-16: 3 Stage Voltage Controlled Ring Oscillator.

3.4.1 Theory

The final stage is the ring oscillator, shown in Figure 3-17, which uses a topology of 3 inverters, each starved by a current sink NMOS transistor. The idea behind this circuit is to control the

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delay of each inverter stage, and therefore the oscillation frequency, by controlling the amount of current to charge and discharge the load capacitance of each stage and, therefore, how quickly the node voltages between inverters change. The input bias current I_{inN} is mirrored by a current mirror to each current sink transistors and the current available to each inverter is limited by these current sink transistors. For example, in the first stage, M0 and M3 operate as an inverter where the current through these transistors is limited by the current sink transistor M7. The amount of current the inverter wants to draw is then limited by the current sunk by the M7 transistor and is kept under than this amount. Hence, the inverter is starved for current.
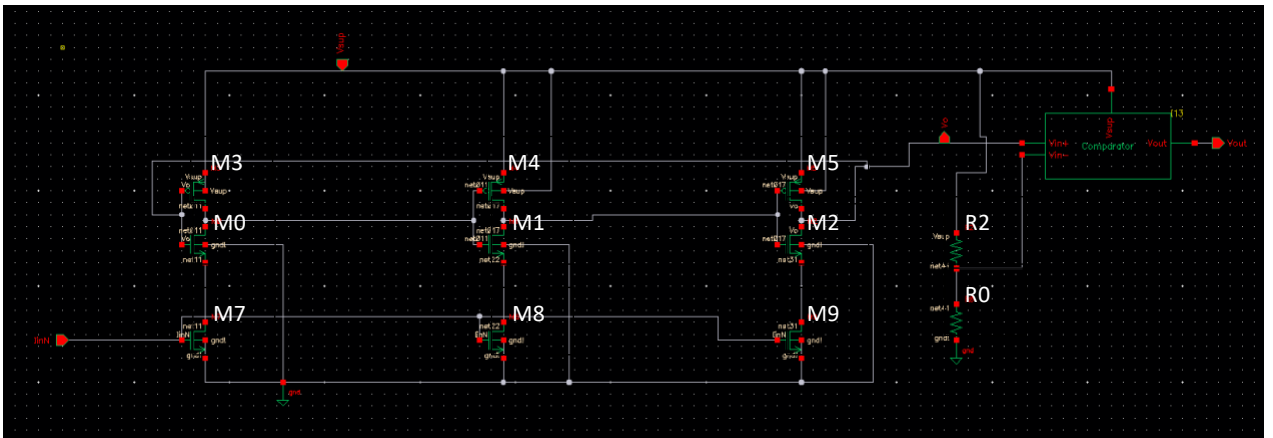
Figure 3-17: Current-Starved Ring Oscillator Circuit.

The oscillation frequency of the ring oscillator can be defined as [15]

$$f_{osc} = \frac{1}{2Nt_p} \qquad \text{(3-23)}$$

Where N is the number of inverter stages and t_p is the propagation delay of each stage. From this equation, to obtain a higher oscillation frequency, the number of stages should be minimized as much as possible. This equation can be further broken down to

$$f_{osc} = \frac{1}{(N \cdot t_{pHL}) + (N \cdot t_{pLH})} \qquad \text{(3-24)}$$

Where t_{pHL} is the time it takes for an inverter to transition a '1' to a '0' and t_{pLH} is the time it takes for an inverter to transition a '0' to a '1'. Dynamic metrics such as propagation delay depends on the capacitance

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at the output nodes of each inverter. For each inverter charging and discharging, the charge on that

output capacitor is defined as [10]

$$Q = C \cdot V \qquad (3\text{-}25)$$

Where V is the voltage of the capacitor and C is the capacitance. Taking the derivative of Eq. 3-25,

the current I after each transition in the active region can defined as

$$I = C \frac{\Delta V}{\Delta t} \qquad (3\text{-}26)$$

Where ΔV is the change of the output voltage on the inverter and Δt is the time it takes for the inverter

to transition. Rearranging Eq. 3-26 gives

$$\Delta t = \frac{C \cdot \Delta V}{I}. \qquad (3\text{-}27)$$

The output voltage node of each inverter detects a change or transition when the output voltage is

equal to the input voltage; this voltage can be called V_M. Therefore, V_M can be substituted into Eq. 3-

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$$\Delta t = \frac{C \cdot V_M}{I}. \qquad (3\text{-}28)$$

The entire ring oscillator can then be analyzed by finding the delay at the individual output node of

each inverter. As explained in Chapter 3.2.1, when a digital '0' is at the input of an inverter, the

NMOS is turned off while the PMOS is turned on and current through the PMOS charges the

capacitance at the output node; when a digital '1' is at the input of the inverter, the PMOS is turned off

while the NMOS is turned on and current through the NMOS discharges the capacitance at the output

node. Therefore, replacing Δt with the respective transitions, the low to high (charging) and high to

low (discharging) delay times are

$$t_{pLH} = \frac{C \cdot V_M}{I_P} \qquad (3\text{-}29)$$

$$t_{pHL} = \frac{C \cdot V_M}{I_N} \qquad (3\text{-}30)$$

Where I_P is the current through the PMOS and I_N is the current through the NMOS. However, due to

the current starved configuration, the current drawn through the NMOS is limited by the current I_D

through the current sink transistors. Using Eq. 3-29 and Eq. 3-30 with I_N replaced by I_D, the oscillation frequency can now be estimated further

$$f_{osc} = \frac{1}{\left(N \cdot \frac{C \cdot V_M}{I_P}\right) + \left(N \cdot \frac{C \cdot V_M}{I_D}\right)} \qquad (3\text{-}31)$$

It can be seen that increasing the current through each current sink transistor will lower their respective transition times, resulting in a faster oscillation frequency. The total capacitance on the drains of the transistors in each inverter is given by [14]

$$C = C_{out} + C_{in} = (C_{DBn} + C_{DBp} + 2C_{GDOn}W_n + 2C_{GDOp}W_p) + (\frac{2}{3}C_{ox}W_nL_n + C_{GDOn}W_n +$$

$$C_{GSOn}W_n + \frac{2}{3}C_{ox}W_pL_p + C_{GDOp}W_p + C_{GSOp}W_p) \quad (3\text{-}32)$$

This is simply the sum of the output and input capacitances of the inverters where C_{ox} is the oxide capacitance of the transistor, C_{DB} is the diffusion-bulk capacitance, C_{GDO} is the gate-drain overlap capacitance, and C_{GSO} is gate-source overlap capacitance.

The output signal V_o of the ring oscillator is sent to a comparator at the end of the circuit so the signal can be amplified and go rail to rail from 0 V to 1.8 V. This also gives a square wave output at V_{OUT} whereas V_o is a sine wave output. V_o is compared against a reference voltage at the $V_{IN\text{-}}$ node, which is formed by the resistor divider network, of the comparator.

3.4.2 Component Values and Transistor Sizing

This circuit uses minimum sized transistors with $W = 2\ \mu m$ and $L = 180$ nm for each inverter for a total of 3 inverters. The ratio of the PMOS W/L and the ratio of the NMOS W/L can be made to be the ratio of the mobilities to equate the high to low and low to high propagation delays. In this case, the width of the PMOS was reduced in order the speed up the inverter by reducing parasitic capacitances and therefore, lowering the high to low transition time. Table 3-6 shows the parasitic capacitances of the process, which were obtained by performing DC operating points in ADE.

Table 3-6: Obtained Intrinsic Capacitances of MOSFETs.

Capacitor	Value
C_{GDOn}	$7.7 \cdot 10^{-10} F/m$
C_{GDOp}	$7.11 \cdot 10^{-10} F/m$
C_{GSOn}	$7.7 \cdot 10^{-10} F/m$
C_{GSOp}	$7.11 \cdot 10^{-10} F/m$
C_{DBn}	$1.5 \, fF$
C_{DBp}	$1.72 \, fF$

Using Eq. 3-32, the total capacitance on the drains of the transistors in each inverter can then be estimated as

$$C = (1.5 \, fF + 1.72 \, fF + 2 \cdot 7.7 \cdot 10^{-10} F/m \cdot 2um + 2 \cdot 7.11 \cdot 10^{-10} F/m \cdot 2u) + \frac{2}{3} \cdot 8.42 \cdot$$

$$10^{-3} \text{ F/m} \cdot 2u \cdot 180nm + 7.7 \cdot 10^{-10} F/m \cdot 2um + 7.7 \cdot 10^{-10} F/m \cdot 2u + \frac{2}{3} \cdot 8.42 \cdot 10^{-3} \text{ F/m} \cdot$$

$$2u \cdot 180nm + 7.11 \cdot 10^{-10} F/m \cdot 2u + 7.11 \cdot 10^{-10} F/m \cdot 2u) = 19fF \qquad (3\text{-}33)$$

The current I_p through the PMOS is

$$I_P = k'_p (W/L)_p [(V_{SG} - |V_{TP}|)V_{SD} - \frac{V_{SD}^2}{2}](1 + \lambda V_{SD}) = 390 * 10^{-6}(2\mu/180nm)[(1.45 -$$

$$0.412 \, V)(0.1) - \frac{0.1^2}{2}] = 79 \, \mu A \ (3\text{-}34)$$

In order to size for the current sink transistors, the amount of current limited to the NMOS needs to be determined. A starting frequency can then be chosen to find $I_{D,start}$ using Eq. 3-26, as long as it is within the FCC allowable frequency range. For a start frequency of 3.4 GHz, the drain current needed to achieve the starting frequency is

$$f_{start} = \frac{1}{\left(N \cdot \frac{C \cdot V_M}{I_P}\right) + \left(N \cdot \frac{C \cdot V_M}{I_{D,start}}\right)}$$

$$3.4 \; GHz \; = \frac{1}{\left(3 \cdot \frac{19 \; fF \cdot 0.2}{79 \; \mu A}\right) + \left(3 \cdot \frac{19 \; fF \cdot 0.2}{I_{D,start}}\right)}$$

$$I_{D,start} \; = \; 76 \; \mu A \qquad (3\text{-}35)$$

Due to the fact that the current through each current sink transistor is mirrored from the output linear current of the V-I converter and that the start current of the output current from the V-I converter is only 3.34 μA, the channel width-length of these transistors must be scaled to achieve the required current. The current can be increased by increasing the W/L of the transistor where the current is being mirrored. Figure 3-18 depicts the current relationship in a NMOS current mirror.
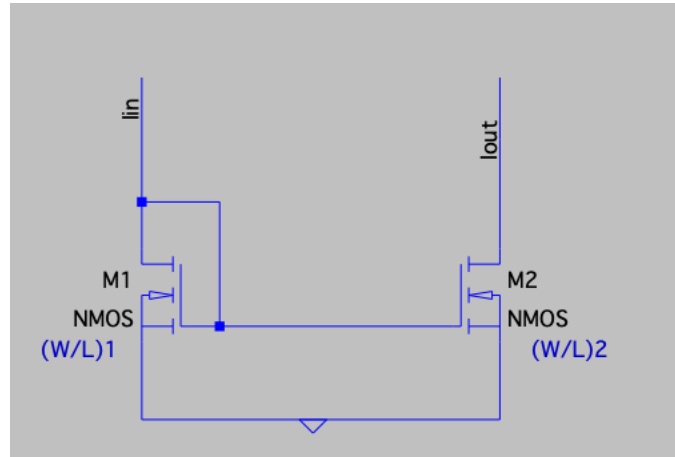

Figure 3-18: NMOS Current Mirror.

This relationship can be denoted as

$$I_{out} \; = \; \frac{(W/L)_2}{(W/L)_1} I_{in} \qquad (3\text{-}36)$$

Where I_{out} is the mirrored current, I_{in} is the input current in the current mirror, $(W/L)_2$ is the size of the transistor of the mirrored current and $(W/L)_1$ is the size of the transistor of the input current. Since the currents are known and $(W/L)_1$ is known from the V-I converter, I_{out} can be replaced with I_D and the size of the current sink transistors can then be estimated as

$$(W/L)_2 = \frac{I_D(\frac{W}{L})_1}{I_{in}} = \frac{76 \; \mu A(\frac{2\mu}{180nm})_1}{3.34 \; \mu A} = \frac{45.5 \; \mu}{180 \; nm} \qquad (3\text{-}37)$$

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To verify that the oscillator has a 500 MHz bandwidth as required, the stop frequency can be determined. The stop current from the output current of the V-I converter is 7.288 μA. The current mirrored to the current sink transistors, and therefore starving the inverter, at the stop frequency is

$$I_{D,stop} = \frac{(45.5\mu/180nm)_2}{(2u/180nm)_1} \cdot 7.288 \; \mu A = 165.802 \; \mu A \qquad (3\text{-}38)$$

Then, the stop frequency is

$$f_{stop} = \frac{1}{\left(N \cdot \frac{C \cdot V_M}{I_P}\right) + \left(N \cdot \frac{C \cdot V_M}{I_{D,stop}}\right)} = \frac{1}{\left(3 \cdot \frac{19 \, fF \cdot 0.2}{79 \; \mu A}\right) + \left(3 \cdot \frac{19 \, fF \cdot 0.2}{165.802 \; \mu A}\right)} = 5.4 \; GHz \qquad (3\text{-}39)$$

This shows that the resulting frequency range will increase from 3.4 GHz to 5.4 GHz with a bandwidth of about 2 GHz for each sweep period, which meets design specifications theoretically. Note that these equations give the ballpark values, and that further iteration and transistor size tuning will need to be done in reality due to short channel effects. Table 3-7 shows the resulting transistor sizes of the ring oscillator circuit.
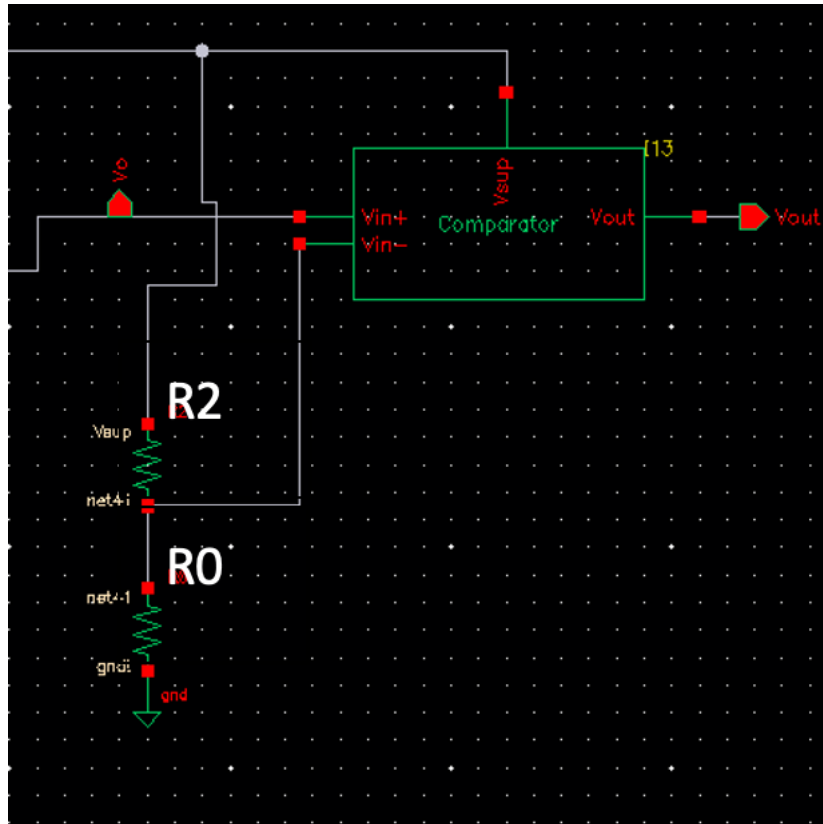
Figure 3-19: Resistor Divider and Comparator Network of Ring Oscillator.

As shown in Figure 3-19, R2 and R0 form a resistor voltage divider network that outputs 1.1

V in the V_{in} - node of the comparator. In simulation, it was seen that V_o oscillated between 1.7 V and

0.6 V; these resistors were sized and chosen so that when V_o oscillated above 1.1 V, the output V_{out} of

the comparator goes high to 1.8 V and when V_o oscillated down below 1.1 V, V_{out} goes low to 0 V.

Table 3-7: Transistor Size and Component Values for Ring Oscillator.

Designator	Width W (m)	Length L (m)	Resistance (Ω)
R0	1 μ	28.83 μ	10.0024 k
R2	1 μ	45.84 μ	15.5 k
M0, M1, M2, M3, M4, M5	2 μ	180 n	N/A
M7, M8, M9	34 μ	180 n	N/A

3.5 Final Circuit

3.5.1 Design

After circuit design of each stage were complete, a new cell was created in order to incorporate all cells of each circuit into a single schematic, as shown in Figure 3-20. Critical inputs and outputs of each stage were connected as desired with two output pins for V_o and V_{OUT} and supply pin for V_{SUP} for monitoring in simulation.
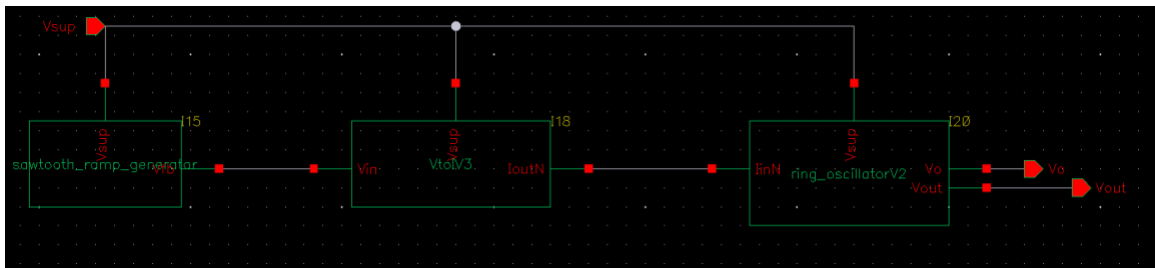

Figure 3-20: FMCW System Circuit.

3.5.2 Layout

Good layout design can greatly affect the performance of the circuit due to intrinsic parasitics found in transistors and other components. Certain transistor layout techniques can help minimize these parasitics, minimize delays, and optimize performance. The TSMC 180nm technology allows for the channel length of the transistors to be as small as 180nm. Figure 3-21 shows a 3D model of a NMOS transistor where the channel length L is the distance between the two n^+ doped regions and the channel width W is the distance by which the gate stretches across this channel [16].
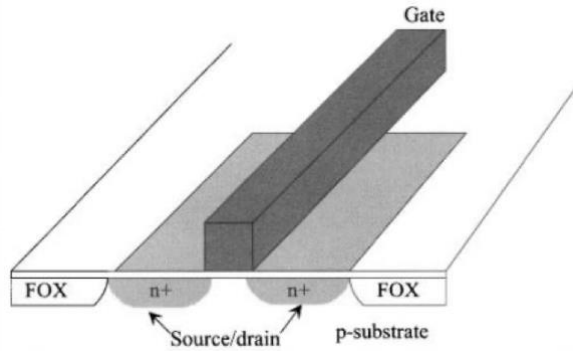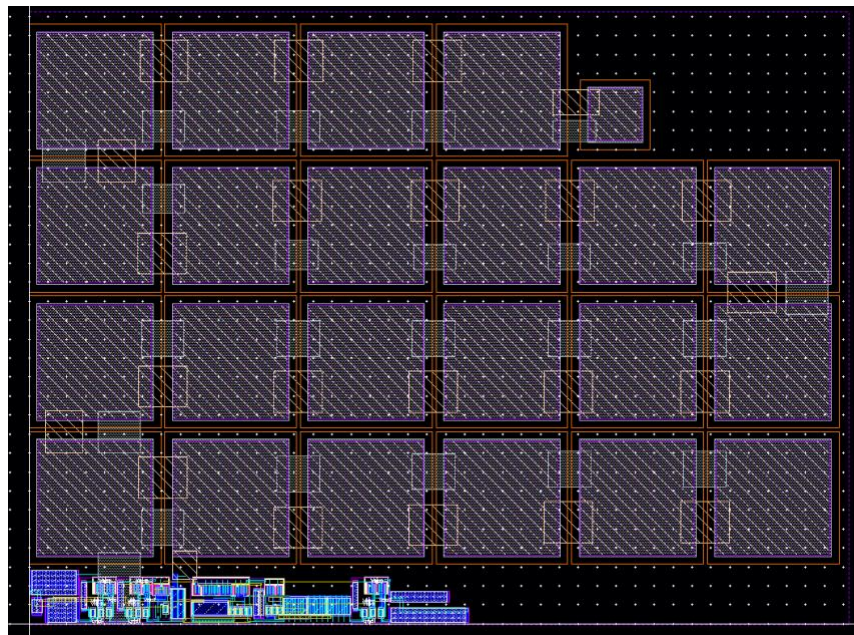
Figure 3-21: 3D Model of NMOS transistor.

Figure 3-22: Complete Layout of FMCW System before IO pads addition.

Figure 3-22 shows the layout of the final circuit before the addition of IO pads. Layout design is typically done in three different ways: full custom, semi-custom, and automatic. For this project, layout was done using the semi-custom option where parameterized cells (PCELLS) of each component in the schematic are automatically generated so only physical wiring and placement of the cells are manually done. PCELLS are SKILL programs that can automatically generate components dependent on the user input parameters. Additionally, layout was done by stages and then routed at the end. Figure 3-23 shows the layout of each individual stages. Components are placed similarly to where they are in the schematic.
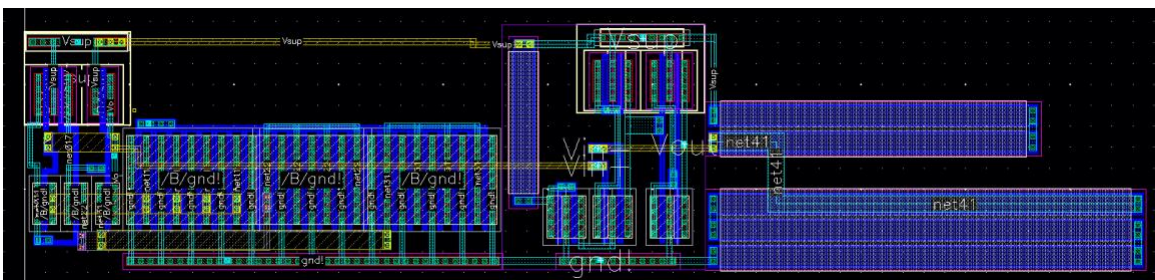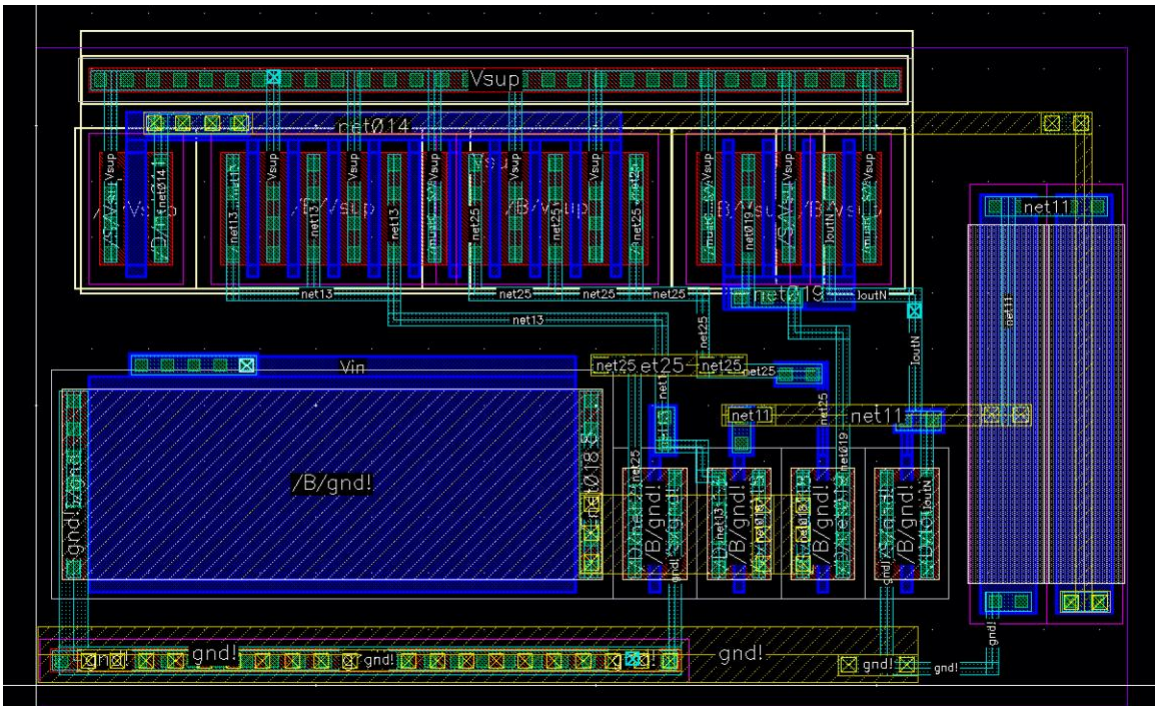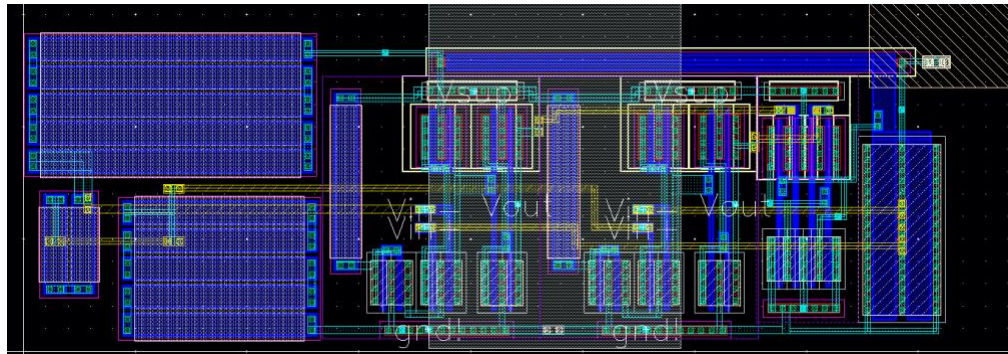
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Figure 3-23: Layout of each stage where (top) is the sawtooth generator layout, (middle) is the V-I Converter layout, and (bottom) is the ring oscillator layout.

A technique used in this layout was fingering of the transistors. Fingering allows for the

effective length and width to stay the same but folds more gates in parallel so that long transistors can

be split into a square shape instead of an elongated shape, which reduces source and drain area, and therefore, reduces capacitance [17]. Figure 3-24 shows M5, in the V-I converter, with total effective width W of 13 μ split into 5 fingers each with a width of 2.6 μ. This allows for a more even and symmetric layout and area of the circuit, rather than just a long transistor.
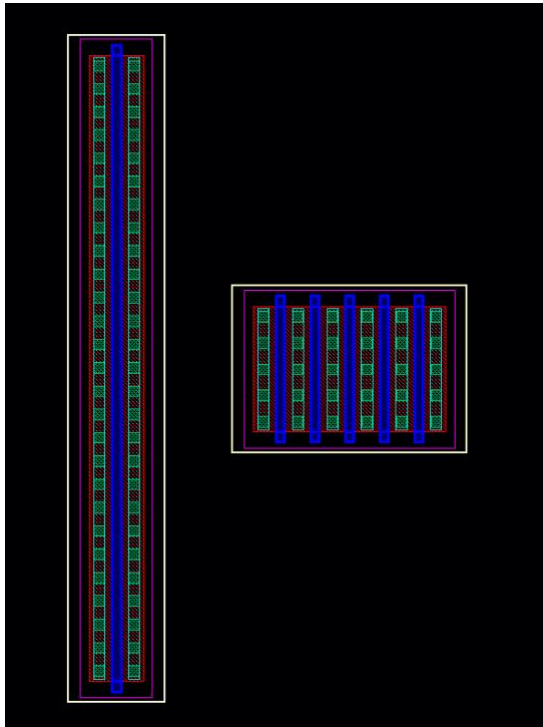

Figure 3-24: (Left) PMOS with No Fingers and (Right) PMOS with 5 Fingers.

Drains and sources of the MOSFETs are connected by either chaining or through the metal1 layer. Chaining is a technique that allows transistors with the same source and drain net connections to be overlapped. Figure 3-25 shows an example where two transistors are chained and overlapped on the same net connection without the use of a metal1 path. This simplifies routing and reduces chip layout area.
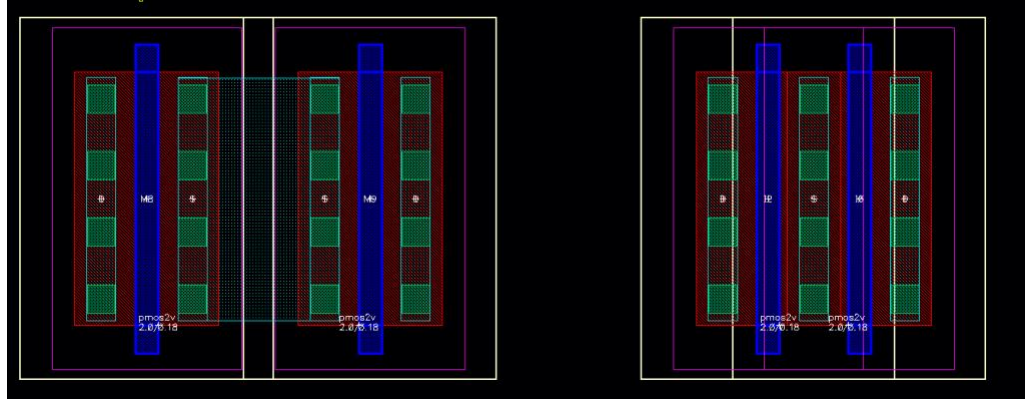
Figure 3-25: (Left) Two Transistors Connected with Metal1 Path and (Right) Two Transistors Chained.

Gate connections were made using metal1 layer, polysilicon layer, and vias. Metal2-metal6 paths are used for longer net connections across the layout due to the fact that they have less sheet resistance and are better for critical input and output signals. Additionally, they were utilized for connections for unwanted overlap of metal1 layer.

Shown in Figure 3-26, two vias were used for each connection between layers to ensure low resistance, stable path connection for electrical conduction. Additionally, the number of contacts to connect GND to the substrate and to connect the nwell of the PMOS to V_{DD} were increased as much as possible to ensure that none of the PN junctions get turned on and to keep the well-substrate PN junction reverse biased. This also allowed for more predictable capacitor values since the material the capacitor coupled to was well controlled.
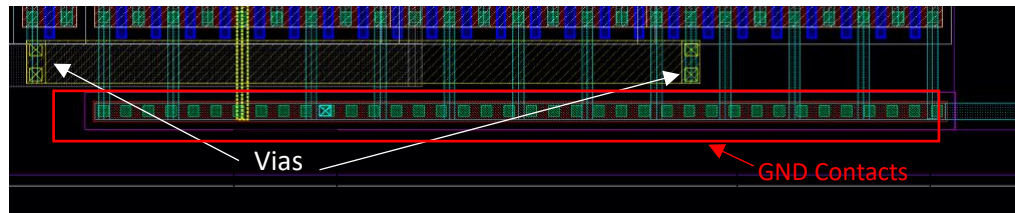

Figure 3-26: Example of Vias and GND Contacts usage in Layout.

Shown in Figure 3-27, the Metal Insulator Metal Capacitor (MIMCAP) cell used has a maximum capacitance of 1.7919 pF for W = 30 μ and L = 30 μ so 20 were used in addition to a 1.2296 pF capacitor to meet the load capacitance design of 39.8 pF in the sawtooth ramp signal

generator. These capacitors are connected through vias in the metal5 and metal6 layer, which are placed very close together to one another but far from the substrate in order to achieve a higher and more optimal capacitor. MIM capacitors were chosen due to its high density and lowest parasitics of all the integrated capacitors.
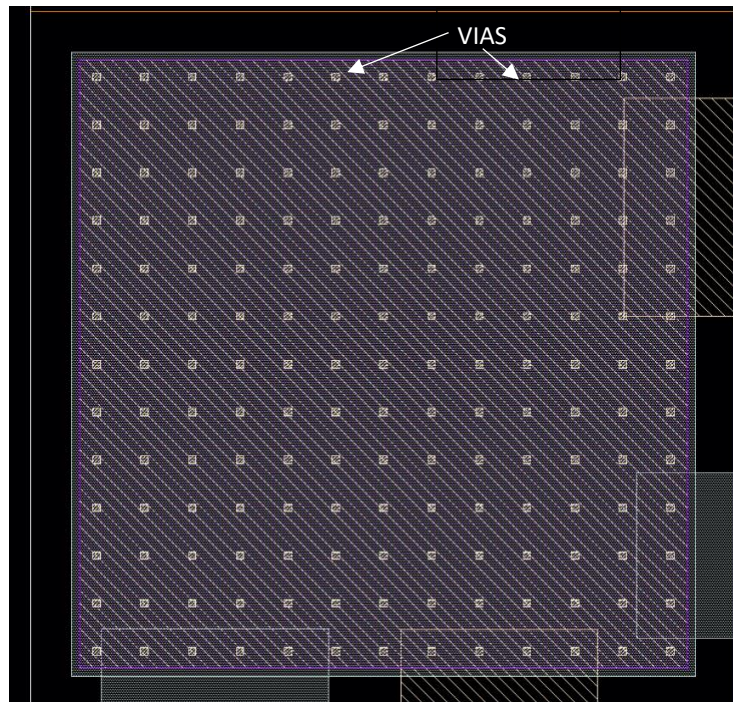

Figure 3-27: A Single MIM Capacitor Cell.

The length of the poly-silicon resistors used in this library are dependent on the resistances. With resistances of about 10K, these lengths can become quite large. A technique used to help with this problem is through the usage of segments which can reduce the size of length while increasing the width. Shown in Figure 3-28, segments make multiple copies of smaller lengths that can add up to the original effective length and therefore, desired resistance. This helps make the layout have a more balanced and symmetric shape/area instead of very long lengthened resistors. Striped layout of the resistors was also used in order to allow for device interdigitation for device and resistor value matching purposes and dummy devices to reduce process gradient effects [16].
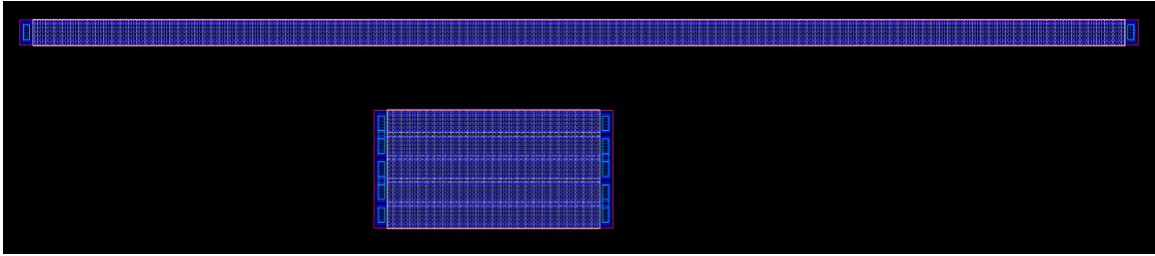
Figure 3-28: (Top) 20kΩ Resistor with No Segments and (Bottom) 20kΩ Resistor with 5 Segments.

Figure 3-29 shows the complete chip with the addition of IO pads. In between the die and the package, there are external bond wires that connect the chip to the package pins. These bond wires are much wider than the wires used in the actual chip that connect each component, so bond wires cannot be connected directly to the on-chip wires. Therefore, in order to connect these wires to the silicon, IO pads need to be added. IO pads help protect against ESD, perform DC-DC conversion, can regenerate digital signals, and give the bond wires a place to attach to among other functions [17].
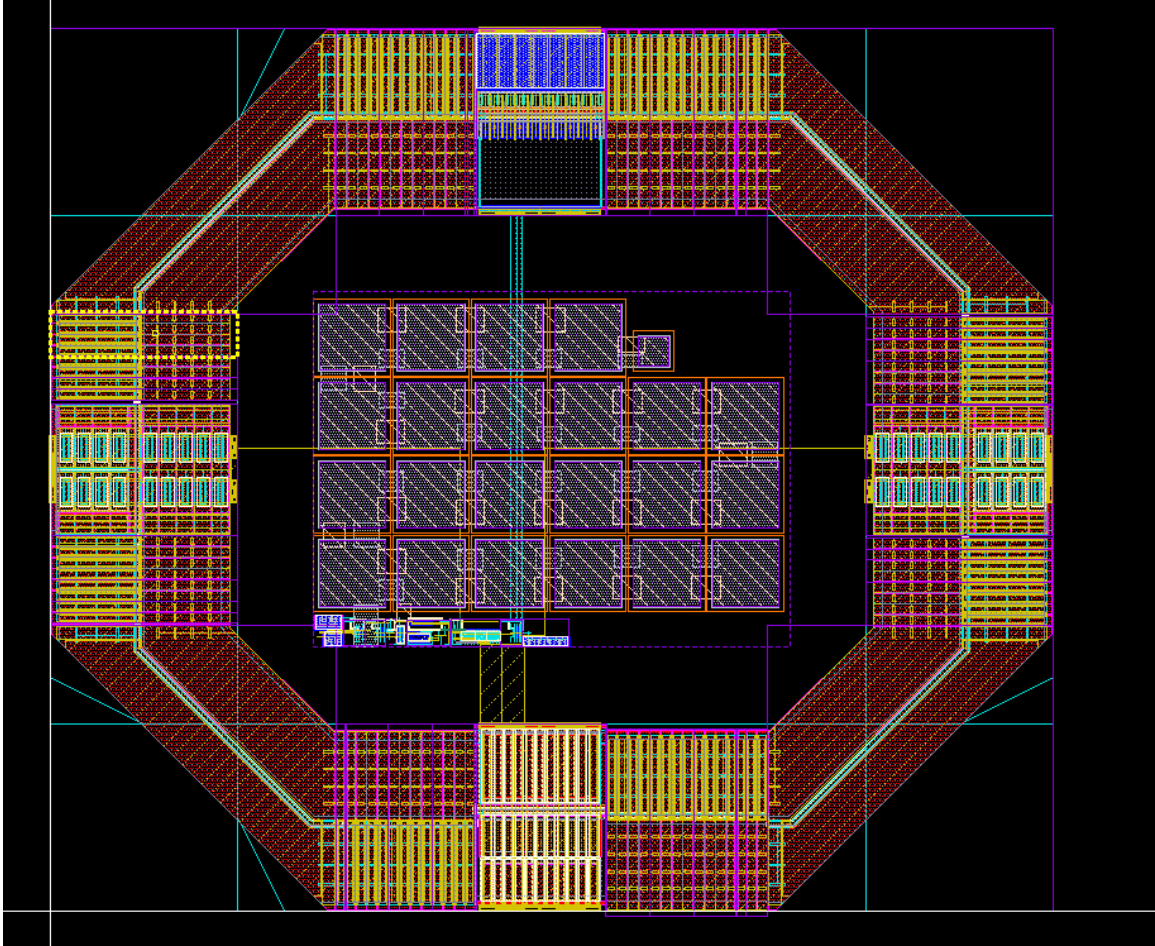
Figure 3-29: Final Layout with IO pads.

The pad ring is essentially the circumference of the chip that contains all the bond pads and I/O drivers. Corner and filler cells are needed to fill the empty spaces between the IO pads to ensure that the ring is continuous so that the power rails such as VDD and GND are connected. The width and length of the pad ring is dependent on the sizes of the circuit and the IO pads. Digital and analog IO pads are of different sizes and have different connections for this process. This design only used four analog IO pads for VDD, GND, V_o, and V_{out}. For this process technology, the size of the corner cells is 132.263µm and the size of the IO pads is 65.526 µm. Therefore, the length of each side of the die should be large enough so that two corner cells and at least two IO pads can fit on each side. This works out to be

$$Length\ of\ Each\ Edge\ of\ Die = 2 \cdot Size\ of\ Corner\ Cell + 2 \cdot Size\ of\ IO\ Pad$$

$$= 2 \cdot 132.263\mu m + 2 \cdot 65.526 \; \mu m = 395.578 \; \mu m \quad \text{(3-40)}$$

The size of the P&R boundary was then set to be 400 μm x 400 μm with the layout of the main

circuitry centered to ensure that all IO pads and corner cells can fit. Power rails and output pins are

then connected to the circuit. It is also important to output match the IO pads. The output resistance

needs to match the connection to the trace and to the antennas of the system. The resistance also needs

to be controllable for high-speed chips.

TESTING/SIMULATION

4.1 Sawtooth Ramp Signal Generator Test

The objective of this stage is to output a linear voltage ramp signal for a period of 10 µs with a target discharge time of 1 ns. This circuit was simulated in ADE L to test for this requirement. V_{Sup} was set to 1.8V using the Analog Stimuli set up and initial conditions of Q = '0' and target start voltage of 0.6687 V at the feedback voltage node V_{fb} so that the circuit had a starting point to charge the capacitor up to the target end voltage of 0.7944 V.

Figure 4-1 shows the output voltage waveform of V_{fb} for 4 cycles. Markers were placed at the beginning and end of the third period to see if the desired period was met and if the target voltage sweep was met. Table 4-1 shows that a sweep period of 10.0048 µs is achieved with a discharge time of only 3.5 ns.
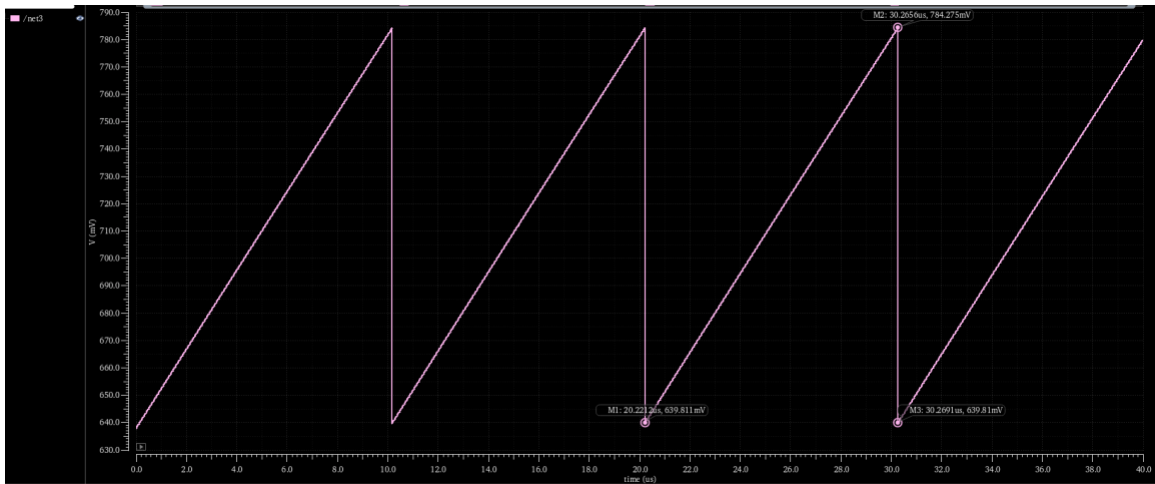

Figure 4-1: Transient Analysis of the V_{fb} voltage for 4 periods.

Table 4-1: Measurements of the Transient Analysis of the Sawtooth Generator.

	Measurement
Marker Time 1	20.2212 µs
Marker Time 2 (time at which V_{fb} at peak)	30.2656 µs
Marker Time 3	30.2691 µs
Period (Time 3 – Time 1)	10.0048 µs
Discharge Time (Time 3 – Time 2)	0.0035 µs = 3.5 ns
Charge Time (Time 2 – Time 1)	10.0444 µs

Simulation shown in Figure 4-1 also shows the actual measurement of the start and end voltage of the sweep. Table 4-2 shows the comparison between the target and actual voltages of the ramp generator. It can be seen that the start voltage has the most error of only 4.32%. Again, most of these errors can be explained by process variation and capacitance introduced by the transistors and resistors. In fact, the effect of the errors in the start and end voltages are miniscule as long as the resulting frequency sweep is within the allowable range for UWB devices.

Table 4-2: Target vs. Actual Measurements for Voltage Sweep.

	Target	Actual	Percent Error (%)
Start Voltage (V)	0.6687	0.6398	4.32
End Voltage (V)	0.7944	0.7843	1.27

4.2 V-I Converter Test

The V-I converter takes the voltage ramp signal from the sawtooth generator stage and converts into a linear output current I_{OUTN} to be used for sweeping the frequency. I_{OUTN} is used to starve the current mirrored to the tail current sink NMOS transistors of the ring oscillator and, therefore, is also used to control the delay of each inverter. With a supply voltage set at 1.8V in the ADE simulation and the output signal V_{fb} of the sawtooth ramp generator used as the V_{IN} node, the output current I_{OUTN} (in red) through the M7 transistor is simulated shown in Figure 4-2. For each sweep period, the current increases from 3.34 µA to 7.288 µA.
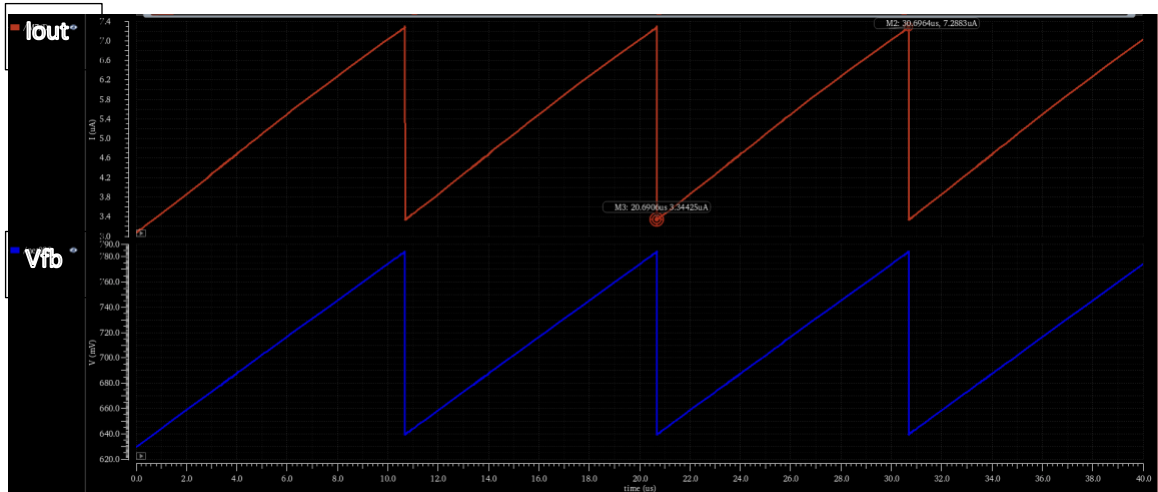

Figure 4-2: Output Current I_{OUTN} (Red) and Output Voltage from Ramp Generator (Blue) for 40 µs.

Table 4-3 shows the comparison between the target and actual currents of the V-I converter. It can be seen that the start voltage has the most error of 11.3%. Again, most of these errors can be explained by process variation and capacitance introduced by the transistors and resistors. However, if the resulting frequency range in the ring oscillator is met, then the errors of these currents do not affect the overall operation of the circuit.

Table 4-3: Targets and Actual Specifications of V-I Converter.

	Target	Actual	Percent Error (%)
Start Current (μA)	3	3.34	11.3
End Voltage (μA)	7	7.289	4.12

4.3 Current-Starved Ring Oscillator Test

The last stage is to take the two currents and output an oscillating signal determined by the propagation delay of each of the inverters in the ring oscillator. For each sweep period, the frequency of this output signal needs to be linearly increasing in the 3.4 GHz – 5.4 GHz frequency range. To test this stage, all three circuits were connected with I_{OUTN} of the V-I converter as the input for I_{inN} of the ring oscillator. Additionally, an initial condition of 0 V was set at the input node of the first inverter to start up the ring oscillator. Figure 4-3 shows transient analysis of the output node V_o of the 3rd inverter and output node V_{out} of the comparator for 4 periods.
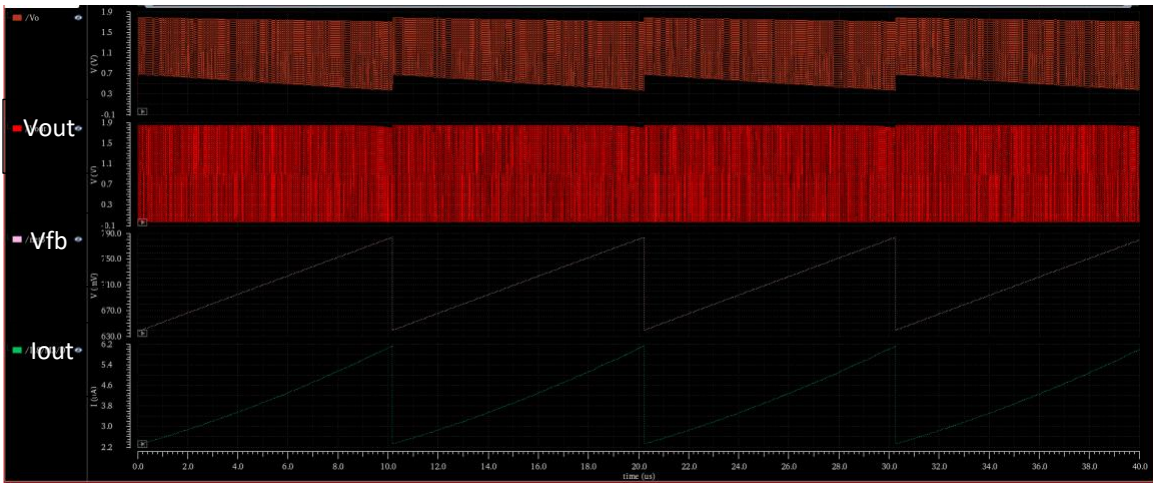

Figure 4-3: Transient Analysis of the Ring Oscillator where V_o is the output voltage of the oscillator and V_{OUT} is the output voltage of the comparator.

Figure 4-4 shows the frequency of the V_{out} signal plotted by using the Derived Plots tool under Measurements. It can be seen that for each sweep period, the frequency ranges from 3.409 GHz to 5.349 GHz which has a bandwidth of 1.94 GHz. Therefore, this system meets the FCC requirements for unlicensed ultra-wideband transmission. Additionally, the output sweeps for a period of 10.0482 µs, which differs from the sweep period of the sawtooth ramp generator; this can be explained by the delay caused by the additional components and capacitance from loading the ring oscillator. Thus, the actual T_{Sweep} of the system is 10.0482 µs.
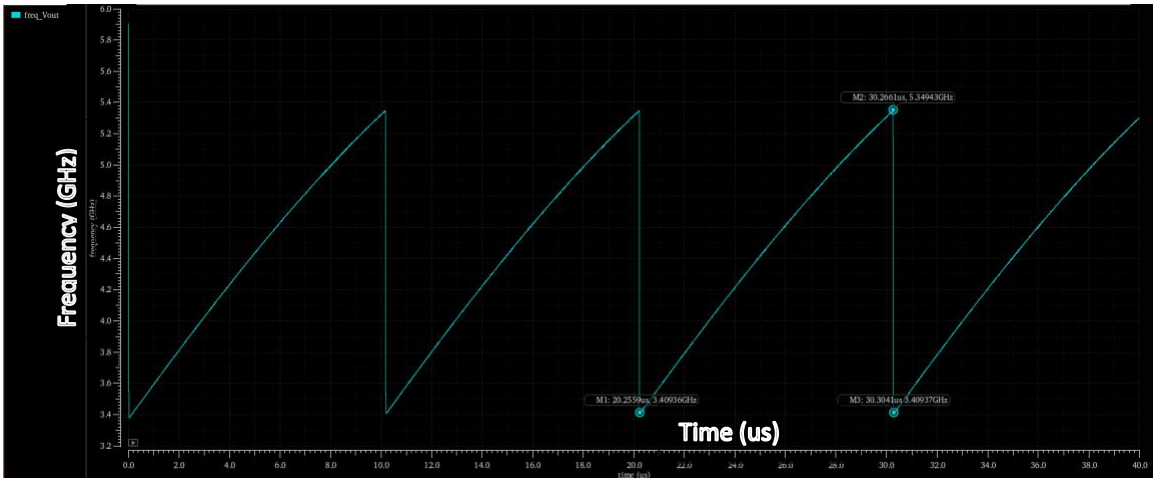
Figure 4-4: Frequency vs. Time plot for V_{OUT}.

It can also be seen that non-linearity effects are introduced, especially in the middle of the frequency sweep period. This can be explained by channel length modulation occurring in the current sink transistors as the V-I converter is loaded with the ring oscillator. The L is not large enough which causes the channel to shorten and have an increase in current with drain bias. However, in the next section, analysis is done to show how much this non-linearity of the frequency sweep affects the distance accuracy measurement.

4.4 DRC/LVS

Design Rules Check (DRC) and Layout versus Schematic (LVS) were also ran in order to make sure the layout met the fabricator's specification and requirements as well as to make sure the layout corresponded correctly to the original circuit schematic. DRC and LVS were actually done for each stage in a block-by-block basis before doing for entire chip. As shown in Figure 4-5, the layout passes DRC with the exception of metal coverage and chip density errors. These rules are to ensure that the density of certain layers in the layout do not get below or above a certain level as well as the coverage of a certain metal layer to be above a certain amount on the chip. However, this project will not be sent to a manufacturer to be fabricated so these errors can be ignored.

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Figure 4-5: DRC Errors Window

Figure 4-6 shows the LVS debug window where the only errors are due to parameter mismatches of the resistors. However, this is an issue with the values specified in the design kit and that after manual confirmation between the resistance values on schematic and layout, there are actually no mismatches and errors.

Figure 4-6: LVS Error Window

Chapter 5

RESULTS

Simulation results from Chapter 4 shows that there are some errors and differences from the target and desired design specifications. This chapter will explain the real-world effects and significance of these errors.

With a FMCW system, distance can be measured, which is important for location and boundary detection. For a frequency range of 3.409 GHz – 5.349 GHz in a single sweep period of 10.048 µs, the theoretical sweep rate can be calculated using Eq. 2-3 where

$$k_{f,theoretical} = \frac{BW}{T_{Sweep}} = \frac{(5.349-3.409)\ GHz}{10.048\ \mu s} = 1.9307 \cdot 10^{14} Hz/s \tag{5-1}$$

This is the sweep rate of the system if the frequency sweep did not have any non-linearity and channel length modulation effects introduced. Figure 5-1 shows the frequency over time plot for this theoretical sweep rate for a period of 10.048 µs. The blue line gives the linear fit equation where the slope is the sweep rate.
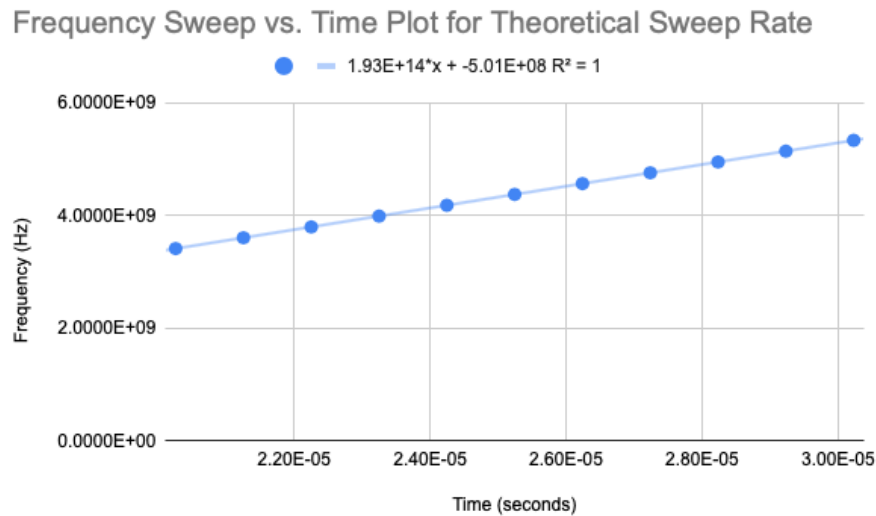

Figure 5-1: Frequency vs. Time with the Theoretical Sweep Rate.
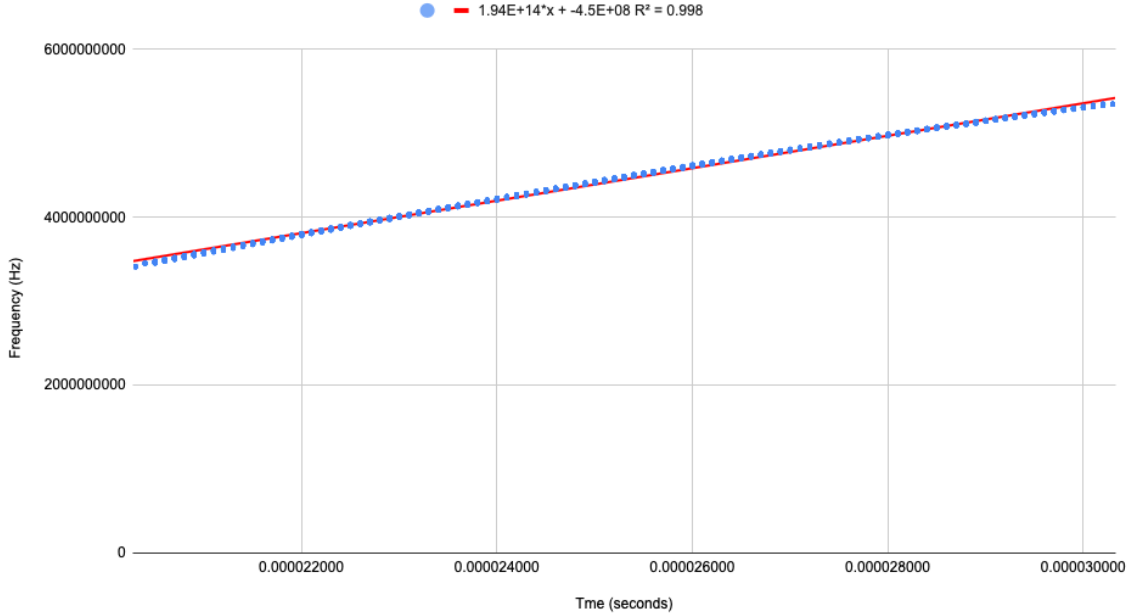
Actual Frequency Sweep of FMCW System

Figure 5-2: Frequency vs. Time with the Actual Sweep Rate.

Figure 5-2 shows the actual frequency over time plot of the output signal of the ring oscillator from 20.559 μs to 30.2661 μs, where the minimum and maximum output frequencies occur, respectively. The red line represents the linear fit regression line where the slope represents the actual sweep rate $k_{f,\ actual}$ of the system, which is 1.93597 x 10^{14} Hz/s. It can be seen that the output frequency sweep has non-linearity effects introduced and further analysis on the distance measurement need to be made to see if the errors in the distance are minimal. Using the data from these plots, the accuracy of the distance measurement can be analyzed by taking the difference in the frequencies at a particular time. Using Eq. 2-5, the theoretical distance of the object from the transmitter can be defined as

$$d_{theoretical} = \frac{\Delta f \cdot c}{2 \cdot k_{f,theoretical}} \qquad (5\text{-}2)$$

Where Δf is the frequency difference of the theoretical and actual output frequency at a particular time and c is the speed of light. Similarly, the actual distance of the object from the transmitter can be defined as

$$d_{actual} = \frac{\Delta f \cdot c}{2 \cdot k_{f,actual}} \qquad (5\text{-}3)$$

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The accuracy can be then be calculated by taking the difference between the two distance measurements and seeing how much it differs. It can be seen in Table 5-1 that the percent error in the distance measurement is consistently about 0.27% and that the error in the distance measurement is never more than 30 cm. Therefore, the proposed system is accurate enough to locate a fallen person within a foot with of their actual location with most of the maximum error occurring in the middle frequencies of the frequency range or during the middle of the period. Although the frequency sweep itself is not exactly linear in each period, the system produces consistent results and that the differences in the distance measurements are miniscule.

Table 5-1: Accuracy Measurements at Various Times.

Time (μs)	$f_{theoretical}$ (GHz)	f_{actual} (GHz)	Δf (GHz)	$d_{theoretical}$ (m)	d_{actual} (m)	$d_{difference}$ (cm)	$d_{percent\ error}$ (%)
21.253	3.6018	3.6274	0.0256	19.889	19.835	5.63	0.27
22.25	3.7943	3.8494	0.0551	42.808	42.693	11.54	0.27
25.24	4.3718	4.464	0.0922	71.632	71.439	19.31	0.27
27.23	4.7568	4.8398	0.0830	64.448	64.311	17.87	0.27
29.23	5.14176	5.185	0.0432	33.594	33.503	9.06	0.27

Table 5-2 shows a summary of the target and actual specifications of the FMCW system. Note that although there are errors and differences between the target and actual specifications, the most important requirement is that the system is operating in the FCC allowable UWB range and that it is linear enough to locate the distance of an object within the orders of centimeters.

Table 5-2: Summary of Target and Actual Specifications.

	Target	Actual
Start Voltage (V)	0.6687	0.6398
End Voltage (V)	0.7944	0.7843
Start Current (μA)	3	3.34
End Voltage (μA)	7	7.289
T$_{Sweep}$ (μs)	10	10.048
Frequency Range (GHz)	3.4 – 5.4	3.409 - 5.349
Bandwidth (GHz)	2	1.94

Chapter 6

CONCLUSION

This thesis presented the development and design of an UWB FMCW radar system that can be used in an eldercare monitoring system. The FMCW chirp signal transmitted from the ring oscillator provides an unobtrusive method to quickly detect when and where a person has fallen.

The final system was able to be designed and simulated in Cadence and successfully meet the desired specifications and requirements. Although the final system introduced some non-linearity in its frequency sweep, it was proved that it can still determine the distance and location of the object with a maximum error within 30 cm in the middle of the frequency sweep. For future works, the linearity of the frequency sweep can be improved to obtain a more accurate distance measurement down to less than 5 cm for all frequencies within the operating range. This can be done by improving the linearity of the current in the V-I converter.

Semi-custom layout of the circuit was also done for chip fabrication with the goal to minimize area as much as possible. The capacitor used in the sawtooth ramp generator took most of the chip area so the design could be improved by reducing the amount of capacitance needed and increasing the W/L size of the transistor responsible for the sweep period. Reducing the capacitances would bring the chip area down by the order of hundreds of micrometers whereas increasing the sizes of transistors would only bring it up by the order of tens of micrometers.

The implementation of this unobtrusive monitoring system would allow elderly and disabled patients to live independently at home without the need for a caretaker. The efficiency and accuracy of the UWB FMCW radar system have become a topic of interest and provides many advantages that many other alternative methods cannot provide.

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