The Dissertation Committee for Miguel Francisco Gandara
certifies that this is the approved version of the following dissertation:

Utilizing Digital Design Techniques and Circuits To Improve Energy and Design Efficiency of Analog and Mixed-Signal Circuits

Committee:

Zhigang (David) Pan, Supervisor

Nan Sun, Co-Supervisor

Eric Soenen

Ranjit Gharpurey

Michael Orshansky

Utilizing Digital Design Techniques and Circuits To Improve Energy and Design Efficiency of Analog and Mixed-Signal Circuits

by

Miguel Francisco Gandara

DISSERTATION

Presented to the Faculty of the Graduate School of

The University of Texas at Austin

in Partial Fulfillment

of the Requirements

for the Degree of

DOCTOR OF PHILOSOPHY

THE UNIVERSITY OF TEXAS AT AUSTIN

May 2021

Dedicated to my wife Disha. “Way before I found my sound, she kept my feet on the ground.”

Acknowledgments

I would like to start by thanking my PhD supervisor, Dr. Nan Sun. I had never seriously considered a PhD before I began working with Dr. Sun during my Master's studies, and without his encouragement I likely never would have pursued that degree. Thankfully, throughout our journey together he remained just as positive and encouraging, and I am deeply thankful for the opportunity to learn from him. I also want to express my deepest gratitude to Dr. David Z. Pan for taking on the role of supervisor late in my PhD journey and helping me to get across the finish line. My sincere thanks to the rest of my committee members, Dr. Michael Orshansky, Dr. Ranjit Gharpurey, and Dr. Eric Soenen, for offering their time and advice during my degree pursuit.

During my professional career, I have been blessed with a number of managers that saw the potential in me, and were absolutely crucial to my growth and success. Ron Strong first encouraged me to pursue graduate studies, Billy Dennie allowed me flexibility to work part-time to focus on my studies, Dr. Eric Soenen and Dr. Martin Kinyua gave me a great first analog design job, and Dr. Tamer Ali and Dr. Ramy Awad pushed me to complete my studies and worked with me to help me to do so. I owe them all for the academic and professional success I have had thus far.

The Sun Research Group is full of smart, passionate, and kind people. I

want to especially thank my colleague and friend Abhishek Mukherjee, for his support through all the ups and downs of the PhD journey. Our regular trips the various eateries of Austin were a great source of stress relief during the long hours of tapeouts. I also want to thank the colleagues that I collaborated with on my two tapeouts and the other projects covered in my dissertation - Dr. Wenjuan Guo, Paridhi Gulati, Ahmet Budak, Dr. Sungjin Hong, Dr. Xiyuan Tang, Yunyi Wang, Dr. Long Chen, Dr. Yeonam Yoon, Dr. Shaolan Li, and Anoosh Michael. Without your crucial assistance during these projects, I could not have possibly have completed this work and you helped to improve the quality of my research. Many thanks to the other members of the Sun Research Group that made the PhD pursuit more enjoyable, Dr. Jeonggoo Song, Dr. Yanlong Zhang, Dr. Wenda Zhao, Dr. Linxiao Shen, Dr. Yi Zhong, Wei Shi, Xiangxing Yang, and Dr. Chen-Kai Hsu. Andrew Kieschnick, the CERC administrator, was always quick to respond to any issue and provided invaluable support on the EDA tools and Linux environment.

Last but certainly not least, I would like to thank my family. My parents, Miguel Gandara and Kathryn Lueders; step-parents, Jeremy Horne and Lydia Persaud; and in-laws, Haresh and Maya Sampat, have been a constant source of love and support throughout this journey. They helped to give me strength during many troubled times in my life. My parents instilled in me the strong work ethic and were some of my first mentors in engineering. Jeremy, Lydia, and the Sampats have always treated me like a son and supported me unconditionally. My siblings Julia, Liam, and Emma have been my biggest

cheerleaders and a reliable stress relief valve. Finally I want to thank the person that's taken every step of this journey with me, my wonderful wife Disha. Her partnership has enabled me to achieve beyond what I thought possible, and I am thankful every day that she is in my life.

Utilizing Digital Design Techniques and Circuits To Improve Energy and Design Efficiency of Analog and Mixed-Signal Circuits

Miguel Francisco Gandara, Ph.D.
The University of Texas at Austin, 2021

Supervisors: Zhigang (David) Pan
Nan Sun

Technology scaling has long driven large growth in the electronics market. With each successive technology generation, digital circuits become more power and area efficient. The large performance increases realized for digital circuits due to digital scaling have not translated to similar performance improvements for analog circuits. First, noise-limited analog circuits are not capable of leveraging the reduced parasitics of advanced processes, since capacitor sizes are generally set by noise requirements. Second, analog circuit performance is closely tied to the achievable device intrinsic gain, which degrades as process sizes shrink. Reduced supply voltages further exacerbate this issue, as the achievable gain per stage is limited by the number of devices that can be stacked while maintaining all devices in saturation. Finally, process variation increases with decreased feature sizes, so analog circuits have deal with increased mismatch and wider variations in threshold voltages, increasing the time required to design a circuit that is robust across process, voltage, and

temperature (PVT) variation. This work seeks to address the limitations of analog circuits in advanced technologies by leveraging digital techniques and digital-like circuits that offer improved scalability. The first half of this dissertation investigates replacing the traditional closed-loop residue amplifier in a pipeline analog-to-digital converter (ADC) with an open loop dynamic amplifier. Previous works incorporating dynamic amplifiers have struggled to achieve large gains and have suffered from offset mismatch between the comparator and amplifier, which will only get worse in more advanced technologies. We propose the usage of a residue amplifier that combines an integration stage, to ensure low noise operation, with a positive feedback stage, to ensure high gain and high speed operation. By utilizing this topology, the proposed amplifier was the first dynamic amplifier to achieve a high gain of 32. Additionally, the proposed amplifier can reuse existing comparator hardware in the ADC, removing all offset mismatch between comparator and amplifier. Digital calibration techniques were applied to ensure a constant gain across PVT. The next part of this dissertation tries to overcome the scaling challenges for noise-limited ADCs with band-limited input signals. By leveraging digital filtering techniques to generate a prediction of the band-limited signal, the conversion can be limited to a range that is a fraction of the total ADC input range, allowing for significant decreases in reference and comparator power consumption. This work extends previous works by enabling accurate predictions for any band-limited signal characteristic. Previous works only focused on accurate predictions for low-activity signals. Finally, the large compute power enabled

by modern technology scaling is leveraged to improve the design efficiency of analog circuits. A new automated circuit sizing tool is proposed that can achieve better performance than manual designs done by experts in a much shorter amount of time. All of these techniques help to alleviate the power and design efficiency limitations caused by technology scaling.

Table of Contents

List of Tables

List of Figures

Chapter 1

Introduction

Technology scaling has enabled increased functional integration into modern Systems on Chip (SOCs). Digital processors now commonly integrated mixed-signal functionality for sensing and communication. While technology scaling has significant benefits for digital circuits, reducing both the power and area with each new technology generation, analog circuits do not obtain the same benefits. First, for medium and high precision designs, the power consumption is set by the noise requirements, which will not scale with technology. Further, designing high precision signal processing elements becomes more difficult as technology scales. Traditional high precision signal processing is done by applying negative feedback to ensure constant performance across process, voltage, and temperature (PVT) variation. These techniques require amplifiers with large gain in order to ensure adequate loop gain to maintain high precision in the negative feedback loop. Device intrinsic gains generally reduce as the device size shrinks, which limits the achievable gain from a single-stage amplifier. Furthermore, reduced supply voltages in advanced processes also limit the amount of cascoding that can be performed while maintaining an adequate output swing. Both of these limitations imply more gain stages are needed in order to achieve the necessary amplifier gain to support closed-

loop operation. These extra gain stages increase power consumption as well as mismatch and noise. Our work seeks to address the scaling limitations of noise-limited designs and the challenges of designing high precision op amps for analog signal processing by leveraging digital techniques and more scaling-friendly amplification topologies.

Pipeline analog-to-digital converters (ADCs) are an attractive option for medium resolution (12-16 bits) and medium to high speeds (tens of Ms/s to hundred of Ms/s). By splitting up a single high resolution conversion into multiple pipelined lower-resolution conversions, the pipeline ADC can achieve high sampling rates with only a linear increase in hardware complexity. The main design challenge associated with modern pipeline ADCs is their requirement for precise gain between stages to ensure adequate dynamic range for each pipeline sub-ADC. As mentioned above, precision gain is typically implemented using closed-loop approaches with large amplifier gain requirements. Previous work [17, 11] has sought to reduce the amplifier gain requirements by utilizing open-loop amplifiers, reducing the gain requirement to match the desired interstage gain in the pipeline ADC. In order to further reduce the residue amplifier power consumption, dynamic amplifiers using integration have been utilized. These amplifiers do not require any static power consumption, greatly improving their power efficiency. Integrator-based amplifiers suffer from two main limitations; the achievable gain is limited and the offset mismatch between the comparator and amplifier requires either large device sizes or additional hardware for offset calibration. Even in integrator-based designs that

utilize special techniques to increase the achievable gain [24, 15], the maximum achievable gain is limited to approximately 16. Our work seeks to increase the achievable gain for dynamic amplifiers by cascading an integrator stage, to achieve moderate gain and sufficient signal-to-noise ratio (SNR), with a positive feedback stage, to achieve high gain and high speed. A prototype 12-bit pipelined ADC sampling at 10 Ms/s was fabricated in 130 nm CMOS technology to prove the feasibility of our residue amplification approach. To the authors' best knowledge, this is the first pipeline ADC to utilize positive feedback in the residue amplifier, and it is the first dynamic amplifier capable of achieving a gain of 32. Our proposed residue amplifier also offers a simple method to ensure there is no offset mismatch between the residue amplifier and the sub-ADC comparator. The strongARM latch that is used as a comparator in many ADC designs already performs this cascaded integrator and positive feedback operation. By stopping the comparator operation before its outputs have fully resolved to supply and ground, the comparator can be utilized as an analog amplifier. Sharing the strongARM latch between the residue amplifier and the sub-ADC comparator ensures no offset mismatch is present. Chapter 2 discusses the proposed residue amplifier and the proposed pipeline ADC architecture in more detail.

Despite the impressive advantages of our proposed residue amplifier, our first prototype suffered from two key limitations that limited the achievable performance and robustness. First, unlike traditional closed-loop amplifiers, our proposed residue amplifier's outputs are not fully settled at the end

of the amplification operation. Since the outputs are still changing when the amplifier output is sampled, the output is sensitive to any jitter in the amplifier's timing control. When utilizing positive feedback, this sensitivity is increased even further, since the amplifier output increases exponentially with time. The jitter present in the timing control loop of our first prototype limited the ADC's ENOB to 10.3 bits. Second, the amplifier gain varies across PVT variation, a key disadvantage compared to closed-loop approaches. This sensitivity is increased by the usage of positive feedback. In order to address the jitter and gain variation, a simple timing control loop is proposed. The timing control is simple and adds minimal jitter to the timing loop. The proposed timing loop also automatically adjusts the amplification time for changing integration time, thus significantly reducing the gain variation across PVT. Finally, the timing control offers a simple control knob to further adjust the amplification time; by sensing the gain in the digital domain and adjusting the amplification time for constant gain, the loop can be closed in the digital domain, which allows for high loop gains without the implementation complexity of analog closed-loop solutions. The proposed timing control loop reduces both the jitter-induced noise and power consumption of the timing loop from the first prototype. The usage of a mixed-signal calibration loop also removes the need for a fractional divider running at the sampling rate, which can be a large source of power consumption for low-power ADCs. A second prototype was fabricated in 130 nm CMOS, and measurement results showed a 4 dB improvement in SNDR, as well as stable performance across a 100°C temperature

range. Both performance improvements were enabled by the enhanced timing control loop with mixed-signal background calibration. Chapter 3 discusses the implementation of our proposed gain control and mixed-signal background calibration loop as well as the measured prototype performance.

Successive Approximation Register (SAR) ADCs are increasingly used in advanced processes due to their highly digital nature. For medium resolution ADCs that are noise-limited, however, the power consumption in the comparator and the capacitive digital-to-analog converter (CDAC) do not scale as well as the digital control. This is because the capacitance associated with each of these blocks must be sized large enough to ensure adequate SNR. As supply voltages reduce in advanced processes, the available input voltage swing also decreases, placing even more stringent noise requirements on the CDAC and comparator. Chapter 4 discusses the usage of digital filtering techniques to reduce the comparator and CDAC power when the input signal is band-limited. By applying some knowledge of the input characteristics, a prediction filter can be designed to apply an initial guess to the SAR CDAC and reduce the required conversion range. Our work extends previous work by enabling prediction filtering for any band-limited input signal. Previous works have only focused on accurate predictions for low-activity signals. The theoretical results of this chapter are supported by modeling and simulation results of a 10-bit, 100 kS/s SAR ADC.

Chapter 5 seeks to improve the design efficiency of analog circuit designers by leveraging the large compute power enabled by technology scaling.

A new circuit sizing tool is proposed that can achieve performance comparable to that of state-of-the-art designs in a fraction of the time required for manual design. Especially in advanced processes, optimizing the circuit sizing can be a tedious and time consuming process. By automating the sizing process, designers can focus on more interesting architectural and system-level design problems.

This dissertation is organized as follows. The rest of this chapter focuses on the fundamental concepts that are used throughout the rest of this dissertation. Sec. 1.1 covers the theory of operation of pipeline ADCs. Sec. 1.2 covers the theory of operation of SAR ADCs. Chapter 2 and 3 cover the proposed residue amplification technique for pipelined ADCS, as well as the proposed gain control and mixed-signal background calibration loop that ensures constant gain across PVT. Chapter 4 discusses the proposed digital prediction technique that allows for accurate prediction of any band-limited signal. Chapter 5 presents a new automated circuit sizing tool and some example case studies leveraging the new tool and a new optimization algorithm developed by another PhD student. Chapter 6 concludes the dissertation.

1.1 Pipeline ADC Operation

This section begins with an introduction to the operation of a simple pipeline ADC. After the introduction, the operation of the Multiplying DAC (MDAC), an important block in pipeline ADC design, is presented in detail. This section concludes with a discussion of redundancy, a commonly used

method in pipeline ADC designs for reducing the offset requirements of the sub-ADC comparators. Figure 1.1 shows an example block and timing diagram for a pipelined ADC. By splitting up an M-bit conversion into N stages, the maximum conversion speed can be increased to the conversion speed of a single sub-ADC. Additionally, increasing the resolution requires only a linear increase in hardware complexity. This is in contrast to flash and SAR ADCs, where an increase in resolution requires an exponential increase in hardware complexity. Each sub-ADC operates in two phases. In the first phase, the sampled residue voltage from the preceding stage is sampled for further processing. In the next phase, the sub-ADC performs its conversion, generates a residue voltage, and sends that residue to the succeeding stage for further quantization. An additional digital block collects all the outputs from the sub-ADCs, scales them appropriately, and combines the individual outputs into a single M-bit output. For further detail on the conversion and residue generation process, Figure 1.2 illustrates a general two stage pipelined ADC. After the first stage samples the input voltage during its first phase, the first stage moves into the conversion and residue generation phase. During this phase, the coarse ADC performs an n-bit conversion of the input. During this phase, the n-bit sub-ADC converts the input voltage into a digital code, D_{coarse}. An n-bit digital-to-analog converter (DAC) then transforms D_{coarse} to an analog voltage. The analog output from the n-bit DAC is then subtracted from the input voltage, producing an error residue voltage, V_{res}. The residue voltage is bounded by:

$$-\frac{V_{ref}}{2^n} \leq V_{res} \leq \frac{V_{ref}}{2^n} \tag{1.1}$$

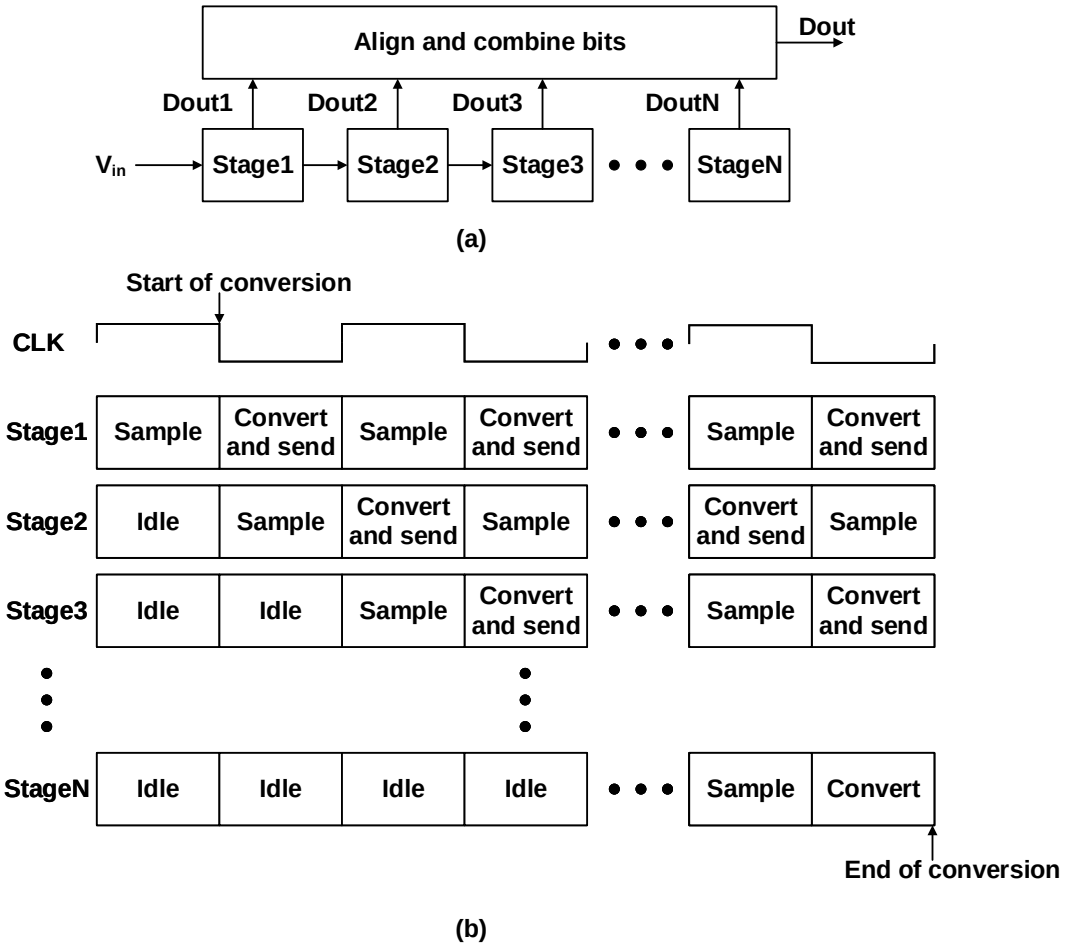

Figure 1.1: Conceptual (a) block diagram and (b) timing diagram of a pipeline ADC

where V_{ref} is the reference voltage of the ADC that sets the maximum full-scale range of the ADC. The residue voltage is then amplified with a gain of G. This amplifier is used to reduce the precision requirements of the downstream ADC. The precision requirements on the m-bit fine ADC without an amplification stage would be $m+n$ bits. For an M-bit ADC, the least significant bit (LSB)

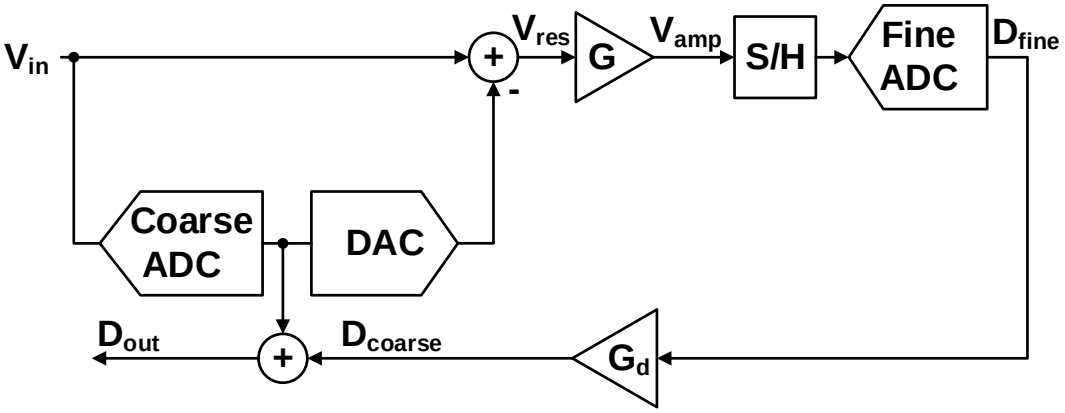

Figure 1.2: Example two-stage pipelined ADC

size, Δ is given by:

$$\Delta = \frac{V_{FS}}{2^M} \tag{1.2}$$

where V_{FS} is the full-scale voltage of the ADC. Without amplification, V_{FS} of the second stage is given by Equation 1.1. Using this value in Equ. 1.2 gives a second-stage size, Δ_2, of:

$$\Delta_2 = \frac{V_{FS}}{2^{n+m}} \tag{1.3}$$

which is equivalent to an $m+n$ bit ADC. With an amplification stage gain of $G = 2^B$, Δ becomes:

$$\Delta_2 = \frac{V_{FS}}{2^{n+m-B}} \tag{1.4}$$

which reduces the precision requirement to $m+n-B$ bits. Since the full-scale voltage of the second stage is generally equivalent to the full-scale voltage of the first stage, the amplification factor G sets the effective resolution of the input to the second stage. Fig. 1.3 further illustrates the required fine ADC decision levels with and without residue amplification. Fig. 1.3(a) shows the

voltage transfer curve at the output of the coarse ADC, assuming a coarse ADC resolution of 2 bits. Without residue amplification, the fine ADC decision levels need to be spaced closely to cover the reduced input range. With residue amplification, the voltage transfer curve becomes 1.3(b), with the fine ADC decision level spacing relaxed by the residue amplifier gain. In traditional

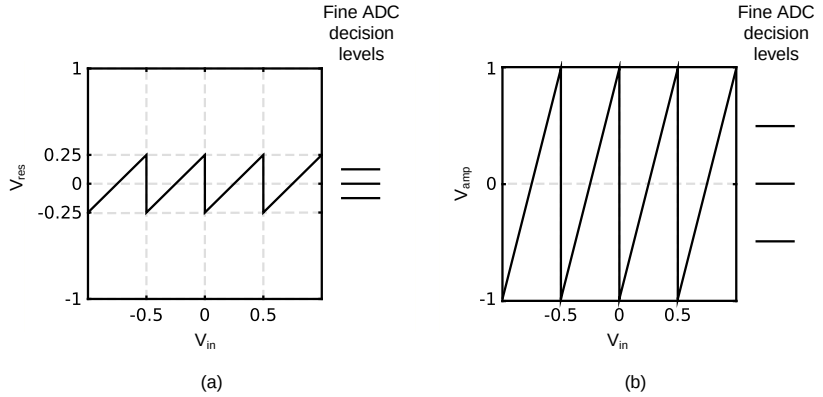

Figure 1.3: Voltage transfer curve at residue amplifier (a) input (b) output

designs, the subtraction and amplification stages are implemented as a single switched capacitor device, the MDAC. Section 1.1.1 discusses the residue amplification operation in more depth. The second stage is sampling the output from the MDAC while the first stage is in its amplify/hold phase. At the end of the second stage sampling phase, the sampled voltage is quantized by an m-bit ADC, producing D_{fine}. D_{fine} is then passed through a digital gain stage with ideal $G_d = G$ and combined with the coarse ADC output to produce the final $(m+B)$ bit digital output, D_{out}. Although this example is only for two stages, this idea could be expanded to any number of arbitrary stages by adding an MDAC with its own amplify/hold phase to the second stage and replicating

more stages. A high resolution ADC can be constructed from a series of low resolution ADCs by partitioning the conversion in this manner. For a pipeline with i stages, a latency of $i-1$ cycles is introduced, but the cycle time is only limited by the longest stage conversion time.

1.1.1 Residue Amplification

Figure 1.4 shows the first stage from Figure 1.2 with an n of one. The sum and gain stages are replaced with an ideal MDAC model. This particular MDAC topology is known as a non-fliparound architecture. A single-ended model is shown for simplicity. At the heart of the MDAC is an operational

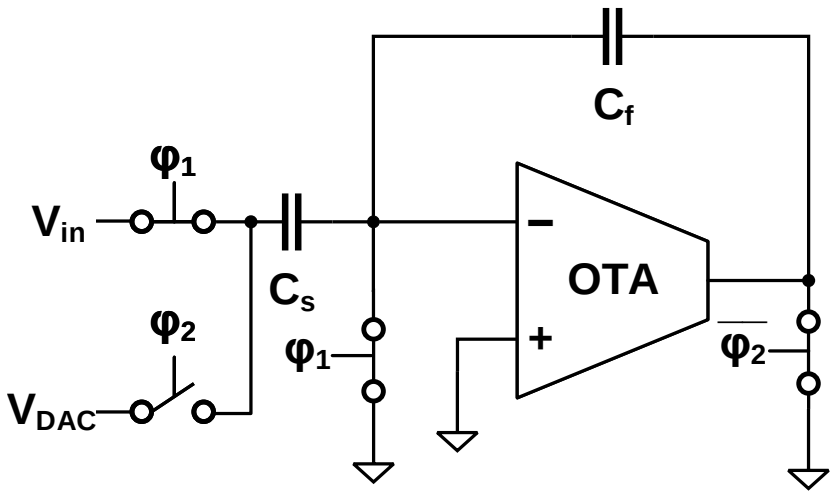

Figure 1.4: Example MDAC

transconductance amplifier. For the purposes of this example, the OTA gain is assumed to be infinite, so that the voltage difference between the two OTA input terminals is zero. When the amplifier gain is less than infinity, static gain

error is added to the MDAC output. For this reason, the closed-loop MDAC topology generally requires open-loop amplifier gains much larger than the desired closed loop gain. ϕ_1 and ϕ_2 are non-overlapping clock signals. ϕ_1 corresponds to the sample/conversion stage and ϕ_2 corresponds to the amplify/hold stage of the pipeline ADC. C_s is the sampling capacitors and C_f is the feedback capacitor. For the purposes of this example, C_s has a value of $2C$ and C_f has a value of C. When ϕ_1 is active, the input voltage, V_{in}, is sampled onto the sampling capacitors. The expression for the charge at node X at the end of ϕ_1, Q_{x,ϕ_1} is:

$$Q_{x,\phi_1} = -2CV_{in} \tag{1.5}$$

At the end of ϕ_1, the sub-ADC performs its conversion and connects the bottom plate of C_s to $\pm\frac{V_{ref}}{2}$. When ϕ_2 is active, the charge at node X, Q_{x,ϕ_2} is:

$$Q_{x,\phi_2} = \begin{cases} -CV_{res,o} - CV_{ref} & \text{if } V_{in} > 0 \\ -CV_{res,o} + CV_{ref} & \text{if } V_{in} \leq 0 \end{cases} \tag{1.6}$$

where $V_{res,o}$ is the amplified residue voltage. From charge conservation, Q_{x,ϕ_1} and Q_{x,ϕ_2} must be equal. Setting these quantities equal to each other and solving for $V_{res,o}$ yields:

$$V_{res,o} = \begin{cases} 2V_{in} - V_{ref} = 2(V_{in} - \frac{V_{ref}}{2}) & \text{if } V_{in} > 0 \\ 2V_{in} + V_{ref} = 2(V_{in} + \frac{V_{ref}}{2}) & \text{if } V_{in} \leq 0 \end{cases} \tag{1.7}$$

Putting Equation 1.7 in terms of G and V_{res} from Figure 1.2, the voltage at the input of the m bit ADC is:

$$V_{res,o} = 2(V_{in} \pm \frac{V_{ref}}{2}) = GV_{res} = \frac{C_s}{C_f}V_{res} \tag{1.8}$$

From Equ. 1.8, the gain is set by the ratio of C_s to C_f. Passive components generally match each other well, so the MDAC has a well-defined gain that should be stable across PVT, assuming the OTA provides sufficient loop gain to minimize the static error at its inputs. Redundancy is a technique often used in pipeline ADCs to relax comparator offset requirements. To illustrate this, Figure 1.4 will be used. From Equations 1.1 and 1.7, the bound for the amplified residue output is:

$$|V_{res,o}| \leq V_{ref} \tag{1.9}$$

From this equation, it can be seen that $V_{res,o}$ is bound by the full-scale input range of the next stage ADC. Comparator offsets affect the decision levels of the sub-ADC, causing some residue voltages to exceed Equation 1.1. This will then cause $V_{res,o}$ to exceed the input range of the next stage ADC. The use of redundancy increases the resolution in the stage sub-ADC without increasing the interstage MDAC gain. In this case, the effective stage resolution remains the same, but the maximum sub-ADC decision error decreases, thus allowing some additional headroom for comparator offsets. Most pipelined designs opt for either 1 bit or ½ bit redundancy. Adding an additional bit to the stage ADC in Figure 1.4 reduces the maximum input residue voltage by a factor of two, so the bound of $V_{res,o}$ becomes:

$$|V_{res,o}| \leq \frac{V_{ref}}{2} \tag{1.10}$$

With 1 bit redundancy, the MDAC can accommodate comparator offsets of up to ½ LSB without overloading the next stage ADC.

1.2 SAR Operation

SAR ADCs use a binary search algorithm to successively approximate the input voltage by comparing the input sampled voltage, V_{in} to a DAC output voltage, V_{DAC}. In many cases, the DAC is implemented using a capacitive charge redistribution method. Fig. 1.5 illustrates a two bit capacitive charge redistribution SAR ADC. A single-ended version of this design is shown for simplicity. In Fig. 1.5, the capacitor of size $2C$ is known as the most significant bit (MSB) capacitor and the first C is known as the least significant bit (LSB) capacitor. The second capacitor of size C is known as a dummy LSB capacitor. The signals d_1 and d_0 correspond to the digital outputs from the first and second conversion steps, respectively. The digital outputs are obtained from the output of the comparator. From the figure, the total capacitance of this ADC is $4C$. A general expression for the total capacitance of an N bit SAR ADC with a unit capacitance of C is:

$$C_T = 2^N \cdot C \tag{1.11}$$

Equ. 1.11 shows that an increase in ADC resolution of 1 bit requires doubling the sampling capacitance. To perform a conversion, the ADC first samples the input. During this phase, the top plates of all capacitors are connected to V_{in} and the bottom plates are connected to V_{ref}. In the first conversion phase shown in Fig. 1.5(b), the $2C$ capacitor is switched from V_{ref} to 0, causing a change in voltage at V_x of $0.5V_{ref}$. The voltage at V_x is then compared to 0. For the case of Fig. 1.5, the sampled input voltage is less than $0.5V_{ref}$,

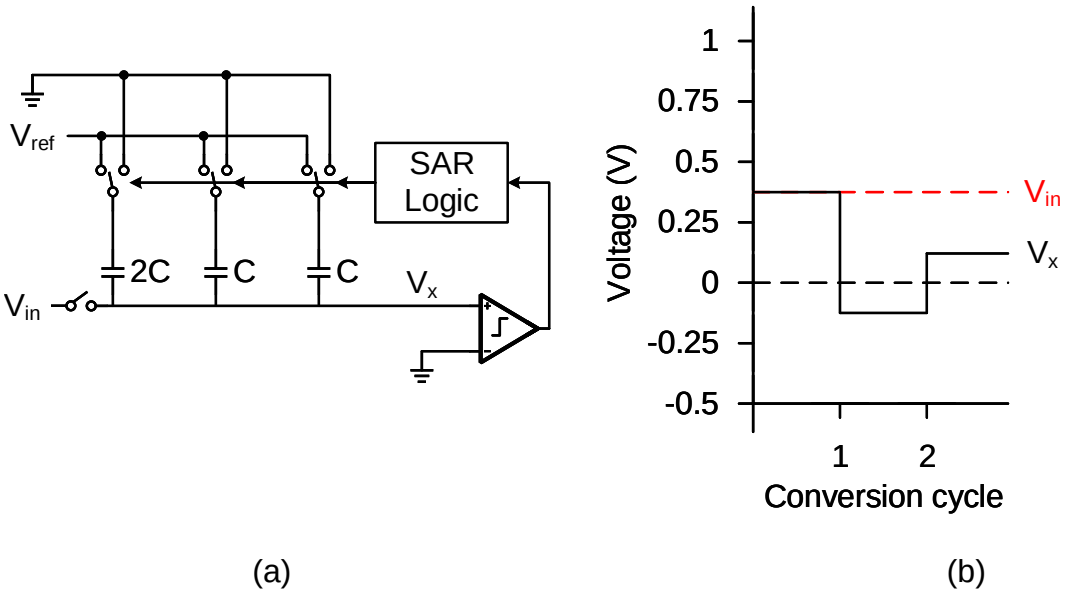

Figure 1.5: (a) Example 2-bit SAR ADC (b) SAR ADC voltage waveforms

so the comparator output will be 0. Since the comparator output is 0, the $2C$ capacitor will be reconnected to V_{ref} and the conversion will proceed by changing the C capacitor from V_{ref} to 0, causing a change on V_x of $0.25V_{ref}$. The comparator then fires to compare the V_x to 0. Each conversion proceeds in this manner until all bits are resolved. For an N bit ADC, N conversion steps are required to obtain the final digital output. This serialization of the conversion limits the achievable speed of this ADC topology. From Fig. 1.5, the SAR ADC only requires a CDAC, a comparator, and digital logic. Most of these blocks are digital or digital-like in nature, so they take advantage of the area, speed, and power benefits of technology scaling. As mentioned earlier, this fact does not hold as well for higher resolution ADCs, where the comparator and CDAC noise limit the overall performance. In this case, pipeline SAR

ADCs are an attractive option because they reduce the accuracy requirements of the SAR ADC to the sub-ADC resolution. This allows for large reductions in CDAC area and power, as well as large reductions in comparator power for noise-limited designs. The trade-off is the required residue amplification stage, which now sets most of the important performance parameters for the pipeline SAR ADC.

Chapter 2

Pipelined SAR ADC Reusing the Comparator as Residue Amplifier

2.1 Introduction

Successive approximation register (SAR) analog-to-digital converters (ADCs) are very popular for medium resolution (8-10 bits) applications because of their mostly digital architecture and high power efficiency. For higher resolution at high speeds, pipelining becomes an attractive option to limit the capacitive digital-to-analog converter (CDAC) size and reduce the number of serial conversions per conversion cycle. The main drawback to this approach is the requirement of residue amplification between each stage. Traditional closed-loop residue amplifiers require large open-loop gains which are difficult to achieve in advanced processes. Moreover, these amplifiers consume static power, which limits the power efficiency when compared to a standard single-stage SAR architecture.

Many recent works have proposed alternatives to traditional closed-loop residue amplifiers. One option is to perform open-loop residue amplification, which greatly reduces the required amplifier gain at the cost of increased nonlinearity. This approach can require complex digital calibration [17] or lin-

earization techniques [32] and still consumes static power. Other recent works have proposed using dynamic amplifiers, or integrators, for residue amplification [27, 15, 24, 11]. Integrator-based amplifiers are attractive because they achieve high power efficiency for a given input-referred noise. One drawback of integrator-based amplifiers is that the maximum achievable gain is limited by transistor g_m/I_D and the voltage supply. Recent works have attempted to overcome this issue [24, 15], but the gain is either still limited [24], or additional gain requires increased timing complexity [15]. Another challenging issue for most residue amplifier architectures is the mismatch between comparator and amplifier offsets. Offset mismatch both increases the amplifier's input swing, increasing non-linearity, and can cause overranging in later stage ADCs. These effects are especially harmful in dynamic-amplifier based pipelined SAR ADCs because 1) the linearity of dynamic amplifiers is generally much more sensitive to input swing than closed-loop amplifiers and 2) the first-stage resolution is generally high in order to maintain the SAR's power efficiency and limit the amplifier input swing, thus reducing the LSB size and the effectiveness of gain redundancy. In general, either large devices or offset calibration techniques must be used in order to meet the offset matching requirements.

In this paper, we propose a novel pipelined SAR architecture, shown in Fig. 2.13. It addresses the aforementioned drawbacks of other dynamic amplifiers without adding any hardware complexity to the traditional SAR architecture by *reusing the first-stage comparator, a strongARM latch, as a residue amplifier*. This architecture maintains the noise filtering of an integra-

tor as in [24], while adding a high-speed positive feedback gain phase. The achievable maximum gain is only limited by the ratio of supply voltage to input swing and the required second-stage linearity. The gain control only requires a simple tunable delay line. Since the amplifier and comparator are the same block, no calibration for offset mismatch needs to be done to limit input swing or prevent overranging. By properly partitioning the pipeline stages, the first-stage residue can be kept small enough that the amplifier does not require any non-linearity calibration.[1]

2.2 Residue Amplification Using a StrongARM Latch

2.2.1 Basic Operation

The schematic of the proposed residue amplifier is shown in Fig. 2.1. The latch is very similar to that in [28], with an added current bias to improve the common-mode rejection of the amplifier. When the *clka* signal is low, the second stage SAR capacitance is disconnected from the amplifier and the amplifier behaves as a normal comparator. When *clka* is high, the amplifier transfers the residue to the second stage SAR with a gain that is proportional to the time *clka* is kept high, τ_{amp}. The proposed amplifier operates in four phases: reset, internal integration, output integration, and regeneration. During the reset phase, *clk* is low and all comparator voltages, V_{op}, V_{on}, V_{xp}, and

[1]This chapter is a partial reprint of the publication: Miguel Gandara, Wenjuan Guo, Xiyuan Tang, Long Chen, Yeonam Yoon, and Nan Sun, "A Pipelined SAR ADC Reusing the Comparator as Residue Amplifier," in *IEEE Custom Integrated Circuits Conference (CICC), 2017*. I was the primary investigator and designer on this published work.

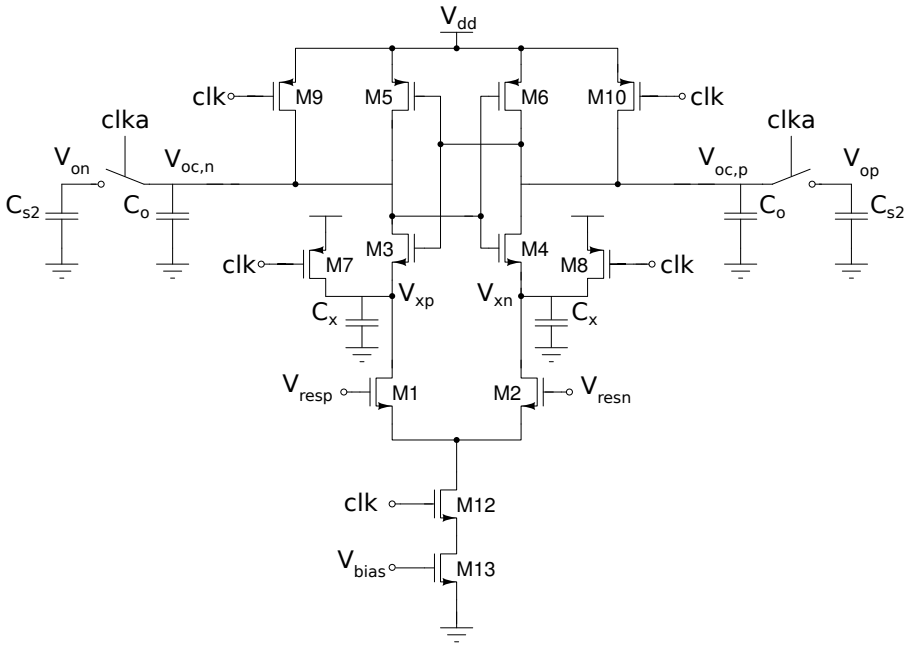

Figure 2.1: Proposed amplifier schematic.

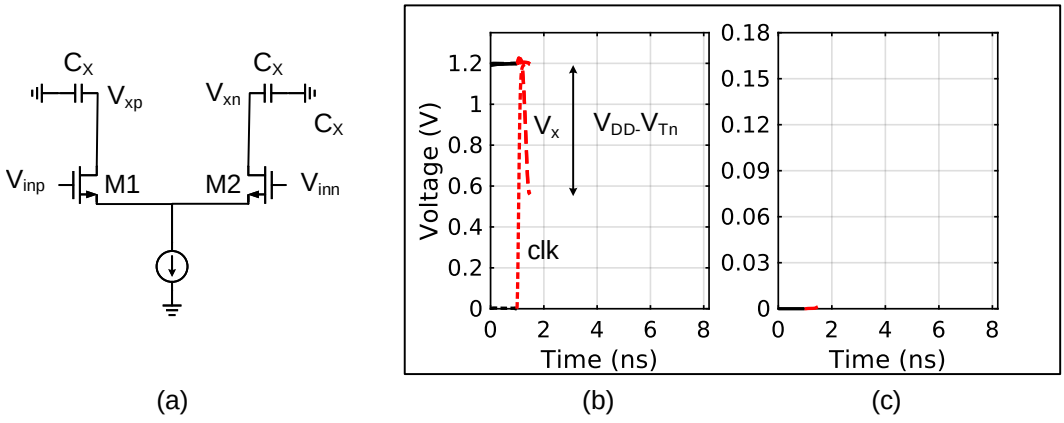

Figure 2.2: (a) Amplifier equivalent schematic during internal integration (b) Single-ended waveforms (c) Differential output waveform

V_{xn} are pulled to V_{DD}. Internal integration starts when *clk* switches from 0 to 1. Fig. 2.2 shows the equivalent circuit during internal integration and the

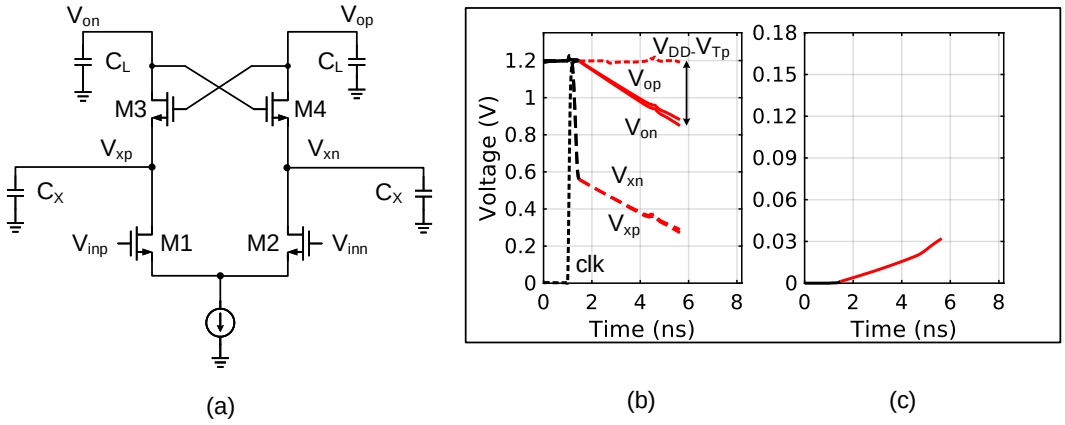

Figure 2.3: (a) Amplifier equivalent schematic during output integration (b) Single-ended waveforms (c) Differential output waveform

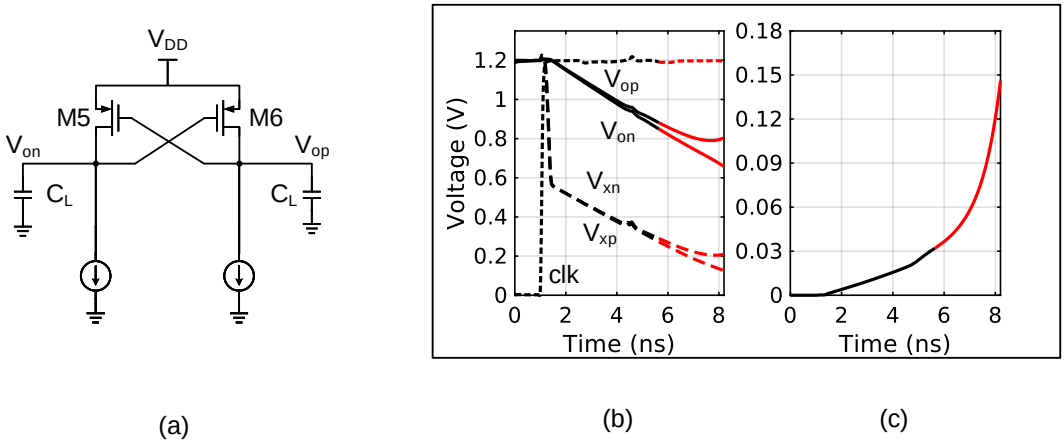

Figure 2.4: (a) Amplifier equivalent schematic during regeneration (b) Single-ended waveforms (c) Differential output waveform

transient waveforms for the comparator voltages. During the internal integration phase, the differential current through M1 and M2 is integrated on the capacitance at nodes V_{xp}/V_{xn}, C_x. Once the V_x node voltages decrease enough to turn on transistors M3/4, the output integration phase begins. Fig. 2.3 shows the equivalent circuit and transient waveforms during this phase. The

differential current from the input pair is integrated onto the output load C_L, the parallel combination of the second-stage DAC capacitance, C_{s2}, and the comparator parasitic capacitance, C_o. M3 and M4 act as cascodes during this phase, with the V_{xp}/V_{xn} nodes following the V_{op}/V_{on} nodes to maintain adequate overdrive voltage to buffer the input pair current. Output integration continues until the voltage at nodes V_{op}/V_{on} drops below the threshold voltage of PMOS transistors M5/6, at which point the regeneration phase begins. The capacitance at the output nodes is generally much larger than the internal capacitance at the V_x nodes, so this phase is usually much longer than internal integration and most integration gain is achieved during this phase. At the end output integration, the integration gain G_{int} will be [3]

$$G_{int} \approx \left(\frac{g_m}{I_D}\right)_{1,2} \left\{ V_{T5,6} + \frac{C_X}{C_{s2} + C_o} \left(V_{T5,6} + V_{T3,4}\right) \right\} \tag{2.1}$$

Fig. 2.4 shows the equivalent circuit and transient waveforms during regeneration. Once the PMOS devices turn on, the amplifier acts as a positive feedback latch until *clk* is deasserted. At the end of the regeneration phase, the total amplifier gain, G is

$$G \approx G_{int} \cdot e^{T_{regen}/\tau} \tag{2.2}$$

where T_{regen} is the total regeneration time and τ is the regeneration time constant, given by

$$\tau \approx \frac{C_{s2} + C_o}{g_{m5,6}} \tag{2.3}$$

Fig. 2.5 shows the amplifier gain as a function of time. An extrapolated version of the integration gain is shown as well to highlight the speed advantage of

the positive feedback stage. For a gain of 32, adding positive feedback to the amplifier increases the speed by more than two times.

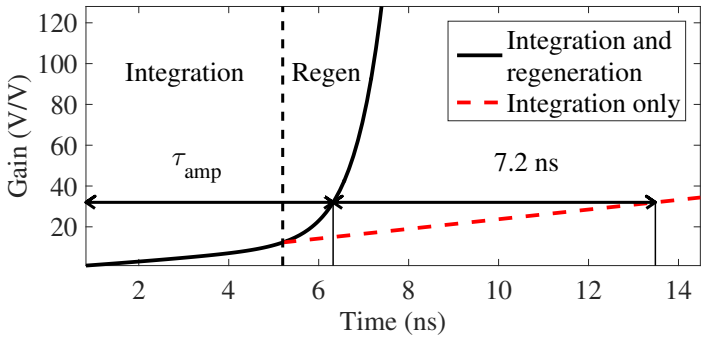

Figure 2.5: Simulated amplifier gain (with extrapolated integration curve)

2.2.2 Noise

Most amplifier noise analysis relies on the assumption that all node voltages are in a steady state and their RMS noise does not change with time. For dynamic circuits, this assumption does not hold, as the RMS noise and gain are both a function of time. In order to calculate the noise for dynamic circuits, expressions utilizing stochastic differential equations must be used [6]. In order to calculate the amplifier noise during the integration and regeneration stages, the time-domain noise of a common-source amplifier with RC load during settling can first be calculated. Fig 2.6 shows the half-circuit of a differential common-source amplifier and its noise model. $I_0(t)$ represents the transconductance of M1 and $I_n(t)$ represents the combined noise current of M1 and the resistor R. The single-sided noise current power spectral density

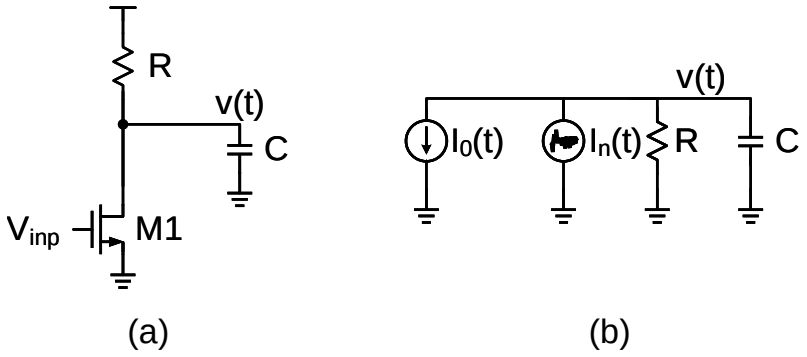

Figure 2.6: (a) Common-source amplifier with RC load half-circuit (b) Noise model

(PSD) of I_n is

$$\overline{I_n^2} = 2kT(\frac{1}{R} + \gamma g_m) \tag{2.4}$$

where γ is the transistor white noise factor and g_m is the transconductance of M1. The differential equation for the voltage at node $v(t)$ is

$$C\frac{dV}{dt} = -\frac{V}{R} + I_0(t) + I_n(t) \tag{2.5}$$

$v(t)$ will have both a signal and noise component, expressed as

$$v(t) = S(t) + N(t) \tag{2.6}$$

By separating the signal and noise components and rearranging terms, the noise component is the stochastic differential equation

$$dN = -\frac{N}{RC} + \frac{I_n(t)}{C}dt \tag{2.7}$$

This is a form of the Langevin equation. By using the general solution of the Langevin equation, the noise power during settling can be calculated as

$$E(v^2(t)) = exp\left(\frac{-2t}{RC} \cdot E(v_0^2)\right) + \frac{kT(1+\gamma g_m R)}{C} \cdot \left(1 - exp\left(\frac{-2t}{RC}\right)\right) \tag{2.8}$$

where $E(v_0^2)$ is the initial noise voltage at $v(t)$. If C is completely reset at the beginning of settling, which will be the case for the proposed amplifier, the initial noise will be

$$E(v_0^2) = \frac{kT}{C} \tag{2.9}$$

For complete settling, $t >> RC$, and Equ. 2.8 reduces to

$$E(v_t^2) = \frac{kT(1+\gamma g_m R)}{C} \tag{2.10}$$

This result matches the noise calculated from traditional PSD-based noise analysis for completely settled circuits. Integration can be treated as a special case of Fig. 2.6 with $R = \infty$ and Equ. 2.8 reduces to

$$\begin{aligned} E(v_t^2) &= \frac{kT}{C} + \frac{2kT\gamma g_m}{C^2} \cdot t \\ &= \frac{kT}{C} \cdot (1 + \gamma G_{int}) \end{aligned} \tag{2.11}$$

and the input-referred integration noise is

$$\overline{v_{in}^2} = \frac{kT}{C} \cdot (\frac{1}{G_{int}^2} + \frac{\gamma}{G_{int}}) \tag{2.12}$$

This equation shows that the input-referred noise improves with larger integration gain. The regeneration case is also a special case of Fig. 2.6 with $R = -1/g_m$. Plugging in $-1/g_m$ for R and calculating the input-referred noise during regeneration yields

$$\overline{v_{in}^2} = \frac{kT\gamma}{C} + v_0^2 \tag{2.13}$$

In the regeneration case, both the signal and noise power scale by G_{regen}^2 so the input-referred noise does not depend on gain. The noise models during

integration and regeneration are combined in Fig. 2.7 to model the noise of the proposed amplifier that combines integration and regeneration. Initially, the switches connected to *int* are closed, and the noise from the input differential pair is integrated onto C. At the end of integration, the *int* switches open and the $\overline{int}$ switches close and regeneration begins. Equ. 2.11 gives the noise at the end of the integration phase. To calculate the noise at the end of regeneration, v_0^2 is set to the noise at the end of the integration phase and the total input-referred noise will be

$$\overline{v_{in}^2} = \frac{kT}{C} \cdot \left(\frac{1+\gamma}{G_{int}^2} + \frac{\gamma}{G_{int}} \right) \tag{2.14}$$

For sufficiently large integrator gain, the additional noise penalty incurred from the regeneration stage should be small, allowing for a large increase in amplification speed without a large loss in SNR.

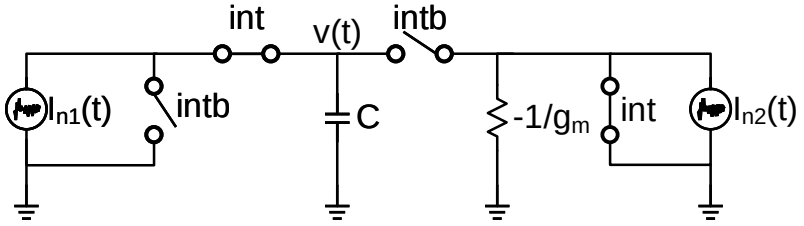

Figure 2.7: Noise model for proposed amplifier with integration and regeneration phases

The proposed amplifier was simulated across operating conditions in order to validate the accuracy of the noise model. In Fig. 2.8, the input pair's G_m/I_D was swept and its noise was measured. Since integration gain is linearly proportional to G_m/I_D, the noise should reduce by the square root of G_m/I_D.

The dashed blue line shows extrapolated noise calculations based on this relationship and the noise value for the maximum G_m/I_D. The simulation results generally track the calculation, and the maximum error is less than 10%. The

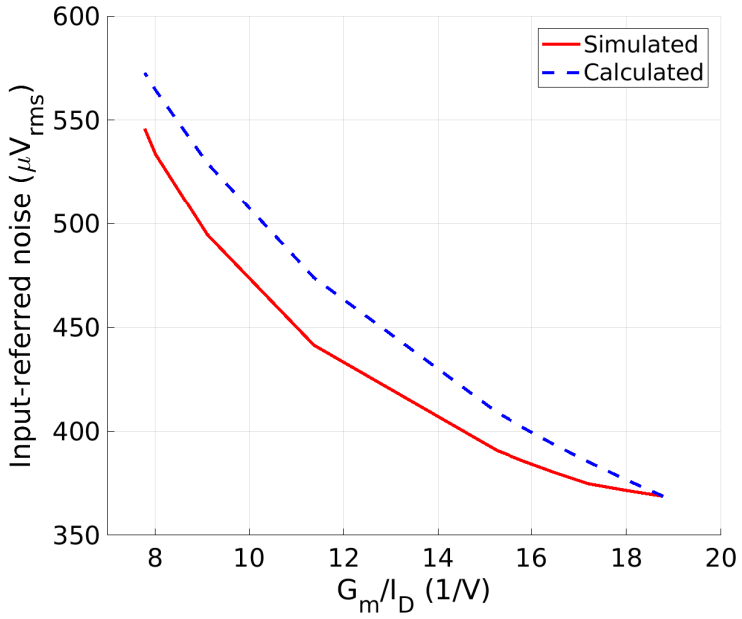

Figure 2.8: Proposed amplifier input-referred noise vs. G_m/I_D

time-domain behavior of the amplifier's noise was also characterized. Fig. 2.9 shows the calculated and simulated input-referred noise across amplification time. Noise is calculated by using transient operating points and the loading conditions of the simulated amplifier to obtain the necessary terms in Equ. 2.14. During integration, the input-referred noise decreases proportional to $\sqrt{t}$ and once regeneration begins the input-referred noise becomes constant, matching the expected behavior.

By adding a tail current source, the sensitivity of the amplifier's noise to

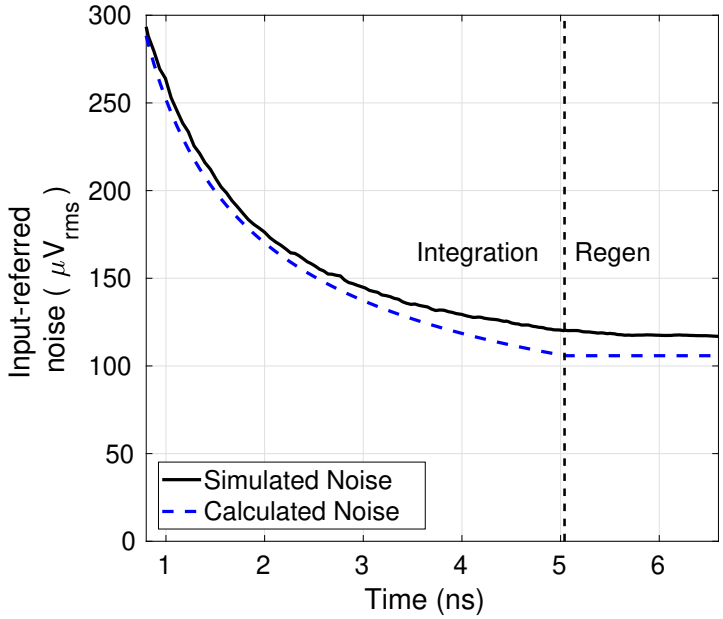

Figure 2.9: Comparison between calculated and simulated input referred noise for the proposed amplifier

its input common-mode is greatly reduced. The addition of the current source helps to stabilize the input pair's G_m/I_D across the input common-mode, maintaining a relatively constant integration gain and therefore a relatively constant input-referred noise. Fig. 2.10 plots the amplifier noise with and without the tail current source. Without the tail current source, the noise varies by more than two times across a 200 mV input common-mode range. Adding the current source reduces that variation to approximately 20% over the same input-common mode range. In high speed systems, the ADC is typically driven by a low-impedance source follower. The output voltage of the source follower can vary along with its threshold voltage, which can easily vary by 200 mV across process and temperature, so the proposed amplifier's

addition of a tail current source can greatly reduce the noise penalty across input common-mode range.

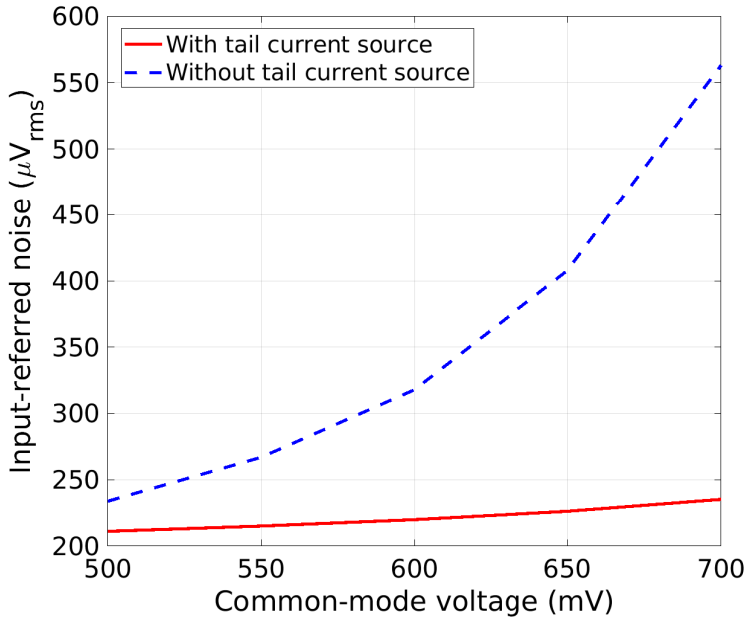

Figure 2.10: Noise variation across common-mode

One key advantage of this amplifier topology is that its operation can easily be tuned for noise and speed requirements. In the integration phase, input-referred noise is inversely proportional to integration time, which is controlled by the bias current and load capacitance [24]. In the regeneration phase, input-referred noise is inversely proportional to load capacitance and is attenuated by the integration gain. For low speed and low noise designs, the integration time can be maximized by reducing the bias current. For high-speed designs with less stringent noise requirements, the bias current can be increased to minimize integration time. Whenever possible, the load capaci-

tance should be minimized so that the regeneration phase can be as fast as possible while still meeting noise requirements. For a given integration time, the input pair's g_m/I_D should be large so that the noise contribution from the regeneration phase is minimized. By carefully controlling bias current and load capacitance, this topology can be used across a wide range of noise and speed requirements.

2.2.3 Linearity

The final major consideration for this amplifier topology is its linearity. In general, the integration phase should be more linear than the regeneration phase, since its gain changes linearly with g_m, whereas the regeneration gain changes exponentially with changes in g_m. By maximizing the integrator gain, and therefore the input pair's G_m/I_D, the linearity should also be maximized. Fig. 2.11 plots the simulated typical corner SFDR across input pair G_m/I_D for the proposed amplifier. The general trend is that larger integration gain results in better linearity, which matches expectation. Another system-level consideration for the amplifier linearity is the first-stage quantizer resolution. Larger first-stage quantizer resolution results in a smaller input swing at the amplifier input, which results in improved amplifier linearity. Larger first-stage quantizer resolutions also generally imply lower speed, since extra conversions are required, so the first-stage quantizer resolution should be set to ensure linearity targets are met without unnecessarily slowing down the conversion speed. Fig. 2.12 plots the worst case SFDR for various first stage quantizer

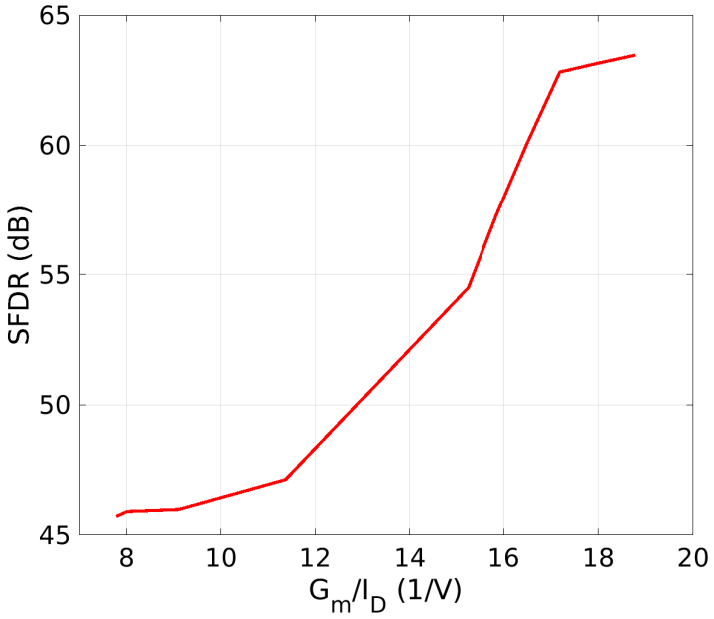

Figure 2.11: Proposed amplifier SFDR vs. G_m/I_D

resolutions and gains from 8 to 64. The dashed horizontal lines represent 6-bit and 7-bit linearity for the black and red lines, respectively. This plot shows that a gain of 64 will not have sufficient linearity for most pipeline designs. The gain of 16 can easily achieve 7-bit linearity with a moderate first-stage resolution of 6 bits. The amplifier can also feasibly achieve a gain of 32, but it requires a first-stage resolution of 8 bits for reasonable linearity. With a well-designed integrator stage, the proposed amplifier can achieve reasonable linearity with only a moderate first-stage resolution.

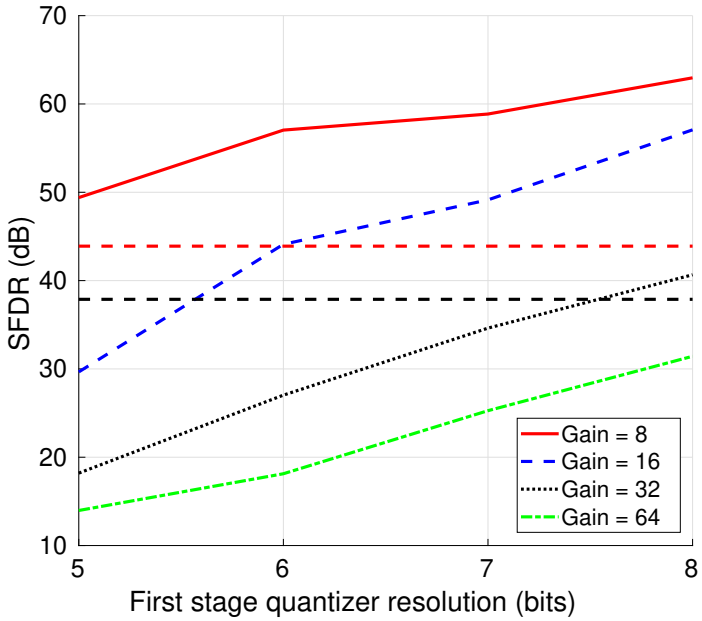

Figure 2.12: Proposed amplifier SFDR vs. input swing

2.3 Pipeline ADC Architecture

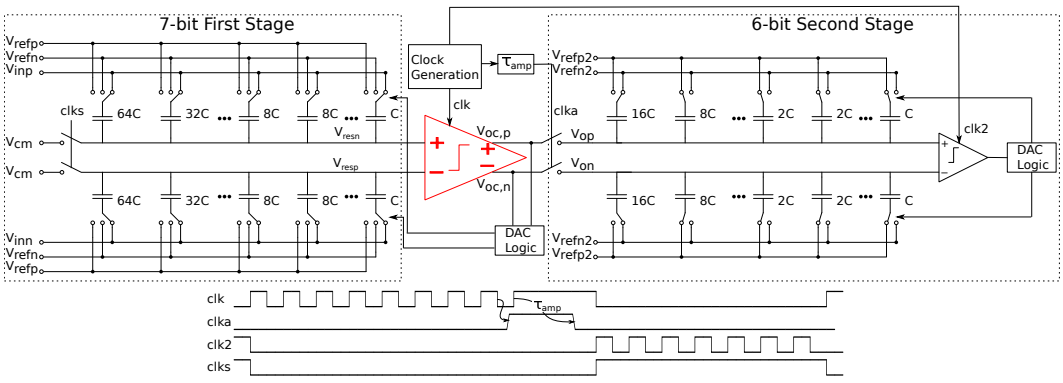

Figure 2.13: Proposed pipeline ADC architecture and timing diagram.

The proposed amplifier from Section 2.2 was integrated into the 12-bit, 10 MS/s two-stage SAR-based pipelined ADC shown in Fig. 2.13. The first-

stage resolution of 7 bits was chosen to reduce the amplifier input swing and eliminate the need for gain non-linearity calibration. Both SAR sub-ADCs use the bidirectional single-sided switching technique from [2] in order to minimize reference energy and reduce the required DAC capacitance. Redundant capacitors are added to overcome the common-mode voltage shifts that occur while using the bidirectional switching scheme. The redundant capacitors ensure the critical conversion cycle will happen after the common-mode voltage shifts become small. By doing this, the offset matching between the comparator operation and amplifier operation is maintained. The amount of required redundancy is significantly reduced by the tail current source in the proposed amplifier. Fig. 2.14(a) shows the common-mode variation across conversion step for the bidirectional switching scheme. Fig. 2.14(b) shows the 1-sigma offset mismatch caused by the common-mode variation for the proposed amplifier with and without the tail current source. Adding the tail current source reduces the maximum offset-mismatch from 23 mV to 3 mV, a reduction of more than 7 times. A voltage-controlled delay line (VCDL) is used to control the amplification time and its delay is tuned to a gain of 32.

Sharing the amplifier and comparator has many benefits. First, no additional amplifier hardware is needed to enable residue amplification, reducing the system hardware complexity. Second, no calibration for offset mismatch needs to be done and the comparator input pair can be sized only to meet noise requirements without regard for offset. With standard residue amplifiers, a mismatch between the amplifier and comparator offsets will cause an

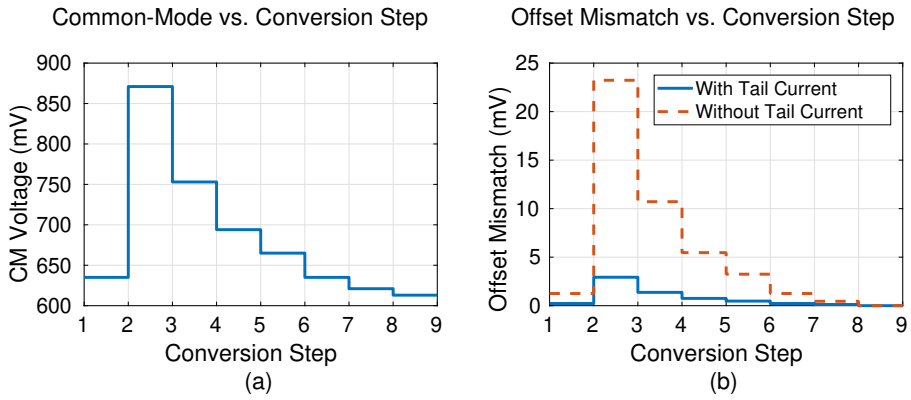

Figure 2.14: (a) Common mode variation across ADC conversion steps (b) Offset mismatch across ADC conversion steps

increase in the input swing seen by the amplifier. This increased output swing is especially harmful for dynamic open-loop amplifiers, where non-linearity is usually very sensitive to input swing. In the proposed amplifier topology, the offset seen during comparator operation and amplifier operation are the same, so even a very large offset will have no effect on the ADC functionality. To illustrate this point, Figure 2.15 shows the offset in comparator and amplifier mode from a 10000 run Monte Carlo simulation, showing that the offsets in both modes are almost perfectly correlated. Finally, since the amplifier sees the much larger second-stage DAC capacitance in amplification phase, the noise and speed can be optimized separately for comparator and amplifier operating modes by changing the ratio of comparator parasitic capacitance to second-stage DAC capacitance. Table 2.1 shows a comparison of important performance parameters for the proposed amplifier when it is in comparator and amplifier operation. When in comparator mode, the noise is only re-

quired to match the first-stage resolution, so the comparator can work in a high speed, high noise mode. Once the second stage DAC capacitance is connected, the amplifier works in a lower speed, lower noise mode. Additionally, Table 2.1 shows that from an energy perspective, the amplifier operation is approximately equivalent to firing the comparator an extra two times, highlighting the power efficiency of the proposed amplification method. Sharing the amplifier and comparator reduces hardware complexity, eliminates offset calibration, and still enables separate optimization between comparator and amplifier operating modes.

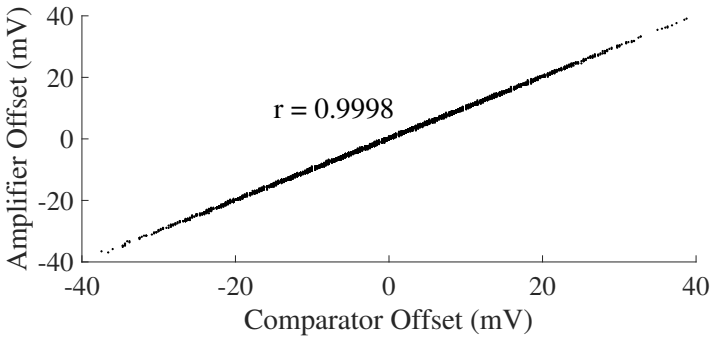

Figure 2.15: Amplifier offset vs. comparator offset and correlation coefficient for a 10000 point Monte Carlo simulation

Table 2.1: Performance comparison between comparator and amplifier operating modes.

	Comparator mode	Amplifier mode
Input-Referred Noise (μV_{rms})	344	101
Integration Time (ns)	0.98	5.2
Regeneration Time Constant (ns)	0.19	1.8
Offset (mV_{rms})	10.67	10.71
Energy per Operation (fJ)	86	148

2.4 Measurement Results

The ADC described in Section 2.3 was fabricated in 130 nm CMOS technology. Fig. 2.16 shows the die photo and layout of the chip. Capacitor mismatch was calibrated in the foreground with a single input. For this proof of concept, the VCDL delay was calibrated to achieve the desired gain in the foreground with a single input, but this work could easily be extended to place the delay-line in an interstage gain background calibration loop to ensure robustness against process, voltage, and temperature (PVT) variation. Fig. 2.17 shows the measured output spectrum with a Nyquist input. The measured SNDR and SFDR at Nyquist was 63.2 dB and 75.4 dB, respectively, leading to a 10.2-bit ENOB. The ENOB was mostly limited by the jitter of the voltage controlled delay line. The total measured power was 280 μW, of which 83% was digital power. Fig. 2.18 shows the power breakdown between digital, analog, and reference power. Fig. 2.19 shows the SNDR/SFDR across input frequency and input amplitude. The dynamic range of the ADC was measured to be 63.9 dB. These numbers translate to a Schreier FoM of 166.4

dB. As this work is mainly a proof of concept, much optimization is possible to further improve the performance. Additionally, this architecture uses only scaling-friendly components and consumes only dynamic power. Fabricating this design in a more advanced process than 130 nm would provide significant performance benefits. Table 2.2 shows that this prototype achieves the largest interstage gain among other state of the art dynamic amplifier works.

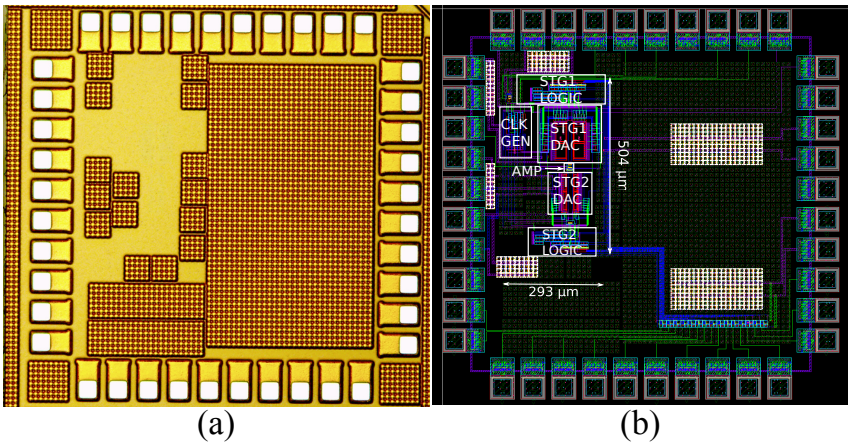

Figure 2.16: ADC (a) die photo and (b) layout.

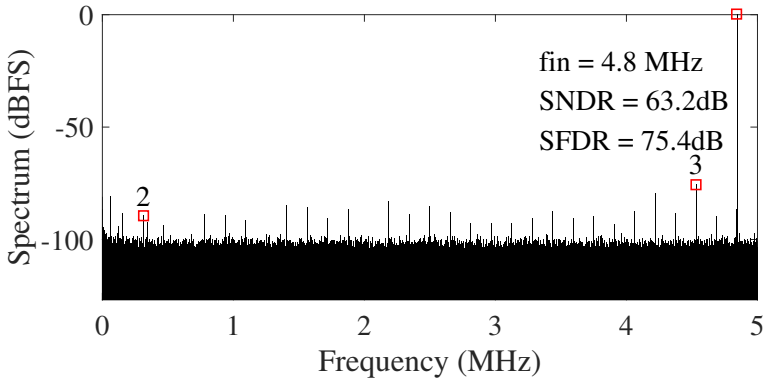

Figure 2.17: Measured ADC output spectra with 32768 points.

Figure 2.18: (a) Measured power breakdown (b) Analog and delay line power breakdown

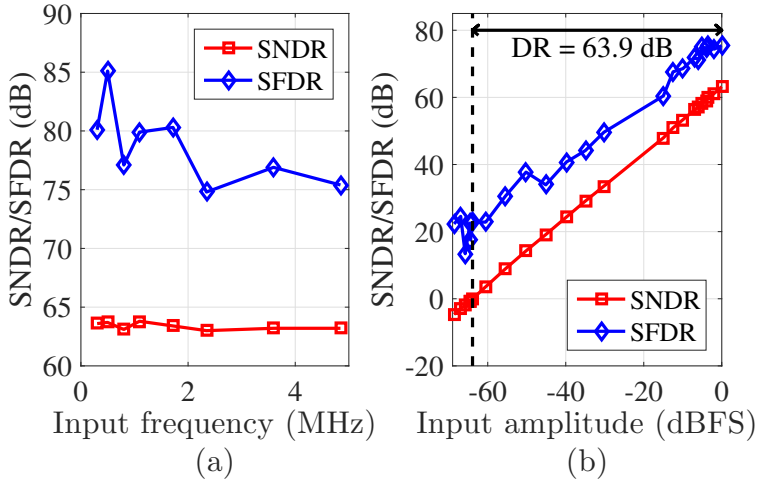

Figure 2.19: Measured SNDR and SFDR vs. (a) input frequency and (b) input amplitude.

Table 2.2: Performance Comparison

	[24]	[27]	[23]	[11]	**This work**
Process (nm)	28	40	65	90	**130**
Architecture	Pipe SAR	Pipe SAR	Pipe SAR	Pipeline	**Pipe SAR**
Res. Amp Architecture	Dynamic	Dynamic	Static open-loop	Dynamic	**Dynamic**
Interstage Gain	16	4	16	3	**32**
Supply Voltage (V)	1.0/1.8	1.1	1.0/1.2	0.5/0.55	**1.2**
Sampling Rate (MS/s)	80	250	160	160	**10**
SNDR (Nyq) (dB)	66	56	66.2	38	**63.2**
ENOB (bit)	10.7	9.0	10.7	6.0	**10.2**
Power (mW)	1.5	1.7	11.1	2.43	**0.28**
HF Walden FoM (fJ/step)	11.5	13.2	41.6	234.0	**23.7**
HF Schreier FoM (dB)	170.3	164.7	164.8	143.2	**166.4**

Chapter 3

A 172dB-FoM Pipelined SAR ADC Using a Regenerative Amplifier with Self-Timed Gain Control and Mixed-Signal Background Calibration

3.1 Introduction

With technology scaling, open-loop dynamic integrators have become an attractive choice for residue amplifiers of pipelined SAR ADCs [24, 27, 15, 11]. A dynamic integrator has two key merits. First, it consumes only dynamic power (no static power), and thus, is much more power efficient than a traditional closed-loop amplifier. Second, it has low noise; in fact, it can be proved that an integrator achieves the lowest noise for a given power budget. Despite these merits, it brings challenges: 1) its maximum achievable gain is limited by the power supply voltage and the transistor g_m/I_D, and is typically less than 10; 2) it requires accurate offset calibration to match the offset of the integrator with the SAR comparator [27, 15, 24]. Offset mismatch increases the amplifier input swing and can cause significant linearity degradation for a dynamic integrator, as its linearity is much more sensitive to the input swing than a closed-loop amplifier; 3) its gain is linearly proportional to the integration time, resulting in a strict trade-off between the amplifier gain and speed.

To address these issues, the authors proposed in Ch. 2 to reuse the strongARM latch comparator in the SAR as a dynamic amplifier, thus removing the need for any offset calibration between the SAR comparator and the residue amplifier. It also naturally combines a front-end integrator, to achieve high noise efficiency, with a backend regenerative positive feedback stage, to attain high gain at high speed with negligible noise penalty as shown in Fig. 3.1.

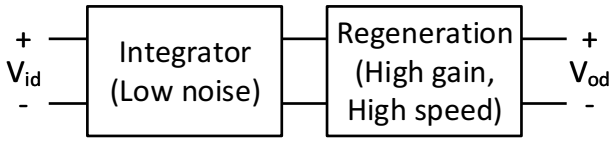

Figure 3.1: Block diagram of a regenerative amplifier in Ch. 2.

Furthermore, this architecture automatically realizes load switching to dynamically adjust the comparator noise and power. When it operates as the SAR comparator, the load is small inverter buffers that drive the SAR logic, and thus, is low power but high noise. When it acts as a residue amplifier, the load is a much larger second-stage SAR input capacitor, and thus, its input referred noise is reduced, which ensures an overall high ADC SNR.

Nevertheless, there are two critical challenges of dynamic amplifiers that the work of Ch. 2 has not addressed: 1) the amplifier gain depends on time, and thus, it requires an accurate and low jitter clock to control the amplification time, but the clock generation is nontrivial and can be power consuming; 2) the amplifier gain, relying on g_m and time, is sensitive to PVT variation. The clock requirement is especially stringent for amplifiers utilizing regeneration Ch. 2, as the gain increases exponentially with time instead of

linearly. In Ch. 2, a voltage-controlled delay line (VCDL) was used to control the gain, but its high jitter caused large gain variations, resulting in ADC SNR degradation. Moreover, the VCDL delay did not track the amplifier gain across PVT variation. Digital background calibration can be used to sense the analog gain variation and adjust the digital gain to match it [24]. This technique improves ADC SNDR, but it does not address the root cause of the problem: *the amplifier gain still varies with PVT*. Amplifier gain variation causes several issues. First, extra redundancy has to be added to ensure that the largest possible gain under PVT variation does not overload the second pipelined stage. Second, when the amplifier gain drops, the noise contribution from the later pipelined stages increases, causing SNR degradation that cannot be mitigated by digital calibration. Third, the digital gain is no longer a power of 2, requiring a tunable fractional multiplier that increases power and design complexity. Besides digital background calibration, other techniques to tackle gain PVT variation use interpolation [11] or replica [8], but these techniques often require power that is comparable to the power of the dynamic amplifier.

This work introduces a low-power self-timed gain control block that provides enhanced robustness to PVT variation. The gain control block is combined with a mixed-signal background calibration loop. Fig. 3.2(a) shows the ADC block diagram with the classic gain calibration, where the digital gain is tuned to match a *varying* analog gain. By contrast, Fig. 3.2(b) shows the proposed scheme, where the analog gain is tuned to match a *constant* digital gain. This scheme takes advantage of the unique feature of dynamic amplifiers,

that *the gain can be adjusted simply by changing the amplification time*. This removes the need for extra redundancy to account for increased gain across PVT, and ensures that the analog gain is always large enough to suppress the second stage non-idealities. Additionally, it does not require a fractional digital multiplier running at the ADC sampling rate, as the analog gain can be maintained to be a power of 2 and the digital scaling can be accomplished with a simple bit shift. A prototype in 130nm CMOS validates the proposed techniques and achieves a 4 times power efficiency increase compared to Ch. 2.

This chapter is organized as follows. Sec. 3.2 describes the proposed gain control block. Sec. 3.3 discusses the proposed mixed-signal calibration. Sec. 3.4 describes the pipelined SAR ADC architecture with self-timed gain control and mixed-signal calibration. Sec. 3.5 shows the measured results.[1]

[1]This chapter is a partial reprint of the publication: Miguel Gandara, Paridhi Gulati, and Nan Sun, "A 172dB-FoM Pipelined SAR ADC Using a Regenerative Amplifier with Self-Timed Gain Control and Mixed-Signal Background Calibration," in *IEEE Asian Solid-State Circuits Conference (A-SSCC), 2017*. I was the primary investigator and designer on this published work.

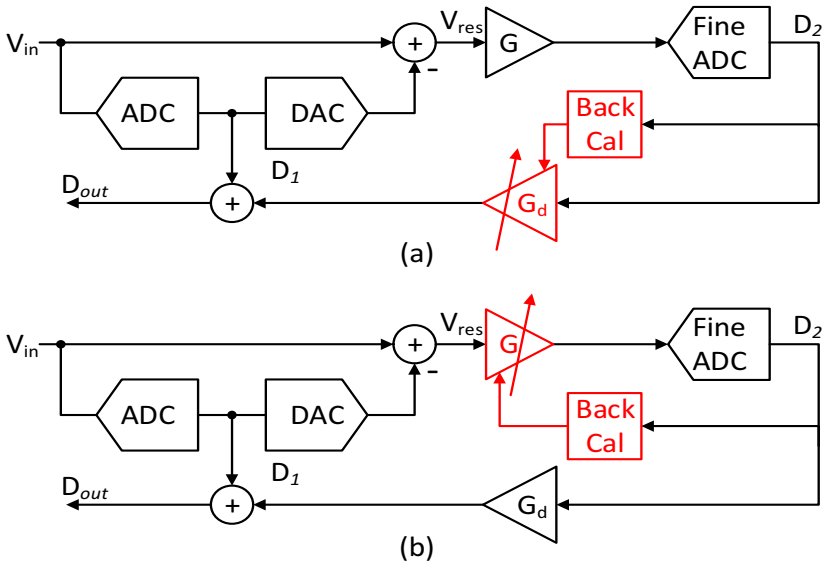

Figure 3.2: Pipelined ADC with (a) digital gain calibration (b) mixed-signal gain calibration

3.2 Proposed Self-Timed Gain Control

Fig. 2.1 shows the schematic of the dynamic amplifier used in this work. When *clka* is asserted, the comparator is configured as the residue amplifier. Fig. 3.3 shows the amplifier output voltages during its amplification phase. The amplifier initially integrates the differential current from M1/M2 onto C_{s2} until the cross-coupled PMOS transistors turn on, at which point the amplifier acts in positive feedback regeneration. For low-noise operation, the integration time is generally set to be much longer than the regeneration time. For the amplifier design used in this work, the integration time is 80% of the total amplification time. Assuming that the differential current is small compared

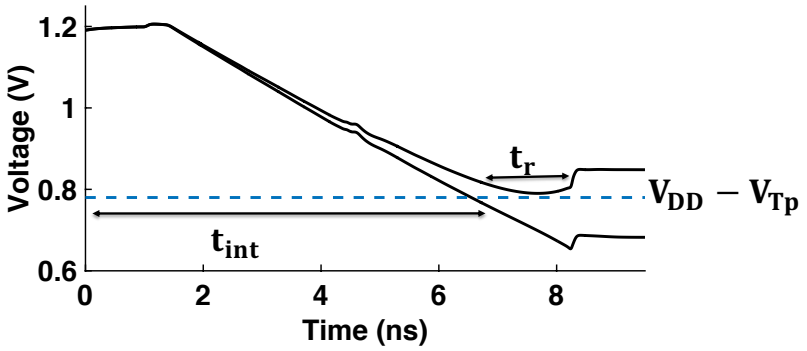

Figure 3.3: Transient output voltages of the proposed amplifier

to the bias current, the time spent in the integration phase is

$$t_{int} = \frac{C_{s2}}{I_D} \cdot V_{Tp} \tag{3.1}$$

where V_{Tp} is the threshold voltage of the cross-coupled PMOS transistors. Since I_D is controlled by a current mirror that is stable across PVT, the variation in integration time is mainly controlled by the PMOS threshold voltage. Since the integration time dominates the overall amplification time, a gain control block that automatically adjusts its delay based on the integration time would provide improved PVT robustness. A tunable delay can be added to this self-timed block in order to adjust the regeneration time to achieve the desired gain. The tunable delay is a small percentage of the overall delay, which reduces the overall jitter of the system.

Jitter is a key consideration for amplifiers that utilize positive feedback, since the output is changing rapidly at the end of the amplification phase. By multiplying the rate of change of the amplifier output during regeneration by

the jitter power, σ_j, the jitter-induced noise, σ_{nj}, can be calculated.

$$\sigma_{nj}^2 = \frac{\sigma_j^2}{\tau_r^2} G_{amp}^2 E\left(V_{in}^2\right) \tag{3.2}$$

where τ_r is the regeneration time constant and G_{amp} is the amplifier gain at the end of amplification. Using Equ. 3.2, the jitter-limited SNR is

$$SNR_j = 20 \cdot log_{10}\left(\frac{\tau_r}{\sigma_j}\right) \tag{3.3}$$

Fig. 3.4 plots the jitter-limited SNR across jitter values for the input sampling network and for the amplifier output. The plot shows that for the same SNR, the amplifier requires much lower jitter levels. Simulations showed that the

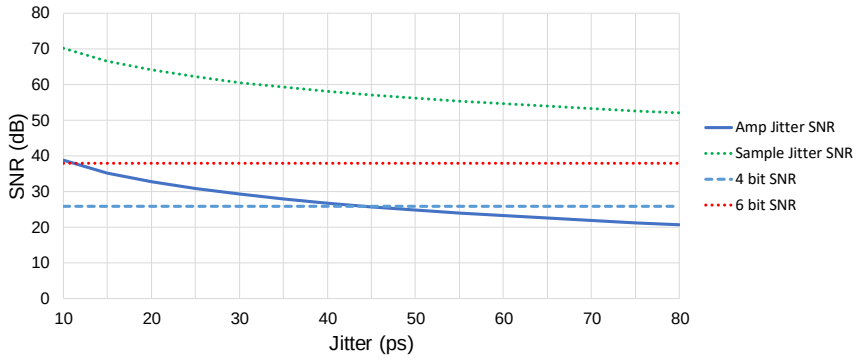

Figure 3.4: SNR vs jitter for continuous time sampling and positive feedback-based amplification

jitter from the VCDL in the prototype from Ch. 2 was around 45 ps, limiting the backend ADC resolution to 4 bits. This large jitter limited the ENOB of the prototype to 10.3 bits, much less than the designed target of 11 bits.

Fig. 3.5 shows the block diagram of the proposed system, which combines a self-timed regeneration detection block that tracks the PMOS threshold

voltage with a tunable delay that is controlled by the mixed-signal calibration described in Sec. 3.3. Both of these functions can be realized using a single dynamic gate, as shown in Fig. 3.6. Two of the SAR shift register outputs, $sar\_ph\langle 1\rangle$ and $sar\_ph\langle 2\rangle$, are used to generate the reset signal, Pre, for a single SAR conversion cycle. The dynamic OR gate turns on once the output

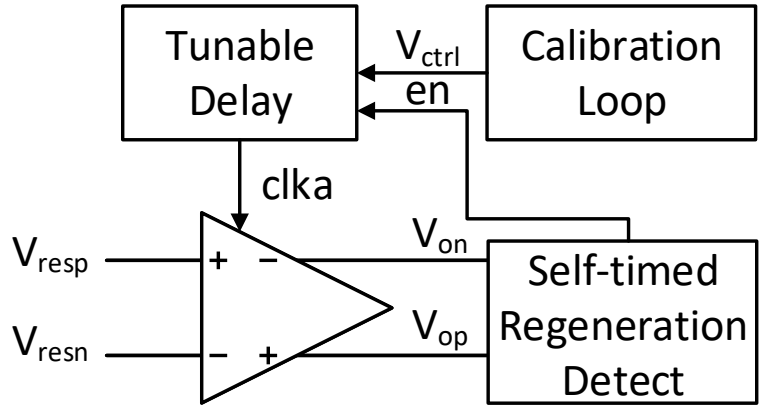

Figure 3.5: Proposed gain control system

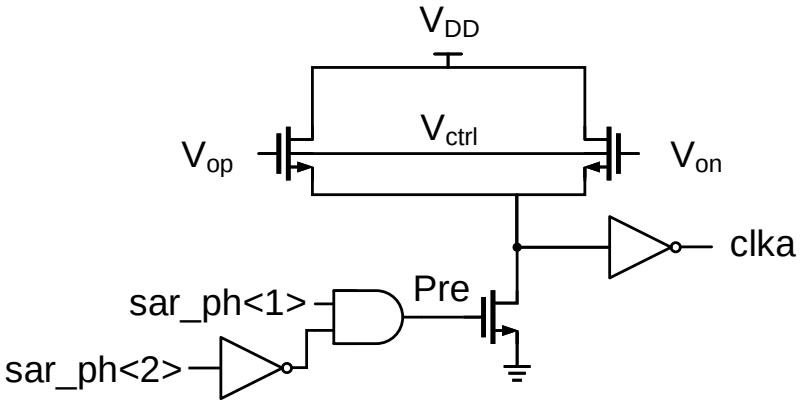

Figure 3.6: Proposed self-timed gain control block

voltage crosses the PMOS threshold voltage, which directly tracks the inte-

gration time across PVT. Additionally, a control voltage, V_{ctrl}, can be applied to the backgate of the PMOS transistors to tune the gate's delay and thus control the regeneration time. Since this implementation is only a single gate, it is both low power and low jitter. The power from the proposed gain control system increases the overall amplifier power by only 10%, compared to a 400% increase in amplifier power from the VCDL in Ch. 2. Figure 3.7 shows the total noise contribution from the timing control blocks for the first prototype from Ch. 2 and from the proposed gain control block. In the first prototype the VCDL dominated the total amplifier noise, contributing 95% of its total noise. The gain control block significantly reduces this contribution, only contributing 1% of the total noise. By adopting this improved gain control scheme, this work is able to achieve an increase in SNDR of 4 dB over the prototype in Ch. 2. The gain control block is sized to ensure any mismatch in the PMOS threshold voltages does not cause significant second-order distortion in the output. The measured gain variation across temperature for the proposed gain control block and the VCDL of Ch. 2 is compared in Fig. 3.8, showing the significant improvement in gain tracking across temperature of the proposed gain control block.

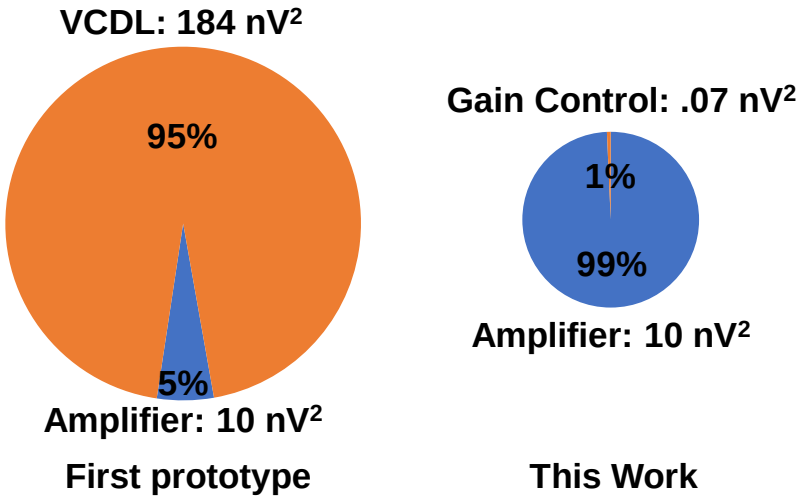

Figure 3.7: Amplifier noise comparison between first prototype and second prototype

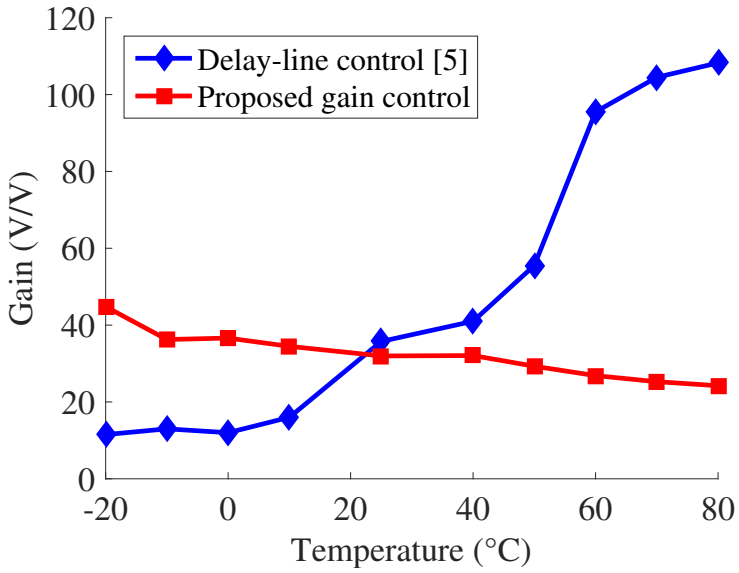

Figure 3.8: Measured amplifier gain vs. temperature

3.3 Proposed Mixed-Signal Calibration

The mixed-signal calibration algorithm shown in Fig. 3.9 is used to precisely control the gain across PVT. Similar to [19, 22], an on-chip pseudo-random number generator (PRNG) outputs a digital dither, R_n, with a value of ± 1 that is applied to the first stage digital to analog converter (DAC) and shifts the residue by one-half LSB of the first stage, $\frac{\Delta_1}{2}$. The digital output

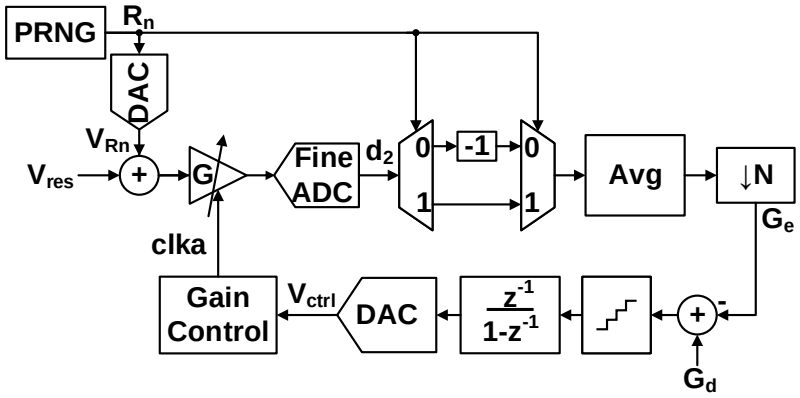

Figure 3.9: Proposed mixed-signal calibration loop

of the second stage is then multiplied by R_n and averaged. The output of the averaging block is an estimation of the gain, G_e, which is

$$G_e = \overline{\left[G\left(V_{res} + \frac{\Delta_1}{2}R_n\right) + \varepsilon_{q2}\right] R_n \cdot \frac{2}{\Delta_1}} = G \tag{3.4}$$

where ε_{q2} is the second-stage quantization noise. As long as $\frac{\Delta_1}{2}$ is well controlled and the averaging block has a low enough bandwidth, G_e can be used to obtain an accurate estimate of the true amplifier gain G. In order to control the gain, the sign of the gain error is applied to a mixed-signal least-mean squares (LMS) loop that controls the backgate voltage of the gain control

block. The effective LMS step size, μ, is controlled by the digital step size of the loop and the voltage step of the DAC. Figure 3.10 shows the gain control sensitivity of the backgate voltage. A 300 mV full-scale range is sufficient for the DAC to correct the gain across all PVT conditions. Based on measurement and simulation results, the required DAC resolution is only 7 bits, allowing for a relatively simple DAC design. By correcting the amplifier gain in the mixed-signal domain, the digital gain applied to the second stage can be implemented as a simple shift register instead of a digital fractional multiplier running at the ADC sampling rate.

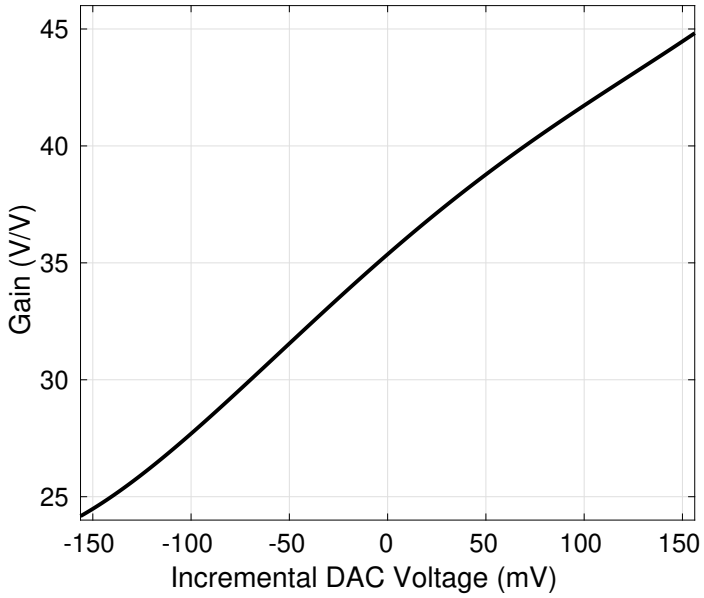

Figure 3.10: Measured gain vs DAC tuning voltage

The mixed-signal calibration loop is low complexity and low power. The multiplication by R_n can be implemented with a demultiplexer/multiplexer

and a negation block. The averager is implemented as a first order infinite impulse response (IIR) exponential moving average filter. The output of the averager is downsampled so that the DAC in the LMS loop runs at a much lower frequency than the sampling frequency, allowing the DAC to be low power. The required 7 bit DAC resolution also ensures extra power does not need to be burned in the DAC to meet noise and lineairty requirements. The off-chip calibration logic was synthesized and, running at low frequency, the simulated power consumption is only 3 μW in 130nm. The on-chip PRNG consumes an estimated 2.1 μW running at $f_s/8$. The clock division ratio of the PRNG was chosen to minimize the power consumption while ensuring the low frequency noise of the dither output was not significantly increased.

3.4 Proposed Pipelined SAR ADC Architecture

Fig. 3.11 shows the architecture of the proposed pipelined SAR ADC. The first stage resolution of 8 bits was chosen to ensure the input swing to the amplifier with the added dither voltage would be small enough to meet the amplifier linearity requirements for a gain of 32. Although the prototype of Ch. 2 was able to achieve a gain of 32 with only a seven bit first-stage resolution, the SNDR of that prototype was limited by the large VCDL jitter, so the non-linearity of the amplifier did not strongly affect the overall ADC performance. With the reduced timing noise of this prototype, the first-stage input swing needed to be reduced in order to meet the 6-bit linearity requirement of the backend ADC at a gain of 32. An additional gain of 4 is achieved by capacitive

attenuation of the reference voltage, providing one bit of redundancy for any DAC errors and the additional dither voltage. The additional loading on the amplifier from the capacitive attenuation also serves to reduce the amplifier noise to the desired level. The prototype uses asynchronous clocking [5] in order to reduce the clock generation logic complexity.

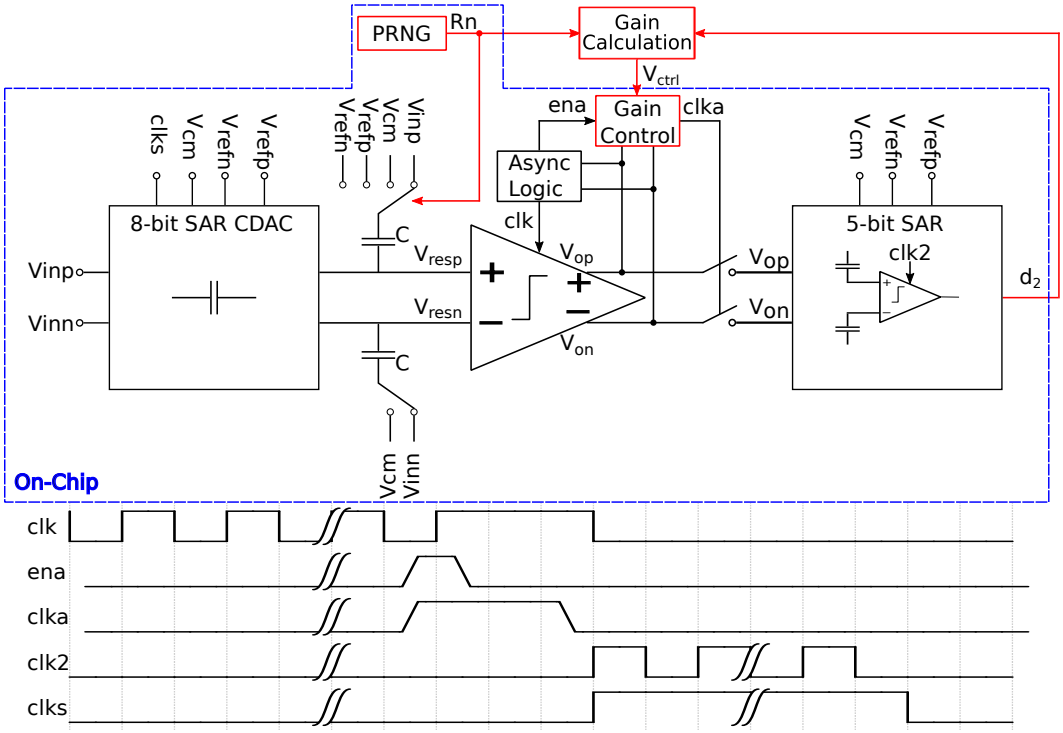

Figure 3.11: Proposed pipeline ADC architecture and timing diagram.

In order to minimize the increased voltage swing caused by the dither voltage, V_{Rn}, V_{cm} is used for the dither application. In traditional bidirectional single-sided switching [2], the V_{cm} application consists of stepping down the dummy capacitor from V_{refp} to V_{cm} on either side of the differential DAC. The problem with this approach is that any error in the common-mode voltage

ε_{Vcm} causes an error in the gain estimator, ε_{Ge}

$$G_e(1+\varepsilon_{G_e}) = G\left(1+\frac{\varepsilon_{Vcm}}{V_{cmi}}\right) \tag{3.5}$$

where V_{cmi} is the ideal common-mode voltage. This imposes a strict requirement on the common-mode voltage to ensure an accurate gain estimation. To overcome this issue, a single dummy capacitor is instead switched from V_{cm} to either V_{refp} or V_{refn}. In this case, the common-mode voltage error gets canceled out in the estimation operation, so even large common-mode voltage errors have negligible effect on the final gain estimation.

3.5 Measurement Results

Fig. 3.12 shows the prototype ADC implemented in 130nm CMOS. Fig. 3.13 shows the measured spectrum. Fig. 3.14 shows the SNDR/SFDR

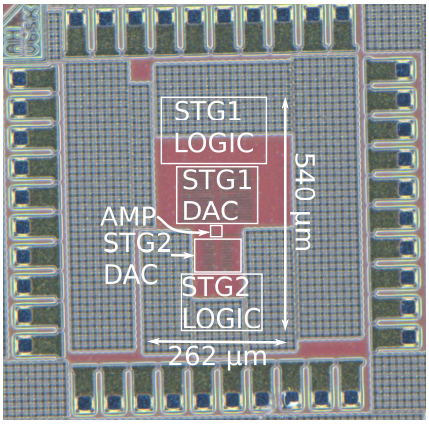

Figure 3.12: ADC die photo

across input frequency and amplitude. Fig. 3.15 shows the measured SNDR

across temperature for the ADC with only a single foreground-calibrated point at room temperature, and for the ADC with background calibration enabled. The averaging filter and DAC control discussed in Sec. 3.3 was implemented using MATLAB. With background calibration, the ADC performance stays relatively stable from -20°C to 80°C. To show the convergence behavior, measurements were taken while the temperature was increased from 25°C to 65°C and then back to 25° C. Fig. 3.16 shows the gain across samples with and without the background calibration enabled. Due to the latency introduced by implementing the averaging and DAC control operations in MATLAB, the gain does not perfectly track the change in temperature initially. However, the number of samples required to achieve convergence is equivalent to 8 ms in the worst case. If implemented in a real-time system, this speed should allow for accurate tracking of environmental changes. The level of gain stability shown in Fig. 3.16 ensures the standard deviation of the SNDR is less than 0.25 dB. Table 3.1 compares the prototype ADC performance with state-of-the-art dynamic-amplifier based ADCs. The low-frequency Schreier FoM is 172 dB and the Nyquist Schreier FoM is 171.2 dB, which is comparable to that of other works fabricated in more advanced processes. Digital power comprises 64% of the total 171 μW, so fabricating this design in more advanced processes would even further improve the power efficiency.

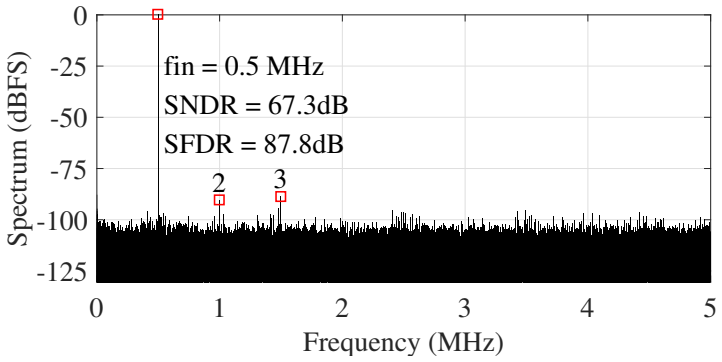

Figure 3.13: Measured ADC output spectra with 32768 points.

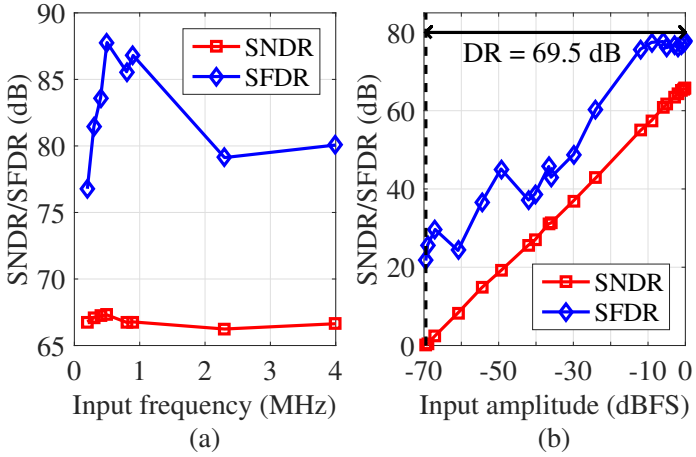

Figure 3.14: Measured SNDR and SFDR vs. (a) input frequency and (b) input amplitude.

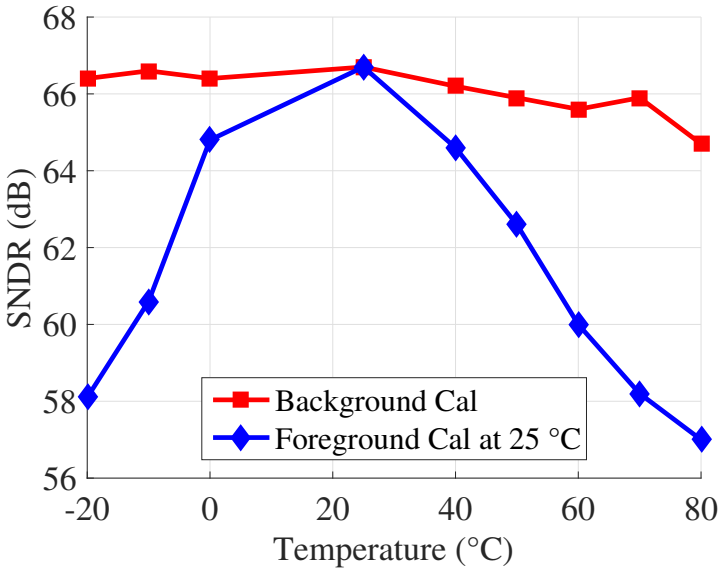

Figure 3.15: Measured SNDR vs. temperature

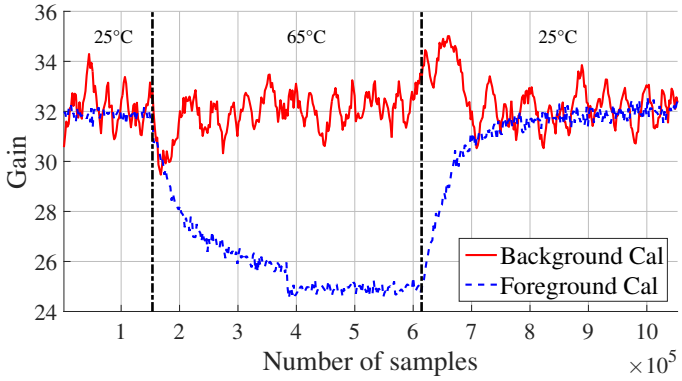

Figure 3.16: SNDR over time with transient steps from 25°C to 65°C to 25° C

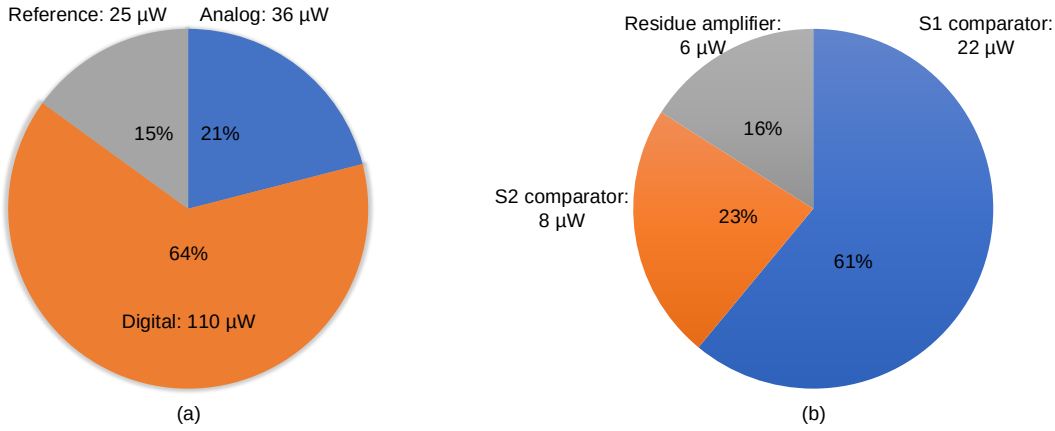

Figure 3.17: (a) Measured power breakdown (b) Analog and delay line power breakdown

Table 3.1: Performance Comparison

	[24]	[27]	Ch. 2	[26]	**This work**
Process (nm)	28	40	130	180	**130**
Architecture	Pipe SAR	Pipe SAR	Pipe SAR	Pipeline	**Pipe SAR**
Requires OTA	No	No	No	Yes	**No**
Requires offline calibration	No	Yes	Yes	No	**No**
Requires offset calibration	Yes	Yes	No	No	**No**
Requires digital fractional multiplier	Yes	No	Yes	No	**No**
Interstage Gain	16	4	32	4	**32**
Supply Voltage (V)	1.0/1.8	1.1	1.2	1.3	**1.2**
Sampling Rate (MS/s)	80	10	10	30	**10**
Peak SNDR (dB)	68	62	63.2	74.2	**67.3**
Peak ENOB (bit)	11	10	10.2	12	**10.9**
SNDR (Nyq) (dB)	66	62	63.2	72	**66.6**
ENOB (Nyq) (bit)	10.7	10	10.2	10.7	**10.8**
Power (mW)	1.5	.07	0.28	6	**0.17**
LF Walden FoM (fJ/step)	9.1	7	23.7	48	**9.2**
LF Schreier FoM (dB)	172	171	166	168	**172**
HF Walden FoM (fJ/step)	11.5	7	23.7	61.5	**9.8**
HF Schreier FoM (dB)	170	171	166	166	**171**

Chapter 4

Digital Filtering Techniques to Reduce SAR ADC Dynamic Energy

4.1 Introduction

Successive Approximation Register (SAR) analog-to-digital (ADC) converters have become widely used due to their energy efficiency and mostly digital nature, which makes this architecture amenable to process scaling. In traditional SAR ADCs, a binary search is performed to determine the output digital code. In this case, an N-bit SAR ADC requires N comparisons per sample. In applications where no assumptions can be made about the input signal, a binary search is the most efficient algorithm. If, however, some assumptions can be made about the input signal characteristics then alternate search algorithms can provide improved performance and reduce reference power [31, 30, 10, 25, 9]. These techniques can help to reduce the power consumption of two blocks that do not scale well in noise-limited designs: the CDAC reference energy and the comparator power. By limiting the CDAC switching to only a few LSBs, the reference energy can be reduced dramatically. Additionally, by reducing the total number of comparisons, the comparator noise can be reduced even for a noise-limited comparator.

Most of the current research has focused on reducing the number of comparisons for low-activity signals, e.g. signals with a small digital code change per sample. These techniques fall into two general categories. Least-significant bit (LSB)-first techniques begin quantization with the LSB, allowing for a reduction of comparisons that is inversely proportional to the code change per sample. Subranging techniques reduce the number of comparison by a fixed amount, given that the code change per sample meets certain requirements.

An LSB-first SAR [31] applies an initial guess to the SAR digital-to-analog converter (DAC) and converts starting from the LSB, as opposed to the most-significant (MSB) bit in traditional SAR ADCs. Once the DAC voltage crosses the input voltage, the conversion moves back towards the LSB. If the initial guess is close to the input voltage, this approach can drastically reduce the number of comparison required to digitize the input signal. Since [31] uses an initial guess of the previous sample, it is only accurate for low signal activity. The usable frequency range of the LSB-first approach can be extended by utilizing a selectable starting bit (SSB) instead of always starting conversion at the LSB [10]. This approach is effective in extending the usable frequency range, however it is still not suitable for signals that have a high pass characteristic.

In general, subranging SAR designs apply a guess voltage to the first m bits of the SAR DAC, and only convert the last $N - m$ bits. As long as the difference between the applied voltage and the input voltage is within the $N - m$ bit window, the final digital value will be correct. In cases where the

difference is larger than the $N-m$ bit window, the subranging SAR can default to standard N bit SAR operation. In [25], a subranging SAR ADC is built that uses the last sample as the applied DAC voltage. As with the LSB-first techniques, only low-activity signals will be inside the subranging window. In [30], the usable frequency range is extended by using a first-order difference equation for prediction instead of the last sample value. While using a first-order difference enables a lower oversampling ratio (OSR), this algorithm will not work well for band-pass or high-pass signals. Additionally, this design includes error protection but does not have an error-recovery mechanism. Another approach reduces reference power even further by limiting switching on the m most-significant bits (MSBs). In this case, the last DAC value for m MSBs is saved and the MSB values are are only changed when the input voltage goes outside the $N-m$ bit window [9]. This technique is only effective when the voltage input voltage stays within the window for many samples, which means that the input signal must change very slowly.

This work extends the previous works to other signal characteristics by applying digital filtering principles to the prediction algorithm. This technique allows for large reference energy reductions in signals that have high-pass and band-pass characteristics. The only requirement on the input signal is that its bandwidth is a fraction of the overall sampling bandwidth. In this work, simulation results are presented for a 10-bit subranging SAR ADC that accurately predicts the first five MSBs and reduces the reference energy by up to 75% compared to a conventional SAR. By utilizing different prediction fil-

ters, the ADC can support input signals of low-pass, band-pass, and high-pass characteristics.

This chapter is organized as follows. Section 4.2 provides the theoretical background for the prediction engine and discusses its implementation. Section 4.3 describes the proposed SAR ADC architecture. Section 4.4 covers the proposed ADC implementation and simulation results.

4.2 Prediction Engine Theory of Operation

The goal of any prediction engine is to generate an estimate of the input signal with minimum error. The expression for the prediction error, X_e, for a given input X and estimator $\hat{X}$ is

$$X_e[n] = X[n] - \hat{X} \tag{4.1}$$

where $\hat{X}$ is a function of the previous samples of X. For the zero-order hold estimator of [31], the error is

$$X_e[n] = X[n] - X[n-1] \tag{4.2}$$

For the first order difference equation of [30], the error is

$$\begin{aligned} X_e[n] &= X[n] - [X[n-1] + (X[n-1] - X[n-2])] \\ &= X[n] - 2 \cdot X[n-1] + X[n-2] \end{aligned} \tag{4.3}$$

By applying the Z-transform to these prediction error equations, the frequency response of the prediction error can be calculated. For the zero-order hold the frequency response is

$$X_e(z) = X(z) \cdot (1 - z^{-1}) \tag{4.4}$$

For the first order difference, the frequency response is

$$X_e(z) = X(z) \cdot (1 - z^{-1})^2 \tag{4.5}$$

Figure 4.1 shows the frequency response of the prediction error for the zero-order hold and first order difference estimators. As expected, both estimators create zeros in the prediction error at DC, meaning the prediction will perform best with low-activity signals. The main advantage of the first order difference estimator is the additional zero the difference operation adds at DC, which extends the usable frequency range for a given error target. By viewing the

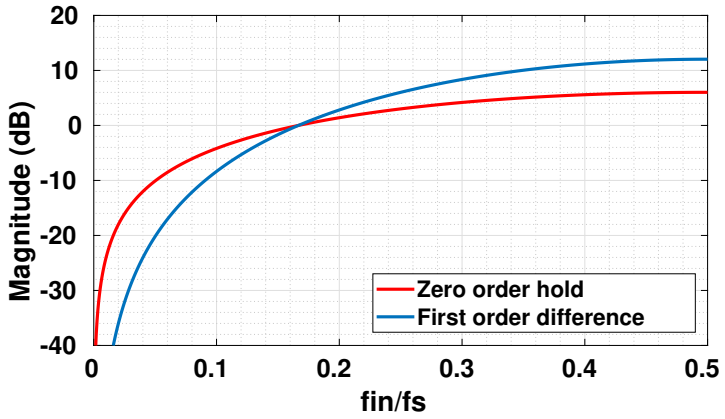

Figure 4.1: Prediction error frequency response for zero-order hold and first order difference estimators

estimator operation as a filtering operation, more advanced prediction filters can be utilized to extend the usable range even further. By shifting the zeros from DC, the in-band prediction error can be further suppressed for the same filter order. Additionally, higher filter orders can also be utilized to further minimize the in-band prediction error. The choice of optimum zero locations

for a given filter order can be calculated by minimizing the integral of the squared magnitude of Equ. 4.1 with respect to its zero locations [18]. Figure 4.2 plots the prediction error magnitude over frequency for second and third-order prediction filters with all zeros at $z = 1$ and zeros optimized for an input bandwidth of $f_s/4$. In order to ensure real filtering coefficients for all filters, any zeros placed away from DC must be conjugate pairs. In the third-order case, the prediction error is minimized by placing the pair of zeros closer to the band edge than in the second-order case. This is due to the third-order filter's extra zero at DC, which provides extra filtering at low frequency that is not present for the second-order filter. The optimum filter coefficients for

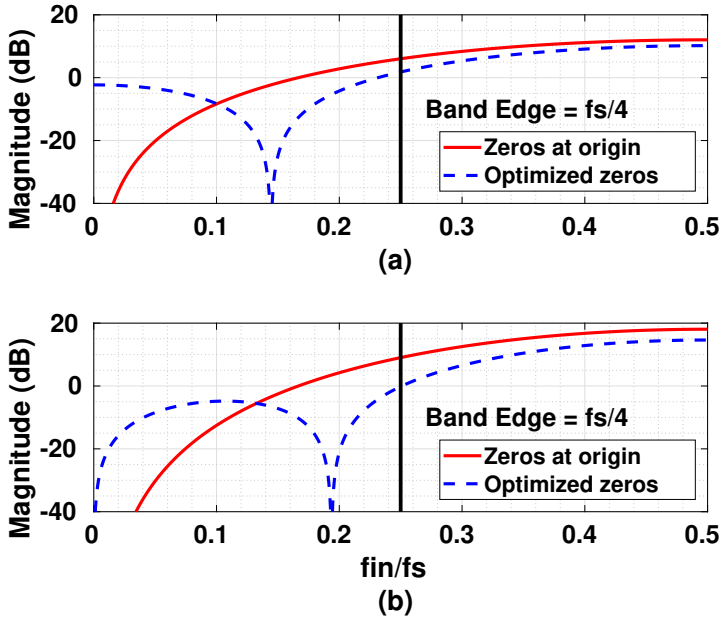

Figure 4.2: Frequency response for (a) second, and (b) third-order prediction filters

various filter orders and the expected reduction in prediction error magnitude is summarized in Table 4.1 [18].

Table 4.1: Zero placement for minimum prediction error

Filter order	Zero locations Relative to band edge	Prediction error improvement (dB)
1	0	0
2	± 0.577	3.5
3	$0, \pm 0.775$	8
4	$\pm 0.340, \pm 0.861$	13
5	$0, \pm 0.439, \pm 0.906$	18

Treating the prediction operation as a filtering operation also opens up the application space for prediction-based ADCs beyond only low-activity signals. As long as the signal is sufficiently band-limited, the prediction filter's coefficients can be modified to accurately predict signals with band-pass or even high-pass shaped input characteristics. The process for translating the optimum low-pass prediction filter to the optimum high-pass or band-pass characteristic is also straightforward. In the case of high-pass shaped input signals, the low-pass filter zeros are shifted by π radians so that all zeros are centered around $f_s/2$. The band-pass will always require double the number of zeros for the same filter order as the high-pass or low-pass cases. This is because the center frequency is no longer at 0 or π radians, so all shifted zeros are in the positive imaginary plane. For real coefficients, an equal number of conjugate zeros must be added, so the total number of zeros doubles. In order to transform the low-pass zeros to band-pass zeros, the zero frequencies are first divided by two to account for the fact that the zero frequency bisects

the signal bandwidth. Next, two sets of zeros are created by shifting the low-pass zeros by ω_0 and $-\omega_0$, where ω_0 is the band-pass signal's center frequency. Fig. 4.3(a) shows the pole-zero plots for an example second-order filter with zeros optimized for a bandwidth of $f_s/8$. Fig. 4.3(a) shows the equivalent filter for high-pass input signals and Fig 4.3(c) shows the equivalent filter for band-pass input signals with center frequency $f_s/4$. With simple transforma-

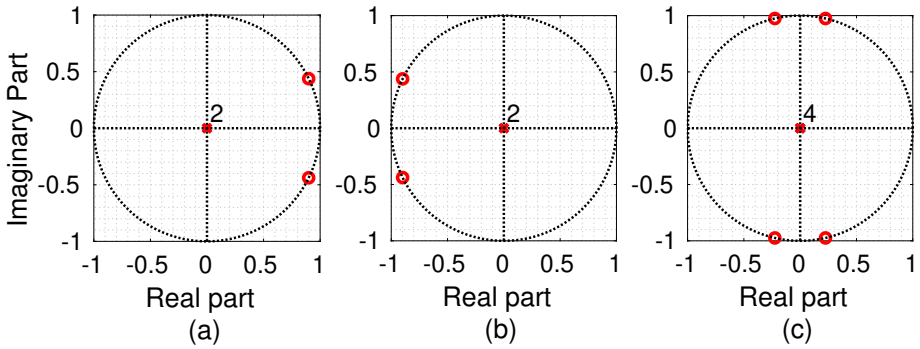

Figure 4.3: (a) Example second-order low-pass filter and its (b) high-pass and (c) band-pass transformations

tions, our prediction ADC architecture can support any band-limited signal characteristic, an expansion of the application space beyond previous work.

In order to evaluate the practical performance of an ADC utilizing our prediction engine, a simple model with an 10-bit input and variable number of predicted bits was built. For an N-bit ADC with M prediction bits, the maximum error for the digital prediction is

$$|D_{pred,err}| < 2^{N-M-1} \tag{4.6}$$

As long as the prediction is within $D_{pred,err}$ of the digital input, the prediction is successful. The success rate for the zero-order hold, first order difference, optimum second-order, and optimum third-order prediction filters is plotted across oversampling ratio (OSR) in Fig. 4.4 for $M = 5$. The OSR is defined as a function of input bandwidth f_{BW}

$$OSR = \frac{f_{BW}}{f_s/2} \tag{4.7}$$

Filter orders above one clearly provide a large benefit in the required OSR,

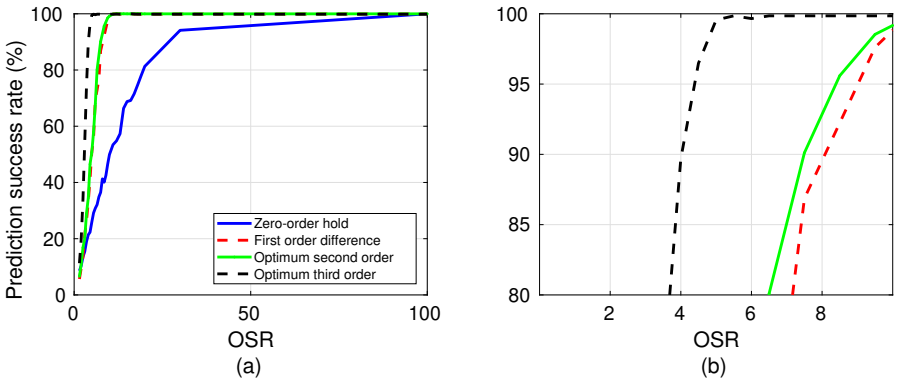

Figure 4.4: (a) Success rate vs OSR for various filter orders (b) Zoomed in view

which directly translates to reduced sampling frequency and reduced power for the same input bandwidth. The optimum second-order filter provides only a small benefit over the first order difference, but the optimized third-order filter can achieve the same success rate as the first order difference with half the required OSR. In order to quantify the achievable OSR across prediction filters and the number of predicted bits, the point at which the success rate surpasses 95% is chosen as the achievable OSR for a given prediction filter. For $M = 5$,

this corresponds to the point where the number of required comparisons is within 10% of its theoretical minimum, so the achievable energy savings is close to maximum. Fig. 4.5 plots the achievable OSR for filter orders between two and five. Filters with optimized zeros provide a larger benefit as the filter

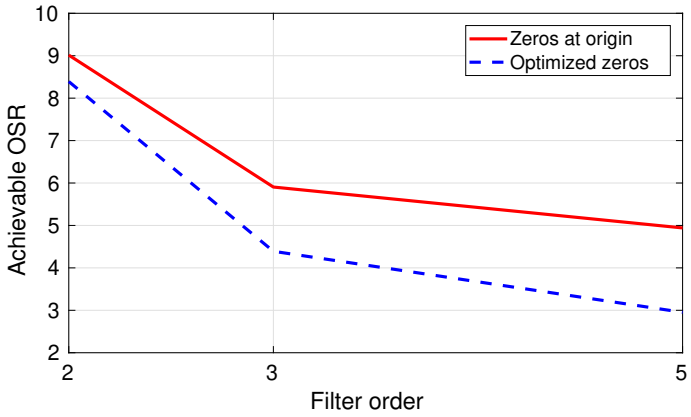

Figure 4.5: Achievable OSR vs filter order

order increases, since the zeros will be spaced more efficiently across the signal bandwidth. For the third and fifth-order filters, the required sampling rate reduces by 25% and 40% when using the optimized zero locations. For the optimized filter, using a third-order filter reduces the required sampling rate by 50% compared to the second-order filter. Using a fifth-order filter reduces the required sampling rate by an additional 33%. In order to balance the achievable sampling rate with the required filter complexity, a third-order filter was chosen for further study. Fig. 4.6 shows the achievable OSR for different numbers of predicted bits using third-order filtering. The optimized third-order filter can achieve a one bit improvement in prediction accuracy for the same OSR. This follows from the predicted error reduction of 8.5 dB given in

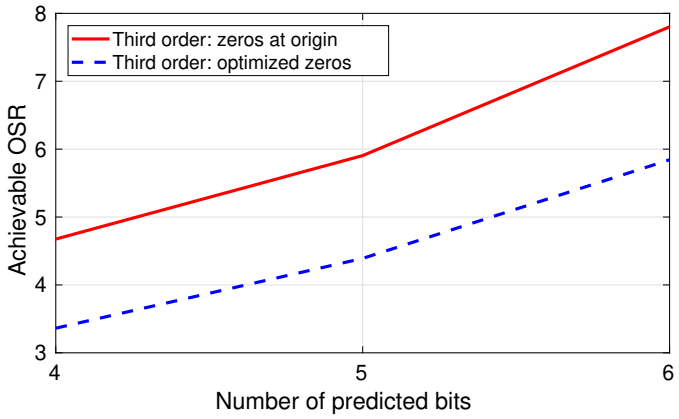

Figure 4.6: Achievable OSR vs number of predicted bits for third-order filters

Table 4.1, which corresponds to more than a bit of error improvement. In order to prove the efficacy of the proposed techniques for other signal characteristics, the third-order filters were transformed for high-pass signals, and the zero-order hold and optimized second-order filters were transformed for band-pass signals. Fig. 4.7(a) shows the success rate across OSR for the high-pass filters, and Fig. 4.7(b) shows the success rate across OSR for the band-pass filters. The success rate across OSR closely matches the results for the low-pass case, as expected. As mentioned, the band-pass filter requires a second-order and fourth-order filter to implement the zero-order hold and optimized second-order performance, respectively. The modeling shows that using higher-order filters allows for dramatic reductions in the required sampling rate, and also allows for accurate predictions across input signal characteristics.

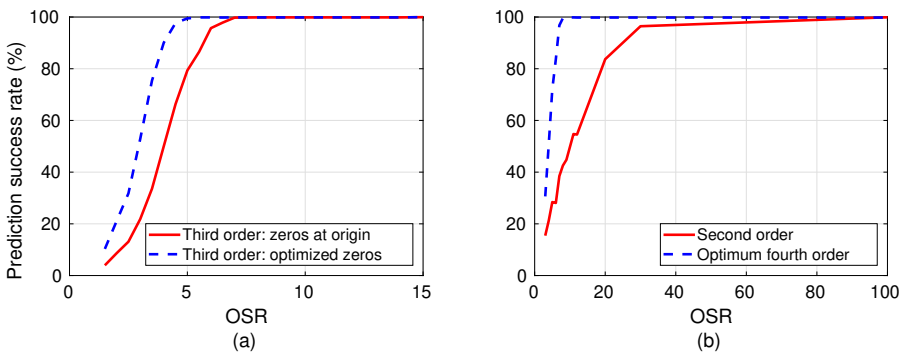

Figure 4.7: Success rate vs. OSR for (a) high pass and (b) band pass prediction filters

4.3 Proposed SAR ADC Architecture

In this work, a subranging SAR design is used. The subranging technique was chosen mainly for its simplified control logic and for its reduced speed penalty. For LSB-first ADCs, the worst-case number of comparisons is $2N$, where N is the resolution of the ADC in bits. For a subranging ADC, the worst-case number of comparisons is $N + k$, where N is the total resolution of the ADC in bits and k is the number of subranged bits. Since any useful implementation of a subranging ADC would have a subrange less than N bits, the subranging ADC will have fewer worst-case comparisons than the LSB-first ADC. Although this work utilizes a subranging ADC, the prediction methodology described in Section 4.2 can be applied to LSB-first ADCs as well.

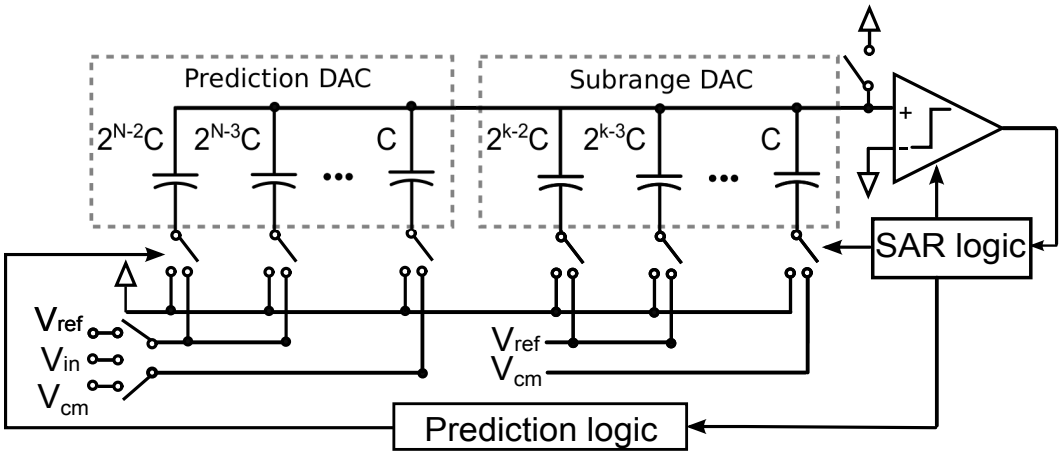

Figure 4.8: Schematic of capacitive DAC for an N-bit ADC with k-bit subranging

4.3.1 Capacitive DAC

Figure 4.8 shows the capacitive DAC for an N-bit prediction ADC with k-bit subranging. For simplicity, only a single-ended DAC is shown. The full DAC consists of two sub-DACs, the prediction DAC and the subranging DAC. Both the prediction and subranging DACs use V_{cm} application on the LSB capacitor in order to reduce the required DAC capacitance by a factor of two [20]. The addition of a subranging DAC addresses the limitations of the binary subranging algorithm used in [25]. In [25], the digital prediction is directly applied to an N-bit DAC and a k-bit binary search is performed utilizing the same DAC. As mentioned in [31], adding a binary step size to an arbitrary initial guess can cause toggling of multiple MSB capacitors per bit-cycle, which will increase reference power consumption. Additionally, this scheme requires a digital adder to calculate the DAC code for each cycle. By

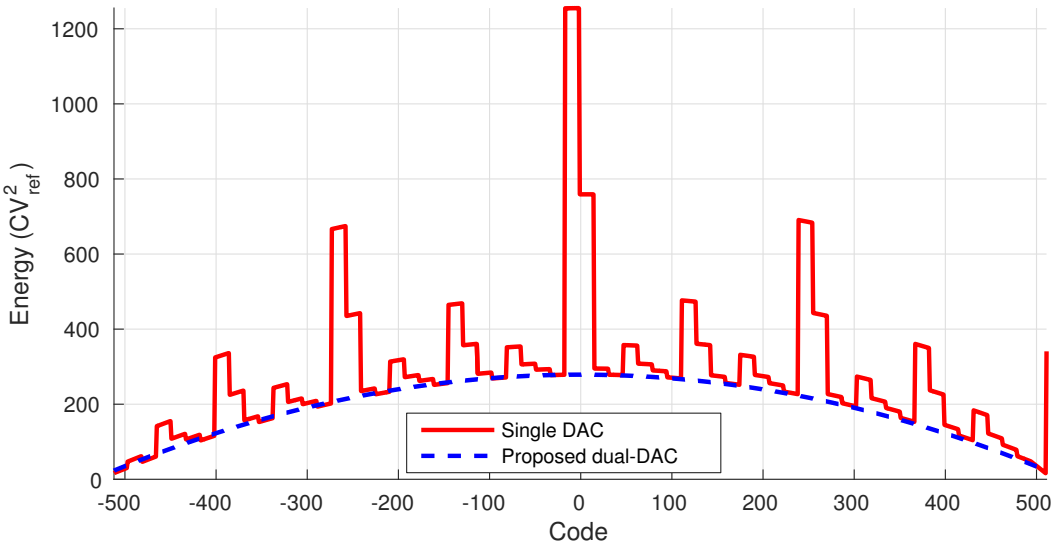

Figure 4.9: Reference energy as a function of input code with a perfect initial guess. Single DAC [25] and the proposed dual-DAC approach are shown.

adding the additional k-bit subranging DAC, the k-bit binary search can be performed without a digital adder and without switching any MSB capacitors. Fig. 4.9 shows the reference energy across digital codes for a 10-bit SAR with 5-bit subranging and a perfect input guess. Even without accounting for the additional digital complexity, adding a subranging DAC reduces reference power by approximately 30% on average.

4.3.2 Subranging Operation

The prediction DAC is used to sample the input voltage and apply the prediction. After sampling the input voltage, V_{in}, the digital prediction is

applied and the final voltage at the top plates of the capacitor array, V_x, is

$$\begin{aligned} V_x &= -\frac{C_N}{C_N + C_k}(V_{in} - V_{pred}) \\ &= -\alpha V_{err} \end{aligned} \tag{4.8}$$

where C_N and C_k are the total capacitance for the prediction DAC and subranging DAC, respectively, and V_{pred} is the ideal output of the prediction DAC. This final voltage is the error of the prediction, V_{err} with an additional attenuation factor, α, from the additional subranging capacitance. Since this error can be positive or negative, the subranging DAC is initialized to $V_{ref}/2$ so that the DAC can increase or decrease the top-plate voltage. The signal-to-noise ratio (SNR) of the ADC also decreases by α, so ensuring a high accuracy guess, and thus a minimized k, is important to minimize SNR degradation.

After applying the prediction, the ADC performs a k-bit SA conversion. The range of the subranging DAC voltage, $V_{DAC,sub}$ is

$$\frac{2^{k-2}-1}{2^{N-1}+2^{k-1}}V_{ref} < V_{DAC,sub} < \frac{2^{k-2}-1}{2^{N-1}+2^{k-1}}V_{ref} \tag{4.9}$$

V_{pred} can be expressed as a function of the digital prediction, D_{pred}

$$V_{pred} = \frac{D_{pred}}{2^{N-1}}V_{ref} \tag{4.10}$$

The digitized input voltage, D_{in} is

$$D_{in} = \frac{V_{in}}{2^{N-1}}V_{ref} + \epsilon_q \tag{4.11}$$

where ϵ_q is the quantization noise. Equ. 4.8, 4.9, 4.10, and 4.11 can be combined to express the maximum error of the digital prediction. The maximum

digital prediction error, $D_{pred,err}$, is given by

$$-2^{k-1} - 1 \leq D_{pred,err} \leq 2^{k-1} - 1 \tag{4.12}$$

where quantization noise is ignored since it contributes a negligible error for a reasonable number of predicted bits. This error range is slightly reduced from the error range calculated in Equ. 4.6 due to the chosen method of error detection, which is explained further in Section 4.3.3, but otherwise matches the expected result. As long as the prediction is in range, the final digital output is obtained by adding the digital prediction value and the digital output from the subranging operation. In this case, the final number of comparisons that are required is k.

4.3.3 Error Detection/Recovery

The proposed ADC uses two methods to detect prediction values that are out of bounds. The first can be used to detect a probable prediction error and bypass the subranging operation. The second uses the subranging output to detect a prediction error. In both cases, a standard SAR operation is performed and thus an error in the prediction does not cause any loss in signal information. When the prediction filter outputs a value that exceeds the N bit range, this is a likely indicator that the prediction is not accurate and thus the subranging operation can be skipped entirely. Fundamentally, this is because the out-of-band gain for prediction filters is larger than one, and grows larger as the filter order grows. This out-of-band gain will inevitably lead to over-ranging and therefore using the over-range indicator can help to save

conversion cycles when the input is changing too quickly. While the over-range indicator can help to skip unnecessary prediction cycles, it is not guaranteed to catch all cases where the prediction error is too large for the subrange. A simple method to detect prediction errors is to check if the subrange output code is at its maximum or minimum. The subrange DAC will always converge to one end of its range when the prediction error exceeds the maximum DAC range, so slightly reducing the usable subrange codes allows for simple error detection. For the case of a 5-bit subranging DAC removing the top and bottom values from the subrange reduces the allowable error by only 6%.

4.4 Implementation and Simulation Results

4.4.1 Prediction filter implementation

As mentioned in Sec. 4.2, the optimized third-order filter can reduce the required sampling rate by 50% compared to the optimized second-order filter. Filter orders higher than third-order start to have diminishing returns, so the optimized third-order filter is chosen for full implementation in order to limit the complexity and filter power. The filter response is designed for an optimum OSR of seven, which allows for large power savings across a wide OSR range, without requiring the modifications to the filter coefficients that the optimized third-order filter relies on. In order to compare the performance of a third-order filter with fixed coefficients to a third-order filter that is optimized across OSR, a full ADC model is built that accounts for the total reference energy and total number of comparisons per cycle. Fig. 4.10 compares the

reference energy savings and number of comparisons per cycle for the fixed and optimized coefficient cases. The optimized coefficients provide only a 12%

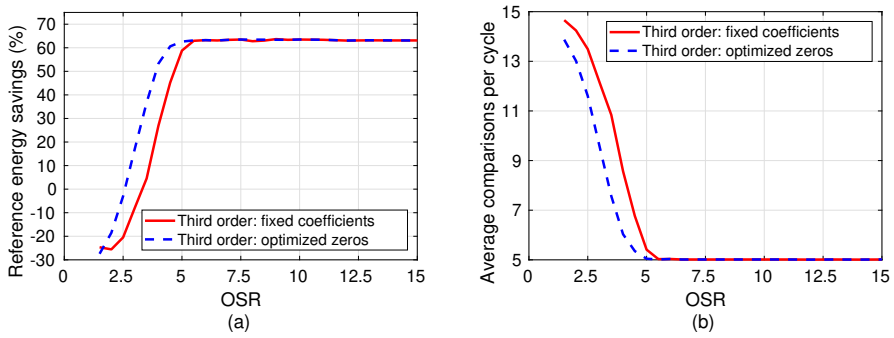

Figure 4.10: Comparison between dynamic and static filter bandwidth vs OSR

reduction in required sampling bandwidth compared to the fixed coefficients optimized for an OSR of 7. This means that a single high-quality prediction filter design can be reused across a wide range of input signal characteristics, reducing required design time. The OSR of 7 was chosen because its coefficients can be closely approximated with fractional values that require only bit shifts for multiplication, removing the need for any digital multiplier in the filter implementation. The designed estimator is

$$\hat{X} = 2.875X[n-1] - 2.875X[n-2] + X[n-3] \tag{4.13}$$

If X_{int} is defined as

$$X_{int} = X[n-1] - X[n-2] \tag{4.14}$$

then $\hat{X}$ can be expressed as a function of additions and bit shifts as

$$\hat{X} = (X_{int} << 1) + (X_{int} >> 1) + (X_{int} >> 2) + (X_{int} >> 3) + X[n-1] \tag{4.15}$$

Using these coefficients, only 4 bit shifts and 5 addition operations are required. The digital filter was designed using Verilog and synthesis tools were used to implement the physical design. Simulation results show that the implemented prediction filter consumes 35 nW from a 0.6 V supply running at 100 kS/s.

4.4.2 ADC implementation and simulation results

In order to further prove the effectiveness of the proposed prediction technique, a 0.6 V, 100 kS/s, 10-bit ADC with 5 prediction bits is designed in 65 nm that utilizes the prediction filter from Sec. 4.4.1. Only simulation results are provided for the implemented predicting ADC. The ADC uses bottom-plate sampling and the clock booster from [4] to ensure sufficient sampling linearity. One redundant conversion is added in the main DAC to compensate for any dynamic errors in the CDAC when the prediction fails. The prediction logic can be bypassed and the ADC can operate in standard 10-bit successive approximation mode for comparison purposes. Fig. 4.11 shows the simulated ADC output spectra with an input of 10 kHz, which corresponds to an OSR of 5. At this OSR, the prediction success rate is only approximately 10%, showing that the ADC can work at full performance even when the prediction accuracy is low and many prediction errors are detected. Fig. 4.12 compares the simulated reference energy savings and average number of comparisons per cycle across OSR for the simulated and modeled ADC. The simulation and model results match almost exactly, showing that a real implementation of the prediction ADC can achieve the modeled performance from Sec. 4.2.

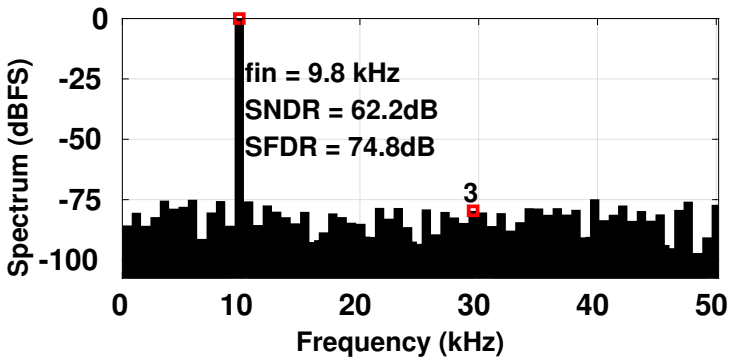

Figure 4.11: Simulated ADC output spectra with 256 points

Table 4.2 compares the power consumption when prediction is enabled and

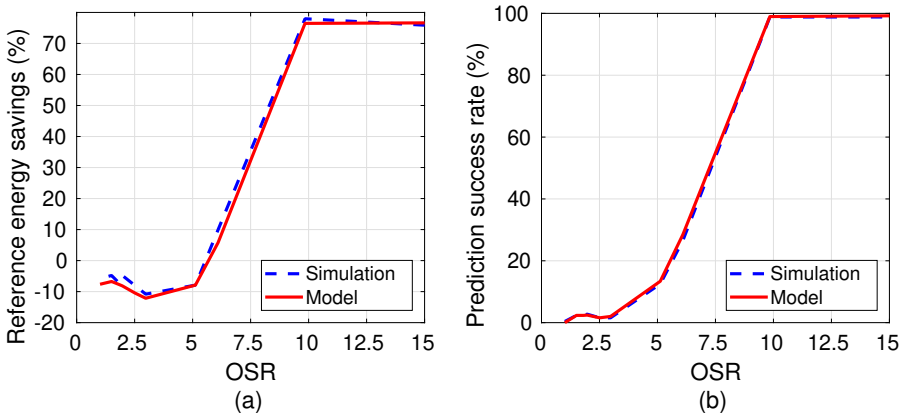

Figure 4.12: Simulated and modeled (a) success rate and (b) reference energy savings vs OSR

when it is disabled. The input frequency is sufficiently low that the success rate of the prediction is greater than 95%. The comparator power reduction is 55% and the reference savings is 73%. An additional 20% is saved in the digital control logic, since fewer decisions need to be latched and less clocking power is consumed when predictions are successful. After accounting for the

prediction filter power, the total power savings is still 36%. More advanced FinFET processes will see even larger benefits, since the digital power will reduce considerably.

Table 4.2: Power comparison for the proposed prediction ADC and a traditional ADC

Block	Prediction enabled power (nW)	Prediction disabled power (nW)	Power savings (%)
Prediction filter	34.8	0	0
Digital control	83.3	105.2	20.8
Reference	19	71.4	73.3
Comparator	48.4	114.9	57.9
Total	185.4	291.4	36.4

Chapter 5

Improving Design Efficiency Through the Use of Automated Circuit Sizing Tools

The explosion in compute power in recent years has increased interest in exploiting advanced algorithms to automate the sizing of analog circuits [12, 7]. Machine-learning techniques are also being applied to improve optimization efficiency [14, 13, 1]. Automated sizing is attractive to designers, as the manual optimization process can be tedious and time consuming. By allowing the automated tool to handle the low-level sizing optimizations, designers can focus on the more interesting work of defining circuit architectures in order to meet system performance specifications. In order for circuit designers to adopt an automated sizing tool, the tool must meet some minimum specifications. First, the sizing optimization must be performed using simulation results using real SPICE models. Especially for the most advanced processes, equation-based approaches are not sufficiently accurate to generate robust circuit sizes for any practical circuit. Second, the optimization algorithm must be able to handle a large set of specifications. Beyond standard design metrics such as gain, settling time, and bandwidth, analog circuit designers also must satisfy a large number of operating point conditions. These specifications include device saturation margins, overdrive voltages, and area

constraints. An optimization algorithm that can efficiently handle the entire set of design specifications is crucial before widespread adoption will occur. Third, the tool must be able to handle functional failures caused by poor sizing in the early stages of optimization. Almost all analog circuits require some time-domain simulation to calculate important design metrics such as noise, linearity, or settling time. These transient simulations will often fail to produce meaningful results during the early stages of optimization when the performance metrics are far away from their desired values. If the optimization tool cannot sufficiently handle these failure conditions, the designer either needs to reduce the design space to reduce the probability of failure, or the transient simulations need to be excessively long in order to ensure meaningful results even when the circuit performance is poor. Either case is not ideal from a design efficiency perspective. Fourth, the optimization tool must be sufficiently general to support any designer use case. In the ideal case, the designer can create their own testbench, defining all variables and performance metrics, and supply it to the tool for optimization. Tools that rely on fixed testbenches to test certain classes of device-under-test will not be general enough for most practical applications. Even for a common block such as an op-amp, the variation of important performance metrics, feedback loops to set operating conditions, and input/output loading conditions is too wide to make any generalized approach useful for most practical applications. Next, any tool must integrate into the current designer workflow as seamlessly as possible. Any tool which requires special flows or scripts to create test cases will

likely not be adopted by designers. Additionally, the optimization tool must provide interactive data about the progress of the optimization algorithm and the sizing results. Optimally, the designer should be able to easily import synthesized sizings directly into their simulation tool of choice for fast debugging and tweaking of circuit architectures. Finally, and probably most importantly, the optimization tool should provide an optimized solution within a reasonable time frame so that the designer is actually reducing time-to-market by utilizing this tool.

In this work, we propose a circuit sizing tool that directly integrates with widely used simulation tools, and is extendable to interface with any simulation engine. This tool also allows the designer to directly use their testbenches in the optimization engine, allowing for easy bring-up of new test cases. The tool does require some simple text files to be created to describe the design variables and constraints, but this functionality can easily be wrapped in a GUI in order to ease the designer's burden. The proposed tool is combined with a new optimization algorithm, Efficient Surrogate Model-assisted Sizing Method for High-performance Analog Building Blocks (ESSAB), and the results from three test cases are provided. This work is a collaboration with another PhD student, Ahmet Budak, that is an expert on optimization algorithms. This chapter will focus on the author's contribution to the work, including the proposed tool architecture and designer considerations around the choice of design variables and output specifications for the provided test

cases.[1]

5.1 Proposed analog IC sizing tool

Fig. 5.1 shows the high-level architecture of the proposed automated sizing tool. The optimization engine provides the bulk of the core functionality, and it is written in MATLAB. Inside the optimization engine, the optimizer collects all of the designer inputs, performs error checking, controls the simulation engine, reads the simulation results, and interfaces with the underlying optimization algorithm in order to create new candidate solutions and resimulate them. Each individual block is designed modularly, so that they can be interchanged for different requirements. The chosen simulation engine for this work is Cadence, since this is the industry standard analog circuit design product. The optimizer has a simulator abstraction layer that allows for new simulation engines to be easily connected to support different simulator use cases. A similar abstraction layer is used at the interface of the optimizer to the optimization algorithm, in this case ESSAB. Any optimization algorithm can be utilized, as long as the abstraction layer is implemented correctly in the algorithm layer.

The designer inputs are contained in three file types. The core designer

[1]This chapter is a partial reprint of the publication: Ahmet Budak, Miguel Gandara, Wei Shi, David Pan, Nan Sun, and Bo Liu, "An Efficient Analog Circuit Sizing Method Based on Machine Learning Assisted Global Optimization", submitted to *Transactions on Computer-Aided Design of Integrated Circuits and Systems* . I was responsible for the design and bring-up of the test cases, as well as the architecture for the optimization tool.

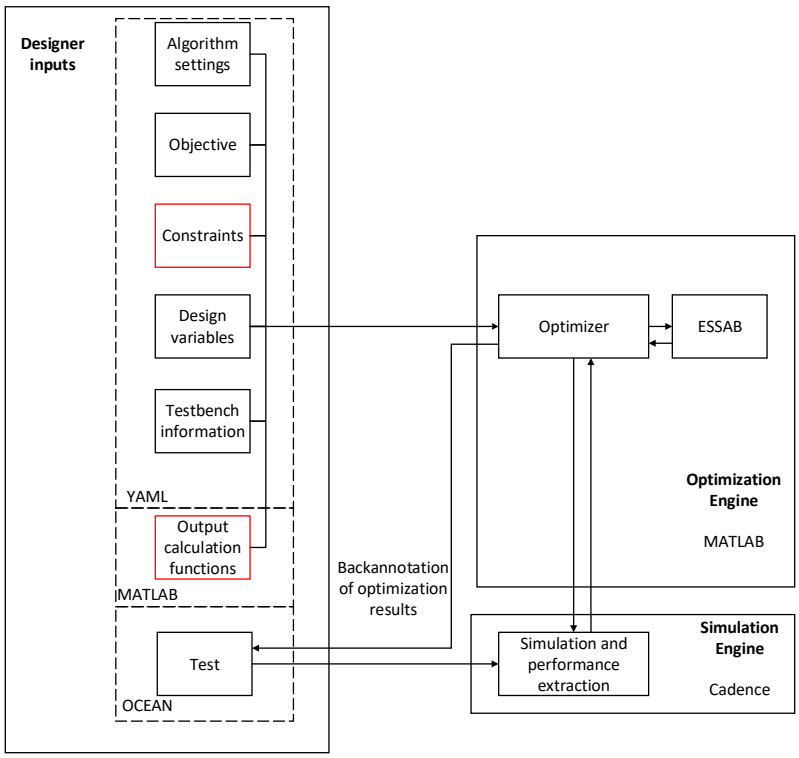

Figure 5.1: Architecture of the proposed automatic sizing tool [29]

input is the test, which is provided by the designer in OCEAN (Open Command Environment for Analysis) format. OCEAN is the standard scripting language used by Cadence to support text-based automation of simulations. Although OCEAN scripts are used to interface the optimizer to the simulator, no scripting knowledge is required of the user. Users can create their testbenches as usual using either Analog Design Environment (ADE) or ADE-XL with all required design variables and output parameters, and when they are done, they can export their setups to an OCEAN script through the Cadence GUI. The exported OCEAN script can be directly utilized by the optimizer.

The optimizer handles all required script modifications, including updating design variables with new candidate solutions and saving output parameters, removing the need for any specialized knowledge from the user. Second, all of the optimizer setup information is contained in a YAML file. The YAML file format is chosen because of its standard format and simple syntax. Most widely used languages feature support for reading and writing YAML files, simplifying automation of the setup file. Eventually, the main user interface will be a GUI which collects all of the user input and generates a YAML file to control the optimizer. The required designer inputs are in black boxes in Fig. 5.1, optional inputs are shown in red boxes. Algorithm settings are any variables to control the behavior of the optimization algorithm, these will be specific to the optimization algorithm. For ease of adoption, these variables should be minimized by the algorithm designer and a set of standard settings should be provided for the designer to use as a starting point. The objective is the performance metric that the user wants to optimize. Both minimization and maximization functions are supported. Constraints are optional parameters that will almost always be used for practical designs. Constraints are additional specifications that ensure the circuit under test performs as expected. Examples of constraints include phase margin, bandwidth, settling time, and noise. Design variables are the parameters that the optimization algorithm adjusts in order to meet the performance specifications. Testbench information is the set of OCEAN files that will be used for the current optimization. Most circuits require testing using multiple operating conditions,

so support for multiple OCEAN scripts in a single optimization operation is crucial for properly validating the design. The optimizer checks for consistency between the objectives, constraints, and design variables specified in the YAML file, and the actual output parameters and design variables in the supplied OCEAN scripts, and will throw an error in case of any inconsistencies.

A final important feature of the proposed tool is the support for backannotation of optimization results into the designer's ADE or ADE-XL views. The optimizer saves all results from the current simulation run, so at any time the designer can load a results file in MATLAB and run a command to automatically backannotate the sizing for any candidate to their ADE or ADE-XL view for further debugging. This is especially helpful during early bring-up of test cases, since the optimizer can sometimes produce unexpected results or highlight unknown weaknesses in the circuit design that require debugging and architectural optimization. This pushbutton functionality ensures the designer can quickly refine their test cases without having to utilize any specialized knowledge.

5.2 Automated sizing test cases

To prove the usefulness of the proposed tool and the effectiveness of the ESSAB optimization algorithm, three test cases are chosen. The first is an MDAC utilizing a folded-cascode OTA. The second is a state-of-the-art inverter stacking amplifier [21]. The third test case is a state-of-the-art distributed input voltage controlled oscillator (VCO) [16]. The last test case is

chosen as an example of a design that relies mostly on transient or periodic steady state (PSS) simulations for performance extraction. In general, transient simulations have a higher failure rate than DC or AC simulations, since the transient performance can be totally different than expectation in the early training phases. Using the VCO test case, the proposed ESSAB method can be tested with designs that have high failure rates in the early optimization phases.

5.2.1 MDAC utilizing a folded-cascode OTA

Fig. 5.2 shows the schematic for the folded-cascode OTA used as part of the MDAC for this design. The design variables and their search ranges are summarized in Table 5.1.

The sizing problem is defined as follows:

$$
\begin{aligned}
&\text{minimize } \mathit{Power} \\
&\text{s.t.} \quad \text{DC Gain} \geq 60 \ \text{dB} \\
&\qquad \text{CMRR} \geq 80 \ \text{dB} \\
&\qquad \text{PSRR} \geq 80 \ \text{dB} \\
&\qquad \text{Output Swing} \geq 2.4 \ \text{V} \\
&\qquad \text{Output Noise} \leq 3 \times 10^{-4} \ \text{V}_{\text{rms}} \\
&\qquad \text{Phase Margin} \geq 60 \ \text{deg} \\
&\qquad \text{Unity Gain Frequency} \geq 30 \ \text{MHz} \\
&\qquad \text{Settling Time} \leq 3 \times 10^{-8} \ \text{s} \\
&\qquad \text{Static Error} \leq 0.1\% \\
&\qquad \text{Saturation Margins} \geq 50 \ \text{mV}
\end{aligned}
\tag{5.1}
$$

In our experiment, the following transistors are required to operate in the saturation region: M1, M3, M4, M7, M9, M10, M12, M13, M15, M16, M17,

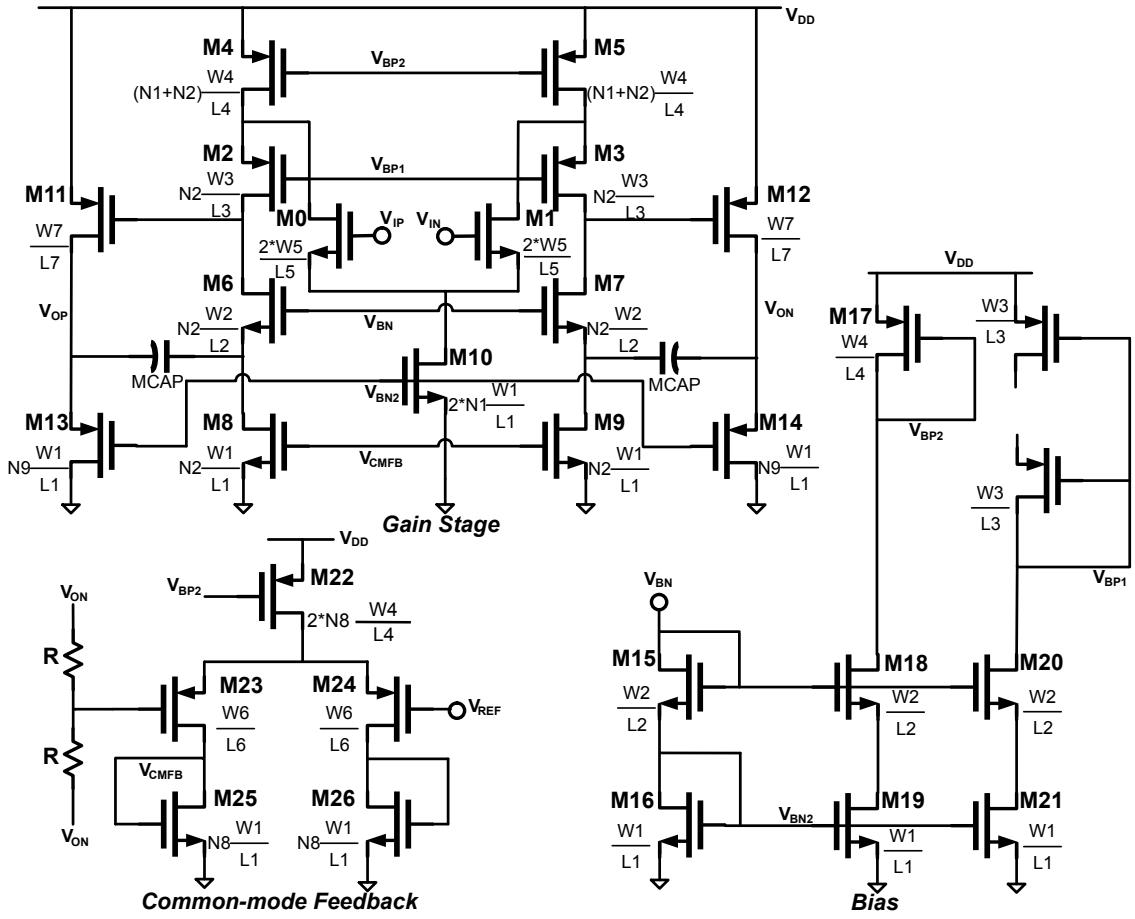

Figure 5.2: Schematic of the folded-cascode OTA

M18, M19, M20, M21, M22, M23, M24, M25 and M26. The total number of specifications becomes 29.

5.2.1.1 Designer considerations

The main consideration for optimizing any OTA that will be used in a feedback configuration is to ensure testbenches are provided that characterize

Table 5.1: Design parameters and their ranges for the folded-cascode OTA

Parameter	LB	UB	Parameter	LB	UB
L1(μm)	0.18	2	W4(μm)	0.24	150
L2(μm)	0.18	2	W5(μm)	0.24	150
L3(μm)	0.18	2	W6(μm)	0.24	150
L4(μm)	0.18	2	W7(μm)	0.24	150
L5(μm)	0.18	2	MCAP(fF)	100	2000
L6(μm)	0.18	2	Cf(fF)	100	10000
L7(μm)	0.18	2	N1 (integer)	1	20
W1(μm)	0.24	150	N2 (integer)	1	20
W2(μm)	0.24	150	N8 (integer)	1	20
W3(μm)	0.24	150	N9 (integer)	1	20

W: transistor width; L: transistor length; UB: upper bound; LB: lower bound

the closed-loop performance of the OTA in addition to the open-loop performance. When only open-loop performance is considered, the optimization tool will tend to oversize the input pair to maximize the gain and minimize input-referred noise. This is especially true for cascode amplifiers, since the input pair's parasitics generally contribute only to the non-dominant pole of the closed-loop amplifier, so the open-loop bandwidth can still meet design requirements with an oversized input pair. Once an amplifier with a large input pair is connected in capacitive feedback, as in the MDAC case, the loop gain will degrade significantly due to the reduction in feedback factor from the large gate parasitic of the input pair. For this reason, it's also generally a

good idea to place constraints on both the open-loop and closed-loop gains, to ensure the difference between the two cases isn't too large. A large difference between closed and open loop gains tends to imply some inefficiency in the sizing of devices that can be easily overcome with some small sizing tweaks. Although the transient settling time and static error define the true closed loop performance of the amplifier, adding constraints for unity-gain frequency and loop gain are helpful to guide the optimization algorithm towards the optimum solution. These extra constraints are especially helpful early in the optimization process, when the transient performance is so slow that invalid results are generated from the transient simulations.

5.2.1.2 Optimization results

A typical design obtained from the optimization algorithm is shown in Table 5.1. The corresponding performance metrics for this design are shown in Table 5.3.

The statistical results based on ten runs are shown in Table 5.4. The average simulation and modeling time is only 3 hours, which is a large speed-up compared to a manual design. The automated design using ESSAB also outperforms other optimization algorithms in terms of average, maximum, and minimum power consumption.

Table 5.2: A typical design obtained by ESSAB (folded-cascode)

Parameter	Value	Parameter	Value	Parameter	Value
L1(μm)	1.28	L2(μm)	0.36	L3(μm)	0.18
L4(μm)	1.9	L5(μm)	0.4	L6(μm)	1.7
L7(μm)	0.48	W1(μm)	6	W2(μm)	9.6
W3(μm)	6	W4(μm)	126	W5(μm)	142
W6(μm)	40.4	W7(μm)	132	MCAP(pF)	1.8
Cf(pF)	1.3	N1	4	N2	5
N8	1	N9	6	Id22 (nA)	240
Id10 (nA)	80	Id13/Id14 (nA)	200	Id3/Id4 (nA)	60

Table 5.3: Performance values of a typical design obtained by ESSAB (folded-cascode)

Power 0.63 mW	DC Gain 96.5 dB	CMRR 96.5 dB
PSRR 138.1 dB	Output Swing 2.69 V	Output Noise $2.72 \times 10^{-4} V_{rms}$
Phase Margin 77 deg	Unity Gain Freq. 34 MHz	Settling Time 2.5×10^{-8} s
Static Error 0.004%	Saturation Margins all satisfied	

5.2.2 Inverter stacking amplifier

Fig. 5.3 shows the schematic for the second test case, an inverter stacking amplifier. The design variables and their search ranges are summarized in Table 5.5.

The sizing problem is defined as follows, which has 21 specifications in

Table 5.4: Statistical results for different algorithms (folded-cascode)

Algorithm	DE	BO-wEI	ESSAB-GP	**ESSAB**
Success rate	10/10	2/10	10/10	**10/10**
N_{feasible}	3600	N.A.	252	**160**
Min. power (mW)	0.82	0.91	0.79	**0.53**
Max. power (mW)	1.55	1.62	1.12	**0.86**
Mean power (mW)	1.18	1.25	0.96	**0.68**
Std. power (mW)	0.33	0.5	0.12	0.09
Modeling time (h)	N.A.	29	6.5	0.4
Simulation time (h)	52	2.6	2.6	2.6

Table 5.5: Design parameters and their ranges for ISA

Parameter	LB	UB	Parameter	LB	UB
L1(μm)	0.3	10	W3(μm)	0.22	40
L2(μm)	0.3	10	W4(μm)	0.22	40
L3(μm)	0.3	10	W5(μm)	0.22	40
L4(μm)	0.3	10	W6(μm)	0.22	40
L5(μm)	0.3	10	W7(μm)	0.22	40
L6(μm)	0.3	10	W8(μm)	0.28	40
L7(μm)	0.3	10	WR(μm)	0.4	40
L8(μm)	0.3	20	C_CMFB(fF)	10	30000
LR(μm)	0.3	10	Cf(fF)	10	30000
W1(μm)	0.22	40	C_in(fF)	10	30000
W2(μm)	0.22	40	Nmain (integer)	1	100

W: transistor width; L: transistor length; UB: upper bound; LB: lower bound

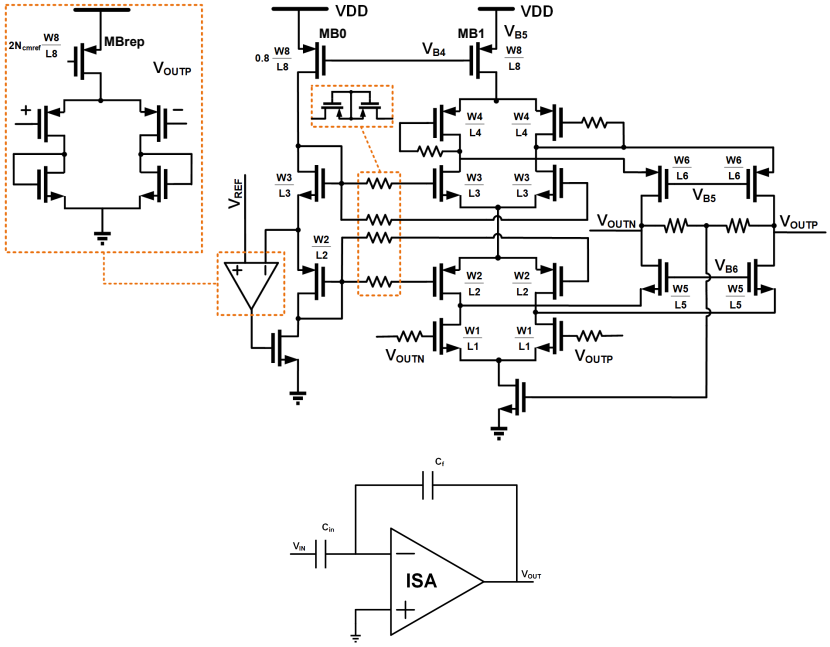

Figure 5.3: Schematic of the ISA

total.

minimize Noise-Power Product
s.t. Open-loop Gain ≥ 70 dB
DC-loop Gain ≥ 40 dB
Closed-loop BW ≥ 30 kHz
PMOS-input Degeneration Gain ≥ 30 dB
NMOS-input Degeneration Gain ≥ 30 dB
Output Offset 1-sigma $\leq 1 \times 10^{-3}$ V
Replica CMFB Loop Gain ≥ 13 dB
Main CMFB Loop Gain ≥ 35 dB (5.2)
Differential Loop Phase Margin ≥ 65 deg
Replica CMFB Loop Phase Margin ≥ 65 deg
Main CMFB Loop Phase Margin ≥ 65 deg
Closed-loop DC Gain ≥ 0 dB
Vds Mismatch main/rep c.s. ≤ 0.1
Output CM Voltage (max) ≤ 0.5 V
Output CM Voltage (min) ≥ 0.4 V
Saturation Margins ≥ 150 mV

5.2.2.1 Designer considerations

One major source of issues for this design was the mismatch between the main path and the replica path that sets the bias voltage for M3 and M2 in the ISA. If the replica current is too large, the M3 and M2 will starve M5 and M6 of current, drastically reducing the output bandwidth. One method to ensure decent matching between the main path and the replica path was to set a constraint on the V_{ds} mismatch of MB0 and MB1. As long as the V_{ds} is reasonably well-matched, the systematic current mismatch should not be large. Additionally, an extra conservative saturation margins of 150 mV was set so that the current sources are biased well into saturation to ensure maximum output impedance. In this case as well, the input devices tended to

be oversized in order to minimize the power-noise product as much as possible. Once the input pair is biased in the sub-threshold region, large increases in input size are necessary to achieve small increases in g_m. This design point is non-optimal from the perspective of the loading of the driving stage and the overall amplifier area. Although not used in the final optimization, the maximum area can be limited by placing a lower bound on the overdrive voltage of the input devices. This will ensure that the devices are not oversized to achieve small improvements in input-referred noise.

5.2.2.2 Optimization results

A typical design obtained from the optimization algorithm is shown in Table 5.6. The corresponding performance metrics for this design are shown in Table 5.7.

Table 5.6: A typical design obtained by ESSAB (ISA)

Parameter	Value	Parameter	Value	Parameter	Value
L1(μm)	1.7	W1(μm)	30.3	C_CMFB(fF)	160
L2(μm)	9.6	W2(μm)	0.8	Cf(fF)	860
L3(μm)	2.3	W3(μm)	0.9	C_in(fF)	13600
L4(μm)	8.2	W4(μm)	37.3	Nmain (integer)	18
L5(μm)	4.2	W5(μm)	4.2	Id_MB0 (nA)	288
L6(μm)	8.8	W6(μm)	2.4	Id_MB1 (nA)	360
L7(μm)	9.5	W7(μm)	13.2	Id_MBrep (nA)	20
L8(μm)	19	W8(μm)	1		
LR(μm)	6.1	WR(μm)	24.7		

Table 5.7: Performance values of a typical design obtained by ESSAB (ISA)

Noise-Power Product 1.81 $pWHz$	Open-loop Gain 70.0 dB	DC-loop Gain 46.5 dB
Closed-loop BW 33 kHz	P-input Deg. Gain 41.9 dB	N-input Deg. Gain 54.8 dB
Out. Offset 1-sigma 5.9×10^{-4} V	Rep. CMFB loop gain 14.1 dB	Main CMFB loop gain 60.0 dB
Diff. Loop PM 89 $deg.$	Rep. CMFB Loop PM 146 $deg.$	Main CMFB Loop PM 88 $deg.$
Closed-loop DC Gain 23.7 dB	Vds Mismatch main/rep 0.05	Output CM V. (max.) 0.41 V
Output CM V. (min.) 0.41 V	Saturation Margins all satisfied	

The statistical results based on ten runs are shown in Table 5.8. All ten runs outperform the simulation results of the design from [21], showing that the optimization algorithm can outperform a manual design from an expert.

5.2.3 Distributed input VCO

The final test case is a distributed input VCO. The schematic for the VCO is shown in Fig. 5.4. The design variables and their search ranges are summarized in Table 5.9

Table 5.8: Statistical results for different algorithms (ISA)

Algorithm	DE	BO-wEI	ESSAB-GP	ESSAB
Success rate	10/10	10/10	10/10	10/10
N_{feasible}	1300	100	73	**50**
Min. noise-power product ($pWHz$)	2.12	**1.68**	1.96	1.72
Max. noise-power product ($pWHz$)	2.55	2.6	2.48	**1.96**
Mean noise-power product ($pWHz$)	2.37	2.27	2.22	**1.81**
Std. noise-power product ($pWHz$)	0.17	0.25	0.22	0.13
Modeling time (h)	N.A.	28	6.5	0.5
Simulation time (h)	72	3.6	3.6	3.6

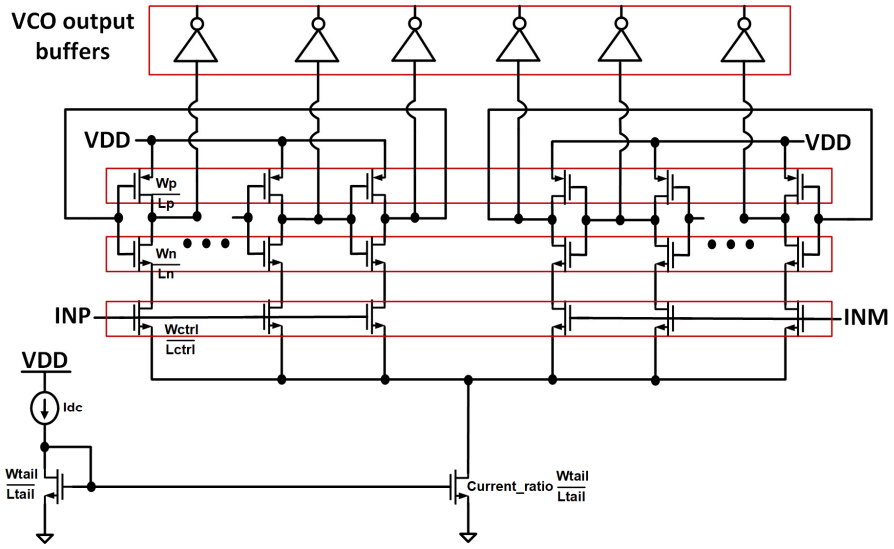

Figure 5.4: Schematic of VCO

The sizing problem is defined as follows, which has 5 specifications.

$$\begin{aligned} &\textbf{minimize} \text{ Noise-Power Product} \\ &\textbf{s.t.} \quad \text{Center Frequency} \geq 75 \text{ MHz} \\ &\qquad \text{KVCO min} \geq 1.28 \text{ GHz/V} \\ &\qquad \text{KVCO max} \leq 1.42 \text{ GHz/V} \\ &\qquad \text{Area} \leq 30097 \mu\text{m}^2 \\ &\qquad \text{Power} \leq 150 \times 10^{-6} \text{ W} \end{aligned} \tag{5.3}$$

Table 5.9: Design parameters and their ranges for VCO (VCO)

Parameters	LB	UB	Parameters	LB	UB
Idc(μA)	10	75	Ltail(μm)	0.04	20
Lctrl(μm)	0.04	1	Ln(μm)	0.04	0.4
Lp(μm)	0.04	0.4	Wtail(μm)	0.12	100
Wctrl(μm)	0.12	100	Wn(μm)	0.12	100
Wp(μm)	0.12	100	Current ratio (integer)	1	20

W: transistor width; L: transistor length; UB: upper bound; LB: lower bound

5.2.3.1 Designer considerations

The main difficulty of enabling a VCO inside the optimization algorithm is ensuring the convergence of the PSS simulation. In order for PSS to converge, an initial estimate of the oscillation frequency needs to be provided to the simulator. Since the oscillation frequency will vary significantly during the early optimization procedure, a transient analysis needs to be run for each candidate to obtain an estimate of the oscillation frequency and this value needs to be used as an input to the PSS simulation. Fortunately, Cadence has a function, $calcVal$, that allows an output from one test to be used as a design variable in another test. By utilizing the $calcVal$ functionality, the result from the transient simulation can be provided to the PSS simulation.

5.2.3.2 Optimization results

A typical design obtained from the optimization algorithm is shown in Table 5.10. The corresponding performance metrics for this design are shown

in Table 5.11.

Table 5.10: A typical design obtained by ESSAB (VCO)

Parameter	Value	Parameter	Value	Parameter	Value
Idc(μA)	23.7	Ltail(μm)	2.45	Lctrl(μm)	0.11
Ln(μm)	0.08	Lp(μm)	0.07	Wtail(μm)	0.64
Wctrl(μm)	6.60	Wn(μm)	0.42	Wp(μm)	1.82
Current ratio	1				

Table 5.11: Performance values of a typical design obtained by ESSAB (VCO)

Noise-Power Product	Center Frequency	Area
$0.75fWHz$	$90.9MHz$	$260\mu m^2$
Power	KVCO	
$65\mu W$	$1.32GHz/V$	

The statistical results for all the reference methods are shown in Table 5.12. Due to the multiple transient-based simulations, the simulation time is much longer than other cases. The proposed ESSAB technique outperforms other methods in terms of absolute noise-power product and variation of results. The standard deviation of the noise power product for the ten ESSAB runs is significantly better than other cases.

Table 5.12: Statistical results for different algorithms (VCO)

Algorithm	BO-wEI	ESSAB-GP	ESSAB
Success rate	3/10	10/10	**10/10**
N_{feasible}	N.A.	141	**54**
Min. noise-power product ($10^{-16} \times WHz$)	10.3	6.3	**5.5**
Max. noise-power product ($10^{-16} \times WHz$)	57.2	100	**10.6**
Mean. noise-power product ($10^{-16} \times WHz$)	33.2	28.8	**8.2**
Std. noise-power product ($10^{-16} \times WHz$)	23.4	35.4	1.9
Modeling time (h)	1.1	0.2	0.05
Simulation time (h)	25	25	25

5.3 Conclusion

This chapter proposed a new automated analog sizing tool that integrates well with current designer workflows. The automated sizing tool is combined with a new optimization algorithm to produce results that outperform other optimization algorithms. ESSAB outperforms other methods for a conventional MDAC design, as well as two additional state-of-the-art designs; an inverter stacking amplifier and a distributed-input VCO. By combining a straightforward user interface with a high performance optimization algorithm, the authors' hope to drive further adoption of automated analog sizing techniques to improve designer efficiency.

Chapter 6

Conclusion

This dissertation has discussed the usage of digital techniques and circuits to improve the power and design efficiency of data converters in advanced technologies. Technology scaling has greatly improved the power efficiency of digital circuits, however it has created a number of challenges in the design of high precision analog and mixed-signal circuits. Device intrinsic gains continue to decrease as process sizes shrink, creating difficulty in achieving the large gains required for traditional closed-loop amplifier implementations. Furthermore, reduced supply voltages limit the usage of cascode amplifiers to increase gain, resulting in extra gain stages in order to ensure high gain. These extra gain stages require extra power consumption and contribute extra noise and mismatch to the system. One data converter topology that has particularly suffered is pipeline ADCs. These ADCs can achieve 12-16 bit resolutions at high sampling speed, but they rely on accurate residue amplification between stages to ensure sufficient dynamic range for each pipeline stage. Our work seeks to address the scaling challenges of building high accuracy residue amplifiers by introducing a new amplifier topology that leverages positive feedback to achieve high gain. Utilizing this type of amplifier has its own downsides, and our work seeks to address these downsides to ensure operation as accurate

as that of a traditional closed-loop residue amplifier. The next part of our work seeks to reduce the power consumption of the least scaling-friendly blocks in SAR ADCs; the CDAC reference power and the comparator power. For ADCs of 10 bits and greater, the power consumption of the CDAC and comparator is generally limited by the noise requirements, therefore technology scaling will not directly allow for scaling of these blocks' power consumption. In the case of band-limited signals, digital filtering techniques can be utilized to reduce both the comparator and CDAC reference power. Our work extends previous work by supporting band-limited signals of any input type, whereas previous work only focused on low-activity signals.

The first section of this dissertation focused on improving the power efficiency of the pipeline ADC residue amplifier by reusing the sub-ADC comparator as a dynamic residue amplifier. Utilizing a dynamic amplifier removes all static power consumption from the amplifier, greatly improving its power efficiency. By using a SAR ADC as the sub-ADC, a large first-stage resolution can be used, allowing a small enough input swing to allow for linear operation of the proposed amplifier. The first prototype addressed the major limitations of previous dynamic amplifier-based works: the limited achievable gain of dynamic integrators and the offset mismatch betweeen comparator and amplifier. By cascading an integrator with a high-gain positive feedback stage, our proposed amplifier can achieve high gain while maintaining the noise efficiency of integrators. Our prototype was the first to achieve a gain of 32 using dynamic amplification. Additionally, since the amplifier hardware reuses the compara-

tor hardware, there is no offset mismatch between comparator and amplifier that requires either extra area to reduce offset, or extra circuitry to correct the offset. Both the SAR ADC and the proposed amplifier would benefit from technology scaling. The prototype ADC was fabricated in 130 nm CMOS and achieved an SNDR of 63.2 at a sampling rate of 10 MS/s while consuming 280 μW. The amplifier power was less than 20% of the total power, so technology scaling would definitely improve the achievable power efficiency.

The second section of this dissertation sought to address the main limitations of the first prototype. First, the timing control was power hungry, dominating the overall amplifier power consumption, and introduced a significant amount of noise to the amplifier, limiting the overall performance. Second, the first prototype had a major disadvantage compared to traditional closed-loop residue amplifier implementations: the gain varied significantly across PVT. To help address both challenges, a low-power single-gate gain control block was proposed. This gain control block provides PVT tracking for the integration time, which comprises 80% of the total amplification time. By tuning the threshold voltage of the gain control block, the amplification time can be tuned enough to cover the variation in the remaining 20% of the amplification time. This gain control block was combined with a low speed and low power mixed-signal calibration loop to adjust the amplifier gain across PVT variations. By shifting the gain control feedback from the analog domain to the mixed-signal domain, digital filters can be used to achieve large loop gains without the expense of achieving large loop gains in the analog domain.

Additionally, the digital filters are inherently scaling-friendly and simple to port to new processes, a big advantage over traditional analog feedback loops. A prototype ADC with the enhanced gain control block and mixed-signal calibration was fabricated in 130 nm CMOS and achieved an SNDR of 67.3 dB, a 4 dB improvement over the first prototype. The prototype also showed stable performance acrosss a temperature range of -20 to 80°C, which was only achievable due to the addition of the mixed-signal background calibration. Despite being fabricated in an older technology with large digital power, the low-frequency Schreier FoM was still 172 dB, showcasing the potential benefits of utilizing this architecture in more advanced processes.

The third section of this dissertation sought to address the main scaling bottlenecks of the SAR ADC: its large reference and comparator energy consumption for noise-limited designs. By leveraging knowledge about the signal characteristics, a starting prediction can be applied to limit the required range of the successive approximation. This technique helps to reduce both CDAC reference power, by switching only the LSBs of the CDAC, and the comparator power, by reducing the total number of comparisons required per cycle. Previous work has focused only on reducing reference power for low-activity signals. Our work expanded the application space of prediction-based SAR ADCs to include band-limited signals of any input characterisitc. We achieved this by viewing the prediction problem as a filtering problem, and applying well-known filtering techniques to minimize the total in-band error of the prediction. Finally, the proposed dual DAC approach reduces the average

switching energy by 30% over previous work that used only a single DAC for prediction and subranged successive approximation. This approach also has the advantage of a 50% reduction in the maximum speed penalty compared to LSB-first designs. The effectiveness of the proposed technique was verified through detailed ADC modelling, and further confirmed through the full design and simulation of an ADC leveraging the proposed prediction algorithms. Simulation results showed a reduction in comparator power of over 50% and a reduction in total reference power of 75%.

The final section of this dissertation sought to address the design efficiency limitations of circuit sizing. A new automated circuit sizing tool was proposed that requires minimal specialized designer knowledge, allowing for easy adoption. By leveraging the ESSAB optimization algorithm developed by Ahmet Budak, the proposed tool can generate circuits with performance on par with state-of-the-art manual designs done by experts. Three test cases were presented, an MDAC utilizing a folded-cascode OTA, a state-of-the-art inverter stacking ISA, and a state-of-the-art distribute-input VCO. In all three cases, the proposed circuit sizing tool is able to meet all constraints and generate a design with excellent performance.

Bibliography

[1] Surrogate assisted optimization for low-voltage low-power circuit design.

[2] L. Chen, A. Sanyal, J. Ma, and N. Sun. A 24-μW 11-bit 1-MS/s SAR ADC with a bidirectional single-side switching technique. In *2014 IEEE ESSCIRC*, pages 219–222, Sept 2014.

[3] L. Chen, A. Sanyal, J. Ma, X. Tang, and N. Sun. Comparator common-mode variation effects analysis and its application in sar adcs. In *2016 IEEE ISCAS*, pages 2014–2017, May 2016.

[4] L. Chen, X. Tang, A. Sanyal, Y. Yoon, J. Cong, and N. Sun. A 0.7-v 0.6-μW 100-ks/s low-power sar adc with statistical estimation-based noise reduction. *IEEE Journal of Solid-State Circuits*, 52(5):1388–1398, 2017.

[5] Shuo-Wei Mike Chen and R. W. Brodersen. A 6b 600ms/s 5.3mw asynchronous adc in 0.13/spl mu/m cmos. In *2006 ISSCC*, pages 2350–2359, Feb 2006.

[6] Lawrence C. Evans. *An Introduction to Stochastic Differential Equations*. American Math Society, 2013.

[7] Mourad Fakhfakh, Esteban Tlelo-Cuautle, and Maria Helena Fino. *Performance Optimization Techniques in Analog, Mixed-Signal, and Radio-Frequency Circuit Design*. IGI Global, 2014.

[8] H. Huang, S. Sarkar, B. Elies, and Y. Chiu. 28.4 a 12b 330ms/s pipelined-sar adc with pvt-stabilized dynamic amplifier achieving lt;1db sndr variation. In *2017 ISSCC*, pages 472–473, Feb 2017.

[9] Seokhyeon Jeong, Wanyeong Jung, Dongsuk Jeon, O. Berenfeld, H. Oral, G. Kruger, D. Blaauw, and D. Sylvester. A 120nw 8b sub-ranging sar adc with signal-dependent charge recycling for biomedical applications. In *VLSI Circuits (VLSI Circuits), 2015 Symposium on*, pages C60–C61, June 2015.

[10] J. Leung, A. Waters, and Un-Ku Moon. Selectable starting bit sar adc. In *Circuits and Systems (ISCAS), 2015 IEEE International Symposium on*, pages 1654–1657, May 2015.

[11] J. Lin, D. Paik, S. Lee, M. Miyahara, and A. Matsuzawa. A 0.55 V 7-bit 160 MS/s interpolated pipeline ADC using dynamic amplifiers. In *2013 CICC*, pages 1–4, Sept 2013.

[12] Bo Liu, Georges Gielen, and Francisco V Fernández. Automated design of analog and high-frequency circuits. *A computational intelligence approach, Springer, Berlin, Heidelberg*, pages 978–3, 2014.

[13] Bo Liu, Qingfu Zhang, and Georges GE Gielen. A gaussian process surrogate model assisted evolutionary algorithm for medium scale expensive optimization problems. *IEEE Transactions on Evolutionary Computation*, 18(2):180–192, 2013.

[14] Wenlong Lyu, Pan Xue, Fan Yang, Changhao Yan, Zhiliang Hong, Xuan Zeng, and Dian Zhou. An efficient bayesian optimization approach for automated optimization of analog circuits. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 65(6):1954–1967, 2017.

[15] B. Malki, B. Verbruggen, P. Wambacq, K. Deguchi, M. Iriguchi, and J. Craninckx. A complementary dynamic residue amplifier for a 67 dB SNDR 1.36 mW 170 MS/s pipelined SAR ADC. In *2014 ESSCIRC*, pages 215–218, Sept 2014.

[16] Abhishek Mukherjee, Miguel Gandara, Xiangxing Yang, Linxiao Shen, Xiyuan Tang, Chen-Kai Hsu, and Nan Sun. A 74.5-db dynamic range 10-mhz bw ct-$\delta\sigma$ adc with distributed-input vco and embedded capacitive-π network in 40-nm cmos. *IEEE Journal of Solid-State Circuits*, 2020.

[17] B. Murmann and B. E. Boser. A 12-bit 75-MS/s pipelined ADC using open-loop residue amplification. *JSSC*, 38(12):2040–2050, Dec 2003.

[18] Shanti Pavan, Richard Schreier, and Gabor C Temes. *Understanding delta-sigma data converters; 2nd ed.* Wiley-IEEE Press, Hoboken, NJ, 2017.

[19] A. Sanyal and N. Sun. A 18.5-fJ/step VCO-based 0-1 MASH $\delta\sigma$ ADC with digital background calibration. In *2016 VLSI*, pages 1–2, June 2016.

[20] A. Sanyal and Nan Sun. An energy-efficient low frequency-dependence switching technique for sar adcs. *Circuits and Systems II: Express Briefs,*

IEEE Transactions on, 61(5):294–298, May 2014.

[21] Linxiao Shen, Nanshu Lu, and Nan Sun. A 1v 0.25 uw inverter-stacking amplifier with 1.07 noise efficiency factor. In *2017 Symposium on VLSI Circuits*, pages C140–C141. IEEE, 2017.

[22] E. Siragusa and I. Galton. A digitally enhanced 1.8-v 15-bit 40-MSample/s CMOS pipelined ADC. *JSSC*, pages 2126–2138, Dec 2004.

[23] V. Tripathi and B. Murmann. A 160 ms/s, 11.1 mw, single-channel pipelined sar adc with 68.3 db sndr. In *Proceedings of the IEEE 2014 CICC*, pages 1–4, Sept 2014.

[24] F. van der Goes, C. Ward, S. Astgimath, H. Yan, J. Riley, J. Mulder, S. Wang, and K. Bult. 11.4 a 1.5mW 68dB SNDR 80MS/s 2 × interleaved SAR-assisted pipelined ADC in 28nm CMOS. In *2014 ISSCC*, pages 200–201, Feb 2014.

[25] J. Van Rethy, M. De Smedt, M. Verhelst, and G. Gielen. Predictive sensing in analog-to-digital converters for biomedical applications. In *Signals, Circuits and Systems (ISSCS), 2013 International Symposium on*, pages 1–4, July 2013.

[26] H. Venkatram, T. Oh, K. Sobue, K. Hamashita, and U. K. Moon. A 48 fJ/CS, 74 dB SNDR, 87 dB SFDR, 85 dB THD, 30 MS/s pipelined ADC using hybrid dynamic amplifier. In *2014 VLSI*, pages 1–2, June 2014.

[27] B. Verbruggen, M. Iriguchi, and J. Craninckx. A 1.7mW 11b 250MS/s 2x interleaved fully dynamic pipelined SAR ADC in 40nm digital CMOS. In *2012 ISSCC*, pages 466–468, Feb 2012.

[28] Yun-Ti Wang and B. Razavi. An 8-bit 150-MHz CMOS A/D converter. *JSSC*, 35(3):308–317, March 2000.

[29] Yunyi Wang. A simulation-based analog ic synthesis tool using sbde optimization algorithm. Master's thesis, University of Texas-Austin, 2018.

[30] N. Wood and Nan Sun. Predicting adc: A new approach for low power adc design. In *Circuits and Systems Conference (DCAS), 2014 IEEE Dallas*, pages 1–4, Oct 2014.

[31] F.M. Yaul and A.P. Chandrakasan. A 10 bit sar adc with data-dependent energy reduction using lsb-first successive approximation. *Solid-State Circuits, IEEE Journal of*, 49(12):2825–2834, Dec 2014.

[32] L. Yu, M. Miyahara, and A. Matsuzawa. A 9-bit 1.8-GS/s pipelined ADC using linearized open-loop amplifiers. In *2015 IEEE A-SSCC*, pages 1–4, Nov 2015.