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Strain Engineered Si-Ge Nanowire Heterostructures and Josephson Junction Field-Effect Transistors for Logic Device Applications

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by

Feng Wen

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Dedication

To my parents and wife for their love and support.

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Abstract

Strain Engineered Si-Ge Nanowire Heterostructures and Josephson Junction Field-Effect Transistors for Logic Device Applications

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There has been relentless effort on the physical scaling of silicon (Si) metal-oxide-semiconductor field-effect transistors (MOSFETs) in pursuit of higher computing power in the past decades. Silicon and germanium (Ge) based nanowires are compatible with the standard Si process and promising for the ultimately scaled devices, by allowing the gate-all-around geometry and integration of strain engineering through radial heterostructures to address device-scaling limitations. In the first part of the thesis, advances in probing the strain of radial nanowire heterostructures and carrier mobility enhancement through strain engineering are presented. We present a sequence of structural characterization techniques for Ge-Si_xGe_{1-x} and Si-Si_xGe_{1-x} core-shell nanowires that extends to all types of Si-Ge radial nanowire heterostructures examined in the thesis. We combine planar and cross-sectional transmission electron microscopy to identify the crystal structure, orientation and morphology of the nanowire heterostructures. We then apply continuum elasticity model to calculate the strain distribution, which coupled with the lattice dynamic theory yields the Ge-Ge or Si-Si Raman modes under strain, showing good agreement with the experimental values acquired via Raman spectroscopy. We also study the electrical properties of Si_xGe_{1-x}-Si core-shell nanowires by fabricating and characterizing *n*-type MOSFETs,

and show that the tensile strain in the Si shell leads to a 40% electron mobility enhancement compared to bare Si nanowire MOSFETs. Additionally, we demonstrate both *n*-type and *p*-type MOSFETs using Si_xGe_{1-x}-Ge-Si core-double-shell nanowires as channel, designed so that holes populate the Ge shell and electrons populate the Si shell, with mobility enhancement of both carriers thanks to the compressive and tensile strain in the respective region. We also extract the valence band offset from the decoupled hole transport in the two shells at low temperature, overcoming the issue that most techniques available to probe the band structure in planar heterostructures are not promptly applicable.

Reducing the operation temperature provides an additional path for system optimization in addition to the shrinking of device geometry. In the second part of the thesis, we explore a Boolean logic device suitable for cryogenic computing. We execute a combined effort of modeling and experimental characterization to examine the feasibility of Josephson junction field-effect transistors (JJ-FETs) for logic device applications at low temperatures. JJ-FETs are similar to MOSFETs, with their source and drain electrodes being superconducting at the operation temperature. We develop a compact model for JJ-FETs operating in the short ballistic regime, and perform circuit level simulations to investigate the criteria of signal restoration and fan-out for JJ-FET logic gates. We also experimentally demonstrate the operation of JJ-FETs based on an InAs quantum well heterostructure platform. We perform self-consistent Poisson-Schrödinger simulations, finding different gate voltage regimes where carriers populate one or more subbands in different vertical positions of the heterostructure. Furthermore, we extend the short ballistic model to interpret the experimental data, and discuss the impact of a low oxide/channel interface quality on the implementation of practical JJ-FET logic devices.

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Chapter 1 : Introduction and Motivation

1.1 CMOS scaling

Complementary metal-oxide-semiconductor (CMOS) has been emerging in the past five decades as the predominant technology for logic device applications in the microelectronics industry. It is a type of metal-oxide-semiconductor field-effect transistor (MOSFET) fabrication process consisting of a complementary pair of *p*-type and *n*-type MOSFETs for logic operations. The concept of CMOS scaling has been applied relentlessly over many generations of the technology nodes to reduce the transistor dimensions. Consequently, consistent improvements in the transistor packing density, circuit operating speed and power dissipation have been realized. Meanwhile, the cost per function has been reduced. One of Intel's co-founders, Gordon Moore, predicted that the packing density of transistors in integrated circuits would double roughly every two years, corresponding to a scaling factor for the gate length of ~0.7×. Figure 1.1 shows the trend of this exponentially increasing transistor packing density over time, following the so-called Moore's law [1].

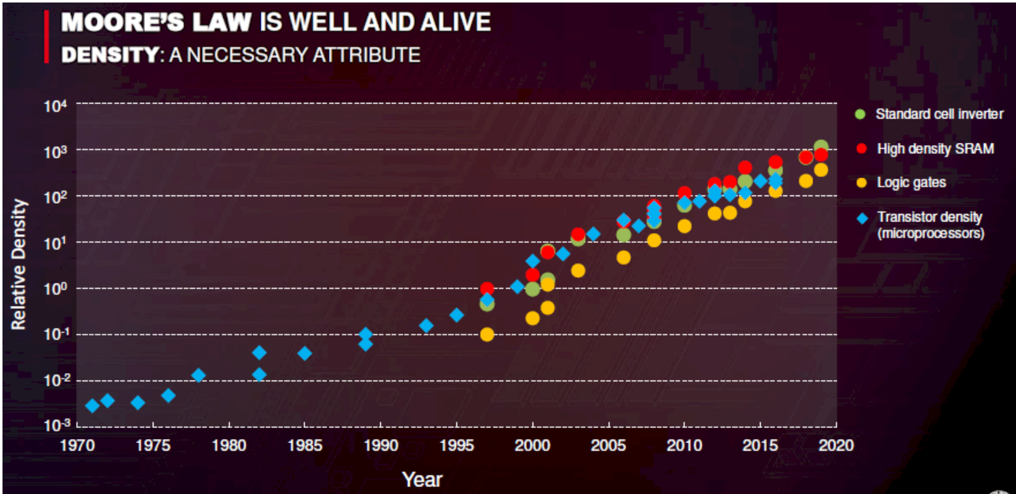

Figure 1.1: Historical data of the CMOS scaling trend from TSMC. (Figure adapted from Ref. [1])

To discuss the innovations in nanoscale CMOS and the potential beyond-CMOS devices, we first briefly describe the traditional MOSFET model and introduce the scaling rules. The exponential growth of the transistor packing density and thus the computation power in the past five decades as shown in Fig. 1.1 have largely been driven by the simple and steady reduction in MOSFET dimensions. This scaling is illustrated in Figure 1.2, where the original device is scaled by a factor of $\alpha < 1$ to a scaled device [2]. The gate length L_G, oxide thickness t_{ox}, gate and wire width, and the supply voltage (V_{DD}) are shrunk to α of their original values, while the doping concentration increases by a factor of $1/\alpha$. The technological scaling rules follow a simple electrostatic consideration, where the dimensions, doping and V_{DD} are scaled simultaneously so that the electric field remains constant in the device. This approach is known as the constant electric field scaling. However, in reality V_{DD} has not been scaled as fast as the device dimension due to the unscaled subthreshold slope (SS), which remains ~60 mV/dec at room temperature and can only be reduced by operating devices at a lower temperature due to its nature of thermionic emission. SS scales linearly with temperature T as $SS = 2.3(k_B T/e)/$ decade; k_B is the Boltzmann constant and e is the electron charge. Hence, for enhancement-mode MOSFETs, the *n*-type (*p*-type) device's threshold voltage V_T cannot be scaled below (above) the minimum (maximum) value required by the on/off ratio or the maximum leakage current at the drain voltage $V_D = V_{DD}$ and gate voltage $V_G = 0$ V. Additionally, several other physical parameters such as the work function and junction built-in voltage are material-related properties and cannot be not scaled easily. Consequently, V_{DD} cannot be well below 1 V. This is accommodated by introducing an additional scaling factor ε for the electric field, known as the generalized scaling. An increased electric field requires a higher doping and leads to a higher power consumption and potential reliability issues. Furthermore, in the recent two to three decades, the wiring is not scaled to the

same extent as the gate dimension to reduce the wiring resistance and therefore the gate delay. Hence, we have two spatial scaling parameters α_d to scale L_G and the vertical dimension, and α_w to scale the gate width and wirings. This approach is known as the generalized selective scaling. Table 1.1 summarizes the scaling factors of the three scaling approaches mentioned above [2].

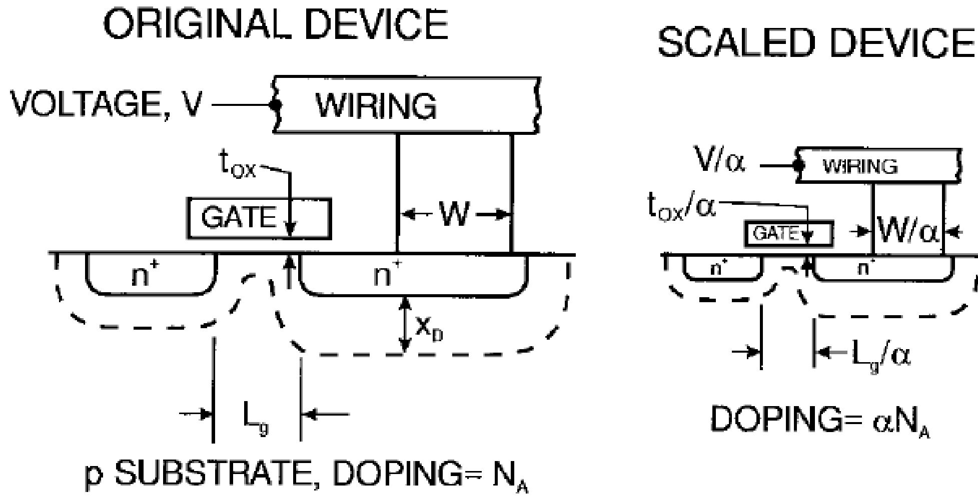

Figure 1.2: Schematic illustration of the CMOS scaling by a factor of α. (Figure adapted from Ref. [2])

Table 1.1: Scaling rules for three approaches (Table adapted from Ref. [2])

Physical parameter	Constant electric field scaling factor	Generalized scaling factor	Generalized selective scaling factor
Channel length, oxide thickness	$1/\alpha$	$1/\alpha$	$1/\alpha_d$
Wiring and channel width	$1/\alpha$	$1/\alpha$	$1/\alpha_w$
Electric field in device	1	ε	ε
Supply voltage	$1/\alpha$	ε/α	ε/α_d
Doping concentration	α	$\varepsilon\alpha$	$\varepsilon\alpha_d$
Device Area	$1/\alpha^2$	$1/\alpha^2$	$1/\alpha_w\alpha_d$
Gate capacitance	$1/\alpha$	$1/\alpha$	$1/\alpha_w$
Gate delay	$1/\alpha$	$1/\alpha$	$1/\alpha_d$

Table 1.1: continued

Power dissipation	$1/\alpha^2$	ε^2/α^2	$\varepsilon^2/\alpha_w\alpha_d$
Power density	1	ε^2	$\varepsilon^2\alpha_w/\alpha_d$

1.2 Short channel effects

Ideally, in each CMOS technology node the scaled MOSFETs should maintain the long channel behavior of its earlier generations. This simple scaling had held true since the Moore's law was proposed in 1965, until the physical dimensions of MOSFETs reached the deep sub-micron and then the nanoscale regime in the recent two decades. These short channel devices require the fundamental physical effects along with practical considerations addressed to operate properly. A MOSFET is considered short when L_G is comparable to the depletion width of the source or drain junction. Non-ideal device characteristics called the short channel effects then arise to make the scaling no longer trivial. The short channel effects are usually attributed to two physical phenomena, the first one is the limitation imposed on the carrier drift property through the channel, and the second one is the modification of V_T. In particular, we distinguish five different short channel effects: velocity saturation, hot carriers, impact ionization, drain induced barrier lowering and punch through, and surface scattering.

First, as indicated in Table 1.1, the magnitude of the electric field across the MOSFET's channel becomes larger in a newer technology node with the generalized (selective) scaling. At low field, the carrier drift velocity increases linearly with the field intensity. However, it tends to increase more slowly at a higher field and eventually saturates due to scattering. As a result, the device performance, e.g. transconductance in the saturation region degrades. The drain current I_D is then limited by velocity saturation instead of pinch-off, as usually described in the long channel

model. Second, after carriers gain sufficient energies from a high electric field, the so-called hot carriers can enter the gate oxide, where they can be trapped and degrade the device performance by increasing V_T and adversely affect the gate electrostatic control. Third, impact ionization is another undesirable effect occurring due to the high carrier velocity. The carriers with enough energy can impact on atoms in the channel and ionize them, followed by the generation of electron-hole pairs. This leads to appreciable substrate leakage current and even affects other MOSFETs on the same chip. Fourth, in the MOSFET channel, a potential barrier in the channel exists to block the carrier flow if V_G is not sufficient for channel inversion. This barrier height should only depend on V_G in well-tempered devices. However, in short channel MOSFETs it is also controlled by V_D. This phenomenon is known as drain induced barrier lowering (DIBL). The reduction of the barrier height due to the drain bias allows carrier flow across the channel even for a V_G below the threshold value. Punch through represents an extreme case where the gate loses control over the channel completely. It happens if the channel is shorter than the sum of the depletion region width of the source and drain to body junctions. Fifth, the carrier mobility is field-dependent in short channel devices. Moreover, since carriers are more strongly confined within the narrower inversion layer in the presence of a more intense electric field, the surface scattering due to the rough semiconductor/oxide interface reduces the carrier mobility.

1.3 CMOS innovations

Various technologies have been implemented to counter the short channel effects, including non-uniform doping such as retrograde doping or halo doping, metal gate and high-k dielectric, thin-body silicon-on-insulator technology, etc. The overall goal is to enhance the electrostatic coupling between the gate and the channel, hence steeper SS, smaller leakage current

and larger drive current can be realized. A range of innovations on the device geometry has also been devised. A double-gate MOSFET has a thin channel layer with two electrically connected gates on each side to modulate the channel. Short channel effects are therefore greatly suppressed because the two gates are more effective to terminate the drain field lines and prevent the source from feeling the drain potential. For even further enhancement of the gate electrostatic control, the industry has also proceeded to develop non-planar device geometries, including the tri-gate FinFET and the gate-all-around (GAA) nanowire or nanosheet MOSFET. Figure 1.3(a-d) illustrates the schematics of the planar MOSFET, FinFET, nanowire and nanosheet GAA MOSFET, respectively. Intel first introduced its 22 nm commercial FinFET devices known as Ivy Bridge in 2011, which allowed further physical scaling from the 32 nm planar devices without overwhelming short channel effects. Samsung, GlobalFoundries and TSMC also offered their own FinFET designs when launching the 14/16 nm technology node a few years later. The FinFET technology has been applied to the 14 nm, 10 nm and 7 nm nodes and still produces the state-of-the-art commercially available product as in 2020. In a FinFET, the gate electrode controls the channel fin from three sides to provide a much-improved SS, providing a larger effective channel width for a higher drive current, while the cost adder is only 2 - 3% compared to the planar counterpart [3]. A steeper SS reduces the leakage current and increases the on/off ratio, alternatively it can allow a lower V_T and thus V_{DD} for the same targeted leakage level or on/off ratio, favoring power and/or speed. One step further from the FinFET is the GAA MOSFET, featuring a channel completely encapsulated by the gate electrode and oxide to mitigate short channel effects even more effectively. There are two approaches to build the GAA geometry, namely nanowires [Fig. 1.3(c)] and nanosheets [Fig. 1.3(d)]. Nanowires are more difficult and expensive to fabricate but optimal for low power applications thanks to the best gate electrostatic

control, while nanosheets are believed to have better suitability for scaling. We will elaborate the nanowire synthesis process in the next section.

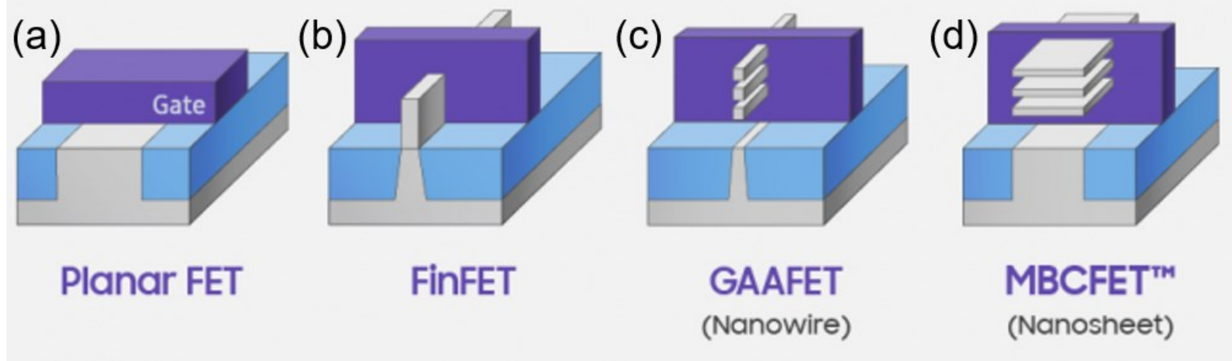

Figure 1.3: Evolution of the MOSFET geometry to enhance the gate electrostatic control. (a) Planar MOSFET. (b) Tri-gate FinFET. (c) GAA nanowire MOSFET. (d) GAA nanosheet MOSFET. (Figure adapted from Ref. [4])

1.4 Nanowire fabrication

Semiconductor nanowires are quasi-one-dimensional structures, where carriers are confined to a few tens of nanometers or less in the two dimensions perpendicular to the nanowire orientation. Their fabrication techniques are categorized into two paradigms, bottom-up and top-down. The bottom-up approach is defined as the nanowires assembled onto the substrate in an additive manner, while the top-down strategy requires removing materials from the substrate to define the nanowires. Figure 1.4(a) presents the schematics to illustrate the two techniques, vertical nanowires are assembled onto predefined templates for the bottom-up technique while horizontal nanowires are patterned into the substrate for the top-down technique. One advantage of the bottom-up nanowire growth over the top-down processing is that the former allows *in-situ* doping during the nanowire synthesis by incorporating dopant precursors. Hence, bottom-up grown nanowires do not require extra doping steps such as ion implantation and the subsequent activation

anneal. The number of masks and thermal budget can therefore be reduced. However, there is an outstanding issue associated with the assembly of these bottom-up grown semiconductor nanowires into the conventional CMOS design and fabrication. In a conventional CMOS process, an individual transistor has its channel coplanar to other devices and horizontal to the substrate. Furthermore, it requires precise control over positioning those devices in order to realize successful logic operation and maximize the packing density. Unfortunately, the available growth mechanisms of bottom-up grown semiconductor nanowires tend to lead to a poor control of the morphology, ordering, and placement required for CMOS manufacturing. Figure 1.4(b) presents the scanning electron microscopy (SEM) image of an entangled mesh of Ge nanowires synthesized using the supercritical fluid-solid-solid (SFLS) mechanism. On the other hand, the top-down process has a much superior compatibility with current CMOS technology since the nanowires are usually sculpted using lithography and etching, which are well-established in the CMOS process. Figure 1.4(c) shows the cross-sectional transmission electron microscopy (TEM) image at the channel position of vertically stacked GAA Si nanowire MOSFETs, whose conformal high-k dielectric and gate metal can be confirmed. Those horizontal GAA MOSFETs are a natural extension of the state-of-the-art non-planar devices without disruptive technology changes. Indeed, the fabrication process is adapted from the replacement metal gate process flow of FinFETs. However, significant fundamental insight can be gained from studying individual nanowire structures. Moreover, the bottom-up growth of nanowires allows academic research to be performed on the properties of those nanowires without an expensive and large-scale top-down process flow. In this thesis, we focus on discussing the properties of Si-Ge based nanowires prepared with the bottom-up growth.

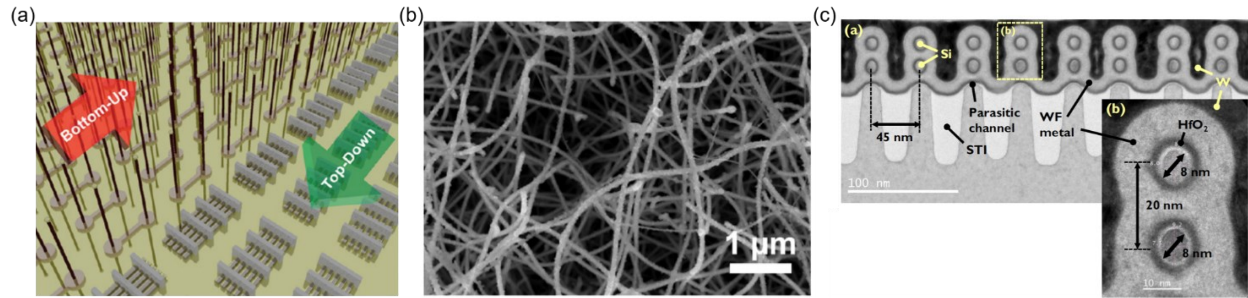

Figure 1.4: Nanowire fabrication techniques. (a) Schematics illustrating the bottom-up and top-down nanowire fabrication approaches. (b) SEM image of an entangled mesh of Ge nanowires grown by the SFLS method. (c) Cross-sectional TEM image of the channels of GAA nanowire MOSFETs. (Figure adapted from Refs. [5, 6])

1.5 Radial nanowire heterostructure

Nanowires synthesized through the bottom-up technique can readily create structures of non-uniform material compositions along the radial direction, namely radial nanowire heterostructures or core-(multi-)shell nanowires [7]. Figure 1.5(a-d) presents an example to synthesize core-shell nanowires using the vapor-liquid-solid (VLS) mechanism for the cores and chemical vapor deposition (CVD) method for the shells. Gold nanoparticles serve as the catalyst for the nucleation and one-dimensional growth of nanowire cores [panels (a-b)]. The shell growth initiates by changing the growth conditions, e.g. temperature, types of the gaseous precursors and their partial pressures [panel (c)]. The shell growth can be repeated to create core-multi-shell nanowires if desired [panel (d)]. Core-shell nanowires allow for enhanced carrier transport properties over bare nanowires if the materials are properly engineered in the two regions. An example is the Ge-Si core-shell nanowire, where the large valence band offset between Ge and Si leads to hole confinement in the Ge core, creating a spatial separation between the carriers and the trap states on the nanowire surface [8]. It is noteworthy that the thickness of the Si shell needs to

be optimized for the effectiveness of the barrier yet against the formation of dislocations. Consequently, a higher hole mobility can be realized in MOSFETs using the Ge-Si core-shell nanowire as channel, thanks to the suppressed scattering from the oxide/channel interface. Figure 1.6(a) shows the schematic of the cross-section of a Ge-Si core-shell nanowire, assuming a cylindrical morphology for both regions. Figure 1.6(b) presents the band structure of the Ge-Si core-shell nanowire. The strain due to lattice mismatch between the core and shell is assumed to be fully relaxed, the concept of strain will be discussed in detail in Section 2.5.1. Therefore, a large valence band offset of ~500 meV is expected at the heterostructure interface, which serves as the hole confinement potential for the quantum well [9]. Holes will then accumulate in the Ge core when the Fermi level E_F lies between the valence band edges of the two regions. Figure 1.6(c) shows the high-resolution planar view TEM image of a single crystalline Ge-Si core-shell nanowire, revealing an epitaxial Si shell on the Ge core. The boundary between the core and shell clearly exhibits itself by the color contrast due to the atomic weight difference between Ge and Si. Lu *et al.* [8] also fabricated MOSFETs using Ge-Si core-shell nanowires as channel and performed electrical transport measurement at room temperature to demonstrate the accumulation of one-dimensional hole gas in this heterostructure. Those MOSFETs have $L_G = 1$ μm and are capacitively coupled by back-gate electrodes through a 50 nm thick SiO_2 as the gate dielectric. Figure 1.6(d) presents the output characteristics data acquired from a Ge-Si core-shell nanowire MOSFET with a Ge core diameter of 15 nm. The device exhibits the behavior of a depletion mode p-type MOSFET, with a substantial conductivity at zero gate bias that decreases at more positive V_G [inset of Fig. 1.6(d)]. On the other hand, Figure 1.6(e) shows that bare Ge or Si nanowire MOSFETs operate in the enhancement mode and conduct no currents at zero gate bias. The distinct behavior between the bare nanowires and the core-shell nanowire heterostructures confirms the

accumulation of hole charge carriers.

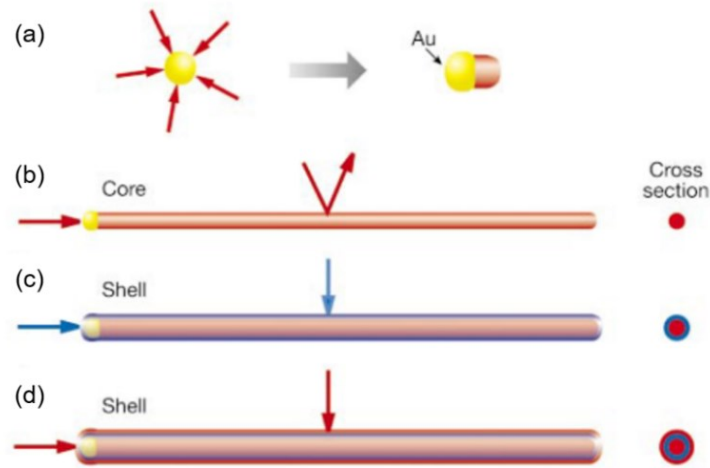

Figure 1.5: Synthesis of core-shell nanowires. (a) Au catalyst and catalyzed nucleation of nanowire cores. (b) One-dimensional nanowire core. (c) Precursor alteration and homogenous reactant decomposition on the nanowire surface lead to a thin, uniform shell. (d) Shell growths can be repeated multiple times by modulating precursors. (Figure adapted from Ref. [7])

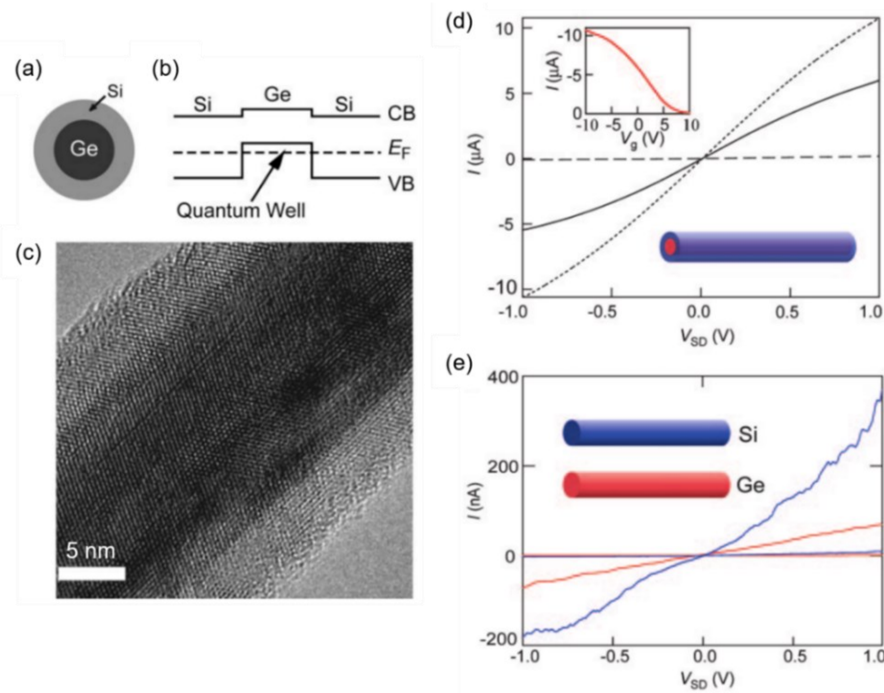

Figure 1.6: Structure and room temperature electrical transport property of Ge-Si core-shell nanowires. (a) Schematic of the Ge-Si core-shell nanowire cross-section. (b) Band diagram along the diameter, effectively

a Si/Ge/Si heterostructure. (c) High-resolution TEM image showing a contrast due to the different atomic mass between the Ge core and Si shell, whose diameter and thickness are 15 nm and 5 nm, respectively. (d) Output characteristics of a Ge-Si core-shell nanowire MOSFET, where different curves correspond to different V_G of 10 V (dashed line), 0 V (solid line) and -10 V (dotted line). The inset shows the associated transfer characteristics at $V_D =$ -1 V. (e) Output characteristics of bare Ge (red curves) and Si (blue curves) nanowire MOSFETs, at $V_G =$ 0 V and -10 V. (Figure adapted from Ref. [8]) Figure 1.6: continued.

To take advantage of radial nanowire heterostructures, it requires a careful control over the core growth, a fundamental understanding of the hetero-interface properties and an exquisite control of the epitaxial shell(s) growth. In the first part of the thesis, we discuss the growth and perform structural and electrical characterization of multiple types of Si-Ge based core-shell nanowire heterostructures, in an effort to explore potential candidates for the channel materials of GAA nanowire MOSFETs.

1.6 Cryogenic computing

1.6.1 Cryogenic CMOS

The previous sections have introduced the physical or dimensional scaling rules and design evolutions, emphasizing on the room temperature operation of MOSFET devices. In addition, the performance of CMOS or other types of semiconductor devices at cryogenic temperatures has been a subject of interest for a considerable amount of time that is almost as long as Moore's law [10]. Three motivations can be distinguished for the research efforts made in this area. First, material properties and device physics change substantially at low temperatures compared to their behavior at room temperature. It is important to understand the origins of those changes in order to design and improve the modern CMOS technology. Particularly, the temperature dependence of certain parameter gives insights on the physical mechanism related to the device reliability. Second, the performance of a semiconductor device improves when the operating temperature decreases. For

example, carrier mobility of a MOSFET increases thanks to a reduced phonon scattering. An appreciable power reduction can also be achieved, since V_{DD} can be lowered in proportional to the temperature without compromising the on/off ratio and leakage current. It is noteworthy in that V_{DD} scaling at room temperature is no longer feasible for modern nanoscale MOSFETs, as discussed in Section 1.1. In addition to pursuing an enhanced operation efficiency, cryogenic CMOS recently draws attention for its potential to be monolithically integrated as the classic electronic controller for scalable quantum processors [11, 12]. Finally, some semiconductor devices can only operate at low temperatures, such as superconducting electronic devices. An example is the Josephson-logic device, which will be discussed in detail in the next section.

The carrier mobility and concentration are among the physical parameters most affected by the temperature. The carrier concentration is determined by the Fermi-Dirac distribution, where the ratio of the potential over thermal voltage governs the occupation probability of states. In other words, this probability remains constant if the potential is scaled proportionally to the temperature. A temperature scaling factor can thus be introduced as $\theta^{-1} = T/300$ K, where T is the device operating temperature. Hence, V_{DD}, V_T and therefore the gate overdrive $V_G - V_T$ are scaled down by a factor of $\theta > 1$, so is the substrate doping level in order to maintain the depletion layer width. In addition, we have the mobility enhancement factor $\theta_\mu > 1$ by decreasing the temperature from 300 K to T. The temperature scaling of long-channel MOSFETs is then quite straightforward. Figure 1.7 shows the output characteristics of a p-type MOSFET operating at $T = 300$ and $T = 77$ K, with $L_G = 9$ μm. In this case, we have $\theta = 4$ and $\theta_\mu = 5$. At $T = 77$ K, $V_G - V_T$ and V_D are reduced by a factor of 4, I_D in the saturation region is then reduced by a factor of $\theta^2/\theta_\mu = 3$ as predicted by the long-channel model. Indeed, the shape of the scaled output characteristics at $T =$ 77 K matches that at $T = 300$ K.

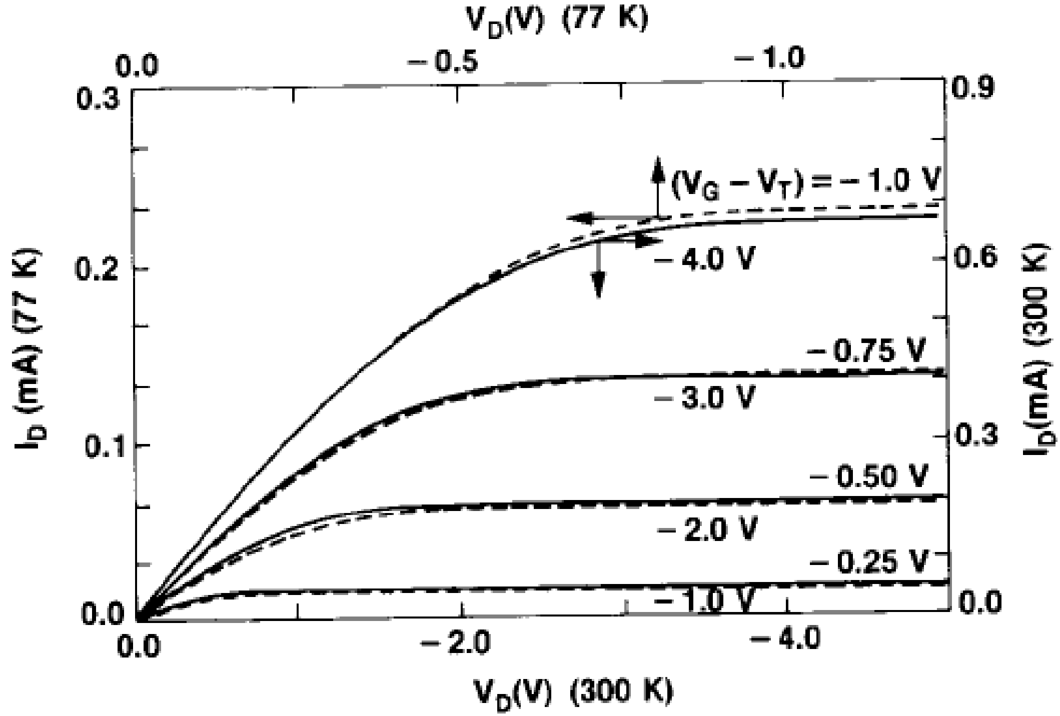

Figure 1.7: Output characteristics of a long-channel *p*-type MOSFET at $T = 300$ K and $T = 77$ K. (Figure adapted from Ref. [13])

However, the above temperature-scaling rule cannot be directly applied to nanoscale MOSFETs, whose I_D is determined by the saturation velocity instead of the low-field mobility. Therefore for a fixed $V_G - V_T$, the current gain of a nanoscale MOSFET at low temperatures is θ_v instead of θ_μ, which is the ratio of the carrier saturation velocity at a cryogenic T to that at $T =$ 300 K. Furthermore, the saturation current is now linearly proportional to $V_G - V_T$ in the velocity saturation regime. The magnitude of θ_v is usually much smaller than that of θ_μ, for example, the measured value of θ_v is 1.4 for electrons and holes if the temperature decreases to 77 K from 300 K [13]. Table 1.2 summarizes the temperature-scaling factors of some important physical quantities for MOSFETs operating in both the long channel and velocity saturation (short channel) regime.

Table 1.2: Temperature scaling factors for MOSFET operation (Table adapted from Ref. [14])

Physical parameter	Temperature scaling (short channel)	Temperature scaling (long channel)
Temperature	$1/\theta$	$1/\theta$
Device dimensions	1	1
Supply voltage	$1/\theta$	$1/\theta$
Channel doping	$1/\theta$	$1/\theta$
Electric field	$1/\theta$	$1/\theta$
Subthreshold slope	$1/\theta$	$1/\theta$
Gate capacitance	1	1
Saturated drain current	θ_v/θ	θ_μ/θ^2
Gate delay	$1/\theta_v$	θ/θ_μ
Power	$1/\theta^2$	$1/\theta^2$
Power delay product	$1/\theta_v\theta^2$	$1/\theta_\mu\theta$

In reality, the MOSFET will operate in an intermediate state of the two regimes. A short-channel device can eventually enter the long-channel regime, when V_{DD} is reduced below the value where the longitudinal electric field no longer exceeds the critical field for velocity saturation. Table 1.2 shows that the gate delay time in the velocity saturation regime is always reduced by a factor of θ_v. For Si, the saturation velocity of electrons at $T = 77$ K is about 40% higher than that at $T = 300$ K, while it increases further by only about 5% if the temperature is reduced to 4.2 K [15]. On the other hand, the gate delay time in the long-channel operation mode can increase if $\theta/\theta_\mu > 1$. Figure 1.8 presents the gate delays calculated based on the presented temperature-scaling rule for Si *n*-type MOSFETs with $L_G = 0.1$ and 1 μm. The calculation results are normalized to the gate delay associated with the MOSFET operation at $T = 300$ K with $V_{DD} = 5$

V. We notice that the gate delay and therefore the channel switching speed do not benefit too much from the low temperature operation.

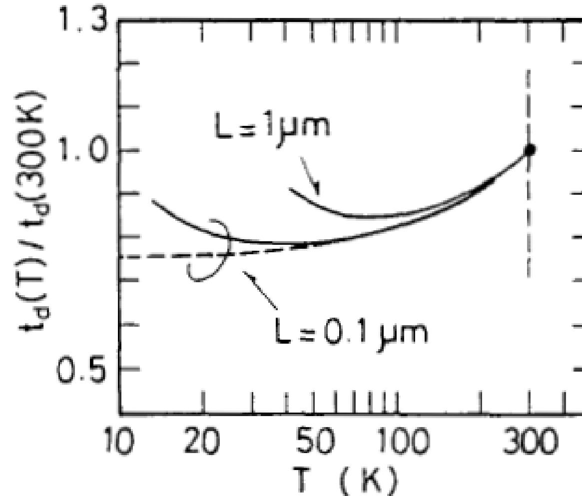

Figure 1.8: Temperature dependence of the gate delay time following the temperature-scaling rule summarized in Table 1.2. $V_{DD} = 5$ V at 300 K. The dashed line branching from the $L_G = 0.1$ μm device is calculated assuming an unscaled V_{DD} of 1 V at temperatures below 60 K. (Figure adapted from Ref. [14])

In short, we will get various advantages of operating Si CMOS systems at cryogenic temperatures thanks to the increased carrier mobility, reduced SS and leakage current, lower thermal noise and thus larger noise margin, increased interconnect conductivity, and improved device and circuit reliability including latch-up, electro-migration, etc. However, the gain in the switching speed is limited by the saturation velocity enhancement that does not exceed a factor of 2. Consequently, the benefit from CMOS cryogenic operation is limited and almost exclusively the power reduction in the worst-case scenario, which must justify the added complexity and cryogenic cooling cost. We will discuss the temperature scaling regarding the break-even cooling cost in detail in Section 5.3. In light of the above discussions, in this thesis we study an alternative type of semiconductor device based on the Josephson junction, which potentially provides more benefits for cryogenic computing than the standard CMOS.

1.6.2 Josephson junction logic devices

At low temperatures, superconductivity is one of the most spectacular material properties that emerges as a result of electrons forming Cooper pairs. Superconducting electronics can play a significant role in digital logic systems operating at low temperatures, since they are able to provide high speed, low power logic circuits and perfect interconnections. Among them, Josephson devices have great potentials for logic applications, and many innovative designs of Josephson-logic circuits have already been reported [16-18]. Josephson-logic devices can also operate at extremely small V_{DD} values in the mV range for ultra-low power consumption [19]. These devices are based on a fundamental unit known as the Josephson junction (JJ), a two-terminal quantum mechanical device consisting of two superconductor contacts separated by a weak link. The JJ allows dissipation-less current flow of the Cooper pair formed by two electrons (supercurrent) at low temperatures if the bias current is smaller than the critical current thanks to the proximity effect, and becomes resistive vice versa. The zero or finite voltage drop across the JJ can represent the binary logic value of '0' or '1'. The JJ is almost an ideal digital switch, exhibiting very abrupt transition between the superconducting and the normal/resistive state. It possesses an ultra-high switching speed, very low power dissipation, and the potential to couple with lossless superconducting transmission lines. The JJ also serves as the elementary block of a qubit [20, 21]. Hence, it is highly relevant to examine if JJs may be used for classic logic applications, which can potentially lead to performance and power consumption benefits over cryogenic CMOS, and simplify the integration of qubits with control circuitries in quantum systems.

A JJ can be used as a current-steering device in the simplest form for logic applications, if no isolation is required between the input and output. Figure 1.9(a-b) shows the schematic of such

a current-steering logic device, along with a timing diagram to indicate its switching delay. The JJ is biased into the superconducting state with a current $I_g < I_0$, where I_0 is the critical current of the JJ. In the later part of the thesis, we will use I_C instead of I_0 to denote the critical current. The JJ is also shunted with a load resistor R_L. Since the JJ is superconducting, there is no voltage drop across the JJ or R_L, the output is logic '0'. If additional source current I_s is injected to the JJ so that $I_g + I_s > I_C$, the JJ will switch to the normal state. The JJ and R_L in parallel form a resistive element and there is a finite voltage drop across them, the output is logic '1'.

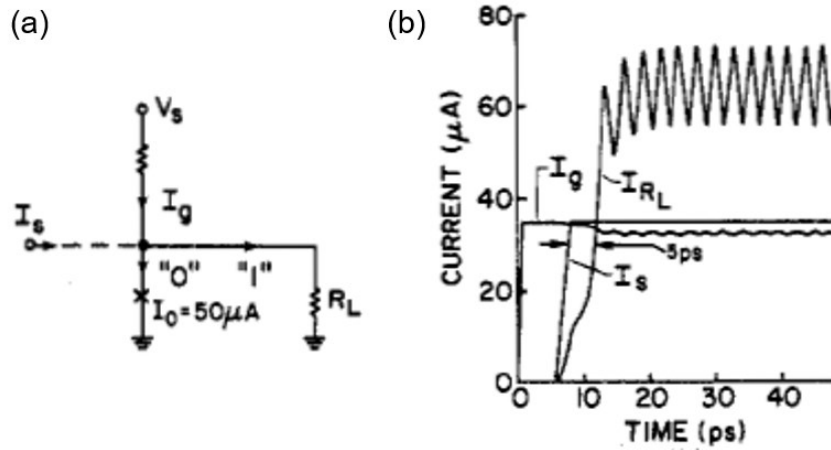

Figure 1.9: (a) Schematic of a JJ current-steering device. (b) Computer simulation indicating the switching delay using $I_g = I_s = 35$ μA, $I_0 = 50$ μA, $R_L = 12$ Ω, $V_s = 10$ mV. (Figure adapted from Ref. [19])

Unfortunately, this current-steering device is not practical for a logic gate as the isolation is neglected, and therefore the output signal propagates in the output as well as the input branch. Moreover, change of the load will alter the output voltage. To resolve these issues, JJ based logic devices with tunable I_C using magnetic coupling, or more complicated forms of current injection have been developed [22, 23]. Compared with those quasiparticle-injection devices, a gate-controlled superconducting transistor is excellent in terms of isolation between the input and output. The feasibility of logic devices based on the Josephson junction field-effect transistor (JJ-

FET), a three-terminal device with a gate-tunable I_C, was discussed decades ago. The JJ-FET design is similar to a MOSFET in the standard CMOS process, except that the source and drain are superconducting at cryogenic temperatures, and L_G is sufficiently short to allow coherent transport of Cooper pairs through the channel. A practical logic gate utilizing JJ-FETs has not been realized, although success on I_C control through field effect have been experimentally demonstrated on various material platforms including Si, Ge and III-V compounds [24-28]. Advances in nanoscale fabrication techniques and emerging channel materials such as nanowires, III-V quantum-wells and graphene, as well as the development of a transparent interface between the semiconductor and superconductor render the topic of JJ-FETs timely [29-32]. Figure 1.10(a) shows the output characteristics of a JJ-FET, demonstrating a gate tunable I_C. Figure 1.10(b) compares the voltage transfer curve of a JJ-FET inverter and a NMOS inverter, assuming $V_T = 0$ V; the schematic in the inset illustrates the actual circuit configuration. It is noteworthy that the JJ-FET can pull the output voltage V_{OUT} down to zero thanks to its superconductivity, while the NMOS can only discharge V_{OUT} to a finite value similar to a resistive voltage divider.

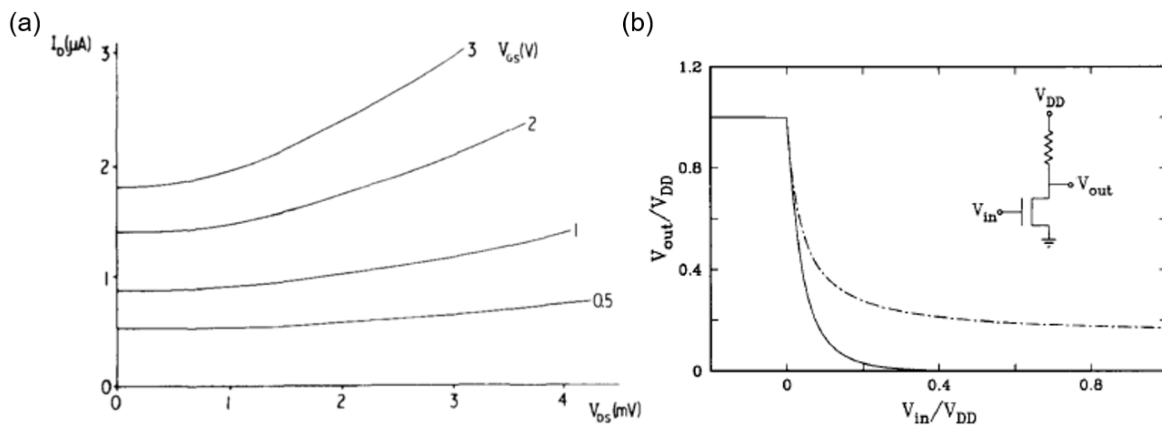

Figure 1.10: (a) Output characteristics of a JJ-FET. (b) Voltage transfer curves of a JJ-FET inverter (solid line) and a NMOS inverter (dash-dotted line). Inset is the device circuitry. (Figures adapted from Refs. [24, 26])

In the second part of the thesis, we perform a combined modelling and experimental effort aimed to benchmark the logic elements built with JJ-FETs through SPICE simulations, and explore practical implementation approaches using in-plane semiconductor junctions based on an InAs quantum well heterostructure.

1.7 Chapter summary and organization

In this introduction chapter, we first discuss the physical scaling to reduce the dimensions of MOSFETs, along with the concurrent short channel effects. Innovations of the device geometry have introduced non-planar structures such as FinFETs and GAA nanowire MOSFETs to improve the gate electrostatic control over the channel, allowing the industry to keep pursuing Moore's law. The semiconductor core-shell nanowire is one promising channel material, which allows simultaneous quantum confinement and mobility enhancement of carriers for improved transport properties. We also discuss the temperature scaling properties of MOSFETs. The small increase in saturation velocity limits the performance enhancement at cryogenic temperatures. We then discuss superconducting electronics, based on JJs in particular, as an alternative to CMOS for the logic device applications at low temperatures. In the first part of the thesis from Chapter 2 to 4, we will discuss the structural and electrical analysis of four different types of strained core-shell nanowires, namely Ge-Si_xGe_{1-x}, Si-Si_xGe_{1-x}, Si_xGe_{1-x}-Si and Si_xGe_{1-x}-Ge-Si core-(double-)shell nanowires. In the second part of the thesis, namely in Chapter 5 to 6, we will present the theoretical modeling of JJ-FET devices and logic gates, and their experimental demonstration using InAs quantum well heterostructures.

In Chapter 2, we first describe the growth mechanism and recipes of coherently strained Ge-Si_xGe_{1-x} and Si-Si_xGe_{1-x} core-shell nanowires. Then we present the TEM imaging techniques

to study the crystal structure and morphology of our core-shell nanowires. We also discuss the concept of strain and show the method to calculate the strain distribution in core-shell nanowires. Afterwards, we discuss the Raman spectroscopy and our experimental setups that allow us to acquire Si-Si and Ge-Ge optical phonon modes from individual nanowires in a non-invasive manner. Then we discuss the lattice dynamic theory that allows us to convert the calculated strain in Si, Ge and Si_xGe_{1-x} alloy to strain-induced shifts of the Si-Si and Ge-Ge optical phonon modes. Subsequently, we present the calculation results of the strain profiles in the two types of core-shell nanowires and thus the shifted optical phonon modes, and compare them with the experimentally acquired Raman data. Lastly, we show a phenomenon where the shell growth rate depends on the orientation of the Si core for Si-Si_xGe_{1-x} core-shell nanowires. In short, this chapter summarizes the growth and structural characterization techniques that apply to all the radial nanowire heterostructures discussed in the thesis.

In Chapter 3, we present the growth recipe, TEM imaging, Raman spectroscopy, and strain calculation results of Si_xGe_{1-x}-Si core-shell nanowires. We apply lattice dynamic theory to calculate Si-Si optical phonon modes under strain and compare the calculation results with the experimental data. They show good agreement and suggest that we can grow coherently strained Si_xGe_{1-x}-Si core-shell nanowires. We also demonstrate *n*-type MOSFETs using Si_xGe_{1-x}-Si core-shell nanowires as channel and find an electron mobility enhancement over the control devices using bare Si nanowires as channel.

In Chapter 4, we present the growth results of strained Si_xGe_{1-x}-Ge-Si core-double-shell nanowires and perform the same set of structural characterizations described in Chapters 2 and 3. Unlike our coherently strained Ge-Si_xGe_{1-x}, Si-Si_xGe_{1-x} and Si_xGe_{1-x}-Si core-shell nanowires, we

find the strain in the Ge and Si shells of Si_xGe_{1-x}-Ge-Si core-double-shell nanowires is partially relaxed. Subsequently, we demonstrate both *n*-type and *p*-type MOSFETs using Si_xGe_{1-x}-Ge-Si core-double-shell nanowires as channel aimed for mobility enhancement of both electrons and holes over the bare Si nanowire counterparts. Then we show the technique to extract the valence band offset between the Ge and Si shell by experimentally probing the hole transport at the liquid nitrogen temperature in combine with simulations. Finally, we present the impact of the shell thickness on the performance of Si_xGe_{1-x}-Ge-Si core-double-shell nanowire MOSFETs.

In Chapter 5, we first discuss the concept of superconductivity and Josephson effects. We model the JJ-FET assuming a short ballistic operation, and construct the associated logic gates and memory elements. Then we study the operation of these logic and memory devices by performing transient analysis simulations, emphasizing on examining the criteria of signal restoration and fan-out. We also show that a global clock can substantially improve the fan-out of JJ-FET logic gates. Afterwards, we discuss design considerations related to the impact of mesoscopic effects and trade-offs among the device parameters. Lastly, we detail the approach used to implement the numerical simulation.

In Chapter 6, we first describe the growth process of the InAs quantum well heterostructure substrate and the JJ-FET fabrication procedures, followed by demonstrating JJ-FET current-voltage ($I - V$) characteristics. We then present self-consistent Poisson-Schrödinger simulation results at various V_G and temperatures to reveal the electrostatics in the heterostructure. We also fabricate long-channel MOSFETs as control devices to measure their $I - V$ and capacitance-voltage ($C - V$) characteristics. Subsequently, we extract the interface trap state density based on the simulated and measured $C - V$ data. Finally, we discuss the non-idealities of the fabricated JJ-

FETs compared to the theoretical model described in Chapter 5, and analyze how they will affect the realization of practical JJ-FET logic gates.

In Chapter 7, we conclude the thesis and suggest recommendations for future directions related to the production of nanowire MOSFETs, and the implementation of practical JJ-FET logic devices. We also discuss the fabrication process and measurement results of Si-based JJ-FETs, and identify the most important factors of their experimental realization.

Chapter 2 : Shell Morphology and Raman Spectra of Epitaxial Ge-Si_xGe_{1-x} and Si-Si_xGe_{1-x} Core-Shell Nanowires[1]

2.1 Introduction

We discuss the growth mechanism of our radial nanowire heterostructures, namely the strained epitaxial core-(multi-)shell nanowires. The core-(multi-)shell nanowires are grown using a combination of VLS growth mechanism for the core, followed by *in-situ* epitaxial shell growth(s) using ultra-high vacuum CVD. We also present the techniques to perform structural characterizations, including planar and cross-sectional TEM imaging, strain calculation and Raman spectroscopy. In this chapter, we use the epitaxial Ge-Si_xGe_{1-x} and Si-Si_xGe_{1-x} core-shell nanowires as the platform, to illustrate the general growth process and structural analysis procedures applicable to the Si-Ge based radial nanowire heterostructures extending through Chapters 2 - 4. We first describe the VLS mechanism and then discuss the growth result of the Ge and Si cores, which are the fundamental building blocks of our radial nanowire heterostructures. The rest of this chapter focuses on investigating the shell morphology, strain distribution and Raman spectra of epitaxial Ge-Si_xGe_{1-x} and Si-Si_xGe_{1-x} core-shell nanowire heterostructures.

Planar and cross-sectional TEM imaging reveal that the VLS growth yields cylindrical Ge and Si nanowire cores, growing along the <111> and <110> or <112> directions, respectively. A

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[1] Part of this chapter was published previously: [33] F. Wen, D. C. Dillen, K. Kim, and E. Tutuc, "Shell morphology and Raman spectra of epitaxial Ge−Si_xGe_{1-x} and Si−Si_xGe_{1-x} core-shell nanowires," *Journal of Applied Physics,* vol. 121, p. 234302, 2017. and master thesis of F. Wen with the same title.

F. Wen performed the nanowire growth, TEM, Raman measurements, simulations, calculations, with assistance from D. C. Dillen and K. Kim. F. Wen and E. Tutuc analyzed the data and co-wrote the manuscript. All authors have contributed to and approved the final version of the manuscript.

hexagonal cross-sectional morphology is observed for Ge-Si_xGe_{1-x} core-shell nanowires, terminated by six {112} facets. Two distinct morphologies are observed for Si-Si_xGe_{1-x} core-shell nanowires that are either terminated by four {111}, and two {100} planes associated with the <110> growth direction, or four {113}, and two {111} planes associated with the <112> growth direction. We show that the Raman spectra of Si-Si_xGe_{1-x} is correlated with the shell morphology due to the epitaxial growth-induced strain, with the core Si-Si mode showing a larger red shift in <112> Si-Si_xGe_{1-x} core-shell nanowires compared to their <110> counterparts. We compare the experimental Ge-Ge and Si-Si Raman mode values in the core regions with calculations based on a continuum elasticity model coupled with the lattice dynamic theory, and find the calculated and measured optical phonon frequencies in the core regions are in good agreement.

The chapter organization is as follows. Section 2.2 discusses the VLS mechanism in detail and the growth recipes we use to grow Ge-Si_xGe_{1-x} and Si-Si_xGe_{1-x} core-shell nanowires. Section 2.3 shows the planar view TEM imaging data of Ge-Si_xGe_{1-x} and Si-Si_xGe_{1-x} core-shell nanowires, and the approach to analyze the data. In Section 2.4, we present the cross-sectional TEM imaging data of those nanowires to reveal the shell morphology. In Section 2.5, we discuss the fundamentals of strain and the technique to calculate strain for radial nanowire heterostructures using finite element method (FEM). Section 2.6 presents the principles of Raman spectroscopy and the experimental approach to acquire Raman spectrum from individual nanowires. Section 2.7 shows the lattice dynamic theory, used to correlate strain and strain-induced shift of the optical phonon modes. In Section 2.8, we present the calculation results of the strain tensor for Ge-Si_xGe_{1-x} and Si-Si_xGe_{1-x} core-shell nanowires, and compare the calculated and experimental Raman modes under strain in the core regions of those nanowires. Section 2.9 shows a phenomenon where we

find the CVD growth rate of the same crystal plane of the Si_xGe_{1-x} shell depends on the orientation of the Si core for Si-Si_xGe_{1-x} core-shell nanowires. Section 2.10 summarizes the chapter.

2.2 Growth of Ge-Si_xGe_{1-x} and Si-Si_xGe_{1-x} core-shell nanowires

Si and Ge are anisotropic cubic crystals. Therefore, the orientation of Si-Ge based nanowires plays an essential role to determine the mechanical and electronic properties of core-shell nanowires. In addition, it requires a fundamental understanding of the hetero-interface properties and an exquisite control of the epitaxial shell growth to take advantage of the radial nanowire heterostructures. Hence, we need to understand both core and shell growths adequately to engineer the desired heterostructure. The Ge and Si nanowire cores are grown via the VLS method. The VLS growth mechanism is widely used as a bottom-up approach to synthesize single crystal nanowires [34]. Figure 2.1 depicts the process of the VLS growth, which consists of three stages. First, a thin metal film is deposited onto the semiconductor growth substrate, e.g. Au on Si. By heating the substrate, the metal film melts and forms eutectic liquid droplets with the substrate material [panel (a)]. At the same time, growth precursors, such as silane (SiH_4) are introduced in the growth chamber. The SiH_4 molecule decomposes at the surface of the liquid droplet that catalyzes the decomposition. Hydrogen atoms escape in the form of H_2 gas while Si atoms enter the liquid droplet, leading to a supersaturation of Si in the liquid [panel (b)]. By increasing the precursor partial pressure, a sufficiently large supersaturation pushes Si to nucleate at the boundary between the liquid and solid phase at the bottom of the droplet. Consequently, the solid phase grows up in the form of a nanowire with the droplet remaining on top [panel (c)]. The process is called VLS because all the three phases of vapor, liquid and solid are involved. It circumvents the generally slow growth of crystals through the direct adsorption of a vapor phase

onto the solid surface, thanks to the catalytic liquid alloy. On the other hand, the shell growth uses a non-catalyzed CVD approach directly for a precise control over the growth rate.

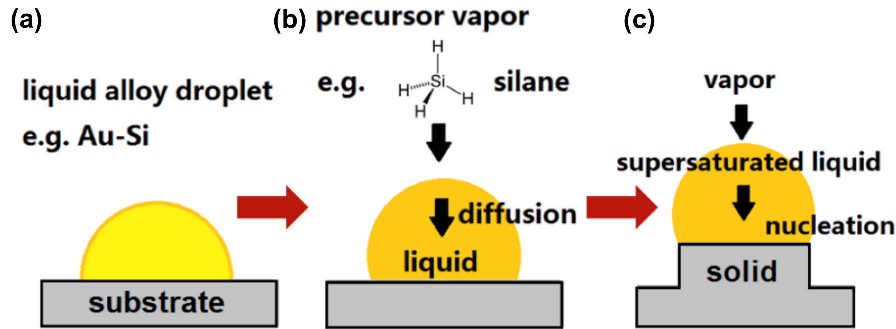

Figure 2.1: Schematic illustrating the VLS growth process. (a) Thermal annealing to form liquid alloy droplet. (b) Precursor molecules cracking at the vapor/liquid interface and diffusing through the liquid droplet. (c) Nucleation at the liquid/solid interface. (Figure adapted from Ref. [35])

Although the growth of Si nanowires was proposed a few decades ago, many fundamental questions about the VLS mechanism remain to be understood. Molecular dynamic simulation and phase-field modeling provide useful insights to explain part of the experimental results, but these theoretical models have limitations of short time scale due to limited computation resources and ambiguity in the choice of parameters to represent the realistic scenario [36, 37]. Experimental results show that the VLS growth depends strongly on both thermodynamics and the kinetic process. For example, there are three different growth orientations in the same batch of Si nanowires grown epitaxially on a Si(100) substrate depending on the diameter. Nanowires with smaller diameter favor the <110> direction, larger diameter nanowires favor the <111> direction and intermediate ones are along the <112> direction [38]. Figure 2.2(a) shows the statistical data of the number density vs. diameter for different growth directions. Si nanowires with diameter greater than 40 nm prefer the <111> direction, whereas those with the diameter less than 20 nm mostly have <110> orientations. The diameter dependence of the growth direction is explained to

a thermodynamics perspective by considering the total free energy of the nanowire, which is decided by the Au/Si interfacial energy and the nanowire sidewall surface energy, and minimized for the preferred growth direction. Moreover, kinetically induced morphology change of the nanowire growth is observed by changing the temperature and precursor partial pressure [39, 40]. Figure 2.2(b) presents one frame extracted from an *in-situ* TEM movie of a Si nanowire grown with Si_2H_6 as precursor at 2.5 mTorr. Both end segments of the nanowire are grown at 425 ºC and appear straight, yet the initial segment is along the <111> direction and the final one is along the <112> direction. The second segment grown at 380 ºC exhibits no well-defined direction, and the third segment grown at 400 ºC is kinked. Since Au does not wet the Si nanowire sidewall and the transition is reversible, it is concluded that the morphology change is the consequence of kinetics rather than of the thermodynamic preference. Figure 2.2(c) shows that the Si nanowire growth direction can be controlled by changing the precursor partial pressure. At 380 ºC and a SiH_4 (2% diluted in He) total pressure of 3 mBar, the Si nanowire grows along the <111> direction. When the total pressure is increased to 15 mBar, the Si nanowire kinks to the <112> direction. Hence, the morphology of the nanowire growth is changed if the system pressure changes.

In our own VLS growths, we find the Si nanowires grow along both <110> and <112> directions at 420 ºC and a SiH_4 partial pressure of 2.5 - 5 Torr, or 460 ºC and a SiH_4 partial pressure of 10 Torr. On the other hand, Si nanowires grow exclusively along the <110> direction at 410 ºC and a SiH_4 partial pressure of 10 Torr. We have not observed a clear diameter dependence of the above two growth directions, our Si nanowires of both orientations exhibit a similar diameter range of 20 - 40 nm. Furthermore, the Si nanowire grows along the <111> direction at 500 ºC and a SiH_4 partial pressure of 0.15 - 0.2 Torr, and has a diameter > 60 nm. During these growths, SiH_4 is the only gas introduced into the growth chamber, and its partial pressure represents the total chamber

pressure since our SiH_4 is not diluted in a carrier gas. Combining these literature studies and our own experimental results, we hypothesize that Si nanowires with larger diameters (> 60 nm), higher growth temperatures (> 500 ºC) and lower SiH_4 partial pressures (< 0.2 Torr) favor the <111> growth direction, while the opposites (< 40 nm, < 410 ºC, > 10 Torr) favor the <110> growth direction and the intermediate scenario yields the <112> growth direction. However, we have not systematically examined the boundary of the growth condition that leads to the respective growth direction. The VLS growth of Ge nanowires should follow the same pattern given the similarity of the two materials. We optimize the growth recipe so that our Ge nanowires grow exclusively along the <111> direction at 270 ºC and a GeH_4 partial pressure of 0.5 Torr, the total chamber pressure is 2.5 Torr since GeH_4 is 20% diluted in He. The Si and Ge nanowires constitute the cores of the Ge-Si_xGe_{1-x} and Si-Si_xGe_{1-x} core-shell nanowires investigated in this chapter.

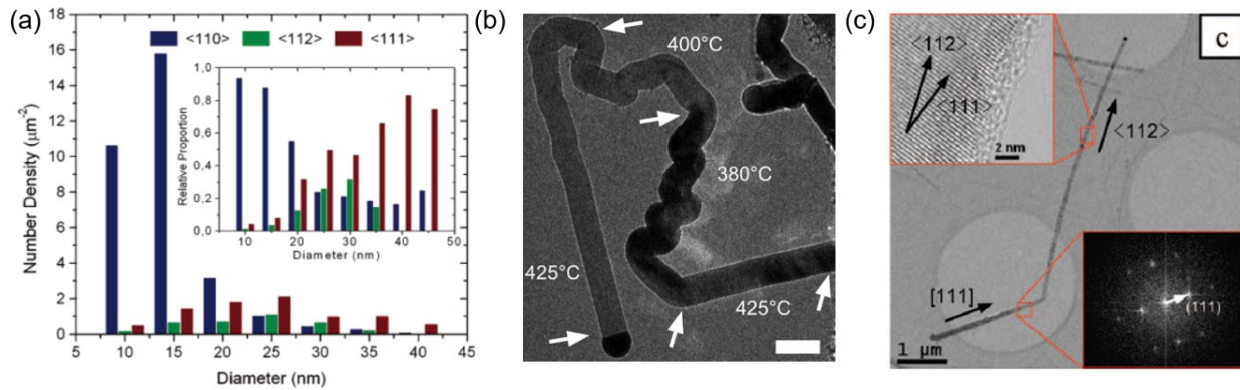

Figure 2.2: (a) Number density vs. diameter for different orientations of Si nanowires. Inset is the relative proportion of each orientation. (b) A frame from an *in-situ* TEM imaging movie of the Si nanowire growth, with temperature changed a few times in the process. Arrows mark the onset and end of the temperature window. Scale bar is 250 nm. (c) A low-magnification TEM image of a two-step growth, the Si nanowire kinks to the <112> direction from <111> when the total pressure of the diluted SiH_4 changes from 3 to 15 mBar. (Figure adapted from Refs. [38-40])

Figure 2.3 illustrates the growth of Ge-Si_xGe_{1-x} and Si-Si_xGe_{1-x} core-shell nanowires investigated in the chapter. The growth consists of a sequence of VLS core growth, followed by

in-situ shell growth using ultra-high-vacuum CVD. An 8 Å thick Au film is evaporated onto a Si(111) substrate following the removal of native oxide using diluted hydrofluoric (HF) acid. The substrate is then transferred to a cold wall ultra-high-vacuum CVD chamber, and annealed in a H_2 ambient at 370 °C, which leads to the formation of Au-Si eutectic alloy particles of around 20 nm in diameter that serve as catalysts for the VLS growth. For the nanowires investigated in this chapter, the Ge nanowire cores are grown at a temperature of 270 °C and pressure of 2.5 Torr using GeH_4 (20% diluted in He) as precursor, while the Si nanowire cores are grown at 460 °C and 10 Torr using SiH_4 (100%) as precursor. All growth pressure mentioned in this thesis refers to the total chamber pressure. The epitaxial Si_xGe_{1-x} shell growth is then performed *in-situ* at various temperatures, 40 mTorr pressure, using a mixture of GeH_4 and SiH_4, with flows detailed in Table 2.1. Table 2.2 summarizes the growth conditions for the different samples examined in this chapter. Growths A, B, C, D and E correspond to NW88, NW213, NW184, NW212 and NW208 in our nanowire growth catalog, respectively. Figure 2.4 presents the SEM imaging data of nanowires from growths A and C, which are the cross-sections of parts of the nanowire growth substrates. Ge-Si_xGe_{1-x} core-shell nanowires usually grow vertically and epitaxially along the Si(111) substrate [panel(a)], while Si-Si_xGe_{1-x} core-shell nanowires grow along different directions [panel(b)], both exhibiting no kinks. The growth morphology of Ge-Si_xGe_{1-x} and Si-Si_xGe_{1-x} core-shell nanowires is determined by the VLS growth stage of their cores. The kinking or worm-like feature near the tip is due to the additional VLS growth during the shell growth process. Since the precursor partial pressure in the shell growth stage is much lower than that during the core growth, the additional axial VLS growth is negligible. Bare Ge and Si nanowires using the same VLS recipes of the cores of the two core-shell nanowires have also been grown, serving as baselines to understand the core morphology and extract unstrained optical phonon mode frequencies.

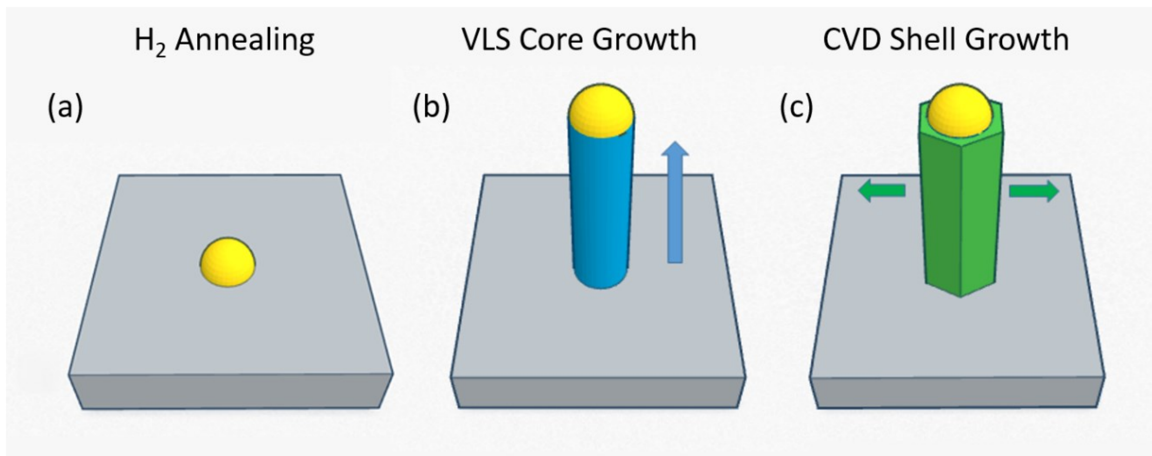

Figure 2.3: Schematics illustrating the Ge-Si_xGe_{1-x} or Si-Si_xGe_{1-x} core-shell nanowire growth process. (a) Hydrogen annealing. (b) VLS core growth. (c) Epitaxial CVD shell growth. Arrows represent the growth direction in each growth regime.

Table 2.1: Growth conditions of the core-shell nanowires discussed in Chapter 2

Core-shell nanowire type	GeH_4/SiH_4 flow during core growth (s.c.c.m.)	GeH_4/SiH_4 flow during shell growth (s.c.c.m.)
Ge-Si_xGe_{1-x}	50/0	10/50
Si-Si_xGe_{1-x}	0/100	10/50

Table 2.2: Specifications of the core-shell nanowire growths discussed in Chapter 2

Sample name	Growth type	Shell growth temperature /time	Shell Si content[1]	t_{sh} {112}	t_{sh} {100}	t_{sh} {111}[2]	t_{sh} {111}[3]	t_{sh} {113}
A (NW88)	Ge-Si_xGe_{1-x}	385 °C /60 min	57%	4.5 nm	N/A	N/A	N/A	N/A
B (NW213)	Si-Si_xGe_{1-x}	390 °C /60 min	65%	N/A	2.9 nm	3.0 nm	3.3 nm	5.0 nm
C (NW184)	Si-Si_xGe_{1-x}	420 °C /60 min	68%	N/A	3.3 nm	3.4 nm	4.8 nm	7.8 nm

Table 2.2: continued

D (NW212)	Si-Si_xGe_{1-x}	450 °C /12.5 min	79%	N/A	3.0 nm	3.1 nm	5.6 nm	9.5 nm
E (NW208)	Si-Si_xGe_{1-x}	370 °C /60 min	N/A	N/A	2.0 nm	2.0 nm	N/A	N/A

1: The method to extract the shell Si content will be discussed in Section 2.6.4.
2: This column represents the {111} facet shell thickness for the Si-Si_xGe_{1-x} core-shell nanowires oriented along the <110> direction.
3: This column represents the {111} facet shell thickness for the Si-Si_xGe_{1-x} core-shell nanowires oriented along the <112> direction.

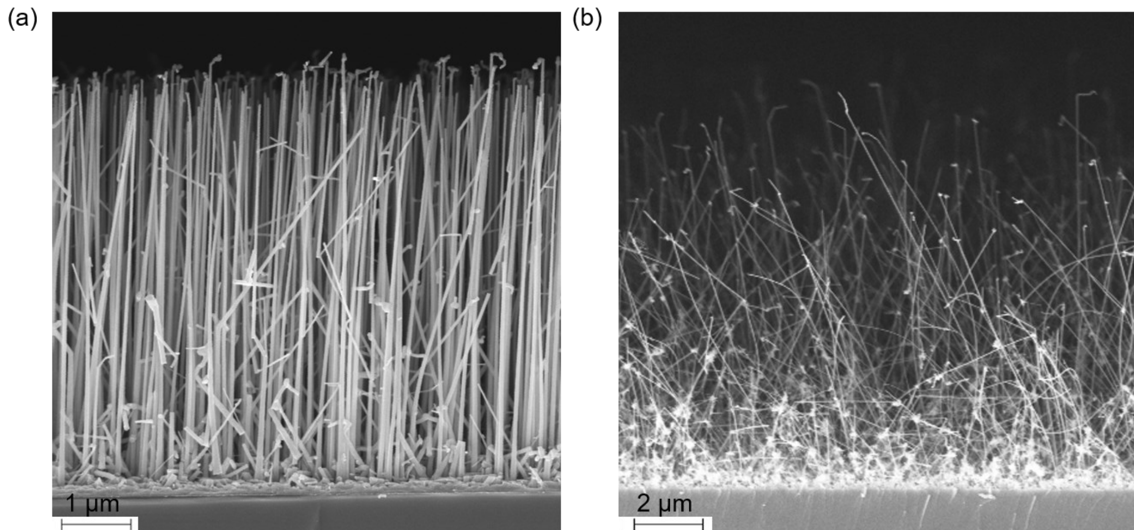

Figure 2.4: SEM images of (a) Ge-Si_xGe_{1-x} and (b) Si-Si_xGe_{1-x} core-shell nanowires from growth A and C.

2.3 Planar view TEM imaging

We apply planar view TEM imaging to confirm the single crystalline nature of our core-shell nanowires and determine their growth directions. The planar view TEM samples are convenient to make. We first prepare a solution of nanowires by sonicating the growth wafer in ethanol and then drop cast the solution onto a carbon lacey copper grid. Since Si_xGe_{1-x} shells grow

epitaxially on the Ge and Si cores, we have single crystal structures where the growth direction of the Ge-Si_xGe_{1-x} core-shell nanowire is along the <111> crystal axis, and that of the Si-Si_xGe_{1-x} core-shell nanowire can be either <110> or <112> crystal axes. These results are also consistent with the bare Si and Ge nanowire growths. Figure 2.5(a-c) illustrates the planar view TEM images of a <111> oriented Ge-Si_xGe_{1-x} core-shell nanowire, a <110> and a <112> oriented Si-Si_xGe_{1-x} core-shell nanowires, which belong to growths NW169 and NW184 in our nanowire catalog, respectively. The core-shell nanowires are indeed single crystal and do not have faceted sidewalls. The insets are the corresponding fast Fourier transforms (FFTs) of the TEM imaging data. The growth direction of the nanowire can be determined by investigating the diffraction pattern or the FFT directly. To observe diffraction spots in the FFT data, diligent search of nanowires across a single tilt TEM sample holder or using a double-tilt sample holder is necessary, since the electron beam needs to be parallel to the orientation of a certain crystal plane in the nanowire, which is the zone axis. The arrows in both the main panels and their insets mark the axial orientations of the nanowires. In the FFT, if the arrow points from one reciprocal lattice spot to its symmetric spot about the center, then the index of that reciprocal lattice spot reveals the axial orientation of the nanowire. For example, in the FFT data of Fig. 2.5(a) inset, the arrow points from $(\bar{1}\bar{1}\bar{1})$ to (111) reflection, therefore the axial orientation of the nanowire is along <111>. Figure 2.6(a-c) presents the approach to label the reciprocal lattice indices for the three types of nanowires, respectively. We first compare the FFTs with the standard diffraction patterns of cubic Si/Ge assuming the electron beam along a certain zone axis. The reciprocal lattice indices are then revealed after overlapping the diffraction spots in the FFTs with those in the standard patterns. The reciprocal lattice constant can also help identify a crystal plane index efficiently, which is directly measured as the distance between an individual reflection spot and the direct beam spot in the center of the

FFT. It is noteworthy that in Fig. 2.6(c), the FFT data of the <112> oriented Si-Si_xGe_{1-x} core-shell nanowire shows 1/3{422} reflections along the [111] zone axis, which are kinetically forbidden for face-centered cubic crystals like Si and Ge. Their appearance is attributed to {111} stacking faults and interpenetrating twins, and in turn suggests the existence of such types of defects in our <112> oriented Si-Si_xGe_{1-x} core-shell nanowires [41].

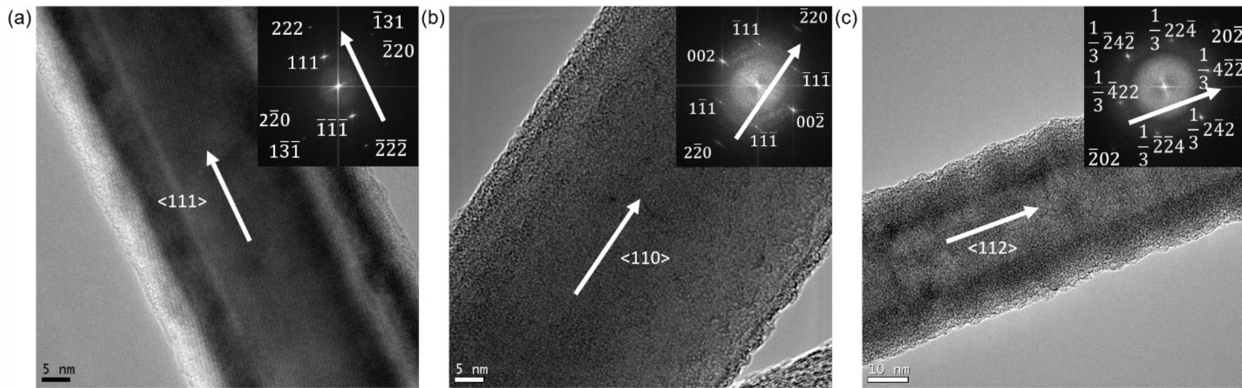

Figure 2.5: Planar view TEM images of Ge-Si_xGe_{1-x} and Si-Si_xGe_{1-x} core-shell nanowires. (a) <111> oriented Ge-Si_xGe_{1-x} core-shell nanowire. (b) <110> oriented Si-Si_xGe_{1-x} core-shell nanowire. (c) <112> oriented Si-Si_xGe_{1-x} core-shell nanowire. The insets are the FFTs of the TEM images. Arrows indicate the nanowire growth directions in each panel.

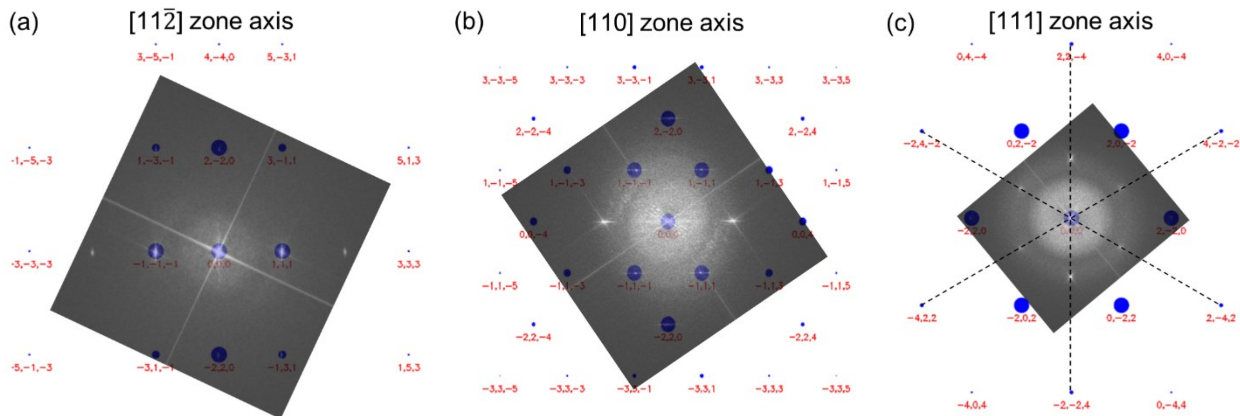

Figure 2.6: Determination of the reciprocal lattice indices in the FFTs by overlapping the FFTs and the standard diffraction patterns of cubic Si/Ge. (a) <111> oriented Ge-Si_xGe_{1-x} core-shell nanowire, assuming

the zone axis along $[11\bar{2}]$. (b) <110> oriented Si-Si_xGe_{1-x} core-shell nanowire, assuming the zone axis along [110]. (c) <112> oriented Si-Si_xGe_{1-x} core-shell nanowire, assuming the zone axis along [111]. Figure 2.6: continued.

2.4 Cross-sectional TEM imaging

Though the planar view TEM imaging helps determine the growth direction of nanowires, it cannot provide information about the core or shell morphology. Cylindrical morphology for both core and shell are usually considered for the purpose of strain calculations in group IV-based nanowires [42-44], and hexagonal morphology are examined for III-V compound-based nanowires [45, 46]. While it is common to assume, and pedagogically easier to describe a cylindrical shape for both core and shell, an epitaxial crystal (shell) growth on a non-planar substrate may not be fully conformal. Indeed, a cylindrical epitaxial shell growth on a nanowire core would be terminated by many high index planes, as opposed to a few energetically favorable low index facets. Consequently, it is important to accurately determine the shell morphology in epitaxial core-shell nanowires and its impact on the elastic strain. To address this problem, we employ cross-sectional TEM imaging to probe the crystal structure and shell morphology of both Ge-Si_xGe_{1-x} and Si-Si_xGe_{1-x} core-shell nanowires, in addition to the planar view TEM imaging. Cross-sectional TEM sample preparation is much more involved and detailed as follows: We first disperse the nanowire solution onto a Si substrate with 285 nm SiO_2 grown by thermal oxidation, which is pre-patterned with alignment markers. We subsequently deposit a 60 nm thick Al_2O_3 film by atomic layer deposition (ALD). The amorphous SiO_2 and Al_2O_3 oxide films provide a sharp contrast and well-defined boundaries with respect to the single crystal nanowire cross-section. We then deposit a patterned TaN film of 10×1 μm^2 rectangular shape onto the center of a pre-located nanowire, with the length perpendicular to the nanowire axis through electron beam lithography (EBL), metal

sputtering and lift-off. The TaN rectangle is used as the alignment marker for the dicing saw to trim the substrate into a 3 × 0.1 mm^2 slab. It also serves as a protective layer during the subsequent focus ion beam milling stage to thin the region containing the nanowire cross-section down to 50 - 100 nm in thickness. Bare Si nanowires are also processed to identify the core morphology. Figure 2.7 presents the cross-sectional TEM image of a <110> oriented Si nanowire from growth NW179 in our nanowire catalog, which clearly exhibits a cylindrical shape.

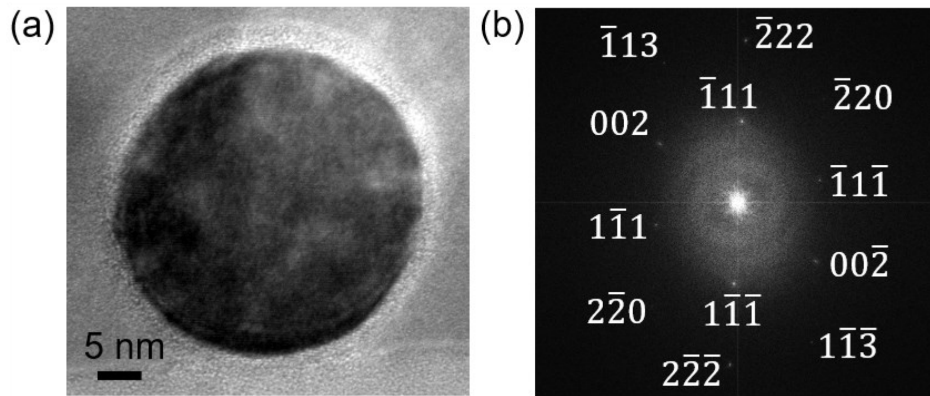

Figure 2.7: (a) Cross-sectional TEM image of a <110> oriented Si nanowire. (b) FFT of panel (a) data.

Figure 2.8 presents the results of cross-sectional TEM imaging on Ge-Si_xGe_{1-x} [panels (a-d)] and Si-Si_xGe_{1-x} [panels (e-l)] core-shell nanowires, for growths A and B, respectively. Figure 2.8(a) shows the schematic of a Ge-Si_xGe_{1-x} core-shell nanowire, constructed based on the high-resolution TEM (HRTEM) data of Fig. 2.8(b), their FFT of Fig. 2.8(c), as well as the dark field scanning TEM (STEM) data of Fig. 2.8(d). The data of Fig. 2.8(b-d) reveals a cylindrical Ge nanowire core, and a faceted epitaxial shell with a regular hexagonal cross-section. Examination of the FFT data of Fig. 2.8(c) reveals spots associated with the {224} and {220} planes. Comparing these data with standard diffraction patterns allows us to identify the <111> crystal axis as the nanowire growth direction [Fig. 2.6(c)]. Because the orientation of Fig. 2.8(b) and 2.8(c) data is

identical, we can translate the diffraction spots to plane indices in Fig. 2.8(b), and unambiguously identify the shell facets as the {112} planes. We note that the TEM data acquired for multiple Ge-Si_xGe_{1-x} core-shell nanowire growths is all consistent with that shown in Fig. 2.8(b-d). For Si-Si_xGe_{1-x} core-shell nanowire heterostructures however, the TEM analysis of multiple samples reveals cylindrical Si cores with two distinct shell morphologies, which we label in the following as type I and type II. Figure 2.8(e) represents the schematic of type I Si-Si_xGe_{1-x} core-shell nanowires, constructed based on the HRTEM data of Fig. 2.8(f), the corresponding FFT data of Fig. 2.8(g), as well as the STEM data of Fig. 2.8(h). Figure. 2.8(i) represent the schematic of type II Si-Si_xGe_{1-x} core-shell nanowires, constructed based on the HRTEM data of Fig. 2.8(j), the corresponding FFT data of Fig. 2.8(k), as well as the STEM data of Fig. 2.8(l). By comparison to the type I shell morphology, type II samples show a hexagonal shell elongated along one direction, with a non-uniform thickness. The FFT data of Fig. 2.8(f) and 2.8(j) reveal spots associated with the {200}, {220}, {113} and {111} planes for type I, and {111}, {220}, {042} and {113} planes for type II Si-Si_xGe_{1-x} core-shell nanowires, respectively. For type I nanowires the angle between two equivalent (inequivalent) facets is 110° (125°), while for type II nanowires equivalent (inequivalent) facets form a 117.3° (121.4°) angle. A comparison of these values with the angles between different crystal planes allows us to identify two {100} and four {111} planes as the facets of type I nanowires, corresponding to a <110> growth axis, and also two {111} and four {113} planes as the shell facets of type II nanowires, corresponding to a <112> growth direction. We also double check the two growth directions by comparing the FFTs with the standard diffraction patterns [Fig. 2.6(a-b)]. The data of Fig. 2.8(e-l), and the presence of two distinct shell morphologies have been verified in multiple samples and in different growths.

Particularly noteworthy, the contrast between the cylindrical core and the hexagonal shell

morphologies can be related to the interplay between growth rate and surface diffusion during the VLS and CVD growth modes. Because the Au-catalyzed core VLS growth has a much higher precursor partial pressure, and thus growth rate compared to the un-catalyzed shell CVD growth, the ratio of diffusion to deposition rate for adatoms during core growth is significantly lower compared to the shell growth. The surface diffusion of adatoms during shell growth allows it to reach a morphology dictated by surface energy consideration. For diamond cubic crystals like Si and Ge, the surface should be terminated with low-index planes that minimize the surface energy. If the surface diffusion is low compared to the growth rate during shell growth, the shell growth will be conformal, hence cylindrical. The above argument applies not only to the shell growth, but also to the nanowire core growth. Indeed, <111> oriented Si nanowires grown at a lower (below 100 mTorr) SiH_4 partial pressures and elevated (above 500 °C) temperatures compared to the Si cores of the Si-Si_xGe_{1-x} core-shell nanowires discussed in this chapter, hence in a regime where the surface diffusion is dominant, have been shown to possess six {112} facets [47-49], consistent with theoretical calculations [50]. Energetic considerations (the surface energy of cubic Si and Ge is summarized in Table 2.3) indicate that Si nanowires grown along <110> crystal axis should be bound by two {100} and four {111} planes [51], similar to the <110> oriented Si-Si_xGe_{1-x} core-shell nanowire morphology of Fig. 2.8(e). Experimental observations of Si nanowire growth by the VLS mechanism along the <112> direction are less common, and appear to be associated with the presence of hexagonal phases [52]. An early study of Si micro-rods [53] oriented along the <112> crystal axis shows {111} and {113} facets, similar to the <112> nanowire morphology of Fig. 2.8(i). This combination of facets cannot be solely explained by surface energy considerations because {113} planes are expected to have much higher surface energy compared to low-index {100}, {110} and {111} planes, even after taking surface reconstruction into account [54].

Table 2.3: Surface energy of various surfaces for cubic Si and Ge [50]

Surface Orientation	Si (ergs/cm^2)	Ge (ergs/cm^2)
{100}	1879.82	1657.18
{110}	1535.88	1412.78
{111}	1254.24	1153.72
{112}	1330.28	1223.66
{113}	2921.98	2600.99

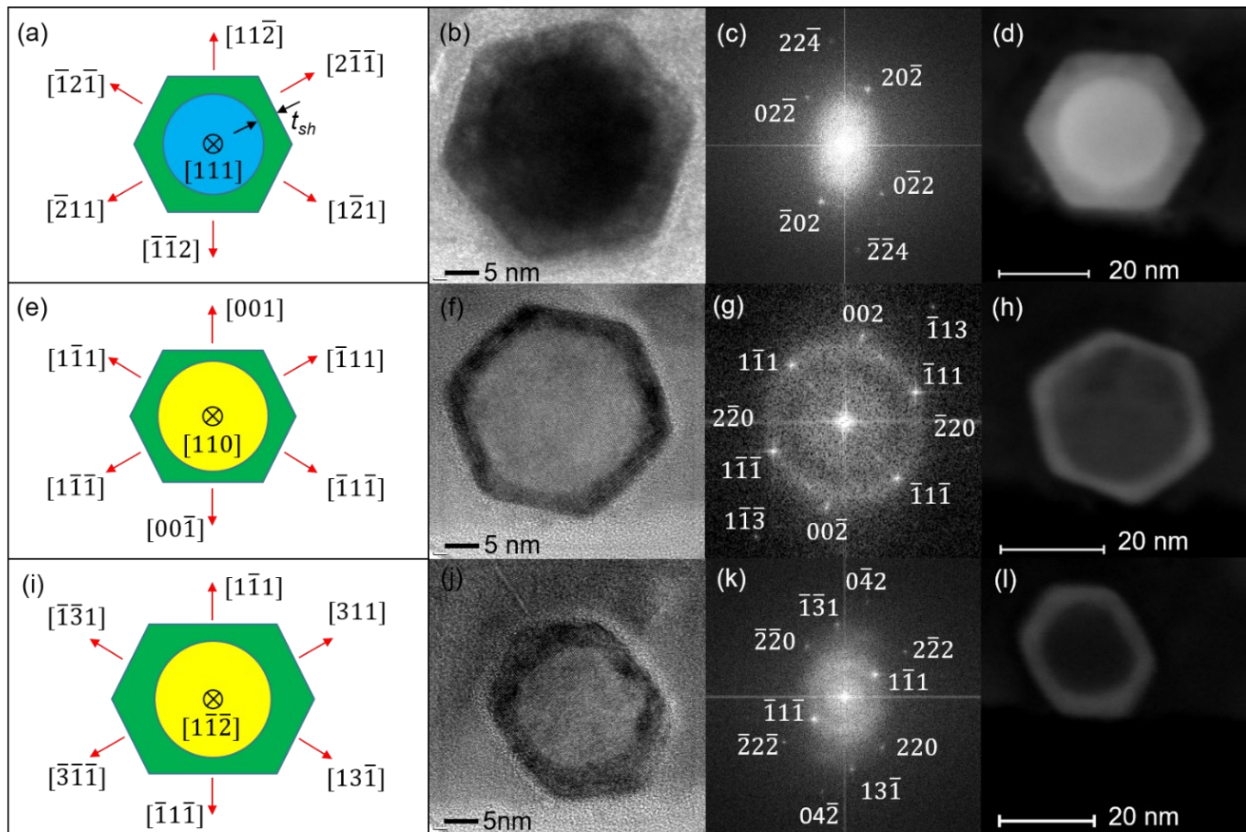

Figure 2.8: Schematics, HRTEM, FFT and STEM data of the three different types of core-shell nanowires discussed in Chapter 2. The HRTEM images and their FFTs are identical in orientation, enabling a direct correspondence between FFTs to plane indices in real space images. (a) Ge-Si_xGe_{1-x} nanowire with the growth direction along the <111> axis, showing a cylindrical Ge core, and hexagonal Si_xGe_{1-x} shell with six {112} facets. (b-d) Cross-sectional HRTEM, FFT and STEM data of a Ge-Si_xGe_{1-x} nanowire. (e) Type

I Si-Si_xGe_{1-x} nanowire with the growth direction along the <110> axis, showing a cylindrical Si core and hexagonal Si_xGe_{1-x} shell with two {100} and four {111} facets. (f-h) Cross-sectional HRTEM, FFT and STEM data of a <110> oriented Si-Si_xGe_{1-x} nanowire. (i) Type II Si-Si_xGe_{1-x} nanowire with the growth direction along the <112> axis, showing a cylindrical Si core and hexagonal Si_xGe_{1-x} shell with two {111} and four {113} facets. (j-l) Cross-sectional HRTEM, FFT and STEM data of a <112> oriented Si-Si_xGe_{1-x} nanowire. Figure 2.8: continued.

2.5 Strain calculation

2.5.1 Introduction to strain

In our radial nanowire heterostructures, elastic strain exists due to the lattice mismatch between the core and shell(s). Strain changes the spacing and symmetry of the crystal lattice and leads to significant alterations in many fundamental properties, including morphology, electronic band structure, charge carrier transport, optical absorption/emission, and phonon spectrum. Consequently, understanding the strain in the structure is crucial to effectively design and engineer a heterogeneous system.

Strain, generally a tensor quantity, is defined as the measure of deformation representing the displacement between particles in the object relative to a reference length, when there is a change in the configuration of a continuum body. The displacement of an object consists of two components: a rigid-body motion and a deformation. The component of rigid-body motion includes a concurrent translation and rotation of the object while maintaining the shape and size. Strain is a description of deformation regarding the relative displacement of part in an object, excluding the rigid-body motion. Displacement is a vector field defining the change in position of a given point between the strained and unstrained cases. The displacement vector $\boldsymbol{u}$ and the strain tensor are linked through the following equation in Cartesian coordinates:

$$\varepsilon_{ij} = \frac{1}{2}\left(\frac{du_i}{dx_j} + \frac{du_j}{dx_i}\right) \tag{2.1}$$

In the three-dimensional case, strain can be expressed as a second rank tensor:

$$\varepsilon_{ij} = \begin{bmatrix} \varepsilon_{xx} & \varepsilon_{xy} & \varepsilon_{xz} \\ \varepsilon_{yx} & \varepsilon_{yy} & \varepsilon_{yz} \\ \varepsilon_{zx} & \varepsilon_{zy} & \varepsilon_{zz} \end{bmatrix} \tag{2.2}$$

The indices correspond to the direction of force and the surface normal on which it is acting, e.g. ε_{xy} indicates a deformation in the y-direction of a surface whose normal is along the x-direction. Terms along the main diagonal of Eq. (2.2) RHS are the normal components of strain, representing the amount of stretch or compression along the material line element. The sign of the normal strain indicates the type of deformation it presents: a negative value designates a compressive strain, while a positive one corresponds to a tensile strain. The off-diagonal terms are shear components, defining the amount of distortion associated with the sliding of plane layers over each other if we decompose the object into planes, thus resulting in shear deformation. The requirement of no rigid body translations or rotations forces off-diagonal shear terms to be symmetric, e.g. $\varepsilon_{xy} = \varepsilon_{yx}$. Hence, the 9-component strain tensor can be reduced to 6 terms. For cubic crystals such as Si and Ge, stress can be directly related to strain through Hooke's Law:

$$\begin{bmatrix} \varepsilon_{xx} \\ \varepsilon_{yy} \\ \varepsilon_{zz} \\ 2\varepsilon_{yz} \\ 2\varepsilon_{zx} \\ 2\varepsilon_{xy} \end{bmatrix} = \begin{bmatrix} C_{11} & C_{12} & C_{12} & 0 & 0 & 0 \\ C_{12} & C_{11} & C_{12} & 0 & 0 & 0 \\ C_{12} & C_{12} & C_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & C_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & C_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & C_{44} \end{bmatrix} \begin{bmatrix} \sigma_{xx} \\ \sigma_{yy} \\ \sigma_{zz} \\ \sigma_{yz} \\ \sigma_{zx} \\ \sigma_{xy} \end{bmatrix} \tag{2.3}$$

where C_{ij} is the material's elastic stiffness constant that forms a second rank tensor with 36 entries. Notice that the cubic crystal symmetry reduces the required number of entries to only three: C_{11},

C_{12} and C_{44}. Indices of the stress tensor components follow the same rule of those of the strain tensor components. Stress is expressed in the unit of Pascal and can be thought of as the pressure in a material due to an applied force. Similar to the strain tensor, the stress tensor σ_{ij} is also symmetric and thus can be reduced to 6 components.

2.5.2 Strain calculations using the finite element method

We employ the continuum elasticity approach to solve the strain profile in Ge-Si_xGe_{1-x} and Si-Si_xGe_{1-x} core-shell nanowires. Since the core and shell regions have distinct morphology and the materials are anisotropic, the strain must be solved numerically. We calculate the elastic strain using a finite element modelling package (Abaqus®, Dassault Systemes). The simulated structure is a three-dimensional rod, with a sufficiently large length to approximate an infinite nanowire. The shell thickness (t_{sh}) is defined for each facet along the perpendicular from the core center to the facet plane [Fig. 2.8(a)]. We measure the shell thicknesses and crystal orientations based on the TEM results as summarized in Table 2.2. For example, in growth A, the Ge-Si_xGe_{1-x} core-shell nanowires examined here have $t_{sh} = 4.5$ nm. In growth C, for <110> oriented Si-Si_xGe_{1-x} core-shell nanowires $t_{sh} = 3.3$ nm and $t_{sh} = 3.4$ nm for the {100} and {111} facets, respectively, while for <112> oriented Si-Si_xGe_{1-x} core-shell nanowires $t_{sh} = 4.8$ nm and $t_{sh} = 7.8$ nm for the {111} and {113} facets, respectively. Figure 2.9 presents an example of the simulated structure representing a Ge-Si_xGe_{1-x} core-shell nanowire, with the meshing strategy displayed and the boundary between its core and shell highlighted in red lines. The coordinate system denotes the crystal orientation of the nanowire, consistent with that shown in Fig. 2.8(a). To include the anisotropic nature of the nanowire, we have to adjust the coordinate system of the simulated structure to match the TEM data, e.g. the axial direction and shell facets are <111> and <112>

oriented in this Ge-Si_xGe_{1-x} core-shell nanowire example. We mesh the structure with wedge shaped elements, leading to a finer spacing within the cross-section and a coarser one along the nanowire axis. This approach minimizes the computation demands while does not lose any accuracy, since the calculation is a quasi-two-dimensional problem in nature. To avoid rigid-body motion, which brings convergence problem, one end of the structure is fixed in space. A tie constraint is maintained between the inner surface of the shell and the outer surface of the core during the simulation for a coherently strained structure. The length of the simulated structure is 200 nm, long enough to make sure the strain does not vary along the axial direction near the center. The lattice mismatch between the core and shell is simulated by giving shell a thermal expansion coefficient α_s and heating the heterostructure from an initial temperature T_i to a final temperature T_f. For radial nanowire heterostructures with multiple shells, each shell is given its own thermal expansion coefficient according to the actual lattice mismatch with the core. The values of the three variables are chosen to satisfy Equation (2.4), while their actual values are unimportant.

$$\alpha_s(T_f - T_i) = \frac{l_s - l_c}{l_c} \tag{2.4}$$

where l_s and l_c are the lattice constants of the shell and core. To extract meaningful strain tensor values, the normal components of the simulated shell strain tensor need a subtraction of the isotropic hydrostatic strain due to thermal expansion. This is because the thermal expansion of the shell already induces a strain tensor, which has the three normal components of an equal value $\alpha_s(T_f - T_i)$ and zero shear components, before the deformation due to the interaction between the core and shell takes place. In addition, the shear components in the calculated strain tensor need to be divided by two as Abaqus uses the engineering strain. Table 2.4 presents the elastic stiffness matrix used in the simulation to determine the linear response to stress of Si, Ge and Si_xGe_{1-x}.

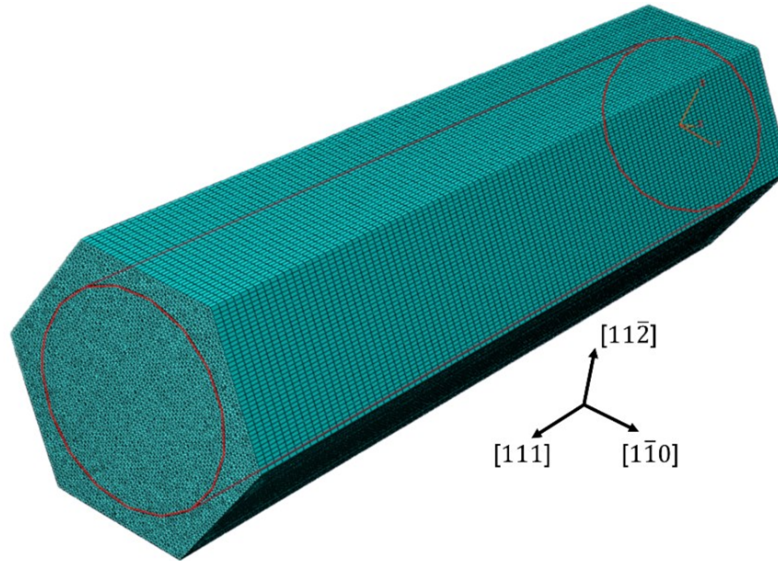

Figure 2.9: An example of the simulated structure for a <111> oriented Ge-Si_xGe_{1-x} core-shell nanowire, where the meshing elements are displayed and the contour of the core is highlighted by red lines. The coordinate presents the crystal orientation of the nanowire.

Table 2.4: Lattice constant and cubic elastic stiffness of Si and Ge [55, 56]

Material	Lattice Parameter (Å)	C_{11} (GPa)	C_{12} (GPa)	C_{44} (GPa)
Si	5.431	165.8	63.9	79.6
Ge	5.658	128.5	48.3	66.8

Lattice constants and elastic stiffness of Si_xGe_{1-x} alloy are calculated as the linear interpolation between those of Si and Ge.

2.6 Raman spectrum measurement

2.6.1 Introduction to Raman spectroscopy

Raman spectroscopy is a powerful non-destructive material characterization approach typically used to determine the vibrational modes of molecules. Raman spectroscopy is widely used to provide a structural fingerprint to identify materials and crystal structures. Raman

spectroscopy relies upon the inelastic scattering of visible to near-infrared photons by the vibrational modes of a sample, known as Raman scattering. A source of monochromatic light, usually from a laser, interacts with molecular vibrations, phonons or other excitations in the sample and results in an energy shift of the laser photons. The frequency and intensity of the scattered light are then measured to gather information about the vibrational modes in the sample, which are fingerprints of the sample since those modes of a molecule or crystal lattice are specific to each material. Figure 2.10 presents the energy level diagram in a sample to illustrate the transitions involved in Raman spectroscopy. The ground state of the sample's molecule has energy E_0 and the electronic excited state has hv_m higher energy than the ground level. In a real sample there can be more than one excited state, corresponding to different vibrational modes. The first transition shows the elastic scattering process where the incident and scattered photon has the same energy, known as Rayleigh scattering. The molecule is first excited to a virtual state (dotted line) from the ground state after absorbing a photon of energy hv_0, then decays back to the original ground state and emits a photon of the same energy. The second and third transitions present the inelastic Raman scattering process, where the scattered photon has lower and higher energy compared to the incident photon, known as Stokes scattering and anti-Stokes scattering, respectively. Similar to Rayleigh scattering, the molecule is still first excited to a virtual state, while the scattered photon can have hv_m lower or higher energy than the incident photon, depending on whether the initial and final states are the ground or excited states.

The procedure to acquire Raman spectrum is as follows, a sample is illuminated with a laser beam. Photons radiated from the illuminated spot is then collected and sent through a monochromator to filter out the elastically scattered photons at the same wavelength of the incident photon, while the inelastically scattered photons are directed to the detector. In a measured Raman

spectrum, we usually have the detected light intensity plotted against Raman shift. Raman shift is typically presented in a wavenumber, which has the unit of inverse length (cm^{-1}). It is calculated as $1/\lambda_{inc} - 1/\lambda_{scat}$, where λ_{inc} and λ_{scat} are the wavelength of the incident and scattered photon, respectively.

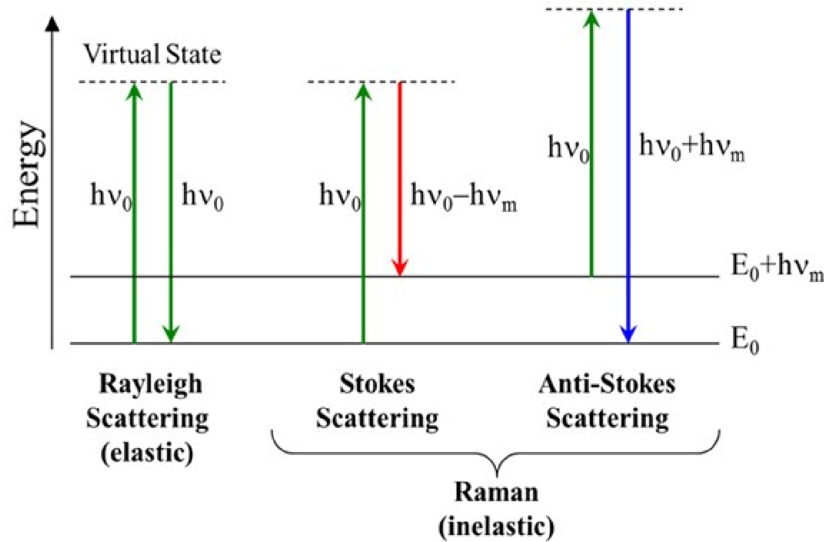

Figure 2.10: Schematics showing the elastic and inelastic scattering of photons in a material.

2.6.2 Raman Spectroscopy of Si and Ge

For cubic crystals such as Si and Ge, the discrete energy levels shown in Fig. 2.10 are the collective oscillations of the lattice. Phonons represent those excited states as quantized vibrational modes, and have an anisotropic energy vs. wavevector dispersion relation. Figure 2.11(a-b) shows the phonon dispersion curves for Si and Ge, respectively. Both Si and Ge have two atoms per primitive cell; hence, they exhibit three acoustic phonon branches as well as three optical phonon branches. The three branches of each kind further divide into a single longitudinal and two transverse branches. For both Si and Ge, the three acoustic phonon modes have zero frequency thus zero energy at the zone center (Γ point). On the other hand, the three optical phonon modes have finite energy. Both acoustic and optical phonon modes are triply degenerate at the zone

center. The magnitude of the momentum of a photon is negligible compared to that of a phonon, therefore only the zone-center phonon modes can show up in a Raman spectrum as required by momentum conservation. Additionally, energy conservation indicates that the wavenumber of the Raman mode is governed by the zone-center optical phonons that have a non-zero frequency. Consequently, only a single peak of 520 and 300.5 cm^{-1} can be observed in the Raman spectrum of Si and Ge, respectively.

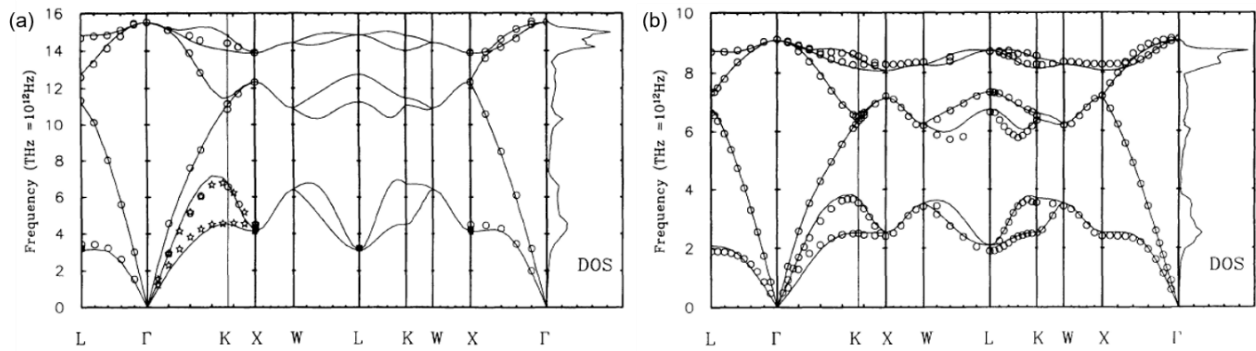

Figure 2.11: Phonon dispersion relation for (a) Si and (b) Ge. (Figure adapted from Ref. [57])

The frequency and dispersion of the phonon modes in Si and Ge are extremely sensitive to strain due to the modification of lattice spacing and crystal symmetry. Generally, strain can lead to a splitting of the triply degenerate zone-center optical phonon modes, along with a larger or smaller wavenumber of the Raman shift depending on whether the strain is compressive or tensile. Therefore, we can use Raman spectra to probe the strain in our radial nanowire heterostructures. We will discuss this method in detail in Section 2.7.

2.6.3 Experimental setup of Raman spectroscopy

We conduct Raman spectrum measurements using the Renishaw InVia μ-Raman spectrometer with a backscattering geometry, 532 nm incident laser with around 1 μm^2 focused

spot size and 13 kW·cm^{-2} power density, and 100× objective lens. The small laser spot size and high resolution of the microscope allow us to acquire spectrum from an individual nanowire. Raman measurements are first done on bare Ge and Si nanowires to provide baselines for the unstrained Ge-Ge and Si-Si Raman modes. We evaporate 20/60 nm Ti/Au onto the substrate before dispersing nanowires to eliminate Raman signals originating from the substrate that can overlap with those from the nanowires. Figure 2.12(a) presents the Raman spectrum of a bare Ge nanowire, showing the Ge-Ge mode at 300.5 cm^{-1}. On the other hand, we observe two types of Raman spectra for our bare Si nanowires, presented in the red and black lines in Fig 2.12(b), respectively. For the first type, there is a single Si-Si mode at 520.6 cm^{-1}. The second type shows two Si-Si Raman modes, with the nominal Si-Si mode slightly red shifted from 520.6 cm^{-1} to 519 cm^{-1} (Si-Si 1) and one additional Si-Si mode at around 495 cm^{-1} (Si-Si 2). In Figure 2.12(a-b), the peak positions corresponding to the active Raman modes are labeled with vertical dashed lines for all three types of bare Ge and Si nanowires.

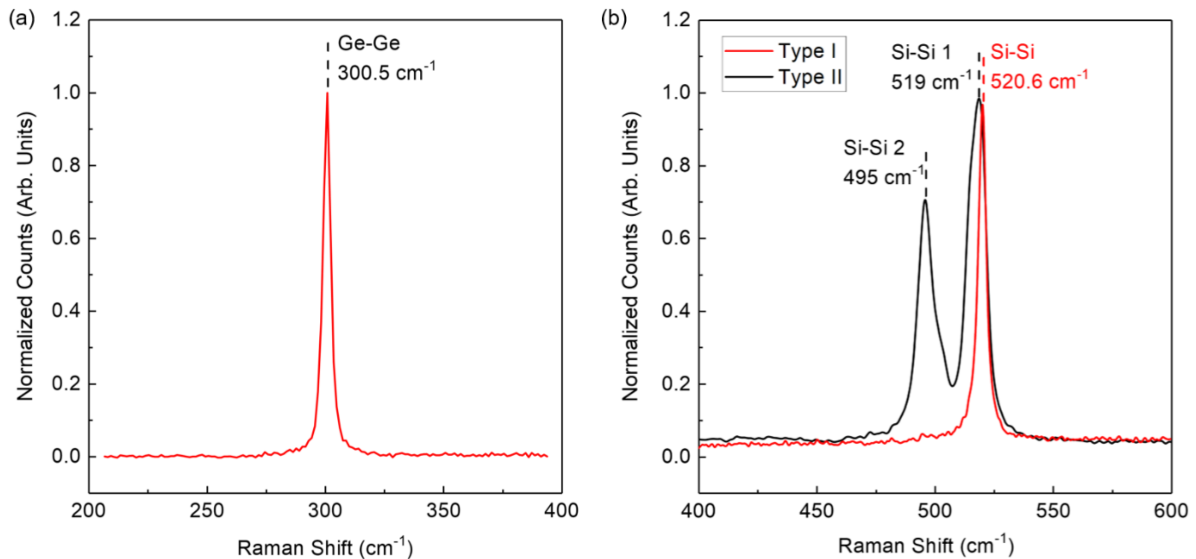

Figure 2.12: Raman spectra collected from individual Ge and Si nanowires. (a) Raman spectrum of a Ge nanowire (NW039 in the growth catalog). (b) Raman spectra of two types of Si nanowires, presented in red

and black lines, respectively (NW185 in the growth catalog). The peak position associated with individual Raman mode is marked with a vertical dashed line. Figure 2.12: continued.

2.6.4 Raman spectra of Ge-Si_xGe_{1-x} and Si-Si_xGe_{1-x} core-shell nanowires

Figure 2.13 reveals the Raman spectrum of an individual Ge-Si_xGe_{1-x} core-shell nanowire from growth A. We observe five Raman modes, including two Ge-Ge Raman modes for both the Ge core and Si_xGe_{1-x} shell, two Si-Ge and one Si-Si Raman modes for the Si_xGe_{1-x} shell. The peak at 305 cm^{-1} is associated with the core Ge-Ge Raman mode, showing a blue shift from the bulk value of 300.5 cm^{-1} due to a compressive strain. The peak at 285 cm^{-1} is associated with the shell Ge-Ge mode. Two Si-Ge Raman modes are observed for the Si_xGe_{1-x} shell at 394 and 419 cm^{-1}, due to the localized Si-Si motion in the neighborhood of different number of Ge atoms in the alloy [58]. The 394 cm^{-1} mode has a significantly higher intensity than the 419 cm^{-1} mode. Finally, the peak at 473 cm^{-1} is associated with the shell Si-Si mode.

The Si:Ge shell content value, $x = 0.57$ is determined from the relative intensities of the Si-Si, Si-Ge (major peak), and Ge-Ge shell Raman modes in the Raman spectra of individual nanowires for growth A [59, 60]. The intensity is the area integration of the Gaussian-Lorentzian fit of the corresponding Raman mode. For a single spectrum, we can extract the shell Ge content using the relative intensity of the shell Si-Si and Si-Ge Raman modes, or that of the Ge-Ge and Si-Ge Raman modes:

$$\frac{I(Si-Si)}{I(Si-Ge)} = \frac{A_1 x}{2(1-x)} \tag{2.5}$$

$$\frac{I(Ge-Ge)}{I(Si-Ge)} = \frac{A_2(1-x)}{2x} \tag{2.6}$$

where A_1 and A_2 are constants, whose values used are 1.85 and 3.2 respectively [59], x is the Si

mole fraction in the Si_xGe_{1-x} alloy. We repeat the calculation for multiple nanowires and take the average of the results as the extracted composition.

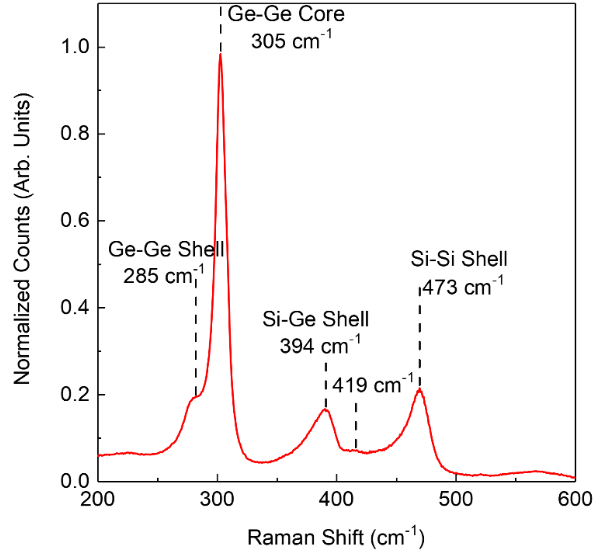

Figure 2.13: Raman spectrum of an individual Ge-Si_xGe_{1-x} core-shell nanowire. The peak position associated with each Raman mode is marked with a vertical dashed line.

We now turn to the Raman signature of the two types of Si-Si_xGe_{1-x} core-shell nanowires. Figure 2.14(a-b) shows the Raman spectrum examples for the two types of Si-Si_xGe_{1-x} core-shell nanowires that are categorized as type I and II in Section 2.4, belonging to growth C. Figure 2.14(a) shows a Raman spectrum revealing two peaks at 515 cm^{-1} and 504 cm^{-1}, which we associate with the Si-Si mode from the core and shell, respectively. The core Si-Si mode is red shifted with respect to the unstrained Si-Si Raman mode of 520.6 cm^{-1}, indicating a tensile strain. Also visible in Fig. 2.14(a) data are the Ge-Ge mode at 292 cm^{-1}, originating from the Si_xGe_{1-x} shell, and two peaks at 409 cm^{-1} and 434 cm^{-1}, associated with the Si-Ge modes of the shell. Figure 2.14(a) inset shows a cross-sectional STEM micrograph of the *same* nanowire the main panel data was acquired from, which reveals the heterostructure is type I, oriented along <110>. Figure 2.14(b) shows a Raman

spectrum similar to Fig. 2.14(a) data, but with a third Si-Si peak at 487 cm^{-1}. Also noteworthy, Fig. 2.14(b) data shows that the core Si-Si mode has a larger red shift by comparison to the unstrained Si-Si Raman mode than Fig. 2.14(a) data. The inset of Fig. 2.14(b) shows a cross-sectional STEM micrograph of the *same* nanowire, revealing a type II heterostructure, oriented along <112>. We have verified the above correlation between absence (presence) of the third Si-Si peak in Raman spectra, with the type I (II) heterostructure via cross-sectional TEM/STEM in multiple nanowire samples. This result is in agreement with previous studies [52, 61] correlating the growth direction and Raman spectra in bare Si nanowires, which show that Si nanowires oriented along the <112> direction can exhibit an additional Si-Si peak associated with hexagonal phases, which we have also experimentally verified [Fig. 2.12(b)]. Hence, we can directly link the terminology of type I and II between our bare Si nanowires and Si-Si_xGe_{1-x} core-shell nanowires, and associate it with the nanowire orientation. Our nanowires do not exhibit kinking, and the Raman spectra collected at different positions along the nanowire are very similar, indicating the crystal structure and growth direction stem from the nucleation phase [40]. Similar to Ge-Si_xGe_{1-x} core-shell nanowires, we can extract the Si shell content, $x = 0.68$, determined using the relative intensities of the shell Si-Si, Si-Ge, and Ge-Ge Raman modes. The shell composition is the same for both <110> and <112> oriented Si-Si_xGe_{1-x} core-shell nanowires.

2.7 Calculate the strain-induced shift of Raman modes using lattice dynamic theory

In the previous section, we show that we can use the red or blue shift of the Raman modes to determine whether the crystal is tensile or compressively strained. In this section, we want to evaluate the connection between strain and the strain-induced shift of the Raman modes quantitatively. The impact of elastic strain on the optical phonon frequencies can be calculated

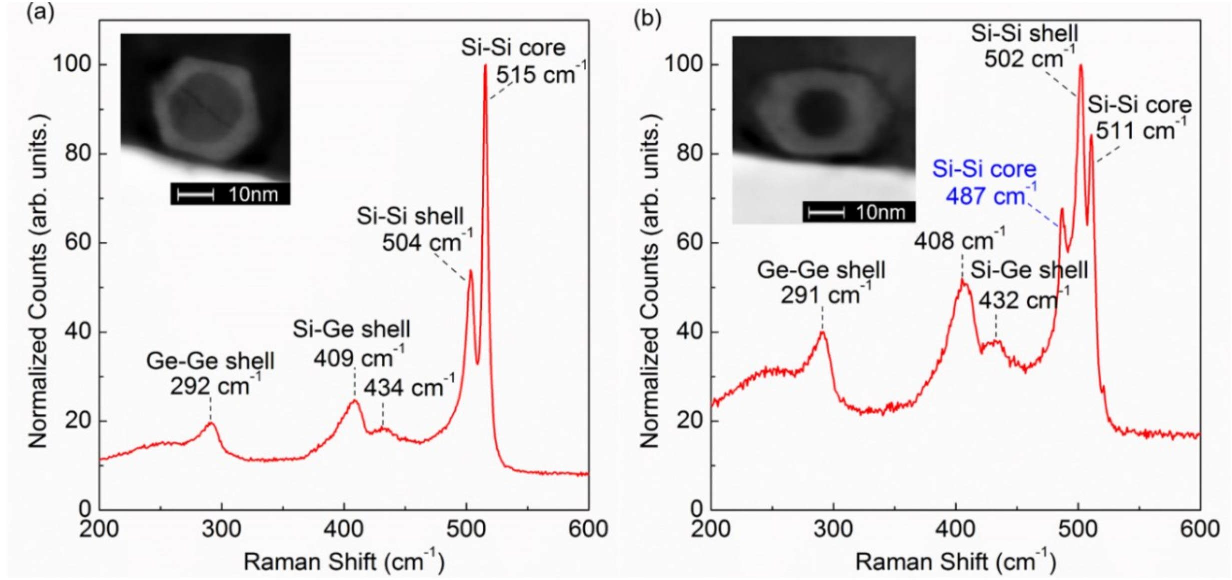

Figure 2.14: Comparison of Raman spectra between <110> and <112> oriented Si-Si_xGe_{1-x} core-shell nanowires. (a) Raman spectrum of a <110> oriented Si-Si_xGe_{1-x} core-shell nanowire with two Si-Si Raman modes. Inset: cross-sectional STEM micrograph of the same nanowire as in the main panel. (b) Raman spectrum of a <112> oriented Si-Si_xGe_{1-x} core-shell nanowire with three Si-Si Raman modes. An additional Si-Si core mode is observed. The thicker shell leads to higher intensity of the Si-Si, Ge-Ge, and Si-Ge shell modes. Inset: cross-sectional STEM micrograph of the same nanowire.

using lattice dynamic theory. Generally, the elastic strain shifts and splits the triply degenerate optical phonon modes at the zone center in a cubic crystal. The strain-induced shift of each optical phonon branch, and the corresponding Raman mode can be calculated by solving the secular equation of lattice dynamic theory [62, 63]:

$$\begin{vmatrix} p\varepsilon_{xx} + q(\varepsilon_{yy} + \varepsilon_{zz}) - \lambda & 2r\varepsilon_{xy} & 2r\varepsilon_{xz} \\ 2r\varepsilon_{xy} & p\varepsilon_{yy} + q(\varepsilon_{xx} + \varepsilon_{zz}) - \lambda & 2r\varepsilon_{yz} \\ 2r\varepsilon_{xz} & 2r\varepsilon_{yz} & p\varepsilon_{zz} + q(\varepsilon_{xx} + \varepsilon_{yy}) - \lambda \end{vmatrix} = 0 \quad (2.7)$$

where ε_{ij} is the strain tensor component and p, q, and r are the material's phonon deformation potential values, given in Table 2.5. The strain tensor components are referenced to the

crystallographic axes $\boldsymbol{u_1} = [100]$, $\boldsymbol{u_2} = [010]$, $\boldsymbol{u_3} = [001]$. The eigenvalue of the secular equation $\lambda_i = \omega_i^2 - \omega_{i0}^2$ describes the strain-induced shift of mode i, where ω_{i0} is the optical phonon frequency without strain. The eigenvector describes the associated phonon wavevector under strain. The intensity of Raman mode i can be computed as follows [44, 64]:

$$I(i) \propto \left| \boldsymbol{E}_{inc}^T \cdot \boldsymbol{R}'(\boldsymbol{i}) \cdot \boldsymbol{E}_{scat} \right|^2 \tag{2.8}$$

where $\boldsymbol{R}'(\boldsymbol{i})$ is the Raman tensor under strain for mode i, expressed in the following equation:

$$\boldsymbol{R}'(\boldsymbol{i}) = \sum_{j=1}^{3} \left(\boldsymbol{u_j} \cdot \boldsymbol{u}_i' \right) \cdot \boldsymbol{R}(\boldsymbol{j}) \tag{2.9}$$

where $\boldsymbol{u}_i'$ is the eigenvector corresponding to eigenvalue λ_i, which is the strained phonon wavevector. $\boldsymbol{R}(\boldsymbol{j})$ is the Raman tensor for unstrained modes using the unstrained crystallographic axes $\boldsymbol{u_1}$, $\boldsymbol{u_2}$ and $\boldsymbol{u_3}$ as phonon wavevectors, in the following forms [65]:

$$\boldsymbol{R}(\boldsymbol{1}) = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 1 \\ 0 & 1 & 0 \end{bmatrix}, \boldsymbol{R}(\boldsymbol{2}) = \begin{bmatrix} 0 & 0 & 1 \\ 0 & 0 & 0 \\ 1 & 0 & 0 \end{bmatrix}, \boldsymbol{R}(\boldsymbol{3}) = \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \tag{2.10}$$

To compare the relative intensity of the calculated Raman modes, the incident ($\boldsymbol{E}_{inc}$) and scattered ($\boldsymbol{E}_{scat}$) light polarizations are assumed parallel to the nanowire axis. This assumption is theoretically justified by an "antenna effect" [66, 67], and experimentally verified with our own measurement setup by observing a $cos^2\theta$ dependence of the scattered beam intensity if the incident light polarization is aligned at an angle θ with respect to the nanowire main axis. As such we will assume $\boldsymbol{E}_{inc}$ || [111] for Ge-Si_xGe_{1-x} core-shell nanowires and $\boldsymbol{E}_{inc}$ || [110] or [112] for Si-Si_xGe_{1-x} core-shell nanowires, while the actual nanowire orientation should be consistent with that

set in the Abaqus strain simulation. We have also experimentally verified $\boldsymbol{E}_{scat}$ to be parallel to $\boldsymbol{E}_{inc}$ by inserting a polarizer before the detector of the scattered light.

Table 2.5: Normalized phonon deformation potentials for Si and Ge:

Material	p/ω_0^2	q/ω_0^2	r/ω_0^2
Si	-1.84 [68]	-2.35 [68]	-0.71 [69]
Ge	-1.66 [68]	-2.19 [68]	-1.11 [70]

Phonon deformation potentials of the Si_xGe_{1-x} alloy are calculated as the linear interpolations between those of Si and Ge.

2.8 Simulation of the strain distribution and calculation of the strain-induced Raman mode shift for core-shell nanowires

We simulate the strain profiles in our core-shell nanowires using the FEM approach described in Section 2.5.2 and calculate the strained-induced Raman mode shift using the procedure detailed in Section 2.7. Figure 2.15 presents the results for Ge-Si_xGe_{1-x} core-shell nanowires of growth A, including the diameter dependence of the calculated and experimentally obtained core Ge-Ge Raman modes [panel (a)], along with two-dimensional contour plots of the strain tensors [panels (b-c)] for a sample nanowire. In Figure 2.15(a) we show the calculated Ge-Ge mode Raman shift as a function of the nanowire diameter (d) for Ge-Si_xGe_{1-x} core-shell nanowire heterostructures with t_{sh} = 4.5 nm, determined from their cross-sectional TEM results. The calculation procedure of the nanowire diameter dependence data of Raman modes is similar for all radial nanowire heterostructures investigated in this thesis, which is detailed as follows. We first build multiple heterostructures with different diameters that can cover the d range in the actual growth, and perform strain simulations for each heterostructure. In each simulation, the output data

provides the strain tensor at each node determined by the FEM meshing strategy. We then calculate the Raman modes under strain and their intensities for each node using Eqs. (2.7) and (2.8), respectively. Figure 2.16(a-f), (g-l) and (m-r) show examples of the three calculated core Raman modes and their associated intensities for <110>, <112> oriented Si-Si_xGe_{1-x} and <111> oriented Ge-Si_xGe_{1-x} core-shell nanowires of growths C and A, respectively. We note throughout this thesis, all contour plots of the nanowire cross-sections that present the Raman data or strain tensors are taken in the middle of the 200 nm long simulation structures, within the region where the simulated strain tensors do not change along the nanowire axis. The coordinates shown in Fig. 2.16(a), (g) and (m) indicate the crystal orientations. Although the solution of the secular equation predicts three non-degenerate core Si-Si or Ge-Ge Raman modes, we find only one Si-Si or Ge-Ge core mode with significant intensity for all three types of core-shell nanowires discussed in this chapter. Consequently, the nodal value of the calculated Raman mode is simply that of the only active mode. In general, the nodal value is the average of all three Raman modes weighted by their intensities. Finally, we compute each data point in the diameter dependence data [the solid line in Fig. 2.15(a)] as the average of all nodal values since the meshing size is uniform.

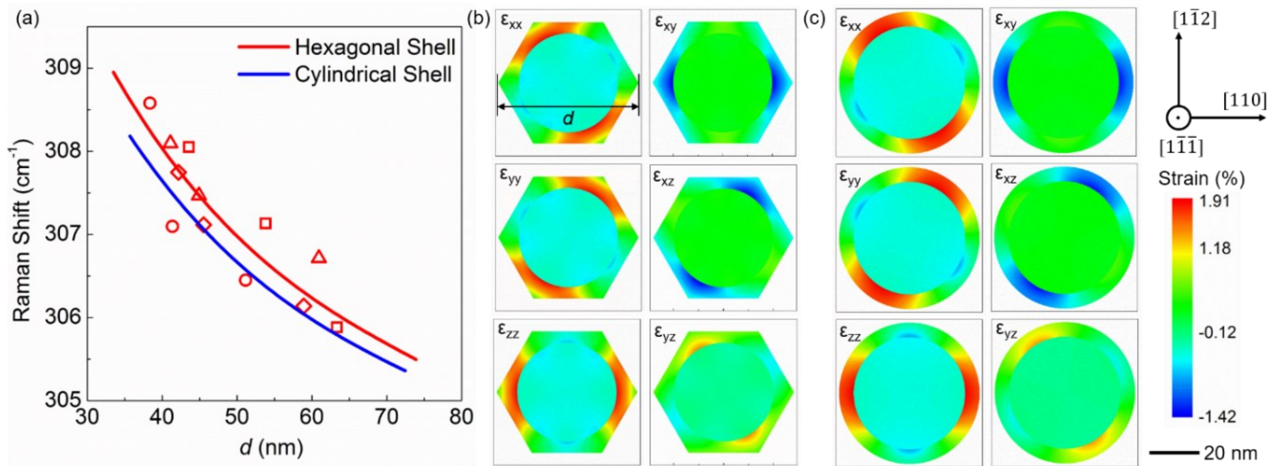

Figure 2.15: Strain distribution and strain-induced Raman mode shift of Ge-Si_xGe_{1-x} core-shell nanowires,

with $x = 0.57$. (a) Diameter dependence of core Ge-Ge Raman modes measured along individual Ge-Si_xGe_{1-x} core-shell nanowires, where the nanowire tapering leads to a diameter change. The different symbols correspond to different nanowires. The red and blue solid lines indicate the calculated core Ge-Ge Raman modes using cylindrical and hexagonal shell cross-sections, respectively. (b) Calculated strain contour plots of Ge-Si_xGe_{1-x} core-shell nanowire with a hexagonal shell. (c) Calculated strain contour plots of Ge-Si_xGe_{1-x} core-shell nanowire with a cylindrical shell. Figure 2.15: continued.

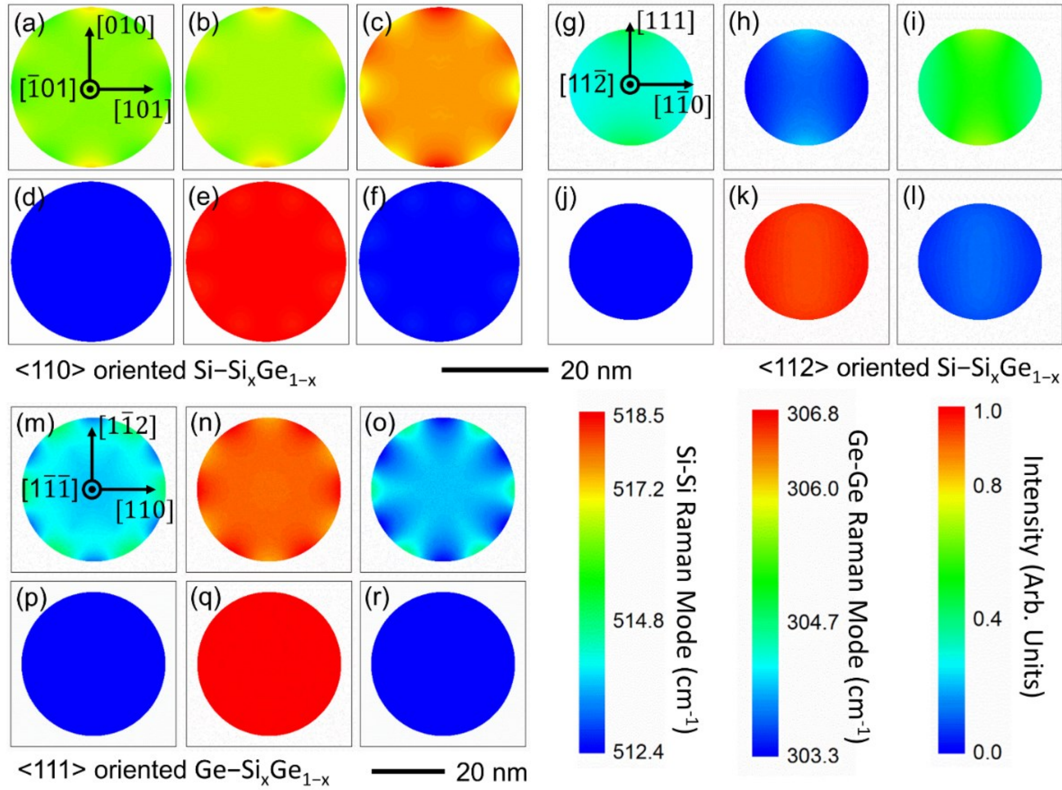

Figure 2.16: Raman modes shift and intensity calculations for the core regions of core-shell nanowires. (a-c) Three Si-Si Raman modes in the core region of a <110> oriented Si-Si_xGe_{1-x} core-shell nanowire and (d-f) the associated intensities. (g-i) Three Si-Si Raman modes in the core region of a <112> oriented Si-Si_xGe_{1-x} core-shell nanowire and (j-l) the associated intensities. (m-o) Three Ge-Ge Raman modes in the core region of a <111> oriented Ge-Si_xGe_{1-x} core-shell nanowires and (p-r) the associated intensities. Only one core Raman mode is active (with non-zero intensity) in each kind of nanowire. The upper scale bar is for panels (a-l), while the lower scale bar is for panels (m-r).

A comparison between the calculated Raman shift for hexagonal and cylindrical cross-sections in Fig. 2.15(a), assuming identical shell areas, shows very similar results within the

experimental error. For both cases, as the ratio of shell over core volume decreases with increasing diameter, the strain in the core and the strain-induced shift of the Ge-Ge Raman core mode are reduced. Altogether, Fig. 2.15 data indicates that while small differences exist between the strain, and corresponding Raman shift for cylindrical and hexagonal shell morphologies, the assumption of a cylindrical shell, perhaps more pedagogical, is also a very good approximation to calculate the strain and the corresponding Raman shift. This cylindrical approximation is particularly convenient if shell facets are not well discernible, like the other types of radial nanowire heterostructures to be discussed in Chapters 3 and 4.

Figure 2.17(a) summarizes the core Si-Si Raman mode shift as a function of diameter acquired from individual Si-Si_xGe_{1-x} core-shell nanowires of growth C, along with the calculations. Using the Fig. 2.14 data, we assign the <110> or <112> growth direction to individual nanowires, if their respective Raman spectrum exhibits two or three Si-Si modes, respectively. For both <110> and <112> oriented nanowires the core Si-Si Raman mode shift increases with diameter, consistent with a larger tensile strain at smaller diameters. Consistent with the Fig. 2.14 data, Fig. 2.17(a) results show a larger shift for the core Si-Si Raman mode in <112> oriented nanowires. Two-dimensional contour plots of the elastic strain in <110> and <112> oriented Si-Si_xGe_{1-x} core-shell nanowires, calculated using finite element simulations are shown in Fig. 2.17(b) and 2.17(c), respectively. The elastic strain tensors are then converted into their corresponding shifted Raman modes and are shown in Fig. 2.17(a) with solid lines. We note that the cubic elastic stiffness, phonon deformation potentials and the nominal unstrained Si-Si Raman mode shift of 520.6 cm^{-1} may be less well-defined in <112> oriented Si-Si_xGe_{1-x} core-shell nanowires due to hexagonal phases [61]. This may account for the wider distribution of the experimentally acquired Si-Si Raman mode values of <112> oriented Si-Si_xGe_{1-x} core-shell nanowires in Fig 2.17(a).

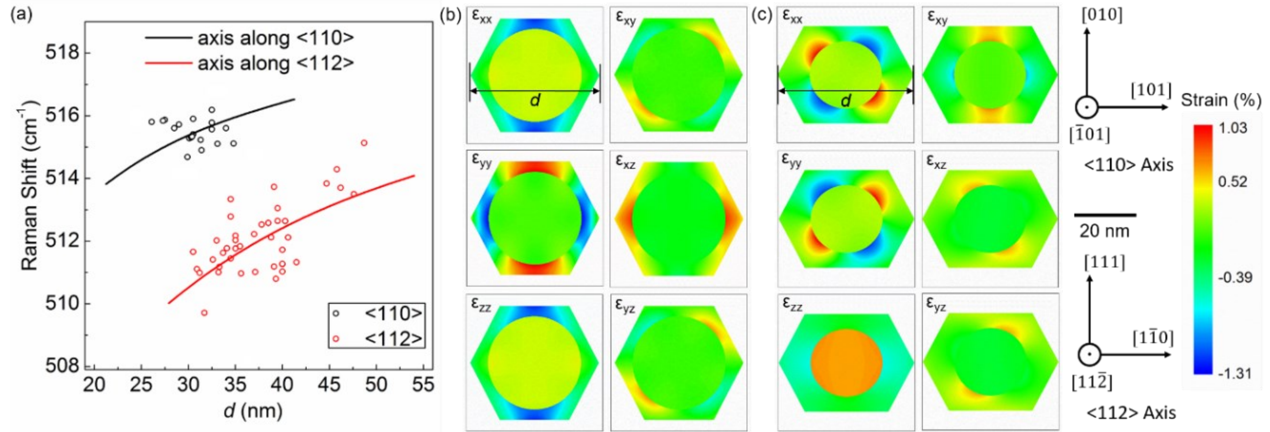

Figure 2.17: Strain distribution and strain-induced Raman mode shift of Si-Si_xGe_{1-x} core-shell nanowire, with $x = 0.68$. (a) Diameter dependence of core Si-Si Raman modes for the two types of Si-Si_xGe_{1-x} core-shell nanowires. The symbols (solid lines) represent experimental data (calculations). (b) Calculated strain in <110> oriented, and (c) <112> oriented Si-Si_xGe_{1-x} core-shell nanowires. The strain profiles are distinct due to the elastic constants' anisotropy.

2.9 Orientation dependent shell growth rate for Si-Si_xGe_{1-x} core-shell nanowires

Lastly, we address an interesting experimental observation, namely that the shell CVD growth results in different shell thickness values, depending on the nanowire growth axis. Indeed, an examination of growths B - D shows that nanowires oriented along the <112> axis consistently have a larger shell thickness compared to nanowires from the *same* growth, which are oriented along the <110> axis. This is noteworthy because it implies that the same family of planes, i.e. {111} possess different growth rates depending on the nanowire growth axis during the *same* growth under identical growth conditions. Furthermore, the difference in the shell thickness becomes more pronounced as the shell CVD growth temperature increases, which suggests a higher activation energy for the shell growth of <112> nanowires. An example is provided in Fig. 2.18(a-f), which shows HRTEM, FFT and STEM data for both <110> and <112> oriented Si-Si_xGe_{1-x} nanowires of growth D. The difference in the shell thickness is noticeably larger than that

in Fig. 2.8 (growth B). The different shell growth rates are presumably due to different surface hydrogen desorption rates, and suggest that hexagonal phases present in <112> oriented nanowires change the surface energies to stabilize facets along {113} planes and also affect the hydrogen desorption rates [71]. Based on previous discussions in this chapter, a possible explanation for the appearance of the seemingly energetically unfavorable shell morphology of <112> Si-Si_xGe_{1-x} core-shell nanowire could be that the hexagonal phases reduce the surface energy of {113} planes to favor them as shell facets. Previous experimental [72], and theoretical [73] studies have also suggested that self-interstitials in {113} stacking faults lead to a reduction of the Si {113} surface energy, and to the presence of hexagonal phases [74, 75]. This may explain the unusual shell faceting of <112> oriented nanowires, at variance to a rectangular cross-section terminated by {111} and {110} planes expected based on energetic considerations [76, 77].

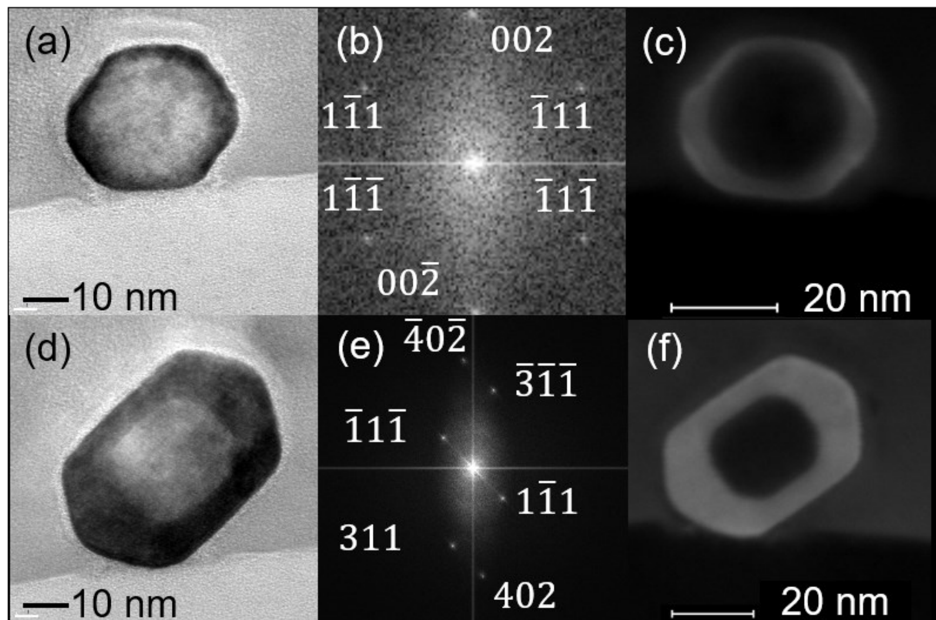

Figure 2.18: Shell thickness difference between <110> and <112> oriented Si-Si_xGe_{1-x} core-shell nanowires are exaggerated at higher shell growth temperatures. (a-c) and (d-f) are cross-sectional HRTEM, FFT and STEM images for <110> and <112> oriented Si-Si_xGe_{1-x} nanowires (growth D), respectively.

We also perform a Si-Si_xGe_{1-x} core-shell nanowire growth (growth E in Table 2.2) with a much thinner shell of ~2 nm at a reduced shell growth temperature of 370 °C, with other growth conditions similar to growths B and C. Figure 2.19 shows the cross-sectional TEM image of one <110> oriented nanowire obtained in this growth, the inset is the corresponding STEM micrograph. The data shows that the Si_xGe_{1-x} shell still covers the whole perimeter of the Si core and appears to be hexagonal, indicating the absence of island growth mode during the shell growth and that the shell morphology is determined in the nucleation phase at the very beginning of the CVD growth.

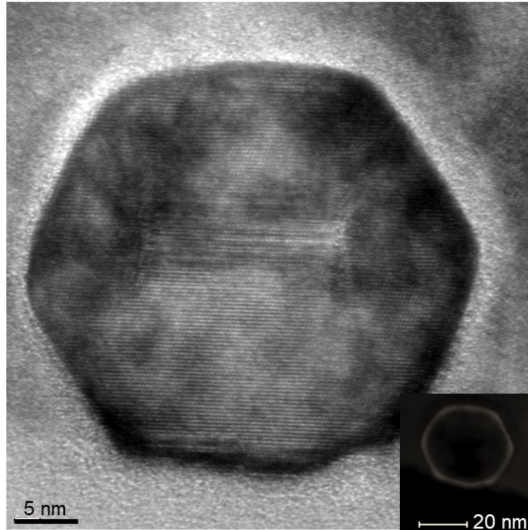

Figure 2.19: Cross-sectional TEM image of a Si-Si_xGe_{1-x} core-shell nanowire with a very thin Si_xGe_{1-x} shell. The shell shape is still hexagonal and covers the complete perimeter of the core. Inset is the corresponding STEM image.

2.10 Summary

In this chapter, we use Ge-Si_xGe_{1-x} and Si-Si_xGe_{1-x} core-shell nanowires as examples to discuss the structural analysis techniques applicable to all radial nanowire heterostructures investigated in this thesis. We discuss the growth, SEM/TEM imaging, FEM strain simulation,

experimental acquisition and calculation of Raman modes of Ge-Si_xGe_{1-x} and Si-Si_xGe_{1-x} core-shell nanowires. We demonstrate that the shell morphology and Raman spectra of the epitaxial Ge-Si_xGe_{1-x} and Si-Si_xGe_{1-x} core-shell nanowires are closely correlated. Cross-sectional TEM imaging reveals two distinct hexagonal shell morphologies for Si-Si_xGe_{1-x} nanowires that depend on the growth direction. Specifically, Si-Si_xGe_{1-x} nanowires growing along the <110> crystal axis are terminated by two {100}, and four {111} planes, while nanowires growing along the <112> crystal axis are terminated by two {111}, and four {113} planes. Remarkably, micro-Raman spectroscopy and cross-sectional TEM imaging performed on the same Si-Si_xGe_{1-x} core-shell nanowire reveal a direct correlation between the Raman spectrum and shell morphology. Therefore, both techniques are key ingredients to accurately probe the strain in the radial nanowire heterostructure. The combination of the cross-sectional TEM imaging to determine the shell morphology and Raman spectroscopy to assess the Si_xGe_{1-x} shell alloy composition allows us to build an accurate simulation structure for strain calculations, and then apply lattice dynamic theory to convert the calculated strain to Raman modes. The good agreement between the calculated and experimental Raman modes suggests the core-shell nanowire is coherently strained.

Chapter 3 : Enhanced Electron Mobility in Non-Planar Tensile Strained Si Epitaxially Grown on Si_xGe_{1-x} Nanowires[2]

3.1 Introduction

We report the growth and characterization of epitaxial, coherently strained Si_xGe_{1-x}-Si core-shell nanowire heterostructure through VLS growth mechanism for the Si_xGe_{1-x} core, followed by an *in-situ* ultra-high-vacuum CVD growth for the Si shell. Raman spectra acquired from individual nanowires reveal the Si-Si, Si-Ge and Ge-Ge modes of the Si_xGe_{1-x} core, and the Si-Si mode of the shell. Due to the compressive (tensile) strain induced by lattice mismatch, the core (shell) Raman modes are blue (red) shifted compared to those of unstrained bare Si_xGe_{1-x} (Si) nanowires, in good agreement with values calculated using continuum elasticity model coupled with lattice dynamic theory. A large tensile strain of up to 2.3% is achieved in the Si shell, which is expected to provide quantum confinement for electrons due to a positive core-to-shell conduction band offset. We demonstrate *n*-type MOSFETs using Si_xGe_{1-x}-Si core-shell nanowires as channel, and observe a 40% enhancement of the average electron mobility compared to control devices using Si nanowires, due to an increased electron mobility in the tensile-strained Si shell.

Quantum confinement of carriers in a high-mobility region benefits the transport property. Hole confinement in the Ge cores has been realized in Ge-Si and Ge-Si_xGe_{1-x} core-shell nanowires [79, 80], due to a large valence band offset between Ge and Si. Electron confinement in group IV

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[2] Part of this chapter was published previously: [78] F. Wen and E. Tutuc, "Enhanced Electron Mobility in Nonplanar Tensile Strained Si Epitaxially Grown on Si_xGe_{1-x} Nanowires," *Nano Lett,* vol. 18, pp. 94-100, 2018.

F. Wen performed the nanowire growths, TEM, Raman measurements, simulations, calculations, MOSFET fabrications and electrical characterizations. F. Wen and E. Tutuc analyzed the data and co-wrote the manuscript. Both authors have contributed to and approved the final version of the manuscript.

core-shell heterostructures is, however, more challenging to achieve due to smaller conduction band offset between Si and Ge. Furthermore, the relative position of the conduction band edge depends on the strain in a Si-Ge system [81, 82]. In epitaxial, coherently strained core-shell nanowire heterostructures the lattice mismatch-induced elastic strain changes both the band structure and the band alignment between the core and shell. Previous studies have reported electron confinement in coherently tensile-strained Si layers on relaxed [83, 84] and compressive-strained [85] Si_xGe_{1-x} planar substrates. Moreover, those heterostructures also show enhanced electron mobility with respect to unstrained Si, due to a reduced electron effective mass in the transport direction, and a reduction of intervalley phonon scattering [86]. Various techniques have been adopted to induce tensile strain in non-planar Si MOSFETs, including nano-patterning of strained Si on insulating substrates [87, 88], the use of SiC as source/drain and/or SiN liner [89], strain response due to gate electrode [90] or oxide [91], and the use of strain-relaxed Si_xGe_{1-x} buffer as virtual substrate [92]. The one-dimensional counterpart of strained Si on Si_xGe_{1-x}, namely coherently strained Si_xGe_{1-x}-Si core-shell nanowires represent a promising platform for high mobility *n*-type MOSFETs, because they combine quantum confinement and enhanced electron mobility in the strained Si shell, with the enhanced electrostatic control of the Ω-gate or GAA geometry.

The chapter is organized as follows. In Section 3.2, we discuss the planar counterpart of Si_xGe_{1-x}-Si core-shell nanowires that inspires this study. Section 3.3 presents the growth and SEM/TEM imaging of the Si_xGe_{1-x}-Si core-shell nanowire. Section 3.4 shows the Raman spectra acquired from individual nanowires, and the calculation results of strain tensors presented in the form of two-dimensional contour plots. Section 3.5 presents the diameter dependence data of the calculated core and shell Si-Si Raman modes under strain in Si_xGe_{1-x}-Si core-shell nanowires. In

Section 3.6, we demonstrate the electron transport properties of Si_xGe_{1-x}-Si core-shell nanowires by fabricating *n*-type MOSFETs using these nanowires as channel. Section 3.7 shows the fabrication process flow of nanowire MOSFETs. Section 3.8 presents the approach to calculate the gate capacitance of nanowire MOSFETs. The contents in Sections 3.7 and 3.8 are applicable to the nanowires discussed in this chapter as well as those in Chapter 4. Section 3.9 summarizes the chapter.

3.2 Performance enhancement in tensile strained-Si *n*-type MOSFETs

We first introduce the planar strained Si *n*-type MOSFETs grown on a relaxed Si_xGe_{1-x} virtual substrate. Figure 3.1(a) shows the schematic of the cross-section of a planar strained Si *n*-type MOSFET. The fabrication process of this planar device starts with a Si(100) substrate, followed by a SiGe graded buffer and then a relaxed Si_xGe_{1-x} virtual substrate, and is finally terminated by a Si layer coherently strained to the virtual substrate. As mentioned in the earlier section, bulk Si with biaxial tensile strain should exhibit a higher mobility than bulk unstrained Si. The tensile strain splits the Si conduction band of six-fold degeneracy into two groups, a two-fold and a four-fold degenerate bands, as illustrated in the band diagram next to the device schematic in Fig. 3.1(a). Since the two-fold degenerate band has lower energy, electrons will preferentially populate this band. Consequently, the mobility enhancement in tensile strained Si reflects the reduction in intervalley scattering, as well as a reduced in-plane effective mass in the conduction band. Figure 3.1(b) presents the room temperature effective mobility μ_{eff} against the vertical effective electric field E_{eff} for the strained Si devices with various Ge fraction in the virtual substrate. The roll-off of μ_{eff} is due to Coulomb scattering at the low field and interface scattering at the high field. The similar shape of these curves indicates that the contributions from the

Coulomb and interface scattering are comparable for the strained and unstrained bulk Si devices. It is found that the mobility enhancement increases with a larger tensile strain in Si, thanks to a higher Ge content in the virtual substrate until a Ge fraction of 30%. A higher Ge content results in a low material quality and poor surface morphology to reduce μ_{eff}, due to the strain induced dislocations in the Si layer.

The Si_xGe_{1-x}-Si core-shell nanowire is the one-dimensional equivalent to this planar heterostructure. However, it does not require such a complicated multi-player heterostructure to avoid defects due to lattice mismatch. In a core-shell nanowire, the shell is not fully compliant to the core/non-planar substrate and therefore the lattice mismatch can be accommodated by both core and shell, resulting in a much thicker critical thickness [93]. Hence, strained Si can be grown directly on the Si_xGe_{1-x} nanowire core without strain-induced defects and allows a GAA geometry for the best immunity to short channel effects.

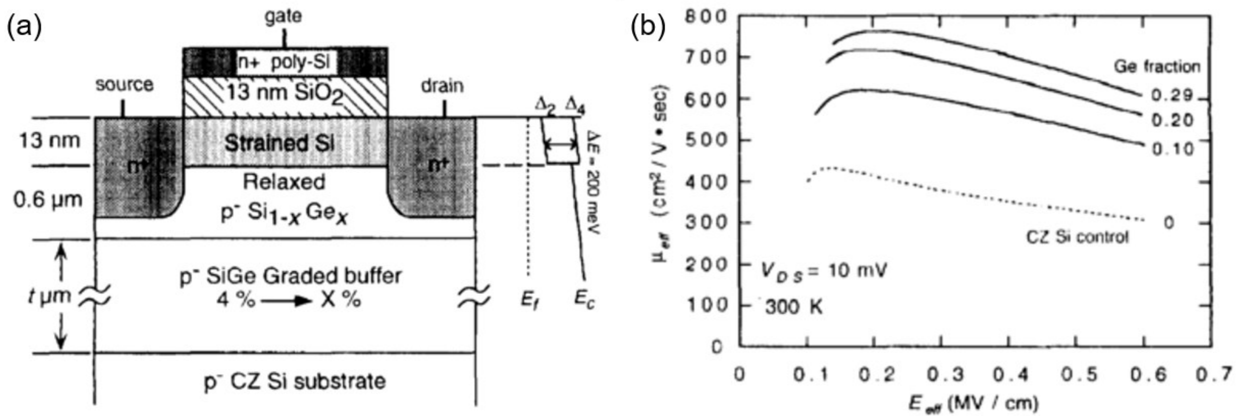

Figure 3.1: (a) Schematic of a strained Si n-type MOSFET. The band diagram is for a Ge composition of 29% in the relaxed substrate. (b) Electron μ_{eff} vs. E_{eff} for long-channel MOSFETs with different Ge fraction in the virtual substrate. (Figure adapted from Ref. [86])

3.3 Growth, SEM and TEM imaging of Si_xGe_{1-x}-Si core-shell nanowires

Figure 3.2 depicts the growth of our Si_xGe_{1-x}-Si core-shell nanowires, consisting of a sequence of VLS Si_xGe_{1-x} core growth, followed by an *in-situ* Si shell growth using ultra-high-vacuum CVD. The growth corresponds to NW228 in our nanowire growth catalog. We start with a Si(111) wafer, using diluted HF to remove the native oxide and then evaporating an 8 Å thick Au film. The substrate is then transferred to a cold wall ultra-high-vacuum CVD growth chamber, annealed in a H_2 ambient at 370 °C for 15 min, which leads to the formation of Au nanoparticles as catalysts for the VLS growth. The Si_xGe_{1-x} nanowire cores are grown at a temperature of 305 °C and pressure of 10 Torr using a combination of SiH_4 (100%, 100 sccm) and GeH_4 (20% diluted in He, 20 sccm) as precursors. Therefore, the precursor partial pressure ratio of SiH_4 over GeH_4 during the core VLS growth is 25:1. The epitaxial Si shell growth is then performed *in-situ* at a temperature of 460 °C, pressure of 40 mTorr, using SiH_4 as gas source (60 sccm). Figure 3.3 presents the SEM image of the cross-section for a part of the Si_xGe_{1-x}-Si core-shell nanowire growth substrate. Similar to the Si core growth of the Si-Si_xGe_{1-x} core-shell nanowire discussed in Chapter 2, the VLS growth of the Si_xGe_{1-x} core does not show an epitaxial pattern from the substrate. While the shell growth will result in additional VLS growth, based on the SEM data in Fig. 3.3, we find that the axial growth during the Si shell growth stage is less than 100 nm for a 10 μm long nanowire, because of the lower precursor partial pressure. We also grow bare Si_xGe_{1-x} nanowires (NW227 in the growth catalog) using the same VLS growth recipe as the Si_xGe_{1-x} core of Si_xGe_{1-x}-Si core-shell nanowires, as well as Si nanowires (NW214 in the growth catalog) at a temperature of 410 °C and pressure of 10 Torr using SiH_4 as precursor. Bare Si_xGe_{1-x} and Si nanowires serve as baselines to extract the unstrained optical phonon frequencies in the core and shell, respectively, while bare Si nanowires are also used to fabricate *n*-type MOSFET control

devices. Recalling the discussions in Section 2.2 on controlling the nanowire growth direction, we have optimized the VLS growth recipes aiming to produce <110> oriented nanowires exclusively for the study in this chapter. Table 3.1 summarizes the detailed growth conditions of the three nanowire growths discussed in this chapter.

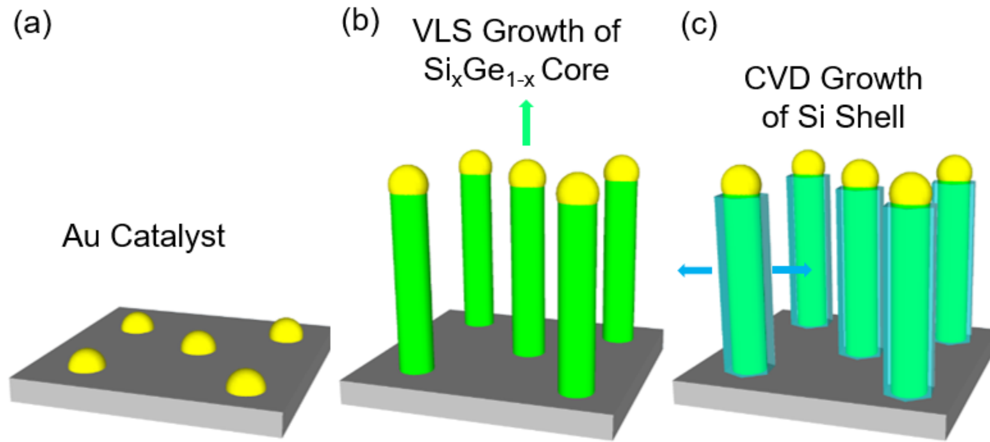

Figure 3.2: Schematic of the Si_xGe_{1-x}-Si core-shell nanowire growth, showing (a) Au catalyst nanoparticles, (b) the Si_xGe_{1-x} core growth by VLS, and (c) the Si shell growth by CVD. Arrows indicate the growth direction in the corresponding regime.

Figure 3.3: SEM image of Si_xGe_{1-x}-Si core-shell nanowires.

Table 3.1: Growth conditions of the nanowires discussed in Chapter 3

Growth type and name	GeH_4/SiH_4 flow during core growth (s.c.c.m.) and chamber pressure (Torr)	Core growth temperature (°C)	Core growth time (min)	GeH_4/SiH_4 flow during shell growth (s.c.c.m.) and chamber pressure (Torr)	Shell growth temperature (°C)	Shell growth time (min)
Si_xGe_{1-x}-Si (NW228)	20/100, 10	305	30	0/60, 40m	460	90
Si_xGe_{1-x} (NW227)	20/100, 10	305	30	N/A	N/A	N/A
Si (NW214)	0/100, 10	410	18	N/A	N/A	N/A

We employ TEM to study the morphology and crystal structure of the Si_xGe_{1-x}-Si core-shell nanowires. Figure 3.4(a) shows the planar view TEM image of an individual Si_xGe_{1-x}-Si core-shell nanowire that illustrates a single crystal nanowire heterostructure with shell grown epitaxially on core, where the sidewall demonstrates no obvious saw-tooth facets [47, 94] or strain-induced surface roughening [43, 95]. The FFT of panel (a) data shown in the inset reveals the growth direction is indeed along <110>. The <110> growth direction holds in the entire 20 - 40 nm diameter range of the Si_xGe_{1-x}-Si core-shell nanowires we have produced. We note it is also the case for bare Si and Si_xGe_{1-x} nanowires. Figure 3.4(b) shows the cross-sectional TEM image of a Si_xGe_{1-x}-Si core-shell nanowire. Facets for the core and shell are not well discernible, except for {100} planes of the shell. We measure the Si shell thickness as $t_{sh} = 4.2$ nm, corresponding to a CVD growth rate of 0.47 Å/min.

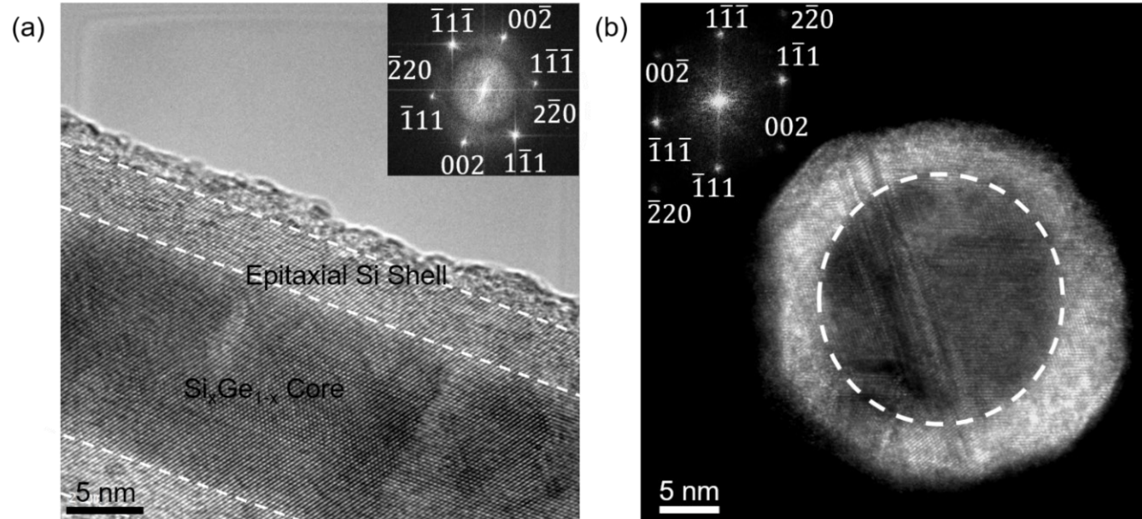

Figure 3.4: (a) Planar view TEM image of a <110> oriented Si_xGe_{1-x}-Si core-shell nanowire, where interfaces are marked for clarity. Inset: FFT of the main panel data. (b) Cross-sectional transmission electron micrograph of a <110> oriented Si_xGe_{1-x}-Si core-shell nanowire. The core-shell interface is marked for clarity. Inset: FFT of the main panel data. The zone axis is assumed along [110] direction.

3.4 Raman spectra and strain calculation of Si_xGe_{1-x}-Si core-shell nanowires

Similar to the Ge-Si_xGe_{1-x} and Si-Si_xGe_{1-x} core-shell nanowires investigated in Chapter 2, one main attribute of such lattice-mismatched Si_xGe_{1-x}-Si core-shell nanowire heterostructure is the associated elastic strain. The tensile strain in the Si shell induces a conduction band energy splitting associated with the crystal asymmetry, resulting in reduced electron effective mass and enhanced electron mobility. The strain will also shift the optical phonon frequencies, and therefore change the Raman spectrum of the heterostructure. We use Raman spectroscopy on individual Si_xGe_{1-x}-Si core-shell nanowire to probe the shifted optical phonon frequencies using the approach detailed in Section 2.6.3. Figure 3.5 shows the Raman spectra of a 28 nm diameter Si_xGe_{1-x}-Si core-shell nanowire [panel (a)], a 40 nm diameter Si_xGe_{1-x}-Si core-shell nanowire [panel (b)], a bare Si_xGe_{1-x} nanowire [panel (c)] and a bare Si nanowire [panel (d)]. The Raman spectrum of the

Si nanowire reveals a single peak at 520.6 cm^{-1}, associated with the Si-Si Raman mode, while that of the Si_xGe_{1-x} nanowire reveals three major peaks at 295, 407 and 478 cm^{-1}, associated with the Ge-Ge, Si-Ge and Si-Si Raman modes, respectively. Compared to the Si_xGe_{1-x} nanowire, Raman spectra of the Si_xGe_{1-x}-Si core-shell nanowires show one additional peak near 510 cm^{-1}, associated with the shell Si-Si mode. Furthermore, the three Raman modes of the Si_xGe_{1-x} core of Si_xGe_{1-x}-Si core-shell nanowires are blue-shifted compared to those of bare Si_xGe_{1-x} nanowire, because of the compressive strain induced by the epitaxial Si shell. Conversely, the shell Si-Si Raman modes in the same Si_xGe_{1-x}-Si core-shell nanowires are red-shifted with respect to the unstrained Si-Si mode, indicating a tensile strain. A comparison of the Fig. 3.5(a) and 3.5(b) data shows that the three core Raman modes of the 28 nm diameter Si_xGe_{1-x}-Si core-shell nanowire have larger blue shifts, while the shell Si-Si mode has a smaller red shift, compared to those of the 40 nm diameter one. This finding can be explained by an increasing compressive strain in the core, and a decreasing tensile strain in the shell with reducing the nanowire diameter at a constant t_{sh}. The average Si:Ge core content value, $x = 0.41$ is determined from the relative intensities among the Si-Si, Si-Ge, and Ge-Ge core Raman modes using the method detailed in Section 2.6.4 [59, 60]. This composition is in good agreement with the value measured from bare Si_xGe_{1-x} nanowires using energy-dispersive X-ray spectroscopy with STEM. We find the composition depends weakly on diameter, and varies by less than 3% in the diameter range probed here [96].

To better understand the dependence of Raman modes on elastic strain and further substantiate the coherently strained nature of our Si_xGe_{1-x}-Si core-shell nanowire heterostructures, we calculate the strain and the strain-induced shift of Si-Si Raman modes in both core and shell regions as a function of diameter, and compare it with the experimental data. We calculate the elastic strain using FEM as described in Section 2.5.2, which takes into account the crystal elastic

anisotropy. For simplicity, we assume all Si_xGe_{1-x}-Si core-shell nanowires have cylindrical cross-sections. The validity for the use of such a cylindrical geometry has been justified in Section 2.8. Figure 3.5 also presents the simulated two-dimensional contour plots of the strain tensor [panel (e-h)], along with the hydrostatic strain $\varepsilon_h = (\varepsilon_{xx} + \varepsilon_{yy} + \varepsilon_{zz})/3$ [panel (i)] and the corresponding conduction band energy (E_C) calculated under strain [97, 98] for a $Si_{0.41}Ge_{0.59}$-Si core-shell nanowire [panel (j)]. The nanowire growth, and cross-section axes are different as indicated in panel (e). We find the distribution of individual strain tensor component in the core is uniform compared to that in the shell [99], while ε_h is uniform in both regions. The average ε_h values, closely related to the volume change [100], is -0.65% in the core and 0.56% in the shell in this example. We note the ε_h magnitude is large compared to values reported in strained Si n-type FinFETs [101].

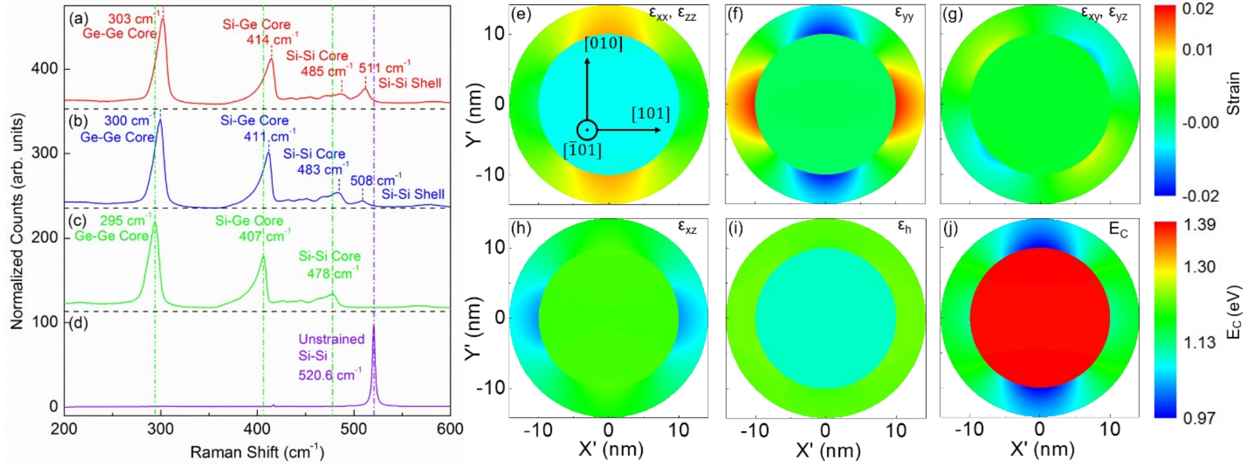

Figure 3.5: Comparison of Raman spectra acquired from an individual (a) 28 nm diameter $Si_{0.41}Ge_{0.59}$-Si core-shell nanowire, (b) 40 nm diameter $Si_{0.41}Ge_{0.59}$-Si core-shell nanowire, (c) $Si_{0.41}Ge_{0.59}$ nanowire, and (d) Si nanowire. The Si-Si in bulk Si, and Ge-Ge, Si-Ge, and Si-Si in bulk $Si_{0.41}Ge_{0.59}$ Raman modes are marked with vertical dash-dotted lines. Two-dimensional contour plots of the simulated (e-h) strain tensor components, (i) ε_h and (j) calculated E_C for a $Si_{0.41}Ge_{0.59}$-Si core-shell nanowire, with t_{sh} = 4.2 nm. The crystal directions are indicated in panel (e).

Next, we discuss the approach to calculate E_C of the $Si_{0.41}Ge_{0.59}$ core and Si shell in a $Si_{0.41}Ge_{0.59}$-Si core-shell nanowire. Unstrained Si and Ge have different conduction band structures. The principal conduction band minima of Si are located along the six equivalent [100] directions at a distance of ~85% from the Γ-point to the X-points in the Brillouin zone, namely the Δ-points, thus having a six-fold degenerate conduction band valley. Using the symbol Δ to denote the position in the Brillouin zone in Chapters 3 and 4 is not to be confused with using Δ to denote the superconductor gap energy in Chapters 5 and 6. On the other hand, the conduction band minima of Ge are located along the eight equivalent [111] directions at the L-points, having a four-fold degenerate conduction band valley since each L-point is shared by two adjacent Brillouin zones. Valley splitting may occur in both materials under strain, depending on the symmetry of the strain tensor in relation to that of the band minima. For example, a uniaxial tensile strain along the [001] direction will split the six-fold degenerate Δ valleys into two groups, a two-fold degenerate valley Δ_2 along the [001] direction and a four-fold degenerate valley Δ_4 along the [100] and [010] directions. We use $k \cdot p$ method that allows us to calculate the strain-induced shift for each of the six Δ and eight L valleys in both the $Si_{0.41}Ge_{0.59}$ core and Si shell regions. The energy shift of conduction band valley i due to strain (ΔE_C^i) relative to unstrained E_C writes [97]:

$$\Delta E_C^i = \Xi_d^i \cdot Tr(\boldsymbol{\varepsilon}) + \Xi_u^i \cdot \left(\boldsymbol{a}_i^T \boldsymbol{\varepsilon} \boldsymbol{a}_i\right) \quad (3.1)$$

where $\boldsymbol{\varepsilon}$ is the strain tensor, $Tr(\boldsymbol{\varepsilon})$ is the trace of the strain tensor, $\boldsymbol{a}_i$ is the normalized column vector parallel to the direction of conduction band valley i, e.g. [100] or $\frac{1}{\sqrt{3}}[111]$, Ξ_d^i and Ξ_u^i are the dilation and uniaxial deformation potentials of the conduction band, respectively. Table 3.2 summarizes the Ξ_d^i and Ξ_u^i values of Si and Ge used in the calculations of this chapter. Unstrained E_C values, either at the Δ or L valleys, are extracted by assuming the Si $2p_{3/2}$ core-level energy

being the same in both the core and shell regions [102]. The Si $2p_{3/2}$ core-level energy also serves as the reference energy, i.e. 0 eV. For $Si_{0.41}Ge_{0.59}$ and Si the Δ valley has a much lower energy compared to the L valley, and we use the unstrained E_C values of 1.434 and 1.149 eV for Δ valley energies in the core and shell regions, respectively [102]. We then apply Eq. (3.1) to calculate ΔE_C^i for each of the six equivalent [100] directions using the simulated strain tensor at each meshing node for both the core and shell regions, and assign the minimum of the six values as the nodal E_C value under strain. We calculate a core-to-shell conduction band offset of 270 meV in the example presented in Fig. 3.5 based on the mean values of the calculated conduction band energies in both regions, indicating an electron confinement in the Si shell. This offset ranges from 265 to 280 meV for the nanowire with a diameter from 25 to 40 nm.

Table 3.2: Deformation potentials for Δ and L valleys of Si and Ge used in Chapter 3 [98]

Material	Ξ_d^{Δ} (eV)	Ξ_u^{Δ} (eV)	Ξ_d^{L} (eV)	Ξ_u^{L} (eV)
Si	-3.09	8.47	-9.02	12.4
Ge	-2.54	7.46	-6.90	11.1

Conduction band deformation potentials of Si_xGe_{1-x} alloy are calculated as the linear interpolation between those of Si and Ge.

3.5 Diameter dependence of the strain and Si-Si Raman modes in Si_xGe_{1-x}-Si core-shell nanowires

Next, we evaluate the impact of elastic strain on the optical phonon frequencies using lattice dynamic theory, following the same approach described in Section 2.7. Figure 3.6(a) summarizes the diameter dependence of the calculated (solid lines), and experimentally acquired (symbols) Si-Si Raman modes for $Si_{0.41}Ge_{0.59}$-Si core-shell nanowires. The unstrained Si-Si

Raman modes of core and shell are marked with red and black dashed lines, at 478 cm^{-1} and 520.6 cm^{-1}, respectively. The experimental data and calculations are in very good agreement, and the diameter dependence is explained by an increasing elastic strain in the core at reduced nanowire diameters, and a larger strain-induced shift of the Raman mode. Figure 3.6(b-d) show the two-dimensional contour plots of the calculated Si-Si Raman mode shift, and Fig. 3.6(e-g) show the associated intensities in both core and shell regions. The three-fold degeneracy of the Si-Si Raman mode in either core or shell can be lifted by the elastic strain, with values for individual modes determined by the eigenvalues of the secular equation of lattice dynamic theory [Eq. (2.7)]. The intensity of each Raman mode is also calculated to identify the active modes using Eq. (2.8). In the $Si_{0.41}Ge_{0.59}$ core, we find only one active Si-Si Raman mode, labelled mode 1. On the other hand, two modes in the Si shell, labelled 1 and 2 have comparable intensity, while a third mode 3 has a weaker intensity. Experimentally only one peak associated with the Si shell can be resolved in the Raman spectra, albeit with a larger full width at half-maximum (FWHM) of 11 - 14 cm^{-1}, compared to 4 cm^{-1} measured in bare Si nanowires [Fig. 3.5(a-d)]. Consequently, in Fig. 3.6(a) we include the calculated values for the three shell Si-Si Raman mode along with the position of the weighted average using the calculated relative intensities [103]. The calculated individual shell Si-Si Raman modes are presented in a corridor of values to indicate the variation across the shell. The total broadening of the shell Si-Si Raman mode ranges from 12.5 to 13.6 cm^{-1} according to Fig. 3.6(a), explaining the increased FWHM observed experimentally. Overall, we find the experimental data agrees well with the calculated Si-Si Raman modes in both core and shell regions, consistent with a coherently strained heterostructure. We also find that the normal strain (diagonal terms in the strain tensor) shifts the shell Si-Si Raman mode from the unstrained value at 520.6 cm^{-1} [104], while the shear strain (off-diagonal terms in the strain tensor) only lifts the

three-fold degeneracy but does not change the weighted average. Therefore, based on the linear deformation potential model applied in this thesis, the calculated shell Si-Si Raman mode shift from 520.6 cm^{-1} is linearly proportional to ε_h. To help visualize the relation between strain and the Si-Si Raman mode shift in the Si shell, the right *y*-axis in Fig. 3.6(a) shows ε_h mapped from the Raman shift (left *y*-axis).

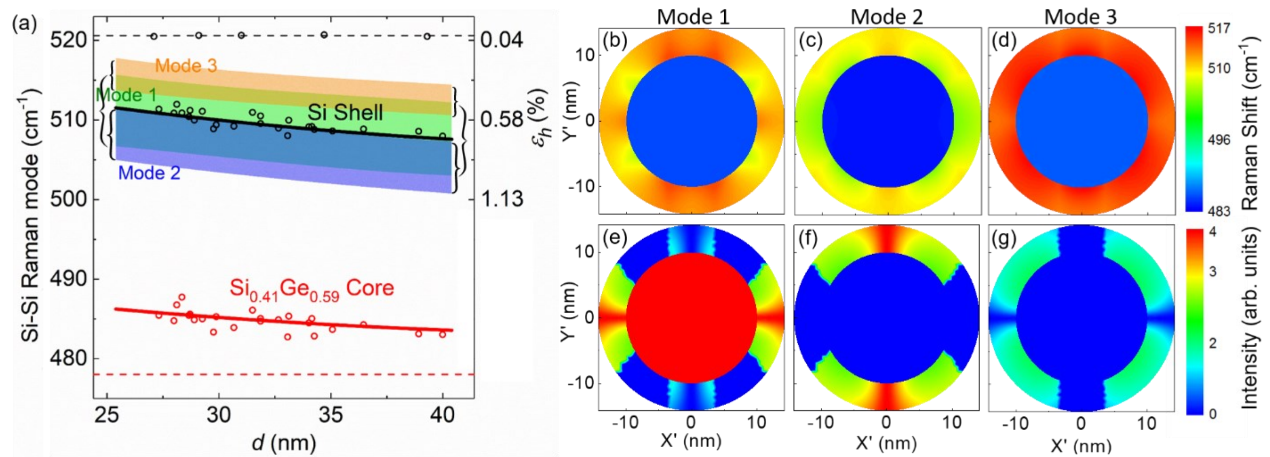

Figure 3.6: (a) Diameter dependence of the core and shell Si-Si Raman modes for $Si_{0.41}Ge_{0.59}$-Si core-shell nanowires. The Si-Si Raman modes for core and shell are shown in black and red, respectively. Symbols represent experimental data, and solid lines represent calculations. The black and red dashed lines mark the position of the unstrained Si-Si Raman modes in shell and core, respectively. Experimental data of Si-Si Raman modes acquired from bare Si nanowire are included for comparison. The calculation results of three different shell Si-Si modes are presented with three corridors to indicate their variations across the shell. Calculated (b-d) Si-Si modes Raman shift, and (e-g) the corresponding intensities for a coherently-strained $Si_{0.41}Ge_{0.59}$-Si core-shell nanowire, assuming the incident and scattered light are parallel to the <110> nanowire growth axis.

3.6 Electron transport in $Si_{0.41}Ge_{0.59}$-Si core-shell nanowires

Next, we turn to the electron transport in <110> oriented $Si_{0.41}Ge_{0.59}$-Si core-shell nanowires using Ω-gated *n*-type MOSFETs with highly doped source and drain. The fabrication

process will be detailed in Section 3.7. Figures 3.7(a-b) show the SEM images of a $Si_{0.41}Ge_{0.59}$-Si core-shell and a bare Si nanowire n-type MOSFET, respectively. The devices have a same L_G of 840 nm and d of 28 and 25 nm, respectively. To realize Ohmic contact between metal contacts and the nanowires, we perform a low energy ion implantation of phosphorous into source and drain regions using gates as self-aligned masks. This approach yields low ($< 300\ \Omega$) metal-to-semiconductor resistance R_C values, and an extension resistance of 34 ± 4 kΩ/µm in the nanowire diameter range investigated. We estimate the total source/drain external resistance R_{ext} to be 50 ± 6 kΩ, for nanowire devices with a 1.5 µm source and drain extension length. Figure 3.7(c-d) shows the $I_D - V_D$ data measured at various V_G for a $Si_{0.41}Ge_{0.59}$-Si core-shell [panel (c)], and a bare Si nanowire device [panel (d)]. The corresponding $I_D - V_G$ characteristics at different V_D for the same devices are shown in Fig. 3.7(e-f). The V_G and V_D value of each trace is indicated in the $I_D - V_D$ and $I_D - V_G$ data, respectively. Consistent with the source and drain doping, the devices show n-type enhancement mode MOSFET behavior with an on/off current ratio at $V_D = 50$ mV larger than 10^6 in $Si_{0.41}Ge_{0.59}$-Si core-shell nanowire devices. The devices possess small DIBL of a few tens of mV shift in the subthreshold region between the $V_D = 50$ mV and $V_D = 1$ V data, where the SS is ~100 mV/dec. In addition, we notice a reduced average V_T of 1.2 V for $Si_{0.41}Ge_{0.59}$-Si core-shell nanowires from 1.4 V for Si nanowires, which we attribute to a smaller bandgap, and lower conduction band for the tensile-strained Si [105]. To decouple the contact and channel intrinsic resistance, in Fig. 3.7(g-h) we plot the total device resistance R_{Total} vs. L_G at different $V_G - V_T$ values. The intersection point of the linear fit to the R_{Total} vs. L_G data at each gate overdrive yields the total source/drain external resistance ($R_{ext} + R_C$) of 45 kΩ.

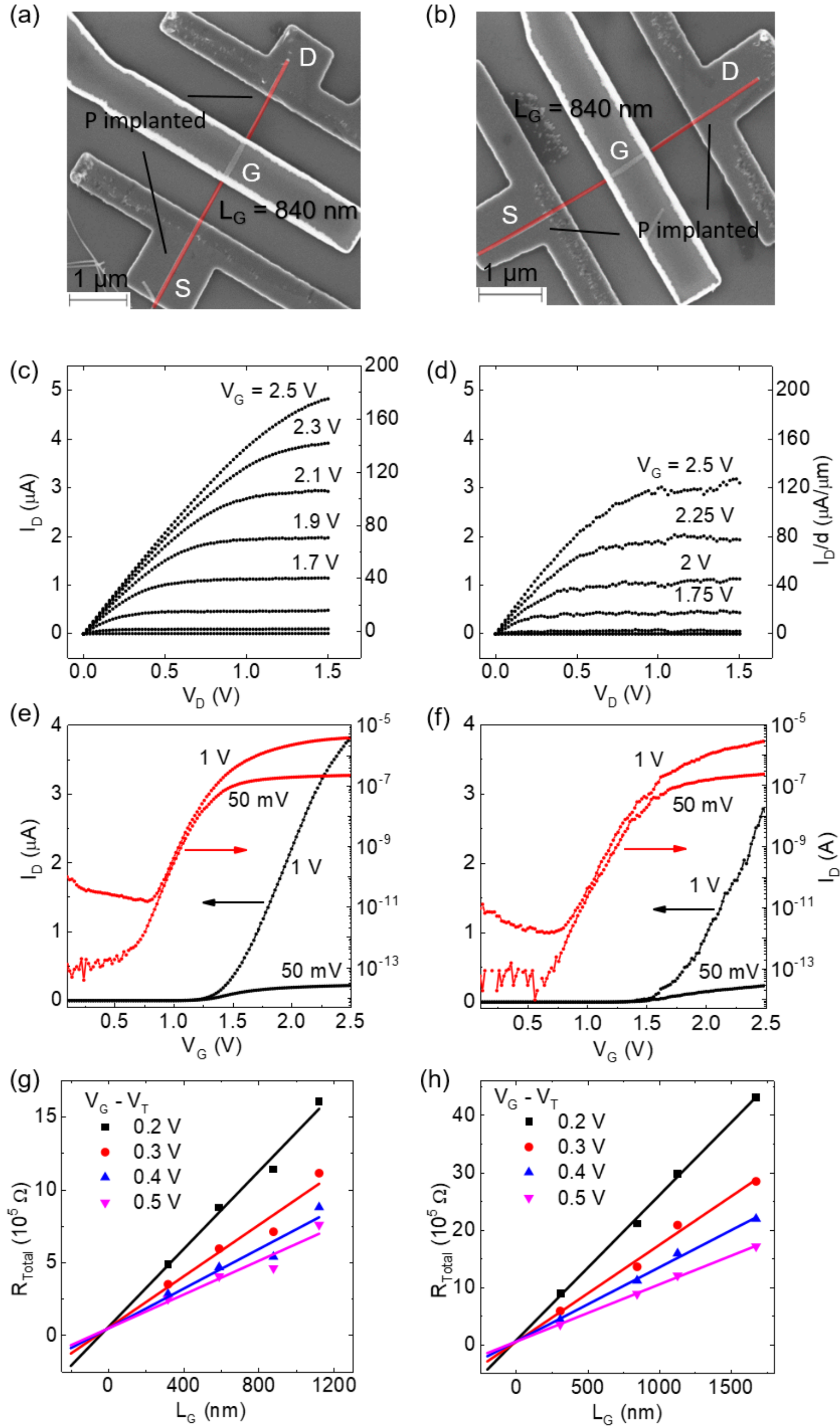

Figure 3.7: Electrical characteristics of $Si_{0.41}Ge_{0.59}$-Si core-shell and bare Si nanowire *n*-type MOSFETs. SEM images of (a) a $Si_{0.41}Ge_{0.59}$-Si core-shell and (b) a bare Si nanowire *n*-type MOSFETs. The source (S),

gate (G), and drain (D) contacts are labeled, and the phosphorus implant region are shaded in red. (c-d) Output and (e-f) transfer characteristics of the same devices shown in panels (a) and (b), respectively. The V_G (V_D) value is indicated in each trace for the output (transfer) curves. R_{Total} versus L_G at different overdrive voltages $V_G - V_T$ for (g) $Si_{0.41}Ge_{0.59}$-Si core-shell and (h) bare Si nanowire *n*-type MOSFETs, respectively. Linear fits (solid lines) to the experimental data (symbols) are also included. Figure 3.7: continued.

To compare the electron mobility (μ_e) in Si and $Si_{0.41}Ge_{0.59}$-Si core-shell nanowires, we extract the μ_e values in multiple devices from the V_G dependence of the intrinsic channel channel conductance $G_{ch} = \mu_e C_\Omega (V_G - V_T)/L_G$, where C_Ω is the Ω-gate capacitance per unit length, and $G_{ch} = (R_{Total} - R_{ext} - R_C)^{-1}$. The C_Ω values are extracted from FEM simulations of an Ω-gated two-dimensional structure, detailed in Section 3.8. We deduce the electron mobility using $\mu_e = (L_G/C_\Omega) \cdot (dG_{ch}/dV_G)$. Figure 3.8 histograms summarize the μ_e values extracted from over eighty Si and $Si_{0.41}Ge_{0.59}$-Si core-shell nanowire *n*-type MOSFET devices. The lines are Gaussian distributions with the mean and variance of the experimental data. We find the mean value of the electron mobilities of $Si_{0.41}Ge_{0.59}$-Si core-shell nanowire devices shows a 40% increase compared to that of Si nanowire devices. We note that the non-optimized gate stack reduces the mobilties for both bare Si and the $Si_{0.41}Ge_{0.59}$-Si core-shell nanowire *n*-type MOSFETs, and offsets in part the mobility enhancement associated with tensile strain in Si. Indeed, we expect that the use of an optimized gate stack to lead to a higher mobility in bare Si *n*-type MOSFETs, and a larger mobility enhancement for $Si_{0.41}Ge_{0.59}$-Si core-shell nanowire *n*-type MOSFETs. It is particularly noteworthy that <110> oriented tensile-strained Si channel has also been found to be most desirable for trigate *n*-type MOSFETs [106], coinciding with the growth direction of small diameter VLS Si (Ge) nanowires [38, 107].

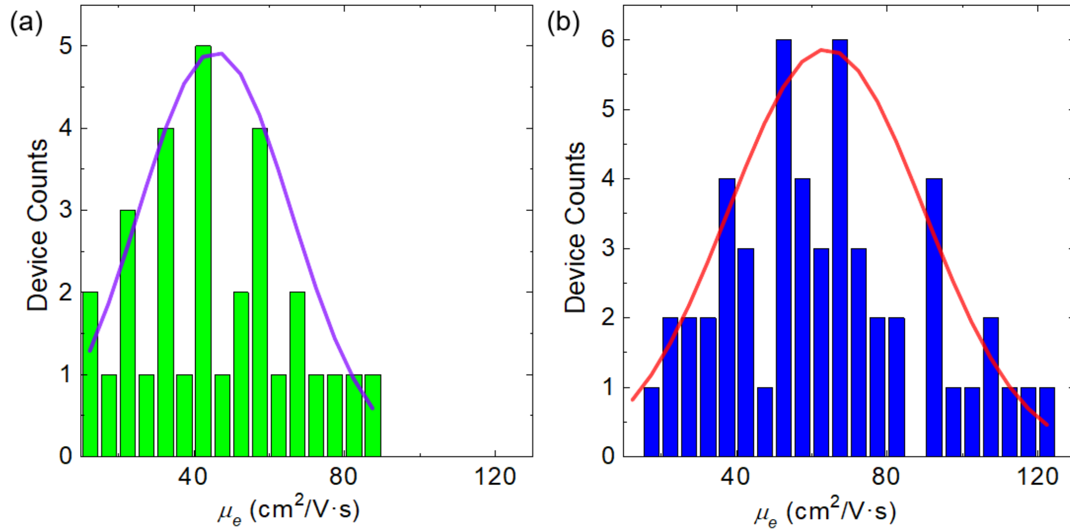

Figure 3.8: Histograms of μ_e values in (a) 31 Si nanowire *n*-type MOSFETs and (b) 52 $Si_{0.41}Ge_{0.59}$-Si core-shell nanowire *n*-type MOSFETs. Solid lines mark the Gaussian distributions corresponding to the experimental data.

3.7 Nanowire MOSFET fabrication

Figure 3.9 shows the schematics to reveal the fabrication process of *n*-type nanowire MOSFETs. We first remove the nanowires from the growth substrate by sonicating a piece of the growth substrate in ethanol, followed by drop-casting the nanowire solution onto a degenerately doped Si(100) substrate covered with a 70 nm thick thermal oxide and predefined alignment markers, which can also serve as the global back-gate [panel (a)]. We then deposit the Al_2O_3 top-gate dielectric using the plasma assisted ALD of 70 cycles at 250 ºC [panel (b)], after removing the Si native oxide in 1:80 diluted HF for 15 sec. We measure the thin film thickness of Al_2O_3 as 7.5 nm using ellipsometry on a planar Si substrate co-processed with the nanowire devices. The dielectric constant (ε_r) of the deposited Al_2O_3 film is 7.6, extracted from MOS capacitor devices. We define the top-gate using EBL, followed by sputtering TaN and metal lift-off in acetone. After a 10 sec O_2 plasma of 35 W cleaning in a reactive ion etching (RIE) tool, we etch the Al_2O_3 film

from the source and drain regions with 1:80 diluted HF for 20 sec [panel (c)]. To realize low extrinsic series resistances in the devices, phosphorus is implanted at an energy of 5 keV with a dose of 5×10^{14} cm^{-2}, using the TaN gate as a self-aligned implantation mask for the *n*-type MOSFET [panel (d)]. We activate the dopants in a rapid thermal annealing furnace at 550 ^{o}C for 10 min in a N_2 ambient. We complete the device fabrication after defining the source/drain contacts by performing EBL, native oxide removal in 1:80 diluted HF for 15 sec, electron beam evaporation of 85 nm thick Ni, and metal lift-off in acetone [panel (e)]. In all EBL steps mentioned above, we use an electron dose of 450 C/cm^2 during the exposure and PMMA A6 spin coated at 4000 rpm as resist, which becomes ~400 nm in thickness after 1 min bake on a 180 ^{o}C hotplate and is developed in MIBK : IPA = 1 : 3 for 30 sec after exposure.

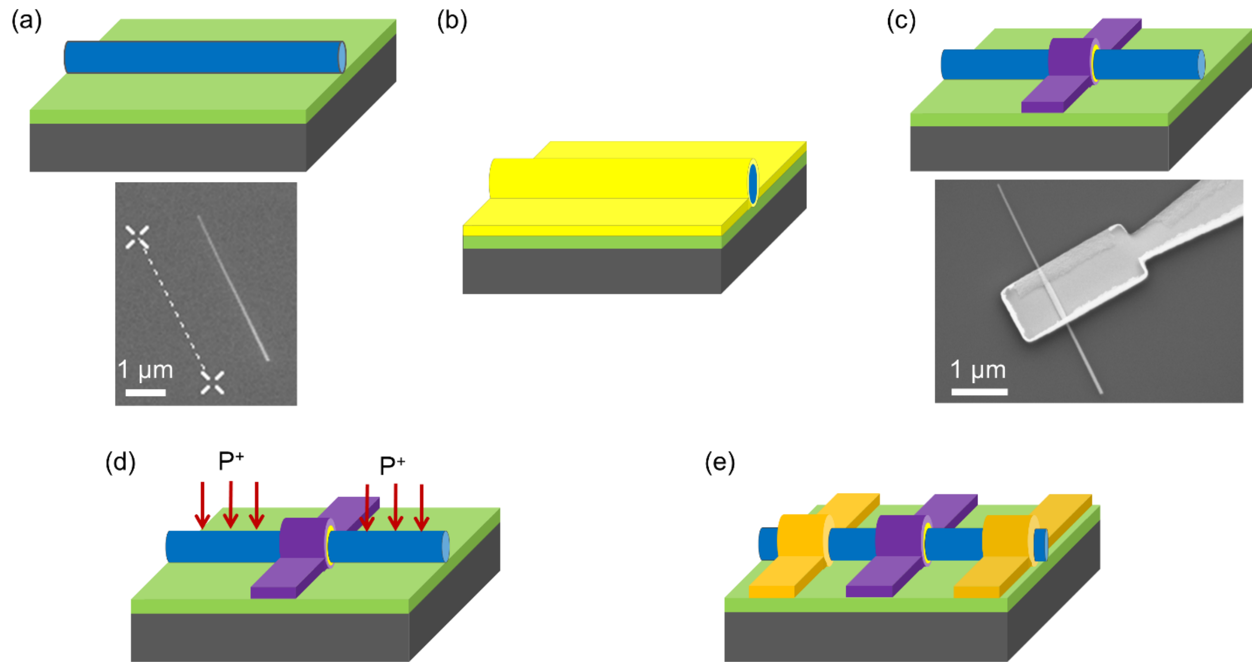

Figure 3.9: Fabrication process of nanowire *n*-type MOSFETs. (a) Disperse Si_xGe_{1-x}-Si core-shell nanowires onto an oxidized Si substrate. (b) Deposit Al_2O_3 gate dielectric using ALD. (c) Perform EBL, TaN sputtering and lift-off to define the gate pattern, followed by etching of the dielectric film elsewhere. (d) Self-aligned phosphorus ion implantation to dope the exposed nanowire segment for source/drain. (e)

Use EBL, Ni evaporation and lift-off to define the source/drain contacts. The lower parts of panels (a) and (c) are the SEM images of the corresponding fabrication stages. The SEM image of a completed device can be found in Fig. 3.7(a-b). Figure 3.9: continued.

3.8 Extraction of C_Ω for nanowire MOSFETs

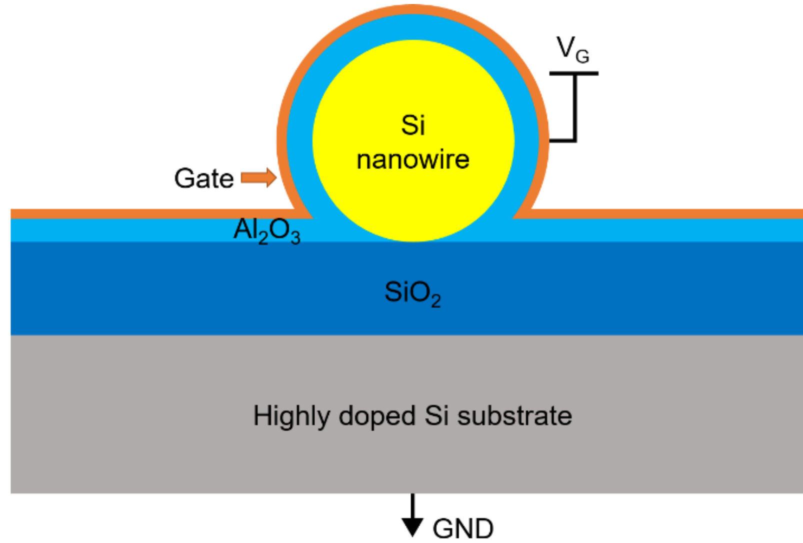

Figure 3.10: Schematic of the simulation structure to extract C_Ω for Si nanowire MOSFETs.

In this section, we demonstrate the approach to calculate C_Ω that applies to all Ω-gated nanowire MOSFETs studied in both Chapter 3 and 4. The simulation structure to extract C_Ω is a two-dimensional Ω-gate cross-section of the device, according to the actual device structure fabricated with the process depicted in Section 3.7. The simulation parameters we adjust usually include the shell thickness and morphology as identified in the cross-sectional TEM imaging, the diameter of the cylindrical core, the thickness and dielectric constant of the conformal ALD oxide, and the band alignment between the core and shell(s) for core-(multi-)shell nanowires. Here for simplicity, we use the bare Si nanowire as an example to illustrate the C_Ω calculation procedure for both n-type and p-type nanowire MOSFETs. Figure 3.10 shows the schematic of the structure to extract C_Ω for bare Si nanowire MOSFETs, the gate oxide has $\varepsilon_r = 7.6$ and $t_{ox} = 7.5$ nm based

on the actual properties of our ALD Al_2O_3. This simulation structure extends to any radial nanowire heterostructures discussed in this thesis by replacing the Si nanowire cross-section with that of the core-(multi-)shell nanowire.

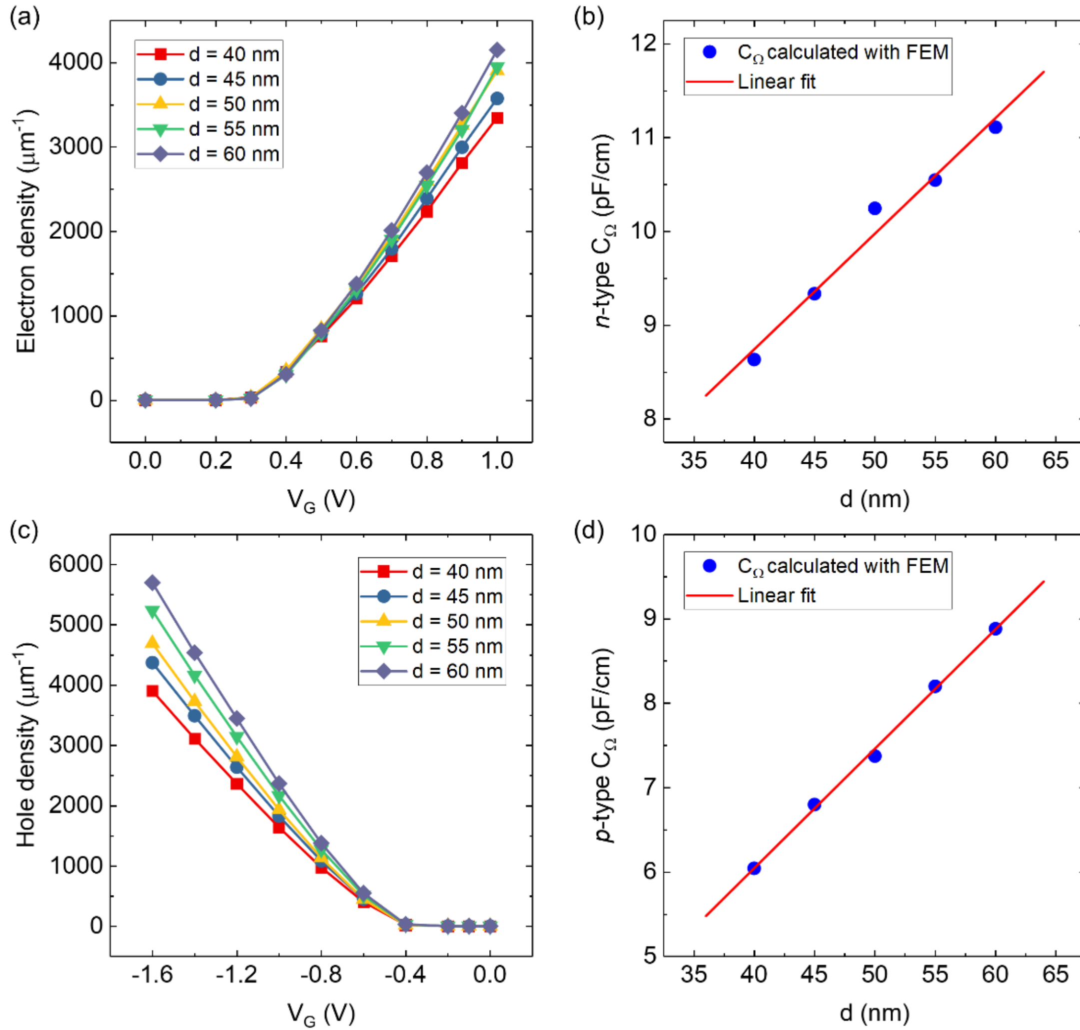

Figure 3.11: Carrier density per unit length and C_Ω vs. d. (a) Number of electrons per μm vs. positive V_G and (b) d dependence of the calculated C_Ω for *n*-type bare Si nanowire MOSFETs. (c) Number of holes per μm vs. negative V_G and (d) d dependence of the calculated C_Ω for *p*-type bare Si nanowire MOSFETs.

We use the FEM solver in the Sentaurus TCAD (©Synopsys) environment to calculate the carrier concentration per unit length (the 3rd dimension perpendicular to the cross-section) as a function of V_G by solving Poisson's equation and continuity equations self-consistently. We use

the density gradient model to account for the quantum mechanical effects. We construct simulation structures of different diameters to cover the experimental range of the growth. Figure 3.11(a) presents a family of curves indicating the V_G dependence of the electron density per unit length for Si nanowires of various diameters. We extract C_Ω from the slopes of the curves in the V_G regime where the electron densities increase linearly. Figure 3.11(b) summarizes the extracted C_Ω plotted against d and the linear fit of the data, from which we obtain the C_Ω value for individual n-type Si nanowire MOSFET to calculate μ_e. Similarly, Figure 3.11(c-d) shows the hole density vs. V_G data for different d, and the corresponding C_Ω vs. d data for p-type Si nanowire MOSFETs.

3.9 Summary

In conclusion, we demonstrate the growth, structural and electrical characterization of epitaxial, coherently strained Si_xGe_{1-x}-Si core-shell nanowires. Conduction band edge energy calculations indicate a positive core-to-shell conduction band offset of 280 meV due to a large tensile strain in the Si shell. Raman spectroscopy reveals peaks associated with Si-Si, Si-Ge, Ge-Ge modes in the core and Si-Si mode in the shell. The core (shell) peaks are blue-shifted (red-shifted) from their unstrained values, consistent with a compressive (tensile) strain in the core (shell) region, and the Raman shift values agree well with calculations using lattice dynamic theory combined with finite-element strain simulation. Enhancement mode n-type MOSFETs using Si_xGe_{1-x}-Si core-shell nanowires as channel show a significant increase in mobility by comparison with Si nanowire control devices.

Chapter 4 : Strained Si_xGe_{1-x}-Ge-Si Core-double-shell Nanowire Heterostructures for Simultaneous Hole and Electron Mobility Enhancement[3]

4.1 Introduction

We report the growth, structural and electrical characterization of epitaxial, strained Si_xGe_{1-x}-Ge-Si core-double-shell nanowire heterostructures designed to provide quantum confinement of holes and electrons in the compressively strained Ge and tensile strained Si shell, respectively. The growth utilizes VLS growth mechanism for the Si_xGe_{1-x} core, followed by a sequence of *in-situ* ultra-high-vacuum CVD for the epitaxial Ge and Si shell growth. Using a combination of micro-Raman spectroscopy on individual nanowires, and lattice dynamic theory we determine a large compressive (tensile) hydrostatic strain of up to -0.9% (0.67%) in the Ge (Si) shell. We demonstrate both p-type and n-type MOSFETs using Si_xGe_{1-x}-Ge-Si core-double-shell nanowires as channel, and observe a 500% (20%) enhancement of the average hole (electron) mobility compared to control devices using Si nanowires, due to an increased hole (electron) mobility in the compressively strained Ge (tensile strained Si) shell. An analysis of the hole transport at liquid nitrogen temperature provides the valence band offset in the core-double-shell nanowire heterostructures. We also present the impact of the Ge and Si shell thickness on the MOSFET device characteristics including V_T, carrier mobility and short channel effects.

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[3] Part of this chapter was published previously: [108] F. Wen and E. Tutuc, "Strained Si_xGe_{1-x}-Ge-Si core-double-shell nanowire heterostructures for simultaneous hole and electron mobility enhancement," *Applied Physics Letters,* vol. 113, p. 113102, 2018.

F. Wen performed the nanowire growth, TEM, Raman measurements, simulations, calculations, MOSFET fabrications and electrical characterizations. F. Wen and E. Tutuc analyzed the data and co-wrote the manuscript. Both authors contributed to and approved the final version of the manuscript.

In previous chapters we have discussed strain engineering, which is currently a requisite element in enhancing the performance of MOSFETs. Tensile or compressive strain has been integrated into *n*-type or *p*-type MOSFETs to increase the carrier mobility and drive current, which remains relevant even when new materials beyond Si are examined, including Ge and various III-V compounds [109, 110]. A variety of innovative techniques have been devised to implement both signs of strain into the same platform, such as compressive and tensile stressed SiN liners [111], global biaxial strain [112] and local epitaxial stressed source/drain [113]. In this chapter, we explore the approach to induce strain through lattice-engineered hetero-epitaxial growth into non-planar MOSFETs using Si_xGe_{1-x}-Ge-Si core-double-shell nanowires. Mobility enhancement and quantum confinement of holes and electrons have been demonstrated in Ge-Si_xGe_{1-x} and Si_xGe_{1-x}-Si core-shell nanowire heterostructures in earlier studies and Chapter 3, respectively [8, 78]. They render the double-shell heterostructure a promising candidate for non-planar GAA MOSFETs to simultaneously integrate quantum confinement and strain-induced mobility enhancement for both electrons and holes.

The chapter is organized as follows. In Section 4.2, we discuss a strained Si/Ge dual-channel planar heterostructure designed for a simultaneous electron and hole mobility enhancement, which inspires the study presented in this chapter. We will discuss its structure, band diagram and carrier transport property. Section 4.3 presents the growth process and TEM imaging data of Si_xGe_{1-x}-Ge-Si core-double-shell nanowires. We have performed multiple growths with different Ge and Si shell thicknesses, and will analyze one of them in detail from Section 4.4 to 4.6. Section 4.4 presents the Raman spectrum of an individual Si_xGe_{1-x}-Ge-Si core-double-shell nanowire, and the two-dimensional contour plot of the strain tensor. Section 4.5 shows the carrier transport properties of both electrons and holes probed in *n*-type and *p*-type MOSFETs using

Si_xGe_{1-x}-Ge-Si core-double-shell nanowires as channel. Section 4.6 reveals the conduction and valence band alignment between the Ge and Si shell. In Section 4.7, we compare the electrical characteristics of Si and Si_xGe_{1-x}-Ge-Si core-double-shell nanowire MOSFETs from different growths. Section 4.8 presents the approach to extract μ_{eff} and the setup to simulate the charge transport property for a nanowire MOSFET. Section 4.9 summarizes the chapter.

4.2 Strained Si/Ge dual-channel planar heterostructure for high mobility *n*-type and *p*-type MOSFETs

We discuss the planar strained Si/strained Ge dual-channel heterostructure used to fabricate high mobility *n*-type and *p*-type MOSFETs in this section [112, 114]. This dual-channel heterostructure combines a surface Si layer of tensile strain with a buried Ge layer of compressive strain. This planar heterostructure is grown on a relaxed Si_xGe_{1-x} virtual substrate, which is established from the Si(100) substrate through a SiGe graded buffer. Figure 4.1(a) presents the cross-sectional TEM image of this planar heterostructure. Although the interfaces among different layers are smooth, strain-induced defects due to large lattice mismatch are visible in the Si layer. Figure 4.1(b) shows the device schematic of a dual-channel heterostructure MOSFET. In the study of Lee *et al*. [112, 114], the authors fabricated both *n*-type and *p*-type MOSFETs, revealing mobility enhancement factors of 1.7 - 1.9 for electrons and 10 - 12 for holes. In this dual-channel heterostructure, the surface Si layer and the buried Ge layer are the conduction channels of electrons and holes for the *n*-type and *p*-type MOSFETs, respectively. The separation of the *n*-type and *p*-type channel is due to the type-II band alignment between the Si and Ge layer [115]. Figure 4.2 schematically illustrates the type-II band alignment between the tensile strained Si and the compressively strained Ge grown on a relaxed Si_xGe_{1-x} virtual substrate. Similar to the planar

heterostructure discussed in Section 3.2, where a tensile strained Si layer is grown directly on the Si_xGe_{1-x} virtual substrate, the six-fold degenerate conduction band valleys in the Si layer of the dual-channel heterostructure is also split into two groups due to a biaxial tensile strain. The group consisting of the two-fold degenerate valleys has a lower energy compared to the group of the four-fold degenerate valleys and the conduction band minimum of the Ge layer, and becomes the bottom-most conduction band for the dual-channel heterostructure. On the other hand, the heavy-hole band is the top-most valence band in the compressively strained Ge layer, and has a higher energy than the valence band maximum of the Si layer. Therefore, electrons and holes will preferentially populate the two-fold degenerate conduction band valleys of Si and the heavy hole band of Ge in the *n*-type and *p*-type MOSFETs using the dual-channel heterostructure as channel, respectively.

The strain profile and thus the electrical characteristics of the dual-channel heterostructure depend on both the composition of the Si_xGe_{1-x} virtual substrate, as well as the thicknesses of the two strained Si/Ge layers. For example, a large Ge content in the virtual substrate can result in a too large tensile strain in the Si layer, and the electron mobility is therefore limited by the defect scattering. On the other hand, if the heterostructure is optimized properly, it allows the realization of MOSFETs with a simultaneous mobility enhancement of both electrons and holes. Moreover, the hole mobility can potentially match the electron mobility to provide a symmetric pair of devices for CMOS. Figure 4.1(c) shows the electron and hole effective mobility as a function of the inversion charge concentration for the long-channel MOSFETs fabricated on bulk Si, strained Si on $Si_{0.75}Ge_{0.25}$ virtual substrate and the dual-channel heterostructure. The optimized *n*-type MOSFET has a layer thickness of 7.5 nm for the Si channel and 6 nm for the Ge channel, while the optimized *p*-type MOSFET has it as 4 nm and 12 nm, respectively. Figure 4.1(d) presents the

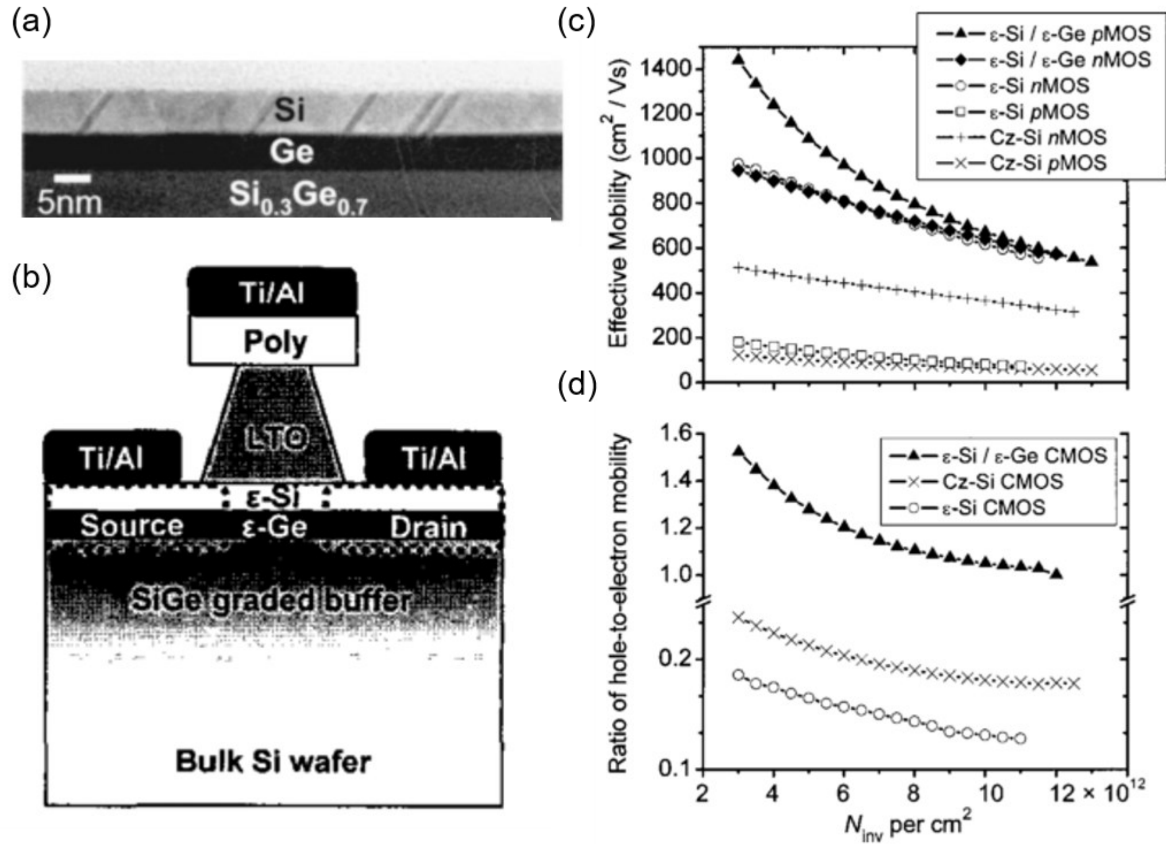

Figure 4.1: (a) Cross-sectional TEM image of the strained Si/strained Ge planar dual-channel heterostructure. (b) Schematic of a completed MOSFET. (c) Effective mobility of electrons and holes and (d) ratio of the hole effective mobility over that of electrons against inversion charge concentration for long-channel MOSFETs, including the dual-channel heterostructure, strained Si and bulk Si devices. (Figure adapted from Refs. [112, 114])

ratio of the hole effective mobility over the electron effective mobility for MOSFETs fabricated on the three types of substrates. For both the MOSFETs fabricated on bulk Si and strained Si on $Si_{0.75}Ge_{0.25}$ substrate, the hole mobility is low compared to the electron mobility. While in the dual-channel heterostructure with a geometry of the optimized *p*-type MOSFET, the hole effective mobility matches and even exceeds the electron effective mobility at lower inversion charge concentrations. Therefore, this dual-channel heterostructure is a promising candidate to fabricate MOSFETs that allows a simultaneously enhanced electron and hole effective mobility that can

also match each other. The Si_xGe_{1-x}-Ge-Si core-double-shell nanowire heterostructure is the non-planar equivalent to this planar dual-channel heterostructure, which potentially becomes one solution to the ultimate scaling of CMOS. Using the Si_xGe_{1-x}-Ge-Si core-double-shell nanowire as channel allows a GAA geometry for the best gate electrostatic control, and provides an enhanced and symmetric carrier mobility for both electrons and holes.

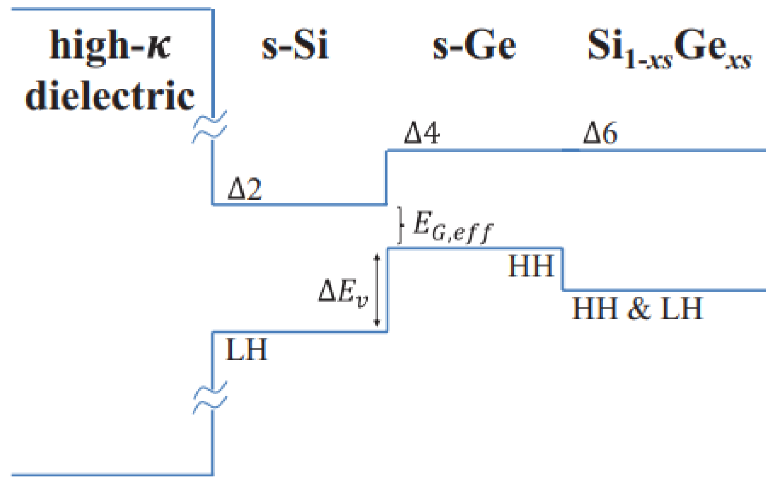

Figure 4.2: Schematic of the energy band diagram of the planar dual-channel heterostructure, showing a type-II band alignment between the strained Si and Ge. (Figure adapted from Ref. [115])

4.3 Growth and TEM imaging of Si_xGe_{1-x}-Ge-Si core-double-shell nanowires

The growth of our Si_xGe_{1-x}-Ge-Si core-double-shell nanowires consists of a sequence of VLS Si_xGe_{1-x} nanowire core growth, followed by a two-stage *in-situ* epitaxial Ge and Si shell growth using ultra-high-vacuum CVD. The additional axial VLS growth induced during the shell growth is again negligible compared with the core growth because of a much smaller precursor partial pressure. In addition, we grow bare Si_xGe_{1-x} nanowires using the same VLS growth recipe to extract the Si_xGe_{1-x} alloy composition, which corresponds to NW239 in our growth catalog. We also use Si nanowires grown with the recipe depicted in Section 3.3 (NW214) to make MOSFET

control devices to compare the carrier mobility with MOSFETs using Si_xGe_{1-x}-Ge-Si core-double-shell nanowires as channel. We have performed three different growths of Si_xGe_{1-x}-Ge-Si core-double-shell nanowires to study the impact of the thickness of Ge and Si shells on the strain and charge transport properties. We use the same Si_xGe_{1-x} core growth recipe and tune the shell thickness by controlling the CVD growth temperature and time. The accuracy of the thickness control is impacted by the temperature variance for the same heater current setpoint in different growths. Therefore, cross-sectional TEM imaging must be applied to measure the actual shell thickness of the Ge and Si shell for each growth, in order to properly calculate the strain distribution and understand the charge transport property. We name the three growths of Si_xGe_{1-x}-Ge-Si core-double-shell (CDS) nanowires as CDS1, CDS2 and CDS3, which correspond to growths NW241, NW238 and NW240 in our nanowire growth catalog, respectively. Table 4.1 summarizes the detailed growth conditions of all nanowires discussed in this chapter. The 5th to 7th column contains the recipes for both the Ge and Si shell growth, separated by a semicolon. For clarity, we only present the structural and electrical analysis of the Si_xGe_{1-x}-Ge-Si core-double-shell nanowires obtained from one single growth (CDS2) until Section 4.7. The detailed growth process of the CDS2 Si_xGe_{1-x}-Ge-Si core-double-shell nanowire is as follows. We first grow the Si_xGe_{1-x} core using the VLS mechanism at a substrate temperature of 320 ºC using SiH_4 (100%, 100 sccm) and GeH_4 (20% in He, 14 sccm) as precursors at 10 Torr. Again, the Au catalyst nanoparticles are generated through an Au thin film deposition on the Si(111) growth substrate followed by the H_2 thermal annealing. Next, the Ge shell is grown *in-situ* epitaxially onto the Si_xGe_{1-x} core at ~305 ºC, employing GeH_4 (55 sccm) as precursor at a chamber pressure of 37 mTorr. Finally, the Si shell is grown *in-situ* epitaxially onto the Ge shell with SiH_4 (60 sccm) as precursor at 485 ºC and a chamber pressure of 41 mTorr.

Table 4.1: Growth conditions of the nanowires discussed in Chapter 4

Growth type and name	GeH_4/SiH_4 flow during core growth (s.c.c.m.) and chamber pressure (Torr)	Core growth temperature (°C)	Core growth time (min)	GeH_4/SiH_4 flow during shell growth (s.c.c.m.) and chamber pressure (Torr)	Shell growth temperature (°C)	Shell growth time (min)
Si_xGe_{1-x}-Ge-Si (NW241)	14/100, 10	320	42	55/0, 37m; 0/60, 39m	305; 485	60; 20
Si_xGe_{1-x}-Ge-Si (NW238)	14/100, 10	320	42	55/0, 37m; 0/60, 41m	305; 485	60; 25
Si_xGe_{1-x}-Ge-Si (NW240)	14/100, 10	320	42	55/0, 37m; 0/60, 41m	310; 490	60; 25
Si_xGe_{1-x} (NW239)	14/100, 10	320	42	N/A; N/A	N/A; N/A	N/A; N/A
Si (NW214)	0/100, 10	410	18	N/A; N/A	N/A; N/A	N/A; N/A

The schematics in Fig. 4.3(a-d) depict the growth process of Si_xGe_{1-x}-Ge-Si core-double-shell nanowires. Figure 4.4 shows the SEM image of the cross-section of a part of the Si_xGe_{1-x}-Ge-Si core-double-shell nanowire growth substrate. The appearance of the nanowires resembles that of the Si_xGe_{1-x}-Si core-shell nanowires presented in Fig 3.3, since they both feature Si_xGe_{1-x} cores grown in similar conditions. For the Si_xGe_{1-x}-Ge-Si core-double-shell nanowires discussed in this chapter, the core VLS growth recipe is tuned to produce an alloy composition of $Si_{0.5}Ge_{0.5}$, verified using Raman spectroscopy as well as STEM coupled with energy dispersive X-ray

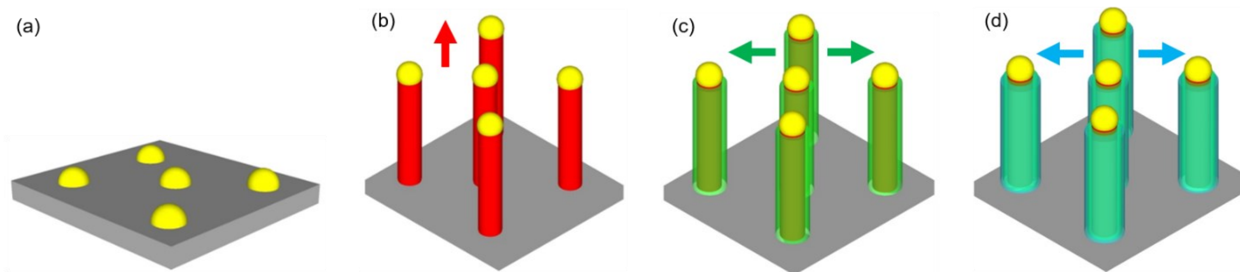

Figure 4.3: Schematic of the $Si_{0.5}Ge_{0.5}$-Ge-Si core-double-shell nanowire heterostructure growth. (a) Au catalyst formed by H_2 annealing. (b) $Si_{0.5}Ge_{0.5}$ core growth by VLS. (c) Ge and (d) Si shell growth by CVD. The arrows indicate the growth directions in the corresponding regime.

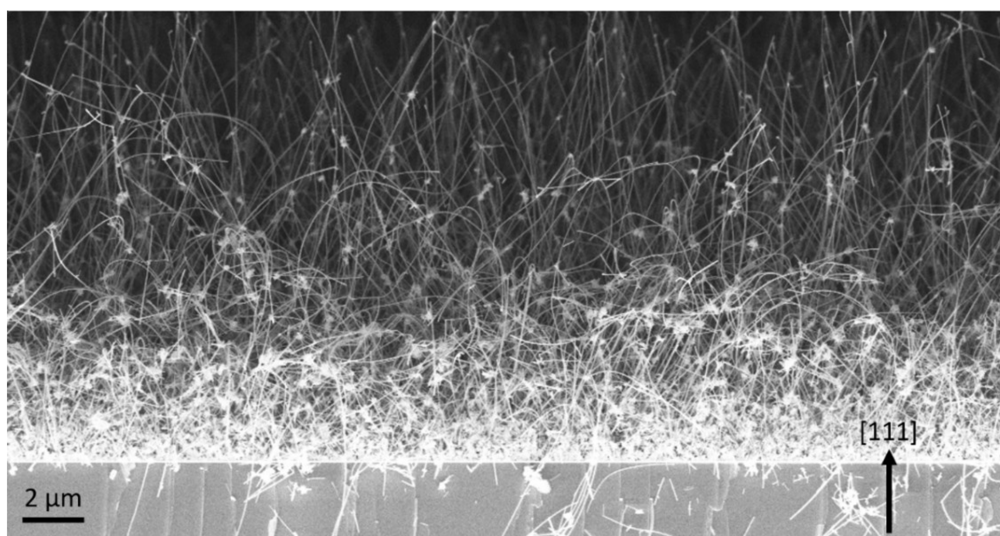

Figure 4.4: Cross-sectional SEM image of as-grown $Si_{0.5}Ge_{0.5}$-Ge-Si core-double-shell nanowires

spectroscopy. Figure 4.5(a) presents the planar view TEM data that reveals the single-crystal structure of the $Si_{0.5}Ge_{0.5}$-Ge-Si core-double-shell nanowire, where the inset FFT indicates the VLS growth is along the <110> direction. This growth direction applies to all nanowires discussed in this chapter. Figure 4.5(b) shows the cross-sectional TEM image of a $Si_{0.5}Ge_{0.5}$-Ge-Si core-double-shell nanowire, from which we determine the Ge and Si shell thickness as 4.5 and 5 nm, respectively. The Ge and Si shell CVD growth takes 60 and 25 min, corresponding to a growth rate of 0.75 and 2 Å/s, respectively. This Si shell growth temperature and thus the growth rate is

higher than that of the Si_xGe_{1-x}-Si core-shell nanowire, which is ~0.5 Å/s at 460 °C, because we find the slower growth rate produces a rough nanowire sidewall.

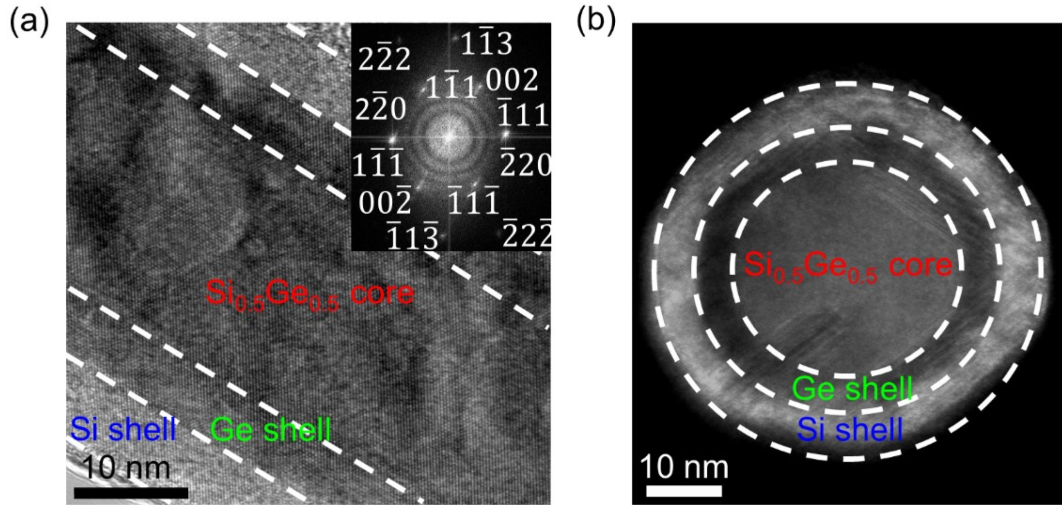

Figure 4.5: (a) Planar view TEM image of a <110> oriented $Si_{0.5}Ge_{0.5}$-Ge-Si core-double-shell nanowire, where the interfaces between core and shells are marked for clarity. Inset: FFT of the main panel data, with the zone axis along the [110] direction. (b) Cross-sectional TEM image of a $Si_{0.5}Ge_{0.5}$-Ge-Si core-double-shell nanowire, where the interfaces are marked for clarity.

4.4 Raman spectra and strain calculation of $Si_{0.5}Ge_{0.5}$-Ge-Si core-double-shell nanowires

The lattice mismatch between core and shells in this radial nanowire heterostructure will introduce compressive strain in the Ge shell and tensile strain in the Si shell. The compressive (tensile) strain can significantly enhance the hole and electron mobility in Ge and Si by suppressing the interband phonon scattering and reducing the effective mass in the transport direction [86, 116]. Because the strain will also shift the optical phonon frequencies, we use Raman spectroscopy on individual $Si_{0.5}Ge_{0.5}$-Ge-Si core-double-shell nanowire to probe the shifted optical phonon frequencies and convert them to an effective strain in the nanowire, through lattice dynamic theory

calculations combined with a continuum elasticity model [62, 64]. The details of the above techniques have been applied to analyze core-shell nanowires in Chapters 2 and 3, and are discussed in detail in Sections 2.6 and 2.7. Figure 4.6(a) shows the Raman spectrum of an individual $Si_{0.5}Ge_{0.5}$-Ge-Si core-double-shell nanowire. It reveals five major peaks that are labeled with dashed lines. Those at 296.9, 408.0 and 489.7 cm^{-1} are associated with Ge-Ge, Si-Ge and Si-Si Raman modes in the $Si_{0.5}Ge_{0.5}$ core. These Raman modes are slightly blue-shifted compared to the bare $Si_{0.5}Ge_{0.5}$ nanowire, indicating a small compressive strain induced in the core. The peak at 308.6 cm^{-1} is associated with the Ge-Ge Raman mode in the Ge shell, which is blue-shifted compared with the bare Ge nanowire mode at 300.5 cm^{-1}, and signals a compressive strain in the Ge shell. On the other hand, the peak at 510.7 cm^{-1}, associated with the Si-Si mode in the Si shell, shows a red shift compared to the unstrained 520.6 cm^{-1} value measured in bare Si nanowires, and indicates a tensile strained Si shell.

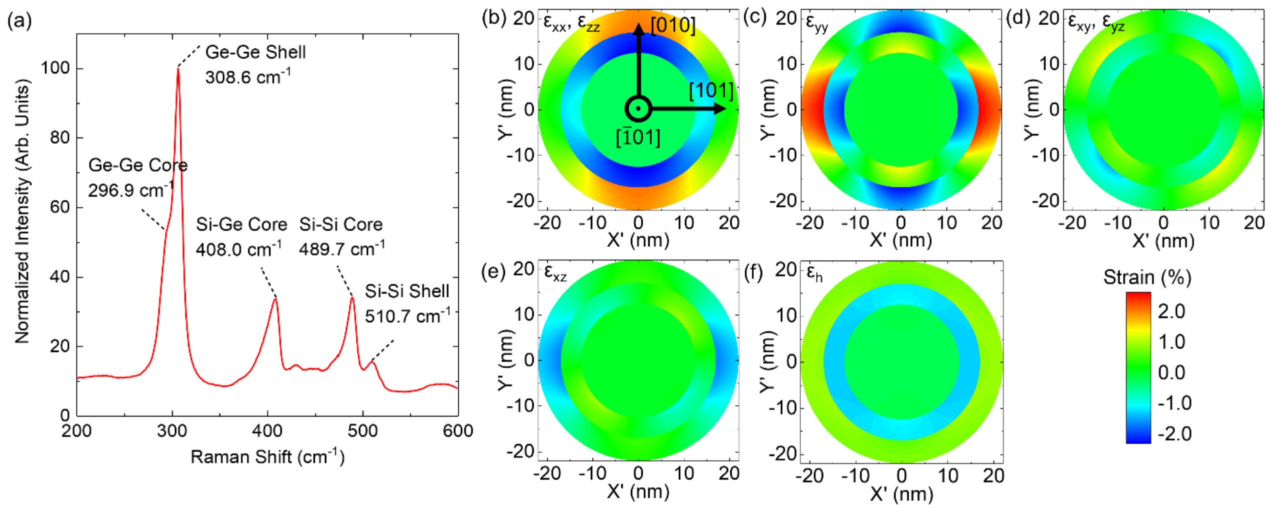

Figure 4.6: Raman spectroscopy and strain calculations of the $Si_{0.5}Ge_{0.5}$-Ge-Si core-double-shell nanowire. (a) Raman spectrum acquired from an individual $Si_{0.5}Ge_{0.5}$-Ge-Si core-double-shell nanowire. Two-dimensional contour plots of the simulated (b-e) strain tensor components and (f) ε_h for a $Si_{0.5}Ge_{0.5}$-Ge-Si core-double-shell nanowire. The crystal directions indicated in panel (b) apply to panels (b-f).

We perform FEM simulations to quantitatively understand the strain distribution in our $Si_{0.5}Ge_{0.5}$-Ge-Si core-double-shell nanowire heterostructures, the detail of the implementation has been presented in Section 2.5 [33, 99]. We use cylindrical geometries for both core and shells in the simulation structure, whose validity has been justified in Section 2.8. Figure 4.6(b-e) shows the simulated two-dimensional contour plots of the strain tensor, along with ε_h [Fig. 4.6(f)] for a $Si_{0.5}Ge_{0.5}$-Ge-Si core-double-shell nanowire. We find that while the different components of the strain tensor are non-uniform in both shell regions [99], ε_h is uniform across the shells, and indeed indicates compressive strain in the $Si_{0.5}Ge_{0.5}$ core and Ge shell, and tensile strain in the Si shell.

Figure 4.7(a-b) presents the diameter dependence data of the shell Ge-Ge and Si-Si Raman modes, along with the corresponding ε_h value on the right y-axis, for the Ge and Si shells in $Si_{0.5}Ge_{0.5}$-Ge-Si core-double-shell nanowires, respectively [78]. The symbols summarize the experimental data acquired from individual nanowires, and the solid lines represent the calculations based on lattice dynamic theory assuming coherently strained heterostructures. The experimental average ε_h values are -0.71% and 0.58% for the Ge and Si shell regions, respectively. On the other hand, the simulation reveals the average ε_h values of -1.2% and 0.8% in the diameter range investigated in this study. While the comparison between experimental data and calculations reveals a partial strain relaxation in the heterostructures, the experimental value is still larger compared to values reported in strained Si p-type (-0.45%) and n-type FinFETs (+0.4%) [101, 117, 118], and can potentially lead to a higher carrier mobility enhancement [105, 116]. To identify at what stage this strain relaxation occurs, we also grow $Si_{0.5}Ge_{0.5}$-Ge core-shell nanowires and measure the diameter dependence of the shell Ge-Ge mode, using the recipe of the VLS core and Ge shell growth of the CDS2 $Si_{0.5}Ge_{0.5}$-Ge-Si core-double-shell nanowire, i.e. $t_{sh}(\text{Ge}) = 4.5$ nm. Figure 4.7(c) presents the shell Ge-Ge mode against diameter for $Si_{0.5}Ge_{0.5}$-Ge core-shell

nanowires, which corresponds to growth NW233 in our nanowire growth catalog. We find that the Ge shell is not coherently strained to the $Si_{0.5}Ge_{0.5}$ core, and the magnitude of ε_h remains close to -0.4% in the diameter range of 20 - 35 nm. Hence, for the $Si_{0.5}Ge_{0.5}$-Ge-Si core-double-shell nanowire, a strain relaxation in the Ge shell occurs prior to the growth of the Si shell. Nevertheless, the additional Si shell drastically increases the magnitude of ε_h in the Ge shell.

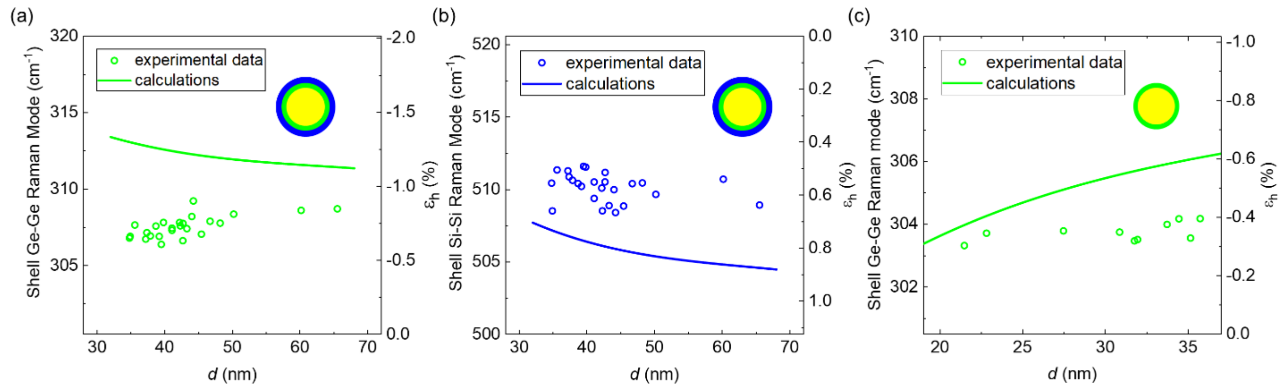

Figure 4.7: Diameter dependence of the shell Raman modes. (a) Ge-Ge modes in the Ge shell for $Si_{0.5}Ge_{0.5}$-Ge-Si core-double-shell nanowires. (b) Si-Si modes in the Si shell for $Si_{0.5}Ge_{0.5}$-Ge-Si core-double-shell nanowires. (c) Ge-Ge modes in the Ge shell for $Si_{0.5}Ge_{0.5}$-Ge core-shell nanowires. The corresponding ε_h value is indicated on the right *y*-axis for each panel. The symbols (lines) represent the experimental data (calculations). The inset illustrates the geometry of the corresponding nanowire heterostructure.

4.5 Electron and hole transport in $Si_{0.5}Ge_{0.5}$-Ge-Si core-double-shell nanowires

We probe the electron and hole transport in $Si_{0.5}Ge_{0.5}$-Ge-Si core-double-shell nanowires using Ω-gate nanowire MOSFETs with highly doped source and drain. Figure 4.8 presents the SEM image of the final device of a $Si_{0.5}Ge_{0.5}$-Ge-Si core-double-shell nanowire MOSFET, where the three terminals are labeled, and the highly doped ion-implanted segments are shaded in red. The fabrication process of *n*-type nanowire MOSFETs is identical to that described in Section 3.7. In the discussion of this chapter, we also fabricate and investigate the performance of *p*-type

nanowire MOSFETs. Their fabrication process is mostly identical to that of n-type nanowire MOSFETs, except for that in the ion implantation stage, boron instead of phosphorus is implanted at an energy of 3 keV with a dose of 10^{15} cm^{-2} for the highly doped source and drain.

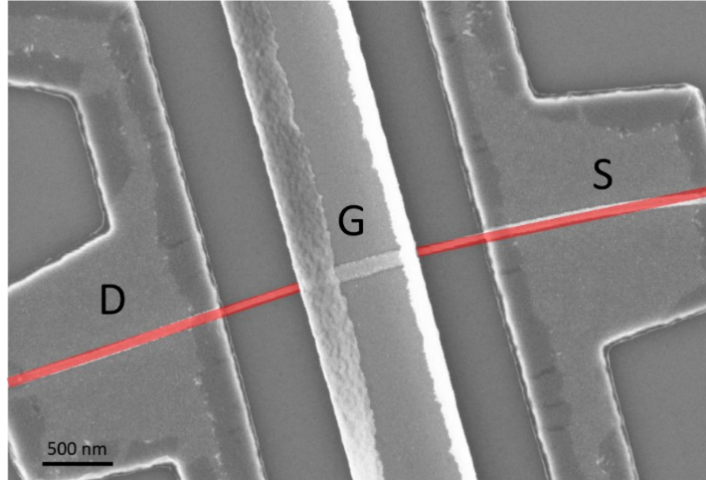

Figure 4.8: SEM image of a $Si_{0.5}Ge_{0.5}$-Ge-Si core-double-shell nanowire MOSFET. The gate, source and drain contacts are labeled. The regions ion-implanted with boron or phosphorus are shaded in red.

Figure 4.9(a-b) show I_D versus V_D at various fixed V_G measured in p-type and n-type MOSFETs, respectively. The corresponding $I_D - V_G$ characteristics at different V_D values are shown in Fig. 4.9(c-d). The on/off ratio at $|V_D| = 50$ mV is 10^4 for the p-type, and 5×10^5 for the n-type MOSFET. The electrostatic gate control is better in the n-type MOSFETs compared to the p-type MOSFET because the Ge channel is buried under the surface Si channel. Therefore, the n-type MOSFET possesses a smaller DIBL and SS, by comparison to the p-type counterpart. Figure 4.9(e-f) presents the R_{Total} vs. L_G at different $|V_G - V_T|$ values. The data is used to decouple the external series and channel intrinsic resistance, and extract μ_{eff} of both holes and electrons. Figure 4.9(e-f) insets show μ_{eff} as a function of $|V_G - V_T|$ for the same devices shown in Fig. 4.9(a-d) (Section 4.8 presents the method for μ_{eff} extraction), demonstrating a peak value of 400 and 120

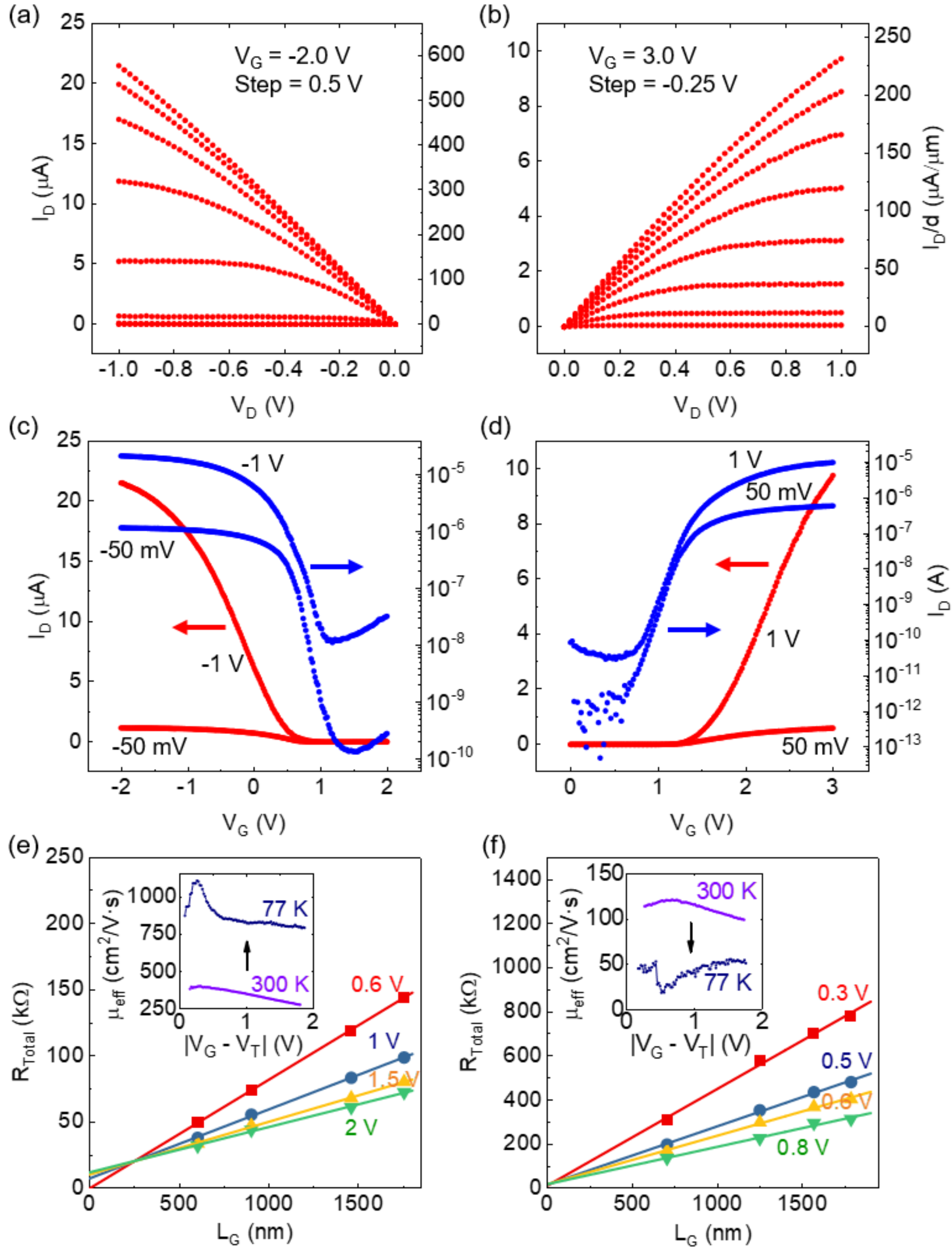

Figure 4.9: Room temperature electrical characteristics of $Si_{0.5}Ge_{0.5}$-Ge-Si core-double-shell *p*-type and *n*-type MOSFETs. (a-b) $I_D - V_D$ data of $Si_{0.5}Ge_{0.5}$-Ge-Si core-double-shell *p*-type ($d = 37$ nm, $L_G = 950$ nm) and *n*-type ($d = 42$ nm, $L_G = 630$ nm) MOSFETs, respectively. The *y*-axis labels apply to both panels. (c-d) $I_D - V_G$ data of the panel (a) and (b) devices. The V_G and V_D values are indicated for each trace. The *y*-axis labels apply to both panels. (e-f) R_{Total} vs. L_G at different overdrive voltages with $|V_G - V_T|$ indicated for each trace, measured in $Si_{0.5}Ge_{0.5}$-Ge-Si core-double-shell *p*-type and *n*-type MOSFETs, respectively.

Linear fits (lines) to the experimental data (symbols) are included. Inset: hole and electron μ_{eff} vs. $|V_G - V_T|$ for the same devices presented in panels (a-d). Figure 4.9: continued.

cm^2/V·s for holes and electrons, respectively. The μ_{eff} vs. $|V_G - V_T|$ data at $T = 77$ K is also included, showing an enhanced peak value of 1100 cm^2/V·s for holes, but also a degraded peak value of 50 cm^2/V·s for electrons. We have extracted the μ_{eff} values at $T = 300$ K from 25 devices of each type of n-type and p-type MOSFETs, including both $Si_{0.5}Ge_{0.5}$-Ge-Si core-double-shell nanowire devices and Si nanowire control devices. We find the mean values of μ_{eff} of $Si_{0.5}Ge_{0.5}$-Ge-Si core-double-shell nanowire devices show a 500% increase for holes and 20% increase for electrons. We note here that a non-optimized gate stack as evidenced by a reduced electron mobility at $T = 77$ K will reduce the electron mobility in both our Si and $Si_{0.5}Ge_{0.5}$-Ge-Si core-double-shell nanowire n-type MOSFETs, and offset in part the mobility gain through strained Si. On the other hand, the buried strained Ge channel is isolated from the device surface and therefore less impacted by the non-ideal dielectric and dielectric/channel interface, hence a more significant hole mobility enhancement is realized. Particularly noteworthy, previous studies indicate a uniaxial strain and channel direction along <110> orientation are most desirable for hole mobility enhancement in compressive strained Ge [119] and electron mobility enhancement in tensile strained Si [106]. This <110> direction coincides with the thermodynamically favorable growth direction of small diameter VLS Si/Ge nanowires [38], as discussed in Section 2.2.

4.6 Band alignment between the Ge and Si shell in $Si_{0.5}Ge_{0.5}$-Ge-Si core-double-shell nanowires

Next, we will discuss the band alignment between the Ge and Si shell, which controls the carrier confinement in the respective region. The band offset in Si-Ge based radial nanowire

heterostructures is expected to depend on strain, similar to planar heterostructures, where the valence band offset (ΔE_V) varies by 0.6 eV from strained Si grown on relaxed Ge to strained Ge grown on relaxed Si [120, 121]. ΔE_V in $Si_{0.5}Ge_{0.5}$-Ge-Si core-double-shell nanowires can be extracted utilizing a decoupled hole transport through the two shells in a p-type MOSFET [122]. At moderate gate bias the holes will first populate the Ge shell due to a positive $\Delta E_V = E_{V,Ge} - E_{V,Si}$ and $E_{V,Ge} - E_{V,Si_{0.5}Ge_{0.5}}$, while at sufficiently strong inversion will populate the Si shell. The hole mobility in the compressively strained Ge shell is expected to be higher than that in the tensile strained Si shell [109]. As a result, there will be a μ_{eff} reduction and a corresponding change in the device transfer characteristics at the onset of this transition. Figure 4.10(a) shows a comparison of the $I_D - V_G$ data measured at $T = 300$ K and 77 K for the same p-type $Si_{0.5}Ge_{0.5}$-Ge-Si core-double-shell nanowire MOSFET. A clear kink in $I_D - V_G$ data is observed at $T = 77$ K, corresponding to a V_G value (V_{kink}) where holes start to populate the lower mobility Si shell, and μ_{eff} reaches its peak value [Fig. 4.9(e) inset]. Figure 4.10(b) presents a sequence of $I_D - V_G$ data simulated assuming different values of ΔE_V between the Ge and Si shell. The kink is reproduced by introducing different hole mobility values in the two regions. Details of the simulation will be presented in Section 4.8. The inset shows the simulated ΔE_V (symbols) as a function of $|V_{kink} - V_T|$, linear fits (solid lines) are also included. By comparing the experimental data with simulations, we extract $\Delta E_V = 250 \pm 30$ meV for the $Si_{0.5}Ge_{0.5}$-Ge-Si core-double-shell nanowires. Given the valence band alignment, we estimate the conduction band offset $E_{C,Ge} - E_{C,Si} = 120 \pm 30$ meV, with the dependence of the Si/Ge bandgap on strain and quantum confinement factored in [82, 97, 123]. The calculation procedure is as follows. As shown in Fig. 4.6(b), $\varepsilon_{xx} = \varepsilon_{zz}$ for the $[\bar{1}01]$ oriented nanowire, we therefore approximate the strain profile in our $Si_{0.5}Ge_{0.5}$-Ge-Si core-double-shell nanowires as a uniaxial strain along the <110> direction.

We then apply the corresponding secular equation to calculate the strain-induced split (zero net shift) of the valence band energy for each meshing node of both the Ge and Si shell regions [124]:

$$\begin{vmatrix} \frac{1}{3}\Delta_0 - \delta E_V - \frac{1}{8}(\delta E_{001} + 3\delta E_{111}) & -\frac{\sqrt{3}}{8}(\delta E_{001} - \delta E_{111}) & \frac{\sqrt{6}}{8}(\delta E_{001} - \delta E_{111}) \\ -\frac{\sqrt{3}}{8}(\delta E_{001} - \delta E_{111}) & \frac{1}{3}\Delta_0 - \delta E_V + \frac{1}{8}(\delta E_{001} + 3\delta E_{111}) & \frac{\sqrt{2}}{8}(\delta E_{001} + 3\delta E_{111}) \\ \frac{\sqrt{6}}{8}(\delta E_{001} - \delta E_{111}) & \frac{\sqrt{2}}{8}(\delta E_{001} + 3\delta E_{111}) & -\frac{2}{3}\Delta_0 - \delta E_V \end{vmatrix} = 0 \tag{4.1}$$

where the splitting energies $\delta E_{001} = 4b_1(\varepsilon_{xx} - \varepsilon_{yy})$ and $\delta E_{111} = -(4/\sqrt{3})b_2\varepsilon_{xz}$ [120]; b_1 and b_2 are the deformation potentials of either Si or Ge. The three eigenvalues δE_V are the energies of the heavy hole, light hole and split-off band under the strain-induced split, respectively, where the spin-orbital split-off energy Δ_0 is 0.044 and 0.29 eV for Si and Ge. The reference energy level, i.e. 0 eV, is the average valence band energy. The nodal strain tensor used is the simulated value of a $Si_{0.5}Ge_{0.5}$-Ge-Si core-double-shell nanowire with $d \approx 40$ nm. We also have a change in the energy gap between the average energy of the conduction and valence bands due to hydrostatic strain, which can be calculated as $\Delta E_{g,av} = \left(\Xi_d + \frac{1}{3}\Xi_u - a\right)^i \cdot Tr(\boldsymbol{\varepsilon})$, where $\left(\Xi_d + \frac{1}{3}\Xi_u - a\right)^i$ is the deformation potential of Δ and L valleys for Si and Ge. We then calculate the average energy of the conduction band valleys under strain as $E_{C,av} = E_{g0} + \frac{1}{3}\Delta_0 + \Delta E_{g,av}$ for the two shell regions; E_{g0} is the unstrained bandgap of Si or Ge, whose value used is 1.22 or 0.81 eV, respectively, accounting for the bandgap increase in presence of a quantum confinement along the nanowire radial direction [123]. Lastly, the strain-induced energy shift and split of the conduction band valleys are calculated using Eq. (3.1) for the six Δ and eight L valleys of the Si and Ge shell,

respectively. We add a constant to the calculated individual Δ (L) valley energy shifts, so that their average value equals the calculated $E_{C,av}$ of the Si (Ge) shell. The value of the strained bandgap is measured between the highest valence band and the lowest conduction band valley for both the Si and Ge shell. Table 4.2 summarizes the deformation potentials of Si and Ge used for the above calculation. Because the individual strain tensor components are non-uniform across the two shell regions, the bandgap value is the geometrical average of all meshing nodes in the respective region. Figure 4.10(c) illustrates the calculated band diagram along a radial slice of the $Si_{0.5}Ge_{0.5}$-Ge-Si core-double-shell nanowire MOSFET at the flat band condition. E_V of the Ge shell and both E_C and E_V of the $Si_{0.5}Ge_{0.5}$ core are the default values of Sentaurus TCAD, the band energy shift due to strain in the $Si_{0.5}Ge_{0.5}$ core is neglected because the carrier transport is through the two shells. We change E_V of the Si shell to be 250 meV lower than that of the Ge shell according to the experimentally extracted ΔE_V value, and then determine E_C of the Si and Ge shell using the calculated bandgaps. The presence of unintentional doping may translate into a V_T shift [122, 125], and it is not expected to change the band offset in the heterostructure. Figure 4.10(d-e) shows the radial dependence of the simulated band energies and charge densities of a $Si_{0.5}Ge_{0.5}$-Ge-Si core-double-shell nanowire MOSFET in *p*-type and *n*-type operation regimes, respectively, using the parameters indicated in Fig. 4.10(c). In Fig. 4.10(d) holes start to accumulate in the Si shell when the gate overdrive voltage exceeds $|V_{kink} - V_T|$ (solid line), compared to the data with a moderate gate bias (dashed line) where holes are fully confined in the Ge shell. On the other hand, electrons are always confined in the Si shell, independent of the gate bias, as shown in Fig. 4.10(e). Consequently, the Ge and Si shells in the $Si_{0.5}Ge_{0.5}$-Ge-Si core-double-shell nanowire form a type-II heterojunction [115], with holes confined in the compressively strained Ge shell and electrons confined in the tensile strained Si shell.

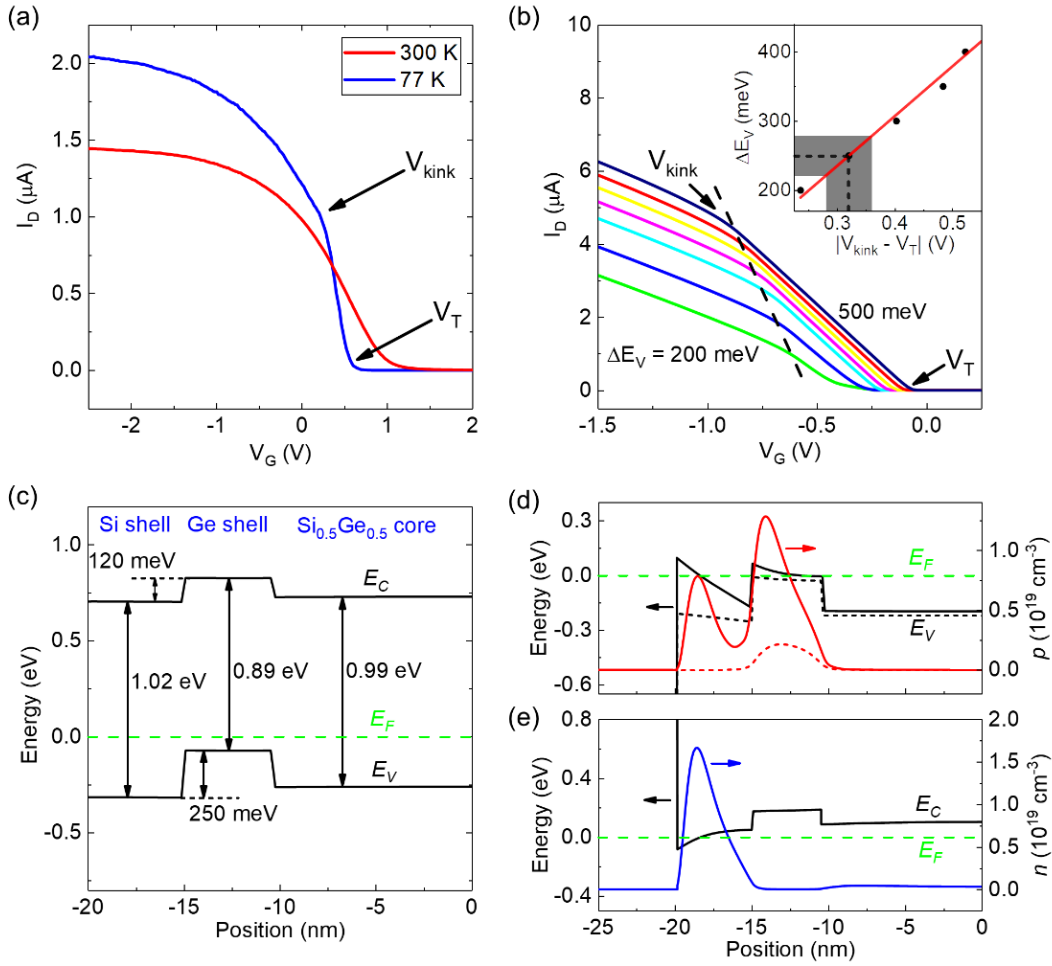

Figure 4.10: Band offset extraction and band diagrams in $Si_{0.5}Ge_{0.5}$-Ge-Si core-double-shell nanowires. (a) Experimental $I_D - V_G$ data of a $Si_{0.5}Ge_{0.5}$-Ge-Si core-double-shell nanowire *p*-type MOSFET with $V_D =$ -50 mV. The red and blue curves represent the data measured at $T = 300$ K and $T = 77$ K, respectively. The V_{kink} and V_T positions at $T = 77$ K are marked. (b) Calculated I_D vs. V_G data assuming different values of ΔE_V. The V_{kink} and V_T positions are marked. Inset: summary of the calculated ΔE_V vs. $|V_{kink} - V_T|$. The range of experimentally extracted $|V_{kink} - V_T|$ and the corresponding ΔE_V values are indicated in grey corridors, and their mean values are marked with dashed lines. (c) Radial dependence of the band diagram under the flat band condition for a MOSFET using $Si_{0.5}Ge_{0.5}$-Ge-Si core-double-shell nanowire heterostructure as channel. Bandgaps, E_F, E_C and the valence band energy (E_V) offsets are shown in the diagram. (d) Radial dependence of E_V and hole density (p) for a *p*-type MOSFET. The solid (dashed) lines represent the data in the regime of $V_G < V_{kink}$ ($V_{kink} < V_G < V_T$). (e) Radial dependence of E_C and electron density (n) for an *n*-type MOSFET.

Table 4.2: Deformation potentials of the Si and Ge shell used in Chapter 4

Materials	b_1 (eV)	b_2 (eV)	$\left(\Xi_d + \frac{1}{3}\Xi_u - a\right)^{\Delta}$ (eV)	$\left(\Xi_d + \frac{1}{3}\Xi_u - a\right)^{L}$ (eV)
Si	-2.33 [126]	-5.30 [126]	0.29 [82]	-3.65 [82]
Ge	-2.16 [126]	-4.65 [126]	-1.90 [82]	-5.17 [82]

4.7 Design and optimization of $Si_{0.5}Ge_{0.5}$-Ge-Si core-double-shell nanowire MOSFETs

Next, we investigate the impact of the Si and Ge shell thickness on the performance of $Si_{0.5}Ge_{0.5}$-Ge-Si core-double-shell nanowire MOSFETs. Table 4.3 summarizes the shell thickness of the three $Si_{0.5}Ge_{0.5}$-Ge-Si core-double-shell nanowire growths discussed in this thesis, namely CDS1, CDS2 and CDS3. Figure 4.11 shows the planar view and cross-sectional TEM imaging data of the CDS1 and CDS3 nanowires. FFTs of the planar view TEM data are included as insets. Same as the CDS2 nanowires, the growth directions of the other two batches of nanowires are also along the <110> direction. It is noteworthy that the FFT data in Fig. 4.11(d) inset shows traces between the diffraction spots perpendicular to the growth axis, suggesting that the CDS3 nanowire has a considerable density of stacking faults, presumably due to its larger shell thickness [127, 128].

Table 4.3: Summary of the Si and Ge shell thickness for $Si_{0.5}Ge_{0.5}$-Ge-Si core-double-shell nanowires

Growth name	Ge shell thickness (nm)	Si shell thickness (nm)
CDS1	3.5	4.5
CDS2	4.5	5
CDS3	6	7.5

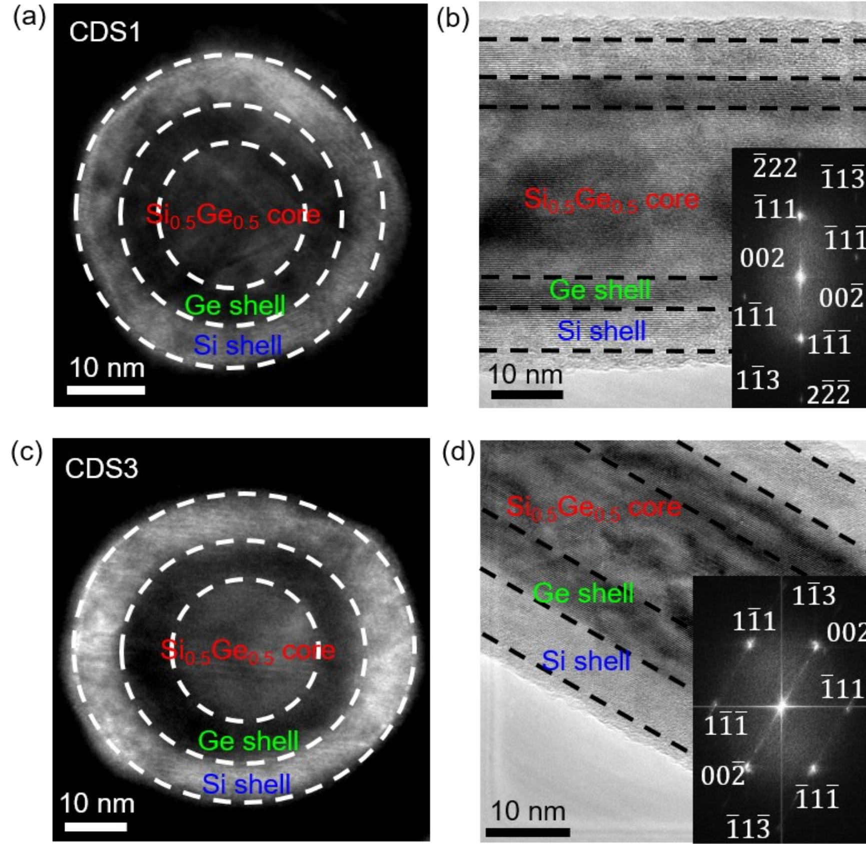

Figure 4.11: (a) Planar view and (b) cross-sectional TEM images of <110> oriented $Si_{0.5}Ge_{0.5}$-Ge-Si core-double-shell nanowires of growth CDS1. (c) Planar and (d) cross-sectional TEM images of <110> oriented $Si_{0.5}Ge_{0.5}$-Ge-Si core-double-shell nanowires of growth CDS3. The interfaces between core and shells are marked for clarity. Insets of panels (b) and (d) are the FFTs of the main panel data.

Figure 4.12 summarizes V_T, μ_{eff} and ε_h for p-type and n-type MOSFETs using $Si_{0.5}Ge_{0.5}$-Ge-Si core-double-shell nanowires as channel for all three growths, along with the Si nanowire (SiNW) MOSFET control devices. Figure 4.12(a) data shows V_T of the p-type MOSFETs. The Si nanowire p-type MOSFET operates in enhancement mode, while the three types of $Si_{0.5}Ge_{0.5}$-Ge-Si core-double-shell nanowire p-type MOSFETs operate in depletion mode. Furthermore, the value of V_T decreases with thinner Si shell, because of a stronger capacitive coupling between the gate and the Ge shell. The strength of the gate electrostatic control can also be visualized by comparing the transfer characteristics of the Si and $Si_{0.5}Ge_{0.5}$-Ge-Si core-double-shell nanowire

MOSFETs. Figure 4.13(a-d) presents the $I_D - V_G$ data measured at room temperature for the Si, CDS1, CDS2 and CDS3 nanowire p-type MOSFETs, respectively. The only surface channel device, which uses the Si nanowire as channel, has the smallest DIBL, SS and leakage current. On the other hand, the buried channel devices using CDS1, CDS2 and CDS3 nanowires as channel demonstrate significantly larger DIBL, SS and leakage current. Moreover, these three figures of merit become poorer when the Si shell thickness increases, indicating more severe short channel effects. Figure 4.12(b) data summarizes V_T of the n-type MOSFETs. No significant difference of V_T is observed among the CDS1, CDS2 and Si nanowire MOSFETs. However, V_T of the CDS3 nanowire MOSFET is considerably higher than the other three. Recalling that the CDS3 nanowire has a large density of defects as identified in Fig. 4.11(d), the increase in V_T can correspond to the extra charge required to fill the defect states in the thicker Si shell. Figure 4.12(c-d) presents the hole and electron field-effect mobility μ_h and μ_e of p-type and n-type MOSFETs, the method to extract μ_e has been detailed in Section 3.6 and also applies to μ_h. As mentioned in Sections 3.6 and 4.5, the non-optimized gate stack will adversely influence the electron mobility in the n-type MOSFETs, and partially offset the mobility gain through the tensile strained Si. Consequently, the mobility enhancement realized in CDS1 and CDS2 devices is not as large as expected for the elastic strain magnitudes. Furthermore, μ_e is much lower in CDS3 than the other three types of n-type MOSFETs, due to the increased scattering from the defects in the Si shell. On the other hand, all three types of $Si_{0.5}Ge_{0.5}$-Ge-Si core-double-shell nanowire MOSFETs have significantly higher μ_h compared to the Si nanowire MOSFET, thanks to the high hole mobility in the compressively strained Ge shell as the buried channel. In addition, thicker Si and Ge shells lead to a larger μ_h enhancement. We attribute this to a combination of a more complete hole confinement in the thicker Ge shell [129], and a reduced scattering from the charged impurities at the dielectric/Si

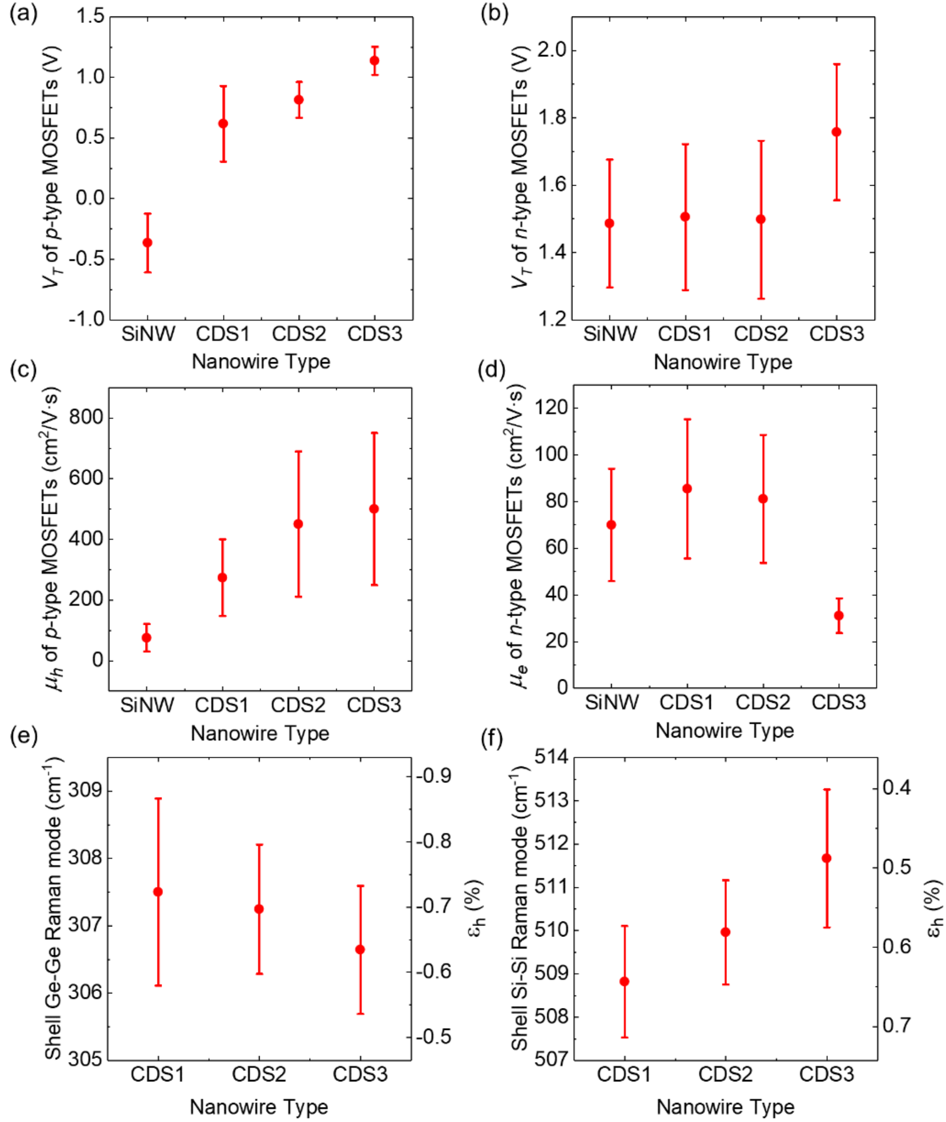

Figure 4.12: Statistical data of Si and three types of $Si_{0.5}Ge_{0.5}$-Ge-Si core-double-shell nanowire MOSFETs. Symbols with error bars represent the mean values and standard deviations. (a-b) V_T of *p*-type and *n*-type $Si_{0.5}Ge_{0.5}$-Ge-Si core-double-shell and Si nanowire MOSFETs. (c-d) μ_h and μ_e of *p*-type and *n*-type $Si_{0.5}Ge_{0.5}$-Ge-Si core-double-shell and Si nanowire MOSFETs. (e-f) Ge-Ge Raman modes of the Ge shell and Si-Si Raman modes of the Si shell acquired from individual $Si_{0.5}Ge_{0.5}$-Ge-Si core-double-shell nanowires, with converted ε_h marked on the right *y*-axis.

interface thanks to a larger spatial separation by the thicker Si shell. Figure 4.12(e-f) shows the Ge-Ge and Si-Si Raman modes and their converted ε_h for the Ge and Si shell respectively, acquired from individual $Si_{0.5}Ge_{0.5}$-Ge-Si core-double-shell nanowires of the three growths. We

find the magnitude of ε_h after partial strain relaxation is larger in the thinner Si and Ge shell. We then summarize the trade-offs for the shell thickness design. A thicker Si shell provides better isolation between the Ge shell and the dielectric/Si interface to benefit the hole transport, but also has larger defect density to hinder the electron transport. A thicker Ge shell can have better confinement of holes, but potentially reduce the hole mobility enhancement due to a lower compressive strain in the Ge shell, and possibly induce the defect formation in the Si shell.

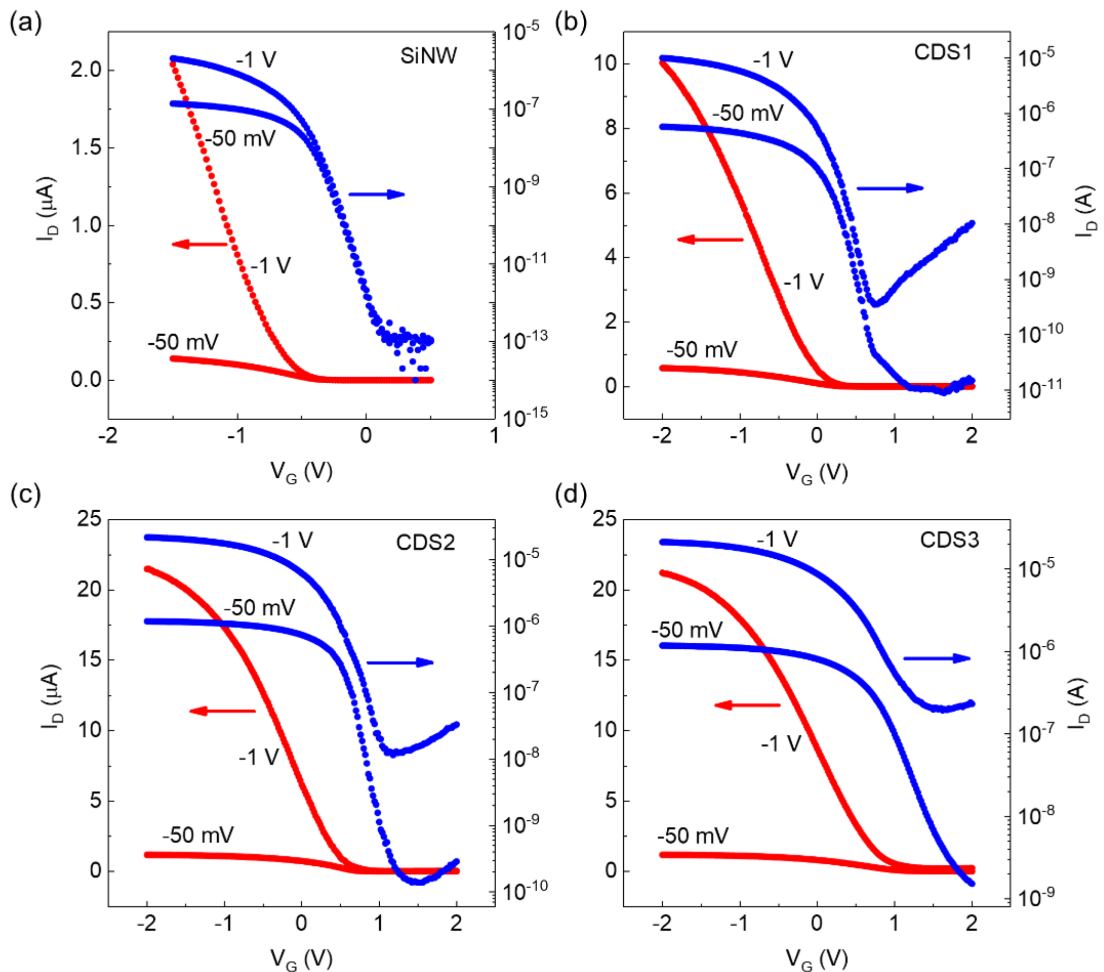

Figure 4.13: Room temperature $I_D - V_G$ data of Si and three types of $Si_{0.5}Ge_{0.5}$-Ge-Si core-double-shell p-type MOSFETs, at V_D = -50 mV and -1 V. (a) SiNW p-type MOSFET (d = 46 nm, L_G = 1760 nm). (b) CDS1 nanowire p-type MOSFET (d = 33 nm, L_G = 1135 nm). (c) CDS2 nanowire p-type MOSFET (d = 37 nm, L_G = 950 nm). (d) CDS3 nanowire p-type MOSFET (d = 45 nm, L_G = 1450 nm).

4.8 μ_{eff} extraction and simulation of charge density and transport

4.8.1 μ_{eff} extraction

R_{Total} of the nanowire MOSFET studied in this chapter is the sum of the intrinsic channel resistance R_{ch}, R_C and R_{ext} of a 1 μm long ungated, doped source/drain extension. The external series resistance $(R_C + R_{ext})$ are determined using data from the scaling properties of R_{Total} vs. L_G presented in Fig 4.9(e-f), same as the method discussed in Section 3.6. The values probed are 21 and 29 kΩ for *p*-type and *n*-type $Si_{0.5}Ge_{0.5}$-Ge-Si core-double-shell nanowire MOSFETs, respectively. We note R_{ext} is the dominant component of $(R_C + R_{ext})$ in these devices, where R_C is lower than 300 Ω as determined from blanket implanted nanowires. We then determined μ_{eff} as a function of $|V_G - V_T|$ using the following equation:

$$\mu_{eff} = \frac{L_{eff}}{R_{ch} C_{\Omega} |V_G - V_T|} \tag{4.2}$$

where $R_{ch} = R_{Total} - (R_C + R_{ext})$, $L_{eff} = L_G - \Delta L$ is the effective channel length, equal to the difference between L_G and the channel length reduction (ΔL) due to dopant ion straddle and diffusion. The ΔL values are determined using data from the *x*-axis intersection point of the linear fits of R_{Total} vs. L_G data at different $|V_G - V_T|$. The ΔL values for the devices probed and discussed in this chapter are approximately 250 nm and 30 nm for *p*-type and *n*-type MOSFETs, respectively. The calculation of C_{Ω} follows the procedure discussed in Section 3.8, using the structure of a two-dimensional Ω-gate cross-section of the device similar to that in Fig. 3.10, with the Si nanowire replaced by a $Si_{0.5}Ge_{0.5}$-Ge-Si core-double-shell nanowire.

4.8.2 Simulation of charge density and transport

Charge density plotted in Fig. 4.10(d-e) is obtained using FEM based on a full quantum

mechanical solution utilizing the density gradient model, which is also part of the approach applied to extract C_Ω. The calculations of the p-type MOSFET $I_D - V_G$ characteristics plotted in Fig. 4.10(b) use a constant hole mobility model with values of 1,000 and 240 $cm^2/V\cdot s$ for the Ge and Si shell region, respectively. It should be noted the mobility values used in the simulation are inconsequential as long as the hole mobility in the Ge region is greater than that in the Si region, since the parameter of interest, $|V_{kink} - V_T|$ is constant over a wide range of mobility values. Ideally, the simulation structure of a three-dimensional Ω-gated nanowire MOSFET should be constructed to replicate the real device geometry. However, due to the limitation of the computation resource and storage space, we use a GAA nanowire MOSFET geometry instead, which can be reduced to a two-dimensional simulation problem. Figure 4.14 shows the schematic of the simulation structure used to calculate the $I_D - V_G$ data of a p-type $Si_{0.5}Ge_{0.5}$-Ge-Si core-double-shell nanowire MOSFET. $R_C + R_{ext} = 0\ \Omega$ is implicitly assumed, since the source and drain electrodes are attached directly to the nanowire cross-section to eliminate any ungated channel extension.

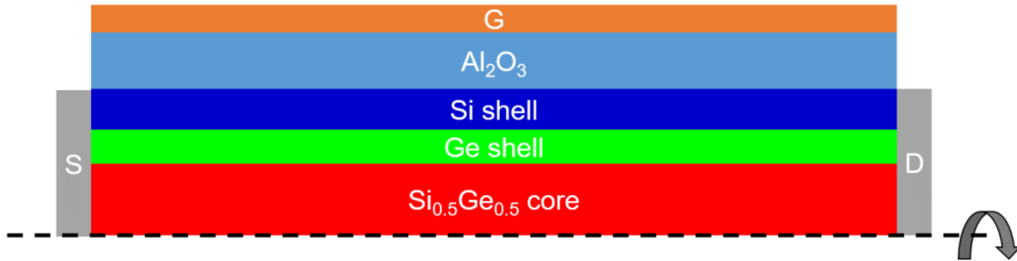

Figure 4.14: Schematic of the simulation structure used to calculate the transfer characteristics of a p-type $Si_{0.5}Ge_{0.5}$-Ge-Si core-double-shell nanowire MOSFET. To calculate the output data, the solver will construct a GAA device geometry by rotating this device slice along the axis marked by the dashed line.

4.9 Summary

In summary, we present the growth of strained $Si_{0.5}Ge_{0.5}$-Ge-Si core-double-shell

nanowires without significant dislocation defects and perform structural and electrical characterization of them. The Ge (Si) shell layer possesses large compressive (tensile) strain to benefit the hole (electron) transport. We demonstrate the device operation of both p-type and n-type MOSFETs, with superior carrier transport properties compared to the Si control devices. We also observe the decoupled hole transport in Ge and Si shell regions with a clear kink in the $I_D - V_G$ data at $T = 77$ K, which marks the onset of holes populating the Si shell from the preferred location in the Ge shell under a moderate gate bias. This experimental observation in combined with the FEM simulation of the hole transport allows us to determine the band offsets and confirm the hole (electron) confinement in the Ge (Si) shell. We also discuss the design and optimization of the $Si_{0.5}Ge_{0.5}$-Ge-Si core-double-shell nanowire by characterizing nanowires with various Si and Ge shell thickness. The Si_xGe_{1-x}-Ge-Si core-double-shell nanowire represents a promising platform for novel CMOS technology, which allows the simultaneous spatial confinement and mobility enhancement of both holes and electrons. It can also improve the mobility symmetry between electrons and holes, by optimizing the growth condition and tuning the Si_xGe_{1-x} core composition as well as the Si and/or Ge shell thickness [114].

Chapter 5 : Compact Modeling and Simulation of JJ-FETs for Cryogenic Boolean Logic Applications[4]

5.1 Introduction

JJ-FETs share design similarities with MOSFETs, except for the source and drain contacts replaced by superconductors. Similarly, I_C thanks to proximity effect is tunable through field effect by changing V_G. The integration of superconducting materials also allows lossless transmission of the electrical signal. In light of recent advances in novel materials and fabrication techniques, we examine here the feasibility of JJ-FET-based Boolean logic and memory elements for cryogenic computing. Using a two-dimensional ballistic transport JJ-FET model, we implement circuit level simulations for JJ-FET logic gates, and discuss the criteria for realizing signal restoration, as well as fan-out. We show that the JJ-FET is a promising candidate for very low power, clocked voltage-level dynamic logic at cryogenic temperatures.

The chapter organization is as follows. In Section 5.2, we discuss the basic concepts of superconductivity, Josephson effect and the model to describe a JJ. In Section 5.3, we discuss the scaling of V_{DD} to break even the cooling cost for cryogenic computing. Section 5.4 presents the short ballistic model to describe the carrier transport in a JJ-FET. Section 5.5 shows the operation and design of the JJ-FET logic gate and memory. In Section 5.6, we discuss the impact of

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[4] Part of this chapter was published previously: [130] F. Wen, J. Shabani, and E. Tutuc, "Josephson Junction Field-Effect Transistors for Boolean Logic Cryogenic Applications," *IEEE Transactions on Electron Devices,* vol. 66, pp. 5367-5374, 2019.

F. Wen and E. Tutuc developed the analytic model of the device, with assistance from J. Shabani. F. Wen implemented and performed the numerical simulations. F. Wen and E. Tutuc analyzed the data and co-wrote the manuscript. All authors have contributed to and approved the final version of the manuscript.

mesoscopic physics on the operation of JJ-FET logic gates, along with some design considerations and trade-offs. Section 5.7 presents the approach to numerically simulate a JJ or JJ-FET. Section 5.8 summarizes the chapter.

5.2 Superconductivity and Josephson effect

5.2.1 Superconductivity

Superconductivity is the set of physical properties associated with a superconductor material, which expels magnetic flux field completely and whose electrical resistance vanishes below a characteristic critical temperature. Bardeen, Cooper and Schrieffer explained the superconductivity in terms of a macroscopic number of conducting electrons that condense into the same quantum state, known as the BCS theory [131]. The BCS theory assumes that there is an attraction between two electrons brought about by the coupling of electrons to the crystal lattice, which can overcome the Coulomb repulsion to form Cooper pairs. The quantum state of the superconductor is described by the condensate wave function:

$$\Psi = |\Psi| e^{i\varphi_{sc}} \tag{5.1}$$

where φ_{sc} is the macroscopic phase of the superconductor and $|\Psi|^2$ denotes the Cooper pair density.

5.2.2 Josephson effect

The Josephson effect describes that when two superconductors are coupled by a non-superconducting weak link, Cooper pairs may tunnel through and lead to a dissipation-less current flow known as Josephson current (I_J) [132]. The described structure is a JJ. The weak link can be

a thin insulating layer, vacuum, a narrow constriction of the superconductor, a normal metal or a semiconductor. I_J can flow if the weak link is small enough to allow a finite overlap of the Cooper pair wavefunctions from both superconductors. Assume the phases of the wavefunctions of the two superconductors are φ_1 and φ_2, respectively. The magnitude of I_J then depends on the difference between the two phases:

$$I_J = I_C \sin(\varphi_1 - \varphi_2) \tag{5.2}$$

I_C has been introduced as the critical current, which is the maximum current value allowed before dissipation occurs. Meanwhile the voltage drop across the junction is also determined by the phase difference:

$$V = \frac{\hbar}{2e} \cdot \frac{d}{dt}(\varphi_1 - \varphi_2) \tag{5.3}$$

Therefore, the phase difference is constant when there is no voltage drop, and evolves over time if the voltage drop is finite, resulting in an oscillating current.

Equations (5.2) and (5.3) indicate that the phase difference determines the state of a JJ. Electron waves in the normal part are responsible for the transport of phase and charge, and therefore phase coherence is required. The mechanism to transfer the macroscopic quantum phase from the superconductor to the electrons in the normal channel is known as Andreev reflection [133]. Andreev reflection describes a type of particle scattering at the interface between the normal material and superconductor. When a conducting electron hits the interface, it cannot enter the superconductor because there is no single particle state in the superconductor within an energy window of $\mp e\Delta$, where Δ is the superconducting voltage gap and $e\Delta$ is usually viewed as the Cooper pair condensation energy. Instead, the electron is retroreflected as a hole in the normal

conductor and produces a Cooper pair in the superconductor. In Chapters 3 and 4, we have used the same symbol Δ to denote the position of the conduction band minima of Si in the Brillouin zone, while from this chapter Δ is exclusively reserved for the superconductor gap voltage.

5.2.3 RCSJ model

The current through a JJ is a non-linear parametric function of the junction voltage. Figure 5.1 shows an equivalent circuit that can be used to describe most types of JJ. The model is called the Resistively and Capacitively Shunted Junction (RCSJ) model. Here the JJ is shunted by a voltage independent resistor (R) and a capacitor (C). Particularly noteworthy, it reproduces well the dynamics of JJs without needing the microscopic details of current transport across the interface between the normal conductor and the superconductor. Hence, Equation (5.4) is obtained from the conservation of the supplied current I:

$$I = C\frac{dV}{dt} + \frac{V}{R} + I_C \sin(\varphi_1 - \varphi_2) \tag{5.4}$$

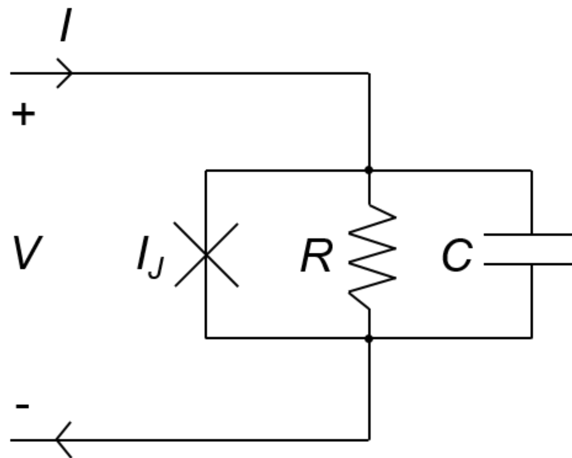

Figure 5.1: Equivalent circuit of the RCSJ model for a JJ, consisting of a voltage independent R, C and the I_J branch.

In the RCSJ model, we have a key parameter that determines the dynamics of the JJ, known as the Stewart-McCumber parameter (Q) [134, 135]. Equation (5.5) gives the expression of Q. Then we can rewrite Eq. (5.4) in the form of Eq. (5.6) after substituting in Eq. (5.3) as well as normalizing $i = I/I_C$ and $\tau = \frac{2e}{\hbar} I_C R t$. Equation (5.6) is similar to the equation describing the movement of a ball bounded in a tilted washer board potential or a pendulum. These two analogies are usually used to explain the RCSJ model in the literature.

$$Q = \frac{2\pi R^2 C I_C}{\Phi_0} \tag{5.5}$$

where Φ_0 is the magnetic flux quantum.

$$i = Q\frac{d^2\varphi}{d\tau^2} + \frac{d\varphi}{d\tau} + I_C \sin\varphi \tag{5.6}$$

where $\varphi = \varphi_1 - \varphi_2$. Generally, either of Eq. (5.4) or (5.6) cannot be solved analytically and we need to perform numerical simulations of a transient analysis. The details of our approach to implement this numerical simulation are presented in Section 5.7. However, in the special case where C and thus $Q = 0$, we can integrate the equation directly and take the time average of V. This leads to the static $I - V$ characteristics of a JJ:

$$V = \begin{cases} R\sqrt{I^2 - I_C^2} & (I > I_C) \\ 0 & (I < I_C) \end{cases} \tag{5.7}$$

In the more complex situation where we cannot neglect Q, the JJ will show hysteresis. That is, if the biasing current through the JJ is increased from 0 A, the JJ will become resistive and have a finite voltage drop across the two terminals when the current exceeds I_C. However, when the

current is decreased again, the JJ will return to the superconducting state at a biasing current smaller than I_C, knows as the return current I_R. Figure 5.2 summarizes the $I - V$ characteristics of the RCSJ model for a JJ with different Q values. In the two extreme cases: if $Q = 0$, the JJ is free of hysteresis, namely $I_R = I_C$; if $Q = \infty$, the JJ cannot return to the superconducting state unless the biasing current is completely removed, namely $I_R = 0$ A.

We have two time constants associated with a JJ, the first one is the RC time constant $\tau_{RC} = RC$ and the second one is the Josephson time constant $\tau_{RL} = L_C/R$, where L_C is the Josephson inductance that equals $\hbar/2eI_C$. We then have a different expression of $Q = \tau_{RC}/\tau_{RL}$. Hence, the distinct behavior of a JJ, whether hysteretic or not, is also determined by the relative magnitude of the two time constants. A JJ is overdamped (underdamped) if $Q \ll 1$ ($Q \gg 1$), whose switching speed between the resistive and superconducting state is determined by τ_{RL} (τ_{RC}) and shows non-hysteretic (hysteretic) $I - V$ characteristics.

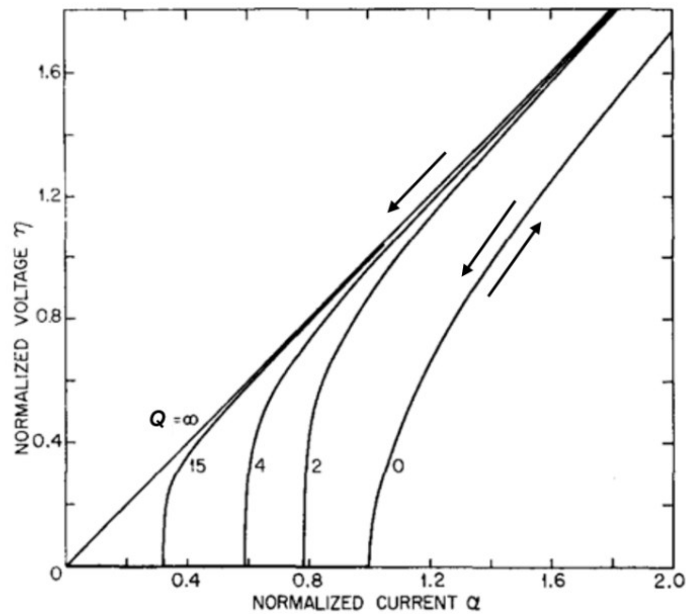

Figure 5.2: $I - V$ characteristics for the RCSJ model with different Q. (Figure adapted from Ref. [135])

5.3 V_{DD} scaling at cryogenic temperatures

As discussed in Section 1.6, reducing temperatures improves several key device metrics of MOSFETs. Examples include enhanced carrier mobility and reduced SS. Channel injection efficiency can also be improved in the absence of phonon scattering [136], and the resistance of metal interconnects is expected to decrease at lower temperatures. It is therefore important to investigate under what conditions cryogenic computing provides a net benefit in terms of dissipated energy per switching operation, and whether other devices can offer a benefit in performance at reduced temperatures. For a given technology, with the supply voltage V_{DD}, the energy dissipated per switching operation is $C{V_{DD}}^2/2$, where C represents the device capacitance. Assuming $V_{DD}(T)$ can be reduced at lower T, by requiring that the total energy dissipated per switching operation, including the cooling cost, does not exceed the room temperature value, we arrive at the following energy balance equation:

$$\frac{CV_{DD}(300\ K)^2}{2} = \frac{CV_{DD}(T)^2}{2} + \frac{300\ K - T}{T} \cdot \frac{CV_{DD}(T)^2}{2} \tag{5.8}$$

The second term on the right-hand side of Eq. (5.8) represents the cooling cost at the ideal Carnot efficiency, corresponding to reservoir temperatures of 300 K and T. Equation (5.8) leads to the following simple scaling law for the operating voltage to break even in the ideal cooling limit:

$$V_{DD}(T) = V_{DD}(300\ K)\sqrt{\frac{T}{300\ K}} \tag{5.9}$$

For example, a V_{DD} value of 0.7 V at room temperature will translate to a break-even value of 83 mV at 4.2 K, the liquid He boiling point, which is further reduced to ~26 mV if one factors in

realistic cooling efficiencies of 5-10% [137]. The gate delay associated with load and parasitic capacitance being charged/discharged will scale with reducing V_{DD}, while the transit time delay of channel being switched may not scale down proportionally because of the low Fermi velocity at low carrier concentration and reduced thermal excitation of carriers [138]. The non-scalability of the gate delay has also been discussed in detail in Section 1.6.1. Moreover, injection limited MOSFET current in deeply scaled devices [136], already nearing the ballistic limit of performance, can be expected to have limited temperatures sensitivity. While the above arguments contain a number of simplifications, they clearly indicate that cryogenic computing using CMOS concepts is subject to significant constraints if a net benefit is expected over room-temperature operation with cooling cost factored in. It is therefore highly relevant to examine if other devices operating at, or below the break-even V_{DD} value may be used for cryogenic computing applications.

In the remaining sections of this chapter, we address the feasibility of JJ-FETs for digital applications. We employ a JJ-FET device model that allows gate-controlled ballistic and coherent transport of Cooper pairs through the channel to examine the criteria for signal restoration of several logic gates. We present the results of transient analysis for JJ-FET logic gates, evaluate the impact of fan-out on the device behavior and discuss various design considerations.

5.4 Device model of the JJ-FET

We begin by introducing a device model for the JJ-FET. The device, schematically represented in Fig. 5.3, has the following key length scales: L_G, the Cooper pair coherence length ξ_0, and the Cooper pair mean free path λ. Depending on the interplay between L_G, ξ_0 and λ, the JJ can operate in either short or long ballistic, or diffusive regimes. The JJ is short if $L_G < \xi_0$, or long if $L_G > \xi_0$. The Cooper pair transport is ballistic if $L_G < \lambda$, or diffusive if $L_G > \lambda$.

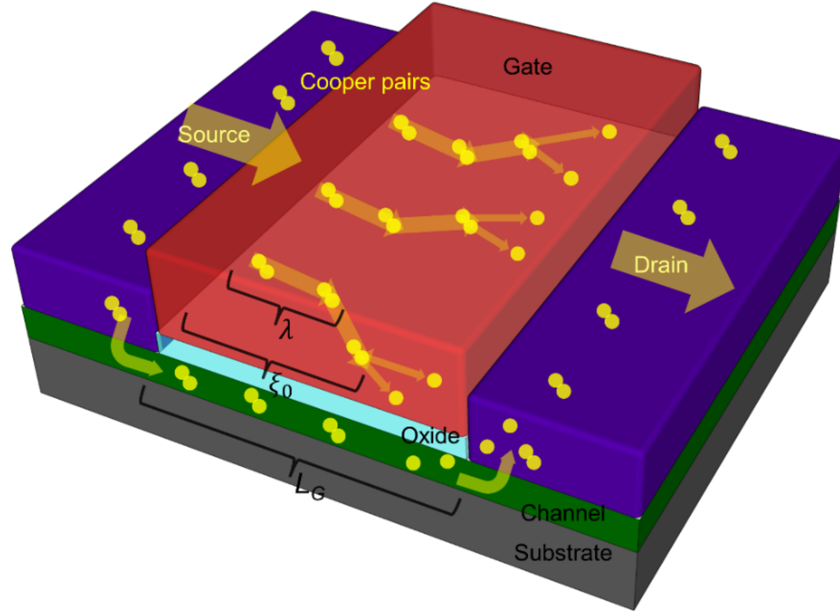

Figure 5.3: Schematic of a JJ-FET, consisting of the superconducting source and drain, metal gate, gate oxide, semiconductor channel, and an insulating substrate. The length scales L_G, ξ_0, and λ are indicated. The scattering or destruction of Cooper pairs will occur if L_G is greater than λ or ξ_0, respectively, as shown in the figure. The arrows indicate the directions of the Cooper pair or electron motion.

We consider here the case of a short ballistic JJ device, which satisfies the Ambegaokar-Baratoff formula [139]:

$$V_0 = I_C \cdot R_N = \pi\Delta \tag{5.10}$$

where V_0 is the characteristic voltage, and R_N the normal resistance of the JJ-FET. The normal state conductance of a two-dimensional ballistic transport layer divided by the average velocity along the channel direction is:

$$G_N = W \cdot \frac{2e^2}{h} \cdot \frac{2}{\pi} \cdot \sqrt{2\pi n_{2D}} \tag{5.11}$$

where W is the device width, h is Planck constant, and n_{2D} is the two-dimensional carrier density. The carrier density can be related to the gate capacitance per unit area C_G and V_G via $n_{2D} = C_G(V_G - V_T)/e$. Using Eqs. (5.10) and (5.11):

$$I_C = G_N \cdot V_0 = 2V_0 W \cdot \frac{2e}{h} \cdot \sqrt{\frac{2eC_G(V_G - V_T)}{\pi}} \tag{5.12}$$

It is instructive to introduce an equivalent transconductance for the I_C dependence on V_G as:

$$\beta = \frac{dI_C}{dV_G} = V_0 \frac{dG_N}{dV_G} = V_0 W \cdot \frac{2e}{h} \cdot \sqrt{\frac{2eC_G}{\pi(V_G - V_T)}} \tag{5.13}$$

If we assume the device is in the overdamped limit with $Q = 0$, where the $I - V$ characteristics are non-hysteretic [134, 135], the static $I - V$ characteristics are relatively simple and similar to Eq. (5.7):

$$V_{DS} = \begin{cases} R_N \sqrt{I_{DS}^2 - I_C^2} & (I_{DS} > I_C) \\ 0 & (I_{DS} < I_C) \end{cases} \tag{5.14}$$

where V_{DS} is the voltage drop across the drain and source contacts, and I_{DS} is the drain current. Because Nb and Al are two commonly used superconductors [18, 140], we consider here the cases where the source/drains consist of either Nb or Al, with Δ values of 1.5 mV or 0.22 mV, respectively [141]. Figure 5.4 shows the static $I - V$ characteristics of JJ-FETs with the two types of superconductor metal contacts, assuming an effective oxide thickness (EOT) of 1 nm and $W =$ 1 µm.

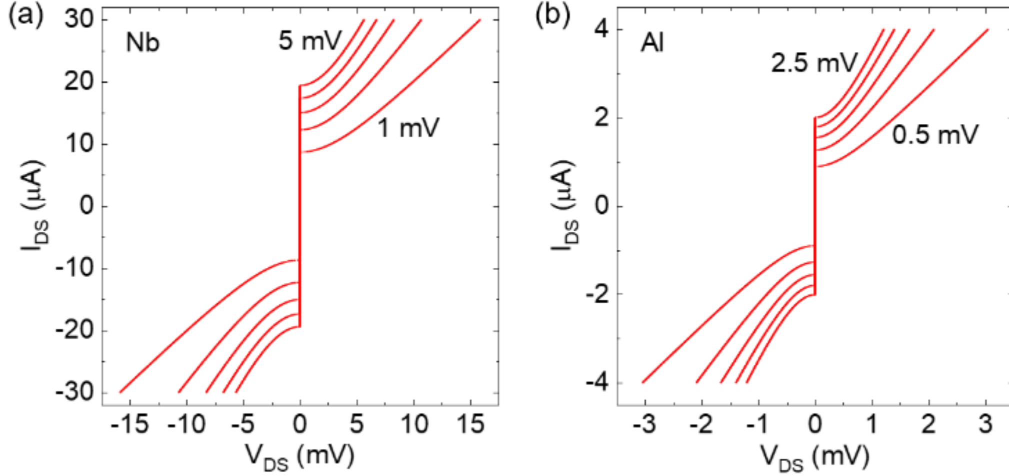

Figure 5.4: Calculated $I - V$ characteristics for JJ-FETs with $W = 1$ μm, effective SiO_2 oxide thickness of 1 nm ($C_G = 3.45$ μF/cm^2) using (a) Nb and (b) Al contacts. The $V_G - V_T$ values indicated in the figure are changed in 1 mV [panel (a)], and 0.5 mV [panel (b)] increments.

A critical question for a logic gate is if the output voltage is sufficiently large to switch the next stage, since transistors are cascaded to perform complex logic operations. To address this question, we assume the output of one JJ-FET is directly driving the gate of a second JJ-FET, whose I_C value, in turn needs to be sufficiently modulated for a switch. Equation (5.14) indicates that V_{DS} will be of the order of V_0 if I_{DS} is comparable to I_C [19]. The relative change in I_C corresponding to a gate swing of V_0 is [142]:

$$\alpha_R = \frac{\beta V_0}{I_C} = \frac{V_0}{2(V_G - V_T)} \tag{5.15}$$

To achieve signal restoration with $\alpha_R \sim 1$, $V_G - V_T$ needs to be comparable to V_0. This is an intrinsic requirement of short ballistic JJ-FET logic gates, independent of the device scaling and geometry. Figure 5.5 shows the plots of α_R against $V_G - V_T$ for both the Nb- and Al-contact JJ-FET.

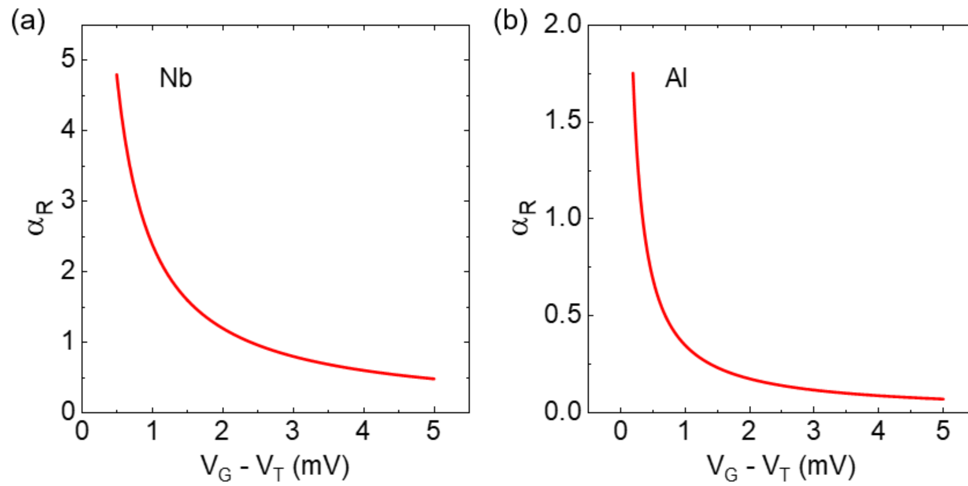

Figure 5.5: Calculated α_R vs. $V_G - V_T$ for the (a) Nb- and (b) Al-contact JJ-FET.

5.5 JJ-FET logic gate and memory

5.5.1 Static analysis

In this section, we consider logic gates based on JJ-FETs. Figure 5.6(a-c) illustrates the schematics of the JJ-FET inverter, NOR gate and static-random-access-memory (SRAM), respectively. A NOR gate is universal and can be the building block for any combinatorial logic circuit. In this study, we assume all logic devices are biased with ideal DC current (I_{Bias}) sources for simplicity. The logic gates operate as follows. For a JJ-FET inverter [Fig. 5.6(a)], when the input voltage at the gate (V_{IN}) is at logic low ($V_{G,Lo}$), the corresponding $I_C < I_{Bias}$, and the JJ-FET is resistive, leading to a finite V_{OUT}. On the other hand, when V_{IN} is at logic high ($V_{G,Hi}$), the corresponding $I_C > I_{Bias}$, the JJ-FET is superconducting, and V_{OUT} is zero. Consequently, we have $V_{G,Lo} = 0$ since the JJ-FETs are cascaded in logic circuits. Signal restoration indicates the finite V_{OUT} at $V_{IN} = V_{G,Lo}$ at least equal to $V_{G,Hi}$ to drive the input of the next stage, i.e. same input/output swing. Similarly, in a JJ-FET NOR gate [Fig. 5.6(b)], the sum of I_C of the two JJ-FETs is smaller

than I_{Bias} only when both inputs are at logic low, leading to a finite V_{OUT}, and zero otherwise. Connecting two JJ-FET inverters back to back yields an SRAM cell [Fig. 5.6(c)], where V_1 and V_2 will reach a stable state of complementary values.

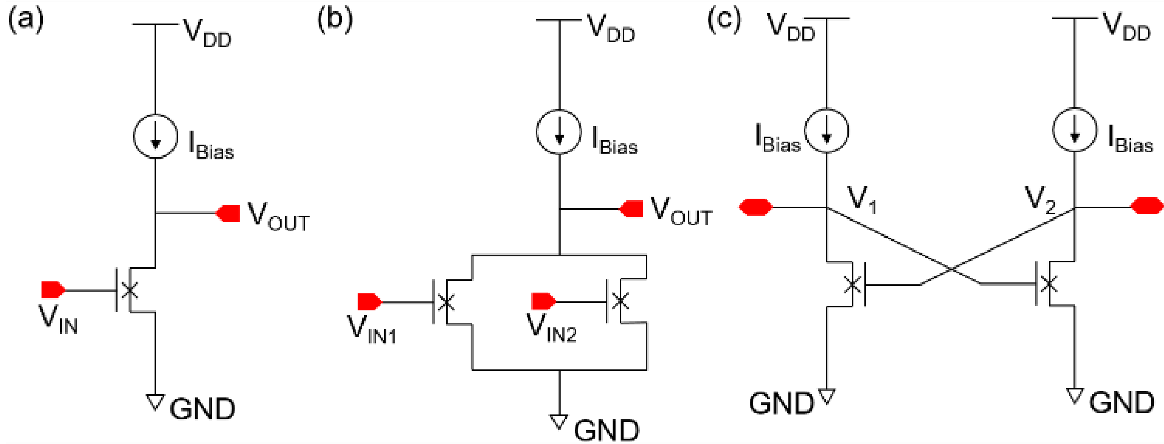

Figure 5.6: Schematics of the JJ-FET (a) inverter, (b) NOR gate and (c) SRAM.

Next, we design the JJ-FET inverter using the static model and investigate its performance, ignoring any parasitic capacitance and resistance of the JJ-FET itself. Though this model may be oversimplified, it sheds lights on the DC operating point, i.e. the V_T and I_{Bias} values that will produce the same input/output swing, namely $V_{G,Hi} = V_{OUT}(V_{G,Lo}) = R_N(V_{G,Lo}) \cdot \sqrt{(I_{Bias}^2 - I_C^2\ (V_{G,Lo}))}$ and an optimal power or speed; the variables in parentheses denote the V_{IN} values. We can estimate the power consumption of the JJ-FET as $\propto I_{Bias}V_{G,Hi}$. Hypothetically, we could have an arbitrarily small swing and thus power consumption by choosing I_{Bias} close to $I_C(V_{G,Lo})$. We could also have an arbitrarily large swing since $R_N(V_{G,Lo})$ diverges when V_T approaches zero. Hence, for any given swing we have a solution to the bias point by appropriately choosing V_T and I_{Bias}, albeit with trade-offs. Therefore, we chose to design the biasing point of the logic gates based on speed.

The rising delay (t_r) is not expected to be reduced compared to that of the traditional counterpart, e.g. an NMOS inverter, because when V_{IN} switches to low the JJ-FET becomes resistive instead of being cut-off. Moreover, the JJ-FET draws additional current to the resistive component, namely I_J, effectively further slowing down the charging speed at the output node. On the other hand, I_J will assist to discharge the output node when V_{IN} switches to high. The falling delay (t_f) is therefore smaller than that of an NMOS inverter, and more importantly, the superconducting JJ-FET can fully discharge the output. Figure 5.7(a) presents the plot of minimum total delay τ_{min} as a function of $|V_T|$ for an Nb-contact JJ-FET inverter. The device has the same geometry as that assumed in Fig. 5.4 and an output capacitance $C_L = 10$ fF, chosen as fan-out of four plus interconnect capacitance. For reference, the gate capacitance of a JJ-FET with $W = 1$ μm and $L_G = 50$ nm is 1.7 fF. We note the actual value of C_L is insignificant to demonstrate the logic operation here, since the characteristics of JJ-FET logic gates using the static $I - V$ model will not change with C_L, except for the delay to scale linearly. For a fixed V_T, a given $I_{Bias} > I_C(V_{G,Lo})$ decides $V_{OUT}(V_{G,Lo})$ and therefore the output swing. Meanwhile, I_{Bias} cannot exceed $I_C(V_{OUT}(V_{G,Lo}))$ so there is a matched input swing. Hence, we have multiple solutions of various I_{Bias} to the bias point at each V_T. We first determine those quiescent points, then extract t_r and t_f for individual points from a set of transient analysis, and finally obtain τ_{min} at that V_T as the minimum of $(t_r + t_f)$ among those points. Effectively the curve in Fig. 5.7(a) is the projection of a trace along the contour plot for $(t_r + t_f)$ against V_T and I_{Bias}. We find that τ_{min} reaches a global minimum at $V_T \approx$ -0.8Δ, where the V_{IN} swing is ≈ 4Δ. Using this biasing point, an example of transient analysis for the Nb-contact JJ-FET inverter is shown in Fig. 5.7(b). It is clear that the falling edge of V_{OUT} is more linear than exponential, compared to the rising edge, thanks to I_J, which remains ~I_C and does not linearly decrease with V_{OUT} as the resistive counterpart. The t_r

and t_f values are 6.4 and 2 ps in this case. Similarly, a NOR gate can be constructed by simply doubling I_{Bias} since $2I_{Bias} < I_C(V_{G,Hi}) + I_C(V_{G,Lo})$.

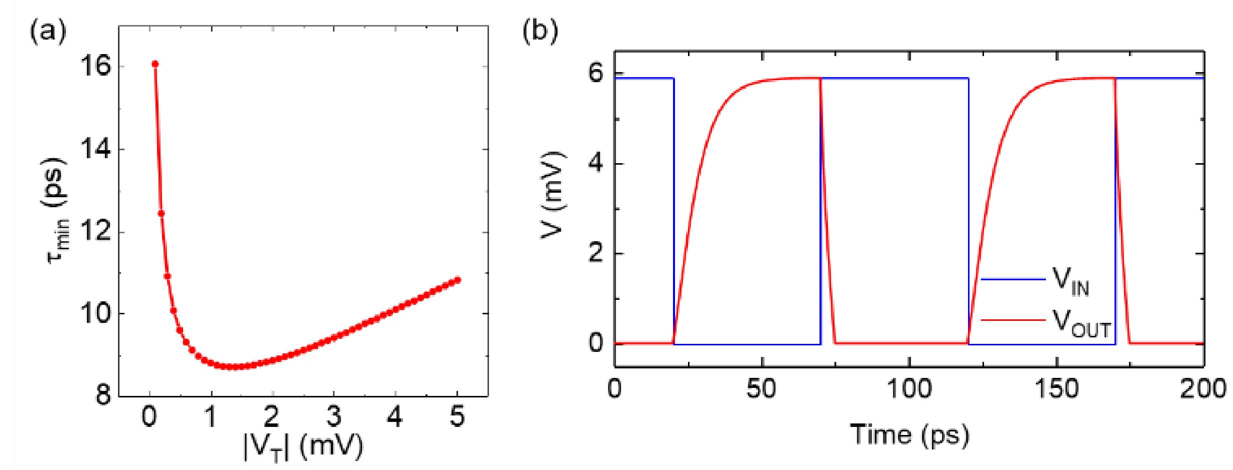

Figure 5.7: (a) $\tau_{min} = min(t_r + t_f)$ among biasing points with their respective equal input/output swing at each $|V_T|$. (b) Transient analysis result with minimum τ_{min} using the following set of parameters: Swing of input/output = 5.9 mV, W = 1 μm, V_T = -1.2 mV, I_{Bias} = 15.1 μA. The superconducting contacts are Nb.

Applying the same set of parameters for the Nb-contact JJ-FET inverter in Fig. 5.7(b), Figure 5.8(a) shows the transient response of the output voltages V_1 and V_2 for the two JJ-FET inverters in a SRAM cell. The initial voltage values at the two outputs are associated with the metastable state ($V_1 = V_2 \approx 1.5$ mV). In presence of any disturbance, which is ubiquitous in an actual circuit, the feedback loop will stabilize the two inverters to their respective conditions. The final state is one of the two stable states where V_1 and V_2 have opposite logic values. In this example, the metastable state ends due to a disturbance at 25 ps and the cell reaches the stable state where $V_1 = 5.9$ mV and $V_2 = 0$ mV, representing a bit '1' stored in the cell. Other initial conditions will work as if the disturbance already given. Figure 5.8(b) presents the voltage transfer curves of the two JJ-FETs in the same SRAM cell, with the static noise margin indicated in a dashed-line

box. The intersection of the two curves in the middle indicates the metastable state while the two at the ends represent the stable states, pointed by arrows.

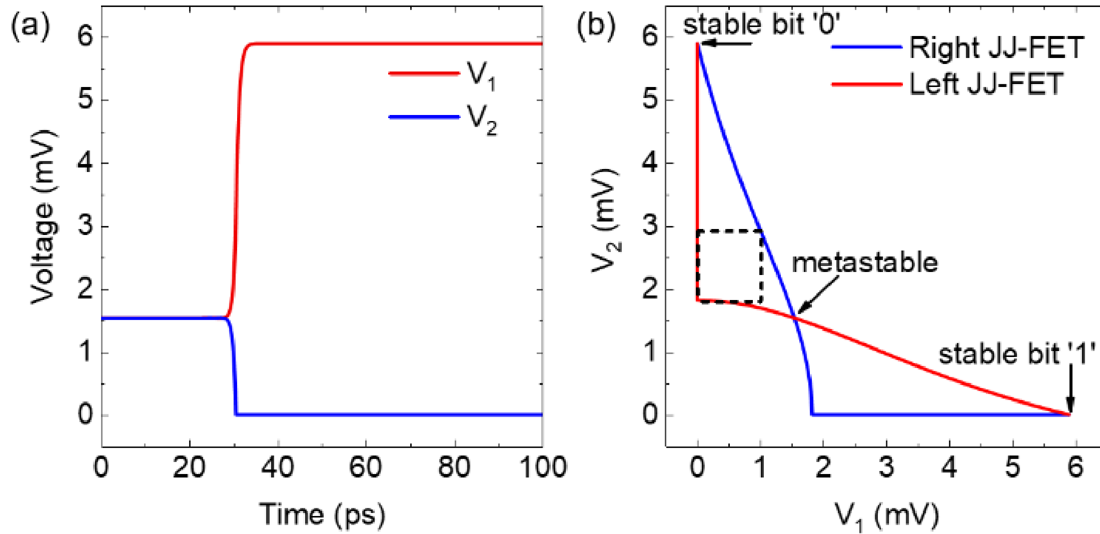

Figure 5.8: (a) Transient response of the node voltages at the outputs of the two JJ-FETs in an SRAM cell. (b) SRAM voltage transfer curves, static noise margin is indicated with a dashed-line-frame box. $C_L = 1$ fF at both outputs. The superconductor contacts are Nb.

5.5.2 Dynamic analysis

Although we can design the DC operating point of JJ-FET logic gates with the static model, we have made a critical assumption that the JJ-FETs are overdamped in the transient analysis. As discussed in Section 5.2.3, if a JJ works in the overdamped regime and carries a current exceeding I_C, it is non-hysteretic and will become superconducting immediately when the current falls below I_C. For an overdamped and resistive JJ-FET, it means the transistor will become superconducting as soon as V_G is increased such that $I_C > I_{DS}$. However, a JJ or JJ-FET is overdamped only when Q is small ($Q \ll 4$) [134, 135]. On the other hand, a JJ becomes underdamped if Q is large, which means it remains in the resistive state even when the junction current is reduced below I_C, leading to $I - V$ hysteresis. The assumption of overdamped operation

becomes questionable if we acknowledge that a logic device has fan-out, and therefore has larger C as well as Q than a single transistor. Moreover, by ignoring L_C, the estimation of gate delay is no longer accurate, as the dominant time constant of an overdamped JJ-FET is $\tau_{RL} = L_C/R_N = \hbar/2\pi e\Delta$. To address these dilemmas, we implement the RCSJ model discussed in Section 5.2.3 to describe the device. The $I-V$ characteristics are controlled by $\varphi(t)$, which is a time-dependent variable representing the macroscopic phase difference between the superconducting source and drain contact:

$$I_{DS}(t) = C\frac{dV_{DS}(t)}{dt} + \frac{V_{DS}(t)}{R} + I_C\sin\varphi(t)$$

$$V_{DS}(t) = \frac{\hbar}{2e}\cdot\frac{d\varphi(t)}{dt} \tag{5.16}$$

We assume the load is purely capacitive and ignore the resistance of the biasing circuitry. Therefore, a JJ-FET inverter's device resistance $R = R_N$ and capacitance $C = C_L + C_J$, where C_J is the junction capacitance assuming the gate capacitance splits symmetrically to the source and drain. The gate-tunable Q for a JJ-FET inverter writes:

$$Q_{inv} = \frac{R^2 C I_C}{\Phi_0/2\pi} = \frac{\pi^{3/2} V_0 \left(C_J + C_L\right)}{\sqrt{2eC_G(V_{IN} - V_T)}} \tag{5.17}$$

where C_J and C_L are normalized to $W = 1$ μm of the active JJ-FET. We have $C_L \propto C_G$ if the output is driving inputs of other JJ-FETs, hence for a JJ-FET logic inverter $Q_{inv} \propto \sqrt{C_G/(V_G - V_T)}$.

We implement the RCSJ model with Verilog-a and perform the simulation in the Cadence Virtuoso environment. Details of the model implementation and the validity test of a JJ's dynamics are presented in Section 5.7. Figure 5.9 presents the results of transient analysis for both Nb- and

Al-contact JJ-FET inverters, with device parameters adapted from the static analysis based on $V_T \approx$ -0.8Δ. Figure 5.9(a-b) shows the input waveforms for the Nb- and Al-contact JJ-FET inverters, respectively. Figure 5.9(c-d) shows the output waveforms for the Nb- and Al-contact JJ-FET inverters with $C_L = 1$ fF. Similarly, the output waveforms for the Nb- and Al-contact JJ-FET inverters with $C_L = 5$ fF are shown in Fig. 5.9(e-f). The values of C_L in the dynamic analysis section are chosen to represent the respective operation regime whether hysteresis will latch the JJ-FET in the resistive state or not. Table 5.1 summarizes the values of Q at $V_{IN} = V_{G,Hi}$ associated with different C_L and zero V_{IN} for both Nb- and Al-contact JJ-FET inverters. Comparing the output waveforms to those using the static model, superimposed oscillations emerge because of the Josephson effect. Similar to a parallel RLC circuit, the amplitude is attenuated by a larger C_L, and the frequency is higher for the Nb-contact device due to a smaller L_C. The Nb-contact JJ-FET inverter is significantly faster than its Al-contact counterpart, e.g. $t_f = 0.25$ and 2.5 ps respectively with $C_L = 1$ fF. The difference in their t_f is comparable to that of their τ_{RL}. If we compare panels (c-d) to (e-f), a distinct difference that can be seen is that the JJ-FET inverter fails to be reset into the superconducting states when V_{IN} switches from zero to high when C_L is increased from 1 to 5 fF. Consequently, the finite Q must be accounted for when designing JJ-FET logic gates to avoid an undefined V_{OUT}. In the simulation, we find $Q \approx 4$ is the critical value for the Nb-contact JJ-FET inverter to be properly reset, and slightly lower for the Al-contact device as $Q \approx 2.5$. The critical value of Q is closely related to the ratio of $I_{Bias}/I_C(V_{G,Hi})$ due to the hysteretic $I - V$ characteristics. This ratio is 0.5 and 0.7 for the parameter set our Nb- and Al-contact JJ-FET inverter assumes, in agreement with the ratio of I_R over I_C corresponding to the critical Q in a hysteretic JJ [135].

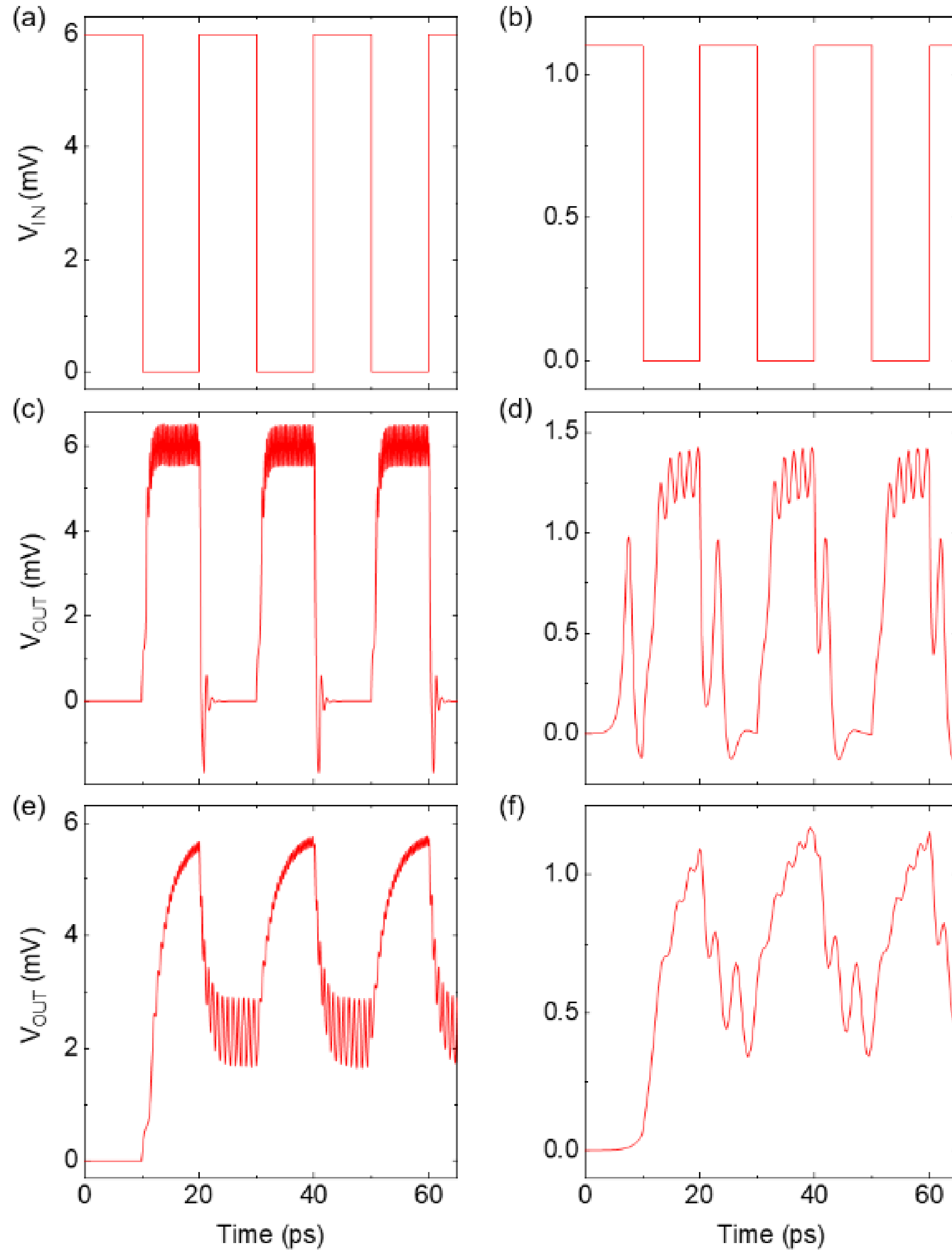

Figure 5.9: Square waveforms of V_{IN} for (a) Nb-contact JJ-FET inverter (0 - 6 mV) and (b) Al-contact JJ-FET inverter (0 - 1.1 mV), with a period of 20 ps. Waveforms of V_{OUT} for (c-d) Nb- and Al-contact JJ-FET inverters with $C_L = 1$ fF and (e-f) $C_L = 5$ fF, respectively. For reference, the gate capacitance is 0.7 fF for $W = 1$ µm and $L_G = 20$ nm. I_{Bias} is slightly reduced to 12 µA from that in the static model for the Nb-contact JJ-FET inverter. I_{Bias} and V_T are 1.06 µA and -0.2 mV for the Al-contact JJ-FET inverter.

Table 5.1: Q of the JJ-FET inverter

Contact and C_L	$V_{IN} - V_T = 1.2\,mV$	$V_{IN} - V_T = 0.2\,mV$
Nb, 1 fF	3.5	N/A
Nb, 5 fF	15.5	N/A
Al, 1 fF	N/A	1.0
Al, 5 fF	N/A	4.4

Similarly, we can write Q for a JJ-FET NOR gate as:

$$Q_{NOR} = \frac{R^2C(I_{C1} + I_{C2})}{\Phi_0/2\pi} = \frac{\pi^{3/2}V_0\left(2C_J + C_L\right)}{\sqrt{2eC_G}\cdot\left(\sqrt{V_{IN1} - V_T} + \sqrt{V_{IN2} - V_T}\right)} \tag{5.18}$$

where I_{C1} and I_{C2} are the critical current of the two JJ-FETs. Figure 5.10 presents the results of transient analysis for JJ-FET NOR gates, with the same device parameters used in the JJ-FET inverters and doubled I_{Bias}. Figure 5.10(a-d) shows the input waveforms for the Nb- and Al-contact JJ-FET NOR gates, respectively. The signal at V_{IN2} has twice the period and is in phase with that at V_{IN1} to enumerate all four possible logic combinations at the inputs. The output waveforms for the Nb- and Al-contact JJ-FET NOR gates are shown in Fig. 5.10(e-f) with $C_L = 1$ fF and Fig. 5.10(g-h) with $C_L = 2.5$ fF. Finally, the output waveforms for the Nb- and Al-contact JJ-FET NOR gates with $C_L = 5$ and 7 fF are shown in panels (i) and (j). Table 5.2 summarizes the values of Q associated with different combinations of V_{IN1}, V_{IN2} and C_L for both Nb- and Al-contact JJ-FET NOR gates. Again, the values of C_L and therefore Q are crucial to determine the behavior of the JJ-FET NOR gates. In Fig. 5.10(e-f), V_{OUT} correctly reproduces the response of a NOR gate, e.g. V_{OUT} only becomes finite when both inputs are low. However, when C_L is increased from 1 to 2.5 fF, V_{OUT} fails to be reset to zero when only one of the inputs switches from low to high and outputs an undefined intermediate state [Fig. 5.10(g-h)]. When C_L is further increased to

5 and 7 fF for the Nb- and Al-contact JJ-FET NOR gates, V_{OUT} remains finite even when both inputs switch to high. Consequently, there are two undefined intermediate states, as shown in Fig. 5.10(i-j).

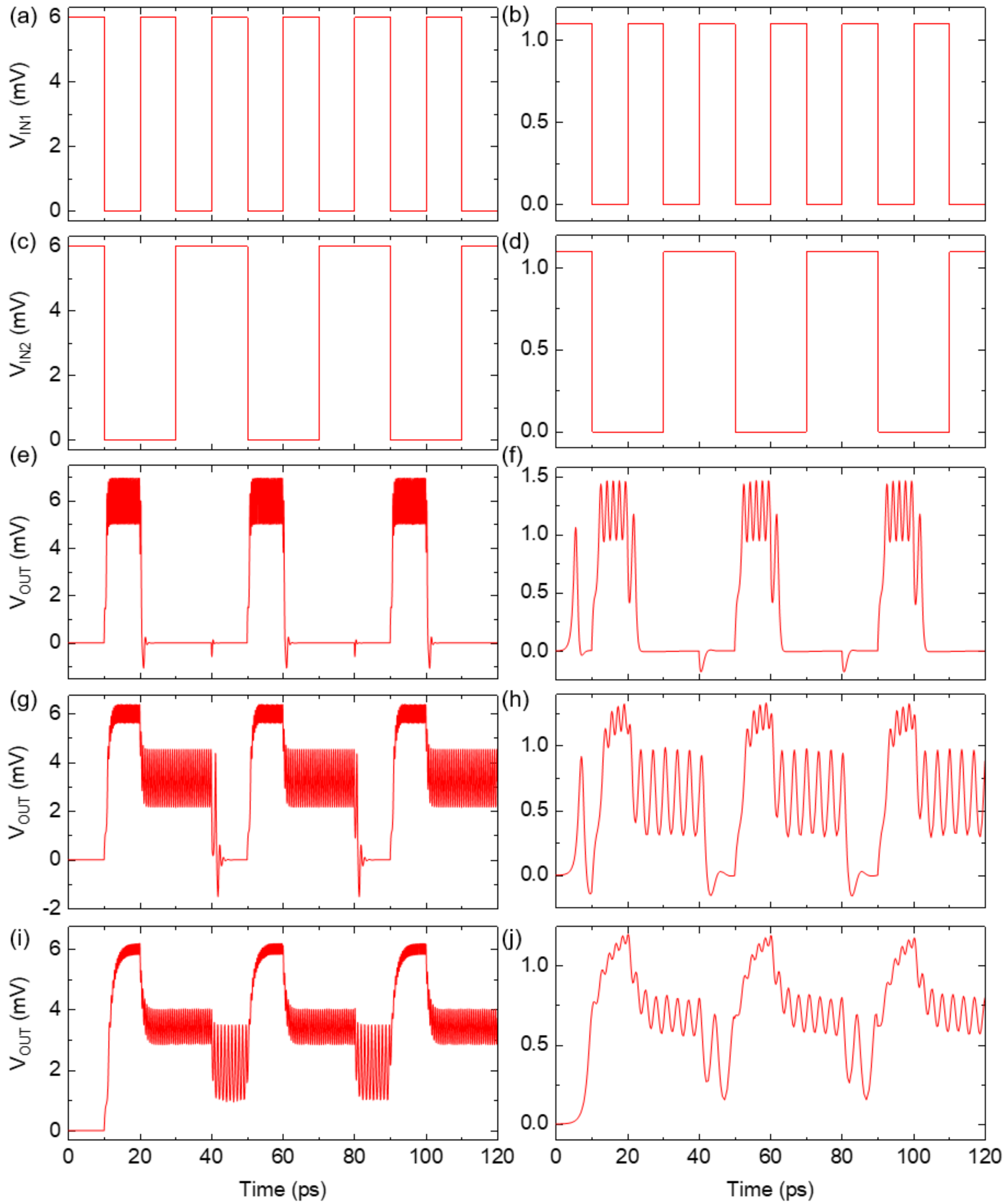

Figure 5.10: Square waveforms of V_{IN1} for the (a) Nb-contact JJ-FET NOR gate (0 - 6 mV) and (b) Al-contact JJ-FET NOR gate (0 - 1.1 mV), with a period of 20 ps. Square waveforms of V_{IN2} for the (c) Nb-

and (d) Al-contact JJ-FET NOR gate, with a period of 40 ps. Waveforms of V_{OUT} for the Nb- and Al-contact JJ-FET NOR gate with (e-f) $C_L = 1$ fF, (g-h) $C_L = 2.5$ fF, (i) $C_L = 5$ fF and (j) $C_L = 7$ fF, respectively. $I_{Bias} = 24$ and 2 μA for the Nb- and Al-contact JJ-FET NOR gates. Figure 5.10: continued.

Table 5.2: Q of JJ-FET NOR gate

Logic values of V_{IN1} and V_{IN2}	00	01 or 10	11
Nb-contact, $C_L = 1$ fF	7.1	2.9	2.0
Nb-contact, $C_L = 2.5$ fF	12.6	6.7	4.3
Nb-contact, $C_L = 5$ fF	21.8	12.0	8.0
Al-contact, $C_L = 1$ fF	2.54	1.0	0.7
Al-contact, $C_L = 2.5$ fF	4.5	2.3	1.5
Al-contact, $C_L = 7$ fF	10.4	5.6	3.8

5.5.3 Global clock to reset underdamped JJ-FETs

In the previous section, we have shown that the $Q = 0$ approximation is not applicable if the fan-out load capacitance is taken into account. The JJ-FETs usually enter the underdamped regime and become hysteretic, at least when inputs are low. On the other hand, JJ-FETs can turn back to overdamped when inputs switch from low to high, thanks to the low Q from an optimized design. In this case, we can harness the unique feature of the superconducting logic device, where t_f is determined by τ_{RL}. Thus, a promising design of JJ-FET logic gate resembles the dynamic logic gate, featuring a pre-charge of V_{OUT} and monotonically rising V_{IN} during evaluation. The JJ-FET logic gate discussed in this chapter belongs to the type of voltage-state JJ logic device. In Section 1.6.2 we have introduced the JJ switching element realized through magnetic coupling or current injection into the channel [19]. Those JJs are underdamped with high Q due to the obsolete fabrication technology and the capacitor device geometry, and require an AC power supply and other circuit elements to isolate the output from the input. An AC power supply is used since in an

underdamped JJ, resetting from the resistive to superconducting state requires the ratio of I_J/I_C to be lowered to a small value for a period of time and this can only be achieved by lowering I_{Bias}. On the other hand, the JJ-FET is non-reciprocal and has a low Q thanks to modern transistor fabrication technology and the co-planar geometry. Moreover, the JJ-FET has a gate-tunable I_C and can conceivably be reset to superconducting state by increasing $V_G - V_T$. We find that a short voltage pulse can be applied to V_{IN} to temporarily boost $V_G - V_T$ and reset V_{OUT} back to zero. Figure 5.11(a-b) presents the output waveforms for the Nb- and Al-contact JJ-FET inverters with $C_L = 5$ fF in response to a square waveform with a period of 50 ps. Due to the underdamped operation, V_{OUT} remains finite when V_{IN} switches to high. Figure 5.11(c-d) shows the results of V_{OUT} with an addition of clock signals (V_{CLK}) with the same period in red and blue lines, respectively. V_{CLK} includes a 5 ps voltage pulse of 10 and 4 mV for the Nb- and Al-contact JJ-FET inverters, which is applied at the rising edge of V_{IN}. The pulse width (t_{PW}) can be narrower with a larger amplitude for higher speed, e.g. a pulse of 20 mV, 2 ps can reset this Nb-contact JJ-FET inverter. Conversely, t_{PW} of such a transient pulse can be relaxed with a lower operating frequency. A simplification is made that V_{IN} and V_{CLK} add to each other. V_{OUT} is successfully restored to zero with V_{CLK} added. Similarly, Fig. 5.11(e-f) shows the results of the voltage pulse activated at the falling edge of V_{IN}, where red and blue lines represent V_{OUT} and V_{CLK}. Though the rise of V_{OUT} is delayed, it does reach the target value. Therefore, a global clock mechanism can be introduced if underdamped operation cannot be avoided, at the expense of lower speed. Indeed, since the logic value of V_{OUT} must be evaluated when V_{CLK} = 0, the waveform half-period should exceed $t_{PW} + t_r + t_H$, where t_H is the hold time. It is noteworthy that V_{CLK} may be synchronized with the clock in a dynamic logic gate.

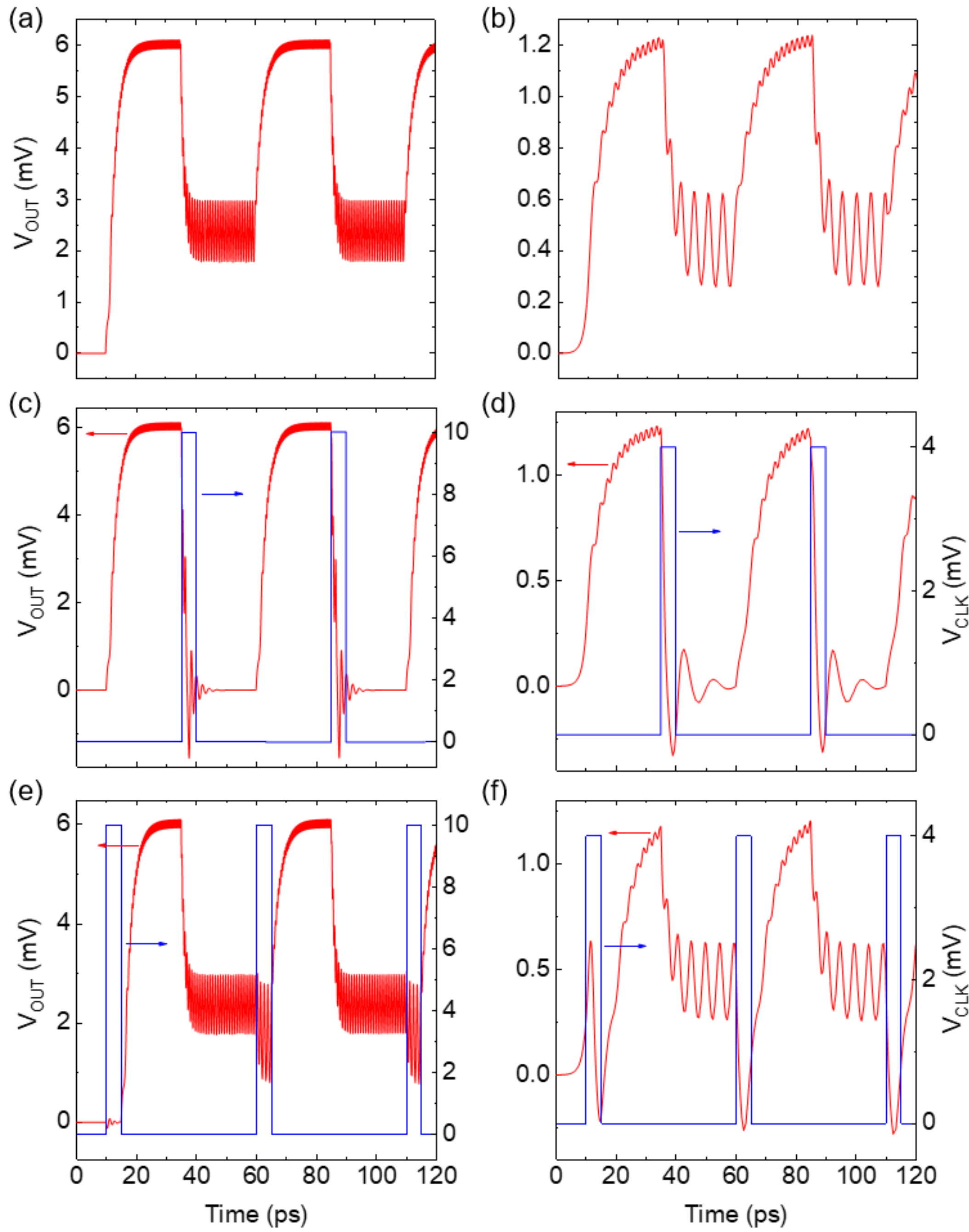

Figure 5.11: (a-b) Output waveforms of Nb- and Al-contact JJ-FET inverters without V_{CLK}. (c-d) Output waveforms with V_{CLK} switching from low to high at the V_{IN} rising edge. (e-f) Output waveforms with V_{CLK} switching from low to high at the V_{IN} falling edge. V_{CLK} is indicated in blue curves in panels (c-f). The other parameters are the same as those used in Fig. 5.9.

5.6 Design considerations and trade-offs

The model we employ in this chapter ignores the mesoscopic effects and applies to ideal contacts. It is therefore necessary to examine the validity of our assumptions. First, mesoscopic effects can potentially change the I_J value. For example, while Kondo resonances can suppress this magnitude, we expect a minimal effect for the device in the short ballistic regime [143]. The experimentally observed V_0 value is close to the ballistic limit $\pi\Delta$ [30], suggesting that the JJ-FET is not operating in the Kondo effect-dominated regime. Second, mesoscopic effects can change the dependence of I_J on $\varphi(t)$. Fortunately, this current-phase relation remains sinusoidal for a short ballistic junction in nanoscale [144]. On the other hand, in a realistic device carriers will observe a tunnel barrier at the channel/contact interface, a key ingredient to validate the sinusoidal current-phase relation [145]. It is noteworthy that the current magnitude is similar to the case where there is no tunnel barrier, since the reduction of current due to normal reflections at the disordered junction is compensated by the current increase from Andreev reflections [146]. We therefore assess that a realistic JJ-FET with finite transparency between the channel and contacts can still achieve V_0 at the short ballistic limit.

Additionally, in our analysis throughout we have assumed the JJ-FET gate overdrive $V_G - V_T$ controls the gate charge (q_G) and therefore I_C by modulating the weak link in the channel. However, this unidirectional JJ-FET model where I_{DS} is set by q_G without a back reaction is thermodynamically unsound [147]. The energy of a JJ-FET is:

$$E_{JF} = \frac{q_G^2}{2WLC_G} + \frac{\hbar}{2e} I_C(q_G)\big(1 - cos\varphi(t)\big) \tag{5.19}$$

where $I_C(q_G)$ is I_C with a gate charge q_G. Since $V_G - V_T = \partial E_{JF}/\partial q_G$, we find q_G is reduced, compared to the unidirectional model:

$$q_G = WLC_G(V_G - V_T) - \frac{\hbar\beta(q_G)}{2e}(1 - cos\varphi(t)) \tag{5.20}$$

where $\beta(q_G)$ is β with a gate charge q_G. The back reaction is negligible when the right hand side second term is small, namely $\gamma = \hbar\beta(q_G)/2eWLC_G(V_G - V_T) \ll 1$, a condition which does not hold for the logic device operation regime discussed here. For the parameters used in the Nb-contact JJ-FET inverter at zero V_{IN}, i.e. $V_G - V_T = 1.2$ mV, $W = 1$ µm and $L_G = 50$ nm, the two terms of Eq. (5.20) RHS are comparable. We note that β decreases with increasing $V_G - V_T$; hence, the back reaction becomes particularly important when V_{IN} is low. This implies that if we ignore the back reaction, the channel can be fully depleted and V_{OUT} will be in an undefined state. The back reaction can be compensated by shifting V_T to a more negative value. For example, the operation of the Nb-contact JJ-FET inverter shown in Fig. 5.9 is restored by setting $V_T =$ -3.5 mV, while the other parameters are the same. While the back reaction adds extra complexity to the design of JJ-FET logic gates, if it is properly compensated at zero V_{IN}, at high V_{IN} its impact is reduced thanks to a smaller γ.

It is of interest to investigate how advances in nano-fabrication will influence the JJ-FET logic gates. Transistor scaling effectively produces smaller L_G and larger C_G. In order to validate the model used in this study, L_G needs to be sufficiently short compared to the superconducting coherence length:

$$\xi_0 = \frac{\hbar v_F}{\pi e\Delta} = \frac{\hbar^2\sqrt{2\pi C_G(V_G - V_T)}}{m^*\pi e^{3/2}\Delta} \tag{5.21}$$

where v_F and m^* are the Fermi velocity and effective electron mass in the semiconductor channel, which are crucial to achieve a significant ξ_0 at the low $V_G - V_T$ required by JJ-FET logic gates. A large C_G in the scaled JJ-FET device promises a long ξ_0 and small γ. Alternatively, it may also allow a lower $V_G - V_T$ to reduce power consumption. However, Q will increase consequently, which imposes a design trade-off of C_G and potentially justifies the necessity of V_{CLK}. The choice of superconductor contacts is another important factor. Choosing a low Δ contact has various benefits. In light of the requirements of finite $V_G - V_T$ for reasonable γ, ξ_0 and Q, and appreciable α_R for signal restoration, we usually have $V_G - V_T \sim \Delta$. Then we can approximate the power consumption $P \propto I_C V_0 \propto \Delta^{5/2}$ and power-delay product $P\tau_{RL} \propto \Delta^{3/2}$, indicating that smaller Δ yields more efficient JJ-FET logic gates. Additionally, we have $Q \propto \sqrt{\Delta}$ and $\xi_0 \propto 1/\sqrt{\Delta}$, promoting the overdamped operation and relaxing the requirement of reduced L_G and m^*. However, we also have $\gamma \propto 1/\sqrt{\Delta}$, which indicates a low Δ JJ-FET is less immune to the back reaction. Also, a larger Δ is favored for faster speed given $\tau_{RL} \propto 1/\Delta$. The above arguments impose a design trade-off for Δ.

Although JJ-FET logic gates cannot relax the requirement of ultra-precise control of V_T compared to cryogenic CMOS, they provide a better circuit tolerance in the sense that JJ-FETs are always in the on-state while a CMOS device has to make a transition between the on-state and off-state within the operating voltage window. Moreover, the speed of the JJ-FET logic gate is limited by τ_{RL} if designed properly for an overdamped operation, as opposed to the RC time constant in a CMOS device, which can be unacceptably high for the low carrier concentrations due to a small V_{DD} at cryogenic temperatures. On the other hand, JJ-FET logic gates possess a smaller break-even operating voltage than cryogenic CMOS if we factor in the static power consumption. JJ-FET logic

gates also demonstrate great compatibility with emerging material platforms, e.g. the III-V quantum-well JJ-FET is a depletion-mode n-type device [30]; the graphene channel can reach its charge neutrality point at a slightly negative V_G [29] and the proposed JJ-FET logic gates can circumvent the issue of a low on-off ratio for CMOS [148, 149]. Moreover, the low m^* and high v_F in III-V quantum-well, and especially in graphene mitigate the conflict between long ξ_0 and low $V_G - V_T$. e.g. Dirac electrons in graphene have an $\xi_0 = 70$ nm and 470 nm in Nb- and Al-contact JJ-FETs, respectively [150].

5.7 Circuit diagram and Verilog-a code for simulation

5.7.1 Circuit diagram

Figure 5.12 shows the circuit schematic we use to simulate the dynamic behavior of a JJ or JJ-FET. On the left-hand side, the three elements in parallel are the direct implementation of the RCSJ model, where we have the two terminals as nodes A and B. A dummy circuit, which is a stand-alone loop as shown on the right hand side of the schematic, is built to store the phase difference between the two terminals of the JJ as the voltage difference between the nodes X and Y. This loop is coupled to the RCSJ part through a voltage-controlled current source (VCCS) with a gain of 1 S, whose control voltage is that across the JJ. We have a capacitor in the loop $C' = \hbar/2e$, therefore Equation (5.3) is automatically satisfied due to current conservation in the loop. Equation (5.2) is also satisfied if we write $I_J = I_C \sin\,[V(X) - V(Y)]$. After we build the circuit model, we implement it with Verilog-a due to its suitability for the behavioral modeling of electronic devices, and perform numerical simulations using the Spectre simulator in the Cadence Virtuoso environment.

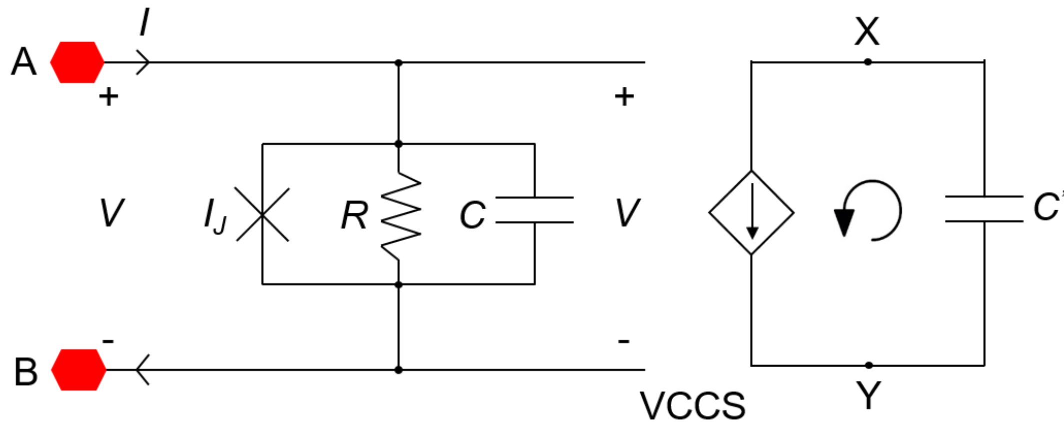

Figure 5.12: Circuit diagram used to model a JJ in the simulation.

5.7.2 Verilog-a code

The Verilog-a code to model the dynamic behavior of a JJ or JJ-FET is as follows:

```
// Verilog-a for JJFET, JJFET_VI, Verilog-a
// This is for ideal I-V curve and exclude all parastitics, use an ideal
model for ballistic transport
`include "constants.vams"
`include "disciplines.vams"
module JJFET_ideal_inductor_trio_sat (G, D, S, B);
  inout G, D, S, B;
  electrical G, D, S, B, dummy1, dummy2; //Body is grounded
  branch (G, D) gd;
  branch (G, S) gs;
  branch (D, S) ds;
  parameter real W = 4u; //width of the JJ-FET
  parameter real L = 100n; //length of the JJ-FET
  parameter real Cg = 0.0345/1; //gate capacitance, 0.0345 F/m2, divided
by EOT = 1 nm
  parameter real pi = 3.14159;
  parameter real delta = 3.05m; //superconducting gap of Nb
```

```
 //parameter real delta = 445.6u; //superconducting gap of Al
 parameter real C_2edh = 4.8355e14; //constant of value 2e/h, 2*1.602e-19/6.626e-34
 parameter real Vres = 0.01m; //residual carrier density 2.15e8/cm2, not used
 /////////////////
 parameter real Vth = -0.2m; //threshold voltage to turn on superconducting state
 /////////////////
 parameter real RnSub = 100; //Rn in subthreshold region, not used
 parameter real gamma = 10; //not used
 parameter real Vt = 26m; //Vt = kT/q, not used
 parameter real k = 4; //factor to adjust Ic, normal transmission coefficient = 1/k
 //parameter real Cj = 0.1n * W;
 localparam real hb_2e = 0.3291f; // hbar/2e
 real Ic, Rn, V0, beta_pre, beta, n, Vov, Cj; //n: 2d carrier concentration
 analog begin
         //V0 = pi*delta/2; //characteristic voltage of Nb JJ-FET
         V0 = 675u; //characteristic voltage from the experimental data
         beta_pre = V0*W*Cg*C_2edh*sqrt(2/pi); //pre-factor of beta
         //if (V(gs) - Vth > Vres) begin
              Vov = V(gs) - Vth;
         //end
         //else begin
              //Vov = Vres; // assume a residual carrier density 2.15e13/m2
         //end
         //beta = beta_pre / sqrt(n);
         Ic = 2 * beta_pre * sqrt(Vov * 1.602e-19 / Cg)/k; //critical current at the gate bias
         Rn = V0/Ic;
         if (V(ds) >= Vov) begin  //saturation
```

```
            Cj = 2/3 * Cg * W * L;
        end
        else begin  //triode
            Cj = 1/4 * Cg * W * L;
        end
        //capacitive, resistive and super current
        I(ds) <+ ddt(Cj * V(ds));
        I(ds) <+ V(ds) / Rn;
        I(ds) <+ Ic * sin(V(dummy1,dummy2));
        //form a dummy current loop to make sure V = hbar/2e *
d(phi)/dt
        I(dummy1,dummy2) <+ hb_2e * ddt(V(dummy1,dummy2));
        I(dummy1,dummy2) <+ -V(ds);
  end
endmodule
```

5.7.3 Simulation of the $I - V$ characteristics of a JJ

We simulate the time response of I and V for a JJ to test the validity of the implementation on the RCSJ model. The JJ is simulated by a JJ-FET of Nb electrodes with a geometry of $W/L =$ 1000/35 nm and a fixed $V_G - V_T = 5$ mV, similar to the device discussed in Section 5.5.2. In the transient analysis, the current supply I is swept from 0 to 40 µA then back to 0 µA in 50 ps, and the corresponding V at each time step is recorded. Figure 5.13(a-b) presents the simulation results of a JJ's $I - V$ characteristics with $C_L = 0$ and 5 fF at the output, respectively. We note that the JJ is also shunted by a small capacitor $C_J \approx 0.2$ fF. The red lines are associated with the full RCSJ model that takes the finite Q into account as described in Eqs. (5.3) and (5.4), while the blue lines are associated with the $Q = 0$ approximation in Eq. (5.7). We observe the expected results, where in the zero load and therefore a low Q scenario the JJ is free of hysteresis, while in the 5 fF load and therefore a high Q scenario the JJ demonstrates significant hysteresis. The result of the full

RCSJ model in panel (a) matches that of the $Q = 0$ static approximation reasonably well, if those superimposed AC signals on V are averaged over time. Hence, we conclude that our Verilog-a code implementation of the RCSJ model successfully reproduces the dynamics of a JJ.

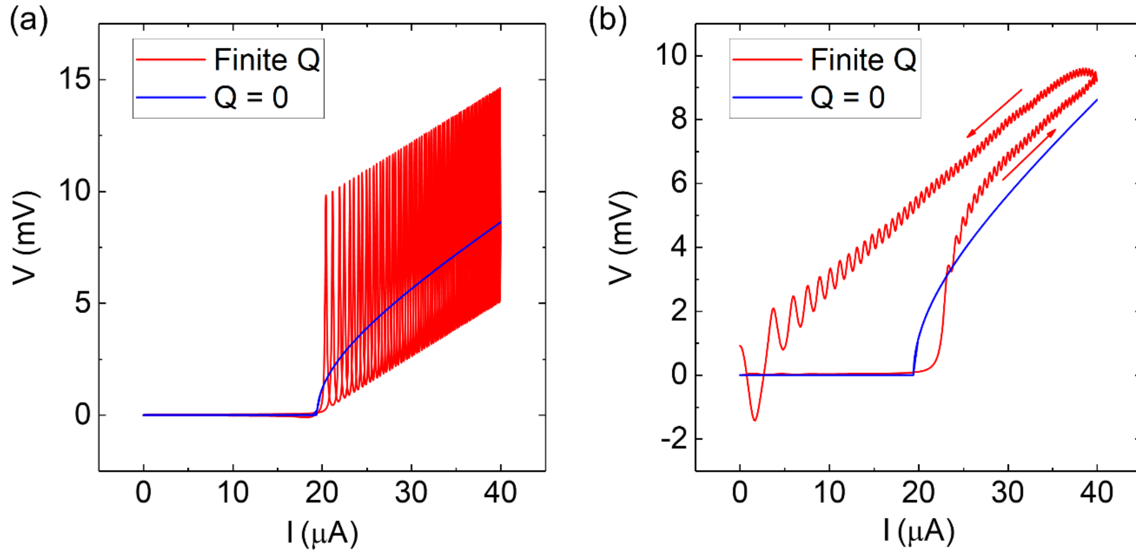

Figure 5.13: Simulation results of a JJ's $I - V$ characteristics. The blue and red lines show the $Q = 0$ static approximations and the full RCSJ model results with finite Q for (a) $C_L = 0$ fF and (b) $C_L = 5$ fF, respectively. The arrows in panel (b) mark the up sweep and down sweep of I.

5.8 Summary

When cooling costs are factored in, the operating voltage of CMOS-based circuits has to be scaled down significantly for cryogenic computing to provide a net power reduction. JJ-FET Boolean logic can harness the superconducting property of these devices at these cryogenic temperatures, and provide low operating voltage on the order of superconductor gap voltage. Assuming a short ballistic transport length, we employ the static and RCSJ model to capture the behavior of JJ-FET logic gates with fan-out. A global clock can mitigate the underdamped operation, if necessary. Transistor scaling and the choice of different superconducting contacts

have notable impacts on the device operation. For example, a reduced gate dielectric thickness guarantees better back-reaction immunity, but favors underdamped operation; the contact with a larger superconductor gap voltage ensures a faster operation speed but at the cost of reduced coherence length, hence requiring a shorter channel length. We find JJ-FET logic gates can be a promising candidate for dynamic logic elements with ultra-short fall times, and can utilize the advantages of emerging channel materials like III-V quantum wells and graphene.

Chapter 6 : Epitaxial Al-InAs Heterostructures as Platform for Josephson Junction Field-effect Transistor Logic Devices

6.1 Introduction

We have examined the theory and design of JJ-FET logic gates in Chapter 5. In this chapter we extend the discussion to the experimental operation of JJ-FETs and explore if practical logic gates can be built. We fabricate JJ-FETs using InAs quantum well heterostructure as channel, epitaxial Al as superconducting electrodes, and scaled down Al_2O_3 gate dielectrics. The V_G dependence of I_C, G_N and V_0 of the JJ-FETs coupled with capacitance measurements reveals different V_G regimes in the proximity effect characterization of JJ-FETs. Self-consistent Poisson-Schrödinger simulations allow us to associate these V_G regimes with the carriers populating one or more subbands at different vertical locations in the heterostructure. We also discuss the importance of oxide/channel interface quality and its impact on the practical implementation of JJ-FET Boolean logic gates with signal restoration.

The chapter organization is as follows. In Section 6.2, we describe the structure of the InAs quantum well heterostructure grown by molecular beam epitaxy (MBE), and detail the fabrication process of the JJ-FET. In Section 6.3, we examine the $I - V$ characteristics of JJ-FETs and extract fundamental device parameters. Section 6.4 presents the simulation results of the heterostructure electrostatics by solving self-consistent Poisson-Schrödinger equations, which reveal different V_G regimes where one or more electron subbands are populated. In Section 6.5, we compare the simulated and experimental $C - V$ data acquired from long-channel MOSFETs, which allow us to estimate the interface trap state density and associate the experimentally observed V_G regimes with those in the simulations. We also investigate the correlation between the electrostatics and the

electron transport properties for both JJ-FETs and long-channel MOSFETs. In Section 6.6, we identify the discrepancy between the fabricated JJ-FETs and the ideal short ballistic devices discussed in Chapter 5, and evaluate how the non-ideality impacts the signal restoration of JJ-FET logic gates. Section 6.7 summarizes the chapter.

6.2 Substrate growth and device fabrication process

The growth of the heterostructure is performed on a semi-insulating InP(100) substrate in an MBE system (growth JS105E in the MBE growth catalog). An 800 nm $In_xAl_{1-x}As$ graded buffer layer is first grown, starting with the composition of $In_{0.52}Al_{0.48}As$ to lattice match the InP substrate and ending with $In_{0.81}Al_{0.19}As$ to join the quantum well region. The quantum well consists of 10/4/6 nm of $In_{0.81}Ga_{0.19}As$/InAs/$In_{0.81}Ga_{0.19}As$ layers with a 10^{12} cm^{-2} Si δ-doping layer placed 6 - 7 nm below the $In_{0.81}Ga_{0.19}As/In_{0.81}Al_{0.19}As$ interface. A 25 nm epitaxial Al film terminates the MBE growth [151, 152]. The *in-situ* growth of Al is crucial to realize a transparent interface between the superconductor and the semiconductor for coherent Cooper pair transport. Figure 6.1 presents the cross-sectional TEM image showing the abrupt and flat interface between the single crystalline Al and $In_{0.81}Ga_{0.19}As$ realized with this technique.

Figure 6.2 summarizes the device fabrication steps of a JJ-FET. We first define the contour of the individual device, which is a mesa with the shape of two pads (source and drain) connected by a narrow bridge (channel), by EBL and wet-etching both Al and III-V compound epi-layers down to the InP substrate [panels (a-c)]. We use Transene aluminum etchant type-D for the Al etching, which has an etching rate of ~1 Å/s at room temperature for the single crystal Al grown in the MBE system. We usually do not assume a fixed etching time but rather check the exposed regions under optical microscope every 1 min. This is because the Al etching rate is sensitive to

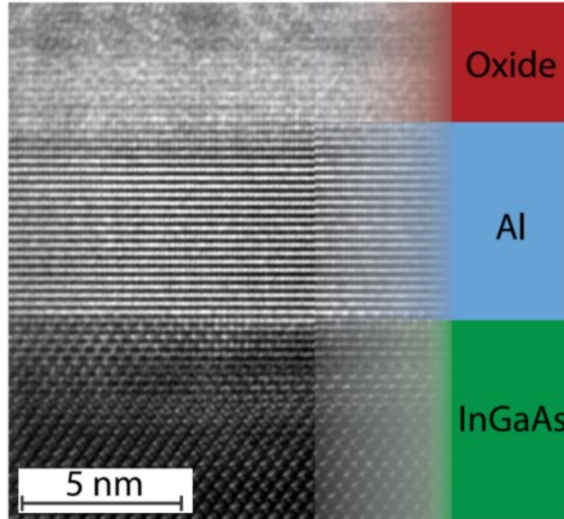

Figure 6.1: Cross-sectional TEM image of the heterostructure to highlight the high-quality interface between the single crystalline Al and $In_{0.81}Ga_{0.19}As$. (Figure adapted from Ref [151])

the ambient temperature fluctuation, and the completion of the Al etching can be reliably determined by the exposed area fully turning grey from silver, thanks to the obvious color difference between the semiconductor substrate and Al. We use a homemade solution to etch the III-V compounds, which consists of 25 parts of 12g citric acid ($C_6H_8O_7$) powder dissolved in 100g DI water with the assistance of a magnetic stirrer (500 rpm for 1 hr), 3 parts of 85% phosphoric acid (H_3PO_4) and 5 parts of 30% hydrogen peroxide (H_2O_2). The etching rate of III-V epi-layers is ~400 nm/min, while InP is almost immune to this etchant. For this particular MBE growth, we use 4 min for the Al etching and 2.5 min for the III-V etching to define the device mesa. We then perform a 2nd EBL and Al wet etch to define the channel area, a nano-gap that breaks the continuous Al film across the mesa bridge [panel (d)]. Additionally, we open an extra EBL window near the nano-gap pattern to determine if the Al etching process is completed. We always check the nano-gap using SEM to make sure Al is fully etched to avoid a shorted junction. Next, we perform a 3rd EBL and deposit 10/70 nm of Ti/Au through electron beam evaporation followed by lift-off to pattern two pads onto the source and drain area, which promote the contact of the wire

bonding and probing for future measurements [panel (e)]. Afterwards, we deposit 10 nm Al_2O_3 as the gate oxide using plasma enhanced ALD of 100 cycles at 250 °C (oxide thickness is measured by ellipsometry on a co-processed Si wafer), followed by a 4th round of EBL, metal deposition of 10/70 nm Ti/Au and lift-off to pattern the gate electrodes [panels (f-g)]. We notice that sometimes the gate metal coverage of the mesa sidewall can be an issue due to the light-of-sight deposition nature of the electron beam evaporation, where the gate metal line has to vertically run along the mesa sidewall for > 800 nm [panel (g)]. In the situation of a broken Ti/Au gate metal line along the sidewall, we will perform an additional sputtering of 120 nm Ta to cover the break, thanks to the more conformal deposition in the sputtering process (10 mTorr process pressure vs. 10^{-6} Torr in the electron beam evaporation). The final step is to open two windows at the source and drain areas to expose the Au surface through EBL and diluted HF etching [panel (h)], which is optional and usually not performed because the wire bonder head (high force required) and tungsten measurement probe can penetrate through the 10 nm Al_2O_3 to make contact with the Au metal electrodes. The HF etching step if executed needs extra attention, because a porous PMMA film may fail to protect the unexposed region and lead to damage of the Al film. In the 1st and 2nd EBL, we use a dose of 420 C/cm^2 during the exposure and PMMA A4 spin coated at 4000 rpm as resist, which becomes ~200 nm in thickness after 1 min bake on 180 ºC hotplate and is developed in MIBK : IPA = 1 : 3 for 20 sec after the exposure. In the 3rd and 4th EBL, although PMMA A4 also proves to work in most of the time, we use PMMA A6 resist as detailed in Section 3.7, since a thinner resist is preferred to define a small feature while a thicker resist is favored for easy metal lift-off. If there is a broken Ti/Au gate line along the mesa sidewall and a metal sputtering is then required for patching, only PMMA A6 or thicker resist can be used because the more conformal sputtered film is incompatible with the lift-off process using a thinner resist, e.g. PMMA A4.

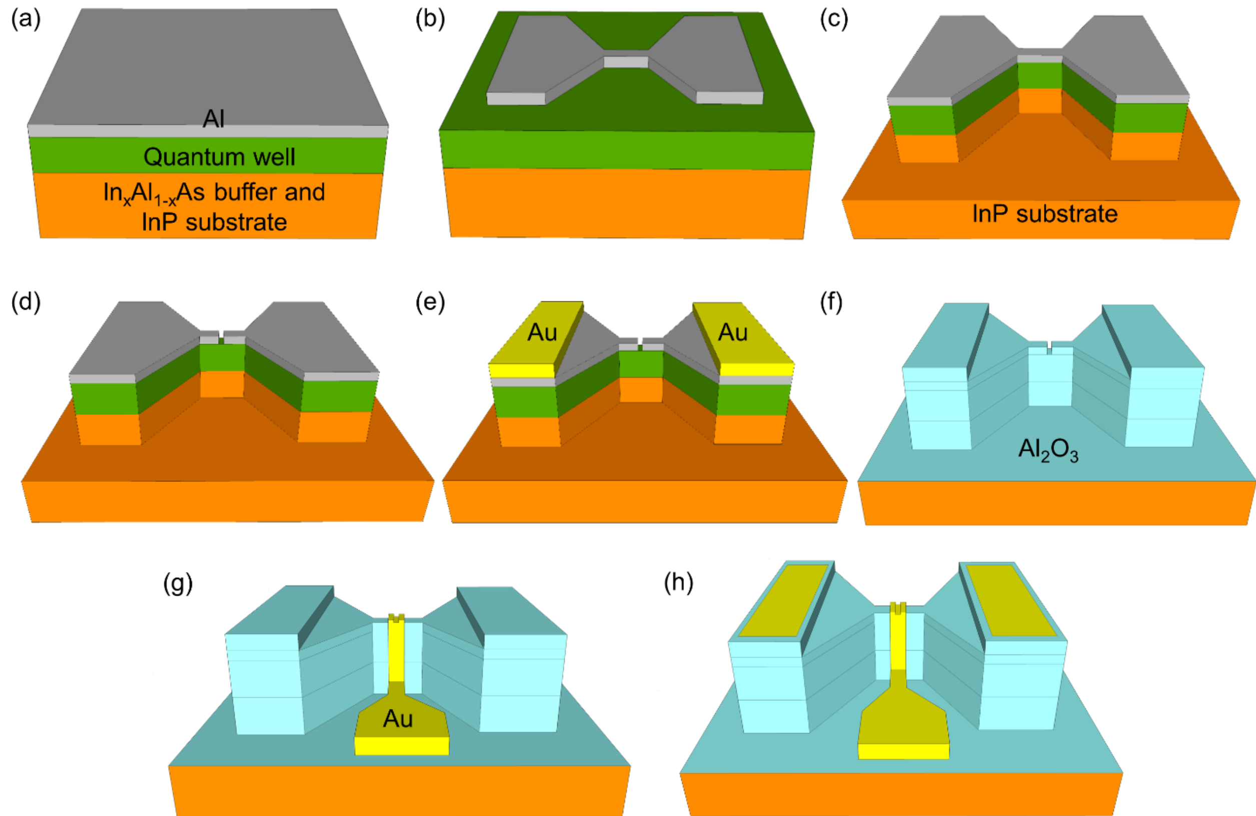

Figure 6.2: Process flow to fabricate JJ-FETs on the InAs quantum well heterostructure platform. (a) As-grown heterostructure consisting of the epitaxial Al, quantum well region, $In_xAl_{1-x}As$ buffer and InP substrate. (b) Perform EBL and wet-etch to remove Al to define the contour of the device. (c) Use the same mask to further wet-etch the entire epi-layers down to the InP substrate. (d) Perform EBL and wet-etch to define a nano-gap in Al as the channel area. (e) Perform EBL and deposit 10/70 nm Ti/Au onto the source and drain. (f) Conformal deposition of Al_2O_3 as the gate dielectric using ALD. (g) Perform EBL and deposit 10/70 nm Ti/Au to pattern the gate contact. (h) Perform EBL and open windows at the source and drain to expose the pre-deposited Au (optional step).

Figure 6.3 presents the SEM and optical images of a JJ-FET at different fabrication stages in the above discussion. Figures 6.3(a) and 6.3(e) show the top-view SEM and optical images of the nano-gap, with the Al and III-V compounds around the device mesa already removed, corresponding to the stage in Fig. 6.2(d). Figure 6.3(b-c) shows the SEM images of the top-view and 45° tilt-view from the side for a completed device using the Ti/Au metal gate. Figure 6.3(c)

reveals a broken gate metal line along the mesa sidewall, which is also confirmed by the absence of gate control over the channel in the electrical measurement. Figure 6.3(d) shows a SEM image of the 45° tilt-view from the side after an additional Ta sputtering, where the color discontinuity along the gate metal is because Au is brighter than Ta in the SEM's detector. Figure 6.3(f) presents an optical image of the channel area of a completed device with the additional Ta sputtering.

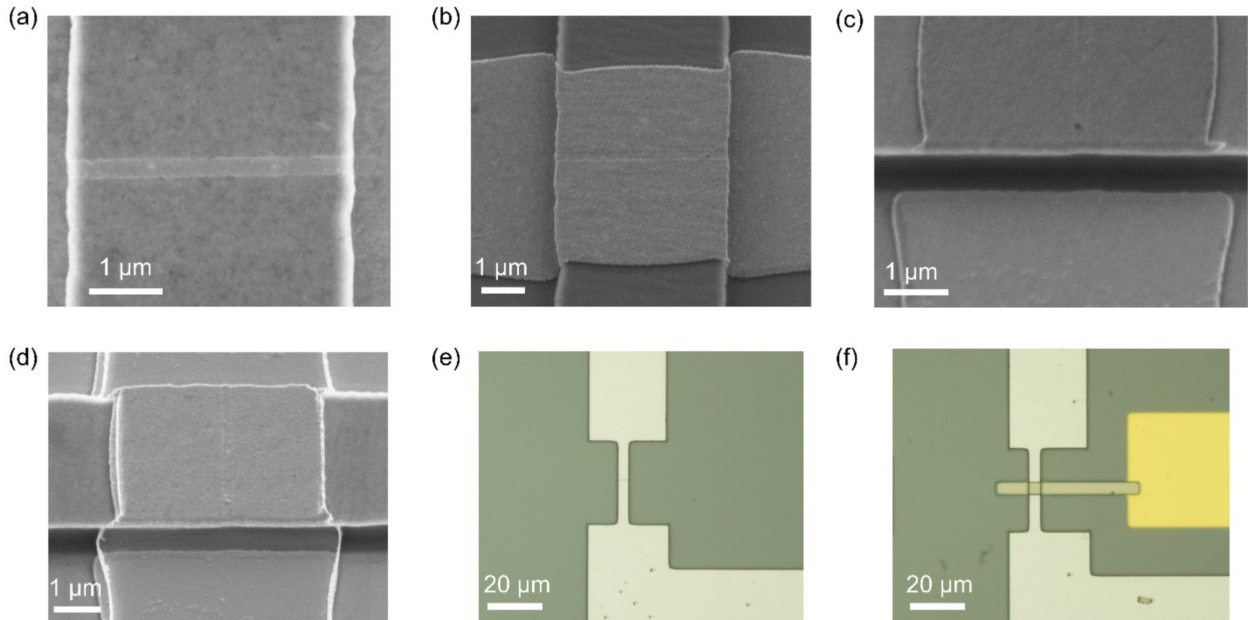

Figure 6.3: SEM and optical images at different fabrication stages. (a) SEM image of the nano-gap, corresponding to the stage in Fig. 6.2(d-e). (b) SEM image of a completed device, using the Ti/Au gate only. Tilt-view SEM images showing (c) a broken Ti/Au metal line before and (d) a continuous metal film after the Ta sputtering along the mesa sidewall. (e) Optical image of the nano-gap. (f) Optical image of a completed device, with Ta sputtering to patch the broken Ti/Au along the mesa sidewall.

Figure 6.4 shows the cross-sectional schematic to illustrate the composition of the quantum-well heterostructure and the JJ-FET device geometry. We fabricate two sets of devices. One set consists of short-channel JJ-FETs with $W = 4$ μm and $L_G = 250$ nm. The second set consists of long-channel MOSFETs with $W = L_G = 100$ μm. The fabrication process of the long-channel MOSFET is very similar to that of the JJ-FETs, except we sputter 150 nm Ta as the gate

metal to prevent measurement probes from penetrating the gate metal and dielectric. We perform electrical measurement in either a dilution refrigerator at $T = 17$ mK for the JJ-FETs, or probe station at $T = 77$ K for the long-channel MOSFETs, respectively.

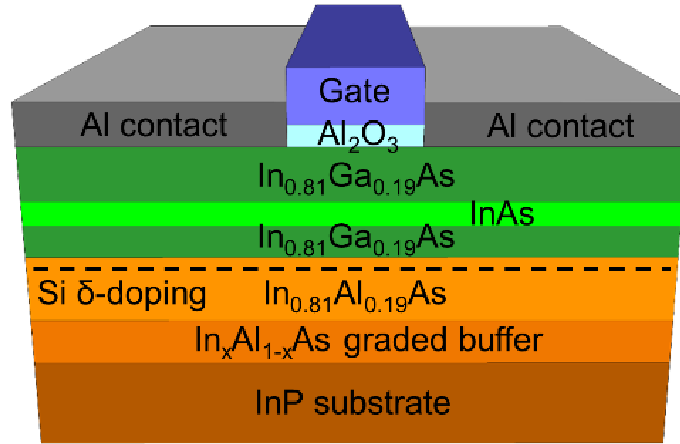

Figure 6.4: Schematic of the JJ-FET, and the InAs quantum well heterostructure platform.

6.3 JJ-FET $I - V$ characteristics

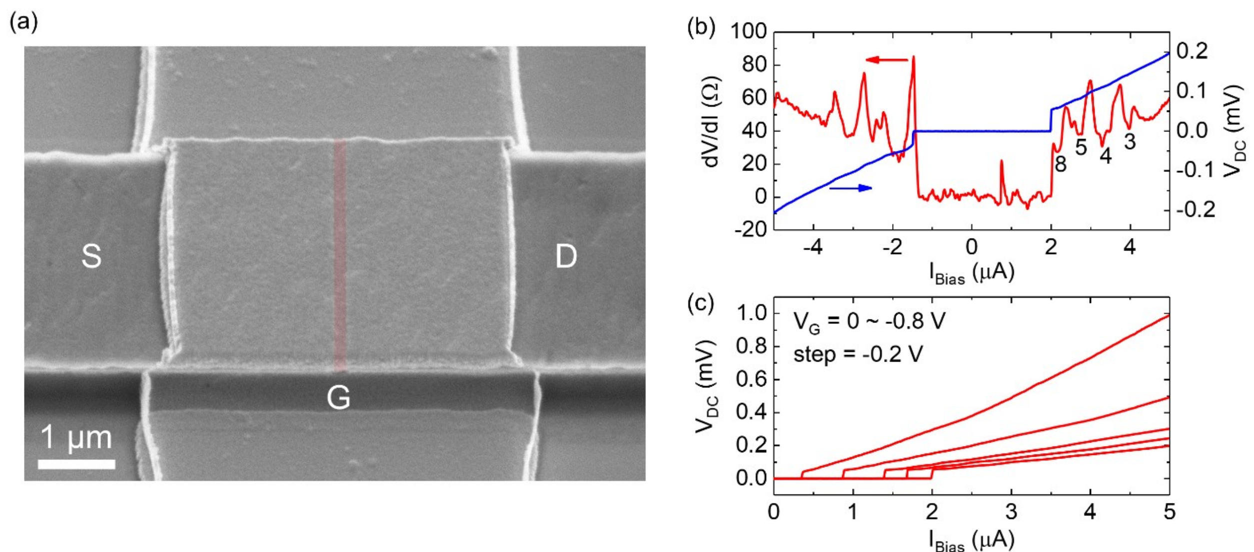

Figure 6.5: (a) SEM image of a completed JJ-FET device using the InAs quantum well heterostructure as channel. (b) dV/dI vs. I_{Bias} and V_{DC} vs. I_{Bias} measured at $V_G = 0$ V, shown with red and blue lines and

corresponding to the left and right y-axes, respectively. The Andreev reflection dV/dI minima are indicated. (c) I_{Bias} vs. V_{DC} at different V_G, where a larger I_C corresponds to a larger V_G value. Figure 6.5: continued.

Figure 6.5(a) presents the SEM image of a completed JJ-FET with Ta sputtered to patch the broken Ti/Au along the mesa sidewall, whose source, drain and gate terminals are labeled, and the channel area is shaded in red. The JJ-FETs are probed with a standard low-frequency lock-in setup, by flowing a fixed I_{Bias}, and measuring the junction differential resistance (dV/dI) with a 10 nA AC excitation current at 17 Hz, as well as the voltage drop (V_{DC}). Figure 6.5(b) presents the I_{Bias} dependence data of dV/dI and V_{DC} for a JJ-FET. In the dV/dI vs. I_{Bias} data, we observe a superconducting region at lower I_{Bias}, and a series of oscillations in the dV/dI values, which correspond to the subharmonic energy gap structure caused by multiple Andreev reflections showing dV/dI minima at $V_{DC} = 2\Delta/n$ (n is a positive integer). The values of n associated with the identified dV/dI minima are labeled. At each minimum, the channel charge gains an energy of $2e\Delta$ to directly inject into the superconductor after elastically scattered between the source and drain for n times [153]. Figure 6.5(c) presents the $V_{DC} - I_{Bias}$ output characteristics at V_G ranging from 0 to -0.8 V in a step size of -0.2 V, showing the n-type depletion mode behavior and a gate-tunable I_C. Figure 6.6(a) presents the dV/dI vs. V_{DC} data by combining the two traces in Fig. 6.5(b), from which the V_{DC} values associated with the dV/dI minima can be directly extracted. The indices n of these dV/dI minima are determined so that their corresponding V_{DC} values and $1/n$ have a linear relation. Figure 6.6(b) shows the V_{DC} values corresponding to these minima vs. $1/n$ data along with their linear fit, whose slope is $2\Delta = 430$ μV and thus allows us to determine the superconducting gap voltage of the epitaxial Al electrode $\Delta = 215$ μV [154, 155]. The measured Δ value agrees with the BCS theory prediction of $1.76\,k_B T_C/e$, given the critical temperature of the Al electrode in our JJ-FETs is $T_C \approx 1.4$ K [131].

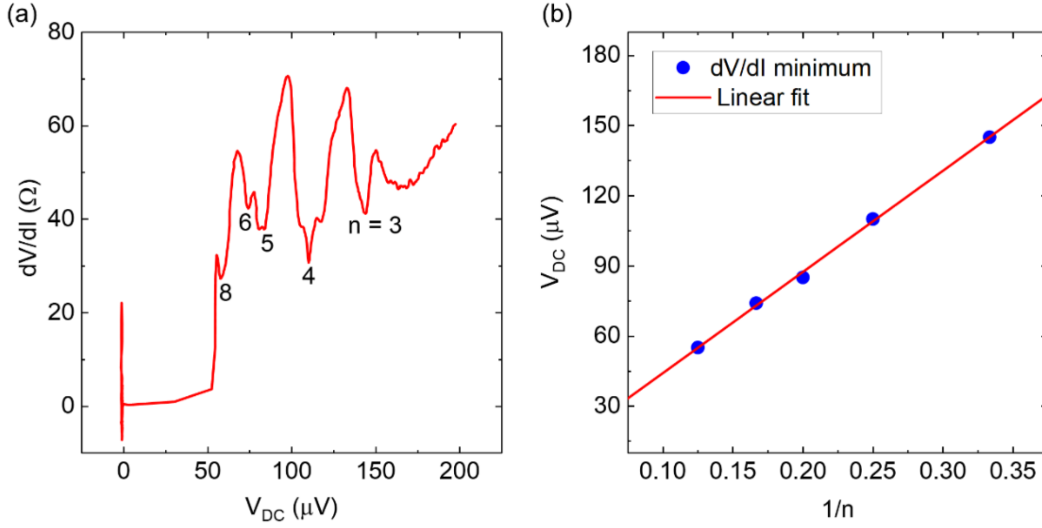

Figure 6.6: (a) dV/dI vs. V_{DC} with n associated with the observed dV/dI minima labeled. (b) The values of V_{DC} corresponding to the labeled dV/dI minima in panel (a) vs. $1/n$ and the linear fit.

6.4 Self-consistent Poisson-Schrödinger simulation

To better understand the band structure and carrier distribution in the heterostructure, we perform self-consistent Poisson-Schrödinger simulations using NextNano [156]. NextNano provides two numerical solvers nn3 and nn+ that are written in FORTRAN and C++, respectively. The latter is the successor of the former and provides a simpler syntax, faster convergence and better accuracy at temperatures of 3 K or lower. In this chapter, all numerical results presented are calculated using the nn+ solver and have been cross compared with those of nn3. Due to the lattice mismatch between the quantum well region and InP substrate, there is a biaxial strain in the former that can alter its band structures. NextNano is capable to calculate the biaxial strain and the strain-induced band deformation for this two-dimensional planar geometry. Figure 6.7(a) summarizes the strain tensor components in the quantum well region assuming it being coherently strained to the InP substrate, which include the in-plane normal strain ε_{xx}, ε_{yy}, the out-of-plane normal strain ε_{zz}, the shear strain ε_{xy}, ε_{yz}, ε_{xz}, along with the hydrostatic strain ε_h. The negative ε_h indicates

the biaxial strain is compressive in the quantum well region. Figure 6.7(b) presents the temperature dependence of the bandgaps in the quantum well region as well as the InP substrate, showing that the bandgaps under the compressive biaxial strain (dashed lines) are larger than those under zero strain (solid lines).

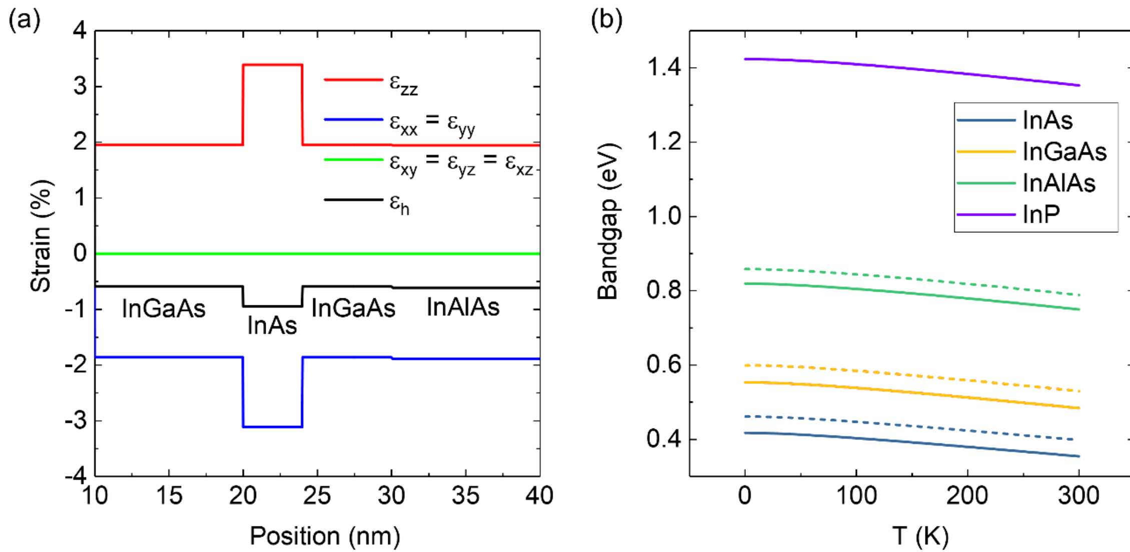

Figure 6.7: (a) Strain profile in the quantum well region, with the materials in different regions labeled. (b) Bandgap vs. temperature for the quantum well region and the InP substrate. Solid and dashed lines present the unstrained and coherently strained data, respectively.

Figure 6.8(a) shows the band diagrams and electron densities (n_e) across the heterostructure at $T = 77$ K and $V_G - V_T = 70$ mV, where a single electron subband is populated; V_T is the threshold voltage denoting the onset of populating the first electron subband. The solid and dashed lines present the data assuming material parameters at zero strain, or the quantum well region coherently strained to the InP substrate, respectively. The biaxial strain increases the bandgaps of the quantum well region as shown in Fig. 6.7(b) and weakens the electron confinement in the InAs well by reducing the conduction band offset between InAs and the $In_{0.81}Ga_{0.19}As$ barriers. Consequently, more electrons populate the bottom $In_{0.81}Ga_{0.19}As$ layer and cause a slight

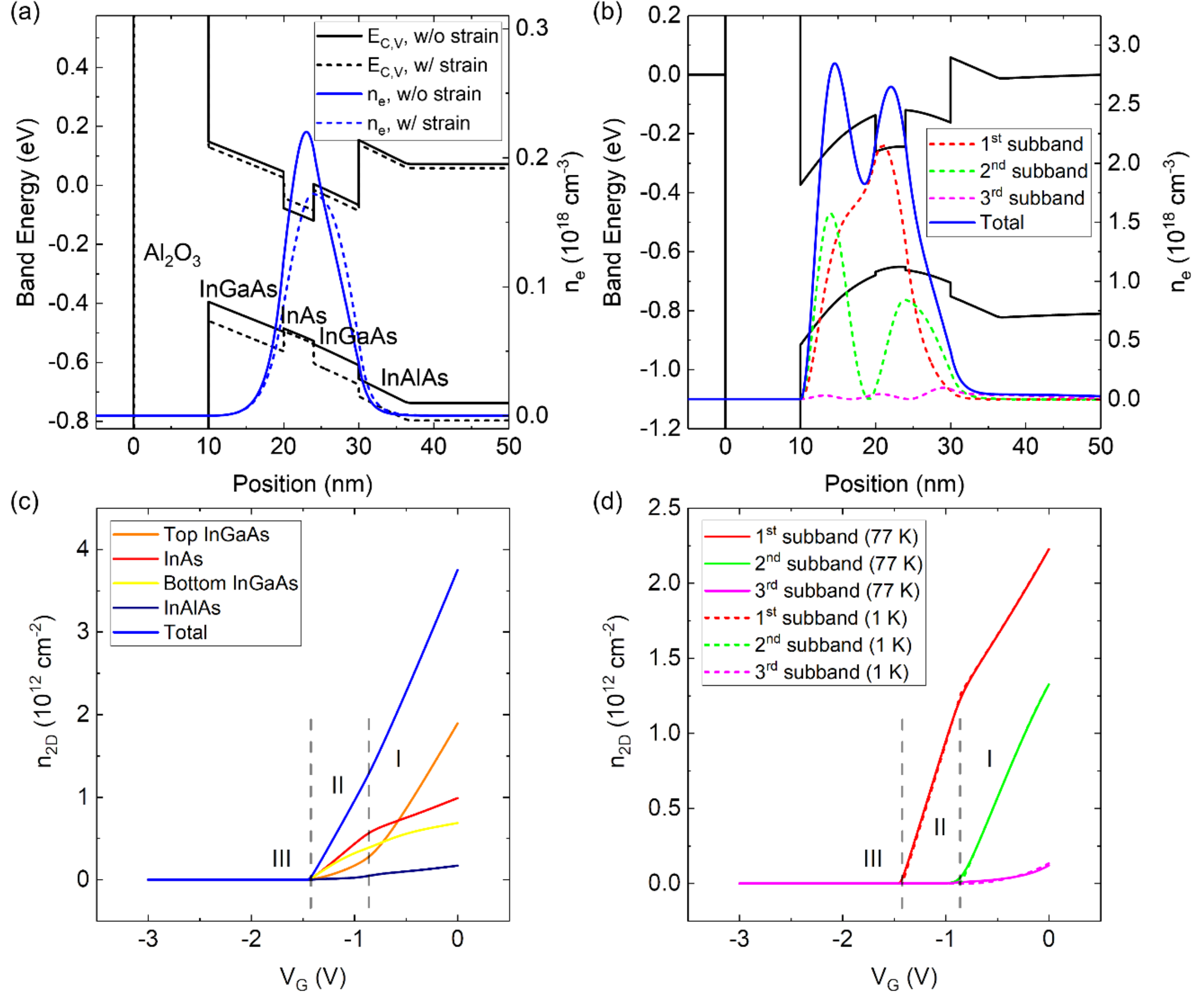

Figure 6.8: (a) Band diagrams and n_e vs. position at $T = 77$ K and $V_G - V_T = 70$ mV. The material corresponding to the different region is labeled. The solid (dashed) black lines show E_C and E_V for the unstrained (strained) heterostructure. The blue lines show n_e. (b) Band diagrams and n_e vs. position at $T = 77$ K and $V_G - V_T = 1.4$ V. The total, and first three electron subbands n_e values are shown with solid and dashed lines, respectively. E_F is located at 0 eV in panels (a-b). (c) Total and individual layers n_{2D} vs. V_G at $T = 77$ K. (d) n_{2D} for the first three electron subbands vs. V_G at $T = 77$ K (solid lines) and $T = 1$ K (dashed lines).

increase in EOT. We observe minor differences in the MOS electrostatics by including the change of band structures due to strain, and assume unstrained material parameters in the rest of the chapter. We also assume in our simulations that the Si donors are fully ionized, and surface accumulation in high indium content compounds, most notably observed in InAs, is ignored.

Figure 6.8(b) presents the band diagram, and n_e at $T = 77$ K and $V_G - V_T = 1.4$ V where multiple electron subbands are populated. The dashed lines show n_e for the first three electron subbands, where we observe the population of the 2nd electron subband leads to a significant n_e in the top $In_{0.81}Ga_{0.19}As$ barrier. Figure 6.8(c) shows n_{2D}, the volume integration of n_e in the respective region, vs. V_G in different layers and the entire heterostructure. We label regimes I, II or III if multiple, single or no electron subbands are occupied. Indeed, n_{2D} in the top $In_{0.81}Ga_{0.19}As$ layer increases rapidly to surpass that in the InAs layer in regime I as electrons populate the 2nd subband. This phenomenon is similar to the Si shell getting populated at a larger gate bias in the *p*-type $Si_{0.5}Ge_{0.5}$-Ge-Si core-double-shell nanowire MOSFET discussed in Section 4.6. Figure 6.8(d) summarizes the V_G dependence of n_{2D} in the first three electron subbands at $T = 77$ K and $T = 1$ K, in solid and dashed lines, respectively. The two sets of data are almost identical except for a noticeable thermal smearing of the onsets of the electron subbands at $T = 77$ K.

6.5 $C - V$ and electron transport data of long-channel MOSFETs and JJ-FETs

Next, we compare the simulated and experimental $C - V$ data to probe the oxide/channel interface quality. Figure 6.9(a) presents the measured $C - V_G$ data of a long-channel MOSFET acquired with source and drain connected as ground, and a coupling AC signal of 100 Hz applied at the gate. We assign different V_G regimes as labeled, and separated by dashed lines. Regime IV is associated with holes responding to the small signal. Although the $C - V$ data indicates hole accumulation at negative V_G, we do not consider hole transport because the epitaxial Al contact favors the electron injection, and no super current exists at that negative V_G. A kink in the C value is observed at $V_G \approx$ -0.2 V, which is associated with the onset of electrons populating the top $In_{0.81}Ga_{0.19}As$ barrier, resulting in an EOT reduction when the device enters regime I from regime

II. Figure 6.9(a) inset shows the equivalent circuit under measurement, where C_{ox}, C_s and C_{it} are the oxide, semiconductor and interface trap capacitance, respectively; $C_{it} = e^2 D_{it}$, where D_{it} is the interface trap state density. Figure 6.9(b) shows the experimental $C - V_G$, and the simulated $C_{sim} - V_G$ data calculated as $C_{sim} = e \cdot \frac{dn_{2D}}{dV_G}$. The oxide capacitance $C_{ox} = 0.69$ μF/cm^2 (EOT = 5 nm) is acquired from a separate capacitor device, and shown with a horizontal dashed line. The measured C is higher than C_{sim} in regimes I and II, and suggests a notable D_{it}, while lower in regime IV due to the low hole injection efficiency from Al contacts and large channel resistance. Particularly noteworthy, the capacitance values remain finite in regime III where the channel charge is expected to be fully depleted. We note that both of our long-channel MOSFETs and JJ-FETs have small on/off ratios and gradual transitions between the two states, to which we refer as the soft turn-off. Hence, the channel is still sufficiently conductive to allow electrons injected to fill the interface trap states in regime III. The insulating InP substrate hinders the direct characterization of MOS capacitors by employing, e.g. the low and high frequency or Terman method [157, 158] to decouple the DC and AC response from the interface trap states for D_{it} calculation. Instead, we estimate an average D_{it} by first calculating a uniform distribution over energy that can accommodate V_G's stretch-out from the valley to kink position between the simulated and experimental data, followed by verifying that the calculated C_{it} in combination with C_{sim} can match the measured C. The valley in the $C - V_G$ experimental data corresponds to a V_G value at which E_F is at mid-gap (E_{MG}) at the top $In_{0.81}Ga_{0.19}As/Al_2O_3$ interface [159, 160], while the kink marks the onset of the 2nd electron subband population in the simulation. The valley and kink positions are marked with arrows in Fig. 6.9(b). At the kink position, the simulated band diagram reveals $E_F \approx E_C$ at the interface between Al_2O_3 and the top $In_{0.81}Ga_{0.19}As$ layer. Hence, we determine $D_{it} \approx e^{-2} C_{ox} \delta V_G / 0.5 E_g = 6.5\times10^{12}$ eV^{-1}·cm^{-2}; E_g is the bandgap of $In_{0.81}Ga_{0.19}As$

and δV_G is V_G's stretch-out induced by D_{it}. We then calculate a new set of $C' - V_G'$ data based on the $C_{sim} - V_G$ data at each V_G beyond the valley point $V_G(\text{valley})$ and the corresponding total n_{2D}, by applying the following equations derived using the equivalent circuit in Fig. 6.9(a) inset. For $V_G \leq V_T$, $C_{sim} = 0$ and $n_{2D} = 0$:

$$C' = 1/(C_{ox}^{-1} + C_{it}^{-1}) \tag{6.1}$$

$$V_G' = V_G + [V_G - V_G(\text{valley})]\frac{C_{it}}{C_{ox}} \tag{6.2}$$

For $V_G > V_T$, the values of C_{sim} and n_{2D} are non-zero and:

$$C' = 1/[C_{ox}^{-1} + (C_{it} + (C_{sim}^{-1} - C_{ox}^{-1})^{-1})^{-1}] \tag{6.3}$$

$$V_G' = V_T' + en_{2D}\left[\left(1 + \frac{C_{it}}{C_{ox}}\right)(C_{sim}^{-1} - C_{ox}^{-1}) + C_{ox}^{-1}\right] \tag{6.4}$$

where V_T' is calculated by Eq. (6.2) at $V_G = V_T$ to account for the D_{it}-induced stretch-out. We note the above equations can be applied to any D_{it} value, without referring to the simulated band diagrams. Alternatively, V_G' can be calculated at V_G above or below V_T using the simulated E_F and E_{MG} as follows:

$$V_G' = V_G + (E_F - E_{MG})C_{it}/eC_{ox} \tag{6.5}$$

Figure 6.9(c) compares the electron branches of the experimental $C - V_G$ and the calculated $C' - V_G'$ data according to Eqs. (6.1), (6.3) and (6.5) using $D_{it} = 6.5\times10^{12}$ $\text{eV}^{-1}\cdot\text{cm}^{-2}$. The $C' - V_G'$ data reproduces the stretch-out observed experimentally, and the C' values agree quantitatively with the measurement in regime II and III. It is noteworthy that the C_{sim} values in regime II are approximately half of C_{ox} due to the quantum capacitance and spatial separation between the

oxide/channel interface and the centroid of the electron wave function. These effects add an extra 5 nm to the EOT, thus setting its lower limit.

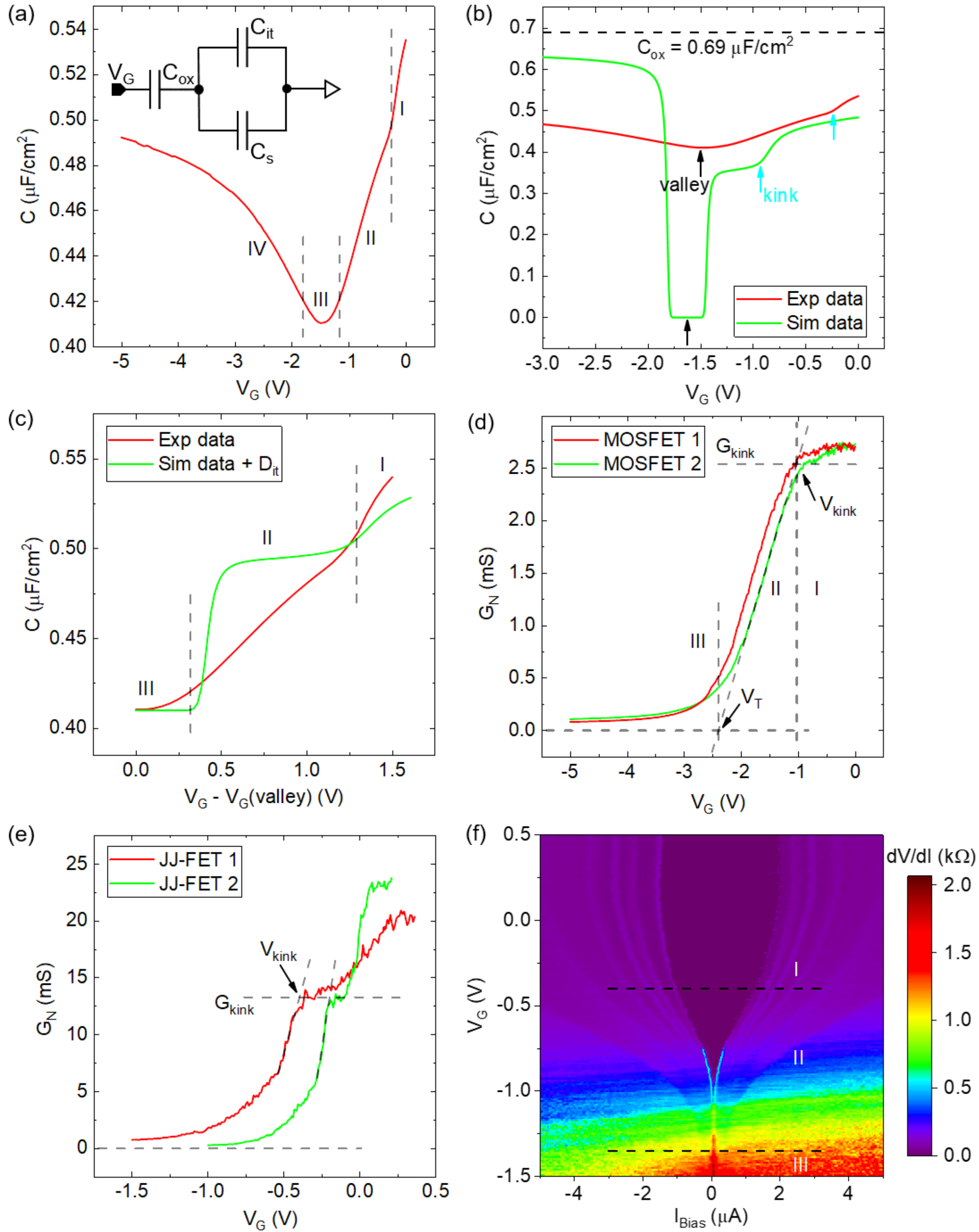

Figure 6.9: (a) Experimental $C - V_G$ data for a long-channel MOSFET at $T = 77$ K. The inset shows the equivalent circuit of the measured device. (b) Comparison of the experimental $C - V_G$ and the simulated $C_{sim} - V_G$ data. The value of C_{ox} is marked with a horizontal dashed line. The black and cyan arrows

highlight the valley and kink positions, respectively. (c) Comparison of the experimental $C - V_G$, and the calculated $C' - V_G'$ data including contributions from a finite D_{it}. (d) G_N vs. V_G data measured in long-channel MOSFETs, and (e) JJ-FETs. The positions of G_{kink} , V_{kink} and V_T are marked. (f) Contour plot showing the dV/dI vs. I_{Bias} and V_G for JJ-FET 1. Figure 6.9: continued.

Next, we apply the V_G regimes discussed above to interpret the electron transport data of long-channel MOSFETs and JJ-FETs. Figure 6.9(d) shows the channel conductance G_N vs. V_G data acquired from two long-channel MOSFETs at a drain bias of 5 mV, where we also label three V_G regimes separated by vertical dashed lines. Noticeable kinks in the $G_N - V_G$ data are marked with a horizontal dashed line. The G_N value increases linearly with V_G in regime II, and the linear fit of this section marks the boundary between regime I and II at $G_N = G_{kink}$ and $V_G = V_{kink}$. This transition is consistent with the electrostatics discussed in Fig. 6.8 as well as the $C - V_G$ data, because the population of the 2nd electron subband leads to inter-subband scattering [161], and the associated electron transport in the top $In_{0.81}Ga_{0.19}As$ layer is suppressed by the disordered oxide/channel interface. The other side of the linear fit intercepts $G_N = 0$ at $V_G = V_T$, marking the boundary between regime II and III. We notice the measured G_N decreases gradually near V_T and remains appreciable deep into regime III, in contrast to the well defined V_T in the simulation data of Fig. 6.8(c-d). This device feature has been described as the soft turn-off, with the on/off ratio < 50 and $SS > 1$ V/dec. The device subthreshold region is impacted by the large D_{it} [162, 163], and possibly lattice defects in the heterostructure, which is revealed by the atomic force microscopy showing a surface RMS roughness of a few nm, suggesting the presence of strain-induced misfit dislocations that can give rise to significant leakage current [152, 164-166]. Figure 6.9(e) shows the G_N vs. V_G data of two JJ-FETs, acquired from the linear fits of normal regions in the $V_{DC} - I_{Bias}$ data. G_{kink} is marked with a horizontal dashed line. Similar to the long-channel MOSFETs, the JJ-FETs also have low on/off ratio and large SS due to the significant leakage current. Figure

6.9(f) presents the contour plot showing the I_{Bias} and V_G dependence data of dV/dI for JJ-FET 1, where the three V_G regimes are labeled, and the boundaries between regime I/II and II/III are marked by its V_{kink} and V_T, respectively. Due to the absence of a clear linear G_N vs. V_G region for $V_G < V_{kink}$, we determine V_T using the measured V_{kink} along with the calculated V_G span in regime II, including the D_{it} induced stretch-out as shown in Fig. 6.9(c). A superconducting region emerges at V_G = -0.95 V and the critical current I_C increases gradually as a function of gate bias up to V_G = -0.7 V, while $V_0 \equiv I_C/G_N$ increases from 30 μV to 100 μV. The I_C value shows a linear dependence on V_G in the rest of regime II, from V_G = -0.7 V to V_{kink}, and is largely insensitive to V_G in regime I. The V_G dependence of I_C resembles that of G_N for $V_G >$ -0.7 V, where V_0 is approximately constant at 100 μV. Figure 6.10(a-b) presents the V_G dependence data of I_C and V_0 for JJ-FET 1, with V_G = -0.7 V and the boundary between regime I and II (V_{kink} = -0.4 V) labeled with vertical dashed lines in both panels. The calculated V_T = -1.35 V that marks the boundary between regime II and III is also labeled. In addition, the position of V_0 = 100 μV is marked with a horizontal dashed line in Fig. 6.10(b).

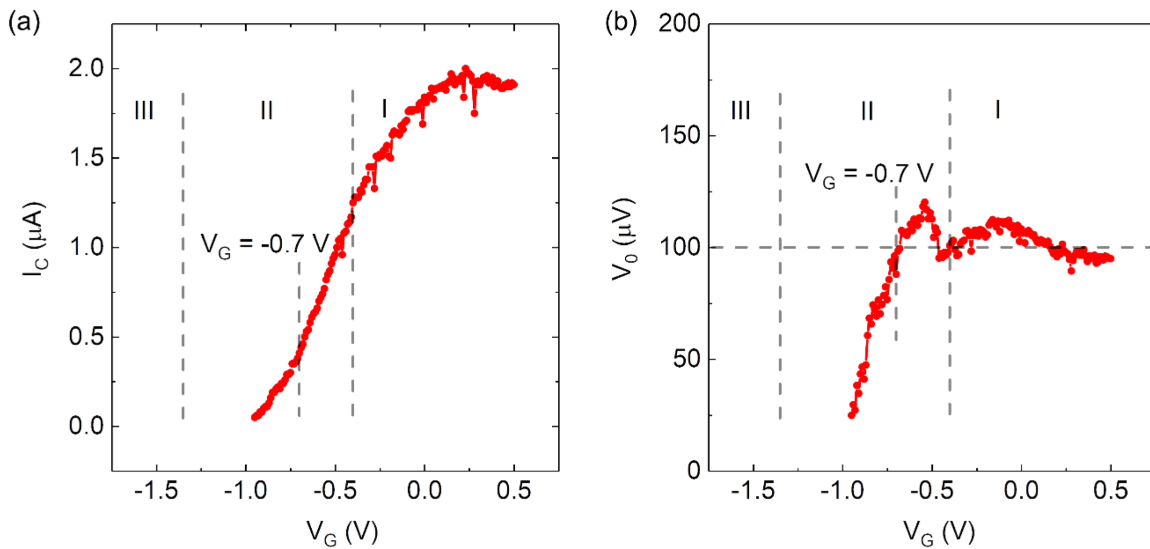

Figure 6.10: Experimental data showing (a) I_C vs. V_G and (b) V_0 vs. V_G for JJ-FET 1. $V_G = V_T$, V_G = -0.7

V and $V_G = V_{kink}$ are marked by vertical dashed lines in both panels. Figure 6.10: continued.

6.6 Feasibility of JJ-FETs using the InAs quantum well heterostructure as channel for practical JJ-FET logic gates

The remaining part of the chapter examines the implications of the previous findings on JJ-FET logic gates based on the InAs quantum well heterostructure. As discussed in Chapter 5, logic gates require signal restoration to be cascaded in order to perform complex functions, where the output (drain) of one JJ-FET directly drives the gate of another JJ-FET, whose I_C thus needs to be sufficiently modulated with respect to I_{Bias} for a switch. Figure 6.5(c) suggests that V_{DC} will be of the order of V_0 if I_{Bias} is comparable to I_C. Hence, the gain factor $\alpha_R = \beta V_0 / I_C = \beta / G_N$ defined in Section 5.4, which represents the relative change in I_C corresponding to a gate swing of V_0, is still a valid indicator to determine if a JJ-FET logic gate built with the fabricated device can achieve signal restoration. An α_R value close to unity requires the JJ-FET to operate at a small $V_G - V_T \sim \Delta$, a range where the electrons populate only one subband. Operating in regime II benefits the ballistic transport of electrons, thanks to the isolation from the $In_{0.81}Ga_{0.19}As/Al_2O_3$ interface and the absence of inter-subband scattering. Recalling the lower limit of EOT set by the heterostructure, ξ_0 needs to exceed a realistic L_G under both constraints of EOT and $V_G - V_T$. With $V_G - V_T = \Delta$, the coherence has a $\xi_0 \propto 1/\sqrt{\Delta}$ dependence on the superconductor gap voltage. Figure 6.11 presents the Δ dependence data of ξ_0 calculated using Eq. (5.21) with EOT = 5 nm and $m^* = 0.023 m_0$ for InAs. The values of Δ and ξ_0 for Al and Nb are marked by vertical and horizontal dashed lines, respectively. The ξ_0 values are approximately 40 nm for Al, and 15 nm for Nb, which exceed the minimum feature size of the state-of-art nano-fabrication techniques and justify the feasibility of the heterostructure as the platform for practical JJ-FET logic applications.

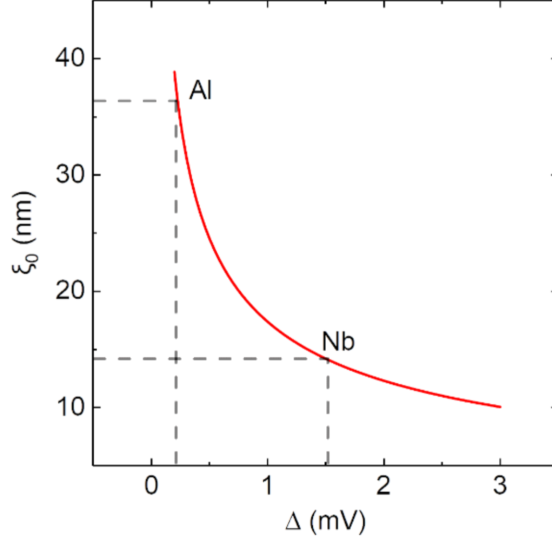

Figure 6.11: ξ_0 vs. Δ, calculated using Eq. (5.21) with $V_G - V_T = \Delta$, EOT = 5 nm and $m^* = 0.023m_0$.

Departures from the short ballistic JJ-FET operation impacts the signal restoration of JJ-FET logic gates. Figure 6.12(a) summarizes the $V_G - V_T$ dependence of the ideal α_R values calculated using Eq. (5.15) with $V_0 = \pi\Delta =$ 675 μV, along with the experimental α_R calculated with β/G_N directly using the measured values of β and G_N for JJ-FET 1. In the Fig. 6.12(a) comparison we use $V_T =$ -1.35 V as determined earlier. We notice the experimental values of α_R are smaller compared to the calculations, and saturate below 0.2%. These differences stem from a V_0 experimental value of 30 - 100 μV, much smaller than the ideal value 675 μV, and the V_G dependence of I_C and G_N substantially deviating from that expected for JJ-FETs operating in the short ballistic regime particularly close to threshold, due to the larger L_G and imperfections of the fabricated device. The key requirement for Eq. (5.15) to be valid, and the value of α_R close to unity is the JJ-FET has a well defined V_T and a precise gate modulation of channel charge at a small $V_G - V_T \sim \Delta$. However, in presence of a large density of interface trap states, these conditions do not hold and the I_C dependence on V_G is significantly reduced. In fact, our JJ-FETs have $I_C = 0$ in the near threshold region where a significant α_R value is expected, because scattering from the

interface trap states and defects can suppress I_C [167]. Figure 6.12(b) presents the V_{DC} vs. V_G data at various I_{Bias} for the same JJ-FET, which can be viewed as a set of voltage transfer curves of a JJ-FET inverter. Although the logic function NOT is fulfilled in this example, practical JJ-FET logic gates cannot be realized with the fabricated devices due to the small α_R and thus low gain. Moreover, there is a mismatch of the logic voltage level between the input and output. Logic '0' of the output V_{DC} always has a perfect 0 V value thanks to the superconductivity, while that of the input V_G depends on V_T and I_{Bias}.

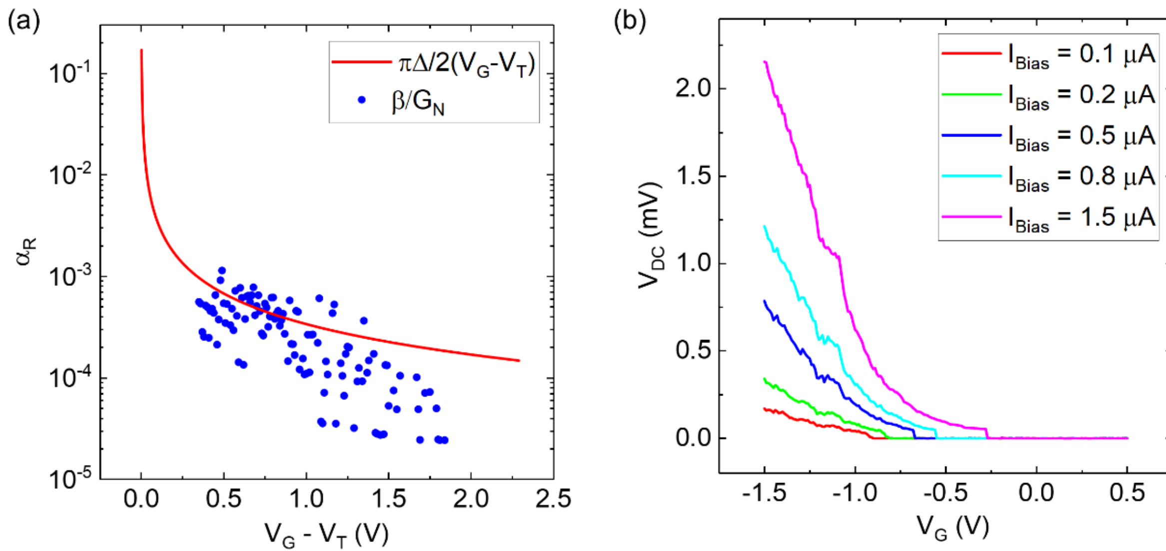

Figure 6.12: (a) Experimental JJ-FET gain factor α_R vs. $V_G - V_T$ (symbols), along with the theoretical values (solid line) expected in the short ballistic regime. (b) V_{DC} vs. V_G at different I_{Bias}. The trace with V_{DC} switching between zero and finite value at a larger V_G corresponds to a larger I_{Bias}.

On the other hand, we anticipate the JJ-FETs can operate in the short ballistic regime if a short L_G as well as very low D_{it}, and lattice defect density are achieved. In these conditions, it becomes realistic to design and implement practical logic devices using this InAs quantum well heterostructure. As discussed in Chapter 5, designing the biasing point of JJ-FET logic gates translates into identifying the combination of I_{Bias} and $V_G - V_T$ that leads to same input/output

swing magnitude, and consequently signal restoration. The logic voltage level mismatch between the input and output can be eliminated by tuning the Si δ-doping level and using gate-stack engineering to adjust V_T.

6.7 Summary

We fabricate JJ-FETs with scaled down Al_2O_3 as gate oxide based on the epitaxial Al-InAs heterostructure platform, and characterize the V_G dependence of I_C, G_N and V_0. We observe different V_G regimes in the proximity effect measurements of the JJ-FETs, which are also revealed in the $C-V$, $I-V$ characterizations of long-channel MOSFETs sharing the same platform. Self-consistent Poisson-Schrödinger simulations allow us to identify different V_G regimes as the electrons populating one or more electron subbands in the InAs well and the top $In_{0.81}Ga_{0.19}As$ barrier. We also evaluate the potential of JJ-FETs using this heterostructure as channel for logic applications, and confirm its feasibility to operate in the short ballistic regime with signal restoration. We find that the smaller V_0, and reduced gate control of I_C and G_N due to interface traps and static disorder can adversely impact the signal restoration of JJ-FET logic gates expected in the short ballistic operation. We expect that a shorter L_G combined with a high oxide/channel interface quality and low crystal defect density can mitigate these issues and lead to practical JJ-FET logic devices.

Chapter 7 : Summary and Future Work

7.1 Thesis summary

Semiconductor nanowires are recognized as the potential candidate for the ultimate CMOS scaling, since they allow a GAA geometry for the best gate electrostatic control over the channel. Furthermore, thanks to the ability to fabricate radial nanowire heterostructures, namely core-(multi-)shell nanowires, a simultaneous quantum confinement and mobility enhancement of carriers in the core or shell regions can be realized. Engineering novel radial nanowire heterostructures as high-performance, ultra-scaled MOSFET channels requires a fundamental understanding of the heterostructure and an exquisite control of the fabrication process. On the other hand, for logic device applications at cryogenic temperatures, superconducting electronics are attractive thanks to its fast speed, low power and lossless signal transmission. Among them, JJ-FETs can provide excellent isolation between the input and output, have abrupt switching and small time constant, and share design similarities with standard MOSFETs to benefit from the state-of-the-art nano-fabrication techniques. In the first part of this thesis (Chapters 2, 3 and 4), we demonstrate a set of techniques to characterize the structural and electrical properties of radial nanowire heterostructures. These heterostructures combine strain engineering at nanoscale for mobility enhancement as well as a reduced dimensionality. We study in detail the nanowire morphology, strain distribution, band structures and carrier transport using TEM imaging, Raman spectroscopy, finite element modeling, and electrical measurements of nanowire MOSFETs. In the second part of the thesis (Chapters 5 and 6), we carry out a combined effort to theoretically justify and experimentally demonstrate the feasibility of JJ-FETs as building blocks for logic device applications. We develop a compact model of JJ-FETs operating in the short ballistic

regime that allows us to perform logic circuit simulation, and fabricate JJ-FETs based on the InAs quantum well heterostructure platform to show the actual device operation.

In Chapter 1, we introduce the technological advancements in the physical dimension scaling and the performance improvement at cryogenic operation temperatures of MOSFETs. We discuss the advantage of GAA MOSFETs using nanowires, particularly Si-Ge based radial nanowire heterostructures as channel. In addition, we introduce JJ and JJ-FET based superconducting electronics for logic device applications at cryogenic temperatures.

In Chapter 2, we present the VLS core growth, CVD shell growth, and structural analysis techniques for Si-Ge based core-(multi-)shell nanowires. We show that the elastic strain in core-(multi-)shell nanowires due to the lattice mismatch between the core and shell(s) depends on the nanowire diameter, shell thickness, Si_xGe_{1-x} alloy composition, and most interestingly the shell morphology. We perform TEM imaging to analyze the shell morphology of Ge-Si_xGe_{1-x} and Si-Si_xGe_{1-x} core-shell nanowires, revealing that while the core grown via VLS is largely cylindrical, the shell grown by CVD is faceted. The TEM data reveals that Ge-Si_xGe_{1-x} core-shell nanowires grow along <111> crystal direction and are terminated by six {112} planes, and Si-Si_xGe_{1-x} core-shell nanowires grow along either <110> or <112> direction and are terminated by {111}, {110}, and {113} planes, depending on the growth direction. Using the continuum elasticity model, we perform FEM simulations taking inputs from the experimental morphology to calculate the strain distributions in all three types of nanowires, showing compressive/tensile strain in the Ge/Si core. The strain coupled with lattice dynamic theory allows us to calculate the shifted optical phonon modes under strain in the core regions, which show good agreement with experimental values probed by Raman spectroscopy.

In Chapter 3, we report a highly strained Si layer coherently grown on Si_xGe_{1-x} nanowire substrates, perform comprehensive structural analysis, and demonstrate enhanced μ_e in MOSFETs using this nanowire as channel. We use Raman spectroscopy to probe the strain-induced shift of optical phonon frequencies in both core and shell regions, showing excellent agreement between the experimental data and calculations using the strain simulated from a continuum elasticity model coupled with lattice dynamic theory. We also perform a scaling study of n-type MOSFETs with highly doped source and drain using Si_xGe_{1-x}-Si core-shell nanowires as channel, and show that the tensile strain in the Si shell could lead to a 40% μ_e enhancement compared to bare Si nanowire MOSFETs.

In Chapter 4, we demonstrate the Si_xGe_{1-x}-Ge-Si core-double-shell strained nanowire heterostructure, which is designed such that in gated structures, holes populate the Ge shell, and electrons populate the Si shell. The combination of compressive strain in the Ge shell, and tensile strain in the Si shell leads to a mobility enhancement for both electrons and holes. We find an astounding enhancement of 500% for μ_h in the Ge shell than the Si counterpart, allowing us to extract ΔE_V in the two shells from the decoupled hole transport. We also study the impact of the Si and Ge shell thickness on the carrier transport to shed light on the optimization of the heterostructure for high-performance CMOS devices with symmetric electron and hole mobility.

In Chapter 5, we develop a compact model for JJ-FET circuit simulations and demonstrate its feasibility for logic and memory applications, assuming the JJ-FET operating in the short ballistic regime. We calculate the DC operation point for signal restoration and perform transient analysis to simulate the dynamic behavior of JJ-FETs. We find the output of the JJ-FET logic gate depends on the fan-out due to device hysteresis, distinct from the CMOS logic gate. We show that

this issue can be resolved if a dynamic logic gate with global clock is applied.

In Chapter 6, we experimentally demonstrate the operation of JJ-FETs using the InAs quantum well heterostructure as channel. We investigate the V_G dependence of I_C, G_N, V_0 and observe different V_G regimes. We also perform $I - V$, $C - V$ measurements of long-channel MOSFETs as control devices and self-consistent Poisson-Schrödinger simulations, which allow us to identify the different V_G regimes as electrons populating one or more electron subbands. We also discuss the discrepancy between ideal short ballistic JJ-FETs and the fabricated devices, and analyze how non-ideal JJ-FETs affect the realization of practical JJ-FET logic gates.

In Chapter 7, we conclude the thesis and suggest recommendations for future researches related to the implementation of practical JJ-FET logic devices.

7.2 Ongoing project and outlook on future work

In this thesis, we investigate the Si-Ge based radial nanowire heterostructure as candidate for the ultimate CMOS scaling. Future research can be performed to explore approaches for mass fabrication of these nanowire heterostructures through a scalable top-down approach instead of the bottom-up VLS synthesis. Alternatively, it is also worthy to research on techniques that allow a precise positioning of semiconductor nanowires prepared via VLS growth or other methods on the wafer scale. Potential pathways include applying a well-controlled post-growth transfer, and developing a method that can lead to an accurately guided growth, etc. We also fabricate JJ-FETs based on the InAs quantum well heterostructure platform, aimed to implement JJ-FET Boolean logic applications. Unfortunately, they fail to deliver the expected functionality as building blocks for practical logic devices, due to the poor oxide/channel interface and low crystal quality. Efforts

can be made in the future to develop a new MBE growth recipe that yields high crystal quality, as well as effective passivation techniques to decrease the interface trap density.

On the other hand, JJ-FETs using the Si platform can be explored, which is known for providing high quality oxide as well as oxide/semiconductor interface, and directly compatible to the standard Si CMOS technology. We have taken steps to develop process flow for Si-based JJ-FETs, and demonstrated planar JJs on phosphorus doped epitaxial Si films. We start with an intrinsic Si(100) substrate, followed by growing a Si epi-layer highly doped with phosphorus in our cold-wall CVD used for nanowire synthesis. The P-doped Si layer forms an Ohmic contact with the superconductor electrode and allows coherent Cooper pair transport. Prior to loading the Si substrate, the native oxide is removed by a wet etch of 1 min in 1: 80 diluted HF. Table 7.1 summarizes the growth conditions of the three P-doped Si CVD growths we examine in detail, where the growth names are the same as those in our growth catalog. We use PH_3 as precursor to introduce phosphorus dopants in the Si epi-layer, diluted in He at a ~ppm level. We adjust the precursor flow rate of SiH_4 and the flow rate ratio of SiH_4 over PH_3 to identify whether the CVD growth is temperature or mass transport limited, and if the doping concentration can be tuned. We use transfer length measurement (TLM) coupled with time-of-fight secondary ion mass spectrometry (ToF-SIMS) to determine the Si epi-layer thickness and the phosphorus doping level. TLM provides the P-doped Si layer sheet resistance R_S and ToF-SIMS determines the layer thickness t, allowing us to calculate the layer resistivity $\rho = R_S \cdot t$ and thus the doping level. The TLM device consists of a sequence of 150 μm × 80 μm Ni pads with different spacings (L) between their long edges, with $L < 15$ μm to minimize the effect of current spreading between adjacent pads during $I - V$ measurements. The device fabrication process includes one EBL, one electron beam evaporation of 80 nm Ni and metal lift-off. Figure 7.1(a-d) presents the of L dependence data

of the two-point resistance between two adjacent Ni pads (R_{2PT}) for TLM devices fabricated on the intrinsic Si substrate [panel (a)], NW247 [panel (b)], NW256 [panel (c)] and NW247 [panel (d)], respectively, along with their linear fits in panels (b-d). Figure 7.1(a) shows that R_{2PT} does not scale with L for TLM devices on the intrinsic Si substrate, indicating a large Schottky barrier between Ni and Si, and R_{2PT} is dominated by R_C. On the other hand, R_{2PT} exhibits a clear linear relation with L in Fig. 7.1(b-d), and allows us to extract R_S and R_C from the slope and y-axis intersection of the linear fit for the R_{2PT} vs. L data. The extracted R_S and R_C of the TLM devices fabricated on the three growths are summarized in Table 7.2. The intrinsic Si wafer has a labeled ρ of 1500 - 3000 Ω·cm and a substrate thickness $t = 375$ μm that can contribute to the electrical conduction, corresponding to $R_S = \rho/t =$ 40 - 80 kΩ/sq ≫ the measured R_S of the three growths. Consequently, we assume only the surface P-doped Si layer is responsible for the electron conduction in TLM devices fabricated on the three growths. We perform ToF-SIMS on samples of the three growths to determine t of the Si epi-layer. ToF-SIMS involves a fast sputtering to dig into the sample and a slow sputtering to knock out the surface atoms for analysis, leaving a crater size of about 100 μm × 100 μm as the analysis area. The flight time between the sample and detector of these knocked-out atoms is determined by their mass, and serves as the signature to distinguish different types of atoms. Theoretically ToF-SIMS itself can identify both the doping level and layer thickness simultaneously, however, it needs a P-doped Si substrate with an exactly known doping level for calibration. Figure 7.2(a-c) presents the SIMS data showing the counts of phosphorus and oxygen atoms vs. the depth of the sputtered crater for the three growths, shown with red and blue lines, respectively. The oxygen counts data has a small hump near the surface peak and marks the interface between the intrinsic Si substrate and the P-doped epi-layer, due to residual SiO_2 on the Si substrate surface before CVD growths, allowing us to determine t of the

epi-layer. We calculate ρ of the Si epi-layer using the measured R_S and t, and then convert it to the corresponding phosphorus doping concentration [168]. t, ρ and the phosphorus doping concentration of the Si epi-layers for the three growths are summarized in Table 7.2. The data shows the CVD growth rate is limited by mass transport, because a higher SiH_4 flow rate leads to a larger t. In addition, increasing the flow rate ratio of PH_3 over SiH_4 does not yield a higher phosphorus doping concentration, due to the limit imposed by the solid solubility of phosphorus in Si at the CVD growth temperature. Figure 7.3 presents the temperature dependence data of the solid solubility of common dopants in Si, which indeed suggests an upper limit of the phosphorus doping concentration in the low 10^{19} cm^{-3} range at $T < 500$ °C [169]. Alternatively, ion implantation of phosphorus into the Si substrate can be applied for a more precise control over the doping level and junction depth.

Table 7.1: CVD growth conditions of three P-doped epitaxial Si film growths

Growth name	SiH_4 gas flow (s.c.c.m.)	PH_3 gas flow (s.c.c.m.)	Growth pressure (mTorr)	Growth temperature (°C)	Growth time (min)
NW247	60	50	75	485	60
NW256	40	100	98	480	60
NW257	15	100	81	480	60

Table 7.2: R_C and R_S of the TLM devices, along with t, ρ and the phosphorus doping concentration of the Si epi-layer for the three growths

Growth name	R_C (kΩ·µm)	R_S (kΩ/sq)	t (nm)	ρ (mΩ·cm)	Phosphorus doping level (10^{19} cm^{-3})
NW247	0.87	0.93	50	4.7	1.3
NW256	1.2	1.4	25	3.5	1.9
NW257	7.7	5.3	12	6.4	0.9

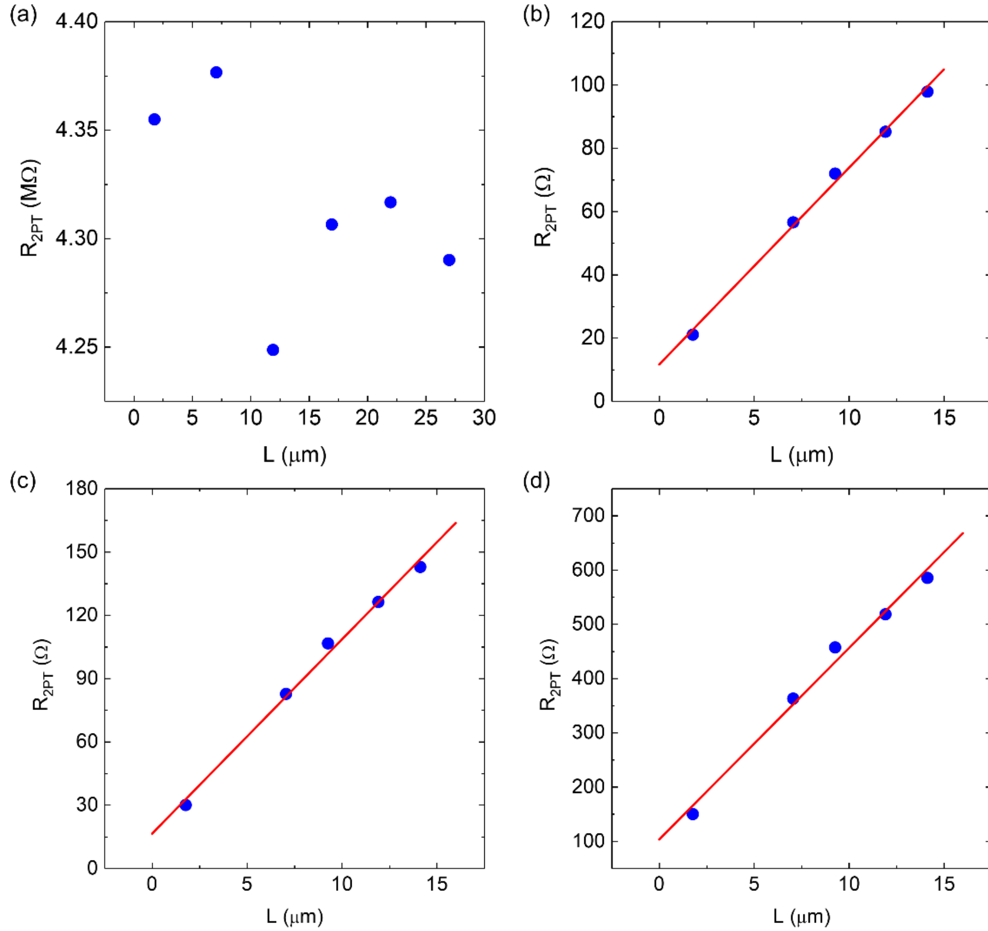

Figure 7.1: R_{2PT} vs. L for TLM devices fabricated on (a) the intrinsic Si substrate and (b-d) the three P-doped Si growths NW247, NW256 and NW257, respectively.

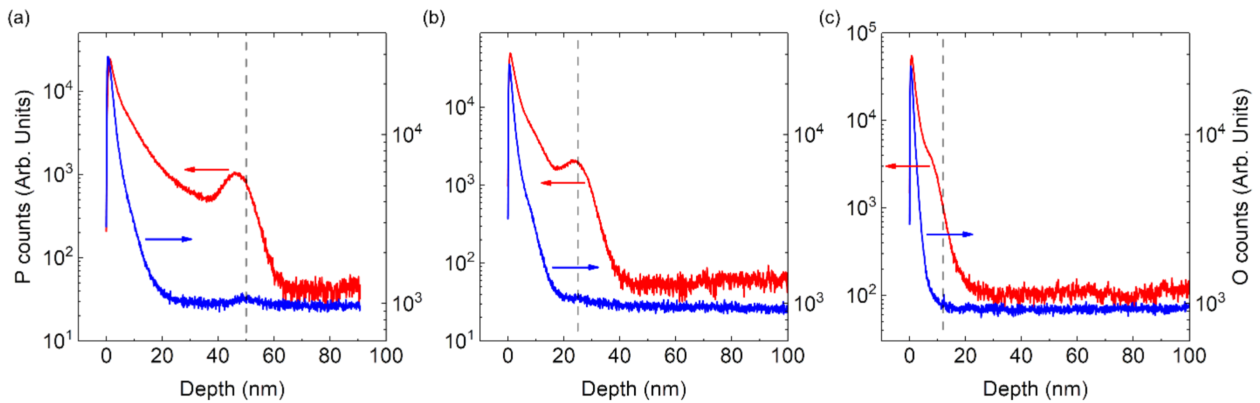

Figure 7.2: SIMS data of the phosphorus (red line) and oxygen (blue line) atom counts vs. the sputtered crater depth, corresponding to the left and right y-axes in log scale for the three P-doped Si CVD growths

(a) NW247, (b) NW256 and (c) NW257, respectively. The left and right *y*-axis labels in panels (a) and (c) apply to panels (a-c). The position corresponding to the Si epi-layer thickness is marked with a vertical dashed line in each panel. Figure 7.2: continued.

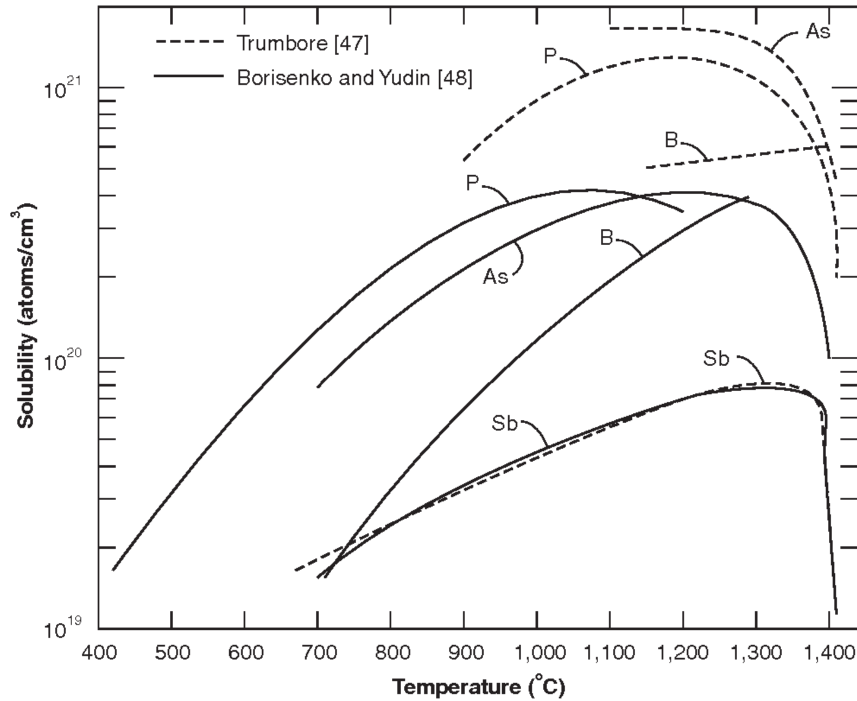

Figure 7.3: Solid solubility of common dopants in Si. (Figure adapted from Ref. [169])

Figure 7.4 uses schematics to illustrate our fabrication process of Si-based JJ-FETs. We first disperse nanowires (any type of the nanowires studied in this thesis) onto the Si substrate with a P-doped epi-layer, and deposit 20 nm of Al using MBE [panels (a-b)]. The Si native oxide has to be removed prior to the Al deposition, which can be realized by *in-situ* hydrogen milling in the MBE system or *ex-situ* HF etching (15 sec in 1:80 HF diluted in DI water). Nanowires are detached by sonicating the substrate in DI water for 10 min, leaving nano-gaps in the Al film [panel (c)]. The thickness of the Al film needs to be chosen carefully, because a too thin Al film (< 15 nm) gets oxidized easily during the process particularly at the ALD stage where the sample is heated up and exposed to air, while a too thick Al film (> 30 nm) will cover the nanowire to prevent it

from being sonicated off the substrate. We then perform the 1st EBL, followed by the wet etch of Al and RIE etch of ~60 nm Si to define the contour of JJ-FETs for the isolation of individual devices [panels (d-e)]. The Al etching process has been detailed in Section 6.2 and the RIE is performed in the etcher model Plasma Therm 2, with HBr/Cl_2 plasma using a gas flow of 25.4/4 sccm at 28 mTorr. The RIE has two steps, consisting of 400 V power for 15 sec to remove the Si native oxide followed by 275 V power for 30 sec to etch Si (DC power mode). We then deposit 10/70 nm Ti/Au on source and drain regions to promote the wire bonding and probing through the 2nd EBL, electron beam evaporation and lift-off [panel (f)]. A conformal gate oxide of 10 nm Al_2O_3 is then deposited using plasma enhanced ALD of 100 cycles at 250 °C, followed by the 10/70 nm Ti/Au gate contact patterned using the 3rd EBL, electron beam evaporation and lift-off [panels (g-h)]. Finally, the Au surface of the source/drain metals is exposed with EBL followed by the removal of ALD oxide in diluted HF (optional and usually not executed as explained in Section 6.2). All EBL steps use PMMA A6 resist as detailed in Section 3.7, which is thick enough to avoid a complete etch through of unexposed regions during the RIE stage. The most challenging part of the fabrication process is the removal of the Si native oxide prior to Al metallization and the Al deposition itself. The process we have developed for the Si-based JJ-FETs cannot guarantee a transparent Al/semiconductor interface as the JJ-FETs based on the InAs quantum well heterostructure discussed in Chapter 6. Partial removal of the native oxide or oxide regrowth during the substrate loading, and impurity contamination in the Al deposition stage will result in a barrier at the Al/Si interface and impede the coherent transport of Cooper pairs.

We fabricate and measure two sets of Si-based JJ-FETs on growth NW247, using both the *in-situ* hydrogen milling in the MBE system and *ex-situ* HF etching approach to remove the Si native oxide before Al deposition. Figure 7.5(a) shows the optical image of a completed Si-based

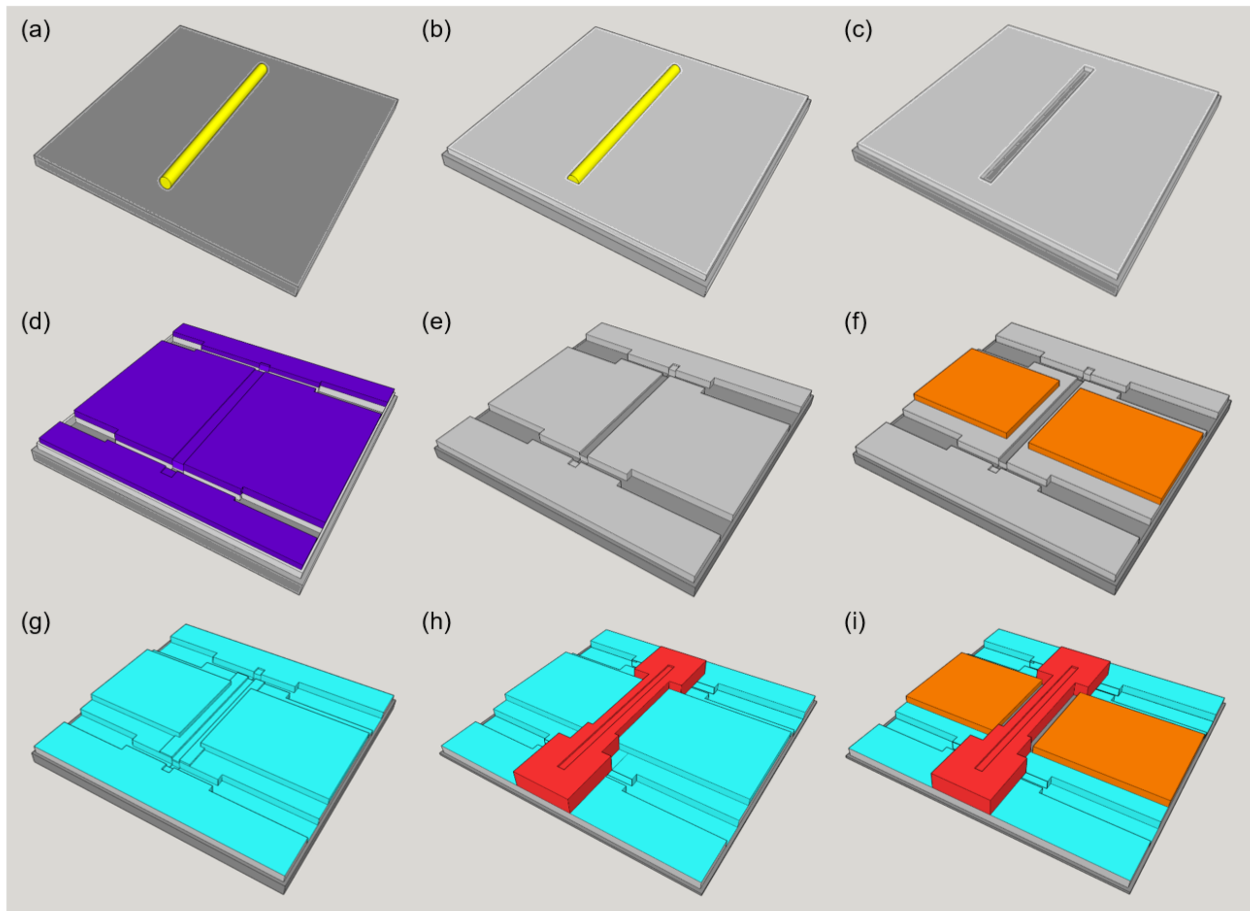

Figure 7.4: Process flow to fabricate Si-based JJ-FETs. (a) Disperse nanowires onto the Si substrate. (b) Deposit Al film in an MBE system using nanowires as shadow mask after the removal of Si native oxide. (c) Sonicate nanowires off the substrate in DI water, leaving nano-gaps on the substrate. (d) Spin on PMMA, followed by EBL, wet etch and RIE to form the device contours for isolation. (e) Strip PMMA in acetone. (f) Perform EBL, Ti/Au deposition through electron beam evaporation and lift-off on source and drain regions. (g) Deposit Al_2O_3 as gate dielectric using ALD. (h) Perform EBL, Ti/Au electron beam evaporation and lift-off to define the gate contact. (i) Perform EBL and selectively etch the oxide film to expose the Au area (optional).

JJ-FET fabricated with the *ex-situ* HF etching method, where the core region of the device is highlighted by a circle whose zoom-in version is presented in Fig. 7.5(b), with the three terminals labeled. In Figure 7.5(b), we see edges on the Si substrate near Al (highlighted by dashed lines and an arrow), because for this particular device the EBL mask we use for the Si RIE has the same

shape but smaller than that for the Al wet etch. The HBr/Cl_2 plasma sometimes undercuts the Al under PMMA and potentially damages the channel if the same mask is used for both the Al wet etch and Si RIE. Although this encroachment of Al does not always happen during the Si RIE stage, for safety we usually leave a margin of 1 - 2 μm between the outlines of the EBL masks for Al and Si etching. Figure 7.5(c) shows the SEM image of a nano-gap defined by the nanowire shadow mask, corresponding to the device fabrication stage presented in Fig. 7.4(e). L_G defined using this technique usually leads to a value smaller than 50 nm, far below the minimum feature size of ~200 nm that can be realized in our EBL system using PMMA as resist.

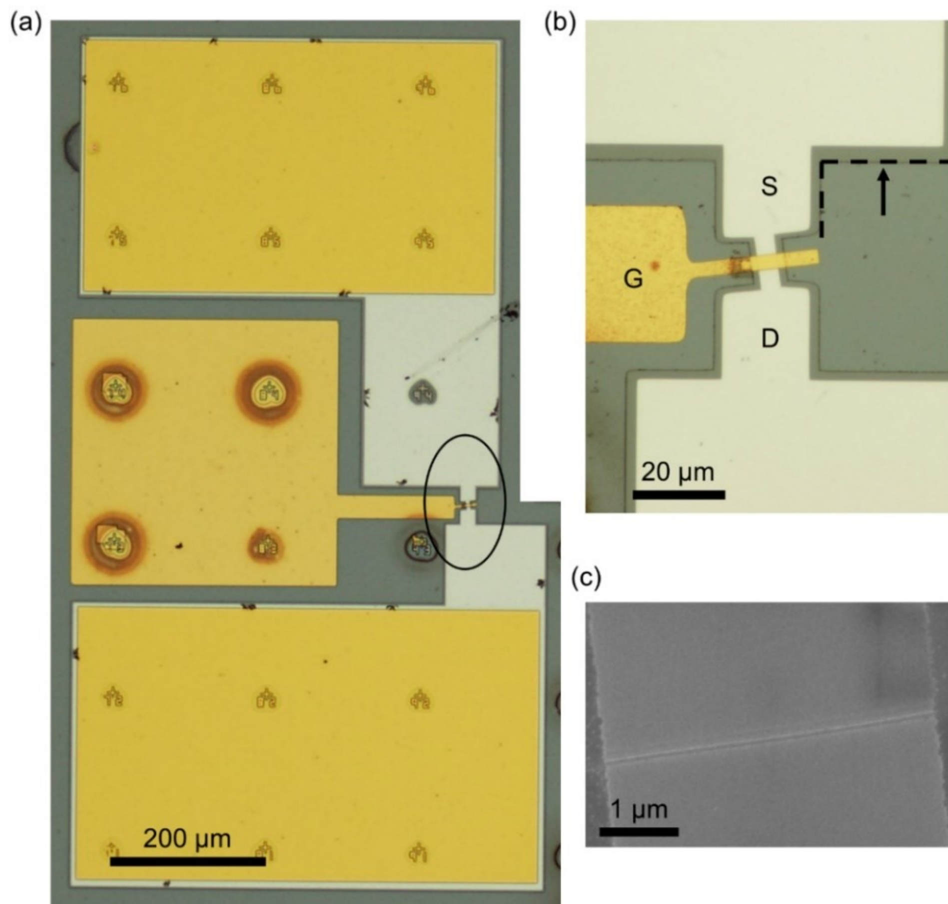

Figure 7.5: Imaging of Si-based JJ-FETs, using *ex-situ* diluted HF etching to remove the Si native oxide prior to the MBE Al deposition. (a) Optical image of a completed device. (b) Zoom-in version of panel (a), corresponding to the circled region. (c) SEM image of the nano-gap.

Next, we discuss the charge transport properties of our Si-based JJ-FETs. Figure 7.6(a) presents the I_{Bias} dependence data of dV/dI for a Si-based JJ-FET whose native SiO_2 is removed using a non-optimized *in-situ* hydrogen milling recipe, acquired at $T = 17$ mK, 1 K and 2 K, respectively. Although the shape of dV/dI data shows a strong temperature dependence and becomes flat at $T > T_C$ to suggest the superconductivity of Al contacts, the device is very resistive in the mid kΩ range that is much larger than the value predicted by R_S of growth NW247, and does not show any proximity effect due to Cooper pairs breaking to quasiparticles at the Al/Si interface. The device is effectively a series of two tunneling junctions instead of a JJ. We therefore conclude that the device suffers from a bad Al-to-Si contact, and the dV/dI value is dominated by a large R_C. Figure 7.6(b) shows the SEM image of the nano-gap corresponding to the device fabrication stage presented in Fig. 7.4(e), where we notice significant damages on the Si surface due to non-optimized hydrogen milling process.

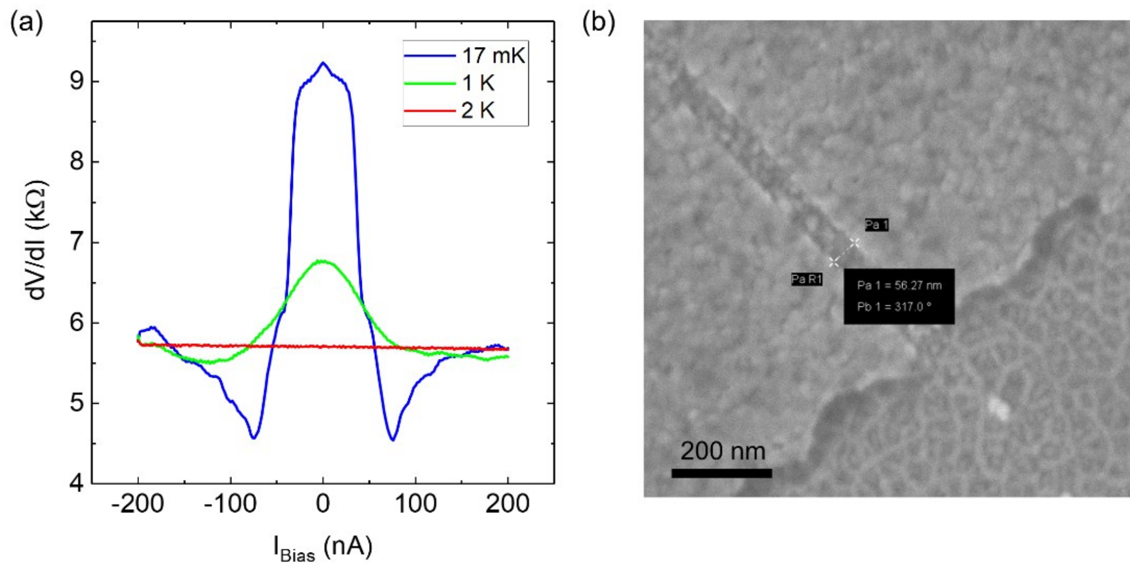

Figure 7.6: (a) dV/dI vs. I_{Bias} data of a failed Si-based JJ-FET, using *in-situ* hydrogen milling to remove the Si native oxide prior to Al deposition. (b) SEM image of the nano-gap, showing Si surface damages.

Figure 7.7 shows the electrical measurement data acquired in the dilution refrigerator, for

a Si-based JJ-FET fabricated with the *ex-situ* HF etching method to remove the native SiO_2 prior to Al deposition. This device does not show any gate modulation over the channel, so no V_G dependence data will be discussed. Figure 7.7(a) shows the I_{Bias} dependence data of dV/dI and V_{DC} at $T = 17$ mK, presenting two abrupt transitions at $I_{Bias} = 55$ and 67 μA. We have $R_N = 14$ Ω for the 1st switching of smaller I_C, corresponding to an $I_C R_N$ product of 770 μV, which is too large for a JJ with Al contacts. Its largest possible value in the short ballistic limit is only 675 μV as discussed in Section 6.6. We also note that the 1st switching is unlikely due to I_{Bias} exceeding the maximum Cooper pair current that can be carried by the 20 nm Al layer, which has a critical current density > 0.1 A/μm^2 [170]. Figure 7.7(b) presents the perpendicular magnetic field (B_Z) dependence data of dV/dI at $T = 17$ mK, with B_Z ranging from 0 to 2 T in log scale. We observe an abrupt transition between the superconducting and resistive state for the 1st switching, with a critical perpendicular magnetic field (B_C) of ~35 mT that is close to the typical value of an Al thin film. However, the 2nd switching is not abrupt, where dV/dI increases gradually against B_Z without a noticeable B_C. Figure 7.7(c) shows the I_{Bias} dependence data of dV/dI at $T = 1.5$ K, I_C of the 1st switching disappears and therefore the device becomes resistive at zero I_{Bias}, while I_C of the 2nd switching is still considerable at 61 μA. Our MBE Al film usually has $T_C = 1.4$ K, which can explain the disappearance of the 1st switching and suggest that the 2nd switching originates from a material with higher T_C in the device. Figure 7.7(d) presents the contour plot showing the I_{Bias} and B_Z dependence data of V_{DC} at $T = 17$ mK, revealing distinct behaviors between the two switching. I_C of the 1st switching decreases rapidly and the transition becomes less abrupt as B_Z increases, while I_C of the 2nd switch is insensitive to B_Z in this range. Figure 7.7 data indicates that the measured device consists of two JJs connected in series, with one JJ having a larger I_C, B_C and T_C than the other. Figure 7.8(a) presents the B_Z dependence data of dV/dI same as that shown in

Fig. 7.7(b) but with B_Z in linear scale, showing that the 2nd switching adds an extra 9 Ω at $B_Z =$ 1.25 T. We measure multiple devices on the same chip and observe similar behaviors. Particularly noteworthy, very thin Al film of a few monolayers has a higher T_C and B_C than thicker or bulk Al [171], and Al-Si alloy prepared with rapidly quenched solidification with a Si ratio of 30% has an enhanced $T_C = 6.2$ K [172]. Figure 7.8(b) presents the room temperature $I - V$ characteristics of the same device discussed above before and after cooling and measurements in the dilution refrigerator, showing a reduced resistance from 1.4 kΩ to 64 Ω. The resistance of 1.4 kΩ is smaller than that of the device discussed in Fig. 7.6, but still much larger compared to the value calculated using R_S and a W/L ratio of 80 (4 μm/50 nm), ~10 Ω, indicating a significant barrier at the Al/Si interface after the MBE deposition. Although the examination of the device with SEM after the measurement [(Fig. 7.9(b)] reveals no obvious change or damage compared to its as-fabricated form [(Fig. 7.9(a)], we believe electro-migration or diffusion of Al into the Si nano-gap occurs during the measurement, and results in a section of ultra-thin Al or Al-Si alloy with enhanced T_C and B_C. The Al electro-migration and diffusion can be caused by the electrostatic discharge (ESD) during the cooling process in the dilution refrigerator, as we have the experience where the gates of multiple devices become leaky after cooling. The junction itself can be a continuous new superconductor, it is also possible that the new superconductor intermixes with the P-doped Si in the junction and induces proximity effect. The absence of a Fraunhofer pattern in Fig. 7.7(d) precludes the possibility of the Si superconductivity proximitized by the 20 nm Al contacts. Based on the findings discussed above, we associate the 1st switching in Fig. 7.7(a) with a thermal transition due to the Joule heating of the source/drain Al contacts from the peripheral resistive elements (bonded wires and chip-mount resistors), and the 2nd switching with the ultra-thin Al or Al-Si alloy in the channel, which has the same thermal origin but a higher T_C.

Future research on Si-based JJ-FETs can focus on solving the two issues discussed above. Efforts can be conducted to improve the Al/Si interface by optimizing the recipe of the *in-situ* hydrogen milling, since the diluted HF etching method cannot provide a perfectly oxide-free interface. It is also important for the electrical characterization instrument to provide an ESD free environment to prevent the electro-migration or diffusion of the MBE Al. Moreover, superconducting bonding wires are preferred for measurements in the dilution refrigerator, in case that pre-mature switching of JJs occurs due to Joule heating instead of I_{Bias} exceeding I_C.

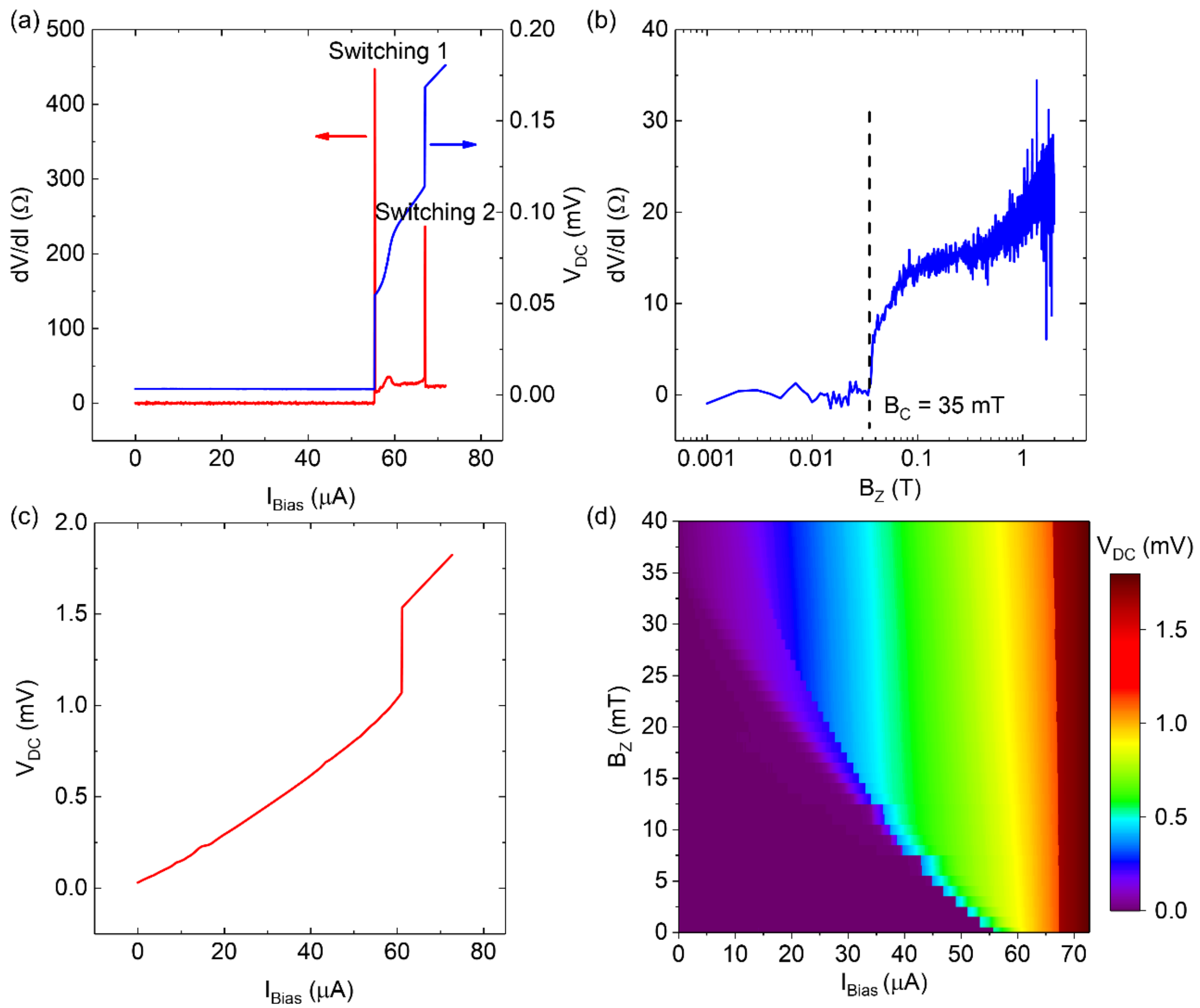

Figure 7.7: Electrical characteristics of a Si-based JJ-FET with Al contacts. (a) dV/dI vs. I_{Bias} and V_{DC} vs. I_{Bias} at $T = 17$ mK, presented in the red and blue solid line. (b) dV/dI vs. B_Z from 0 to 2 T at $T = 17$

mK. $B_C = 35$ mT of the 1st switching is marked with a vertical dashed line. (c) V_{DC} vs. I_{Bias} at $T = 1.5$ K. (d) Contour plot showing V_{DC} vs. I_{Bias} and B_Z at $T = 17$ mK. Figure 7.7: continued.

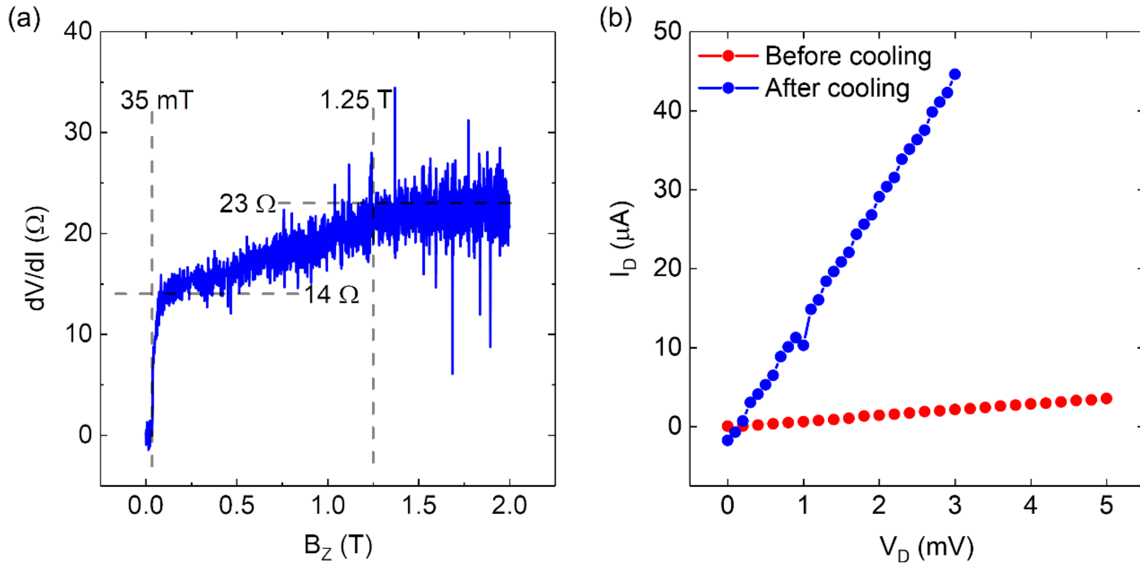

Figure 7.8: (a) dV/dI vs. B_Z at $T = 17$ mK for a Si-based JJ-FET with Al contacts. R_N of the 1st switching (14 Ω) and the total R_N of the two switching (23 Ω) are marked by horizontal dashed lines. B_Z values corresponding to the two JJs becoming resistive (35 mT and 1.25 T) are labeled with vertical dashed lines. (b) $I - V$ characteristics at $T = 300$ K for the same Si-based JJ-FET, before and after cooling and measurements in the dilution refrigerator.

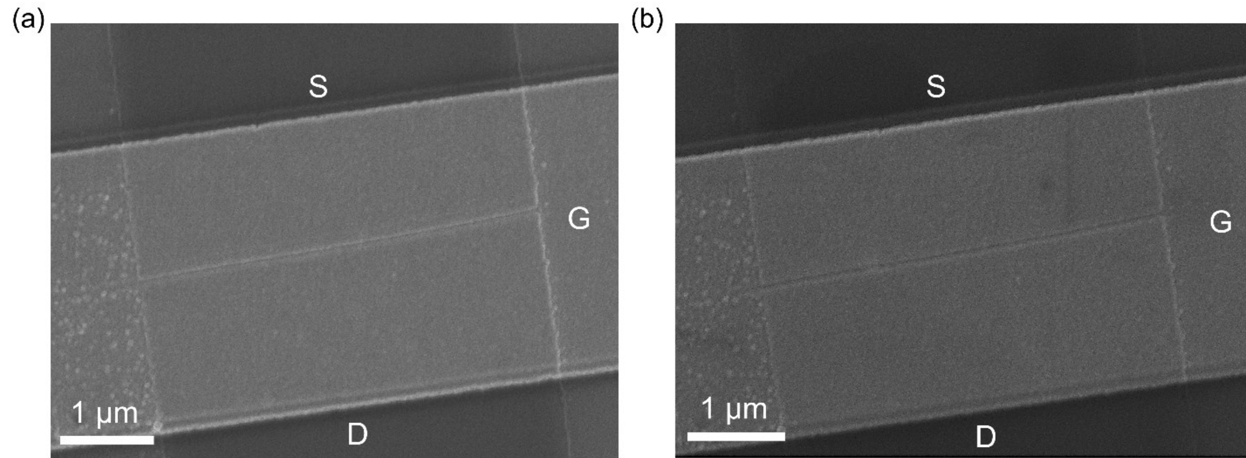

Figure 7.9: SEM images of the Si-based JJ-FET whose electrical measurement results are shown in Fig. 7.7 and Fig. 7.8, (a) before and (b) after the cooling and measurements in the dilution refrigerator. The three terminals gate, drain and source are labeled in both panels.

Appendix A: List of Journal Publications

1. **F. Wen**, J. Shabani and E. Tutuc, "Josephson Junction Field-effect Transistors for Boolean Logic Cryogenic Applications", IEEE Transactions on Electron Devices, 66 (12), 5367-5374, 2019.

2. **F. Wen** and E. Tutuc, "Strained Si_xGe_{1-x}-Ge-Si core-double-shell nanowire heterostructures for simultaneous hole and electron mobility enhancement", Applied Physics Letters 113 (11), 113102, 2018.

3. **F. Wen** and E. Tutuc, "Enhanced Electron Mobility in Non-Planar Tensile Strained Si Epitaxially Grown on Si_xGe_{1-x} Nanowires", Nano letters 18 (1), 94-100, 2017.

4. **F. Wen**, D. C. Dillen, K. Kim, and E. Tutuc, "Shell Morphology and Raman Spectra of Epitaxial Ge-Si_xGe_{1-x} and Si-Si_xGe_{1-x} Core-Shell Nanowires", Journal of Applied Physics 121 (23), 234302, 2017.

5. W. Hsu, **F. Wen**, X. Wang, Y. Wang, A. Dolocan, A. Roy, T. Kim, E. Tutuc, and S. K. Banerjee, "Laser Spike Annealing for Shallow Junctions in Ge CMOS", IEEE Transactions on Electron Devices, 64 (2), 346-352, 2017.

6. W. Hsu, X. Wang, **F. Wen**, Y. Wang, A. Dolocan, T. Kim, E. Tutuc, and S. Banerjee, "High Phosphorous Dopant Activation in Germanium Using Laser Spike Annealing", IEEE Electron Device Letters, Vol. 37, Issue 9, 2016.

7. D. C. Dillen, **F. Wen**, K. Kim, E. Tutuc, "Coherently Strained Si–Si_xGe_{1-x} Core–Shell Nanowire Heterostructures," Nano Lett., 2016, 16 (1), 392–398, 2015.

Appendix B: List of Symbols

A_1, A_2	Constants used to calculate Si_xGe_{1-x} composition with Raman spectrum
B_C	Critical perpendicular magnetic field of superconductor
B_Z	Perpendicular magnetic field
C_{it}	Interface trap capacitance
C_{ij}	Entry of material stiffness matrix
C_L	Load capacitance of logic gate
C_{ox}	Gate oxide capacitance
C_s	Semiconductor capacitance
C_{sim}	Simulated capacitance in NextNano
C_{Ω}	Gate capacitance per unit length for nanowire MOSFET
$C-V$	Capacitance-voltage
d	Diameter of nanowire
D_{it}	Interface trap density
dV/dI	AC differential resistance of JJ-FET
e	Electron charge
E_0	Energy of molecule/crystal ground state
E_C	Conduction band energy
E_{eff}	Effective electric field
E_{g0}	Unstrained bandgap
E_F	Fermi level
$\boldsymbol{E_{inc}}$	Incident light polarization in Raman spectroscopy

E_{JF}	JJ-FET total energy
$\boldsymbol{E_{scat}}$	Scattered light polarization in Raman spectroscopy
E_V	Valence band energy
G_{ch}	Channel conductance of MOSFET
G_{kink}	Channel conductance where kink occurs
G_N	Normal state channel conductance of MOSFET/JJ-FET
h	Planck's constant
I_{Bias}	DC biasing current
I_C	Critical current of JJ/JJ-FET
I_D	Drain current of MOSFET
I_{DS}	Current through JJ-FET
I_J	Josephson current
I_R	Return current of JJ
$I-V$	Current-voltage
k_B	Boltzmann constant
L	Length between adjacent pads in TLM device
L_C	Josephson inductance
L_G	Gate length of MOSFET/JJ-FET
m^*	Effective mass
m_0	Electron mass
n, p	Three-dimensional electron or hole density in TCAD simulation
n_{2D}	Two-dimensional electron density
n_e	Three-dimensional electron density in NextNano simulation

P	Power consumption
p, q, r	Phonon deformation potential
Q	Stewart-McCumber parameter
q_G	Channel charge of MOSFET/JJ-FET
$\boldsymbol{R}(\boldsymbol{i})$	Raman tensor
R_{2PT}	Two-point resistance between adjacent pads in TLM device
R_C	Contact resistance of MOSFET
R_{ch}	Channel resistance of MOSFET
R_{ext}	Nanowire MOSFET extension resistance
R_N	Normal state resistance of JJ/JJ-FET
R_{Total}	Total resistance of nanowire MOSFET
SS	Subthreshold swing
t	Thickness contributing to conduction for TLM device
T	Temperature
T_C	Critical temperature of superconductor
t_f	Falling delay of logic gate
t_H	Hold time of logic stage
T_i, T_f	Lattice temperature in Abaqus simulation
t_{ox}	Gate oxide thickness of MOSFET
t_{PW}	Pulse width time of clock signal
t_r	Rising delay of logic gate
t_{sh}	Nanowire shell thickness
$V_{G,Hi}$	Input gate voltage, logic high

$V_{G,Lo}$	Input gate voltage, logic low
V_0	Characteristic voltage of JJ/JJ-FET
V_{CLK}	Clock signal for dynamic JJ-FET logic gate
V_D	Drain voltage of MOSFET
V_{DC}	DC voltage across JJ-FET
V_{DD}	Supply voltage of logic circuit
V_{DS}	Voltage across JJ-FET
v_F	Fermi velocity
V_G	Gate voltage of MOSFET/JJ-FET
$V_G - V_T$	Gate overdrive of MOSFET/JJ-FET
V_{IN}	Input voltage of logic gate
V_{kink}	Gate voltage where kink in occurs of MOSFET/JJ-FET
V_{OUT}	Output voltage of logic gate
V_T	Threshold voltage of MOSFET/JJ-FET
$V1, V2$	Complimentary pair of SRAM storage value
W	Channel width of MOSFET/JJ-FET
α	Constant electric field scaling factor of CMOS
α, ε	Generalized scaling factor of CMOS
$\alpha_d, \alpha_w, \varepsilon$	Generalized selective scaling factor of CMOS
α_R	Gain factor of JJ-FET logic gate
β	Transconductance of critical current of JJ-FET
γ	Back-reaction factor of JJ-FET
Δ	Position in the Brillouin zone or superconductor gap voltage

ΔE_C^i	Energy shift of conduction band valley i due to strain
$\Delta E_{g,av}$	Change of bandgap energy
ΔE_V	Valence band offset
δE_V	Energy shift of valence band valley due to strain
ε_{ij}	Strain tensor
ε_r	Dielectric constant
$\theta, \theta_v, \theta_\mu$	Temperature scaling factors of cryogenic CMOS
λ	Electron mean free path
λ_{inc}	Incident light wavelength in Raman spectroscopy
λ_{scat}	Scattered light wavelength in Raman spectroscopy
μ_e	Electron field-effect mobility of *n*-type MOSFET
μ_{eff}	Carrier effective mobility of MOSFET
μ_h	Hole field-effect mobility of *p*-type MOSFET
ξ_0	Cooper pair coherence length
ρ	Resistivity
σ_{ij}	Stress tensor
τ_{min}	Minimum gate delay of the JJ-FET inverter
φ_s	MOS surface potential
φ_{sc}	Superconductor macroscopic phase
Ψ	Cooper pair condensate function
ω_i	Strained phonon frequency
ω_{i0}	Unstrained phonon frequency
$\Xi_d^i, \Xi_u^i, a, b_1, b_2$	Band deformation potentials

Appendix C: List of Acronyms

ALD	Atomic layer deposition
CDS	Core-double-shell
CMOS	Complementary metal-oxide-semiconductor
CVD	Chemical vapor deposition
DIBL	Drain induced barrier lowering
EBL	Electron beam lithography
EOT	Effective oxide thickness
ESD	Electrostatic discharge
FEM	Finite element method
GAA	Gate-all-around
HF	Hydrofluoric acid
JJ	Josephson junction
JJ-FET	Josephson junction field-effect transistor
MBE	Molecular beam epitaxy
MOSFET	Metal-oxide-semiconductor field-effect transistor
RCSJ	Resistively and Capacitively shunted junction
RIE	Reactive ion etching
SEM	Scanning electron microscopy
SFLS	Supercritical fluid-liquid-solid
SRAM	Static random access memory
TEM	Transmission electron microscopy
TLM	Transfer length measurement

ToF-SIMS	Time-of-fight secondary ion mass spectrometry
VCCS	Voltage controlled current source
VLS	Vapor-liquid-solid

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