Design of custom ASIC for front-end electronics in a 130 nm CMOS process

by

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Thesis

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Abstract

Researchers at Birkeland center of space science at the University of Bergen is developing an instrument to be attached to a satellite, to measure energetic particles in the atmosphere and particle precipitation. This instrument will consist of a radiation sensor developed by SINTEF and custom electronics developed at the University of Bergen.

This thesis covers the development and simulations of aforementioned electronics. The process of designing and developing a charge sensitive amplifier, a shaping amplifier and bias current supply circuit.

A functional amplifier was designed and implemented and its functionality is proven with simulation results. Some work remains to make the amplifier, fully functional according to the requirements of the instrument.

Preface

This thesis was carried out at the University of Bergen as part of my studies in the Department of Physics and Technology. The work was carried out during the autumn semester 2017 and the spring of 2018.

This thesis is part of the DEEP project, which is in its starting phase, at Group 3, Birkeland Centre for Space Science (BCSS). The goal of the thesis was to specify the specifications and requirements for the complete instrument, and then to design and develop the analogue electronics-part.

My earlier electronics-experience was focused on the digital electronics, so analogue integrated circuits was a challenging subject to me. Much of the work of this thesis was getting the feel of the behaviour of transistors, amplifiers and integrated circuits, and learning the tools.

Acknowledgements

Thank to professor Kjetil Ullaland, my supervising professor, associate professor Johan Alme, and PHD student Are Haslum at University of Bergen.

Thanks to Hilde Nesse Tyssøy, Johan Stadsnes, Finn Søraas at the Birkeland Centre for Space Science, and Dieter Röhrich at the Subatomic physics-group.

Thanks to friends, family, my co-students in room 312, and BCSSs coffee machine for an endless supply of coffee.

Fredrik Lindseth

Bergen, June 2018

Contents

Glossary

anisotropic The property of being directionally dependent, which implies different properties in different directions.

CMOS Complementary Metal Oxide Semiconductor. An integrated circuit technology consisting of p-type and n-type transistors. As opposed to bipolar transistors.

Coronal Mass Ejection An event that occurs on the suns surface that releases enormous amounts of energetic particles. These events are the cause of geomagnetic storms that affect radio transmissions and satellites and can disable complete power grids.

DEEP An instrument, and a project at the Birkeland Centre for Space Science, at University of Bergen.

Energetic particle precipitation is a shower of energetic particles hitting the atmosphere. These originate from solar events.

flux The rate of particles flowing trough an area.

front end electronics The electronics between a detector and a digital system. Typically an integrated circuit consisting of a Charge Sensitive Amplifier and a shaping filter.

PIN diode A P-intrinsic-N diode consisting of a p-doped part and a n-doped part with an undoped intrinsic area in between. Commonly used as radiations detectors.

Semiconductor Intellectual Property Core A block of finished circuitry bought from a vendor. May be licensed to another party or can be owned and used by a single party alone.

SINTEF The largest independent research organisation in Scandinavia, headquartered in Trondheim, Norway.

Solar Proton Events An event that occurs when particles emitted by the sun become accelerated. These particles penetrate the ionosphere and can cause significant damage to spacecraft and astronauts.

Acronyms

ADC Analogue to Digital Converter.

ASIC Application Specific Integrated Circuit.

BCSS Birkeland Centre for Space Science.

COTS Commercial Of The Shelf.

CSA Charge Sensitive Amplifier.

DEEP Distribution of Energetic Electron and Proton.

ENC Equivalent Noise Charge.

EPP Energetic Particle Precipitation.

FPGA Field Programmable Gate Array.

FWHM Full Width Half Maximum.

keV kilo electron Volt.

LNA Low Noise Amplifier.

MPW Multi Project Wafer.

PASA PreAmplifier ShAper.

RMS Root Mean Square.

SNR Signal to Noise Ratio.

TSMC Taiwan Semiconductor.

UIB University of Bergen.

CHAPTER 1

Introduction

The Earth's atmosphere is continuously bombarded with charged particles from outer space and the Sun. These are the particles that cause the northern lights and affect the performance of the global positioning systems, and also the upper atmosphere, and potentially the climate.

There are lots of unknowns in space weather and scientists are not sure how Energetic Particle Precipitation (EPP) affects the chemistry and temperature in the atmosphere. Accurate measurements to find the extent of these effects out has not been done, measurements of the deposited energy in particular.

The previous climate assessment model, as shown in Figure 1, only considers photons from the Sun, but has not yet included the energy associated with EEP. To do so better measurements of in particular energetic electrons, i.e. those with 30 keV and up, are needed.

1.1 The DEEP-instrument

The acronym DEEP stands for Distribution of Energetic Electron and Proton and is an ongoing project at the Birkeland Centre for Space Science (BCSS) at University of Bergen aimed at designing an instrument capable of providing a solid quantification of energetic electron precipitation.

If this project is successful a better quantification of the EPP will enable researches to better estimate the associated impact on changing chemistry and temperature in the middle atmosphere. [19].

To achieve these goals the researchers need to measure the angular distribution of the incoming particles relative to the Earth's magnetic field lines and

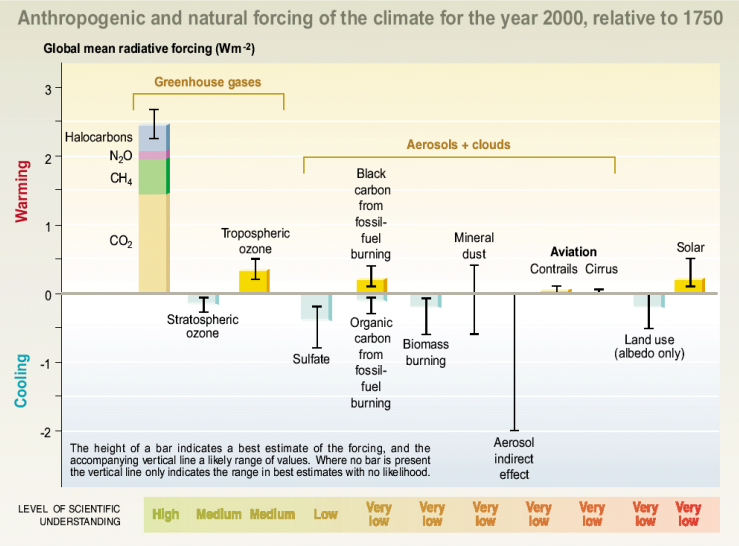

Figure 1.1: A schematic overview of the different effects on the global climate. The category Energetic particle precipitation belongs to is the rightmost column, "Solar" [9]

the energy of these particles.

As the angular distribution typically is highly anisotropic, looking at high or low angles give an over- or an underestimate of the incoming particle flux. Hence a full angular distribution is needed to achieve accurate measurements of the total EPP energy deposition.

To be able to produce this data a satellite with particle detectors will be launched a low polar orbit (500–800 km) and collect data. Measurements taken during both quiet and geomagnetically disturbed time will give a good indication of the total energy deposited to Earth's upper atmosphere.

Since the DEEP instrument has these specific requirements, the system has to be custom-made to fit the requirements. It might be possible to buy the individual parts, but not the complete system. To be able to produce the equipment needed, the University of Bergen (UIB) are therefore developing their own electronics and data analysis.

1.2 System Overview

Figure 1.2 shows a diagram of the envisioned system. A particle detector is the first component in the system. It emits an analogue signal when hit by energetic particles, which is the input signal to an amplifier. This Charge Sensitive Amplifier (CSA) converts the charge from the detector to a voltage pulse that

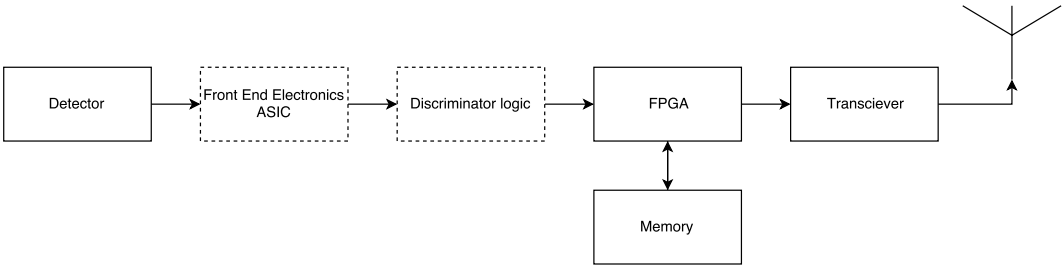

Figure 1.2: Diagram of the DEEP instrument, with the parts covered in this thesis highlighted with a dotted outline

is amplified and transformed, before the signal continues to a shaping filter. The shaping filters create a bandpass filter that removes noise and reduces the pile-up effects, and output a signal that is converted to a digital signal in a specialised circuit, like an Analogue to Digital Converter (ADC). Subsequently the output is sent to an Field Programmable Gate Array (FPGA) with some processing power to analyse and simplify the data, and send the results to a base station on earth.

The detector is already designed and the memory, FPGA and data transformation is a subject of another thesis [1]. The transceiver will be determined at a later time, when it is known which satellite this instrument will be attached to.

In the following chapters the electronics between the detector and the FPGA, as highlighted in Figure 1.2, will be described in detail.

1.3 How the System Works

When energetic particles hits the particle detector, a charge, Q, is generated in the silicon of the detector. This charge is proportional to the energy of the incoming particle. Ideally this pulse can be approximated δ-like pulse, $I_{in}(t) = Q_{in}\delta(t)$, where $\delta(t)$ is the Dirac-function and Q_{in} is the charge delivered by the pulse [15].

The CSA then converts the charge pulse to a voltage pulse. The CSA has a feedback capacitor, C_f, that integrates the incoming charge and produces a pulse $\Delta V = \frac{Q}{C_f}$. The charge pulse is on the order of femto Coulomb, C is pico Farad and ΔV is in the range of mV [10].

The first step in the front-end electronics is the gain stage, where the goal is to have as much amplification possible, without saturating the amplifiers

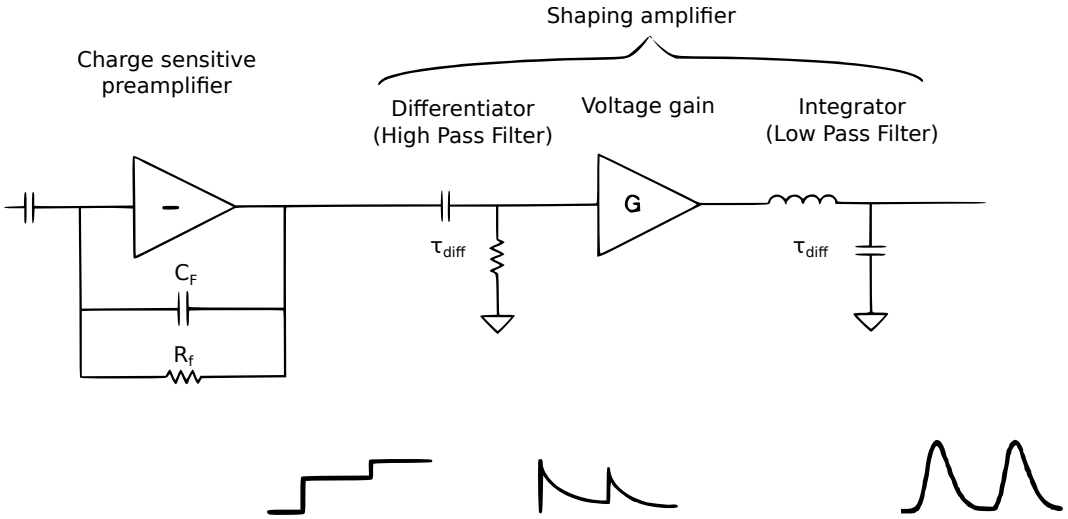

Figure 1.3: Schematic of a CSA and shaping amplifier, showing how the signal could look at different stages [10].

output signal. High gain early in the signal pipeline helps the signal-to-noise ratio.

The CSA also has a feedback resistor, R_f, that causes the input to go back to ground with a time constant $\tau = R_f \times C_f$ Now when the signal rises quickly in response to the input, the resistor discharges the signal causing the signal to have a long tail, see Figure 1.3 for an illustration of the pulse at different points in the signal path.

After the CSA is the shaping amplifier which consists of two main parts. A high-pass-filter and a low-pass-filter. The high-pass-filter is a differentiator of the low frequency signals and is used to bring the signal back to baseline before the next pulse arrives.

The low-pass-filter forms an integrator for the high frequency signals. The goal of the integrator is to give a signal that has slower variations around the peak of the signal coming from the CSA, to flatten the peak. This is to avoid needing a very quick circuit to capture the peak and to be less sensitive to jitter [15]

By adjusting the time constants of both the filters one can set the shape of the output-pulse.

The final pulse has a rise time of $\tau_{integrator}$ and a rise time of $\tau_{differentiator}$ which should be equal, since when $\tau_{differentiator}$ becomes smaller than $\tau_{integrator}$ the amplitude is reduced, since its the slower time constant that sets the return to baseline[15]. The pulse then has a shaping time of τ and a bandwidth of

$\frac{1}{\tau}$. [15]

These pulses are then outputted to a digital conversion-circuit, an ADC, a time over threshold-circuit or a counter, that can discriminate energy levels of the incoming particles [10].

After this the signal is passed to an FPGA for digital signal analysis. The signal analysis consists of coincidence between the two detector layers, binning of data from different energy levels and then packing a data packet. This is stored in memory, and then transferred back to a base station on Earth via satellite link.

1.4 The Goal of This Thesis

The objectives of this Master's thesis is start the work to build up to a complete design of a front end electronics, and further to prove by simulations that the performance of the instrument satisfies the specifications shown in Table 1.1.

Characteristic	Specification
Bandwidth [kHz]	500
Gain [dB]	60
Shaping time	2 µs
Signal-to-noise ratio	3, at 30 keV
Noise Figure [ENC]	1000
Power Consumption [mW]	1.2
Temperature range [° C]	-20 to $+60$

Table 1.1: Requirements for the shaping amplifier circuit [19]

The sub-goals of this thesis are to decide on a transistor technology from a foundry and select the transistors that will be used, and also select the computer software to be used for the design. Subsequently the specifications of the amplifier and shaping filter will be determined. Finally, further a functional design of the CSA and the shaping amplifier must be created and verified with simulations.

The first step is to start with calculating the signal and the noise from the detector, and the required dynamic range of the CSA.

Further calculation is needed to determine the maximum amplification that can be obtained without saturating the CSA, and make sure the minimum signal fulfils the signal-to-noise-ratio specified in table 1.1, and that the CSA can function, and give the required results, when the particle rate (flux) is high.

The next step is to decide on a circuit topology for the different parts of the front-end electronics. A topology for the CSA and the shaping amplifier, how to generate the bias currents needed, for the parts of the system shown in Figure 1.2.

When circuit topologies are selected and the schematics are drawn, the necessary transistor parameters has to be determined, i.e the widths and lengths of all the transistors, and then adjusting these until all the requirements from table 1.1 are met. This has to be proven with simulations and test-benches.

A necessary final step for a functional circuit is the circuit layout of the complete system and simulations to verify that it works as intended, but this part is not covered in this thesis.

1.5 Related Work

The most relevant book that covers similar problems as this thesis is the "CMOS Front-End Electronics for Radiation Sensors by Angelo Rivetti". It addresses all the topics in this thesis, and also uses the circuit schematics that was the starting point of this thesis, with the PreAmplifier ShAper (PASA) from H. Soltveit, as an example. Further the "Radiation Detection and Measurement by Glenn F. Knoll" has been used as a source for physics behind radiation detectors.

"Analysis And Design of Analog Integrated Circuits by Gray, Hurst, Lewis and Meyer" and "CMOS VLSI Design — A Circuits and Systems Perspective by Neil H. E. Weste and David Money Harris" covers more general integrated circuits and electronics design and process technology and design methodology, respectively.

1.5.1 DEEP

The physicists behind the theory of this instrument are Hilde Nesse Tyssøy, Johan Stadsnes, Finn Søraas, Kjetil Ullaland and Dieter Röhrich. All of them associated with the Group 3 at Birkeland Centre for Space Science at the University of Bergen. The technical reports and papers published on this subject has been the reference for theoretical basis and background for this instrument.

1.5.2 Energetic particle precipitation

The proposed particle detectors bear resemblance to the Medium Energy Proton and Electron Detector (MEPED) on board the NOAA POES satellite. The data produced from this project did not have a high enough angle- and energy resolution to resolve the purposes of the DEEP-project.

1.5.3 Front-end electronic implementations

Several implementations of similar designs has been completed. For example there are several variations of this design used at CERN [18][17]. Some of these were designed by Hans Petter Soltveit, and more designs are shown in the textbooks [15].

1.6 Thesis Outline

This thesis is divided into the following chapters:

Chapter 2: Theory

Provides theory to the physics behind the instrument and the technology in the following chapters. The origin and effects of particle precipitation, the origin and effects of radiation on electronics.

Chapter 3: Technology

Covers the technology behind radiation detectors, amplifiers and integrated circuits. Foundry technology, Application Specific Integrated Circuit (ASIC)-design, front end-electronics.

Chapter 4: Low Noise Amplifier Design

Covers the design of a Low Noise Amplifier (LNA) and a Shaping Amplifier. Amplifier topologies. Amplifier characteristics, design trade-offs and CMOS technology selection.

Chapter 5: Development And Testing

This chapter presents the chosen topologies and design choices of the amplifiers and the bias circuit with complete circuit schematics. Simulation results, performance of the CSA, shaping amplifier and bias circuit. The chapter also covers set-up to create a test-bench in Cadence Virtuoso.

In addition comes discussion and conclusion in Chapter 6 and Chapter 7.

Appendix

This section includes a complete set of articles, schematics and details from simulations that were not included in the main thesis.

Appendix A: Wiki Articles

Wiki-articles that were written to document the tools and test-benches.

Appendix B: Circuit Schematics

A comprehensive collection of circuit schematics.

Appendix C: CMOS Technology Selection

Tables containing information about the different CMOS technologies that were considered for this thesis.

CHAPTER 2

Theory

This chapter provides a theoretical background to energetic particles, the flux of these and their pitch angles, and also the chemical effects of these particles on the atmosphere.

2.1 Particle Precipitation

As previously discussed in Section 1.1 the goal is to measure energetic particles hitting Earth's atmosphere. Another more common colloquial term for these particles are radiation.

The relevant particles hitting the Earth's middle atmosphere (50–90 km) are electrons and protons in the range of 30 kilo electron Volt (keV) up to 1500 keV and protons from 150 up to 9600 keV [19]

The particles of interest are relativistic electrons ($\approx 100 - 500$ keV) and high energy protons (> 1 MeV) that result from Solar Proton Events. Low energy protons behave as electrons in the detector, therefore it is mandatory to measure both electrons and protons.

The goal is therefore to measure both low and high energy protons in the range from 150 up to 1200 keV, to be able to correct for these effects in the electron data, and provide data suitable for quantitative analysis [19].

The distribution of energy levels in particles is skewed towards more of the lower energies and not many particles that have energies above 1000 keV. There are typically order of magnitude between electron fluxes of 30 keV, 300 keV and 1 MeV.

The electrons with less than 1000 keV will not hit the proton detector,

because of the magnets around the pin-hole of the detector. The magnets create a magnetic field covering the pin hole that bend their trajectory. There will be some loss in high energy particles that will not be measured, due to they cannot deposit all of their energy in the silicon detectors. Most electrons that have an energy above $approx$2000 keV will not deposit all their energy, and will appear as a particle with another energy level [1]. The amount of these high energy particles that cannot be measured represents a small percentage of the total, and it has been decided that this a tolerable loss.

2.2 Heliophysics

The origin of the charged particles hitting the Earth's atmosphere is the Sun and more specifically solar winds and coronal mass ejecting, colloquially called solar flares. Coronal holes are colder parts of the Sun's corona, and from these holes, the Sun's magnetic field are projected out, as shown in Figure 2.2. Here the Sun ejects charged particles that travel with twice the speed of the normal solar winds, and i.e. twice the energy.

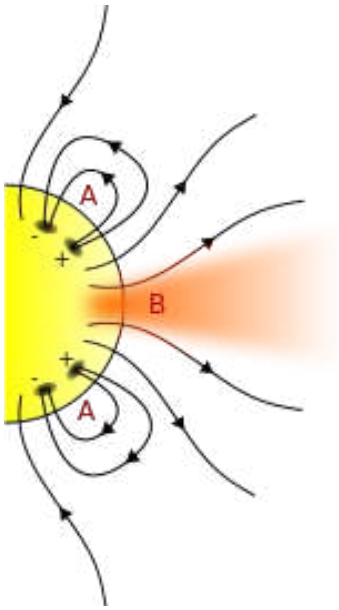

Figure 2.1: Closed magnetic field lines (A) and a coronal hole (B) [2]

The amount of particles ejected varies and the solar activity coincides with a 11-year cycle with a 27-day cycle, associated with the solar rotation, on top of the lng cycle.

The solar wind travels to Earth and the interacts with the Earth's magnetic field lines. Electrons and proton interacts with the molecules and atoms of the atmosphere and creates NO_x which is a catalyst for breaking down Ozone (O_3) in upper atmosphere, see Figure 2.3 for an extended chemical reaction. This impacts temperature gradients and subsequent the pressure gradients in the atmosphere winds change.

2.3 Pitch Angles

The speed and angular distribution of the particles relative to the magnetic field is determining the amount of energy deposited in the atmosphere. These particles travel along Earth's magnetic field lines and as they interact with the field they oscillate. The angle between the particle speed and the magnetic field, the pitch angle, is one of the main parameters this project want to measure. Figure 2.3 illustrate this.

The pitch angle distribution of the particles have been estimated from measurements earlier [13], but there are large uncertainties associated with these estimates. The goal now is to measure the pitch angles from 0 to 180 degrees with a 15 degree resolution. This will to give useful data for the physicists to estimate the dissipated energy to the atmosphere.

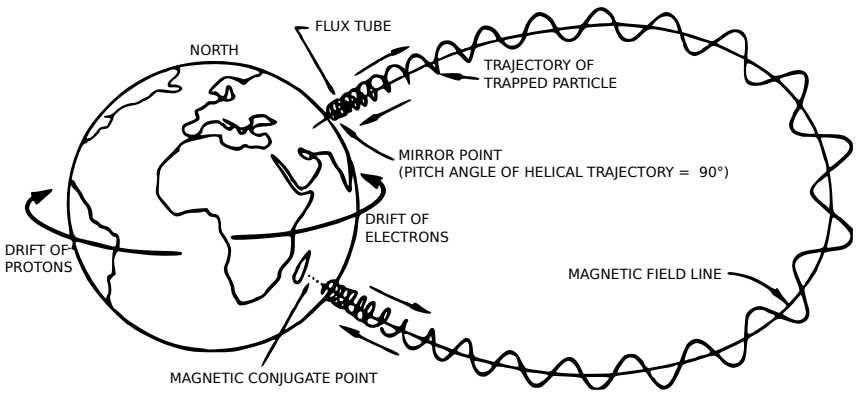

Figure 2.2: The Earth with its magnetic field lines and the motion of the trapped particles. A particle's pitch angle between the velocity vector and the magnetic field line [8].

2.4 Chemical Effects of Electron Precipitation

The resulting ionisation of the particles interacting with atoms in the atmosphere, is of interest as they can change the chemical composition of the Earth's atmosphere. [19]. See Figure 2.3 for an overview of the chemical cascade that can happen and how it affects the amount of ozone in the atmosphere.

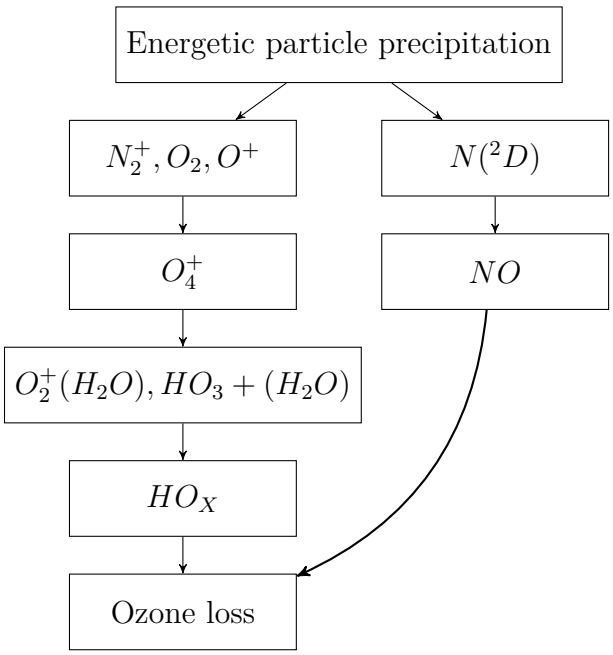

Figure 2.3: A figure showing the chemical effects of EPPon the atmosphere. Adapted from [12]

2.5 Particle Flux

The rate of energetic particles, the flux, hitting the atmosphere and the detector varies greatly with the solar cycle and the latitude and longitude of the satellite. In a particular area in the ocean outside of Brazil, the South Atlantic Anomaly, the flux is particularly high, due to Earth's magnetic field strength is not uniform in its shape or distance from the surface. Here the magnetic field is low over the ocean causing the ionosphere to dip deeper than usual, as shown in Figure 2.5 [11].

This area is of interest as the DEEP instrument will have to pass this and the higher flux will need to be taken into account. Normally rate of $2 \times 10^5 cm^{-3} s^{-1} sr^{-1}$ electron flux above 30 keV is expected to be the average,

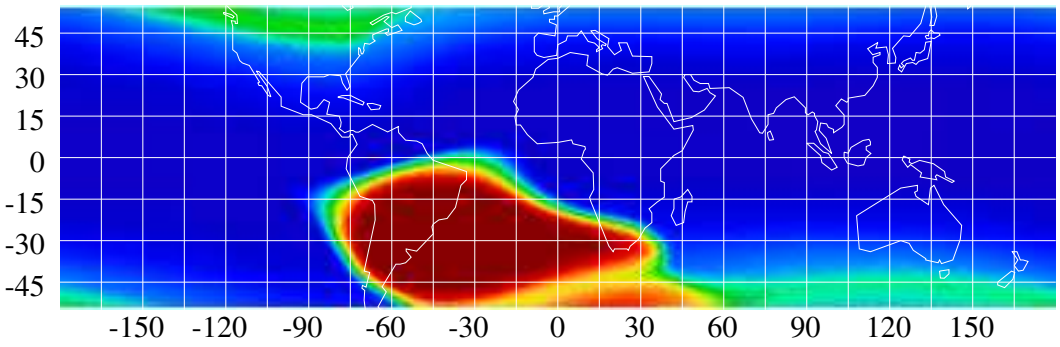

Figure 2.4: The red area is the anomaly at an altitude of approximately 560 kilometres [11]

with a peak in flux about 1×10^6 for Coronal Mass Ejection-events.

CHAPTER 3

Technology

This chapter will give an overview of the technology used, explain design choices and trade-off in the design and explain the process of producing integrated circuits

3.1 Radiation Detectors

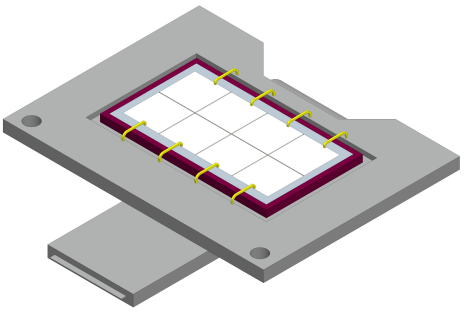

Figure 3.1: The arrangement of the pixels of the electron detector used on this instrument [6]

Radiation can be detected and measured in several ways. The detector chosen for this instrument is a silicon PIN diode-detector which is a diode with a wide, un-doped intrinsic semiconductor region between a p- and an n-type region. This detector was designed by SINTEF in collaboration with UiB. A model of the complete detector (without the house) is shown in Figure 3.1.The particle detector consist of two layers of solid state detector-pixels arranged

in a grid as shown in Figure 3.1. There are two different detectors, one for electrons and one for protons and the electron-pixels. The electron-detector is composed of two layers of pixels with 2×4 pixels. The top pixels are $4.4 \times 4.4 \times 1$ mm and the bottom pixels are $5 \times 5 \times 1$ mm. The proton detector is also composed of two layers, but with a pixel-grid of 2×2 pixels. The top pixels are $4.4 \times 4.4 \times 0.3$ mm and the bottom pixels are $5 \times 5 \times 1$ mm. The distance between the two pixel-layers are 0.1mm [1].

3.1.1 Silicon PIN-detector Operation

When charged particles hit the PIN-detector and ionise the silicon, electron-hole-pairs are created. Electrons travel to the cathode and holes to the anode and a charge is transferred to an amplifier.

The amount of energy deposited, and the number of electron-hole pairs that are generated, in the PIN-detector is dependent on the thickness of the detector, the energy of the incoming particle and the depletion region of the PIN-detector-diode.

The mode of operation for the PIN detectors are pulse mode, and this mode preserves information about the amplitude and the timing of individual event.The output of the detector depends on the size of the time-constant, or RC constant, of the pre-amplifier. A small RC, compared to the charge collection time, gives a signal voltage almost equivalent to the input current pulse from the detector. This is commonly used when one expects high event rates. For this case the maximum output from the detector is $V(t) = R(i(t))$ What is more commonly used is a large RC, compared to the charge collection time, which gives a signal shape with a long trailing tail. Pulse mode has several advantages over the other detector modes. Firstly it has a significantly higher sensitivity than the other modes, since each individual quantum of radiation can be detected and the second advantage is that each hit on the detector has an amplitude that gives information about the particle that hits [10].

3.2 Energy Resolution

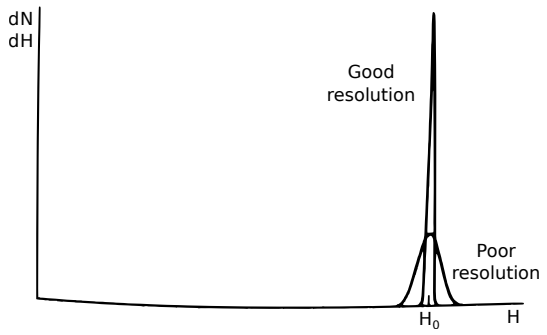

Figure 3.2: Good vs bad energy resolution in a detector. Assume the same number of pulses and the area under each peak is the same [10]

Figure 3.2 illustrates the difference between good and bad energy resolution. Ideally the peak would have no width, but with a poor resolution it is smeared out. With a low and wide peak, it is difficult to differentiate the different energy levels.

3.3 Radiation Tolerant Electronics

Charged particles hitting electronics other than the detector causes problems by inducing charges and shifting voltage levels. This can corrupt signals and over time destroy the whole circuit.

Other problems arise of accumulated dose in the silicon of the transistor and high energetic particles can cause latch-up due to the inherent parasitic transistor, as shown in Figure 3.3.

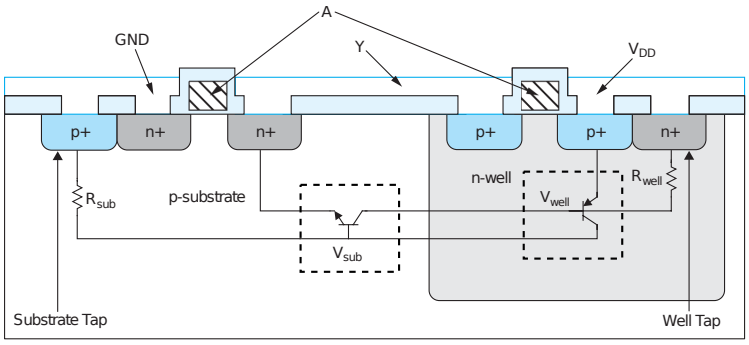

Figure 3.3: Figure showing parasitic transistor, highlighted in dotted boxes, the cause of latchups [20]

The effects of radiation on analogue electronics have to be taken into account in both the design of the circuit diagram and the layout, and the concrete steps taken to minimize these effects are described in the following section.

3.3.1 Mitigating Effects of Radiation in Integrated Circuits

To completely mitigate these effects is impractical because of the amount of extra electronics and shielding that would be required. The solution is therefore to limit the effects to a tolerable level. To do this, several well-established techniques can be used, but the most common are guard rings that protect high impedance nodes from leakage currents and watchdog-circuits that monitor the currents in the circuit and disable parts if the amount of current is increasing out of specifications. Then the circuit reset the system and charge dissipates, keeping the circuit safe.

3.4 Designing for Space Application

Since this system is meant to operate in low-Earth-orbit, there are other effects than radiation that has to be taken into account. Because of the vacuum in space, it is difficult to remove heat since there is no air cooling, therefore low power electronics necessary. This is reflected in the power requirement of the instrument.

Also since there is no way to repair the system after launch, it must be robust and survive the mission duration. The only way to know if the instrument is robust, is to test and design for the required specifications.

3.5 Satellites

Exactly which satellite this instrument will be attached to is not known, neither is the rocket that will launch the system, so the goal is to have the instrument ready and look for possible candidates to attach the instrument as a secondary payload.

The plan is to have a satellite orbiting the Earth in a path that crosses Norway and Brazil, and the South Atlantic Anomaly.

This satellite orbit in an altitude of about 600 km, and this will cause the particles in the atmosphere to destroy the satellite more quickly compared to higher altitudes, because of the increased amounts of radiation.

3.6 Communication

As it is not known which satellite DEEP will be attached to, the exact available bandwidth that will be available is unknown. As the scope of this thesis is only the analogue part of the DEEP instrument, this part is not a focus, but is further discussed in Hogne Andersens master thesis [1].

3.7 DEEP Particle Detector Configuration

DEEP will have multiple detector houses where each detector house have two layers of detectors.

In the detector house, electrons and protons will be measured in separate detectors, where the different detectors have a different configuration of silicon

detector-pixels. See Figure 3.1 for an illustration of a single detector, without house. The goal is to be able to measure the pitch angle in 15 degree intervals over 180 degrees measuring range. To measure so wide a range of angles, each detector house is angled, as shown in Figure 3.6.

The measurements in this instrument will have excellent energy resolution as well as pitch angle resolution. By taking measurements for full orbits of the Earth one can measure the total energy input to the Earth's upper atmosphere [19].

3.7.1 The Detector House

The final design of the detector house has not been determined, but a preliminary CAD-model has been designed. See Figure 3.5 and Figure 3.4 for the CAD model for the individual detector houses.

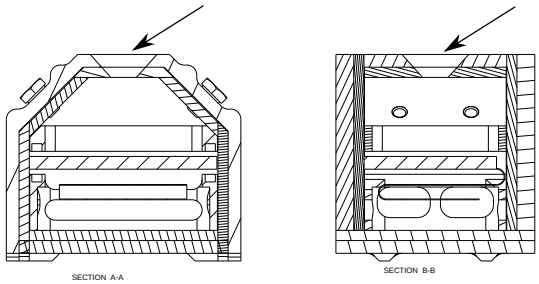

Figure 3.4: The cross section of the detector house. The detector opening (pinhole) is at the top of the housing (arrows), and the hatched area is the detector [6]

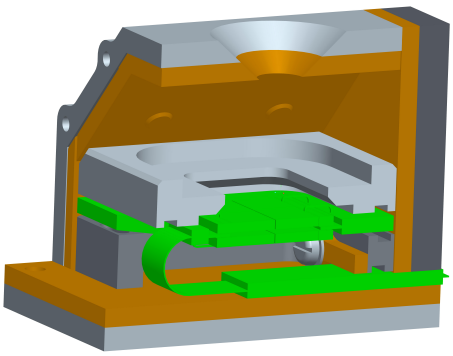

Figure 3.5: A cross-section of the electron detector-house. The gray part at the top is aluminium for shielding, the orange is wolfram, also for shielding. The green part is the detector and readout electronics. The light gray part inside is baffles to shield the detector from particles with a large incoming angle. The other parts are mechanical parts to make the detector house mechanically usable and manufacturable [6]

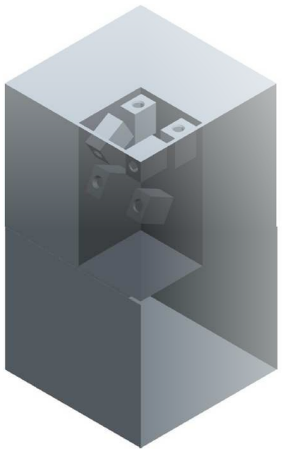

Figure 3.6: This shows it is imagined that the detector houses will be rotated in the instrument. One can see the houses aligned in different directions to get a wide range of the incoming particles [19]

3.7.2 Charge Estimation

Electron [eV]	Charge [fC]
30 E3	1.34
60 E3	2.67
120 E3	5.34
240 E3	10.68
480 E3	21.36
960 E3	42.72
1.5 E6	66.76

Proton [eV]	Charge [fC]
150 E3	6.68
300 E3	13.35
600 E3	26.70
1.2 E6	53.41
2.4 E6	106.81
4.8 E6	213.62
9.6 E6	427.25

Table 3.1: Energies of incoming particles and their corresponding generated charge. The calculation is done by multiplying the energy with elementary charge,e and converting to Coulomb

The particle with the least energy are electron and proton of 30 keV and the most energetic electrons are 1500 keV. To ionise an electron-hole-pair in silicon 3.6 electron volt per $e^{-}h^{+}$ [10]. This ionisation energy is one of the advantages of using a semiconductor detector, as gas-filled detectors have a factor 10 higher ionisation energy and therefore a factor 10 lower charge carriers/electron/holes for the same amount of incoming energy [10].

To calculate the charge out of the detector the following equation is used:

$$\frac{e}{\epsilon_i \times Q}$$

For electrons and with e = 30 kev, $\epsilon_i = 3.66$ eV and Q = 1.6×10^{19} this results in a charge of 1.34 fC for the least energetic electron and for the most energetic electron $e = 66.7$ fC, as shown in Table 3.1.

To get this signal up to a level where it can be used in a digital circuit it needs to be amplified. A normal amplification for an integrated circuit like this is in the range of $\frac{10mv}{\text{fC}}$ so the particles with the least energy would create a signal of 13 mV. These low energy signals are the most critical, as they might be lost in the noise floor of the electronic circuit.

3.8 Detector Capacitance

Knowing the detector capacitance is critical for the operation of the amplifier. Matching the capacitance of the input transistor to the capacitance of the detector is necessary to reduce noise [15], and therefore we need to calculate the detector capacitance.

The detector is a silicon P-Intrinsic-N (PIN) diode, and to set up a large enough electric field, required to transport holes and electrons fast enough to avoid recombination, the detector will be reverse biased with 100V to set up the conditions to capture a good signal [10, page, 382]. Depending on the voltage of this bias, the size of the depletion region varies, and with it, the detector capacitance.

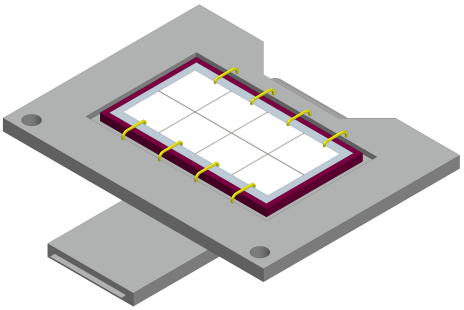

Figure 3.7: A 3D-model showing the radiation detector and the layout of the individual detector pixels

A first estimate of the output capacitance of the detector is done by using the formula for an idealised parallel plate capacitor.

$$\text{Ideal plate capacitor} = \frac{\epsilon_0 \times k \times detector\ area}{detector\ thickness} = 5.2\ pF$$

where ϵ_0 is the permittivity of vacuum, ϵ is the permittivity of silicon, A is the detector area in m^2 and d is the detector thickness in meters.

$$C_{tot} = C_d + C_{pair} \times pairs + C_{cable} \times length$$

Where C_{tot} is the total capacitance of the detector, C_d is the capacitance inherent in the detector, C_{pair} is the capacitance of each input pair, $pairs$ is the number of input pairs, C_{cable} is the capacitance of a centimetre with cable from the detector to the amplifier and $length$ is the length of the cable in

centimetres.

$$\text{Total detector capacitance} = C_{tot} = 7.7pF$$

The generated pulses can be modelled as a current pulse in with a width of 50 ns. This current can be converted to coulomb to get the number of electrons.The expected average number of incoming particles are 100,000/s, so the input pulse has a periodicity of 10 µ seconds, not taking micro bursts or the fact that the statistic distribution of particles is a Poisson-distribution and the amount of time between each particle is not even.

The input pulse appears in the results as a negative square pulse and since the CSA is an inverting amplifier the output will be a positive square pulse with a rise time determined by the slew rate and the fall time determined by the time constant

3.9 ASIC Design

An Application Specific Integrated Circuit (ASIC) is a custom circuit for created for a specific purposes. This can be a circuit tailored for a specific need, as in this instrument, or a circuit that performs a task, meant for the commercial market.

To create ASICs one need transistor technology from a fabricator of ASICs, a foundry, and software to design the circuit in. See Appendix C for a comparison of the available technologies. The advantages of making custom ASICs are foremost that they can be tailored to ones specific requirements, with the possibility of reduced power, many channels, constrained power budget, strict physical space-requirements, increased speed and accuracy compared to Commercial Of The Shelf (COTS) components that are often a middle ground. It is expensive, to produce an ASIC, but still cheaper than buying COTS ASICs.

The drawbacks of custom ASIC is that it is difficult to design, and that it takes many hours to design, test and verify an integrated circuit. The software is required to design is expensive, the foundry technology is expensive, and it is expensive to produce the physical integrated circuit.

It is in the nature of an ASIC to be custom and non-standard, but there are a number of ASICs available from commercial vendors that have been designed for radiation detection purposes. A Norwegian company, IDEAS have several appropriate ASICs, and the literature, has more examples and names a couple

of chips: Medipix, RENA-3.

One way to reduce the cost of an ASIC, which is mostly production costs, is to share a silicon wafer in a Multi Project Wafer (MPW), with other projects. Producing integrated circuits this way is cheaper when several projects can share the cost of masks, which is the main cost when producing integrated circuits.

3.9.1 Taiwan Semiconductor

Taiwan Semiconductor (TSMC) is one of the foundries that the University of Bergen has access to via the Europractice collaboration, an organisation working to provide easier access to integrated mixed circuit-tools and training to companies and universities. TSMC provides a 130 nanometre CMOS mixed process, meaning it is usable for both analogue and digital designs. The 130 nm process is not on the cutting edge of the field, but a tried process, that is widely used, cost-effective and a stable technology.

Since this is an analogue design, transistor size and speed is not the most critical characteristics of the technology of choice, but low power, low noise and possibly the ability to be able to put digital circuits on the same integrated circuit, Analogue to Digital Converters in particular.

3.9.2 Process Requirements

The requirements that were taken into consideration when selecting the process was that the process was available through Europractice, that there was a MPW run available for this technology, that it was a CMOS process and, not BiCMOS or SiGe. It was also required that the technology supported analogue processes.

It was also taken into consideration to find a stable technology, i.e not something new and experimental.

It is also a point to not use the smallest available transistors for analogue processes, as speed is not a requirement and as the transistor sizes decrease the amount of leakage current increases, as the oxide layer of the gate is getting thinner and thinner.

3.10 Digital Conversion

For the conversion from analogue to digital signal there are multiple alternatives. A common solution is to use an Analogue to Digital Converter (ADC), either as a separate chip, external to the ASIC, as an ADC IP-on-integrated circuit, or as a completely custom solution.

For some technologies one can buy finished blocks that are placed on the layout of this ASIC. By implementing the ADC with an IP-on-integrated circuit-solution, one can manufacture a single chip with all components on a single wafer, saving area, cable length and possibly effect.

The downside by using an ADC compared to, for example, a time-over-threshold solution, which is in practice a single-bit ADC, is that the ADC has a higher power consumption. Since a low power consumption is an important requirement this might be a favourable solution for this instrument.

Figure 3.10 illustrates the signal shape through the front-end electronics and the process of shaping the signal, and preparing it for digitising.

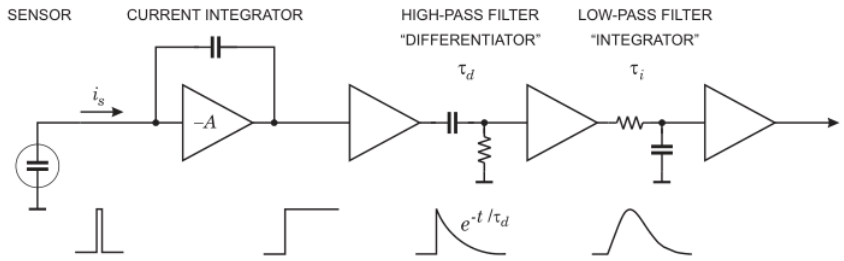

Figure 3.8: The shape of the signal from the detector through the amplifier and the shaping amplifier.

CHAPTER 4

Low Noise Amplifier Design

This chapter will give an overview of amplifier topologies and the different parameters important in their design, as well as a discussion about CMOS technologies.

4.1 Charge Sensitive Amplifier Overview

When a charged particle hits the radiation detector, a short pulse is generated, which has an amplitude that is dependent on the energy of the incoming particle. This creates a negative pulse on the input of the amplifier which in turn translates to a positive signal on the output of the amplifier, due to the inverting nature of the amplifier. The current through the feedback charges the feedback-capacitor (C_f) which discharges slowly with a rate of $\frac{1}{R_f \times C_f}$

The CSA is the first stage after the detector and must be able to use small signals, in the order of femto Coulomb. Because of these small signals, it is critical to have a low noise figure, and a good Signal-to-Noise ratio. This chapter will go into detail of designing an amplifier that fulfils these requirements.

The signal from the detector and the amplifier is a pulse/step, and this needs to be converted into a pulse that can be digitised by an ADC. This is done with a CR-RC-shaping amplifier, which forms a band-pass-filter, as shown in Figure 3.10. The shaper also filters out noise from the signal. The final shape of the output pulse is determined by the order, and time constants of the shaping amplifiers.

4.2 Amplifier Topologies

There are several commonly used amplifier topologies used for designing a CSA. A comparison of the amplifier characteristics of some commons topologies are shown in Table 4.1. For this project a folded cascode-topology was chosen, shown in Figure 4.2. The reason for this choice is that the folded cascode is a well-known design that is easy to stabilise and has a good output swing.

Characteristic	Common–Source	Common–Gate	Cascode
Noise Figure	Lowest	Rises rapidly with frequency	Slightly higher than CS
Gain	Moderate	Lowest	Highest
Linearity	Moderate	High	Potentially Highest
Bandwidth	Narrow	Fairly broad	Broad
Stability	Often requires compensation	Higher	Higher
Reverse Isolation	Low	High	High
Sensitivity to Process Variation, Temperature, Power Supply, Component Tolerance	Greater	Lesser	Lesser

Figure 4.1: A comparison based on the most relevant considerations for Low Noise Amplifier design [3]

A major choice that needs to be taken is the topology of the amplifier and for this project the alternatives considered were folded vs telescopic cascode amplifier and the loading of this amplifier, single vs double cascode load. With a double cascode load, the output resistance, R_o, and gain is increased.

Another trade-off is the size of the input transistor. A wider transistor gives the amplifier increased gain, up to a certain point, but also increased noise. The same consideration goes for the bandwidth, increased bandwidth increases the noise.

The time constant, τ, of the feedback on the amplifier needs to be determined to a point that gives the desired signal.

The amplifier needs to tolerate pile-up effects from particle hits and be able to counteract undershoots of the generated signal, and avoid baseline drifts.

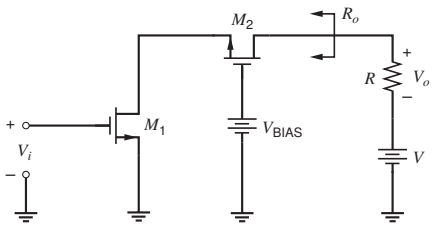

Figure 4.2: Common source cascode amplifier [7]

4.3 Noise

Noise in this setting refers to disturbance in the signal, generated in the electronics. This noise is intrinsic to the components and cannot be eliminated by shielding the circuitry. The noise has its roots in the movement of the charged particles that move around in the electronic devices. There are a finite number of these particles, and they move at a finite speed, and this leads to a degradation of the signal. This effect is illustrated in Figure 4.3.

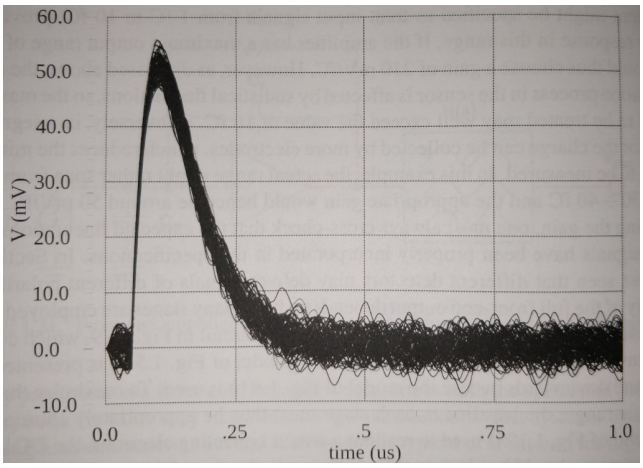

Figure 4.3: Noise effects on the output of the amplifier. An ideal signal would have no variation [15]

Incoming particles with a low energy generates an equivalent a low signal, but the amount of noise stays constant. This makes the noise figure for low energy particles is critical.

For a CSA it is common to refer to the noise as Equivalent Noise Charge, noise referred to the number of input electrons. This provides an easy comparison of the noise floor and the incoming signal. For example for a system with a gain of 12 mV/fC, and has a Root Mean Square (RMS)-noise output of 2 mV, the ENC can be obtained by dividing the noise by the gain as shown here:

$$\frac{2mV}{10mV/fC} = 0.2fC = 1248ENC$$

4.3.1 Maximum Noise

To find the number of incoming electrons one can take the input signal (i.e 30 keV) and divide 30×10^3 by 3.6 [16] to get the number of incoming electrons

(8333). To calculate the output electrons one has to calculate backwards from the output voltage.

With a SNR of 3 and a minimum of 8333 electron-hole-pairs generated the maximum allowed noise is 2778 electrons per shaped pulse.

4.3.2 Noise Sources in a CMOS Transistor

Noise is generated by the transistors forming the amplifier circuit, by leakage currents in the detector and by the bias network. These noise sources can be modelled as current or voltage sources, depending on where in the circuit they appear in relation to the circuit input.

Due to thermal agitation the speed and movement of the charge carriers varies and this appears as noise. This noise is dependent on temperature and has a random spectrum, i.e. white noise. This noise appears even with no signal or power connected, because the energy of the noise is related to the temperature. The most common non-random noise is flicker noise or 1/f noise where the major contributor is the input transistor. There are also noise from the detector and bias network, and leakage currents related to the reverse bias on the detector.

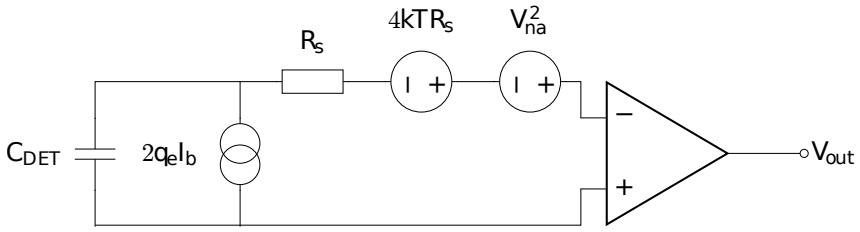

Figure 4.4: A simple noise model for a Charge Sensitive Amplifier (CSA), see for example Knoll [10]

$$ENC^2 = (\frac{e^2}{8})[2q_eI_b\tau + (4kTR_s + v_{na}^2)\frac{C_D^2}{\tau} + 4A_fC_D^2]$$

4.3.3 Minimum Noise in the Charge Sensitive Amplifier

The different noise sources contribute differently to the total when the shaping time is varied, as shown in Figure 4.5. With a low shaping time the parallel noise dominates, while on higher shaping time the series noise starts to dominate. To minimise the noise one has to find this noise corner and use a shaping time as close to this as is usable.

To minimise the thermal noise the gate capacitance of the input transistor needs to be 1/3 of the detector capacitance [15].

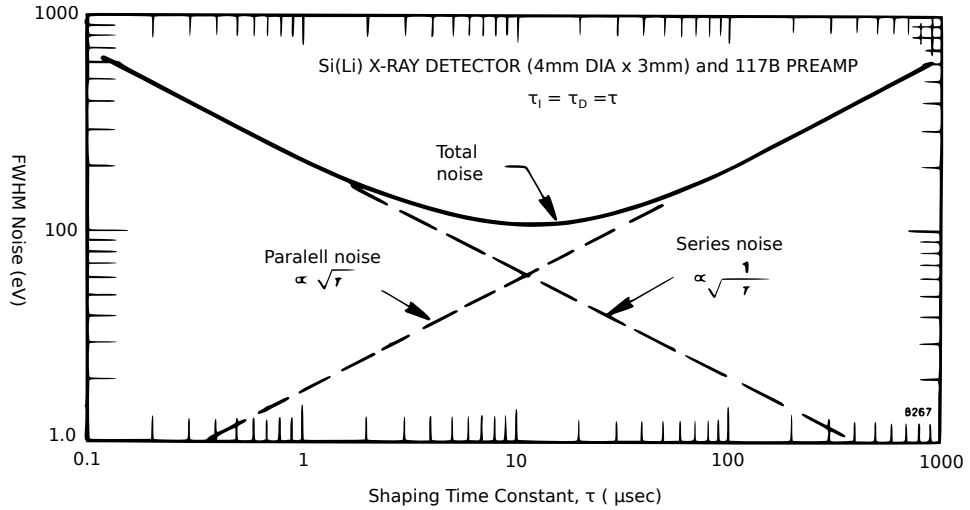

Figure 4.5: Noise versus shaping time showing the noise corner, where series noise is equal to parallel noise. The shaping time at this point is the ideal [14]

4.4 Pile-up Effects

A consideration when selecting the peaking time is pile-up effects. The amplifier must return to baseline before the next pulse arrives, otherwise the two signals will pile up. The arrival of particles usually follows a Poisson-distribution, so one can calculate the probability for a pile-up to happen, for a given flux and shaping time. See Table 4.1.

t (µ s)	$r = 1 \times 10^5$(counts/s)	$r = 2 \times 10^5$(counts/s)	$r = 5 \times 10^5$(counts /s)	$r = 1 \times 10^6$(counts/s)
0.5	0.05	0.10	0.22	0.39
1	0.10	0.18	0.39	0.63
2	0.18	0.33	0.63	0.87
3	0.26	0.45	0.78	0.95
4	0.33	0.55	0.87	0.98
5	0.39	0.63	0.92	0.99

Table 4.1: Pile up probability associated with selected shaping time and count rates [19]

4.5 Stability

4.5.1 Baseline Drift

The feedback resistor of the amplifier is finite and needs to be implemented as an active device due to a passive would take too much silicon area. This leads to a feedback impedance of a parallel by $R_{feedback}$ and $1/sC_f$:

$$Z_f = \frac{R_f}{1 + sC_f R_f}$$

This creates a pole and this pole of the CSA and that of the differentiator do not cancel each other, resulting in an impulse response of the CSA as shown in figure 4.6.

The impact of this undershoot is that it affects the baseline of the signal, causing it to drift. After some time the baseline drifts back to 0, but if another signal pulse arrives in the interval with the undershoot, no energy, or a wrong energy level might be reported. This effect is more pronounced for high energy signals, due to their increase in signal swing. This effect can be mitigated by Pole-Zero Cancellation.

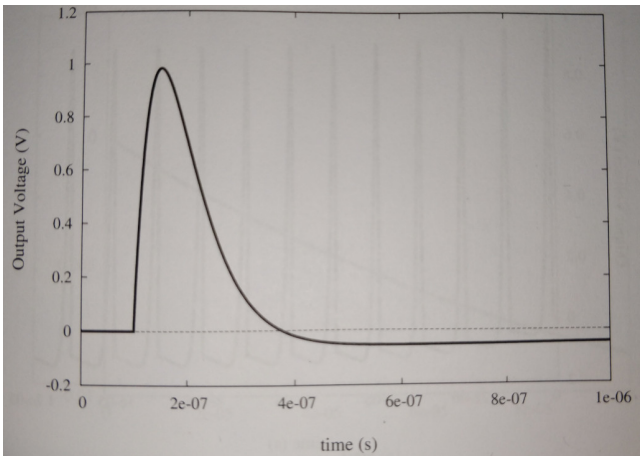

Figure 4.6: CR-RC impulse response with finite CSA feedback resistance. The dotted line is the baseline, and one can see the signal dipping below it [15]

4.5.2 Pole-Zero Cancellation

A common way to fix the baseline drift is to shifting a zero to match the pole of the CSA, by adding a resistor in parallel to C_Z

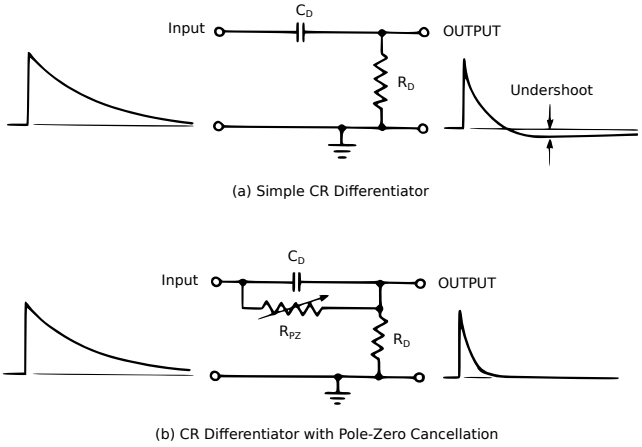

Figure 4.7: The effects of Pole-Zero Cancellation on the output signal [14]

4.6 Differential Input Considerations

Fully differential uses more power and area on the silicon, but suppress external noise better than the single input-amplifier. The singled ended on the other hand has less internal noise. The ratio of power between them are $2 \times \sqrt{2}$ [15].

Most ADC in the range that could be used in this project have differential inputs so a differential output of the ASIC is needed. The input is single-ended

so circuits has to be designed to do this conversion.

4.7 The Input Transistor

For the consideration NMOS vs PMOS on the input transistor, PMOS provides a better 1/f than the NMOS, but the NMOS has a better transconductance for the same power budget [15]. The size of the input transistor should be scaled such that it is responsible of 50% of the total noise in the amplifier. This way makes it so that the transistor is not larger than it needs to be and not to large that it dominates the noise.

4.8 Amplifier Characteristics

A characteristic that can cause distortion of the signal is slew-rate limitations. Slew rate is the maximum change of the signal and is ideally infinite.For this application the requirement for the slew rate needs to be high enough to avoid distortion of the signal.

The slew rate is related to the time constant, $\tau = \frac{1}{R_f \times C_f}$, of the CSA, and charging and discharging of the feedback capacitor. This capacitor also needs to discharge quickly enough to avoid pile-up effects.

Power Supply Rejection Rate

Disturbance on the amplifier power supply rails introduces additional noise that often over shades the one contributed by the transistors and resistors in the circuit [15]. Because of this it is important to isolate the amplifier circuitry from the power rails. This can done with a bias network that supplies currents to sub-circuits, where all currents are more of less independent from V_{DD} and V_{SS}.

4.9 Power Distribution Network

Every transistor that is externally biased gets its bias from the VT Bias Reference-cell. The current references from the bias network needs to be distributed around the whole design, with a minimum amount of noise, while being easy to lay out and should consume little chip area.

The on-chip power distribution network consist of power and ground wires within the layout cells and more wires connecting cells together.

The transistors in the amplifier- and the shaping amplifier-cells each require several bias currents which needs to be supplied from this cell. As there will be 72 channels in the final design, each having an amplifier, two shaping amplifiers and circuitry to get a differential output, it is obvious this could be a substantial amount of interconnects.

The distribution of power across a design is non-trivial, as there are several pitfalls and different strategies to accomplish this in the best possible way. A compromise has to be reached between the amount and length of wires supplying currents directly from the bias circuit, and if one should have a tree structure that spreads voltages around.

By having a tree structure one reduces the amount of wires and the length of wires at a cost of complexity, and more circuits to scale and distribute the currents locally [20].

Decoupling capacitors are necessary to compensate for the voltage drops due to sudden current draw from a circuit. These are capacitors spread around the power network to provide local reserves

4.10 Shaping Time

The optimal shaping time is dependent on the rate of particles and the size of the pinhole in the detector house, see Figure 3.4 for an illustration of the detector house with the pinhole. By adjusting the size of the pinhole the rate of particles can be increased or decreased and this can be set to fit the electronic circuits. A too high flux will cause the CSA to saturate.

The final dimension of the pinhole has yet to be determined, but an ideal shaping time for this project has been determined to be $\approx$ 1µ second, based on a geometric factor of $\approx 1.8 \times 10^{-2} cm^2 ster$. By adjusting the pinhole and thereby the geometric factor, the shaping time can be adjusted, independently of the electronics. [19] With a shaping time of 1 µ second there is less than 20% chance of pile up effects will occur during high flux.

4.11 Differential Considerations

The instrument was designed with a single-ended input and a single-ended output in mind. A differential output could be needed since most ADCs require differential input, but if a Time Over Threshold-comparator is used for digitising the signal, a differential output is not necessary.

4.12 CMOS Technology Selection

Through the Europractice-collaboration CMOS technologies from multiple companies are available, notably AMS, IHP, TSMC and ON Semiconductor. These companies have more than 50 different IC technologies available, ranging from transistor sizes from 800 nanometre to 28 nanometre and a wide variety of specialised technologies. See Appendix C for a table comparing some available technologies.

Not all the technologies available are optimised for analogue circuits and some did not have MPW runs, making them unsuitable for our purpose.

TSMC13RF from Taiwan Semiconductor (TSMC) was chosen as it fulfilled the requirements stated in Section 3.9.2, and as this technology was already available both in via the Europractice collaboration-technology packs and already installed on UiB computers.

Name	TSMC 013 um tech
Technology	Logic
Geometry	0.13um
Device Application	General Purpose
Core Voltage (V)	1.2
I/O Voltage (V)	2.5
Poly Layers	1
Metal Layers (Min)	3
Metal Layers (Max)	8
RO Speed (ps/gate)	19
Gate Dielectric tox (core)	20A
Gate Dielectric tox (I/O)	50A
Default number of masks	36
Number optional masks	8
Gate density	219 Kgate/mm2

Table 4.2: Main parameters for the TSMC 13RF-technology [5]

There are several transistors available in the technology. There are a total of 60 types of NMOS and 60 types og PMOS-transistors in the TSMC 13 RF-technology with varying combinations of technologies. High/Low/Standard Threshold Voltage, Design For Manufacturability, NanoWire and Metal on Insulator on Semiconductor and combinations of these.

The selected transistor was the standard NMOS1V and the PMOS1V-transistors. There IV-characteristic is shown in Figure 4.12.

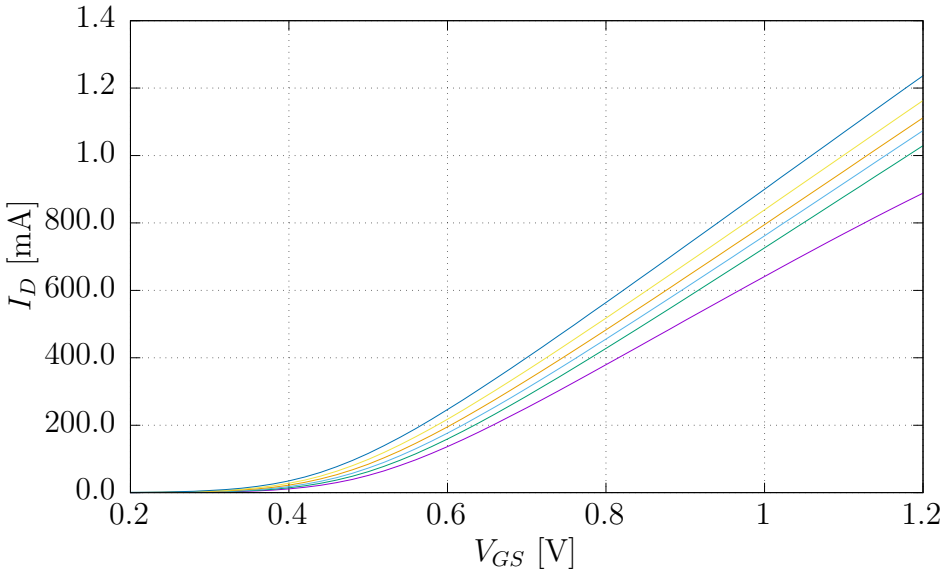

Figure 4.8: Transistor characteristic of the TSMC NMOS 1V, with a minimum geometry, showing V_{GS} vs I_{DS} for different V_{DS}

The transistors in the TSMC13RF-technology have a minimum channel length of 130nm, but to reduce the impact of production variations in the channel length, all lengths are 300nm if not otherwise stated.

CHAPTER 5

Development And Testing

This chapter will explain design choices for the CSA, the shaping amplifier and the bias current-supply circuit, as well as the set-up of test-bench in Cadence Virtuoso and simulation results.

5.1 Schematic System Overview

Figure 5.1 shows an overview of the three first blocks in the system. The different sensors are modelled the same way, detailed in Section 5.5

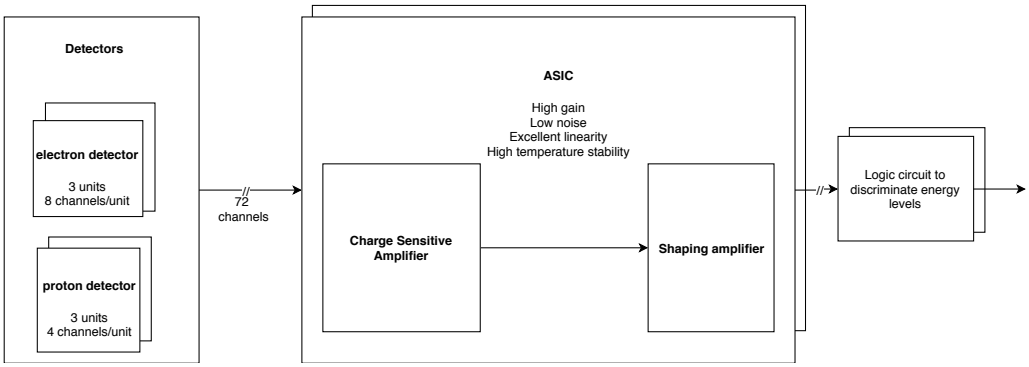

Figure 5.1: Block diagram of the DEEP instrument.

5.2 Charge Sensitive Amplifier

Of the amplifier topologies discussed in the previous chapter, a folded cascode amplifier was chosen, followed by a source-follower on the output. This topology was chosen since it is easy to stabilise, has a high gain, and is less sensitive to process variations than other topologies.

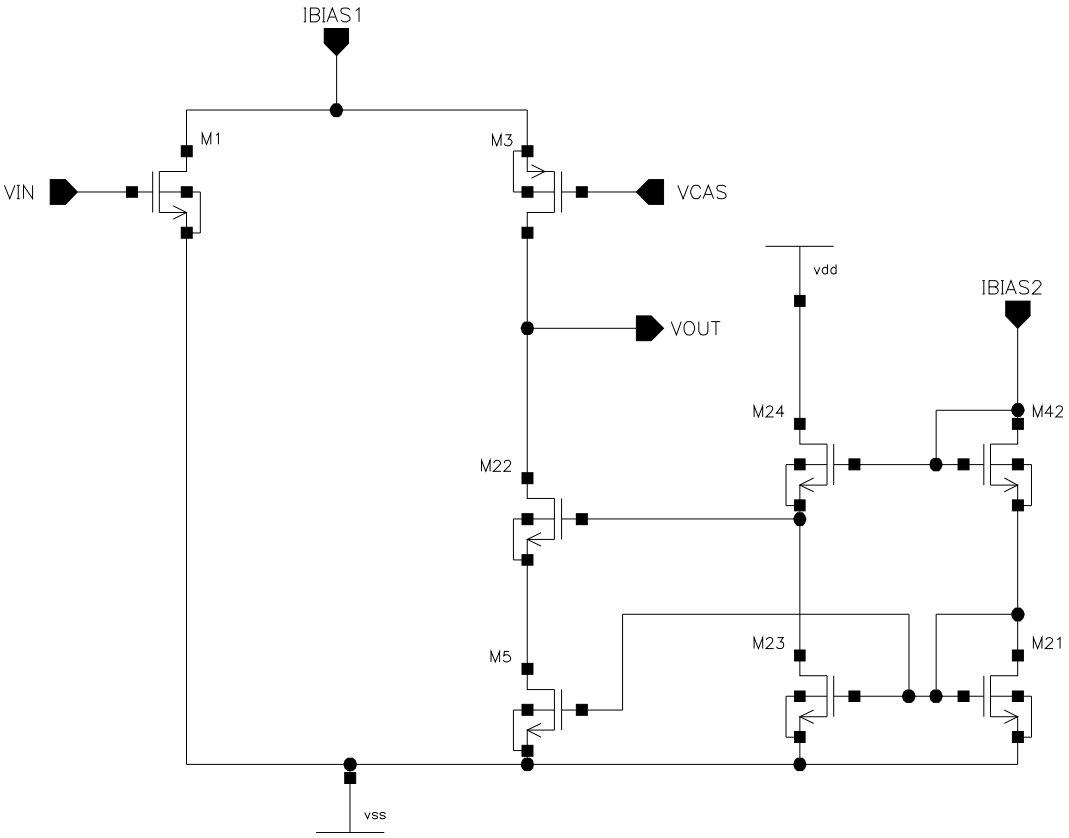

Figure 5.2: Folded cascode amplifier with NMOS input transistor, with cascode load[20].

The final design of the CSA is shown in Figure 5.2 and Table 5.1 shows the widths and lengths of the transistors. MM1 and M3 creates a folded-cascode amplifier, M24, M42, M23 and M21 is the the cascode current mirror for loading the output. The feedback is from the base of M1 to the source of M3, and the feedback resistor and capacitor is not shown here, but can be seen in Figure 5.3.

The bias currents, I_{BIAS1} and I_{BIAS2} are supplied from the self-biasing V_tReference Circuit described in Section 5.3.

The current on I_{BIAS1} is set to 2.25 mA, where half of the current flows through the M1-transistor and half flows through the M3-transistor. The bias

current I_{BIAS2} is set to 75 µ A. The voltage on V_{CAS} is set to 600 mV.

Component	Width	Length
M1	2.5m	300n
M3	1m	300n
M22	150u	300n
M5	150u	300n
M23	10u	300n
M24	10u	300n
M21	10u	300n
M42	2.5u	300n

Table 5.1: Widths and lengths of all transistors in the CSA circuit diagram shown in Figure 5.2

To set $V_{DS1} = V_{ov}$, the overdrive voltage of M42 is doubled by reducing $\frac{W}{L}4$ by a factor of 4 [7].

5.2.1 Amplifier Feedback

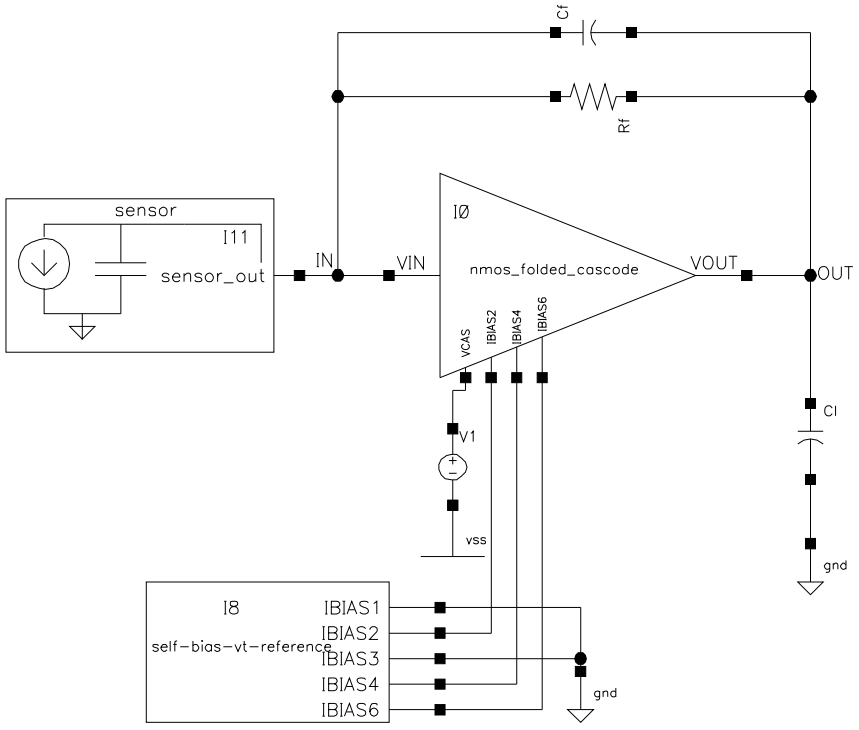

Figure 5.3: Top level schematic of the CSA with feedback, bias network connected, and a detector model as input

The cascode amplifier will only work in a feedback configuration due to its large gain. For testing purposes this can be solved by connecting a wire from

the output to the input, but this fix will not work with an ideal input source due to the feedback is driving the same not as the input source.

The resistance in the feedback, R_f, is realised with a large (in the range of mega Ohm) NMOS-transistor. This transistor contributes to parallel noise so its size is a compromise between noise and count rate..

The time constant of the feedback, $\tau = R_f * C_f$, is the time constant of the discharge of the signal.

The goal of R_f is to discharge the signal, to keep the amplifier going into saturation and distorting the signal, keeping the time constant large will increase the chance of pile-up effects, due to the increased charge-collection time , and also keeps the CSA from going into saturation by discharging C_f.

The resistor R_f is realised with a NMOS to reduce the footprint of the component, but in the simulations it is a regular resistor.

5.2.2 Dynamic Input Range

The amplifier must be able to handle a wide range of input energies and this is a challenge. The electron detectors have an input range of 30 keV to 1500 keV, i.e a dynamic range of 50, and the electron channel has an input range of 150 keV to 9600 keV, a dynamic range of 64.

The smallest incoming particle with a charge 30 keV gives a 24mV signal on the output, and the largest particle with 1500keV gives an output of 1.2V

Since the requirements of this instrument was a signal-to-noise-ratio of 3 for the 30 keV-particles, an output signal of 24 mV sets the maximum noise of 8mV.

5.2.3 Output Loading

The CSA is loaded with a double cascode load. The transistors M22, M42, M24, M5 and M25, from the schematic in Figure 5.2, form this load. Each cascode load increases the output resistance by a factor of $1 + gm * ro$ [7].

As the cascode amplifier only has one stage so Miller-compensation is not possible, and as the output resistance is kept low the folded cascode suppresses the Miller-effect [7].

5.3 Self-biasing V_t Reference Circuit

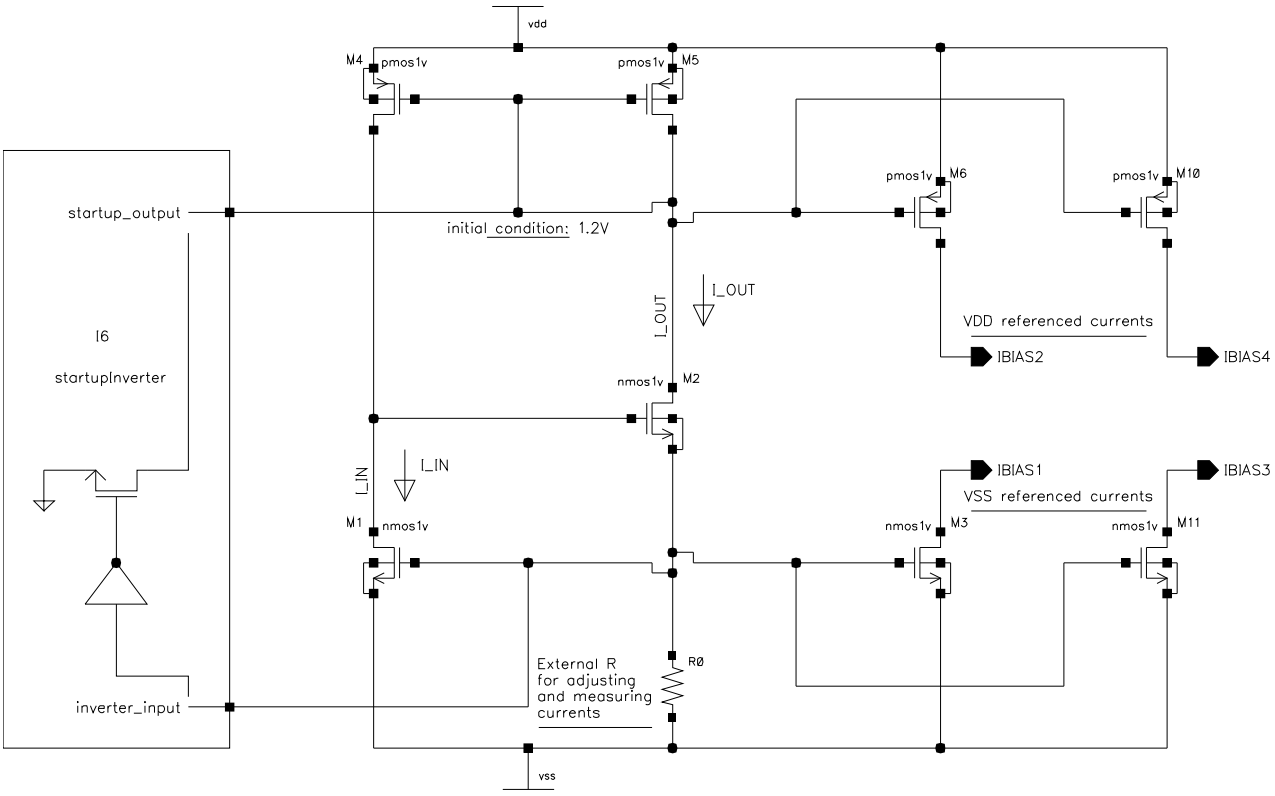

Figure 5.4: Circuit diagram of the V_t bias reference circuit

To supply separate currents to bias all transistors a V_t bias reference was designed. MOS Widlar current sources does not provide adequate power supply independence for many types of analogue circuits. Lower sensitivity can be obtained by causing the bias circuit to depend on a voltage other than V_{DD} or V_{SS}.

This bias topology is also stable across a wide range of temperatures as shown in in the simulation results in Figure 5.7 and in the calculation in Section 5.3.3.

The resistor, R0, shown in the circuit diagram is meant to be connected externally to the integrated circuit. This allows adjustments of the currents, and provide a place to measure the currents.

Component	Width	Length
M1	30.2u	300n
M2	25u	300n
M4	60u	300n
M5	60u	300n
M7	60u	1.3u
M8	260n	130n
M9	100u	300n
M6	As needed	300n
M3	As needed	300n
M10	As needed	300n
M11	As needed	300n

Table 5.2: The width and lengths of all transistors in the V_t bias reference circuit diagram shown in Figure 5.4. M7,M8 and M9 are in the start-up inverter-component to the left, also shown in Figure 5.9. M3,M6,M10 and M11 are sized per the current requirement for that bias-branch

5.3.1 Threshold Reference Circuit

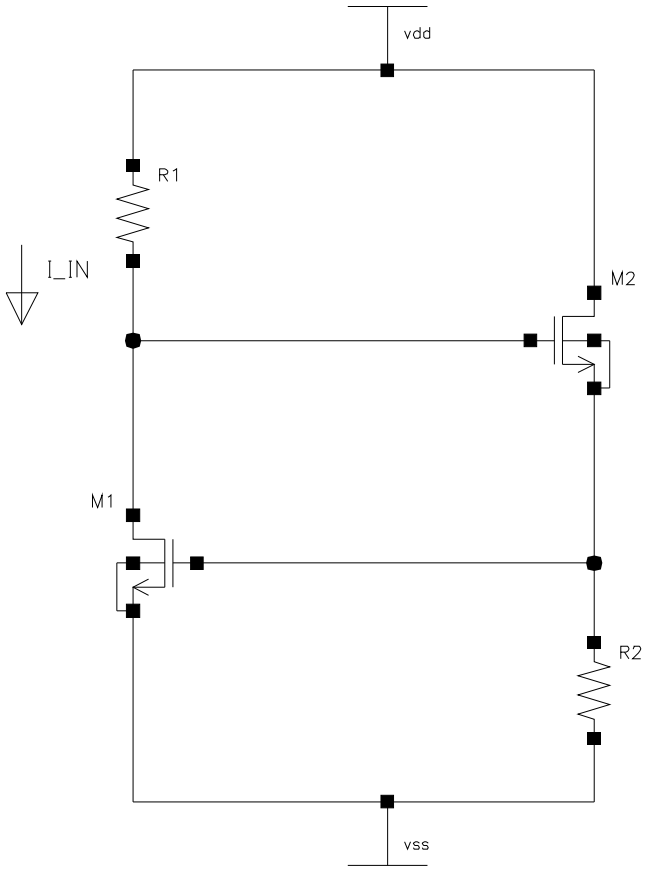

Figure 5.5: The current reference circuit part of the V_t bias reference circuit. The size of the transistors are shown in Table5.2

The circuit diagram shown in Figure 5.5 is part of the schematic shown in Figure 5.4, and is used to determine the size of M1 and M2. The goal when sizing these transistors is to set the sizes to the two branches gave the same current, 100 µA in this case. The plot shown in in Figure 5.6 illustrates how the size of M1 and M2 are selected. For the current mirror consisting of M4 and M5 the sizes are set $W_{M4} = W_{M5}$. The current I_{out} is calculated according to Equation 5.3.1.

$$I_{out} = \frac{V_{GS_1}}{R_2} = \frac{(V_t + V_{dsat1})}{R_2} = \frac{V_t + \sqrt{\frac{2I_{in}}{k' \frac{W}{L} 1}}}{R_2}$$

$WL1$, $WL2$ and R_2 here are the components shown in Figure 5.5.

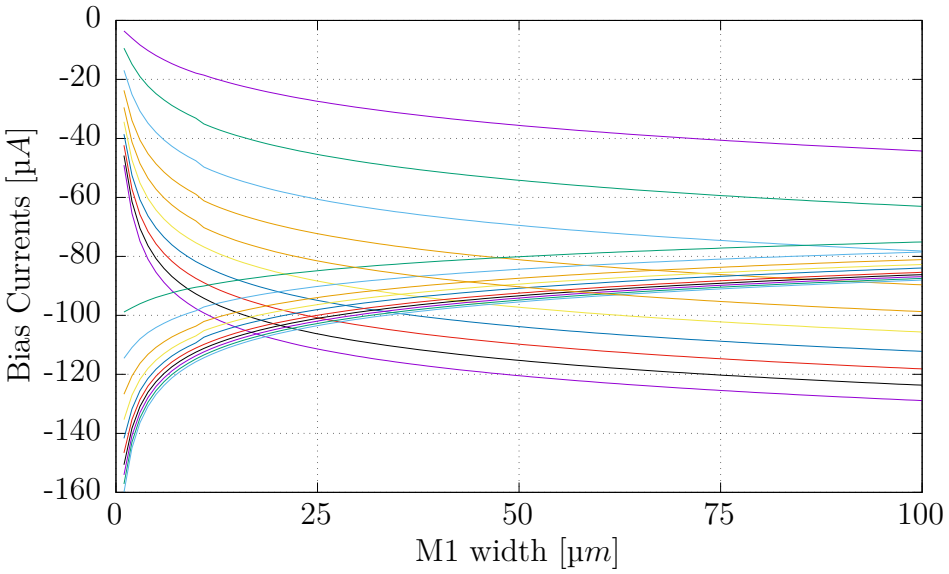

Figure 5.6: Simulation of the input vs the output current of the threshold Reference Current. The point where the currents cross is the possible sizes that can be chosen for M1 and M2

5.3.2 Temperature Dependency

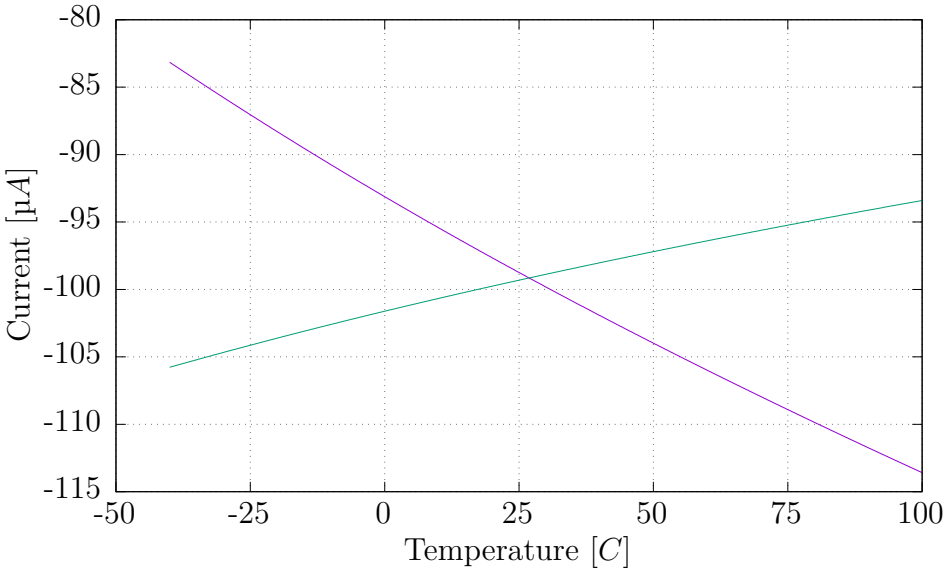

Figure 5.7: Simulation of the input vs the output current of the threshold Reference Current, and how they change with temperature

Figure 5.7 shows the temperature dependency of the threshold reference currents. Using a V_t bias reference gives a stable output current over a wide range of temperatures. The target is to have the part where the currents

cross, as the normal operating temperature for the instrument, to get as stable currents as possible. As stated in the requirements in table 1.1 the temperature range this system will be in is quite wide. The normal operating range for this will be -20 to +60. The instrument will not need to operate in the most extreme temperatures, which is under launch, but it must survive.

5.3.3 Power Supply Isolation

Another advantage with this circuit is independence from the power supply. The sensitivity of the output current to variations of the power supply can be calculated as shown in Section 5.3.3.

$$S_{I_{out_{vdd}}} = \frac{V_{ov} S_{Iin_{vdd}}}{2V_{GS1}}$$

For the chosen design this results in the following dependency on the power rails:

$$S_{I_{out_{vdd}}} = \frac{462.1mV}{4k\Omega} = 115.5\frac{\mu V}{T}$$

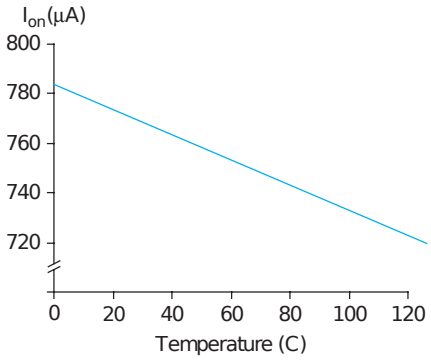

Figure 5.8: Simulation results showing a typical saturation current vs temperature[20]

This solution gives less noise across the different bias currents, and reduces crosstalk [17].

I_{BIAS2} is currents referred from V_{DD} and I_{BIAS1} is current referred to V_{SS}. For the mirrors that are referred to VDD PMOS-transistors are used, and for the VSS-referred NMOS are used.

The reference currents can be copied by connecting transistors in parallel with the diode-connected one. If one assumes V_t is equal and disregard channel modulation the currents can be expressed by

$$\frac{I_{DS1}}{I_{DS2}} = \frac{\frac{W}{L}1}{\frac{W}{L}2}$$

[15]

To make sure the current mirror can deliver enough current to the transistors up top M6/M16 has to be large enough. Since the electron mobility

is worse in pmos than nmos, the pmos has to be scaled approximately 2x the size of the nmos.

If the p-part of the mirror uses to much of the voltage there will not be enough to to get the n-part (m16) to saturation.

M16 is supposed to be in saturation per definition since $V_{DS} = V_{GS}$ but since the voltage on the drain is not enough this will not work.

5.3.4 Start-up Circuit

The current mirror described in Section 5.3.1 has two modes of operation, and only one of them is usable for this purposes. To make sure it is in the correct mode after start-up a Start-Up Circuit is required, shown in Figure 5.9.

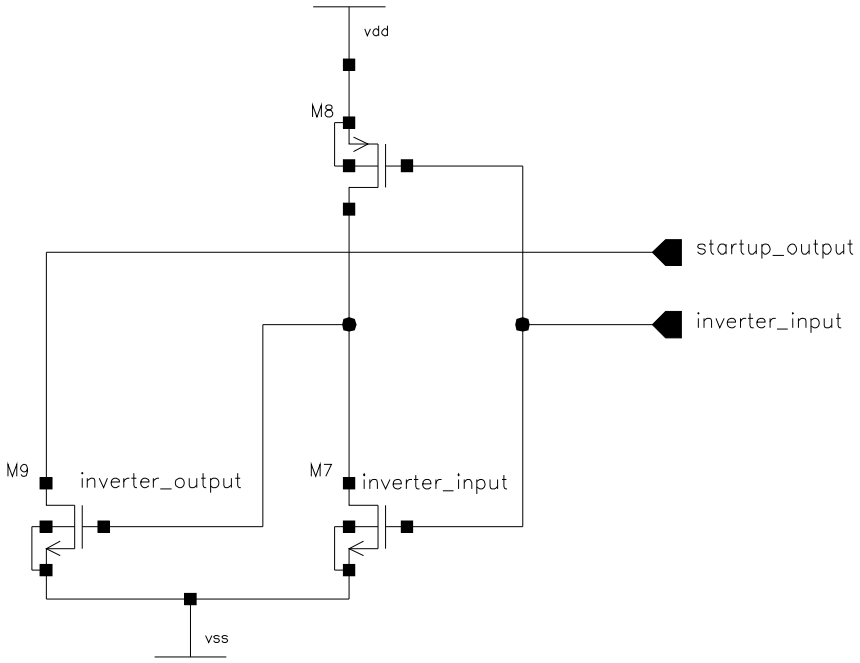

Figure 5.9: Self-biasing V_t reference-start up circuit. The size of the transistors are shown in Table5.2

The circuit diagram shown in in Figure 5.9 M7 and M8 forms a low skew inverter that inverts when the voltage is above 330 mV. This requirement is satisfied when $\frac{W}{L}7 << \frac{W}{L}8$.

With M7 L=1.3 μ, W=60 μ and M8 L=130n, W=260 n the inverter activates at $0.325V$. A simulation of this inverter is shown in Figure 5.10. The 260nm width of M8 is 2x the minimum length and is to avoid the worst of the production variation.

A goal with the sizing is to make sure the inverter is mostly on and not so much off, to avoid wasting power having the transistor in saturation.

M9 in the Start-up circuit is not supposed to be in saturation, only when the bias circuit has to be forced low. In the simulation it was necessary to set a initial condition on the drain-node of M9 to 1.2V to make sure the simulation behaved regularly in each simulation run.

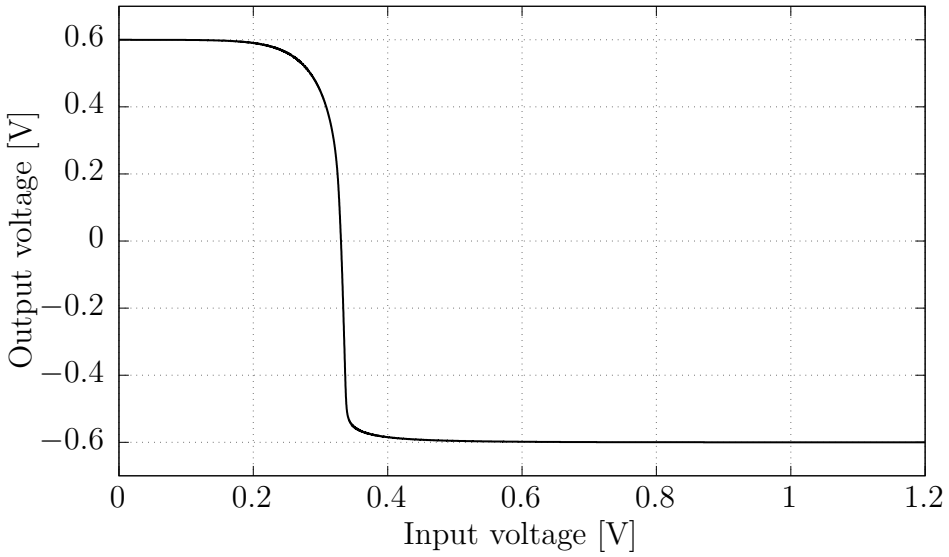

Figure 5.10: The inverter characteristics of the skewed inverter of the of the Start-up circuit

The voltage 0.4 V is set by the voltage over R0, M2 and M5. If the voltage there is to low the current mirrors in the bias circuit works in the wrong area

5.3.5 Power Optimisation

Further optimisation of this circuit can be done by turning down the current in the Threshold Reference Circuit to supply the smallest current needed for the circuits supplied by bias current network, and then scale the current up locally. Currently the current mirror in the VT referenced bias network supply the largest current necessary, 100 µA, and then each output transistor scale the currents down to the required current for that branch. By scaling down these transistors, the required power will be reduced a significant amount.

5.4 Shaping Amplifier

The shaping amplifier was realised with a CR-RC filter, shown in Figure 5.11. The voltage buffer-components are described in Section 5.4.4.

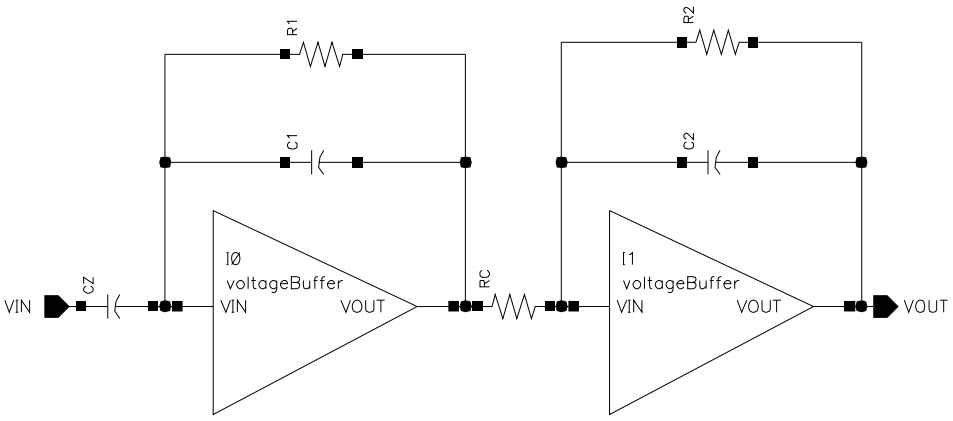

Figure 5.11: Circuit diagram of the shaping amplifier

Component	Value
C_z	5p
R_1	100k
C_1	500f
R_V	36.8k
R_2	100k
C_2	500f

Table 5.3: Component values for the circuit diagram shown in Figure 5.11

The capacitor C_Z is not terminated over ground as shown earlier in a schematic, but the input to the first voltage buffer can be considered as virtual ground.

$I_{C_Z} = I_{in}(s) \times \frac{C_Z}{C_F}$, therefore C_Z is sized larger than C_F

Since the time constants of the integrator and the differentiator are set equal ($\tau_1 = \tau_2 = tau$), the output voltage can easily be calculated as

$$V_{out}(t) = \frac{Q_{in}}{C_f}\frac{C_Z}{C1}\frac{R_2}{R_C}(\frac{1}{\tau})e^{-\frac{t}{\tau}}$$

The gain of the two stages is set to be as large as permitted by the dynamic

range. The output of the second stage is $V_{out2}(t) = \frac{Q_{in}}{C_f}\frac{C_Z}{C1}e^{-\frac{t}{\tau}}$. To exploit the dynamic range, the gain of the second voltage buffer is set to 2.718, to compensate for the gain loss of having the output reduced by a factor $\frac{1}{e}$[15].

5.4.1 Performance Goals

Goal: Peaking time 50ns. Gain: $\frac{10mV}{fC}$ out of the CSA.

5.4.2 Time Constants

$\tau_z = \infty$ gives no derivation/the signal never returns to baseline, figure 6.6.

If $\tau_p > \tau_z$, τ_p starts to dominate the signal. This gives a flat signal top and a long tail, return to baseline, and no real peak. Figure 6.5. These two considerations are what has to be balanced in a trade-off. Setting $\tau_p = \tau_z$ provides a good compromise to maximise the amplitude while, ...

5.4.3 Shaping Filter Design

With a goal of a peaking time of 50 ns and a quick return to baseline. These two requirements are the inverse of each other so a compromise will have to be reached.

To reduce the amount of different components, and thus making it easier to lay out, R_1 was selected to be equal to R_2, and C_1 to C_2, to minimise the number of different components.

To maximise the gain in the CSA, so that one can use the whole dynamic range and to minimise the total noise, the following calculation is done:

$$V_{out_{peak}} = \frac{Q_n}{C_f}\frac{C_Z}{C_1}\frac{R_2}{R_C}\frac{1}{e}$$

Where Q_n is the input charge, C_1, R_1 *and* R_2 are the components that set the time constant for the shaping and e is the euler-number.

$$\implies \frac{C_Z}{C_1}\frac{R_Z}{R_C} = 10e = 27.18$$

Now the signal from the CSA is rail-to-rail and the relative noise is low in the shaping-stages.

Sizing of the components

By selecting these component values: $C_1 = C_2 = 0.5\,pF, R_1 = R_2 = 100\,k\Omega \implies C_Z = 5\ pF, R_C = 36.8\ k\Omega$ the requirements set in Section 5.4.1 are met.

5.4.4 Voltage Buffer

The output impedance of the cascode configuration is high and thus the output is sensitive to the connected load. Therefore it is necessary to protect the output of the CSA with a high input impedance and low output impedance, and this is typically done with a source follower. The source follower can be used to buffer a high gain cascode stage with a voltage buffer, as shown in Figure 5.12.

The voltage buffer was designed, and a circuit schematic was drawn, but it was not made into a functional device due to time limitations.

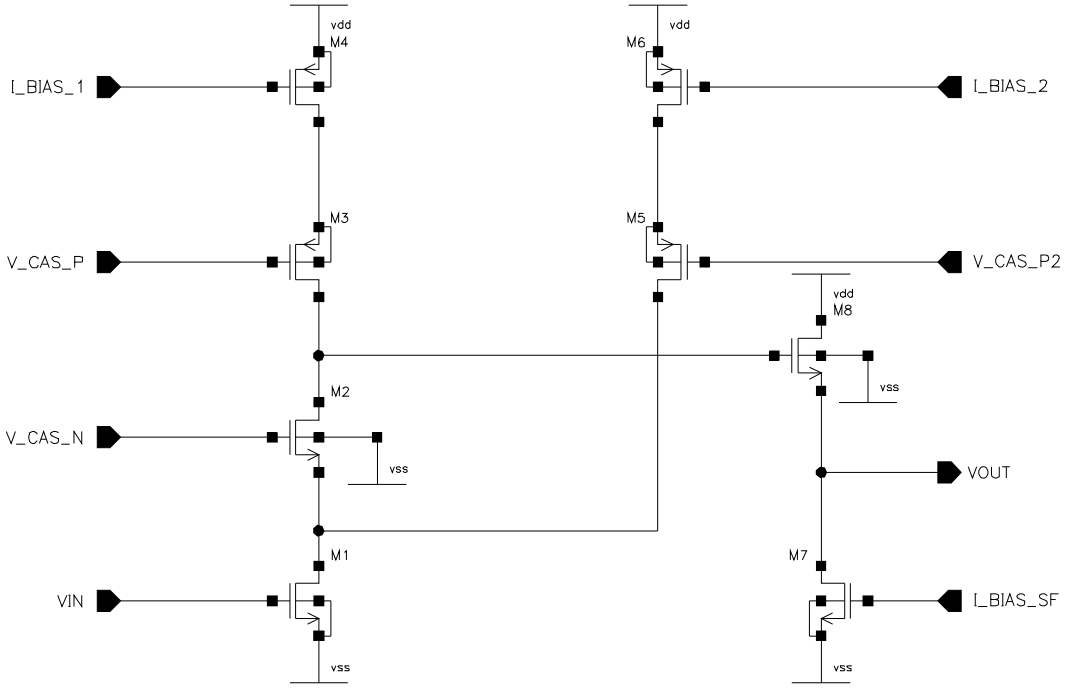

Figure 5.12: Circuit diagram of the NMOS-input buffered telescopic cascode amplifiers used as voltage buffers used in the shaping amplifier [20]

5.4.5 DC Baseline Between Blocks

To exploit the complete dynamic range between the CSA and the shaping amplifier one can use a non-symmetric DC-level. Instead of swinging from -0.6 to +0.6, the baseline can be se at 0 V and the signal swing is up to 1.2 V, and from 0 V to -1.2 V in the inverting stages, one can acquired a higher signal resolution.

5.4.6 CR-RC^N-shapers

By adding multiple integrators one can increase the order of the shaper, and by doing this, the peaking time increases. The peaking time is given by the integration time constant multiplied by the number of integrators. The peak amplitude can be calculated

$$V_{out,\max} = \frac{Q_{in}}{C_f} G \frac{n^n}{n!} e^n$$

where G indicates the overall additional gain that might be inserted into the chain of integrators.

See for example CMOS: front-end electronics for radiation sensors [15] for more on this.

5.5 Radiation Detector Model

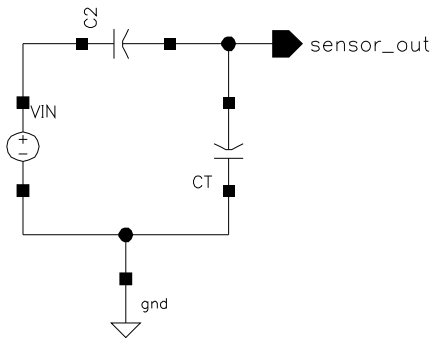

Figure 5.13: Circuit diagram of the detector-model used in the simulation.

For simulation purposes a detector model was created and used as input to the amplifier. The resulting circuit diagram is shown in Figure 5.13. The V_{IN}-source in the detector model was modelled with a typical rise time of 10 ns [10].

The signal pulse has a width of 50 ns and the capacitance is in accordance to the calculations in Section 3.8. There is also a capacitance in series with the input to only let through the AC.

5.6 Test Bench Set-Up

To verify that the designed circuits fulfil the specifications a complete test-bench is required. The the parameters that need to be characterised are gain, bandwidth, stability and phase margin, power consumption, power supply rejection rate, noise, slew rate, linearity of the amplification, I_{input} vs I_{output},shaping time / RC delay, pile-up effect tolerance

To be able to determined several tests have been set up in Cadence as shown in Figure 5.14.

As Figure 5.14 shows, one can set up tests with expressions that are applied to the output of the tests. ADEXL have functions such as rmsNoise(), that gives the RMS noise of a signal, db20(), that gives the the magnitude of a signal vs another signal, and bandwidth(), that gives the bandwidth of a selected signal.

Outputs Setup | Results

Test	Name	Type	Details	Spec
ac		signal	/VOUT	
ac	magnitude	expr	db20(VF("/VOUT"))	
ac	phase wrapped	expr	phase(VF("/VOUT"))	
noise	rms noise	expr	rmsNoise(1 1e+10)	< 1000
ac	phase unwrapped	expr	phaseDegUnwrapped((VF("/VOUT") / VF("/VIN")))	> 60
ac	bandwidth	expr	bandwidth(VF("/VOUT") 3 "low")	> 2M
ac	phasemargin	expr	(phaseMargin(VF("VOUT")) + 180)	> 60
ac	gain	expr	dB20((VF("VOUT") / VF("VIN")))	> (60 + 180)
tran		signal	/VOUT	

Figure 5.14: Test set-up in Cadence Virtuoso

All of these expressions can be given specifications that are larger, smaller, equal to a specification or they can be given as “minimize” og “maximize” that can be used to run Monte Carlo simulation that explore variations and tries to optimise the circuit to the specified values.

DC Simulation

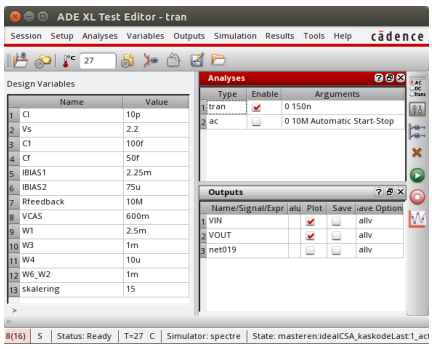

Figure 5.15: An example of a DC simulation with variables used for component parameters, shown in the table to the left

DC steady-state parameters of every transistor was used in the development of the designs. Performing this simulation allowed the designer to get insight in the operating parameters of individual transistors to determine gm, ro, and overdrive voltages and to visualise easily the modes of operation and determine if the transistors were in saturation. See Figure 5.15 for an example of a DC-test set-up.

5.7 Simulation Results

5.7.1 Gain Simulations

The amplifier has an open loop gain of 34 dB. This limits the integration in the feedback of the CSA and this should ideally be infinite, but for this purpose 60 dB would be enough. When increasing the input signal from Vs from 1 mV to 0.5 V, the operating area, M3 leaves saturation when the input reaches around 2.2 V, meaning gain is lost on high input signals.

A gain of 44 dB results in $\frac{1.3mV}{fC}$, which is the current maximum gain, as seen in the simulation results in Figure 5.16.

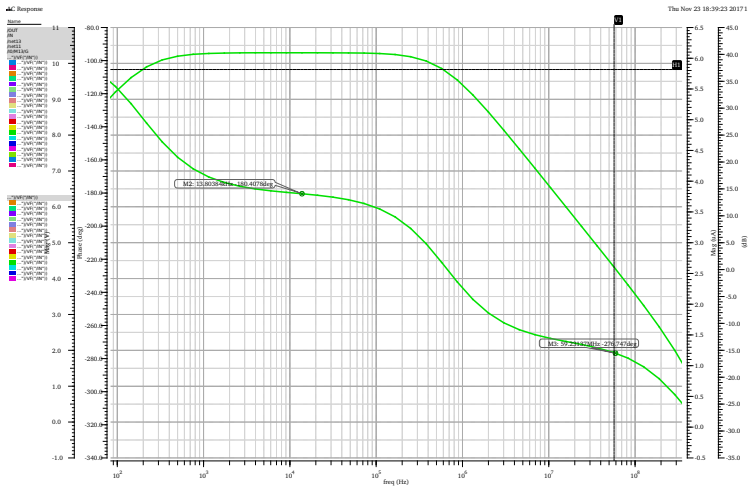

Figure 5.16: Bode plot showing the gain and the phase margin for the CSA

Transient simulation

A 100 µA input signal was put on the input to simulate an incoming charge. Figure 5.17 shows the input step and how the output changes in response.

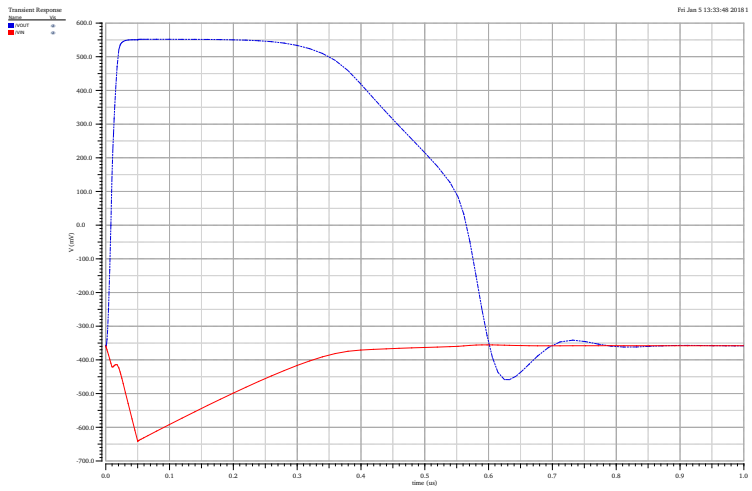

Figure 5.17: Simulation showing an input pulse (red) and its corresponding output pulse (blue)

5.7.2 Power Consumption

To make an estimate of the consumed power a DC simulation was run on all circuits and all component parameters were extracted from the simulation results. Further the "pwr"-parameter of all components were summed and a small adjustment was done to account for power not-used by transistors that were not in saturation, but was supposed to /had to be in saturation for the design to work.

A single channel of this instrument consists of a CSA, two voltage buffers and require a bias-network to supply currents. The total effect is obtained by summing the effect used in these design and results in 8.63 mW per channel, and for all 72 channels that totals to 621 mW.

This is lower than realistic, since voltage buffer is not working, and bias network / power network needs more transistors to supply all the necessary currents and the voltage buffer is not using as much as it probably will (since it is not amplifying and not scaled).

5.7.3 Area Usage

To make an estimation of the area required to create a layout of this circuit, the width and the length of each transistor has been multiplied and then the area for each transistor has been summed. These estimations are for the nominal transistor models and are just an estimate of the final area.

The area estimated for the CSA, as shown in Figure 5.2 is $1.15 \times mm^2$. This is not including transistors needed to set bias currents, R_f and C_f does not use any area. The usage of the bias network-design, as shown in Figure 5.4 is $16.6 \times 10^{-3} mm^2$, with four bias currents being supplied. An estimate was also done for the voltage buffer-design shown in Figure 5.12 resulting in an area of $4.8 \times 10^{-6} mm^2$, but as this is only an early prototype, this number might not be reliable.

5.8 Sensitivity Analysis

To explore which components, currents, voltages were important for the operation of the amplifier a sensitivity analysis was performed.

ADEXL the simulation suite in Cadence Virtuoso allows to set up tests where one sweep circuit parameters over a range of values. This allows the

designer to test a wide range of variable values with an experimental method in a quick and easy way and too see how the characteristics behave with different stimuli. Figure 5.18 illustrates a sweep simulation.

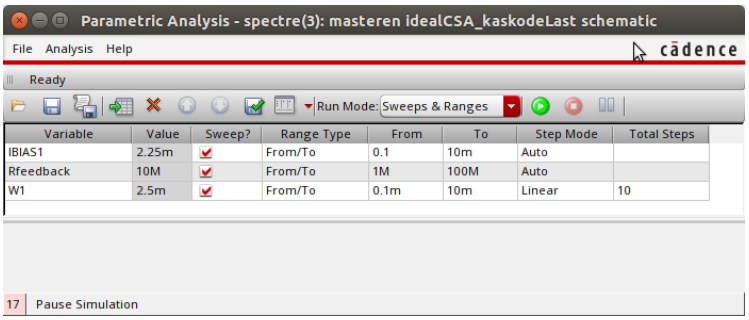

Figure 5.18: An example of a parameter-sweep simulation in Cadence Virtuoso showing three different sweeps with 10 simulation points of the W1-variable

For the sensitivity analysis of the CSA firstly the size of all transistors in the CSA was swept to see how variations affected them. Further the incoming bias currents and voltages were swept to see which values were gave valid results and how to size them to use the least amount of power.

Corner simulations was not done for these circuits due to technical difficulties with the simulation-models.

CHAPTER 6

Discussion

6.1 Performance Comparison With Published Designs

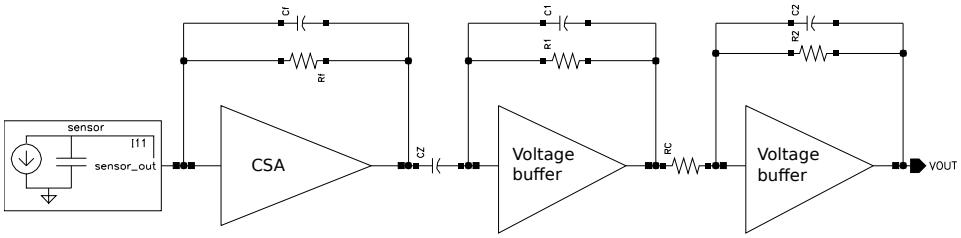

Figure 6.1: The resulting complete front-end electronics

Characteristic	My work	PASA [18]	FAIR [17]
Noise figure [e]	—	244 ± 17	330 ± 12
Gain [mV/fC]	1.3	12.74	12.64
Peaking time [ns]	—	160	≈ 170
Recovery time [ns]	—	900	200
Area[mm^2]	—	18	12
FWHMns	—	190	71
Power consumption [mw/c]	8.63*	11.65	16
Process technology	TSMC0.13u	AMS0.35u	AMS0.35u

Table 6.1: Comparison of this work to published shaping amplifiers. The entries with * are rough estimates

6.2 Simulation Model Accuracy

The simulation results should be very accurate, but one still would have to do a rigorous test of the physical design in the end. The design models used are SPICE models from TSMC and are probably complex models that model all circuit parameters to a reasonable complexity.

6.3 CAD Tools

Cadence Virtuoso was used to design this project. The software is taught in courses and licenses and technology packs are set up on the computers.

It is not the most accessible software, but Cadence has created a large selection of training videos online which explains the creation of test-benches and layout practices.

Cadence Virtuoso would probably be used again for the next project.

6.4 Future Work

The thesis started out with an unrealistic goal, and everything took longer than estimated resulting in only parts of the system was completed. The work got stuck at some parts and this kept the thesis from progressing at the necessary speed to produce a complete, working design.

Due to that the project still is in an early phase there are many requirements that change and parts of the work done here might need to be modified to fit these updated requirements. There are quite a lot of remaining tasks that need to be completed before the system is operational and can be sent to production.

The CSA should be completely characterised and optimised for power usage. Further a layout of the integrated circuit needs to be designed.

The shaping amplifier design needs to be realised and the components sized, so the circuit fulfils the requirements. The shaping amplifier also needs to be fully characterised with simulations and a layout needs to be made.

When all circuit schematics has been verified and a layout is made, a complete channel layout needs to be put together, with a CSA, shaping amplifier and connections to the bias network is in place. An electromagnetic simulation of the single channel should also be performed.

A layout with all 72 channels is the next thing that needs to be done. This is the final integrated circuit in this layout the power distribution network needs to be designed, and after the chip is put together, an electromagnetic simulation for the complete circuit must be done.

If a ADC Semiconductor Intellectual Property Core for the process is decided to be the solution for digitising the analog signals, this needs to be integrated in, before the final chip is produced and verified.

CHAPTER 7

Conclusion

A thorough study of charge sensitive amplifier theory has been carried out in order to obtain knowledge essential to the design of the front end electronics.

Based on the attained knowledge a low noise amplifier with 34 dB gain, 621 mW has been designed in a 0.13 µ m CMOS process. The amplifier fulfils some of the specifications given, based on results from simulations in Cadence Virtuoso. These results are only simulations, but it is believed these results can be obtained with a manufactured design, but even if these results can be obtained, the amplifier is not competitive compared to other published designs, and need more work to be usable.

APPENDIX A

Wiki Articles

Several wiki-pages were written on the wiki of Department of Physics and Technology during the work on this thesis. The topics of these articles were test-bench set-up and usage, and set-up and configuration of Cadence Virtuoso. The wiki is browsable at https://wiki.uib.no/ift.

APPENDIX B

Circuit Schematics

In this appendix a complete list of all schematics are listed. See the section in Chapter 5 for the sizes of all components and transistors.

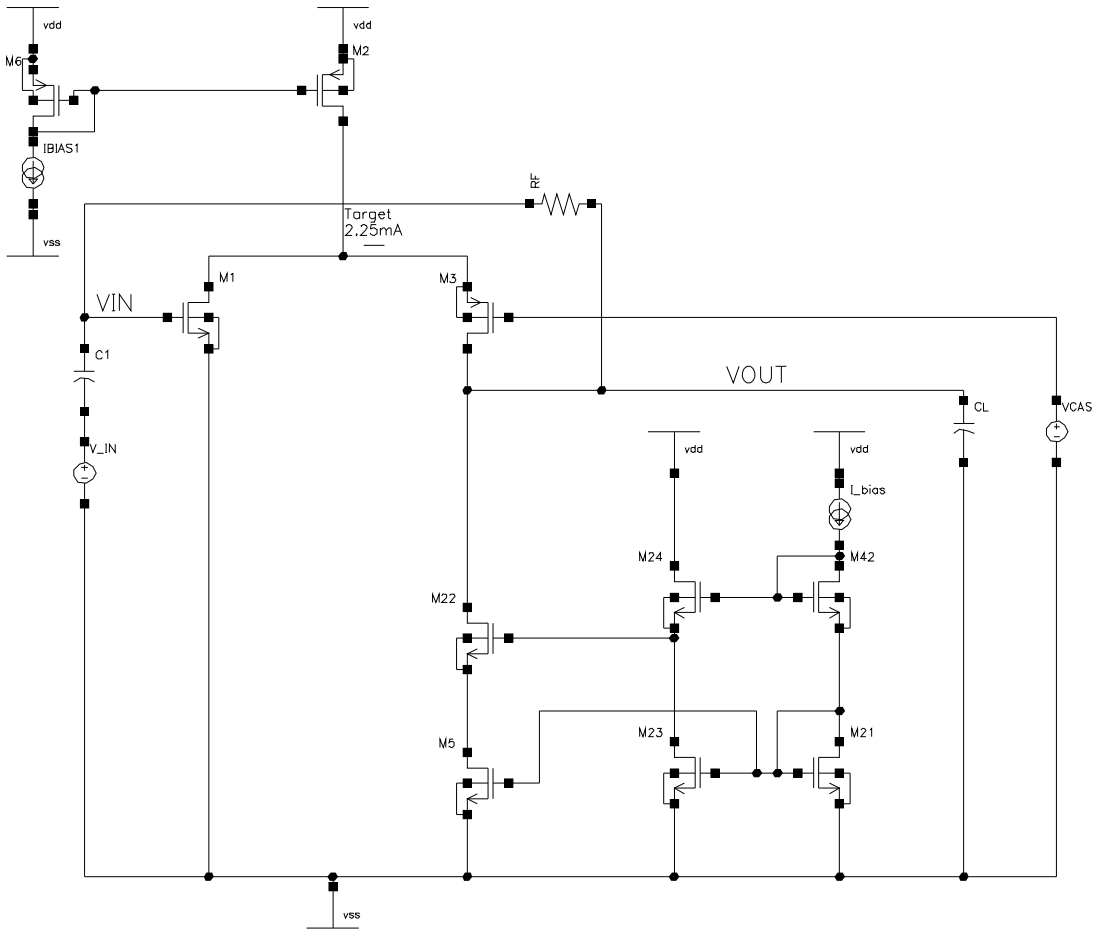

Figure B.1: Folded cascode amplifier with NMOS input transistor, with cascode load. This schematic shows a simulation setup with ideal sources for the bias currents, a feedback capacitor, capacitive load, but no feedback capacitor.

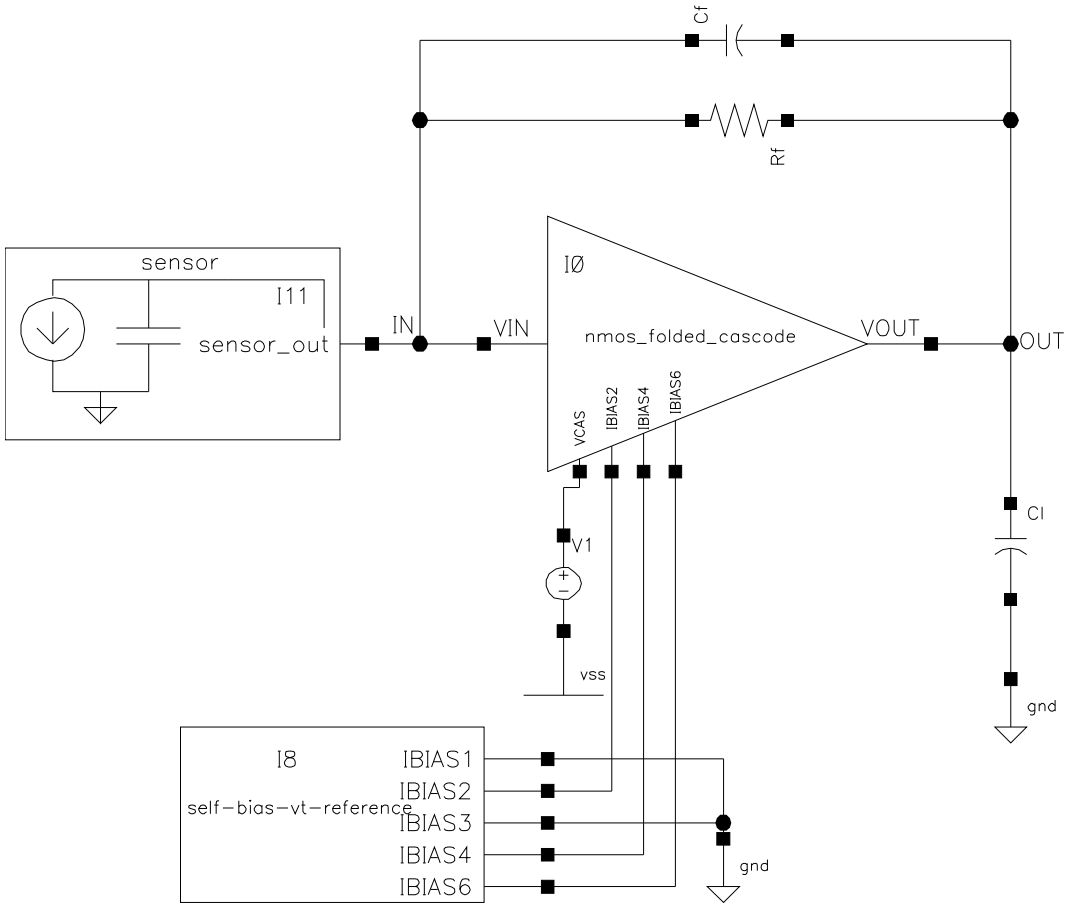

Figure B.2: Top level schematic of the CSA with feedback, bias network connected, and a detector model as input.

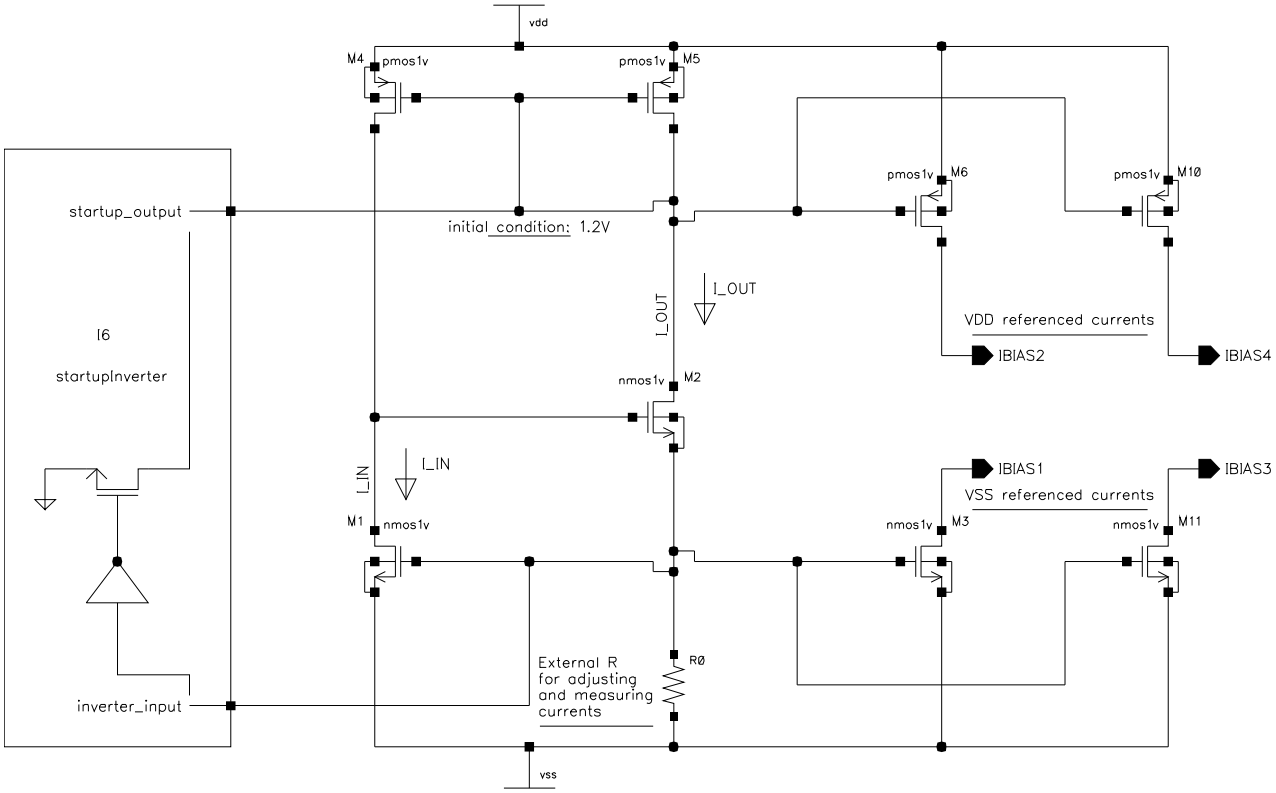

Figure B.3: VT bias reference circuit.

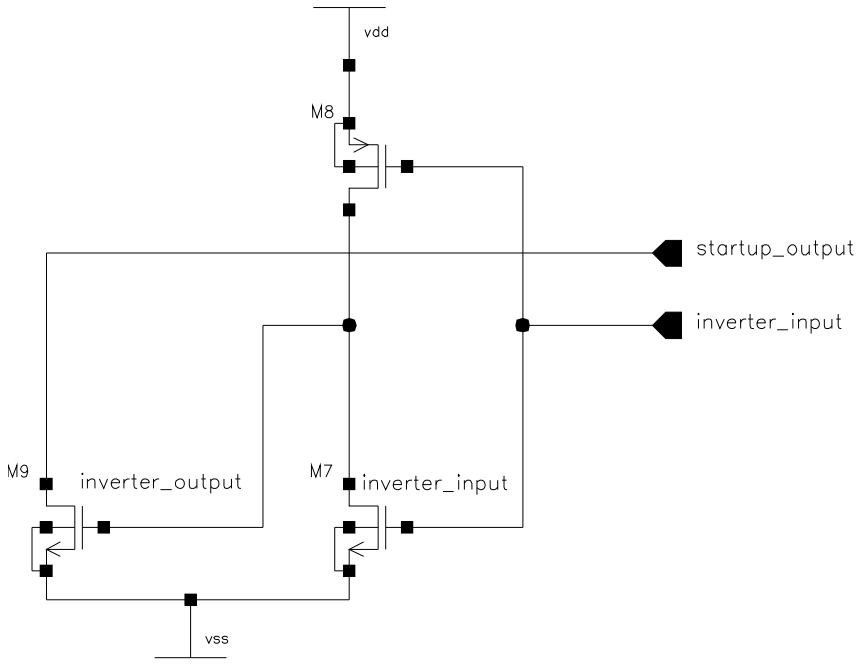

Figure B.4: Self-biasing V_t reference-start up circuit.

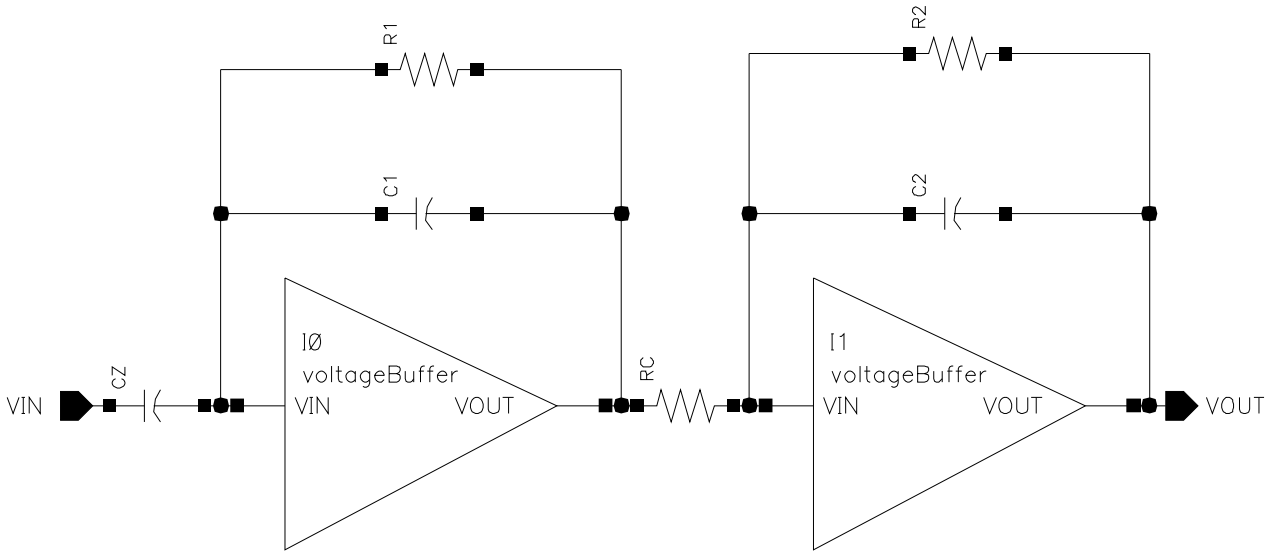

Figure B.5: Top level view of the CR-RC shaping amplifier.

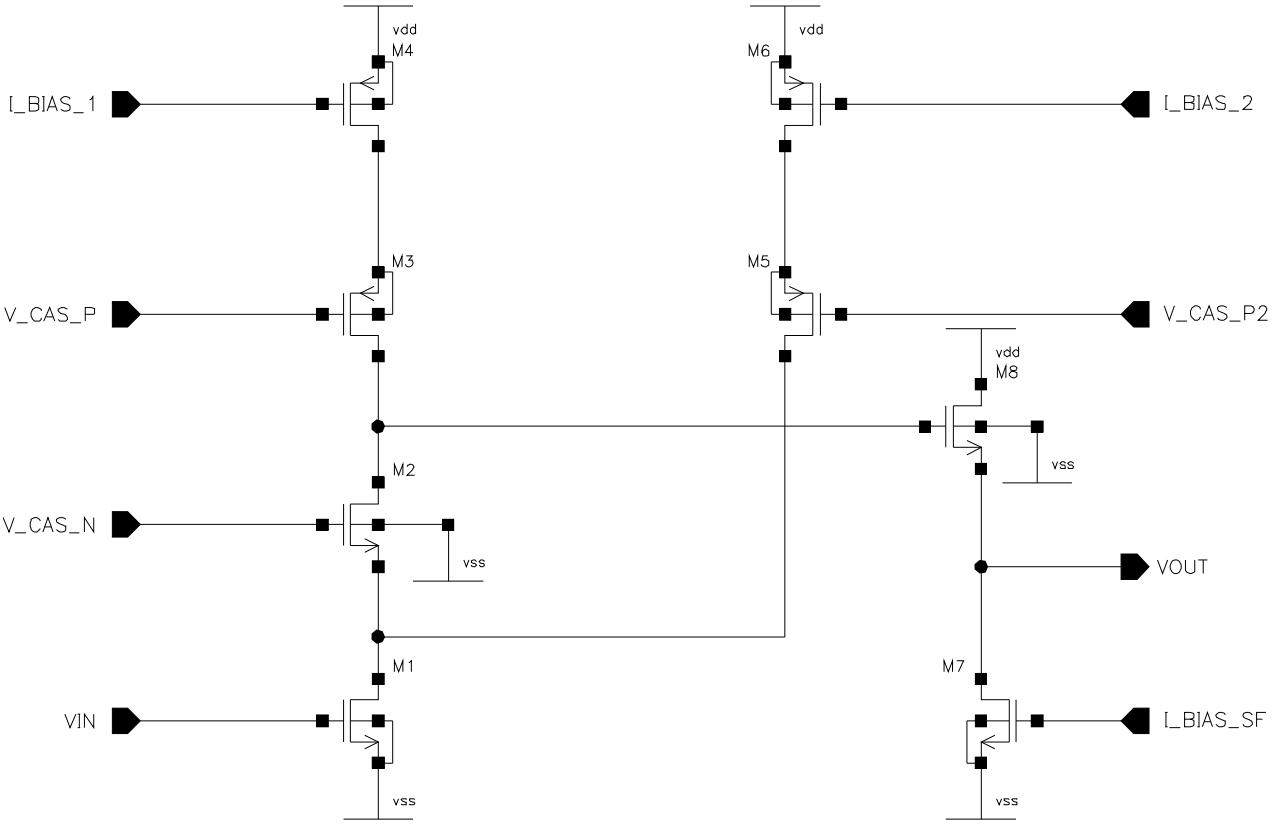

Figure B.6: The voltage buffer used in the shaping amplifier.

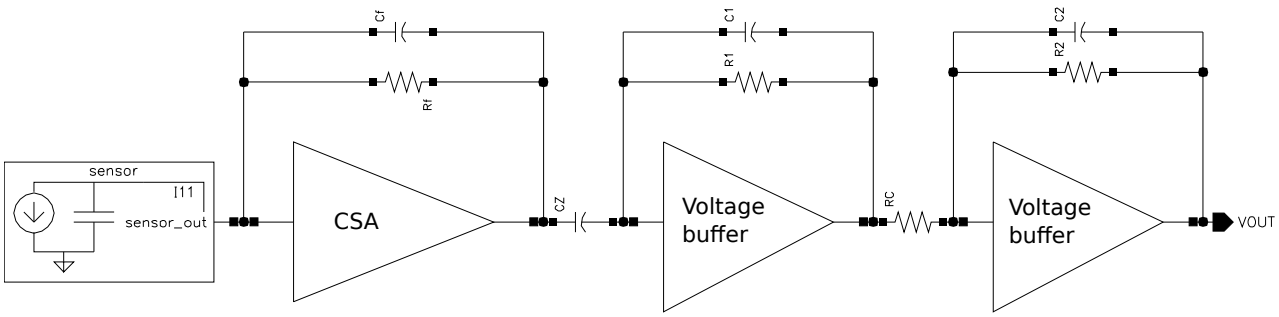

Figure B.7: Complete front-end electronics.

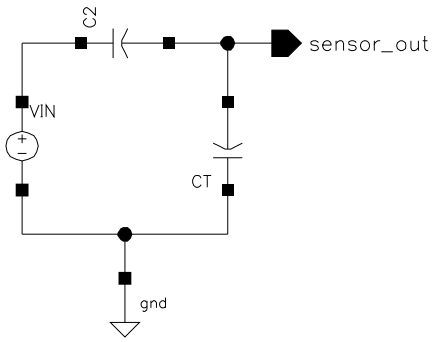

Figure B.8: Circuit diagram of the detector-model used in the simulation.

APPENDIX C

CMOS Technology Selection

The information in this appendix is from open sources [4], and is therefore limited in what is disclosed, since technology specification are industry secrets. The disclosed information also differs between technologies, so direct comparison is difficult. A comparison has been performed non the less and a conclusion was reached based on the following information.

Technology	SG25	SG25H1	SG25H3	SG25H3P	SG25H4	SGB25V
Node [um]	0,25	0,25	0,25	0,25	0,25	0,25
Type	CMOS	BiCMOS	BiCMOS SiGe	BiCMOS	BiCMOS	BiCMOS SiGe
MPW	unknown	unknown	Y	unknown	Y	

Table C.1: Available CMOS technologies in the IHP-foundry [5]

Technology	GD module (SGB25V)	SG13S	SG13C	SG13G2	RFMEMS
Node [um]	0,25	0,13	0,13	0,13	
Type	BiCMOS	RF CMOS SiGe	RF CMOS	Bipolar SiGe	Compromise of SG13S and SG13C
MPW	unknown	Y	unknown	Y	unknown

Table C.2: Available CMOS technologies in the IHP-foundry [5]

Technology	BEOL (only)	SG25_PIC	SG25H_EPIC	TSV
Node [um]		0,25	0,25	
Type	0,25 / 0,13			
MPW	Y	Y	based on SG25H4	

Table C.3: Available CMOS technologies in the IHP-foundry [5]

Process Type		Mixed Signal CMOS					Mixed Signal CMOS
Drawn MOS Channel Length	ţm	0,35					0,18
Operating Voltage	V	3,3	3,3	3,3 / 5,0	3,3	3,3 / 5,0	1,8 / 5,0
Number of Masks		13	14	17	16	20	22
Number of Alignments		18	19	21	21	24	22
Number of Metal Layers		3	3	3	4	4	3
Number of Poly Layers		1	2	2	2	2	1
Substrate Type		p					
Diffusion Pitch	ţm	0.9					0,48
Metal1/2/3/4 Pitch	ţm	0,95 / 1,1 / 1,2			0,95 / 1,1 / 1,1 / 1,2		0,44 / 0,56 / 0,56 / 0,56 / 1,20/ 4,50
Metal1/2/3/4 connected Pitch	ţm	1,05 / 1,4 / 1,4 / 1,14					0,56 / 0,56 / 0,56 / 0,56 / 1,20 / 6,04
Poly1 Pitch	ţm	0,8					0,42
High Resistive Poly	kOhm/square	-	-	-	-	1,2	-
Poly1/Poly2 Precision Caps	fF/ţmš	0,86					
NMOS/PMOS Effective Channel Length	ţm	0,38 / 0,50					
NMOS/PMOS Saturation Current (3.3V)	ţA/ţm	540 / 240					
Flip-Flop Delay	ns	0,53					0,18
NAND2 Delay	ns	0,12					0,03
NAND2 Area	ţmš	43,68					11,29
NAND2 Power	ţW/MHz	0,01					0,00
NAND2 Leakage Power	pW	0,24					27,52
Precision Poly	Ohm/square						-
Single MIM Capacitor	fF/ţmš						-
Dual MIM Capacitor	fF/ţmš						-
High VT Devices							-
NMOS/PMOS Effective Channel Length	ţm						0,18 / 0,14
NMOS/PMOS Saturation Current (1,8V)	ţA/ţm						600 / -250
WMP run:		?	?	?	?	Y	Y

Table C.4: Available CMOS technologies in the AMS-foundry [5]

Name	TSMC 013 um tech	TSMC 013 um tech	TSMC 013 um tech	TSMC 013 um tech
Technology	Logic	Logic	MS/RF	MS/RF
Geometry	0.13um	0.13um	0.13um	0.13um
Device Application	General Purpose	General Purpose	General Purpose	General Purpose
Core Voltage (V)	1.2	1.2	1.2	1.2
I/O Voltage (V)	2.5	3.3	2.5	3.3
Poly Layers	1	1	1	1
Metal Layers (Min)	3	3	3	3
Metal Layers (Max)	8	8	8	8
RO Speed (ps/gate)	19	19	19	19
BEOL Dielectric	FSG (k=3.6)	FSG (k=3.6)	FSG (k=3.6)	FSG (k=3.6)
BEOL Metal	CU	CU	CU	CU
Well Formation	Retrograde	Retrograde	SSR	SSR
Isolation	STI	STI	STI	STI
Gate Materials	Silicide	Silicide	Silicide	Silicide
Silicide Material	Co-salicide	Co-salicide	Co-Salicide	Co-Salicide
Gate Dielectric tox(core)	20A	20A	20	20
Gate Dielectric tox(I/O)	50A	70A	50	70
Default # of masks	36	36	23 + 12	23 +12
# optional masks	8	8	+/-15 (for 1P8M)	+/-15 (for 1P8M)
Gate density	219 Kgate/mm2	219 Kgate/mm2	219 Kgate/mm2	219 Kgate/mm2
MPW run	Y		Y	
Note				

Table C.5: Available CMOS technologies in the TSMC-foundry [5]

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