Design of a Multisensing Control System

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ABSTRACT

The goal of this paper is to design a reconfigurable multisensing control system. The implemented design tools are based on static random access memory field programmable grid array (SRAM FPGA) circuit board and a very high speed integrated circuit hardware description language (VHDL). The design steps start with software development which consists of HDL processes where V HDL program that describes the architectural behavior of the multisensing control system. An HDL synthesis is the second step, which converts the design in behavioral description file into gates. These steps are followed by implementation techniques and downloading the design from PC

onto FPGA via a joint test action group (J TAG) cable. Different type of sensors; namely two ultrasonic, smoke detector, water level switch, thermostat, and light detector are connected to the inputs of the programmed FPGA and activated to test the design. The results show that the overall average delay timing between inputs to outputs is equal to 6.437 ns which is relatively small as compared with delay time at sensors and 1/0 modules. Therefore, it can be clearly stated that the speed of control is limited by sensors and 1/0 modules rather than the processing performance of the proposed design. This is a stark contrast to traditional control system where the processing performance is typically the limiting factor. Thus the use of FPGA and V HDL to deploy multi sensing control system efficiently improves its reliability, flexibility, and real time data processing. Finally, it can be concluded that the proposed multisensing control system can be effectively implemented in so many application areas including building security, home automation, robot activities, airports and industry control systems.

Keywords: FPGA , Sensor, V HDL

1- **INTRODUCTION**

Multisensing control systems have great applications nowadays in buildings, home, industry and robot. There are

different design choices in implementing multisensing control systems such as application-specific integrated circuits (ASICs) based systems, processor or dedicated digital signal processors (DSPs) based systems, and personal computer (PC) based systems. ASICs based system engineers create fixed hardware design. Once a design has been programmed onto ASICs, it cannot be changed. In addition, if an error exists in the hardware design and not discovered, it cannot be corrected without a very costly product recall (shonil, 2006). Dedicated digital signal processors are class of hardware devices that fall somewhere between ASICs and PC in terms of performance and design complexity (shonil,2006). However, algorithm designed for a DSPs cannot be highly parallel without multiple DSPs, 1/0 modules have fixed functionalities, performance slows as applications grow and operating system runs control (NI,2007). But in order to develop hardware multisensing control system that offers reconfigurability and greater speed of control process, one must use a hardware design language such as V HDL and field programmable gate array. FPGA and V HDL based control systems offer parallel executions, multi rate controls, no slow down as applications grow, 1/0 functionality is reconfigurable,

control logic is dedicated hardware, and does not have an operating system which gives the highest level of reliability (NI, 2007). In particular this research has developed a reconfigurable multisensing control system based on FPGA so as to manage and improve the process performance of a control system that deals with multiple inputs sensors and outputs. In addition, the proposed multisensing control system allows reconfiguration after the control system is deployed.

2- DESIGN TOOLS

The basic design idea of a multisensing control system is to develop a system that lets the user defines the control strategy. In this research the control action required can be generated individually according to each sensor ouput (logic 1), or it can be reconfigured to operate in combinational manner, i.e. more than one senor must have logic 1 at their outputs to generate the required control actions. The design tools composed of FPGA/SRAM circuit board type, which can be programmed as Often as needed, and V HDL programming language, a dedicated language for hardware design.

2-1 Field Programmable Grid Array (FPGA)

A Field Programmable Grid Array (FPGA) is a regular structure logic cells (or modules) and interconnected, which is under complete control. This means that you can design, program, and make changes to your circuit whenever you wish. In the SRAM logic cells, a look up table (LUT) determines the output based on the values of the input (Xilinx, 2006). Other features of FPGAs are channel base routing, post layout timing, more complex tools, fine grained, fast register pipeling, reconfigurable 1/O functionality, and multi rate control. Fig. I shows FPGA circuit board.

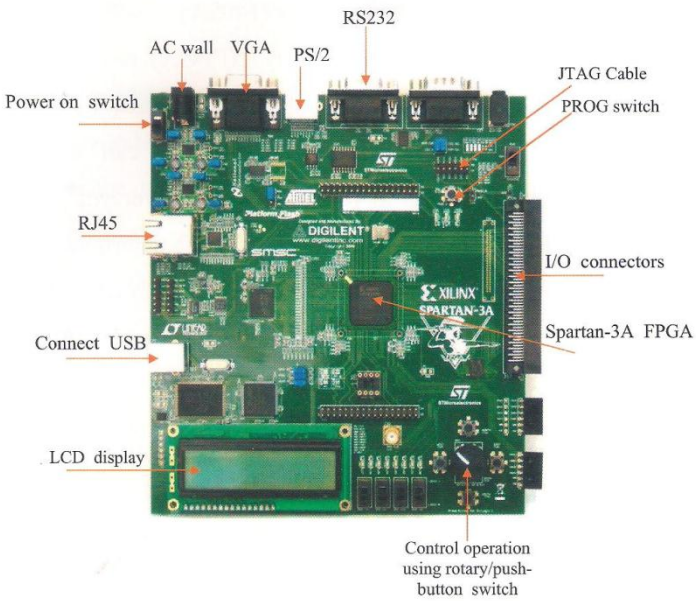

Fig. 1 FPGA circuit board (Xilinx, 2007)

2-2 VHSIC Hardware Descriptive Language

Very high speed integrated circuit (VHDL) hardware description language is a powerful and versatile language, which offers numerous advantages:

2-2-1 Design methodology: VHDL supports many different design methodologies (top-down, bottom-up, delay of detail) and is very flexible in its approach to describing hardware.

2-2-2 Technology independence: VHDL is independent of any specific technology or process. Where its code can be written and then targeted for many different technologies(cedcc,2008).

2-2-3 Wide range of descriptions: VHDL can model hardware at various levels of design abstraction. It can describe hardware from the standpoint of a "black box" to the gate level. Also allows for different abstraction-level descriptions of the same components and allows the designer to mix behavioral descriptions with gate level descriptions.

2-2-4 Standard language: the use of a standard language allows for easier documentation and the ability to run the same code in a variety of environments. Additionally, communication among designers and among design tools is enhanced by a standard language(cedcc,2008).

2-2-5 Design management: use of VHDL constructs, such as packages and libraries, allows common elements to be shared among members of a design group.

2-2-6 Flexible design: VHDL can be used to model digital hardware as well as many other types of systems, including analog devices (cedcc,2008).

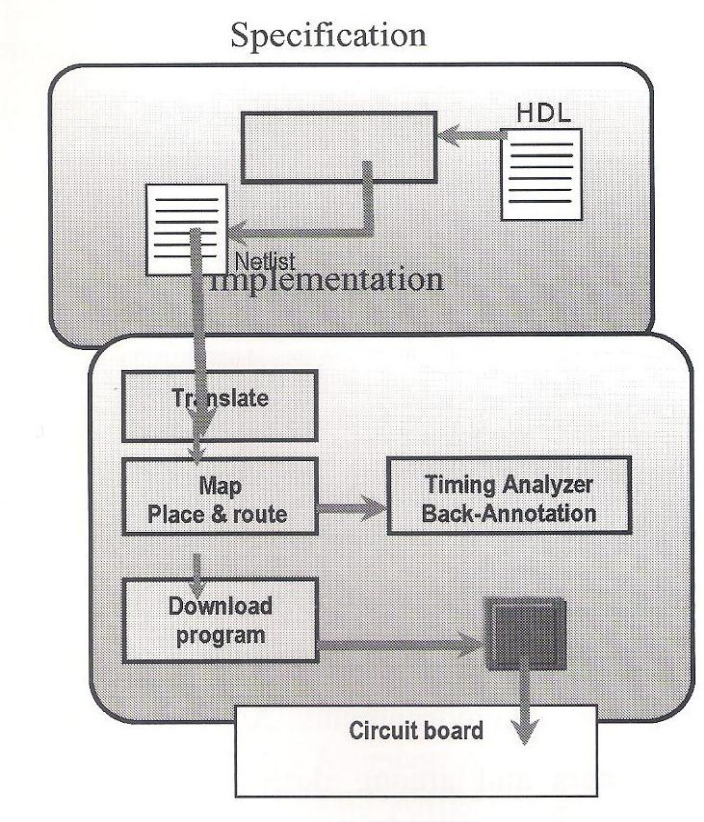

Fig.2 Software design flow diagram(Xilinx,2006)

3- SOFTWARE DEVELOPMENT

The software design flow diagram is shown in Fig.2. There are two methods of design, schematic capture method and HDL

design process which is used as a design method for this work. The design initially targeted at the FPGA is on the board.

3-1 HDL Design Process

A VHDL program that describes the function or behavior of the multisensing control system circuit in a text file rather than a graphical low-level description. HDL design process start by design entry section which consists of creating new project, specifying HDL as a top level source, selecting the type of FPGA (for this project SPARTAN-3A), and declaring ports by names and directions(inputs, outputs).

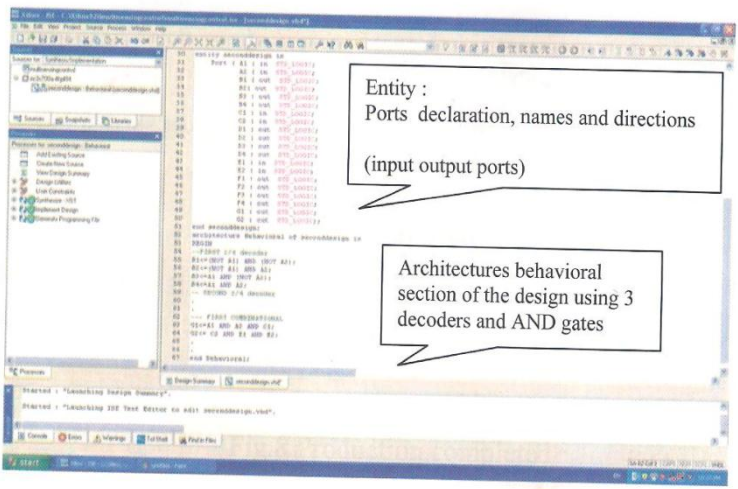

Fig. 3 Multisensing and control editing window

At the end of the previous pro-cess the source code window will automatically open as shown in Fig. 3, where the HDL editor can be used to add architectures behavioral of the design. The developed architectures behavioral module composed of three 2/4 decoders which give 6 inputs and 12 outputs, and two 3 inputs AND gates.

3-2 HDL Synthesis

HDL synthesis is the next step in the design, which converts the design in behavioral description file into gates. The Synthesis tools figure out what gates to use based on a V HDL program file. After synthesis the netlist has been generated. The resulting netlist is a vendor and device family specific as described by FPGA. The synthesis output results also include synthesis reports, syntax check, and technology schematic as shown in Fig.4

3-3 Design Implementation

The implementation mainly consist of translating, mapping, and downloading the program .

Translate:

It comprises the program that is used to import the design netlist and prepare it for layout. In addition translate process generates a comprehensive report which includes 1/O utilization

(Xilinx, 2006)

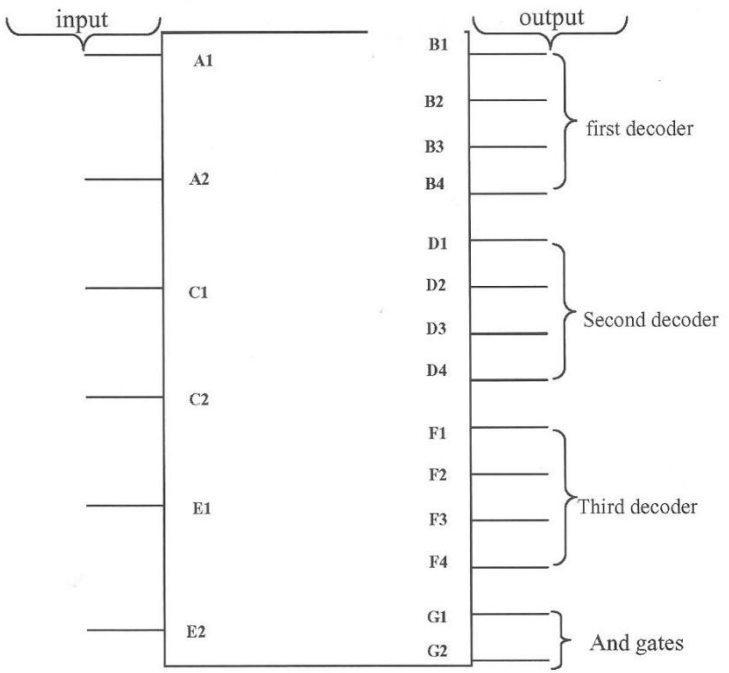

Fig.4 technology schematic

Map

It describes exactly where each portion of the design is located in the actual device. The resulting post-map static timing report is generated as a detailed description report of on-chip logic and interconnection.

Place and Route:

In this step the pin locations for 1/0 ports of the design has been specified on FPGA by using pin number, signal name, pin name, pin usage, and direction. Then a design data sheet has been generated with accurate delay timing report between inputs and outputs.

When place and route, translate, and map processes are compiled correctly a design summary report has been generated as shown in Table 1.

Download the Design to the FPGA:

This is the last step in the design verification process. In this step the FPGA circuit board jumpers has been selected for SRAM programming. Then the FPGA has been programmed by downloading the design program to the FPGA via a J TAG cable connected to a PC parallel port. When the programming completed, a program succeeded message has been displayed.

Table 1: Detailed reports

Detailed Reports					
Report Name	Status	Generated 10:21:26 2008	Errors	Warnings	Infos
Synthesis Report	Current	Tue May 13 10:21:51 2008	0	0	0
Translation Report	Current	Tue May 13 10:22:21 2008	0	0	0
Map Report	Current	Tue May 13 10:22:53 2008	0	0	0
Place and Route Report	Current	Tue May 13 10:21:26 2008	0	0	I Info
Static Timing Report	Current	Tue May 13 10:23:11 2008	0	0	3 Infos

4- Hardware Components and Connectivity

Six different types of sensors are used to test the multisensing control system design. The sensors include two ultrasonic, smoke detector, water level switch, thermostat, and light detector. These sensors have been selected because, of their DC output voltage, frequently use, and availability in the local market. The following sections describe these sensors; note that the design can be tested by any other sensors.

4-1 Ultrasonic Sensor

Ultrasonic sensors generate high frequency sound waves and evaluate the echo which is received back by sensors. Sensors

calculate the time interval between sending the signal and receiving the echo to determine the distance to an object (Sinclair,2001). VM125 ultrasonic radar module is used with the following specifications: range 20-250 cm; digital output voltage 5Vdc(5mA max); input voltage12 Vdc; response time is around 5ms.

4-2 Smoke detector

Smoke sensor from system sensor model 215 IE photoelectric smoke detector uses state-of-art optical sensing chamber (Wikipedia,2007).Smoke detector Model 2151 E is used with the following specifications: output voltage 1.2Vdc; standby current 35pA•, operating temperature 100 - 600 C; response time is around 100ms.

4-3 Float level switch

The measurement sensing the level of a liquid in a container of uniform cross-section is therefore a useful quantity that is proportional to the volume of the liquid(Sinclair,2001). A float switch is a great way to automatically turn any appliance such as a pump, on or off. A ball inside the tethered float switch simply changes position from top to bottom with the rising or falling motion it changes the floats angle, thus breaking or establishing the electrical circuit to turn the pump on or off as water rises, at a

predetermined level the switch turns on the pump once the level has been reduced to the setting level(Libaba,2008). The float level switch used has the following specifications: max. rated voltage 250 V DC or AC; response time around 100ms.

4-4 Thermostat

Thermostat is a wide temperature sensor used in controlling or regulating temperature. This research uses an air conditioner thermostat that can be adjusted manually to regulate room temperature. It has the following specifications: temperature range 0 - 35 0 C; response time around 200 ms.

4-5 Photoconductive sensor LDR (light depended resistor)

The photoconductive sensor is by far the most common type of photoconductive sensor used industrially. It is mechanically and electrically rugged, and has a good record of reliability (Sinclair, 2001). An ORP12 LDR has peak response at the yellow-orange region of spectrum makes this LDR particularly useful for detecting the presence of the flame(Sinclair,2001). This section highlights the specifications of OPR12 used: peak spectral response 610 nm; max. voltage (DC or Peak AC) 100 V; max. Dissipation at 50 C; response time is around 350 mse

Fig.5 shows the hardware connectivity of a multisensing control system. The sensors outputs signals (DC voltage) are connected via signal conditioning circuits (potential divider) to the inputs of the programmed FPGA according to the pin locations of 1/0 ports specified after place and route step in the design implementation process. SNA 74373 8-bit 3-state transparent latch is used at the input of FPGA for protection purposes. ULN 2003 Darlington amplifier (max 50 Vdc output) is used to amplify the 125 Vdc FPGA outputs. The outputs of Darlington amplifier has been connected to different indicators from local market such as light emitting diodes, commercial buzzers, commercial lamps and DC motors to demonstrate the output results.

FPGA

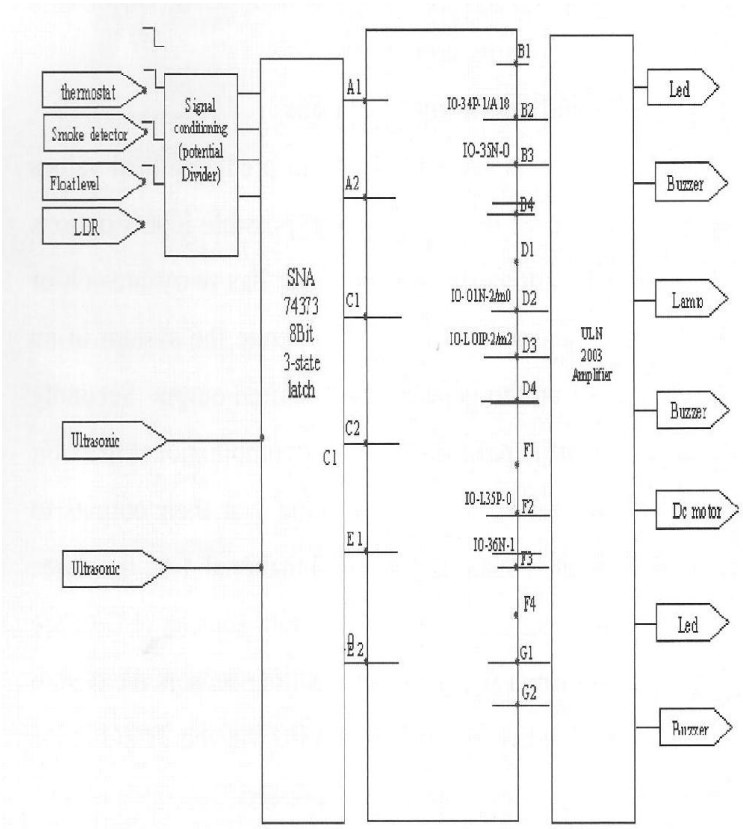

Fig.5: I/O devices connectivity

5- EXPERIMENTAL RESULTS

All preparation for the implementation of this experiment conducted under laboratory conditions.

5-1 Setting and operating conditions

The sensors are adjusted manually to predetermined values and activated as shown in Table (2). The possible inputs options equal to 26 combinations since each sensor has two states on or off Firstly each sensor is activated to operate the system in an individual manner and to generate the required output. Secondly the system is reconfigured to operate in a combinational manner; each two or three sensors must have logic 1 at their outputs to generate the required action. For combinational test the three sensors thermostat, smoke detector and light sensors (LDR) are configured to confirm a fire. Before activating sensors the design has been downloaded onto FPGA from PC via the JTAG cable and the PROG switch has been pressed to operate the multisensing control system. An oscilloscope is used to measure the total delay time between inputs to outputs.

Table 2: Setting values and activation sources

Sensor	Predetermined Setting Values	Source of Activation
Temperature sensor (thermostat)	25 0c (room temperature)	Electric heater Im far from the thermostat
Float level Switch	(container dimensions) 20 cm height 25 cm width 35 cm length	Reducing the water level gradually from the container to be lower than 20 cm height
Smoke detector	1.5 m height	Burning pieces of wood inside censer I .5 m below the smoke detector
Ultrasonic	30 cm	Moving object at 30 cm far from the ultrasonic sensor.
Light sensor (LDR)	Im height	Burning pieces of papers Im below the LDR

5-2 Individual setting results

Table 3 shows the delay timing numbers of multisensing control system for each sensor where,

Tamp: Darligton amplifier duty cycle from the data sheet

Tio : Delay time between input to output of FPGA (process performance) from the data sheet generated after place and route during the design implementation step.

Ts: Sensor response time.

Table 3: Calculated and measured delays for each sensor

Sensor Name	Tio (ns)	Ts (ms)	Tamp µs	Calculated Total delay timing (ms)	Measured Total delay Timing(ms)
Thermostat	6.386	200	100	200.1006386	210
Light sensor (LDR)	6.399	350	”	350.1006399	365
Smoke detector	6.409	100	”	100.1006409	105
Float level switch	6.416	100	”	100.1006416	105
Ultrasonic	6.490	5	”	5.1006490	8
Ultrasonic	6.523	5	”	5.1006523	8

Note: total delay (calculated) Ts+ Tio + Tamp

From the above table the overall average delay (Tio) between inputs and outputs of the design (programmed FPGA) is equal to 6.437 ns, which can be neglected in comparison with sensor response time (Ts) and Darlington amplifier time (Tamp). This means that the total delay is almost equal to the sensor response time plus the amplification time.

5-3 Combined setting results

The design is reconfigured for combinational test as shown in table 4 to confirm fire; thermostat, LDR, and smoke detector must have output of logicL The average delay time (Tio) is 6.532 ns. The total delay measured approximately equals to 366 ms which is; approximately equal to the largest sensor response time (LDR) among the three sensors used.

Table 4: Combined setting results

Sensor Name	Ts (ms)	Tio (ns)	Tamp µs	Measured total delay timing (ms)
Thermstat	200	6.686	100	366
Light sensor (LDR)	350	6.305	100	
Smoke detector	100	6.605	100	
Average	216.667	6.532	100	
Max	350	6.686	100	

For both individually and combinational sensors setting the results show that the process performance and the speed of the control loop rate of multi sensing and control system is limited only by sensors and 1/0 modules.

For real applications and in comparison with the experimental results of multisensing control system the delay timing number also affected by the following:

Sensor location which is the main factor in the time needed to activate the sensor (sensor response time).

The distance between the multisensing control system and the sensor increases the propagation delay slightly which can be neglected. Hence, the most important requirements for real application is sensor location plus sensor type and characteristics, and geometry of application area.

6- CONCLUSION

The main objective of this paper is to demonstrate the design of multisensing and control system that can be characterized by reconfigurability, fast, multi rate control, flexible, and reliable which does not exist in traditional systems. These characteristics are derived from the advantages and benefits of design tools used, V HDL programming language as a software design tool and FPGA SRAM technology as a hardware tool. The results show the average delay time of the design, i.e the time spent from inputs to outputs of the programmed FPGA is equal 6.437 ns and 6.532 ns for individual and combined setting, respectively. This means that, the multisensing control system speed is only limited by the sensors and 1/0 modules. This is a stark contrast to traditional control system where the processing performance is typically the limiting factor. The designed multisensing control system is suitable for implementation in buildings security, home automation, airports management, robot, and factory control.

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