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Creation of principles for the implementation of operating systems for high-precision fire equipment

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ABSTRACT

The use of fire extinguishing software is based on the principles of system analysis, when any software is created for specific tasks or adapted to use on existing equipment samples. Therewith, a considerable part of the software cannot be implemented in conditions when the operation of technical means is autonomous or specialised. This includes devices of increased accuracy with the requirement to receive a response with a minimum delay. The originality of the study is conditioned by the fact that the principles of creating software for situations with minimal response require its consolidation with equipment that works on the principles of microcode. Based on the analysis of the current state of analogue-to-digital and functional conversion methods, it is shown that a promising area of research and improvement is the creation of converters on switched capacitors that combine the functions of ATFC, and also have an increased number of input values with high accuracy and speed. The methodological basis for creating new methods for constructing ATFC is a combination of structural and algorithmic principles for improving the accuracy of analogue-to-digital conversion based on the properties of capacitor cells. The practical significance of the study is determined by the possibilities of using hardware microcode as modules for the main software set.

Keywords: Fire hazard, Reference voltage, Instrument manufacture, Tactile pulse, Microcode

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1. Introduction

The methodological foundations for building an automated fire safety system (ATFC) on switched capacitors combine structural ones – by changing the logarithm base and the ratio of capacitances, and algorithmic ones – by choosing the number of conversion sub-bands, the number and magnitude of steps on each of them [1]. In particular, some studies propose to use a pre-calculated series of values of the bases of logarithms that directly determine the conversion error, and obtained from the ratio of capacitances of cell capacitors [2]. The basis of the logarithm affects the conversion error by setting the value of the step of forming the logarithmic characteristic. The choice of the number of steps will determine the performance [3]. The properties of capacitor cells during the redistribution and accumulation of charge allow building logarithmic characteristics in steps from top to bottom and from bottom to top, which contributes to the optimisation of the transformation in time [4]. The choice of the number of conversion steps, the step size, and the separation of the entire conversion range form an algorithmic part of the methodology for improving accuracy and speed [5]. It is possible to find the optimal ratio between the error value and the conversion time by dividing the entire conversion range into several sub-ranges and setting a different logarithm basis and step value for each of them [6]. It is possible to reach the set value of the input value as quickly as possible and refine it until the desired accuracy is achieved [7; 8].

The advantage of this approach is the ability to select the desired metrological characteristics even before the conversion begins [9;10]. And the methods and principles of construction proposed within the framework of the developed methodology and the schematic implementation of the ATFC ensure that the actual values of errors and conversion time obtained will be less than those originally set [11]. The new structures on capacitor cells will work according to algorithms with the refinement of the desired metrological characteristics during the conversion process [12-14]. The basis and mechanism of refinement is precisely the possibility of choosing the basis of taking the logarithm, which directly affects the conversion step and the conversion error [15].

The introduction of blocks of various capacities and control-switching blocks into the converter structures allows choosing a sub-range of conversion [16; 17]. The calculated series of relationships between the base of the logarithm and the capacitances of capacitor cells simplifies the manufacture of tank blocks [18-20]. The manufacture of several capacitors is more technologically advanced and simple than the manufacture of a resistor [21]. The capacitor manufacturing technology also allows producing cells with the most similar capacitance parameters, which reduces the errors of non-identity of cells and contributes to increasing the number of input values, both by increasing the number of corresponding cells, and by certain algorithmic and circuit improvements [22; 23].

The proposed methodological principles open up new opportunities for increasing the number of input values without loss of accuracy, improving accuracy and speed, and for selecting the necessary metrological characteristics of ATFC for specific tasks of automation, information and measurement technology [24; 25].

2. Materials and methods

For the construction of a multifunctional and multi-input converter, the study suggests a new method of analogue-to-digital conversion [26]. It indicates the input voltages $U_{IN1}, U_{IN2}, \ldots, U_{Inn}$, the reference voltage U_0, the compensating voltage U_k and the number of dosages – conversion steps n_k. During the conversion, the compensating voltage U_k changes from the initial level of the reference voltage U_0 and is compared with the input voltages $U_{IN1}, U_{IN2}, \ldots, U_{Inn}$ – the conversion takes place until all comparators that fix the equality of the compensating and each of the input voltages are triggered [27].

A more detailed essence of the proposed method of analogue-to-digital functional conversion is as follows. During the development of a dosed amount of electricity in a capacitor cell, its output signal is supplied to the combined inputs of all logarithmators divided into two groups [28]. At the same time, that is, synchronously, elements (pulses) of their original pulse-number codes are formed at the outputs of all logarithmators. Therefore, by connecting alternately in this time interval the output of each logarithmator of the first and second groups, respectively, to the input of addition and subtraction of the reverse counter, at the output of this counter, an algebraic sum of the elements of the output pulse-number codes of the logarithmators is obtained [29; 30].

At the end of the conversion, the last logarithmator (it will be a logarithmator, to the input of which the smallest of all input signals will be brought) will record the algebraic sum of the original number-pulse codes of logarithmators at the output of the reverse counter. This sum is converted by a digital anti-logarithmator into the source code of the proposed functional converter [31]. Thus, the algebraic addition of the original number-pulse codes of logarithmators occurs element by element in parallel and thereby significantly increases the speed of the functional converter [32].

The functional conversion of input signals is carried out using the following components: CB – control block, RVS – reference voltage source, LB – logarithmator block, Com1 and Com1 – the first and second commutators, RC – reverse counter, AL – anti-logarithmator. The control block (CB) contains: OV – monovibrator, G1 and G2 – the first and second generators, PT – a generator of pulse sequences Q1 and Q2, ZX – coincident-current element, OR – logical addition element, T – counter trigger. The logarithmator block LB contains: "input IE" – a group of information inputs, CGr – a group of comparators, GER – a group of matching elements, KK – capacitor cell, which includes C1 and C2 – the first and second capacitors, K1-K3 – analogue keys.

The control block CB has direct and inverse outputs, the triggers T are connected respectively to the combined V-inputs of the first and second counters L1 and L2; the first and second comutators Com1 and Com2, and the output of the matching element ZX is connected to the combined clock inputs of the counters L1 and L2, the

transfer outputs of which are connected respectively to the first and second inputs of the element OR; the output of the first generator G1 is connected to the clock C-input of the pulse sequence generator RVS, the first output of which is connected to the first input of the coincident element ZX, the second input of which is connected to the output of the second generator G2. The start input IE is combined with the input of the monovibrator OV, the output of which is connected to the input of the installation S of trigger T and the combined reset inputs R of the counters L1, L2, and L3, the anti-logarithmator AL and the generator of pulse sequence IE. In the LB block, the outputs of the logarithmators are connected in accordance with the information inputs of the first Com1 and second Com1 switches, the control inputs of which are connected in accordance with the outputs of the first L1 and second L2 counters, and the outputs of the switches are connected in accordance with the addition and subtraction inputs of the reversible counter LR, the output of which is connected to the information input of the anti-logarithmator AL, the output of which is the output of a functional converter (IE), a group of information inputs of which is combined with the corresponding information inputs of logarithmators.

In addition, for the block of logarithmators LB, the first inputs CGr are information inputs of the logarithmators, the outputs of which are connected to the corresponding first inputs of the group of matching elements GER, the outputs of which are the outputs of the logarithmators, and the analogue IREG input of the capacitor cell KK is the information input of the first key K1, the output of which is combined with the information input of the second key K2 and through the first capacitor C1 is connected to the common bus. The clock C-input of the KK cell is the control input of the second key K2, the output of which is combined with the information input of the third key K3 and through the second capacitor C2 is connected to the common bus. The input start V and reset R of the KK cell are respectively the control inputs of the first K1 and the third K3 keys, the clock C-input and the reset input R of the KK cell are connected to the corresponding outputs of the pulse sequence generator RVS. The V input of the KK cell is combined with the output of the monovibrator OV, analogue IREG – KK cell input is connected to the output of the reference voltage source RVS, the second inputs of the comparators are combined with the output of the MC cell, the clock C-input of which is combined with the second inputs of the group of matching elements GER.

3. Results and discussion

The proposed method of analogue-to-digital functional conversion is implemented using the following scheme. The pulse applied to the IE start input starts the monovibrator OV. The output pulse of the monovibrator OV resets the outputs of the pulse sequence generator RVS, counters L1, L2, RC and the anti-logarithmator AL to zero, sets the trigger T to the state of the logical unit at the direct output and closes the first key K1 of the capacitor cell KK. During the action of the pulse of the monovibrator OV, the first capacitor C1 of the KK cell is charged to the level of the reference voltage (Uref) of the RVS source and the level of the logical unit is set at the outputs of the comparators of the CGr group, which allows the passage of pulses from the output Q2 of the pulse sequence generator PT through the group of matching elements GER (to increase accuracy, the pulse sequences Q1 and Q2 are separated by pauses). At the end of the pulse of the monovibrator OV with each pulse of the first generator G1 at the outputs of the RVS shaper alternately (first at the output Q1, and then at Q2) impulses appear.

First, the study considers the process of logarithmation of input signals. The pulses Q1 of the RVS shaper close the third key K3 of the capacitor cell KK, dropping the charge from the second capacitor C2 to the common bus, and the voltage level is set to zero on the capacitor C2. The pulses Q2 of the RVS shaper close the second key K2 of the capacitor cell KK, through which the charge is redistributed between the capacitors C1 and C2. With each pulse Q2, the first capacitor C1 gives part of its charge (since the capacity of the first capacitor C1 is chosen much larger than the second capacitor C2, that is, C1>C2) to the second capacitor C2 and the voltage level on the first capacitor C1 decreases.

After the n-th pulse Q2 of the RVS shaper, the voltage on the first capacitor C1 will become equal:

$$U_n = \zeta^n U_{ref}, \quad (1)$$

where,

$$\zeta = \frac{C_H}{C_D + C_H}, \quad (2)$$

If in the process of reducing the voltage on the first capacitor C1, it will become equal to or less than, for example, the voltage (U_{BX_i}) at the i-information group entry information inputs "Login" IE Converter (and therefore at the first entrance of the i-th comparator group CGr), then it triggered the i-th comparator group CGr (at the output level appears logical zero), fixing the date of completion of the conversion of the i-th logarithmator. If this moment came after n -th tactile impulse, then:

$$U_n = U_{BX_i}, \tag{3}$$

and the number (ni) of pulses Q2 of the PT shaper received at the control input of the second key K2 will be:

$$n_i = \frac{1}{l_n \zeta} ln \frac{U_{BX_i}}{U_{ref}} \tag{4}$$

that is, the logarithm of the voltage ratio U_{BX_i} to U_{ref}.

This number of pulses enters through the i-th matching element of the group of matching elements of the GEZ to the output of the latter (that is, to the output of the i-th logarithmator) and represents the output number-pulse code of the i-th logarithmator. After the conversion is completed by the i-th logarithmator, a logical zero from the output of the i-th comparator is brought to the first input of the i-th element of the match of the group of matching elements GE3, prohibiting the further passage of the Q2 pulses of the shaper to the output of the i-th logarithmator.

Similarly, the conversion occurs in other logarithmators, since the process of lowering the voltage on the first capacitor C1 of the capacitor cell KK continues until the last of the comparators of the CGr group works, that is, until the conversion in the last logarithmator ends (this logarithmator will be the one to the first input of the comparator of which the smallest of all input signals will be brought). With each pulse Q2 of the shaper, the pulses of the second generator G2 are allowed to pass through the matching element ZX to the clock inputs of the counters L1 and L2, the source codes of which alternately connect the outputs of the logarithmators through the switches Com1 and Com1 in accordance with the addition and subtraction inputs of the reverse counter RC. At the end of the conversion, the code will be written in the last logarithmator at the output of the RC reverse counter:

$$N_c = \frac{1}{ln\zeta}\left(\sum_{d=1}^{m} ln \frac{U_{ld}}{U_{ref}} - \sum_{k=1}^{p} ln \frac{U_{lk}}{U_{ref}}\right), \tag{5}$$

where *d* – the number of logarithmators of the first group connected to the inputs of adding the reverse counter RC, and varies from 1 to m; *k* – the number of logarithmators of the second group connected to the inputs of subtracting the reverse counter RC, and varies from 1 to p. The source code Nc of the RC reverse counter is fed to the input of the digital anti-logarithmator AL, at the output of which the result of the functional transformation is generated:

$$N_{fp} = anti \ln N_c, \tag{6}$$

Since the pulses at the outputs of all the logarithmators performing the conversion appear simultaneously, then alternately connecting the RVS shaper of the output of each logarithmator to the corresponding input of the RC reversing counter allows the logarithmors to be converted in time:

1) to obtain the algebraic sum of the logarithmator source codes and implement multiplication and division operations;

2) to obtain the sum of the source codes of logarithmators, on m shortened inputs of the first group of which the input signal is given, and to provide the implementation of a power function with an exponent m, that is;

3) to obtain the difference of the source codes of logarithmators, on the short-circuited inputs of the second group of which an input signal U_{BX} is supplied, and to ensure the implementation of the root with the exponent, i.e., $\sqrt[p]{U_{BX}}$.

All this significantly reduces the time of analogue-to-digital functional conversion, that is, significantly increases the speed. Many measurement tasks require converting the difference between two voltages. The conventional approach involves the precise determination of the difference and further logarithmation for analogue-to-digital conversion. However, this method accumulates conversion errors. In order to increase the accuracy, the study considers a method for taking the logarithm of difference between two voltages. It is necessary to designate two input voltages: $U_{IN1}(U_1)$ – corresponds to a larger input voltage, that is,

descending, $U_{IN2}(U_2)$ – corresponds to a smaller input voltage, that is, ascending, U_0 – reference voltage and two compensating voltages U_{k1} and U_{k2}, n_k – the number of dosages-conversion steps. During the conversion, two compensating voltages are formed simultaneously: U_{k2} by redistributing the charge in the form of a descending open, by accumulating the charge in the form of a growing open. The process occurs until the equality of the first input and the first compensating voltage and the equality of the second input and the second compensating voltage.

Next, the study took a closer look at the process of taking the logarithm of difference between two voltages. The essence of the method of the logarithmic analogue-to-digital conversion of the difference of two input voltages U_1 and U_2 is to convert the difference $U_1 - U_2$ into a product of two multipliers $U_1\left(1-\frac{U_2}{U_2}\right)$ and the determination result as the sum of the logarithms of these multipliers. Next, the logarithm of the first multiplier is determined as the logarithm of the ratio $\frac{U_1}{U_o}$, where U_o – value of the reference voltage, which is set equal to or greater than the nominal value of the input voltage U_1, and the logarithm of the second multiplier $\left(1-\frac{U_2}{U_2}\right)$ is determined by the method of balancing, which form of compensation voltage U_k by changing the charge on the storage capacitor recurrent metered amounts of electricity to transfer the compensation voltage U_k through the input voltage U_2 and determines the result of the logarithm of the second multiplier, the number of doses, and a metered amount of electricity form the charge metering capacitor to the level of the input voltage U_1, and the capacity of the metering capacitor set according to the equation:

$$C_d = \frac{1-\zeta}{\zeta} C_H, \tag{7}$$

where C_H – capacity of the storage capacitor, ζ – dosing coefficient, which is set to less than one.

The logarithm of the difference between the two input voltages is determined using a simplified functional circuit that contains a control unit (CD), two logarithmic analogue-to-digital converters (LACP1 and LACP2), a logic element OR and a pulse counter (IC), each of the LACPS contains a storage CN and metering capacitors CD, three analogue keys (KI, K2, K3), a comparator (KM) and a matching element (ZX), an output LACP3 (Out1) and an output LACP2 (Out2). The proposed method of logarithmic analogue-to-digital conversion of the difference of two voltages is implemented using the circuit as follows. With the "Start" pulse, the control unit resets the counter L0 to zero, the keys K1 of the LACP1, LACP2 converters are closed, and the accumulator capacitor CN of the LACP3 converter is charged to the reference voltage level U_o, and the capacitor CN of the LACP2 converter is discharged to zero.

During the operation of the "Start" pulse, the logical zero level is set at the direct outputs of the control unit N_1 and N_1, and the logical unit level is set at the inverse unit $\overline{N_1}$ and $\overline{N_2}$, as a result of which the keys K2 of the LACP1, LACP2 converters are closed and the dosing capacitor CD of the LACP1 converter is discharged to zero, and the dosing capacitor CD of the LACP2 converter is charged to the voltage level U_1. At the end of the "Start" pulse, the conversion process begins.

In the LACP1 converter, with each clock pulse of the sequence N_1, the short circuit key is closed and the accumulating capacitor CN gives part of its charge to the metering capacitor CD and the voltage level on it Uk decreases. In the pause between the pulses N_1, the control unit generates sequence pulses $\overline{N_1}$, which close the key K2 and the metering capacitor CD is discharged to zero. The clock pulses of the sequence N_2 pass through the matching element ZX, which is opened by a logical unit from the Km comparator, to the output of the converter LACP1 (Out1). When the voltage level U_k on the accumulating capacitor CN reaches the input

signal level, their comparator Km enters the state of logical zero, which prohibits the further passage of the sequence clock pulses N_1 through the matching element ZX to the output of the converter LACP3 (Out1). The number of sequence pulses N_{vix1} that passed through the matching element ZX from the moment of the end of the "Start" pulse to the transition of the Km comparator to the logical zero state is the initial numerical pulse code of the LACP3 converter. The value of this code is (Eq. 8):

$$N_{vix1} = \frac{1}{log\zeta} log \frac{U_2}{U_0}, \tag{8}$$

that is, the logarithm of the voltage ratio U_1 to U_o. Where:

$$\zeta = \frac{C_N}{C_D + C_N}, \tag{9}$$

In the LACP2 converter, the conversion occurs as follows. During the action of the clock pulse of the sequence N_2, the K3 key closes (and the K2 key opens). When the key K3 is closed, the charge is redistributed between the capacitors, that is, the metering capacitor C_D gives part of its charge to the accumulating capacitor C_N. In the pause between clock pulses (the action of sequence pulses $\overline{N_2}$), the key K3 opens, and the key K2 closes. Thus, the metering capacitor C_D is charged to the voltage level U_1, and the storage capacitor C_N keeps the voltage level on it unchanged. Initially, the metering capacitor C_D had a charge:

$$Q_0 = C_D U_1, \tag{10}$$

During the action of the first tactile pulse N_2, the voltage on the accumulating capacitor (u_{CN1}) becomes equal to:

$$U_{CN1}(C_D + C_n) = C_D U_1, \tag{11}$$

$$U_{CN1} = U_1 K, \tag{12}$$

and its increase will be:

$$U_{CN1} = U_1 K, \tag{13}$$

where:

$$K = \frac{C_D}{C_D + C_N}, \tag{14}$$

In the pause between the first and second tactile pulses N_2, the metering capacitor C_D will be charged again through the pulse-closed $\overline{N_2}$ key K2 to the voltage level U_1. During the action of the second tactile pulse N_2 , the charge of the capacitors will be affected not only by the voltage U_1, but also by the voltage U_{Cn1} remaining on the accumulating capacitor C_N after the action of the first tactile pulse. Therefore, using the superposition principle, during the action of the second tactile pulse N_2, the accumulating capacitor C_N will be charged to the voltage U_{CN2}:

$$\mathrm{U_{CN2}} = (\mathrm{C_D} + \mathrm{C_N}) = \mathrm{C_D U_1} + \mathrm{U_{CN1} C_N} = [1 + \mathrm{C_N}]\mathrm{KU_1};\ \mathrm{U_{CN2}} = [1 + \zeta]\mathrm{KU_1}, \tag{15}$$

and the increase in voltage on the accumulating capacitor will amount of:

$$U_{CN2} = U_{CN2} - U_{CN1} = \zeta K U_1, \tag{16}$$

At the end of the second tactile pulse (during the action of the sequence pulse $\overline{N_2}$), the metering capacitor C_D will be charged again through the closed key K2 to the voltage level U_1. During the action of the third tactile pulse N_2, the accumulating capacitor C_N will be charged to the voltage U_{CN3} :

$$\mathrm{U_{CN3}} = (\mathrm{C_D} + \mathrm{C_N}) = \mathrm{C_D U_1} + \mathrm{U_{CN2} C_N} = C_D U_1 + [1 + \zeta]\mathrm{KU_1} C_N, \tag{17}$$

and the increase in voltage on the capacitor C_N will amount to:

$$\mathrm{U_{CN3}} = KU_1\zeta^2, \tag{18}$$

Similarly, after the expiration of the I-th tactile pulse N_2, the storage capacitor C_N will be charged to the voltage U_{CNi} :

$$\mathrm{U_{CNi}} = [1 + \zeta + \zeta^2 + \cdots + \zeta^{i-l}]KU_1, \tag{19}$$

and the increase in voltage on the capacitor C_N will amount to:

$$U_{CNl} = KU_1\zeta^{i-l}, \tag{20}$$

Thus, the value of the voltage on the accumulating capacitor CN changes according to the law of geometric progression with the denominator $\zeta = 1-K$. Therefore, representing the expression in brackets as the sum n of the terms of the geometric progression according to the well-known equation:

$$S_n = \frac{1-a_1\zeta^n}{1-\zeta}, \tag{21}$$

where a_1 – the first term of the geometric progression, the value of the voltage on the accumulating capacitor C_N is obtained after an arbitrary order of the i-th clock pulse of the sequence N_2 :

$$U_{CNi} = [1 - \zeta^i]U_1, \tag{22}$$

If, after the n-th tactile pulse of the sequence N_2, the voltage on the accumulating capacitor $C_N\left(U_N\right)$ becomes equal to the input voltage U_2, that is $U_N = U_2$, the Km comparator is triggered, switching to the logical zero state. This zero prevents the further passage of clock pulses N_2 through the matching element ZX to the output of the converter LACP2 (Out2). The last equation can be written as:

$$U_2 = [1 - \zeta^N]U_1, \tag{23}$$

$$\zeta^N = \left(1 - \frac{U_2}{U_1}\right), \tag{24}$$

Logarithming the last expression, the value of the original number-pulse code $\left(N_{vix2}\right)$ of the LACP2 converter is obtained, that is, the logarithm of the second multiplier:

$$N_{vix2} = N = \frac{1}{log\zeta} log\left(1 - \frac{U_2}{U_1}\right), \tag{25}$$

Thus, during the conversion time, the element will allow the output numerical pulse codes to be converted from LACP1 to LACP2 and the sum will be recorded in the Lsr counter:

$$N_{vix} = N_{vix1} + N_{vix2} = \frac{1}{log\zeta} log\frac{U_1}{U_0} + \frac{1}{log\zeta}\left(1 - \frac{U_2}{U_1}\right) = \frac{1}{log\zeta} log\frac{U_1}{U_0} + \frac{1}{log\zeta} log\frac{U_{1-U_2}}{U_1} = \frac{1}{log\zeta} log\frac{U_1(U_{1-U_2})}{U_0U_1} = \frac{1}{log\zeta} log\frac{(U_{1-U_2})}{U_0}, \tag{26}$$

or:

$$N_{vix} = N_{vix1} + N_{vix2} = \frac{1}{log\zeta} log\frac{U_1-U_2}{U_0}, \tag{27}$$

that is, the logarithm of the voltage difference $U_1 - U_2$.

For analogue-to-digital conversion, the recurrent algorithm is somewhat different. Recurrent ADCs belong to the class of bit-by-bit encoding. Therefore, they need a number of standards, usually a number of model voltages that are multiples of each other. In a recurrent ADC, the input voltage is alternately compared with each of the reference voltages U_i and the value of the one at which the passage through the level U_{IN} was recorded is stored. The stored value is used as a reference voltage for further conversion. The number of

reference voltages corresponds to the bit depth of the source code N. And taking the logarithm as the basis ζ, it is necessary to ensure the multiplicity of two adjacent standards with a coefficient ζ.

The output code is formed by comparing the input and reference voltages $U_1 - U_N$, and the current values U_i that were less than U_{IN} are discarded and zeros are put in the corresponding digits of the output code. In particular, the voltages will not be taken into account U_1, U_2, as well as U_4, U_6, U_{N-1}. The advantage of recurrent ADCs on switched capacitors is the high manufacturability of manufacturing and the direct dependence of the type of source code on the method of forming the weight coefficients of discharges and reference voltages. However, their speed and accuracy are typical for bit-by-bit encoding ADCs.

A method was proposed that allowed increasing the speed of the logarithmic analogue-to-digital conversion while maintaining high accuracy. A special feature of the proposed improved recurrent ADC is the conversion in two stages. At the first stage, there is a repeated appeal only to the standard of the first category. At the second stage, the input voltage is compared with the standard of each of the subsequent discharges only once. At the first stage of the conversion, the compensating voltage U_1 is compared with the input U_{IN} voltage. The comparison takes place until the transition through the input voltage level is recorded. The result of the first stage of the conversion is to establish the value of the input voltage quickly, but with a relatively greater error. At the second stage, the approximation to the required value occurs each time with a different step. Changing the step allows selecting the desired error and conversion speed. Physically, the step change is carried out by changing the scale factor. Compared to the well-known recurrent ADC method, the improved method requires a significantly smaller number of steps.

Such improvement of the recurrent method allowed substantially reducing the number of standards (approximate values) and considerably increased the conversion speed. Next, the study considered the implementation of the proposed method. The simplified scheme of a logarithmic analogue-to-digital converter, wherein the proposed recurrent method is implemented, contains ASC – adjustable scale converter, EFFU – a block for generating an exponential function, Km – comparator, CG – clock pulse generator, CB – control block, L – result counter, RR – result register, ECcom – a multiplier / switch, EM1 and EM2 – the first and second memory elements. U_0 – reference voltage, U_{BX} – input voltage, F_T – clock frequency, N_1, N_2 – respectively, the highest and lowest digits of the output code, U_{k1} and U_{k2} – compensation voltage at the first and second conversion stages, $K_1 - K_n$ – transmission coefficients of the adjustable scale converter ASC at inputs 1-n; A, D, CiD – control signals. The values of the voltage transfer coefficients (K_i) are preset at the inputs of the adjustable scale amplifier ASC for any i-th input according to the equation:

$$K_i = \zeta^{\frac{N_n}{2^i}}, \tag{28}$$

where N_n – nominal value of the source code; $\zeta = const$, and $\zeta < 1$, its value also depends on the desired accuracy. The coefficient ζ sets the value of discrete increments of the transmission coefficient of the ASC scale amplifier; it can be determined based on the nominal value of the source code NH by the equation:

$$\zeta = e^{N_n^{-1} lnD^{-1}}, \tag{29}$$

where D is the dynamic range of the input signals, equal to the ratio of the maximum value of the input voltage to the minimum.

The operation of the logarithmic analogue-to-digital converter proceeds as follows. The control block CB resets the result counter L and the result register RR with the initial setting signal, records the reference voltage level (U_0). In the first memory element EM1 and generates control signals A and C, which allow the operation of the converter in the first section. Signal A is fed to the control input of the adjustable scale amplifier ASC and turns on the first input of this amplifier, and signal C allows the operation of the result counter L.

In the first section of the conversion, with a logical unit at the output of the Km comparator, the control unit stores the signals A and C, that is, the resolution of the converter operation in the first section is preserved. At the first operation of the Km comparator, that is, the transition of the Km output to logical zero, the CB control block excludes the signals A and C and switches to the converter operation in the second section. The

maximum value of the transmission coefficient of the adjustable scale amplifier ASC will be at the first input, that is, when i=1:

$$K_1 = \zeta^{\frac{N_n}{2}}, \tag{30}$$

After the initial installation, the conversion process begins. At the first stage of the conversion, during the action of the first clock pulse, the voltage at the output of the ASC amplifier takes the value:

$$U_1 = U_0 K_1 = U_0 \zeta^{\frac{N_n}{2}}, \tag{31}$$

This voltage U_1 is recorded in the EM2 memory element and goes to the output of the exponential function generation unit, from which it is fed to the Km comparator and compared with the input signal U_{BX}. When the output voltage of the exponential function generation unit is greater than the input signal, the Km comparator is set to the state of a logical unit at its output, and otherwise – a logical zero. The first clock pulse is recorded in the counter L.

The second clock pulse connects the output voltage EM2 to the first input of the adjustable scale amplifier ASC, and the first memory element EM1 – to the output of the amplifier ASC, the voltage on which takes the value:

$$U_2 = U_1 \zeta^{\frac{N_n}{2}} = U_0 \zeta^{2\frac{N_n}{2}}, \tag{32}$$

The voltage U_2 exceeds the input signal level, and the comparator retains the level of the logical unit at the output. Since the state of the Km comparator has not changed, the action of the second clock pulse is similar to the action of the first, that is, the second pulse is recorded in the result counter L.

The third clock pulse connects the first memory element EM1 to the input of the adjustable scale amplifier ASC, and the second memory element EM2 to the output of the amplifier ASC, the voltage on which takes the value:

$$U_3 = U_2 \zeta^{\frac{N_n}{2}} = U_0 \zeta^{3\frac{N_n}{2}}, \tag{33}$$

The voltage U_3 exceeds the level of the input signal and the comparator further retains the level of the logical unit at the output. Since the state of the Km comparator has not changed, the action of the third clock pulse is similar to the previous ones, that is, the third pulse is recorded in the result counter L.

The second clock pulse connects the output voltage EM2 to the first input of the adjustable scale amplifier ASC, and the first memory element EM1 – to the output of the amplifier ASC, the voltage on which takes the value:

$$U_4 = U_3 \zeta^{\frac{N_n}{2}} = U_0 \zeta^{4\frac{N_n}{2}}, \tag{34}$$

Since this voltage U_4 is less than the input voltage, the Km comparator switches to a logical zero state at its output. After this zero, the control block CB prohibits the passage of clock pulses to the result counter L and to the clock input of the EFFU unit, that is, the memory elements EM1 and EM2 remain connected to the adjustable scale amplifier as in the state after the third pulse. The number of clock pulses n_1 recorded in the result counter L determines the value of the highest digits (N_1) of the source code of the logarithmic analogue-to-digital converter according to the equation:

$$N_1 = n_1 w_1, \tag{35}$$

where w_1 – weight of the first (highest) digit of the converter source code, which is equal to

$$w_1 = \frac{N_n}{2}, \tag{36}$$

Therefore, the value of the highest digits of the source code of the logarithmic analogue-to-digital converter:

$$N_1 = 3\frac{N_n}{2}, \tag{37}$$

After the first transition of the comparator "1" to the logical "0" state since the start of the converter, the conversion begins in the second section. At the second stage of the conversion, the control block CB translates the generating control signals B and D. Signal B allows the operation of the ASC on inputs 2-n, and signal D allows the operation of the Rg register.

The fifth tactile pulse writes a logical zero to the first digit of the Rg result register and turns on the second input of the adjustable scaling amplifier ASC, i.e., sets the second value of the transmission coefficient value:

$$K_2 = \zeta^{\frac{n_n}{2^2}}, \tag{38}$$

Therefore, the voltage at the output of the ASC amplifier, and therefore at the output of the EFFU block, the formation of the exponential function, becomes equal to:

$$U_5 = U_3 K_2 = U_0 \zeta^{3\frac{N_n}{2}} \zeta^{\frac{N_n}{2^2}} \zeta^{\frac{N_n}{2^3}}, \tag{39}$$

The voltage U_5 is recorded on the first memory element EP1 connected to the output of the ASC amplifier. Since the voltage U_5 exceeds the input signal level, the Km comparator switches to the state of a logical unit at the output and the control unit allows the passage of clock pulses to the clock input of the EFFU unit.

The sixth tactile pulse writes a logical unit to the second digit of the Rg result register and sets the third value of the ASC amplifier transmission coefficient. By the same tactile pulse, the voltage U 5 is applied to the input of the ASC amplifier from the first memory element EM1 and the output voltage of the ASC amplifier becomes equal:

$$U_6 = U_5 K_3 = U_0 \zeta^{3\frac{N_n}{2}} \zeta^{\frac{N_n}{2^2}} \zeta^{\frac{N_n}{2^3}}, \tag{40}$$

Since this voltage U_6 is less than the input voltage, the Km comparator switches to a logical zero state at its output. Beyond this zero, the CB prohibits the passage of clock pulses to the clock input of the EFFU unit and the memory elements EM1 and EM2 remain connected to the adjustable scale amplifier ASC as in the state after the fifth pulse.

The seventh tactile pulse has the same effect as the fifth (only sets the fourth value of the transmission coefficient of the ASC amplifier), etc. After receiving n tactile pulses in the second conversion section, the output voltage of the EFFU unit will have the value:

$$U_{n2} = U_{n1} \prod_{i=2}^{i=n} \zeta^{A_i \frac{N_n}{2^i}}, \tag{41}$$

where U_{n1} – value of the voltage in the first sub-band after n_1 clock pulses; A_i – coefficient that takes in each i-clock the conversion of the value 1 or 0 in accordance with the state of the comparator logical "1" or logical "0".

The value of the voltage U_{n2} on the second sub-band after *(n)* the clock pulses, that is, after connecting the last input of the adjustable scale amplifier, will be equal to the input voltage:

$$U_{n2} = U_{BX}, \tag{42}$$

with an error not exceeding the weight of the last minor digit. (n+1) the value of the lower digits of the source code (N_2) of the logarithmic analogue-to-digital converter will be recorded in the Rg result register by a tactile pulse:

$$N_2 = \sum_{i=2}^{n} A_i \frac{N_n}{2^i}, \tag{43}$$

The source code (N) of the logarithmic analogue-to-digital converter, wherein the proposed recurrent method is implemented, equal to the sum of the codes in the first and second sections:

$$N = N_1 + N_2, \tag{44}$$

$$N = \frac{N_n}{2}\left(n_1 + \sum_{i=2}^{n} A_i \frac{1}{2^{i-1}}\right), \tag{45}$$

that is, there is a logarithm-proportional ratio of the input voltage U_{BX} to the reference U_o :

$$N = \frac{1}{log\zeta} log \frac{U_{BX}}{U_o}, \tag{46}$$

Developed on the basis of the proposed improved recurrent method, the converter belongs to logarithmic ADCs and has an increased speed compared to the classical recurrent ADC.

There are two ways to change the basis of the logarithm. Namely, with a change in the reference voltage or with a change in the ratio of capacitances of the capacitors of the cell. Since it is these values that affect the height of the voltage step. The basis of the logarithm in converters on switched capacitors depends on the ratio of capacitances, accumulating and dosing capacitors:

$$\zeta = \frac{C_N}{C_D + C_N}, \tag{47}$$

where ζ – basis of the logarithm; C_D – capacity of the metering capacitor; C_N – capacity of the accumulating capacitor; C_D C_N.

Next, the study considers how the transformation occurs with a change in the base of the logarithm. First, the conversion range is divided, for example, m -sub-bands and a compensation voltage U_k is formed on each (U_{k_1}) -sub-band according to the following expression:

$$U_{k_i} = U_{B_i} \zeta_i^{n_i}, \tag{48}$$

where n_i – the number of dosages on the i-sub-band; U_B - the initial value of the voltage on the i-sub-band; ζ_1 – the basis of the logarithm on the i-sub-band.

At each sub-band, changing the compensation voltage from the initial level U_B to the moment of transition through the input signal level (the moment of equality is fixed by the comparator). The initial voltage level U_k on the first sub-band is equal to the reference, that is $U_{B_1} = U_0$, the number of dosages on the i-sub-band is proportional to the logarithm of the input voltage U_{IN}:

$$n_i = \frac{1}{log \zeta_1} log \frac{U_{IN}}{U_{B_i}}, \tag{49}$$

and it determines the number of steps of the transformation characteristic on each of the sub-bands. The basis of the logarithm ζ changes on each subrange.

The value of the base of the logarithm in the descending scan depends on the minimum value of the input voltage. For an ascending sweep – from the maximum value of the input voltage. The initial value of the compensating voltage affects the basis of the logarithm for both scans. The required value ζ is physically implemented by changing the ratio of capacitances of capacitors. Each of the sub-bands corresponds to a separate weight of the sub-band v_i. The conversion time can be determined as follows:

$$t_n = \sum_{i=1}^{m} n_i T, \tag{50}$$

where N – the repetition period of the clock pulses.

The conversion process with a variable logarithm basis changes the ratio of capacities and a one-way descending scan. When forming a descending scan, the initial level of the compensating voltage on the first sub-band is set as equal to the reference, that is $U_{B_1} = U_0$. The reference value for a descending scan will correspond to the maximum possible value of the input voltage.

During the conversion of the first sub-band, the compensation voltage U_k is changed from the initial level to the moment of transition through the input signal level. After that, for the next sub-band U_{B_1}, the initial level is set equal to the penultimate value of the compensation voltage. At the end of the conversion on the first sub-band, the number of dosages is equal to:

$$n_1 = \frac{1}{log \zeta_1} log \frac{U_{IN}}{U_0}, \tag{51}$$

and the penultimate level of the compensation voltage (it is also the initial level for the second sub-band):

$$U_1 = \zeta_1^{n_1 - 1} U_0, \tag{52}$$

At the end of the conversion on the second sub-band (the second operation of the comparator), the number of dosages will be equal to:

$$n_2 = \frac{1}{log \zeta_2} log \frac{U_{IN}}{U_1}, \tag{53}$$

and the initial value of the compensation voltage on the third sub-band:

$$U_2 = \zeta_2^{n_2-1} U_1 = \zeta_2^{n_2-1}(\zeta_1^{n_1-1} U_0), \tag{54}$$

At the end of the conversion on the second sub-band (the second operation of the comparator), the number of dosages will be equal to:

$$n_3 = \frac{1}{log\zeta_3} log \frac{U_{IN}}{U_2}, \tag{55}$$

and the initial value of the compensation voltage on the fourth sub-band:

$$U_3 = \zeta_3^{n_3-1} U_2 = \zeta_3^{n_2-1}(\zeta_1^{n_1-1}(\zeta_1^{n_1-1} U_0)), \tag{56}$$

Then the general formula describing the change in the compensation voltage will have the following form:

$$U_k = U_{B_1} = U_0 \prod_{i=1}^{m} \zeta_i^{n_i-1}, \tag{57}$$

The result of the transformation N_1 with a one-way descending scan on the first sub-band is obtained by multiplying the number of dosages reduced by one $n_1 - 1$ by the weight v_1, of the first sub-band and writing this product in the result counter:

$$N_1 = (n_1 - 1)v_1, \tag{58}$$

or:

$$N_1 = \left(\frac{1}{log\zeta_1} log \frac{U_{IN}}{U_0} - 1\right) v_1, \tag{59}$$

At the end of the conversion on the second sub-band, the number of dosages reduced by one is multiplied by the weight of the second sub-band:

$$N_2 = (n_2 - 1)v_2, \tag{60}$$

or:

$$N_2 = \left(\frac{1}{log\zeta_2} log \frac{U_{IN}}{U_1} - 1\right) v_2, \tag{61}$$

This product is added to the content of the result counter and at the end of the conversion, a number will be written in the result counter on the second sub-band:

$$N = N_1 + N_2, \tag{62}$$

$$N = (n_1 - 1)v_1 + (n_1 - 1)v_2, \tag{63}$$

or:

$$N = \left(\frac{1}{log\zeta_1} log \frac{N_{IN}}{N_0} - 1\right) v_1 + \left(\frac{1}{log\zeta_2} log \frac{U_{IN}}{U_1} - 1\right) v_2, \tag{64}$$

Finally, the result of the transformation is equal to the sum of the products of the individual mentioned sub-bands:

$$N = \left(\frac{1}{log\zeta_1} log \frac{N_{IN}}{N_0} - 1\right) v_1 + \left(\frac{1}{log\zeta_2} log \frac{U_{IN}}{U_1} - 1\right) v_2 + \cdots + \left(\frac{1}{log\zeta_m} log \frac{U_{IN}}{U_{m-1}} - 1\right) v_m, \tag{65}$$

That is, the result of the transformation is found as the sum of the products of the number of dosages and the weight on each sub-band by the equation:

$$N = \sum_{i=1}^{m} (n_i - 1)v_1, \tag{66}$$

$$N = \sum_{i-1}^{m} \left(\frac{1}{log\zeta_i} log \frac{U_{IN}}{U_{Bi}} - 1\right) v_i, \tag{67}$$

Therefore, with a descending scan on each sub-band, the number of dosages has a strict logarithmic dependence. The source code is formed taking into account the number and weight of each of the sub-ranges.

When converting with an ascending sweep, we set the initial level of the compensating voltage on the first sub-band equal to the reference, that is $U_{B_i} = U_0$. The reference value for and ascending scanning will correspond to the minimum possible value of the input voltage. Further, the conversion will occur similarly to

the previous one, only the expansion of the compensation voltage will be ascending. The conversion process with a variable logarithm basis by changing the ratio of capacitances and a two-way scan. The peculiarity of a logarithmic ADC with a change in the base of the logarithm and a two-way scan is as follows.

On each sub-band, the compensation voltage U_k is changed from the initial level U_{B_i} to the moment of transition through the input signal level; moreover, the initial level U_{B_i} on the i-sub-band is set equal to the last value of the compensation voltage on the previous sub-band:

$$U_k = U_{B_i} = U_0 \prod_{i=1}^{m} \zeta_i^{n_i}, \tag{68}$$

The initial level on the first sub-band is equal to the reference level, that is $U_{B_i} = U_0$. Next, the study considers the conversion process. At the end of the conversion on the first sub-band, the number of dosages will correspond to the equation (51), and the last level of the compensation voltage (it is also the initial level for the second sub-band):

$$U_1 = \zeta_1^{n_1} U_0, \tag{69}$$

Using a multiplier, the number of dosages n_1 is multiplied by the weight v_1 of the first sub-band and write this product in the result counter:

$$N_1 = n_1 v_1, \tag{70}$$

$$N_1 = \frac{v_1}{log\zeta_1} log \frac{U_{IN}}{U_0}, \tag{71}$$

On the second sub-band, the direction of the unfolding compensation voltage was changed from descending to ascending. At the end of the conversion on the second sub-band (the second operation of the comparator), the number of dosages will correspond to (51), and the last value of the compensation voltage on the second sub-band, which will be the initial value for the third sub-band:

$$U_2 = \zeta_2^{n_2} U_1, \tag{72}$$

Using a multiplier, the number of dosages n_2 is multiplied by the weight v_2 of the second sub-band:

$$N_2 = n_2 v_2, \tag{73}$$

$$N_2 = \frac{v_2}{log\zeta_2} log \frac{U_{IN}}{U_1}, \tag{74}$$

In the result counter N_2, this product is subtracted from the first product N_1. Therefore, at the end of the conversion, a number will be written in the result counter on the second sub-band:

$$N = N_1 - N_2, \tag{75}$$

The value N differs from the value of the result for a one-way scan in the expression (62)-(63) by the sign between the and codes N_1 and N_2 obtained on the first and second sub-bands:

$$N = n_1 v_1 - n_2 v_2, \tag{76}$$

$$N_1 = \frac{v_1}{log\zeta_1} log \frac{U_{IN}}{U_0} - \frac{v_2}{log\zeta_2} log \frac{U_{IN}}{U_1}, \tag{77}$$

On the third and other odd sub-bands, the transformations are performed in the same way as on the first (descending scan). On the fourth and other paired sub-bands, the transformations are performed as on the second (ascending scan). Finally, at the end of the conversion, the logarithm of the input signal will be recorded in the result counter and $N = U_{IN}$:

$$N = n_1 v_1 - n_2 v_2 + n_3 v_3 - n_4 v_4, \tag{78}$$

or:

$$N_1 = \frac{v_1}{log\zeta_1} log \frac{U_{IN}}{U_0} - \frac{v_2}{log\zeta_2} log \frac{U_{IN}}{U_1} + \frac{v_3}{log\zeta_3} log \frac{U_{IN}}{U_2} + \cdots + \frac{(-1)^{m-1} v_m}{log\zeta_m} log \frac{U_{IN}}{U_{m-1}}, \tag{79}$$

Therefore, the transformation with a two-way scan occurs on odd sub-bands from top to bottom, and on even sub-bands – from bottom to top. And, accordingly, the source code of the transformation is formed alternately with different signs.

4. Conclusions

General principles of analogue-to-digital functional transformation with a variable logarithm basis. The undoubted advantage of circuits with switched capacitors is that the phenomena that occur in them and provide the very process of conversion – redistribution and accumulation of charge – allow obtaining any value of the base of the logarithm. The characteristic of the ATFC conversion on switched capacitors is logarithmic, and forms a sequence from the voltage change on the accumulating capacitor. The construction of the transformation characteristic is possible in steps from top to bottom forming a descending sweep, or steps from bottom to top with an ascending sweep, and also, alternately changing the direction of unfolding on separate sub-bands, a two-way sweep is obtained. The base of the logarithm is responsible for the height of each individual step and, accordingly, for the conversion rate. Schemes with a variable logarithm basis allow choosing the necessary accuracy and speed of the conversion.
In real-time measurement, automation and automation systems, the reaction speed is the determining characteristic. To simplify programming and speed up work, so-called recurrent formulas are used. The essence of recurrent algorithms is to remember the last value and use it for calculations. The essence of the development of the recurrent method of analogue-to-digital functional conversion is that the weight of the highest digit is used repeatedly and at the time of the transition of the compensation voltage through the input signal level, the value of the highest digits of the output code is recorded as the product of the weight of the highest digit by the number of uses of this weight (not counting the transition), and the values of the lowest digits are determined as in the classical recurrent method

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