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Things that keep people and nations together are far more important than things that divide us.

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General introduction

Wide bandgap (WBG) power transistors such as SiC MOSFETs and GaN HEMTs are a real breakthrough in power electronics. These power semiconductor devices have lower conduction and switching losses than their Silicon competitors. However, the fast switching transients can be an issue in terms of Electromagnetic Interferences (EMI) to the system point of view. Consequently, one must slow down the switching speeds of WBG transistors to comply with EMI limitations, which reduces their advantages in terms of higher switching frequencies and lower total losses. To take the full potential of WBG power devices, it is then critical to guarantee low switching losses and a careful control of EMI perturbation sources.

In the literature, several solutions have been proposed with active gate drivers to actively control the switching transitions of power devices: in the early 2000s, tunable gate driving have been introduced with Silicon power MOSFETs and IGBTs. The fundamental idea is to adjust, or directly set, the time derivatives of the drain-to-source voltage (d*v*/d*t*) and/or drain current (d*i*/d*t*), thanks to an active gate driver. This offers a perfect optimization of the switching losses versus EMI trade-off, and guarantees fixed and robust d*v*/d*t* and d*i*/d*t* which are not affected by dispersions on power devices nor operating conditions. The techniques proposed are either based on a passive or open-loop driving scheme, or a closed-loop control between the high voltage drain-to-source terminal and the gate node. For this latter technique, a feedback loop is introduced to actively control the gate current during the power switching, based on the sensed d*v*/d*t* and d*i*/d*t* on the power terminals. However, in the case of silicon power devices, the switching times can be higher than several microseconds or even hundreds of microseconds, which makes it feasible to introduce a closed-loop control between the high voltage terminals to the low voltage gate terminal. In the case of SiC MOSFETs, the switching transients occur in less than 10ns, and even faster with GaN HEMTs, in less than 3ns. In this context, it is really challenging to introduce a feedback loop between the high voltage drain-source terminals towards the gate, and to obtain a closed-loop control of d*v*/d*t* and d*i*/d*t*. With such fast WBG power devices, most active gate driving solutions are based on open-loop control, which cannot adapt to dispersions nor change of operating points.

In this work, an active gate driver is proposed to control the switching speed of wide bandgap semiconductor power transistors. An innovative closed-loop control

circuit makes it possible to adjust separately the d*v*/d*t* and d*i*/d*t* during the switching sequences. Overall, the d*v*/d*t* values can be reduced to comply with system-level limits of EMI, with less switching losses than existing methods. The first chapter of this thesis will present the challenges, literature review of active gate driving and WBG power devices. The proposed technique is then introduced, and the specifications and integration technique are detailed.

In the second chapter, the proposed method is thoroughly investigated, with analytic and numerical models to assess the key performances: feedback loop bandwidth, optimal circuit design and area consumption. The assumptions are clearly described, and the analytic models are compared with numerical simulations. This modeling offers the possibility to optimize the performances and to realize a sub-nanosecond feedback loop for an active gate driving solution.

In the third chapter, selected and optimal designs are implemented in two integrated circuits in CMOS technology. The integrated circuits are designed and then experimentally implemented in high voltage power commutation cells. A particular attention has been paid to minimize the effects of parasitics, and to be able to experimentally demonstrate the fast operation of closed-loop control. The experimental results confirm the highest speed of active d*v*/d*t* closed-loop control, within less than one nanosecond. With such performances, it has been shown experimentally that it is possible to actively control switching speeds higher than 100 V/ns under voltages of 400 V.

Finally, a general conclusion and a discussion on future works are presented, to further extend and transfer this approach in the context of power converters based on WBG power devices.

1 Active Gate Drivers: review and key specifications

This chapter presents a review and critical analysis of Active Gate Drivers (AGD) for dv/dt and di/dt control for power semiconductor devices made with silicon and wideband gap (WBG) materials. First, selected application examples are described in the context of high efficiency power converter systems. Then, a brief overview of switching transients of power devices is presented as well as examples of switching energy measurements. Then, benefits of WBG transistors are discussed, followed by challenges and advantages of Active Gate Drivers. The state-of-the-art of switching trajectory control is then classified by types of transistors and types of control systems. Finally, the AGD integration approach is presented, the choice of the AGD technology explained, and the proposed dv/dt control method is introduced.

1.1 Applications for WBG devices

Power electronic systems have a growing market worldwide. A report published in July of 2020 [1], based on data of twenty large companies, states that the global power electronics market size is projected to grow from USD 35.1 billion in 2020 to USD 44.2 billion by 2025, at a grow rate of 4.7% even considering the impact of Covid-19 on sales reduction. Regarding wide bandgap (WBG) transistors more specifically, the market is projected to grow to USD 600 million by 2025 [2].

This growth is mainly due to the electrification of transportation systems such as trains, cars and aircrafts. Fully electric systems are replacing mechanical, pneumatic, and thermal systems in order to not only to increase system efficiency and reliability, but also to reduce ecological footprint of such systems.

Another area pushing power electronic market is the growing production and distribution of renewable energy such as wind power and photovoltaics. These applications need high efficiency power converter systems. Recently, these power converters are being designed with the so-called wide bandgap power transistors (WBG). These transistors need lower gate charge to turn-on and off when compared to their silicon counterparts. Consequently, they switch at higher speeds and have reduced switching losses. However, this high speed engenders numerous issues which will be more detailed in this thesis in the next sections.

The energy transition from fossil fuels to renewable sources should be accomplished with increase in efficiency of electrical systems. Public investments worldwide should be focused in increasing the amount of renewable sources when producing electricity and decreasing the waste of energy with more efficient systems.

When designing a static power converter system, a system designer needs to choose a gate driver (GD). A survey made in 19/05/2020 by Wolfspeed/Cree™ in a technical webinar shows that the engineers are more worried about high d*v*/d*t* values than short circuit protection or negative voltage generation in their projects (**Figure 1.1**).

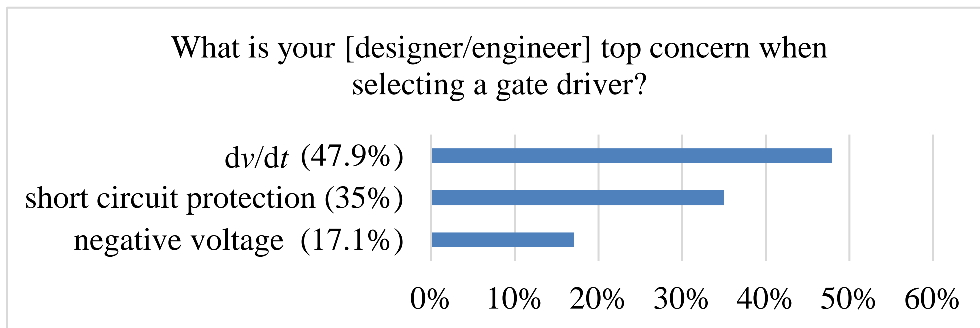


Figure 1.1. Survey made during the webinar: "A Designer's Guide to Silicon Carbide" by Wofspeed/Cree™ on 19/05/2020. It shows the importance of the d*v*/d*t* when choosing a gate driver (GD) and designing a power converter system.

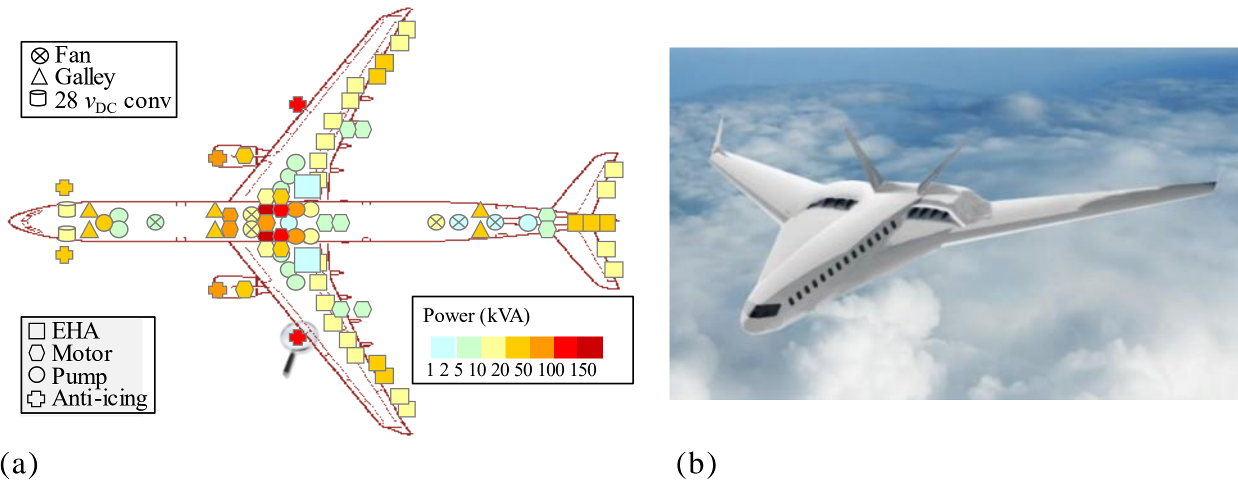
To reduce the switching speed and at same time keeping a high efficiency of power conversion systems, WBG power devices can be used with Active Gate Drivers (AGD) as it will be explained in the next sections. Notice that in the literature, the expression Active Gate Drivers (AGD) is also found as active gate voltage control [3] [4] [5], trajectory control, slew rate control [6], active gate charge control [7], switching speed control [8] and wave-shaping.

1.1.1 Applications for aeronautic industry

In 2017 IEEE ECCE conference, one keynote speech was given by Dr. Nateri K. Madavan of NASA. Among the many thought-provoking ideas, he mentioned a stated goal to reduce the carbon consumption of the air transportation industry by 50% between the years 2005 and 2050 [9].

Figure 1.2 (a) shows the systems that consumes electric power in modern liner airplanes. **Figure 1.2** (b) is an artistic representation of a future hybrid powered or all electric powered aircraft. The global aviation industry produces around 2% of all human-induced carbon dioxide (CO_2) emissions. To reduce this environmental

impact, aircrafts with electrical propulsion should have the power source provided from a renewable source.



(a) (b)

Figure 1.2. (a) Systems consuming electric power in modern liner aircrafts. (b) Hybrid and all electric propulsion systems concepts in development for a more ecological footprint. Credit: University of Illinois [10].

More Electric Aircraft (MEA) and All Electric Aircraft (AEA) are concepts that can only be effective if power converters have a significant reduction of losses and weight, which can only be enabled by the use of disruptive technology such as SiC and GaN semiconductors. These WBG transistors will allow a strong increase of switching frequencies with the consequent filter reduction and/or decreasing semiconductor losses. Loss reduction may avoid liquid cooling inside aircrafts, and consequently increasing reliability and reducing maintenance costs and weight.

As previously mentioned, for a better energy efficiency and to reduce its ecological footprint, the transport sector is turning to the development of more electrical solutions which, in order to be competitive, require the increase on the voltage and the use of WBG technology. This approach requires rethinking the complete design of some electric systems such as a power drive system for aircraft applications (see **Figure 1.3**). Optimization of power drive system using WBG devices is the goal of “EPOWERDRIVE” project conducted in the French Research Institute IRT Saint-Exupéry. The goal is to increase power density, efficiency and reliability, as well as to reduce manufacturing cost of power drive system in a 540 V / 70 kVA power drive system.

This public-private project is sponsored by Airbus™, AKKA™, Apsi3D™, ELVIA™, Liebherr™, Meggit™, Nidec™, Safran™ and the French National Research Agency (ANR). It englobes 4 different work packages:

1 – Multi Disciplinary Optimization (MDO) of power drive systems;

2 – EMI (Electromagnetic interference) issues in power drive systems using WBG devices;

3 – Technologies for power converters in power drive systems;

4 – Technologies for motors in power drive systems and applications of additive layer manufacturing.

One of the main research topics in work package 3 is how to design an innovative gate driver (GD) for GaN and SiC devices which allows low switching speed (to decrease filtering needs) and at the same time keep low switching losses (to increase efficiency and power density). This innovative GD technique is the focus of this thesis, which is sponsored by "E-POWERDRIVE" project.

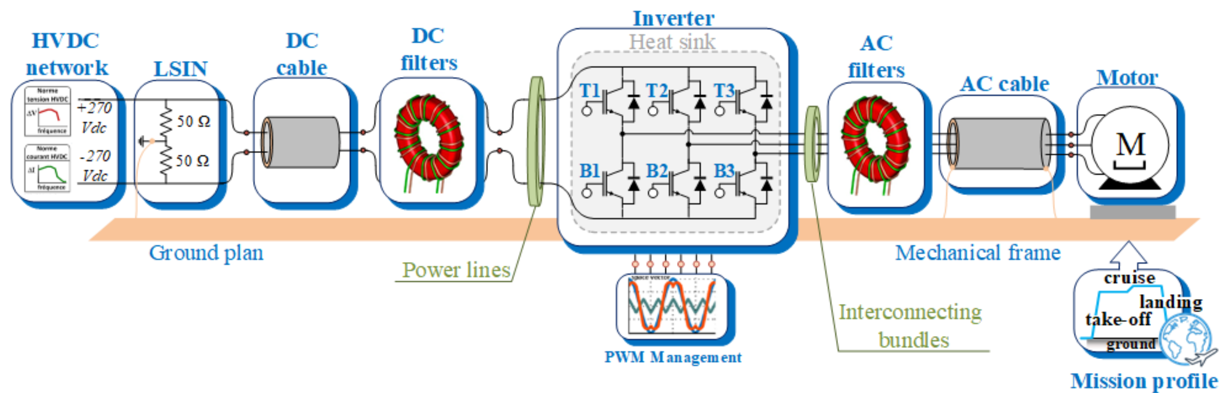


Figure 1.3. Power drive system in airplane with an electric motor used for cabin pressurization system. It represents the system to optimize (converter, filters, cable and motor) in the E-POWERDRIVE project at IRT Saint-Exupéry [11].

1.1.2 Applications for space industry

For space applications, circuits that provide and convert electric energy are required to have high efficiency and low weight. The amount of energy stored in the batteries are limited and efficient systems increase the time and performance of the electronics on board. In addition, a more efficient system leads to higher power density, which represents lower cost for launching into space. Higher efficiency and power density can be significantly improved by using WBG devices. Given the voltage level of converters for space application (under 200V for DC/DC converters), GaN are more suitable devices to replace existing Si MOSFETs [12]. Many other scientific works are being conducted by Thales Alenia Space™ and CNES™ in Toulouse regarding the substitution of power MOSFETs with GaN transistors for

space applications. GaN transistors are not only more efficient but are also more resistant to radiation [13].

Figure 1.4 is an artistic representation of European Space Agency's ExoMars spacecraft. Typical input voltage from power converter systems in spacecraft and satellites with solar panels are 20 V to 125 V and the number of output voltage levels is from 2 to 10 [14], for example 12 V, 5 V, 3.3, V and 2.5 V.

Figure 1.4. Space applications require power supply systems that are highly efficient. European space agency ESA explorers contains hundreds of static DC/DC converters for power management units on board. Credit: ESA/ATG Medialab.

1.1.3 Terrestrial transportation and industry applications with electric motors

Electric motor systems account for about 60% of global industrial electricity consumption and close to 70% of industrial electricity demand [15].

Regarding safety for road vehicles, human errors of perception, judgment and operation are the cause to 90% of road accidents. Power electronic systems can indirectly play a major role in improving the safety of vehicles [16]. Autonomous driving requires electric actuators to implement decisions made by a computer. Other than safety systems, a more obvious system is the propulsion for electric vehicles. **Figure 1.5** shows the most power-consuming place where power devices are used in electric cars. The system called inverter makes the interface between the electrical machine and the energy storage device that can be a battery.

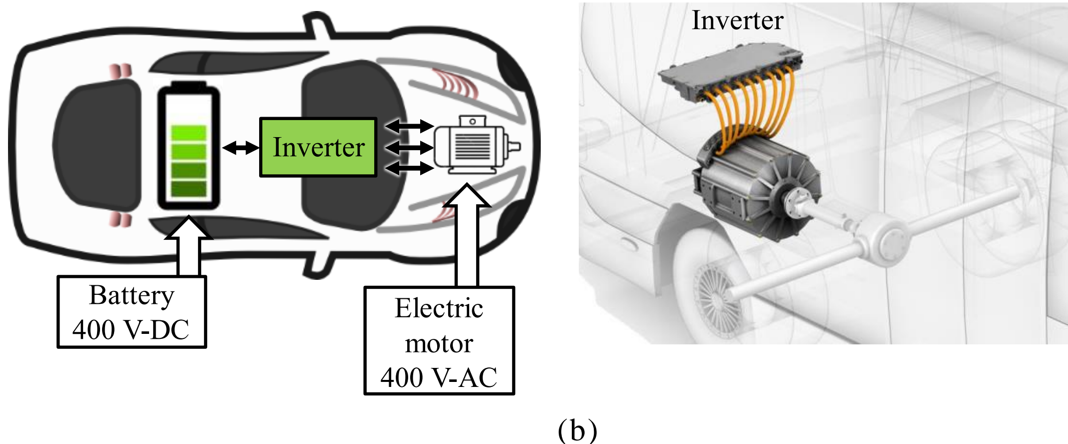


Figure 1.5. Power inverters are used in automotive and transportation industry. (a) The power inverter connects and control the power flow from batteries to the electric motor (b) 3D representation of the solid-state electronic devices required to control the speed of electric motors.

Most of the vehicles store energy in 400V batteries. Given this voltage level, GaN transistors are more suitable devices to increase efficiency and power density. However, some higher power propulsion system require 800V storage systems (BMW^{TM}, Tesla^{TM}) and for that reason, SiC components are being used [17]. This study estimates a 7% increase in mileage by "simply" replacing silicon IGBT with 3rd generation SiC transistors in 800V DC bus voltage.

Solid-state electronic power devices can control the speed of electric motors. Most of the motors sold in the market are AC type and to control their speed, a power inverter with power transistors is required. One example of scientific publication with static converters using GaN transistors specifically for automotive applications can be found in [18].

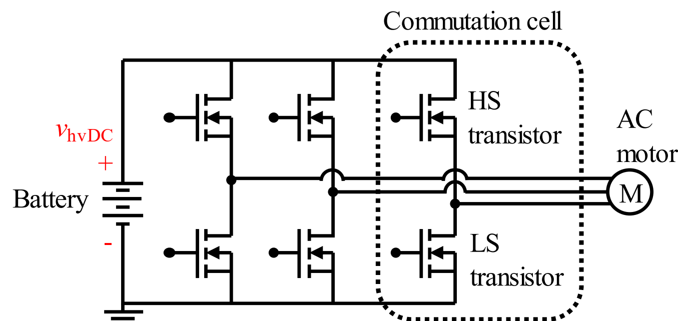


Figure 1.6. Example of three-phase inverter circuit, which is composed by many switching legs with usually a pair of power device components called high side transistor (HS) and low side transistor (LS). The power transistor represented can be a Si or SiC MOSFET, IGBT or GaN HEMT. Power inverters can also be regenerative sending energy back to the batteries when the electric vehicle is braking.

All the 6 power devices of the inverter in **Figure 1.6** require a GD to switch-on or switch-off. Regarding research work about GD's for a power inverter, one paper from 2019 from a Semikron™ team [19] shows a compact automotive inverter with SiC transistors with a dedicated power Integrated Circuit (IC). This paper reports to achieve low switching losses thanks to high d*v*/d*t* of 40 V/ns. With a compact packaging of only 600 cm^3 it can have a peak power of 30 kW with 1200 V SiC transistors and 5 nH commutation inductance loop.

Regarding the train industry, a similar power converter is used comparing to other terrestrial electric vehicles. Because the required power is higher, the v_{hvDC} bus voltage is also higher. High voltage and up-to-date IGBT or SiC (more recently for higher efficient systems) modules are used for this application with breakdown voltage of 3.3 kV. The common DC link bus voltage (v_{hvDC}) is converted to AC voltage for the AC motors and it is converted to another DC voltage level for the battery banks. See **Figure 1.7** extracted from [20].

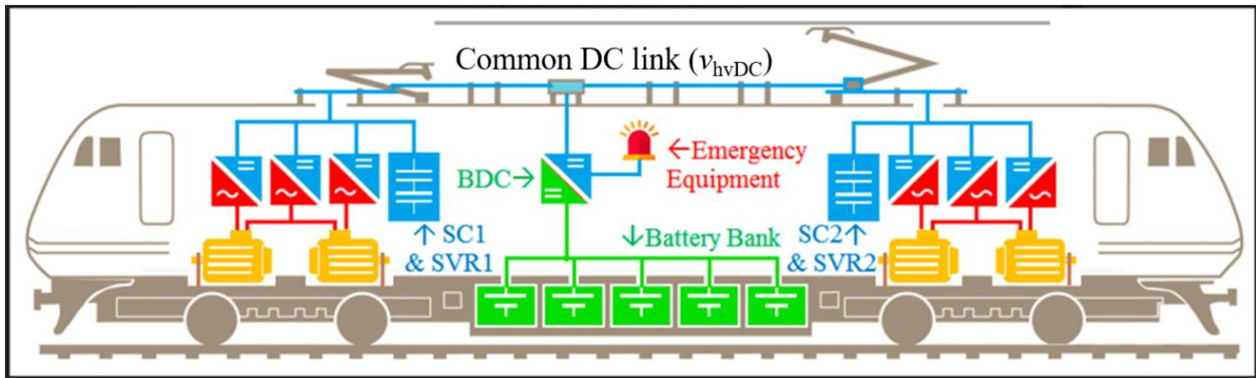


Figure 1.7. Power inverters are used to convert DC voltage from the DC link (v_{hvDC}) to AC for the motors and for another value of voltage in DC for the batteries. Image extracted from [20].

1.1.4 Low power applications for WBG transistors

Consumer electronics need static power conversion systems for the power supply circuit. The rise of IOT (Internet Of Things) represents a growing market for power electronics and therefore also for power ICs (Integrated Circuits). The number of objects connected to the internet is projected to achieve 75 billion in 2025 [21].

Efficient AC adapters for USB chargers usually have a flyback topology shown in **Figure 1.8**. The use of WBG power transistors increases the efficiency of these high AC voltage to low DC voltage converters. Using a GaN power transistor and a GD adapted for this device, smaller power adapters can be manufactured

having the same capability in power, which means a faster charge time to the consumer electronic product like laptops or smartphones.

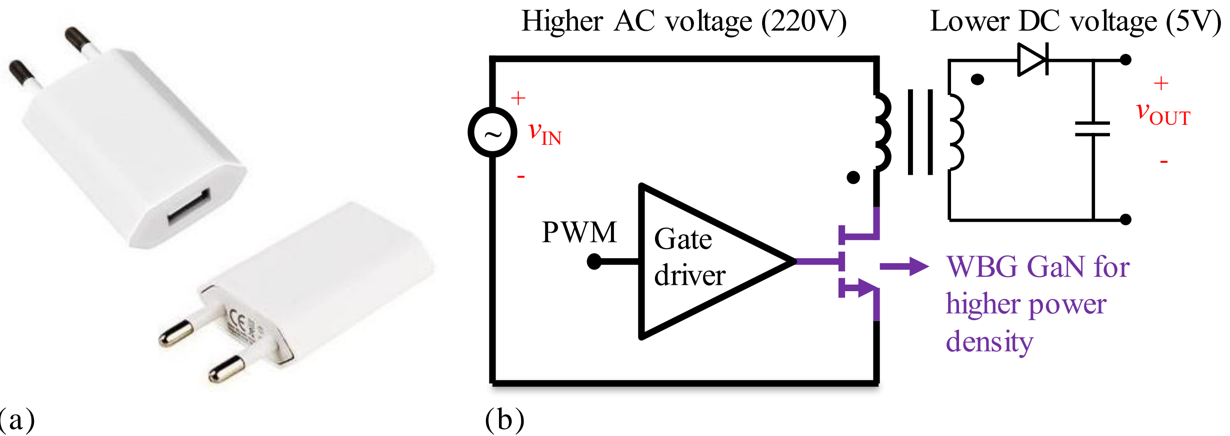


Figure 1.8. Power adapters for USB chargers. (a) Photo of a product and (b) schematic of a Flyback converter topology. To make smaller products and achieve higher power density, WBG power transistors should be employed.

A DC-DC buck converter can also be fabricated with GD and power device with all-GaN technology. Paper [22] reports stable 10V output with inputs ranging from 15 V to 30 V with a monolithic power GaN IC. **Figure 1.9** shows the CMOS-compatible fabrication of the all-GaN converter power IC for consumer electronics applications (or also called home electronics).

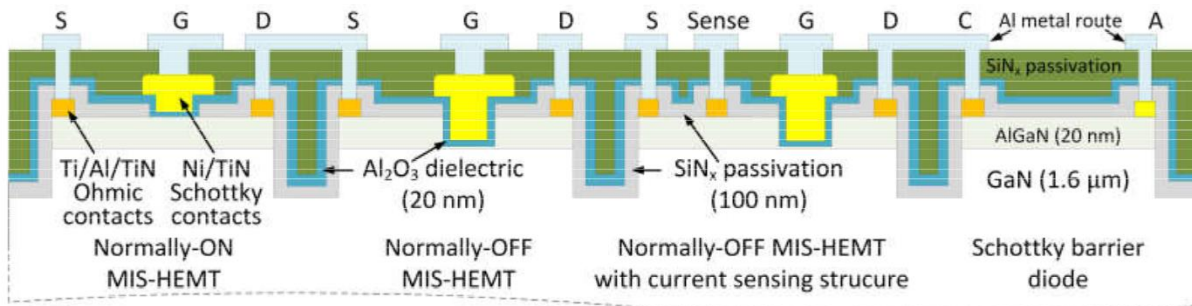


Figure 1.9. Schematic cross section of GaN power IC platform based on AlGaN/GaN MIS-HEMTs and Au-free Ti/Al/TiN ohmic contact. From [22].

Other transistor topologies can be Metal-Insulated-Metal High Electron Mobility Transistors (MIM-HEMT) and Schottky Barrier Diodes (SBD) [23]. This technology can have a more competitive price even with lower performance comparing to other GaN technologies.

Other works with GaN and GD integrated from CEA Institute are presented for example in [24], where an integrated inverter leg is presented and tested, switching 400V at 1MHz under 3A.

1.2 Wide bandgap power devices

The physical properties of the power devices using WBG materials are superior to the ones using silicon. **Figure 1.10** shows one of the advantages to use SiC and GaN, which is the specific on-state resistance. For a same breakdown voltage, GaN has a lower specific ON resistance than SiC and Si. Consequently, this allows a reduction if the active area and/or a lower on-state resistance with WBG power devices.

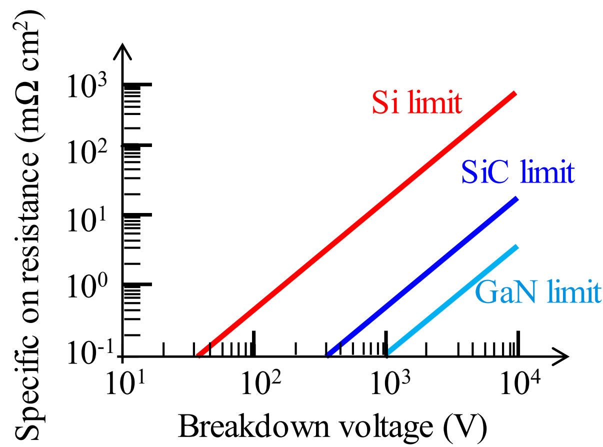


Figure 1.10. Theoretical specific ON-resistance of unipolar transistors made with Si, SiC and GaN. Using WBG devices instead of Si, a smaller device is possible for the same desired breakdown voltage and ON-resistance. Smaller devices have less parasitic elements and therefore higher dynamic performance.

Technological process to develop GaN devices are being actively explored. Even low cost 200 mm wafer size technology GaN-on-Si can demonstrate experimentally values of specific on-resistance much lower than theoretical values for silicon devices [25].

WBG devices present lower ON-state resistance and intrinsic (or parasitic) capacitance than equivalent components made in Silicon, for the same voltage and current. For that reason, power converters designed with SiC or GaN can achieve higher values of efficiency and power density as illustrated in **Figure 1.11**, where it is shown Pareto fronts of possible solutions of converter designed with Si, SiC and GaN transistors.

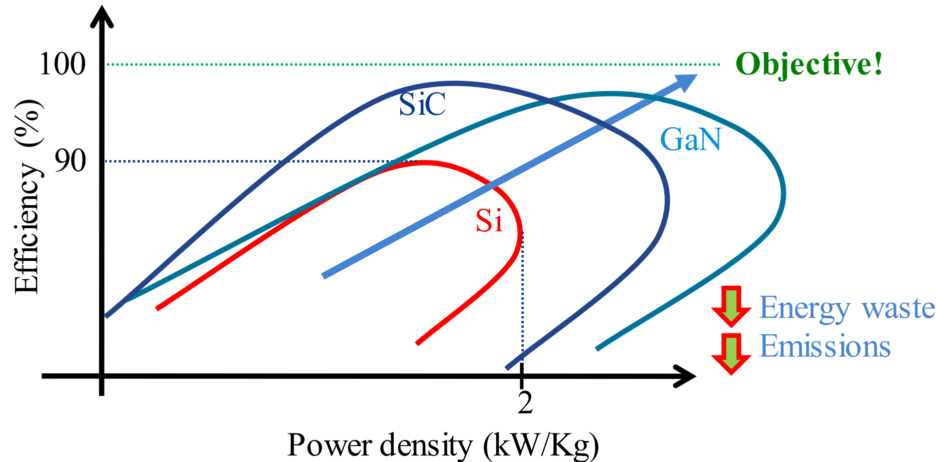


Figure 1.11. In the context of power inverters design, WBG power transistors represent higher efficiency and higher power density.

WBG power devices require lower gate charge to turn-on or off. Thus, these devices can achieve higher switching speed in the order of many hundreds of volts per nanosecond. To prevent negative EMI effects of such fast transitions, trajectory control systems can operate to change the derivative of output voltage. This is the role of the Active Gate Driver developed in this work.

In order to take full advantage of WBG technology, circuit designers have to understand the unique features of those transistors. The design must focus on reliability, noise, efficiency, speed and cost [26]. The Active Gate Driver developed in this work has the goal to improve all these aspects as it will be shown in this text.

1.3 Switching behavior of power transistors

1.3.1 Analytic models of d*v*/d*t* and d*i*/d*t* during transients

Most applications shown above use converters based on one or several commutation cells. The output of this cell is usually connected to an inductive impedance, which can be either an output filter or a motor winding. In order to explain the switching process, we will assume a pure inductive load connected to the middle point of the commutation cell and the positive terminal of the source v_{hvDC}, as shown in **Figure 1.12**. Notice that the load current (i_{L}) can be controlled by a PWM voltage (v_{PWM}) applied to the LS GD.

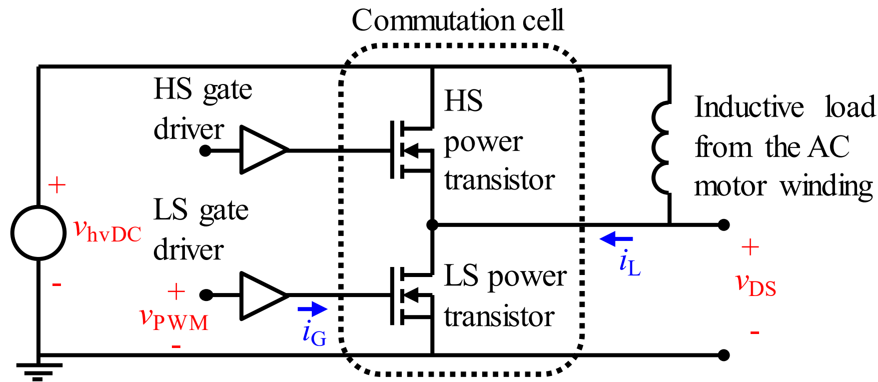


Figure 1.12. Commutation cell to control the current of one winding in the electric motor. The power transistor represented can be a Si or SiC MOSFET, IGBT or GaN HEMT.

A simplified switching transient is explained using **Figure 1.13** below where only the LS (low side) transistor and GD of **Figure 1.12** is represented. The circuit shows the names of the variables and represents the turn-on and off transients of a power device. The transient behavior is qualitatively similar if the transistor is made with silicon (Si), silicon carbide (SiC) or gallium nitride (GaN), if the power devices are of the same unipolar type (i.e. only majority carriers with almost no recovery phase).

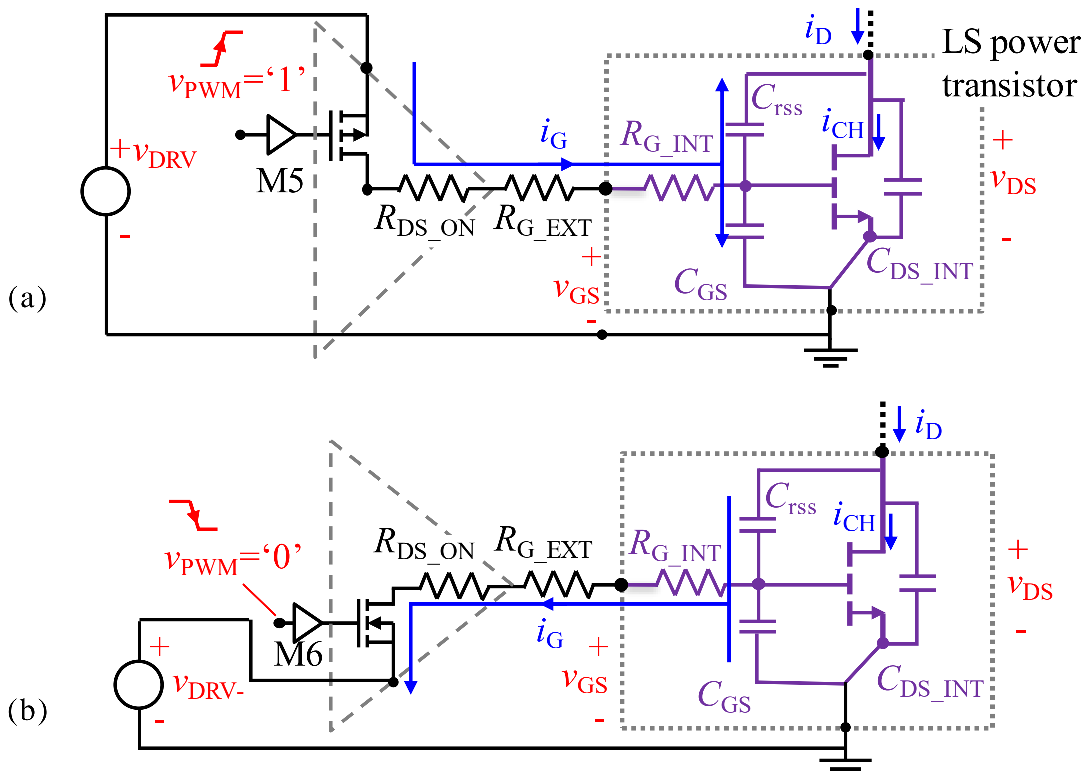


Figure 1.13. Schematic of the LS power transistor switching (a) ON and (b) OFF.

Notice in **Figure 1.13** that three values of resistance will limit the gate current (i_G). The R_{DS_ON} of the last stage buffer of the driver or also called main driver stage, will be in series with 2 other resistances. These resistances are labelled as R_{G_EXT} and $R_{G_INT.}$ R_{G_EXT} is usually a discrete resistance added between the output of the GD and the power device to limit the gate peak current (i_G), the dv_{DS}/dt and the di_D/dt in the transistors. R_{G_INT} can be an added component inside a power transistor or power module or can be just the equivalent intrinsic resistance of gate terminals on the transistor die.

$$R_G = R_{DS_ON} + R_{G_EXT} + R_{G_INT} \quad (1.1)$$

Several previous works explain with equations the turn-on and off transients for silicon IGBT and for SiC MOSFET devices. The PhD thesis of Timothé Rossignol [27], previously done at LAPLACE lab, detailed the switching behavior for SiC MOSFETs. Also the PhD thesis of Yanick Lobsiger at ETH in Zurich detailed the behavior of an IGBT power device [28].

The simplified qualitative waveforms for one power transistor (**Figure 1.13**) are presented in **Figure 1.14**. One entire turn-on event (**Figure 1.14** (a)) is separated in, at least, four time intervals determined by time instants t_0, t_1, t_2, t_3 and t_4. More accurate models can split it up into 7 different phases but in this work the focus is the controllability of dv/dt independently from di/dt. Therefore, considering four time intervals is a fair analysis for this work. For the turn-off sequence (**Figure 1.14** (b)), it is split up in another four intervals determined by time instants t_5, t_6, t_7, t_8 and t_9. In the case of turn-off, two modes can be separated, for high load current when there is a current in the channel of the power device (i_{CH}>0 A) and for low load current (i_{CH}=0 A). The behavior during these time intervals will be explained below.

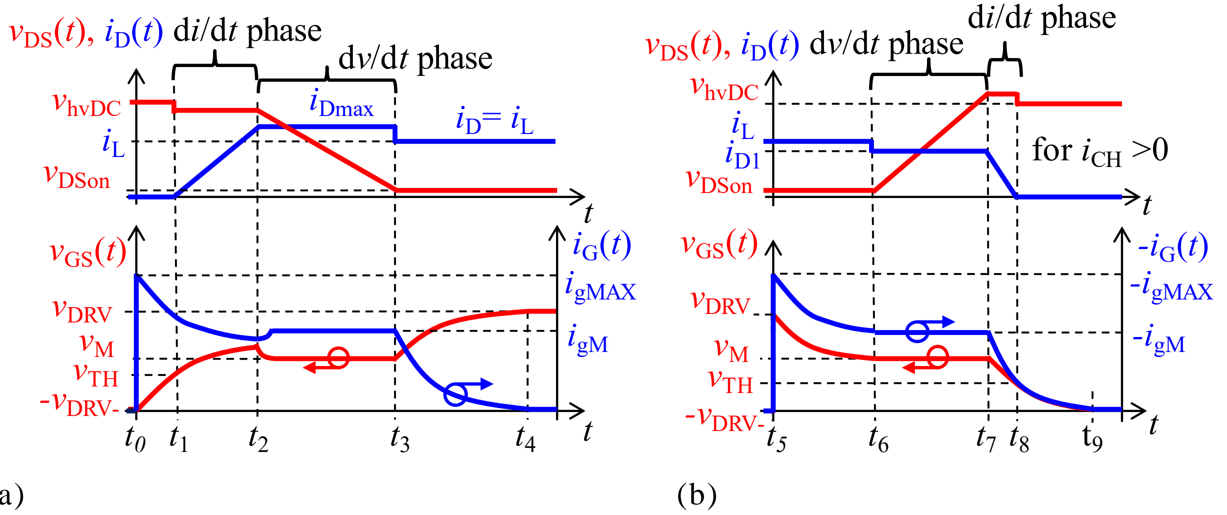


Figure 1.14. Simplified waveforms of a power device assuming inductive load during the (a) turn-on and (b) turn-off (with i_{CH}>0) switching transients. Typical behavior when a voltage step is applied to the gate of a power device with total series resistance R_G.

The propagation delay phase ($t_0 < t < t_1$).

When M5 is turned-on inside the GD, (**Figure 1.13** (a) and **Figure 1.14** (a)) v_{DRV} voltage is applied to the output of the gate drive and a current i_G starts to charge the gate of the power transistor. The power device's threshold voltage (v_{TH}) is still not achieved, therefore the current in the power transistor is still very close to zero. The power transistor is off and the v_{GS} raises until it reaches the threshold value. The derivative of v_{GS} depends on the current supplied by the driver (i_G) and the equivalent input capacitance of the component $C_{iss_{OFF}}$ when it is still in off-state (1.2). This capacitance depends on the gate oxide capacitance (C_{OX}) in series with the space charge region capacitance (C_{SCR}) plus the overlap capacitance between the gate and doped areas (C_{OV}), as shown in (1.3).

$$\frac{dv_{GS}}{dt} = \frac{i_G}{C_{iss_{OFF}}} \tag{1.2}$$

$$C_{iss_{OFF}} = \frac{C_{OX}C_{SCR}}{C_{OX} + C_{SCR}} + 2C_{OV} \tag{1.3}$$

The di/dt phase ($t_1 < t < t_2$).

The threshold value is achieved and a current (i_{CH}) starts to increase in the power device. The v_{GS} keeps increasing at a rate (1.4) dependent on the different capacitance viewed from the driver ($C_{iss_{SAT}}$). The channel starts to conduct, and the

transistor is in the saturated region. When this interval ends, the entire load current is flowing through the low side transistor (LS).

$$\frac{\mathrm{d}v_{\mathrm{GS}}}{\mathrm{d}t} = \frac{i_{\mathrm{G}}}{C_{\mathrm{iss_{SAT}}}} \tag{1.4}$$

In this phase, the power transistor works in saturation region and the channel has a pinched off physical form. Regarding the drain current, for high levels of current, its expression can be linearized using a constant transconductance value (g_{fs}).

$$C_{\mathrm{iss_{SAT}}} = \sim 2/3C_{\mathrm{OX}} + 2C_{\mathrm{OV}} \tag{1.5}$$

$$i_{\mathrm{D}}(t) = g_{\mathrm{fs}} \cdot (v_{\mathrm{GS}}(t) - v_{\mathrm{TH}}) \tag{1.6}$$

In this phase, due to the parasitic inductance of the power loop of the switching leg (in **Figure 1.12**), a voltage drop Δv_{DS} is observed in $v_{\mathrm{DS}}(t)$ voltage, as shown in (1.7).

$$\Delta v_{\mathrm{DS}}(t) = (L_{\mathrm{S}} + L_{\mathrm{D}}) \cdot \frac{\mathrm{d}i_{\mathrm{D}}}{\mathrm{d}t} \tag{1.7}$$

$$v_{\mathrm{DS}}(t) = v_{\mathrm{hvDC}} - (L_{\mathrm{S}} + L_{\mathrm{D}}) \cdot \frac{\mathrm{d}i_{\mathrm{D}}(t)}{\mathrm{d}t} \tag{1.8}$$

where L_S is the parasitic source inductor of the power switch and L_D represents the contribution of all the parasitic inductors involved in the switching loop.

By solving equation (1.8), a condition with underdamping or overdamping can be obtained [29], depending on the values of total impedance seen in series with the GD and power device (R_{G}), the capacitance values C_{rss}, C_{GS}, transconductance g_{fs} and parasitic inductances L_{D} and L_{S}. In the case of underdamping behavior, the derivative of i_{D} is given by:

$$\frac{\mathrm{d}i_{\mathrm{D}}}{\mathrm{d}t} = \frac{g_{\mathrm{fs}} \cdot (v_{\mathrm{GS}}(t) - v_{\mathrm{TH}})}{g_{\mathrm{fs}} \cdot L_{\mathrm{S}} + R_G \cdot C_{\mathrm{SAT}}} \tag{1.9}$$

where C_{SAT} is the input capacitance during this time interval.

At the end of the di/dt phase, the body diode of the symmetrical device (HS device) will be blocked and a reverse recovery current is added to the channel current (i_{CH}) of the main device (LS device) so the value i_{Dmax} is achieved.

The maximum value of drain current achieved depends on the HS diode reverse recovery-like ($i_{\mathrm{rr_max}}$) as explained in details in [29]. The term recovery-like

is because it can either be in the GaN HS body diode or in a discrete Schottky diode for the SiC application.

$$i_{\mathrm{Dmax}} = i_{\mathrm{L}} + i_{\mathrm{rr_max}} + C_{\mathrm{DS_INT}} \left| \frac{\mathrm{d}v_{\mathrm{DS}}}{\mathrm{d}t} \right| \tag{1.10}$$

It will be explained in a latter subsection that the proposed d*v*/d*t* control technique in this manuscript will not affect the d*i*/d*t*. The d*i*/d*t* will be set to a high value by choosing a low value of $R_{\mathrm{G_EXT}}$ to obtain low switching losses. The proposed d*v*/d*t* control technique developed in this manuscript could be easily adapted to control the d*i*/d*t* also by using a parasitic source inductance of a power device as proposed in 2003 by [30].

Although it will not be developed in this work, controlling the d*i*/d*t* may be interesting because it directly affects the reverse recovery process of a diode in a switching cell [31]. Also, several academic works focus in developing power device structures, diodes and transistors with high d*i*/d*t* capability. [32]

The d*i*/d*t* also causes overvoltage ($v_{\mathrm{L}} = L \cdot \mathrm{d}i/\mathrm{d}t$), due to the presence of parasitic inductances of the circuit, which can be destructive to the power devices. Thus, it becomes important to be able to control or at least to limit the d*i*/d*t*. In the power converter system design perspective, to be able to control the d*i*/d*t* can also be an advantageous degree of freedom to achieve a homogeneous distribution of the currents of parallelized chips with separate drivers during switching.

The d*v*/d*t* phase ($t_2 < t < t_3$).

After the current is switched, the voltage v_{DS} starts to drop in the power device. During the d*v*/d*t* phase, the gate voltage v_{GS} of the power device remains approximatively constant at Miller's plateau voltage value (v_{M}) because v_{DS} is decreasing from its nominal DC level v_{hvDC} until almost zero. Equations which define the main current and voltage levels of this phase are shown below.

$$i_{\mathrm{CH}} = i_{\mathrm{L}} + i_{\mathrm{C_{rss}}} + i_{\mathrm{C_{DS}}} \tag{1.11}$$

$$i_{\mathrm{CH}} = i_{\mathrm{L}} + C_{\mathrm{rss}} \cdot \frac{\mathrm{d}v_{\mathrm{GD}}}{\mathrm{d}t} + C_{\mathrm{DS_INT}} \cdot \left| \frac{\mathrm{d}v_{\mathrm{DS}}}{\mathrm{d}t} \right| \tag{1.12}$$

$$v_{\mathrm{M}} \approx v_{\mathrm{TH}} + \frac{i_{\mathrm{CH}}}{g_{\mathrm{fs}}} \tag{1.13}$$

where i_{CH} is the current in the channel of the power device, i_{L} the current in the inductive load L, $i_{\mathrm{C_{rss}}}$ the current in the reverse transfer capacitance and $i_{\mathrm{C_{DS}}}$ the current in the drain-to-source intrinsic capacitance of the power device.

In the dv/dt phase, the variation for v_{GS} is negligible $\left(\frac{\mathrm{d}v_{\mathrm{GS}}}{\mathrm{d}t} \cong 0\right)$, therefore the variation in v_{GD} is equal to the variation in v_{DS} $\left(\frac{\mathrm{d}v_{\mathrm{GD}}}{\mathrm{d}t} = -\frac{\mathrm{d}v_{\mathrm{DS}}}{\mathrm{d}t}\right)$. Solving (1.12) for $\mathrm{d}v_{\mathrm{DS}}/\mathrm{d}t$, we obtain:

$$\frac{\mathrm{d}v_{\mathrm{DS}}}{\mathrm{d}t} \simeq -\frac{i_{\mathrm{G}}}{C_{\mathrm{rss}}} = -\frac{(v_{\mathrm{DRV}} - v_{\mathrm{M}})}{(R_{\mathrm{DS_ON}} + R_{\mathrm{G_EXT}}) \cdot C_{\mathrm{rss}}} \tag{1.14}$$

Notice that the dv_{DS}/dt value will depend on the current charging the gate of the power device and this current can be controlled with a voltage value applied to the gate, an impedance, with $R_{\mathrm{G_EXT}}$ or with a current (a transistor in saturation represented by a current source)

In this phase, the channel of the power transistor is still pinched-off, however the capacitance seen in the gate of the power device is only the overlap capacitance that is between the gate and drain terminals:

$$C_{\mathrm{rss}} = C_{\mathrm{OV}} \tag{1.15}$$

In the book "Power MOSFETs: Theory and Applications" from Grant, 1989 [33], an expression for the dv/dt is given for inductive only load, for the switch-on instant, as shown below.

$$\frac{\mathrm{d}v_{\mathrm{DS}}}{\mathrm{d}t} = \frac{-g_{\mathrm{fs}}(v_{\mathrm{DRV}} - v_{\mathrm{TH}}) + i_{\mathrm{L}}}{\left(1 + g_{\mathrm{fs}}(R_{\mathrm{DS_ON}} + R_{\mathrm{G_EXT}})\right)C_{\mathrm{rss}}} \simeq \frac{(v_{\mathrm{DRV}} - v_{\mathrm{M}})}{\left(R_{\mathrm{DS_ON}} + R_{\mathrm{G_EXT}}\right)C_{\mathrm{rss}}} \tag{1.16}$$

Another similar way to express the equation (1.14) is given by Baliga 2008 [34]:

$$\left|\frac{\mathrm{d}v_{\mathrm{DS}}}{\mathrm{d}t}\right| = \left|\frac{(v_{\mathrm{DRV}} - v_{\mathrm{M}})}{\left(R_{\mathrm{DS_ON}} + R_{\mathrm{G_EXT}}\right)C_{\mathrm{rss}}}\right| \tag{1.17}$$

The final gate-charging phase ($t_3 < t < t_4$).

In this step v_{GS} raises from the constant Miller value to the positive value of the driver (v_{DRV}). The v_{GS} in this part has an exponential form. In this phase, the gate voltage continues to increase with the consequent reduction in R_{dsON} of the power device.

$$\frac{\mathrm{d}v_{\mathrm{GS}}}{\mathrm{d}t} = \frac{i_{\mathrm{G}}}{C_{\mathrm{iss_{ON}}}} \tag{1.18}$$

In this phase, the channel is not pinched-off, the capacitance seen in the gate of the power device is expressed by:

$$C_{\mathrm{iss_{ON}}} = \sim C_{\mathrm{OX}} + 2C_{\mathrm{OV}} \quad (1.19)$$

During the turn-off switching transients:

The propagation delay phase ($t_5 < t < t_6$).

When M5 is off and M6 is turned-on inside the GD (**Figure 1.13** (a) and **Figure 1.14** (a)), $v_{\mathrm{DRV-}}$ voltage is applied to the output of the GD and a current i_G starts to discharge the gate of the power device. A RC circuit is formed and the time-constant associated to it is composed by the total resistance in series ($R_{\mathrm{DS_ON}}$ of the last stage buffer added with $R_{\mathrm{G_EXT}}$ and $R_{\mathrm{G_INT}}$) with the total capacitance (C_{GS}+C_{rss}) [29].

The dv/dt phase ($t_6 < t < t_7$).

At t_6 the power device is in the ohmic region. The voltage starts to rise between drain and source in the power device. During the dv/dt phase, similarly to the turn-on, the gate of the power device remains approximatively constant at Miller's plateau voltage value (v_M). The i_D current drops from i_L to i_{D1} because the load current is shared so it charges the $C_{\mathrm{DS_INT}}$ of the LS transistor and discharge the $C_{\mathrm{DS_INT}}$ of the HS transistor. Similarly to the switch-on, for high load current, the dv/dt depends on the current i_G and only the capacitance C_{rss}. This analysis is made in the case of high load current i_L. In case of low load current, the dv/dt will depend only on the discharge rate of the output capacitances $C_{\mathrm{DS_INT}}$ by the load current.

The di/dt phase ($t_7 < t < t_8$).

After the voltage is switched on, the drain current starts to drop in the power device. A drain-to-source voltage overshoot is expected in this phase associated to parasitic inductances in the power loop.

The final gate discharging phase ($t_8 < t < t_9$).

In this phase, v_{GS} reduces from v_{TH} to 0 V or the negative voltage the GD is connected to. The more negative this voltage, the more a false turn-on by crosstalk and coupling capacitance is prevented when the symmetrical opposite transistor switches on [35] [36].

1.3.2 Measurements of switching waveforms

For system level reliability of GaN devices, different companies use different topologies for measurements [37]. In this paper, TSMC™ proposes a half bridge (HB) with RC load instead of the classical RL load used from Panasonic™, or just inductive load like Texas Instruments™ or a boost topology like Transphorm™.

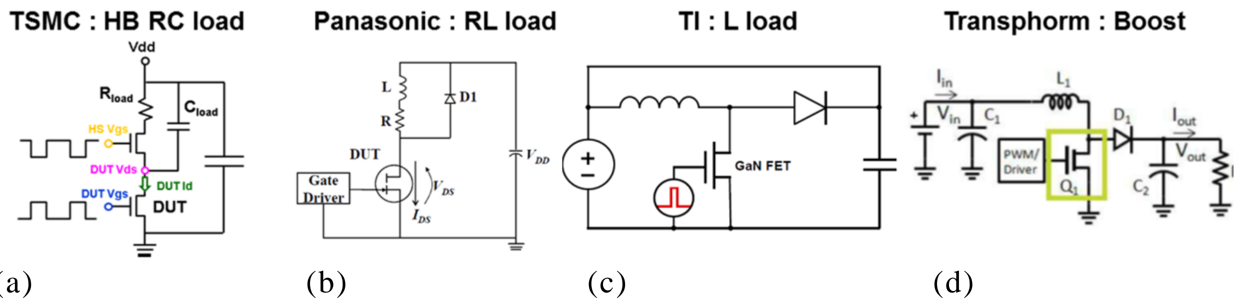


Figure 1.15. Different topologies used for reliability tests of GaN transistors, [37].

In order to measure switching waveforms and/or switching energy, different methods can be used. The most classical one is the double pulse method. Another improved method without intrusive current measurement devices is the opposition method [38]. Thermal methods can also be used to measure switching losses in GaN and SiC power devices. [39].

Using the double pulse method in **Figure 1.15** (c), measurements of dv/dt as a function of i_L are presented. Those measurements (**Figure 1.16**) are from the PhD thesis by Thimothé Rossignol [27]. The power device is a SiC MOSFET CMF20120D switching i_L=5.5 A with v_{hvDC}=600 V, -3.6 V<v_{GS}<22 V, with a gate driver capable of providing up to i_{gMAX}=14 A. Those measurements validate the analytical model developed in [27].

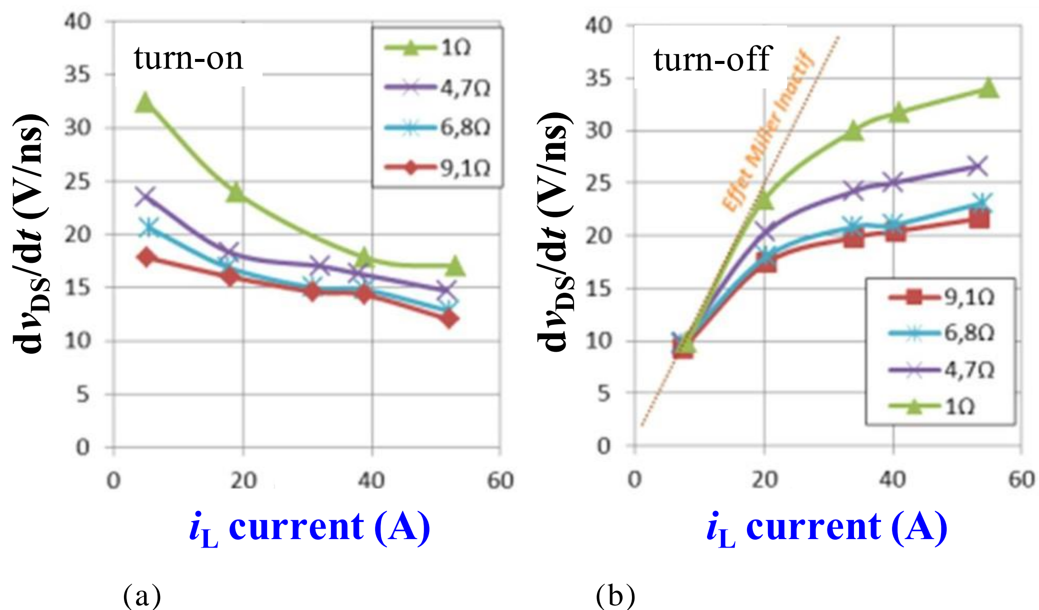


Figure 1.16. Measured dv/dt as a function of load current with different external resistor R_{G_EXT} values for (a) turn-on and (b) turn-off transients. From the PhD thesis by Timothé Rossignol [27].

Notice that for the turn-off event, for a wide range of load current values, the dv/dt cannot be controlled by the gate driver and only the C_{oss} value of the power device and all the parasitic capacitance added in parallel by the PCB between drain and source of the DUT will impose the dv/dt value. This is one of the reasons why the proposed method in the present thesis is applied only to control the dv/dt at the turn-on event.

Measurements made in IRT-Saint Exupéry for characterization of SiC MOSFET and GaN HEMT uses the opposition method. This opposition method has been proposed for power devices in early 2000, as in [40]. Example of experimental values are shown in **Figure 1.17**. The opposition method has the advantage of not needing to precisely measure the current i_D in the power device with a high bandwidth method in order to measure switching energy lost during turn-on and off events [38].

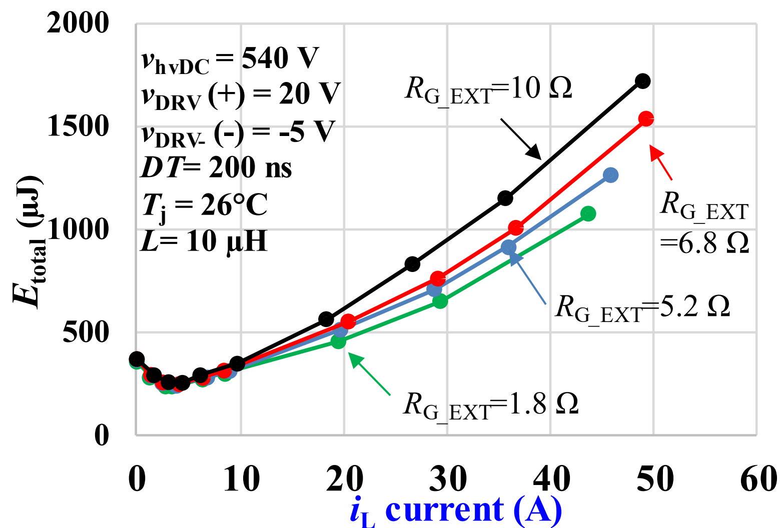


Figure 1.17. Total switching energy at turn-on for different voltages when changing the load current (measured at IRT-SE) The power device is a 2nd generation SiC MOSFET [41].

1.4 Overview of commercially available gate drivers

1.4.1 Recommended gate drivers (GD) for WBG power devices.

To take advantage of the high efficiency provided by WBG transistors, it is recommended to choose a GD with high current capability. With a higher current capability, the propagation delay can be reduced, the switching losses and the self-turn-on failure probability minimized. **Table 1.1** compares main specifications of

some of the GD's recommended for WGB transistors. The gate driver from Infineon in this table has a galvanic isolation by integrated coreless transformer technology. The Silicon Labs one has isolation up to 5 kV by opto-coupling.

TABLE 1.1. COMPARISON OF SOME COMMERCIAL GATE DRIVERS FOR WBG TRANSISTORS

	Silicon Labs SI8261BAC-C-IS	TI UCC27525	Infineon IED020I12	IXYS IXD614
max output current (i_{gMAX})	4 A	5 A	2.4 A	14 A
output voltage (v_{DRV})	0/30 V	-4.5/18 V	-12/20 V	-4.5/35 V
propagation delay t_p	40ns CL= 200 pF	17ns CL= 1.8 nF	160ns CL= 100 pF	50ns CL= 15 nF
rise and fall time t_r/t_f	5.5/8.5 ns	7/6 ns	30/50 ns	25/18 ns
max temperature (T_{MAX})	125 °C	125 °C	150 °C	125 °C
year of releasing	2011	2015	2017	2017

Other companies manufacturing GD's specifically for WGB power transistors are: uPI Semiconductor Corp., Microchip Technology Inc., Renesas Electronics and pSemi (a Murata Company).

The GDs presented in **Table 1.1** can use only the classical methods to control dv/dt and di/dt by changing R_{G_EXT} or external C_{GD} or C_{GS} capacitors.

1.4.2 Gate drivers with d*v*/d*t* control

GD's manufacturers are implementing dv/dt controls with different strategies in some of their products. However, few information is provided concerning the dv/dt control technique for each product.

Texas Instruments™ produces the LMG3410, which integrates in the same package a normally ON GaN power device and a silicon GD, which also integrates the low voltage power MOSFET in the cascade-like connection. This circuit has an adjustable slew rate of GaN transistor from 25 to 100 V/ns. However, this circuit offers only tunable gate current capability, which affects both the dv/dt and di/dt and does not offer an independent dv/dt and di/dt control. This dv/dt is adjusted with an external gate resistor (from 17 kΩ to 150 kΩ) that is not between the output of the power device and the gate.

Infineon™ produces the GD 1EDI20I12SV for IGBT with slew rate control. The gate current can be controlled with 11 levels of current making a controllability of dv/dt from 0.5 to 3.5V/ns.

Toshiba™ has the GD for MOSFET power device called TCK401G. It contains a slew rate control logic and active Miller clamp. It is recommended for

battery charge applications up to 28V. The output current (i_{gMAX}) of this driver is around 40 µA.

Fairchild has a product for slow switching PMOSFETs called FDG901D. It can control the slew rate on Si MOSFETs from 0.0003 to 0.162 V/µs. This device is slow because it is designed to limit the inrush current in battery switching applications with high capacitance loads.

Linear Technology™ has a product which is a DC/DC controller with slew rate control named LT1738. It provides a maximum sink and source current of 0.3 A with a slew rate of around 20 V/µs. In this product, current and voltage slew rates can be independently set to optimize harmonic content of the switching waveforms vs efficiency. The slew rate control is made with an external FET. The dv/dt sensing is made with a sensing capacitor (recommended 5 pF) for under 25 V operation, 2.5 pF for 50 V and 1 pF for 100 V.

Another example of advanced GD for IGBT and SiC is the NXP MC33GD3100 ASIL C/D. It is capable to provide up to 15 A peak gate current with a separated source and sink output to better control the dv/dt and di/dt. It has a common-mode transient immunity (CMTI) above 100 V/ns. There is also an active Miller clamp to prevent self-turn-on issue caused by crosstalk. It has junction and galvanic isolation up to 8 kV.

GD described in this section does not control the dv/dt in closed-loop system with high bandwidth enough to control WBG power devices. Because they do not control dv/dt from di/dt independently, they don't achieve the best trade-off possible between switching speed (or EMI) and switching energy (E_{ON}) as it will be discussed latter in this work.

1.5 Benefits of Active Gate Drivers for power transistors

There are many advantages of using an Active Gate Driver to improve the performance of power devices. One advantage is achieving independent control of dv/dt compared to the di/dt to improve the trade-off between the switching losses and the dv/dt. This is explained in section 1.6.4.

Previous studies [42], shows all the possible way to achieve dv/dt and di/dt control for each switching event (turn-on or turn-off) of Silicon IGBT power devices. This subchapter study will show the recently published academic work to drive WBG power devices in GaN and SiC as well as for Silicon IGBT in the last years.

Controlling the gate impedance ($R_{G_EXT_ON}$ and $R_{G_EXT_OFF}$), voltage (v_{DRV}) or current (i_G) of the power device, the output waveform of the voltage v_{DS} or current i_D of a power device can be controlled, see **Figure 1.18**.

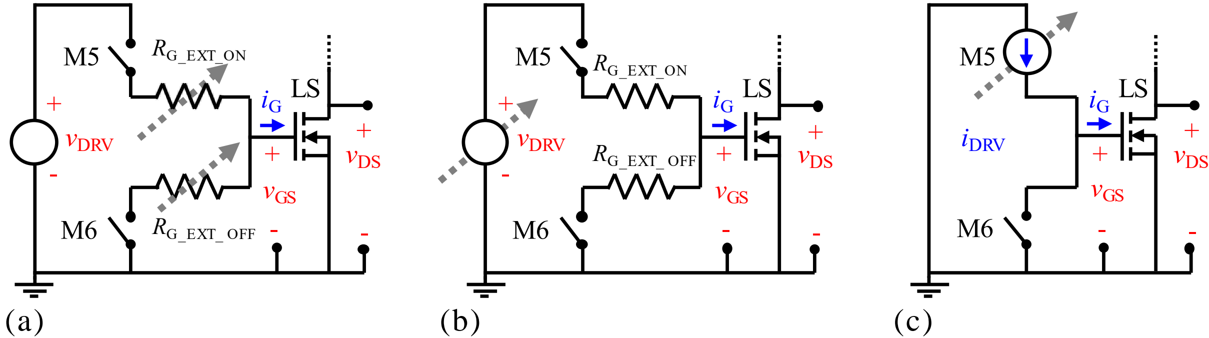


Figure 1.18. Three similar methods to control the dv/dt or the di/dt of the LS power device. The current i_G during the Miller's plateau can be affected by changing the (a) external gate resistor, (b) voltage value or (c) current value.

For example, by increasing the value of the external resistance $R_{G_EXT_ON}$, the di/dt and the dv/dt will decrease as shown in **Figure 1.19**.

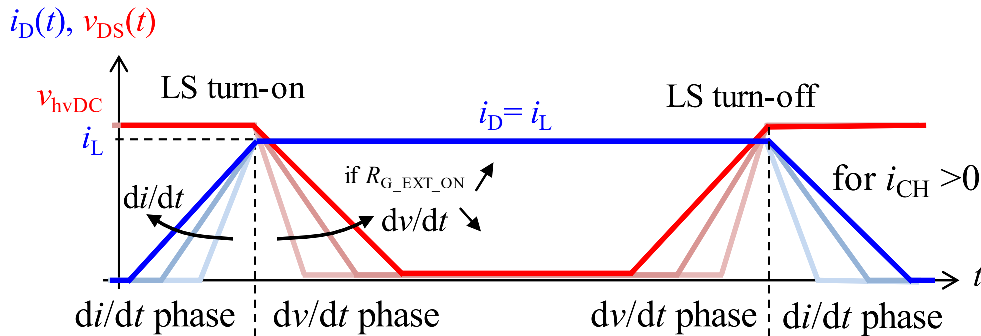


Figure 1.19. Increasing the value of $R_{G_EXT_ON}$ will decrease both the dv/dt and the di/dt. The voltage and current waveforms in the LS power device are simplified for this example. Only valid for high values of load current, i_{CH}>0 A for the turn-off.

One other example of method to control the impedance between the output of the GD and the gate of the power device is by using a segmented output driver (**Figure 1.20**).

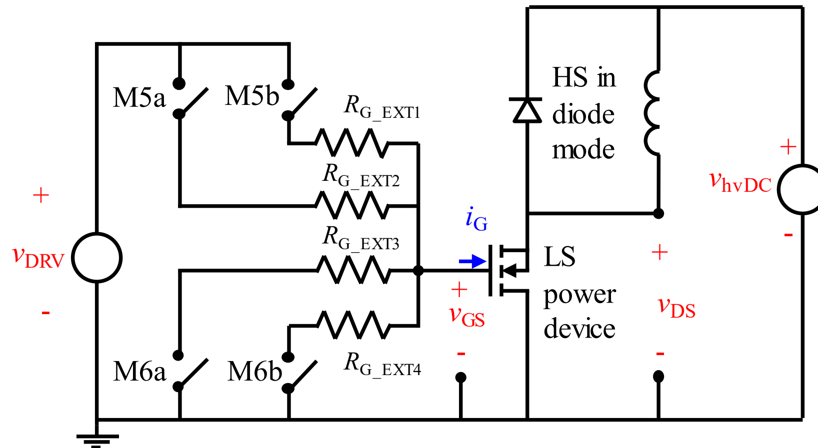


Figure 1.20. A segmented output topology. The i_G current is controlled by the impedance and the number of transistors in parallel.

Another similar segmented output strategy to control the switching speed is, instead of using different values of R_{G_EXT}, to use transistors in parallel in the output of the GD with different values of saturation current (i_{Dsat}) [43]. By enabling more or less CMOS transistors in parallel in the output of the GD, the value of the current i_G can be controlled and therefore the dv/dt and the di/dt.

In order to improve efficiency of a system, one could use a similar strategy of segmented topology but applied to power devices. Paralleling smaller power transistors combining with smart gate driving and individual die temperature estimation can lead to less switching losses and higher power density of power modules [44].

1.5.1 Problems caused by high d*v*/d*t* values

The correct control of dv/dt can be beneficial to achieve the lowest value of switching losses and therefore the highest efficiency of the systems. However, high values of dv/dt can cause several issues for an engineer designing power converters, especially when using WBG devices. Issues caused by high dv/dt values are listed below.

- Crosstalk issues, or also called self-turn-on failure [45], dv/dt induced turn-on [46], or secondary turn-on [47]. It happens when the opposite transistor in a commutation cell can turn-on unintentionally causing a shoot-through current. A high dv/dt value in the switching node (node called v_{DS} in this manuscript) will make a current flow through the Miller capacitor C_{rss} of the low side (LS) power device. This current will provide some charges to the gate of the LS

device. If these electrical charges are sufficiently high, it can turn-on the LS power transistor while attempting to turn-on the HS transistor. This can cause an unintended extra power consumption or even damage or destruct the switching leg. To prevent this failure, the engineer can choose to use the active Miller clamp technique, a lower R_{G_EXT} value or a GD with higher sink current capability. All these methods provide less resistive path to the current passing through C_{rss} to ground node. Using negative voltage in the GD supply will also reduce this undesired effect. **Figure 1.21** illustrates this issue.

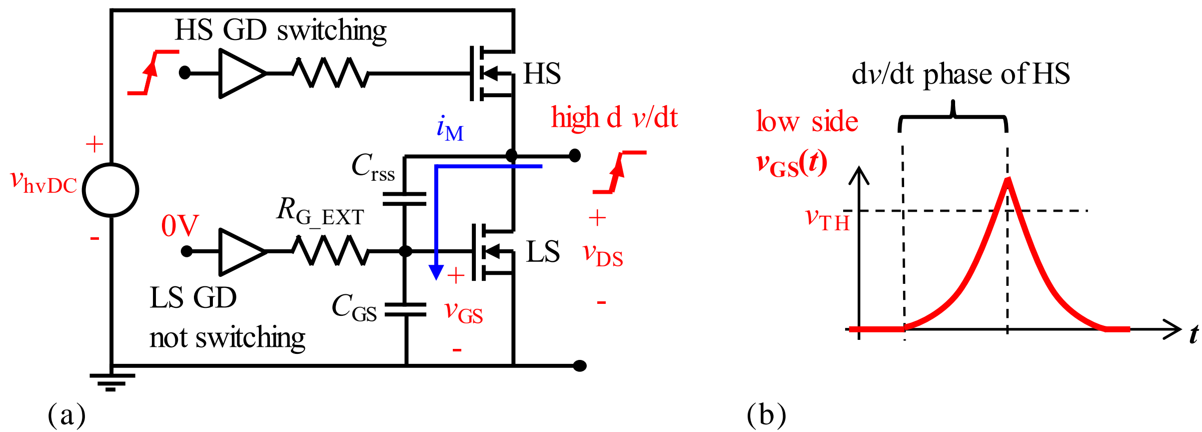


Figure 1.21. Self-turn-on failure caused by crosstalk from capacitive coupling and high dv/dt. (a) Circuit illustration and (b) v_{GS} voltage rising with the dv/dt phase of the symmetrical device. If the voltage rising is above v_{TH}, a self-turn-on failure will happen in the switching cell.

- dv/dt related to v_{GS} safe operation area (SOA). By capacitance coupling, high values of dv/dt can cause spikes in the v_{GS} voltage that can make the power device operate outside SOA and consequently damage the power device [48].
- CMTI (common-mode transient immunity) isolation of GD's has a maximum dv/dt (previously below 50 V/ns, with solutions now available above 100 V/ns). Several research works focus on integrating CMR (common-mode rejection) transformers on-chip. CMR transformers embedded on-chip can withstand dv/dt of 50 V/ns without disturbing the command signal [49].
- EMI (*Electromagnetic interference*) issues: different systems, e.g. (aeronautic standards) impose low values of differential and common-mode current to flow in the input and output of the converters [11]. The higher the dv/dt, the higher these currents and the bulkier the dv/dt filter needs to be. Standards in aeronautics impose a maximum dBμA of conducted common-mode and differential-mode currents at a large frequency range. These currents at high

frequency range are directly proportional to the d*v*/d*t* value of voltage in the switching node [50].

- Overvoltage in motors connected to power inverters. High d*v*/d*t* values in the output of power converters connected to motor through long cables can produce high overvoltage in motor terminals. This overvoltage can cause partial discharge (see **Figure 1.22**) in the insulator material of motor windings which can reduce the lifetime of these motors [51]. In order to mitigate this problem, d*v*/d*t* filters can be added to the output of power inverters. Consequently, the lower the d*v*/d*t*, the smaller and more lightweight the filters.

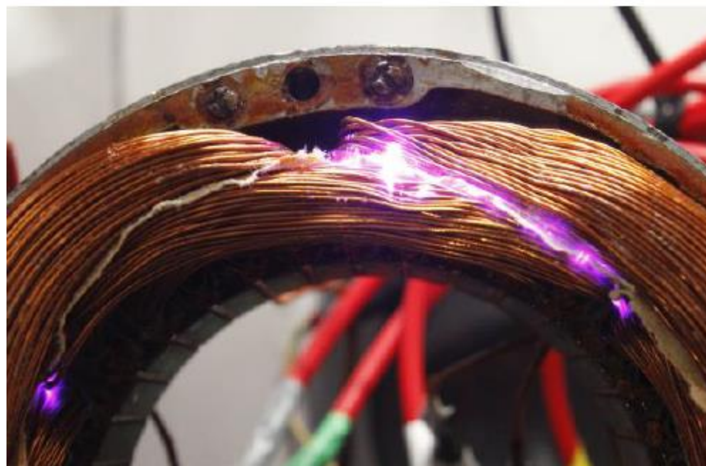


Figure 1.22. Partial discharge in electric machine winding is one problem caused by overvoltage in the winding. The overvoltage in the electric machine winding is related to the d*v*/d*t* value during switching transients of a power device used in inverters for motor speed control.

- Voltage balancing during switching transient of series-connected transistors. Power devices in series need to have the same switching speed to avoid that only one device holds the whole DC bus voltage (v_{hvHC}) during a switching transient [52] [53] [54] [55].

1.5.2 Gate driver techniques for d*v*/d*t* and d*i*/d*t* control

Before 2015, the academic work regarding switching control for IGBT (d*v*/d*t* and d*i*/d*t* control) has been classified into the three types: passive, active open-loop and active closed-loop by [42], as shown in **Figure 1.23**.

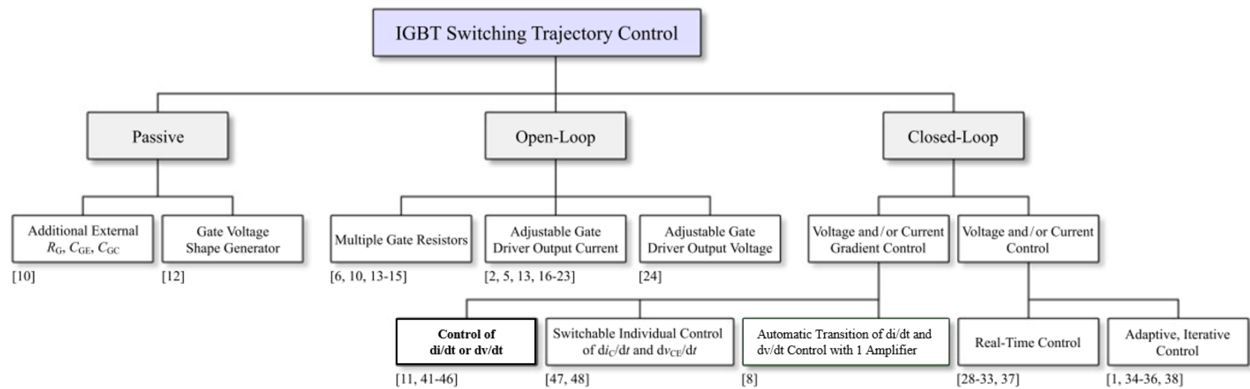


Figure 1.23. Classification of GD's concepts enabling a shaping of the IGBT's switching trajectories subdivided into passive, open-loop and closed-loop types. Published in [42] in 2015.

After the year 2015, using the same classification in three main groups, the following academic articles have been published (**Figure 1.24**). These different techniques will be explained in the following sub-sections.

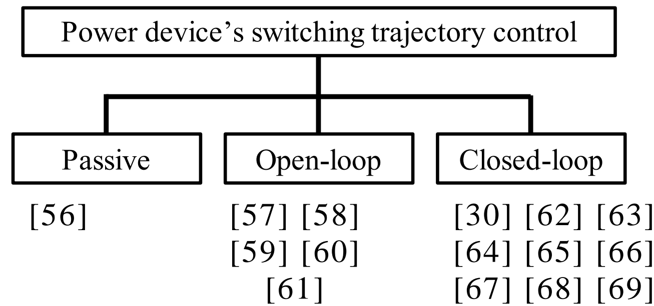


Figure 1.24. Academic papers published after 2015 classified into three types of gate driving strategies. In chronological order for each type.

These academic publications can also be classified by technology of power device as shown in **Figure 1.25**.

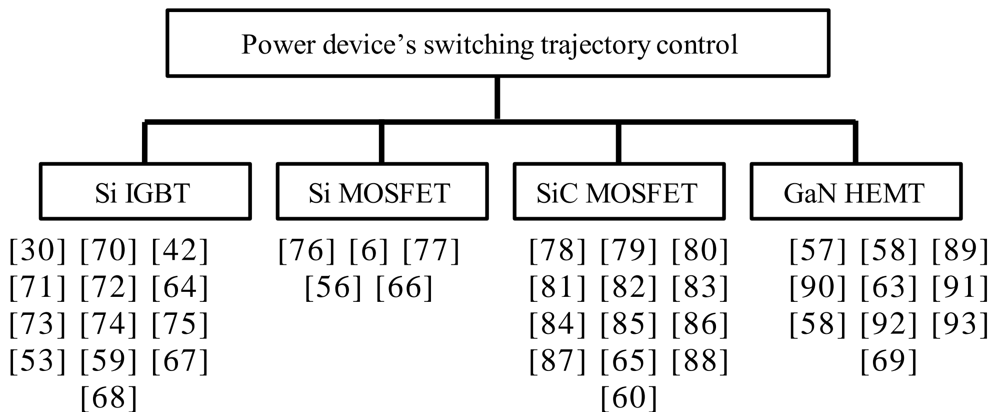


Figure 1.25. Research work published about AGD classified by type of power device. In chronological order for each device.

1.6 State-of-the-art of AGD in academic publications

A table comparing the latest publications regarding AGD can be seen in the **Table 1.2** below. Parameters regarding the dv/dt, di/dt, v_{hvDC}, the type and technology are included to be compared. In this table it is possible to see WBG devices with faster switching. Some papers with GD integrated in CMOS technology do not report results measured with the full bus voltage they were designed to operate and only v_{GS} signals.

Table 1.2. dv/dt control state-of-the-art publications after 2014 except for one.

Ref	Year	Type	Turn-on (V/ns)	Turn-off (V/ns)	di/dt control	v_{hvDC} (V)	Integrated in
[30]	2001	IGBT	3	4.1	Y	600	discrete
[57]	2015	GaN	20	N	N	200	140 nm
[63]	2016	GaN	27	N	N	300	discrete
[64]	2017	IGBT	0.7	0.27	Y	600	discrete
[58]	2018	GaN	4	Y	Y	12	?
[56]	2018	GaN	8	N	N	400	1.45 µm
[94]	2018	GaN	N	33	N	40	350 nm
[93]	2018	GaN	sim	sim	N	sim	180 nm
[65]	2019	SiC	50	15	Y	400	discrete
[59]	2019	IGBT	5	1.2	Y	600	discrete
[60]	2019	SiC	37	Y	N	300	discrete
[66]	2019	Si	4.5	N	N	300	130 nm
[67]	2019	IGBT	N	N	N	600	discrete
[68]	2020	IGBT	N	1.75	Y	700	discrete
[48]	2020	GaN	Y	Y	Y	?	180 nm
[69]	2020	GaN	175	N	N	50 and 400	180 nm

1.6.1 Passive techniques

Passive methods are simple, and a system engineer can chose to set the dv/dt and di/dt values by choosing the external components R_{G_EXT}, or adding external components C_{GD_EXT} and C_{GS_EXT} as shown in **Figure 1.26**.

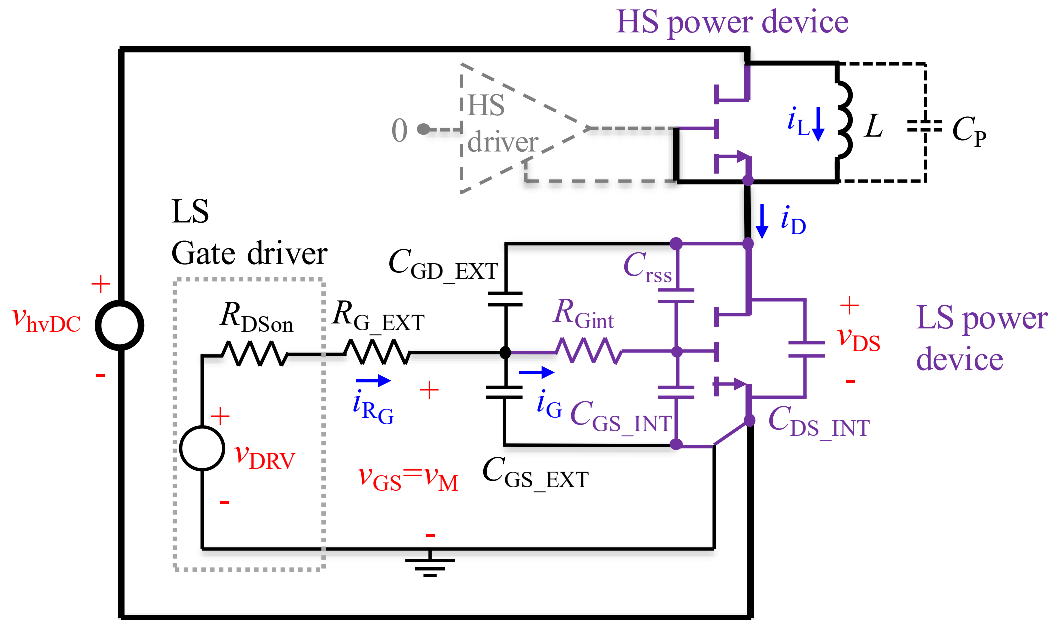


Figure 1.26. Schematic of a switching leg with focus to the methods to control the switching trajectory. The LS (low side) WBG transistor can be controlled by different elements (R_{G_EXT}, C_{GD_EXT} and C_{GS_EXT}) that can affect the gate charge speed during different moments of a switching transient.

Another passive method to control the switching is to change either the voltage, current or impedance of the driver in a time scale of a switching event. For example, if only during the dv/dt phase the current going to the gate of the power device is lowered, the dv/dt reduces without affect the di/dt. If the values of voltage v_{DRV_1}, v_{DRV_2}, v_{DRV_3} and v_{DRV_4} (or current or impedance) are fixed, not adjustable, it is a passive control method.

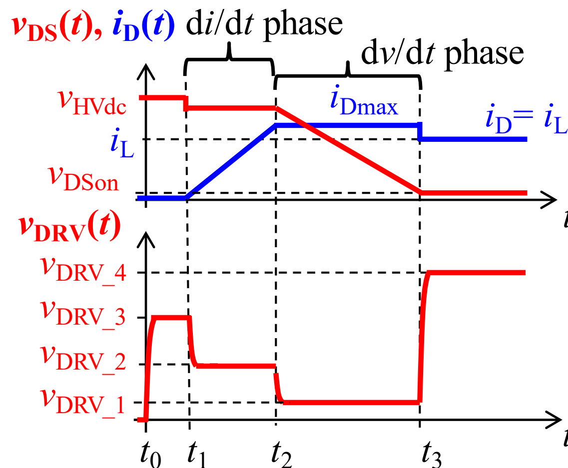


Figure 1.27. Changing the value of voltage provided to the gate of a power device in the time scale of a switching event.

1.6.2 Active open-loop techniques

If these values v_{DRV_1}, v_{DRV_2}, v_{DRV_3} and v_{DRV_4} (defined in **Figure 1.27**) can be controlled and changed, the control method is classified as active open-loop system, as previously explained and documented in [42]. Notice that the current and voltage waveform depends on the gate current i_G. This gate current can be controlled by either a voltage shape applied to the GD's or a current or impedance value changing with more or less transistors or external resistors in parallel.

1.6.3 Active closed-loop techniques

Closed-loop d*v*/d*t* or d*i*/d*t* control uses a signal from v_{DS} or its derivative to set and correct the derivative of these voltage or current by acting on the gate of the power device. Closed-loop systems have the advantage of reducing the sensitivity to external disturbances. Such a system automatically compensates for any parameter that can affect the switching speed such as: manufacturing dimensions and doping levels, temperature, load current, DC bus voltage, gate voltage, capacitance and transconductance non-linarites. Closed-loop systems can compensate for all these parameters variation and a higher switching speed could be achieved for lower switching losses.

1.6.4 Independent control of d*v*/d*t* and d*i*/d*t*

In 2003, Park [30] demonstrated an AGD capable of controlling the d*v*/d*t* independently to the d*i*/d*t* for IGBT power devices. The method used is a closed-loop control. See **Figure 1.28** for schematics and measured waveforms during switch-on.

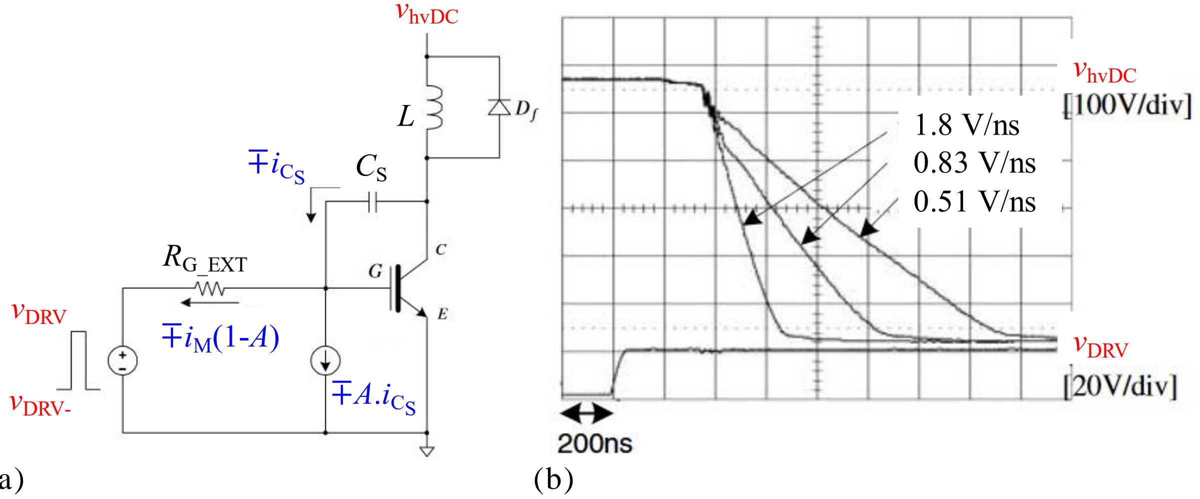


Figure 1.28. (a) Equivalent circuit for flexible and independent control of d*v*/d*t* from d*i*/d*t*. (b) Experimental d*v*/d*t* control of the switching node voltage. [30].

The method consists in sinking a current $i_{\mathrm{FB}} = A \cdot i_{C_S}$ after the external gate resistor R_{G_EXT} only during the d*v*/d*t* phase. To detect the d*v*/d*t* phase, a current is sensed between the collector and the gate of the IGBT with an external capacitor of 1.5 nF.

The controlled d*v*/d*t* is given by the following expression:

$$\frac{\mathrm{d}v_{\mathrm{DS}}}{\mathrm{d}t} = \frac{-v_{\mathrm{th}} + \frac{\mathrm{i_L}}{g_{\mathrm{m}}} - v_{\mathrm{DRV}}}{R_{\mathrm{G}} \cdot C_{\mathrm{rss}} + (1 - G) \cdot C_{\mathrm{M}}} \tag{1.20}$$

where *G* is the current gain. Adjusting the value of *G* over a range including positive and negative polarities makes it possible to electronically increase or decrease the effective value of the total Miller capacitance and therefore the d*v*/d*t* without changing the d*i*/d*t* value [30].

With the same expression above, Sun [63] in 2016 used this same system to control the d*v*/d*t* of GaN power transistors and achieve a controllability at turn-on from 10 V/ns to 2 V/ns. The proposed method in this thesis is similar to these two previous works and will use analog design CMOS integration to achieve higher bandwidth and therefore show controllability of higher values of d*v*/d*t* for WBG devices.

1.5.6 Discussion / Summary

The difference between these tree methods can be summarized in **Table 1.3** below. The passive method is the simplest and therefore can be the less expensive to implement in mass production. If the active open-loop method needs an FPGA or digital logic to control the switching waveform, the active closed-loop could be simpler and have lower cost if the control is done using only analog techniques like the one proposed in this thesis. Similarly, concerning the feedback loop bandwidth with proper analog design techniques, the passive method could achieve the highest bandwidth of the three methods. However passive methods have no adaptability of parameters changes. Those parameters can be fabrication parameters like doping and dimension variations or changes in the voltage (v_{DS} and $\underline{v}_{DRV}$) and current (i_L) of the power system.

TABLE 1.3. COMPARISON OF TYPES OF SWITCHING TRAJECTORY CONTROL METHODS

	Passive	Active open-loop	Active closed-loop
Complexity/cost	+++	+	+
Bandwidth	++	+	+
Adaptability to parameters variation	0	+	+++

The proposed method in this thesis has several advantages compared to other methods used to control d*v*/d*t*.

- Compared to an added constant external capacitor C_{GD}, the emulated capacitance $G \cdot C_S$ will not affect the device immunity through Miller coupling. The risk of a cross conduction fault is then mitigated. Another advantage is that the emulated capacitance can be changed through the feedback gain G. Moreover, the value of the required high-voltage C_S capacitor can be reduced using our technique; hence, its integration within the CMOS circuit is possible.

- Compared to open-loop techniques, the closed-loop method adapts the response for different systems and power devices under different conditions, while an open-loop approach would have to be designed for each different applications and power devices [58].

- Compared to other previously demonstrated closed-loop techniques, our approach is simple, extremely fast and highly integrated. While other closed-loop methods convert analog signals to digital signals using an ADC, their speed is limited to tens or hundreds of nanoseconds. Very high switching speeds and/or very short

switching times cannot be controlled by the solutions presented today in the literature [65].

- Compared to other integrated solutions [91], [95], our solution offers both low (e.g., 48 V) and medium voltage (e.g., 400 V) applications, while using only low voltage CMOS devices and technology (e.g., 10 V, 20 V). Only a small (pF range) high-voltage sense capacitor is required, which is easily integrated with standard low-voltage CMOS technologies.

1.7 Integration approach and choice of CMOS technology

GD's can be made with different blocks with discrete devices connected to the power devices or the blocks can be integrated in one silicon bare die. Another integration approach consists in integrating the power device and GD with the same fabrication process on the same die.

The miniaturization has been a tendency happening since the beginning of solid-state electronics and confirmed by Moore's law. According to this law, "the number of transistors on a microchip doubles every two years, though the cost of computers is halved", then more complex system can be integrated in a smaller device. The advantages of integration or also called miniaturization is to reduce power consumption, reduce signals propagations delays and reduce cost. **Figure 1.29** illustrates the benefits of integration.

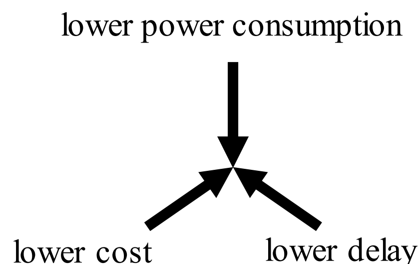


Figure 1.29. Benefits of integration and scaling down transistors.

As an example of the benefits of integration applied to power electronics, [96] integrates GD and power device in a GaN-on-Si technology (**Figure 1.30**) and reports to be able to achieve a high value of d*v*/d*t* of 350 V/ns in the switching node voltage. With smaller devices, the interconnection parasitic values are reduced, allowing higher d*v*/d*t*. With higher d*v*/d*t*, higher power efficiency is achieved.

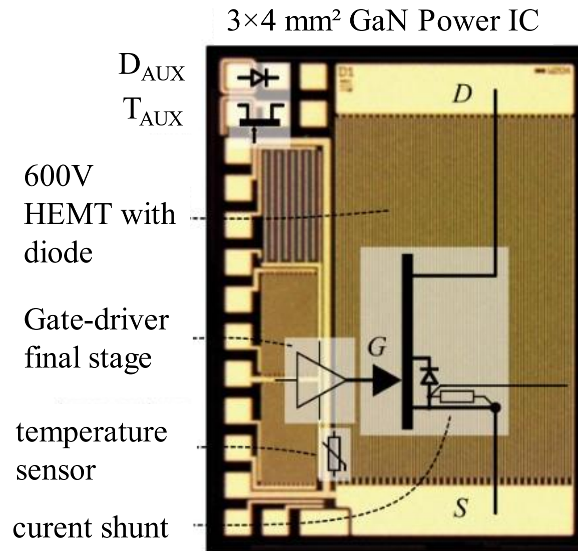


Figure 1.30. 600 V GaN power IC: HEMT with freewheeling diode, temperature and current sensors, GD final stage, auxiliary transistor and diode. [96].

Another example of research work integrating a buck converter can achieve switching frequency of 100 MHz using 0.15-µm depletion-mode GaN-on-SiC process. 20 V/5 W converter was created and achieved measured total efficiency of 88% and power stage efficiencies above 91% [90].

The high interest in works that integrate systems can be also seen when firstly a discrete GD is produced and a few years later a similar system is integrated in one IC. A team from the University of Tennessee published an AGD in IEEE Transaction on Power Electronics [78] in 2014 and an integrated circuit in one power IC in the same journal TPEL in 2017 [84]. Thanks to this integration, they were able to achieve crosstalk suppression while increasing the d*v*/d*t* from 24.9 V/ns with discrete driver to 42 V/ns with integrated driver with SiC power transistors.

Another advantage of projects integrating the GD with the power device is high temperature applications with SiC transistors. High temperature GD's can be designed to operate with SiC transistors at 500 °C [97].

The choice of the CMOS technology to be used in the developed AGD is based on the output stage architecture and the digital logic circuits. Based on typical gate-to-source voltages of GaN and SiC transistors, the maximum breakdown voltage of the output stage in the gate driver will be different. In case of GaN power devices, this voltage can be 5 V, depending on the chosen GaN technology. In case of SiC MOSFETs, this voltage is typically higher than 30 V. The maximum breakdown voltage for CMOS transistors inside the gate driver depends on the doping, but typically a minimum length of 0.5 µm is necessary to have a maximum drain-to-

source voltage ($|v_{DS_MAX}|$) voltage of 5 V. Using a technology of 0.5 µm or smaller would be similar for this point of view. For example, if a technology of 65 nm is employed, it would be necessary to use 5 V transistors in this technology and the minimum gate length for these 5 V transistors would be 500 nm. Regarding the digital logic circuits, a technology smaller than 0.18 µm could be used. CMOS technologies with 180 nm minimum gate lengths are a good trade-off between performances, cost and consumption of 1.8V digital circuits, and typically have efficient higher voltage transistors with high current capabilities. Indeed, in the AGD developed in this thesis, lateral transistors with more than 40V breakdown voltages were required for the GD output stage, in the case of driving SiC MOSFETs. On the other hand, digital and analog functions were previously developed at LAPLACE, for signal isolation and digital communication techniques, using 1.8V and 5V transistors. Hence, a 180 nm BCD (Bipolar – CMOS – DMOS) CMOS technology was considered for this work. Moreover, the Xfab BCD CMOS on SOI technologies, such as the XT018, offers the capability to operate at higher temperature (above 175°C junction temperature), and unique dielectric isolations thanks to Deep Trench Isolations (DTI).

Table 1.4 below presents the main specifications of the transistors used to design the AGD for SiC transistors. Further detailed are provided in chapter 3 and also in the thesis of Yazan Barazi [87].

TABLE 1.4. ELECTRICAL PARAMETERS OF THE CMOS TRANSISTORS USED IN THE TECHNOLOGY X-FAB 0.18 SOI. [98]

Type	ne 1.8 V NMOS	pe 1.8 V PMOS	ne5 5 V NMOS	pe5 5 V PMOS	nhvta low Ron 40 V NMOS	phvta low Ron 40 V PMOS
L_{min}	0.18 µm	0.18 µm	0.5 µm	0.5 µm	0.4 µm	0.5 µm
$\|v_{GS_MAX}\|$	1.98 V	1.98 V	5.5 V	5.5 V	5.5 V	5.5 V
$\|v_{DS_MAX}\|$	1.98 V	1.98 V	5.5 V	5.5 V	40 V	40 V
$\|v_{th}\|$	0.58 V @W=10 µm	0.65V @W=10 µm	0.78 V @W=100 µm	0.82 V @W=100 µm	1.08 V @W=100 µm	1.07 V @W=100 µm
R_{DS_ON} (KΩ.µm)	-	-	-	-	10.3 @W= 100 µm	27.5 @W= 100 µm
i_{DS} (µA/µm)	515 @W=10 µm	195 @W=10 µm	520 @W=100 µm	280 @W=100 µm	200 @W=100 µm	131 @W=100 µm

1.8 Proposed AGD approach

The proposed method in the work presented here will use a similar approach to the one in **Figure 1.28** published in 2003 [30] with a different architecture. The controllability of dv/dt is given by:

$$\frac{dv_{DS}}{dt} = \frac{-v_{DRV} - v_M}{R_G \cdot C_{rss}} + \frac{i_{FB}}{C_{rss}} = -\frac{v_{DRV} - v_M}{R_G \cdot (C_{rss} + G \cdot C_S)} \tag{1.21}$$

This equation will be plotted in chapter 3 showing the dv/dt as a function of the gain G.

When designing a half bridge, there is a trade-off between the switching losses (E_{ON}, E_{OFF}) and switching speed (dv/dt, di/dt). As long as the Miller effect is an active phenomenon (all turn-on or some turn-off transients at high load current), dv/dt is typically limited by the choice of the gate resistor R_{G_EXT}. **Figure 1.31** introduces this classical trade-off (solid line) for the specifications detailed in the next sections (obtained with a CADENCE™ simulation with a model of a GS66508T GaN device). Using an independent dv/dt control from the di/dt value, it is possible to go from the point A to the point C (dashed line) but increasing lower switching losses compared to a simple change in the total gate resistor value R_G (from point A to B). This change in the switching speed versus switching losses trade-off can be further dynamically tuned by changing the AGD parameters.

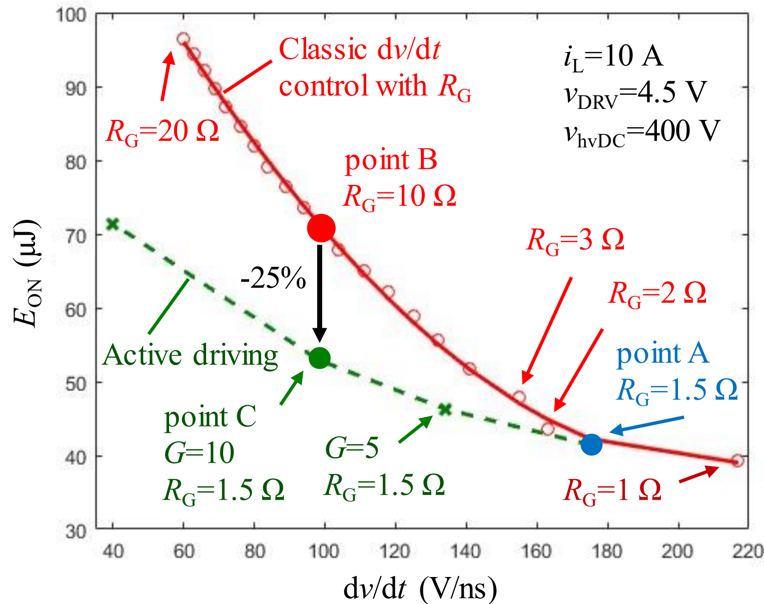


Figure 1.31. Trade-off E_{ON} vs dv/dt as a function of R_G (solid line) or closed-loop gain G (dashed line) values for a constant bus voltage, load current and temperature. The proposed method aims to reach the point C without increasing the external gate resistor R_G.

The amount of saved energy during turn-on is explained in **Figure 1.32**. The proposed method reduces the amount of switching losses because the d*v*/d*t* value is reduced without modifying the d*i*/d*t*. As a consequence, the dissipated switching energy during the d*i*/d*t* event (hatched area in **Figure 1.32** (d)) is saved with our technique. The proposed method will not change the d*i*/d*t* because the proposed feedback loop will not be active during this phase.

First, the d*i*/d*t* value can be set by adjusting the value of R_G, and then the d*v*/d*t* can be separately adjusted to reduce the negative effects of the EMI. One has to note that the parasitic stray inductance is neglected in this section (to explain the method), which is a reasonable assumption for high-frequency applications of GaN power transistors with optimal PCB designs (e.g., power loop stray inductances in the range of 1 nH).

Another positive consequence of this method is that both points B and C (**Figure 1.31**) will also generate lower drain current overshoots during the d*v*/d*t* sequence [t_4, t_2] (**Figure 1.32**) than point A; i.e., the d*v*/d*t* of point A generates an extra transient current proportional to the parasitic drain-to-source capacitors of the power transistors.

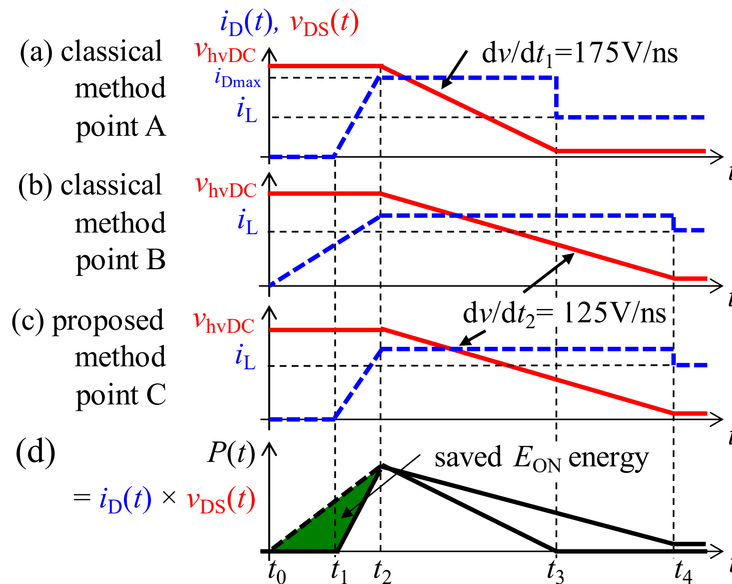


Figure 1.32. Explained benefit of the method to save *E*on energy during each transition of a WBG power device. Reducing only the d*v*/d*t* for attenuate negative effects in EMI and not reducing d*i*/d*t* will save the hatched area represented in the figure (d).

The main idea of the proposed active gate driving is to control d*v*/d*t* by emulating an increase in the Miller capacitance (or C_{rss} equivalent capacitance) of the power device only during the switching event and the d*v*/d*t* sequence. To do so,

a current proportional to dv_{DS}/dt has to be subtracted from the gate current during the turn-on event. Hence, a feedback loop is used to generate this current, which is directly connected to the gate of the power device to reduce the gate current amplitude during the Miller plateau. This feedback method has been previously proposed but with key limitations:

- With discrete components, only low switching speeds can be actively driven (e.g., fall time of tens or hundreds of nanoseconds, as in [63], notice that this reference also does not proposed an on-chip high voltage capacitor),

- With integrated solutions in CMOS GD's, only low-voltage applications are addressed, where the maximum drain-to-source voltage is lower than the CMOS technology limit (e.g., 12 V, as in [99]).

Figure 1.33 shows a (a) diagram and (b) transistor-level diagram of the proposed method. A low value capacitor C_S is used as a sensor of the derivative of the power transistor voltage v_{DS}. A capacitor with high breakdown voltage is required, since it has to hold the high DC bus voltage. To amplify the current generated into this sensor during the dv/dt, a large-bandwidth gain current mirror is proposed, which is the core idea for this method. The main challenge in this approach is to propose a circuit that can simultaneously supply a high amplitude feedback current with a very small time-delay response.

Typically, this feedback current i_{FB} may be higher than 1 A, and the delay in the feedback loop should be lower than 1 ns, since SiC and GaN power devices switch in few nano seconds. This feedback current i_{FB} is proportional to the derivative of the power transistor voltage v_{DS}, current gain G and the value of the capacitor C_S acting as a dv/dt sensor (as shown in (1.22) below).

$$i_{FB} = -G \cdot C_S \cdot \frac{dv_{DS}}{dt} \tag{1.22}$$

Typical C_S values are much lower than the GaN C_{rss}, leading to C_S in the order of 0.7 pF to 2 pF. To reach these specifications, a CMOS integration with optimal design is required. The analysis for an optimization is discussed in chapter 2.

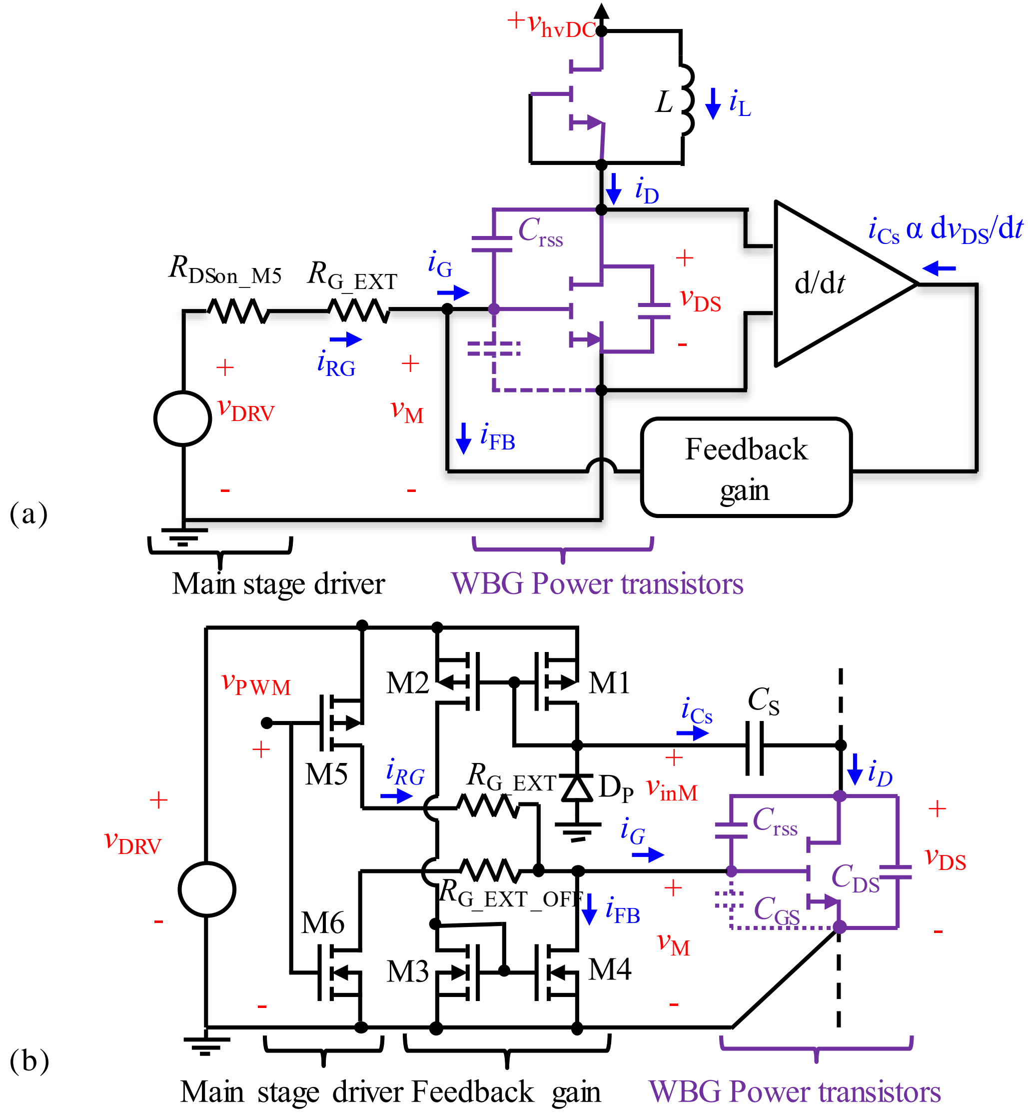


Figure 1.33. The proposed method to control dv/dt during turn-on transients of WBG power devices. (a) Diagram of the method. (b) Physical implementation of the method. (with v_{M} the value of v_{GS} during the Miller plateau).

Applying Kirchhoff's law at the gate node, the dv_{DS}/dt reduction is proportional to the feedback current i_{FB}. The following expression is obtained and is valid as long as there is a current flowing through C_{S} with $i_{\mathrm{FB}} < i_{\mathrm{RG}}$ for stable operation, and a constant v_{M} voltage on the dv/dt sequence:

$$\frac{\mathrm{d}v_{\mathrm{DS}}}{\mathrm{d}t} = -\frac{v_{\mathrm{DRV}} - v_{\mathrm{M}}}{R_{\mathrm{G}} \cdot C_{\mathrm{GD}}} + \frac{i_{\mathrm{FB}}}{C_{\mathrm{GD}}} = -\frac{v_{\mathrm{DRV}} - v_{\mathrm{M}}}{R_{\mathrm{G}} \cdot (C_{\mathrm{GD}} + G \cdot C_{\mathrm{S}})} \tag{1.23}$$

Note that the feedback circuit acts like an active equivalent gate-drain capacitor placed in parallel with C_{GD} equal to $G \cdot C_S$. Due to the feedback current amplification through current mirrors, the sense capacitor C_S can be downsized and further integrated on-chip. The feedback loop is composed of four low-voltage transistors, M1 to M4, and a high-voltage sensing capacitor C_S. For the SiC architecture transistor M4 is a high voltage (40V) CMOS transistor. The current buffer, also called the main stage driver, is composed of a PMOS transistor M5 and a NMOS transistor M6 used to source and sink the high gate currents, respectively. This buffer has a split output architecture, making it possible to use different resistors to adjust the turn-on and turn-off switching losses separately. Diode D_P is used only as a protection device at the input of the current mirror and is reverse biased during normal operation. In case the current in C_S is too high, diode D_P will clamp v_{inM} voltage at -0.7 V, guaranteeing that the gate voltage for M1 and M2 will not exceed the nominal maximum voltage value (5.5 V), therefore preventing breakdown destructive voltage in transistors M1 and M2.

Figure 1.34 introduces the waveforms for the main signals related to this approach that are used to actively control dv/dt. At the beginning of the dv/dt phase (at time t_2), a delay $t_{D50\%}$ is first required before the feedback loop starts to sink the current i_{FB}. This delay is mainly due to the settling time of the feedback loop circuit. The current i_{FB} quickly reaches its final value i_{FB_F}, which is subtracted from the current i_{RG} provided by the driver. When i_{FB_F} increases, the gate current i_G is decreased, leading to an increase in time t_3 in order to provide enough time to transfer the overall charges required by the gate of the power transistor during the Miller plateau. As a result, the dv_{DS}/dt is actively reduced. For the sake of simplicity, a constant Miller Plateau voltage is considered.

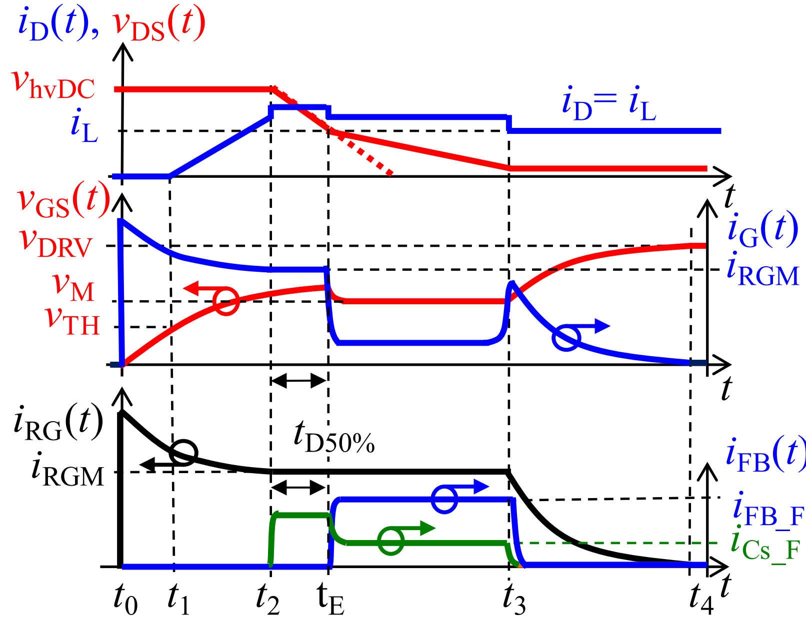


Figure 1.34. Waveforms of the proposed method. The method will subtract a current only during the dv/dt phase of a switching transient.

During the turn-off transition, the sensing capacitor C_S sources (instead of sinking) a current that flows through the body diode of M1. The width of M1 (W1) has to be sized correctly to handle the C_S discharge current without breaking M1 or increasing the voltage at node v_{inM} excessively.

It can be noted that if the total subtracted current i_{FB_F} increases too much, due to a high loop gain and overly fast feedback response, it can accidentally reach the value of the current supplied by the driver. In that case, the gate current i_G in the power device during the Miller plateau is cancelled. Then, the v_{DS} and v_{GS} voltages start to oscillate and the closed-loop system becomes unstable. A limit of the method comes from the maximum amount of time $t_{D50\%}$ required by the feedback current loop to operate. If this time delay is higher than the duration t_3 - t_2 observed in open-loop, the turn-on transition will be missed, and the feedback loop will have no effect on reducing dv/dt. It is important to ensure that the loop is able to operate as fast as possible. Finally, the time delay $t_{D50\%}$ characterizes the system performance both in terms of time response and stability. In our case, we will optimize the integration and circuit design to have less than 1 ns delay and to actively control initial fall time of 3 ns and above (dv/dt_{peak} =-175 V/ns in the case of 400 V applications).

The simulation behavior of the previously explained waveforms is presented below. **Figure 1.35** (a) shows the dv_{DS}/dt reduction for the system operating at point A (open-loop) and C (closed-loop), as defined in **Figure 1.31** and **Figure 1.32**.

Figure 1.35 (b) shows the extension of the Miller plateau due to the added virtual capacitance effect and closed-loop control. **Figure 1.35** (c) shows the gate current i_G that is going to the power device gate terminal, and **Figure 1.35** (d) shows the drain current i_D of the power transistor and a beneficial reduction in overcurrent, while keeping approximatively the same initial di/dt.

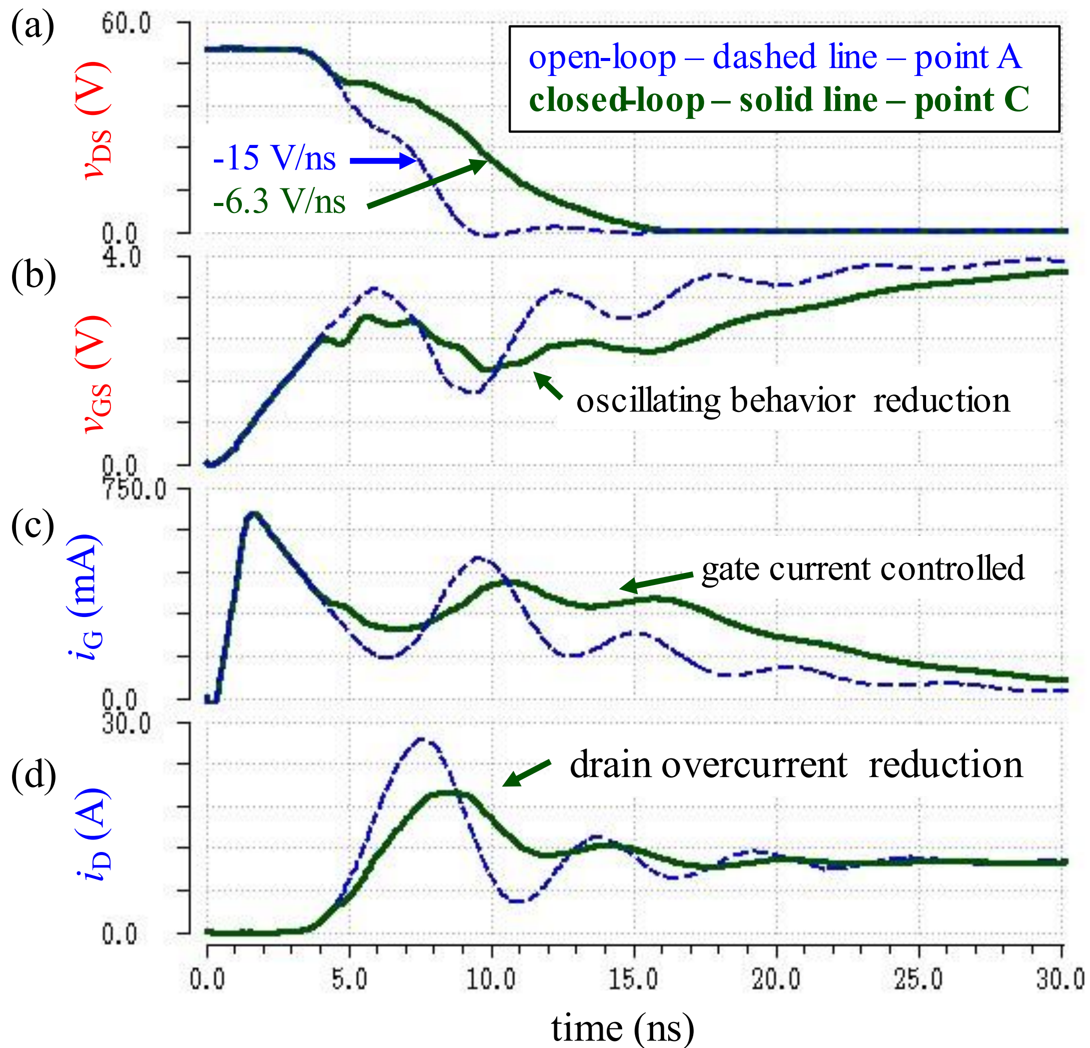


Figure 1.35. Simulation waveforms for (a) v_{DS}, (b) v_{GS}, (c) i_G and (d) i_D with (case C) and without (case A) the proposed method, including estimated PCB parasitic elements; (d) also shows a beneficial effect of reduction in overcurrent (i_D) during turn-on that is also provided by the proposed method. Case study for the 48 V application.

1.9 Chapter conclusion

This chapter focused on the state-of-the-art of Active Gate Drivers (AGD) for d*v*/d*t* and d*i*/d*t* control for power semiconductor devices made in both silicon and wideband gap power semiconductors (GaN and SiC materials). In the beginning, selected application examples were described to show the importance and the growing market of AGD in the power electronics sector. The benefits of WBG transistors are introduced and the challenges, limitations and key performances of AGDs are detailed. Second, a brief overview of the switching transients of power devices is presented. It is followed by examples of measurements of switching energy and general characterization of elements and systems in the context of power electronics with high efficiency. The state-of-the-art of switching trajectory control systems are classified by types of power transistors and types of control methods. Finally, the importance of integrating systems in one CMOS chip and the proposed method is briefly introduced and is further detailed in the next chapters.

2 Theoretical Analysis of dv/dt and optimization of design parameters

This chapter will focus on the optimization studies of the feedback loop performance. In order to get a very fast control loop to manage high dv/dt of SiC or GaN power transistors, the several components involved in the integrated circuit have to be analyzed carefully and sized accordingly to get both high bandwidth (or very fast settling time performance) and small silicon area for a lower price. The theoretical expressions and the dependencies of the main variables are detailed.

2.1 Introduction

In the paper titled "Area/Bandwidth of CMOS current mirrors" [100] from 1986, the area and bandwidth of current mirrors are studied as a function of the total gain. A similar study is performed in this chapter.

The feedback loop is composed of 3 stages and is shown in **Figure 2.1**. The most intuitive way to represent a circuit consists to show the inputs on the left-hand side and the outputs on the right-hand side. One way to consider the feedback loop is that the current amplification is made by 3 different stages: a sensing capacitor C_S, and two current mirrors, one with PMOS and the other with NMOS transistors providing the gains G_P and G_N respectively.

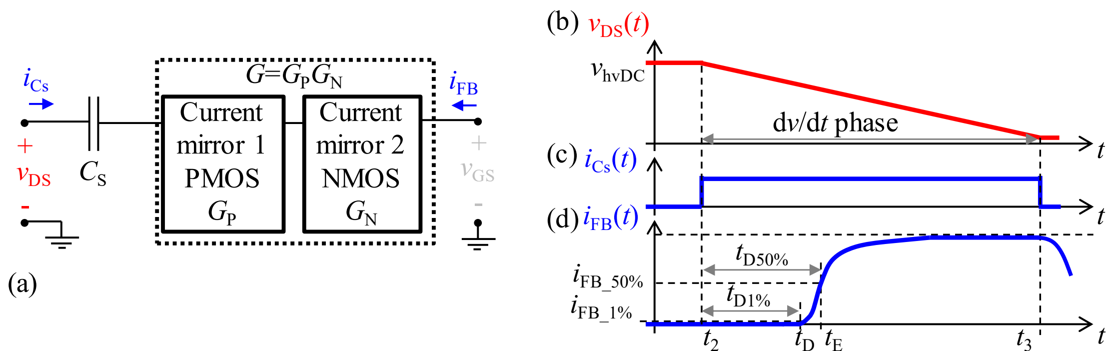


Figure 2.1. (a) The feedback loop can be represented as a current amplifier divided in 3 stages: a dv/dt sensing capacitor C_S, the current mirror 1 with PMOS transistors and the current mirror 2 with NMOS transistors. It should be noticed that the open-loop analysis does not connect the output of the current mirrors to the gate of the power device (v_{GS} node). (b) During the turn-on dv/dt sequence, the system presents a delay $t_{D50\%}$ between the rising-edges of (c) the input current i_{Cs} and (d) the output current i_{FB}.

The product $C_S \cdot G_P \cdot G_N$ represents the virtual capacitor added between the gate and the drain of the power device leading to the reduction of the switching speed during the turn-on. It can be noticed that this term, related to the amplification of the input current, is distributed between the three different stages. To achieve high bandwidth and utilize small amount of silicon area, the relationship between different parameters and technologies must be found, which is the focus of this chapter.

2.2 Presentation of the circuit topology

In the previous chapter the diagram of the proposed method for the control of the switching speed has been presented. In this chapter the transistor-level schematic is shown in **Figure 2.2** below. First, at the left side of the figure, are shown the “big” transistors PMOS M5 and NMOS M6. These two transistors, constituting the main output stage of the gate driver, either source or sink the gate charge during a turn-on or turn-off event respectively. The gate charge is provided to the capacitances C_{rss} and C_{GS} connected to the gate of the WBG power device, shown at the right side of the figure. At the center of the figure the feedback loop required to control the d*v*/d*t* is shown. It is composed of four transistors M1 to M4 and one d*v*/d*t* sensing capacitor named C_S.

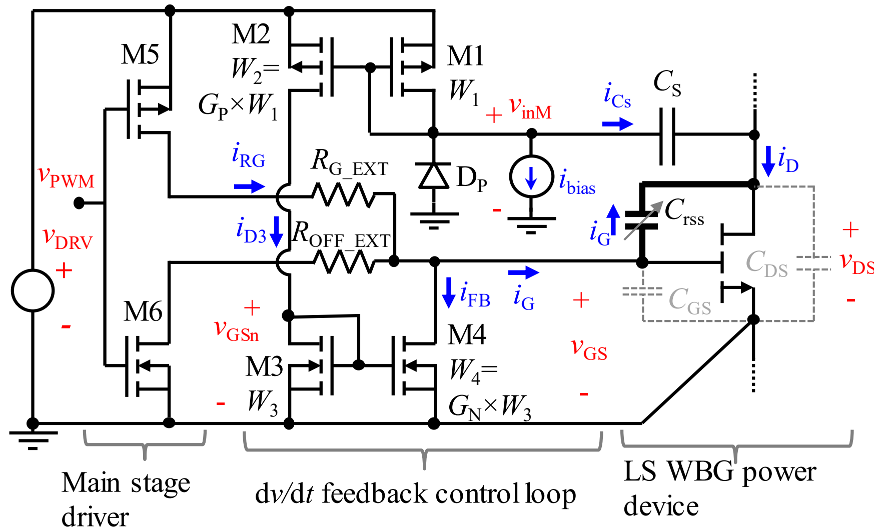


Figure 2.2. The transistor-level schematic of the proposed circuit. Transistors M1 to M4 are the two current mirrors that amplify the current sink by the sensing capacitor C_S. Transistors M5 and M6 are the main stage driver. The effect of the feedback loop is to emulate a virtual capacitance added in parallel with C_{rss} that can be controlled electronically by the product $G.C_S$, i.e. a chosen gain G multiplied by the capacitor value C_S.

As previously mentioned, the three stages of the control loop composed by the capacitor C_S and the transistors M1-M2 and M3-M4 have to be analyzed. Each part is considered separately in the next sub-chapters.

2.3 HV capacitor for integrated d*v*/d*t* sensor

The proposed method to control d*v*/d*t* uses a high voltage sensing capacitor directly connected to the drain of the power device and it will therefore withstand the full voltage range of the DC bus (v_{hvDC}). We can implement this capacitor into the gate driver chip in order to remove an external on-board component and to reduce therefore the parasitic effects (inductive and also common-mode capacitive coupling). On-chip capacitors usually have very thin oxide and a dedicated metal layer called MIM (metal-insulator-metal). MIMs capacitors usually can withstand only a few volts, typically the supply voltage (v_{DD}) of the transistors (e.g. 0.8 V, 1.8 V or 5 V) or up to 40 V or 60 V for high voltage CMOS processes, but not much more. Another type of on-chip capacitors are the MIS (metal-insulator-semiconductor) capacitors with MOS (metal-oxide-silicon) the most famous of them [101]. With a very thick oxide of 1 µm, a MOS capacitor could have a breakdown voltage slightly above 100V but not much more [101]. In order to withstand 540V for aeronautical applications, a breakdown voltage of at least 1 kV should be achieved to provide an appropriate safety margin.

For high voltage applications, MOM (Metal-oxide-metal) capacitors can be used [102] [103] [104] [105]. MOM capacitors can use the lateral capacitance, existing between two separate wires drawn on the same metal layer, with one [106] [107] [108] or several metal layer [109] [110] [111] to obtain what is called fringe capacitor providing a thicker oxide isolation. Another alternative is to use the oxide isolations existing between the different metal layers in a CMOS process to implement a vertical HV capacitor. **Figure 2.3** shows the first capacitors designed in our circuit to withstand respectively 450 V, 1400 V and 3500 V. The 450 V capacitor could be used for 50 V application with a good safety margin. For 400 V applications (with GaN 650 V devices), a capacitor with a measured breakdown voltage of 1400 V is suitable and available. A capacitor capable to withstand up to 3500 V is also designed to explore the limits offered by the technology with this vertical isolation approach.

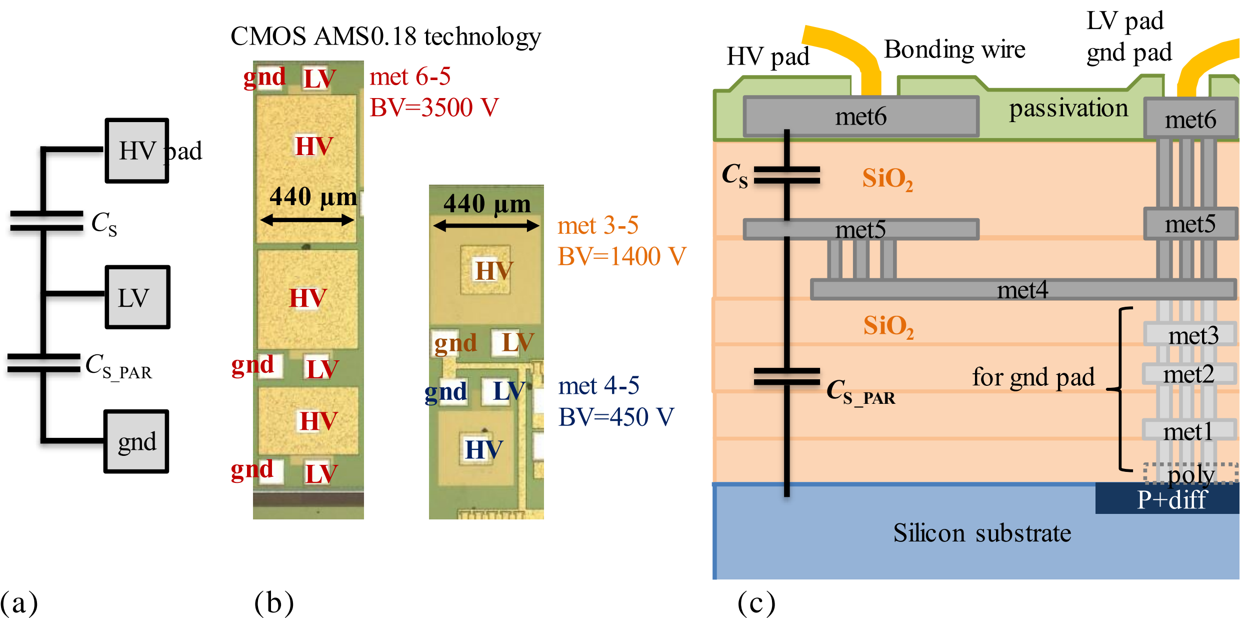


Figure 2.3. The high voltage sensing capacitor C_{S}. (a) Schematic (b) photo of all capacitors designed in AMS0.18 technology. (c) Cross-section of a metal 5 to metal 6 vertical capacitor. The value of the oxide thickness is confidential and is related to the used technology.

It is observed a parasitic capacitance present between the low voltage (LV) plate and the silicon substrate, named C_{S_PAR}. To minimize this undesired capacitance, the strategy consists of using for the bottom plate the highest level of metal layer possible. The proposed design uses the top metal layer for the HV plate and one of the metal layers underneath for the LV plate. Therefore, the level of the metal layer used for the bottom plate depends on the desired insulator thickness. Notice that there is a passage to a lower metal level then the LV plate to carry the current. However, the area of this current path is considerably smaller than the LV plate, therefore the parasitic capacitance can be neglected comparing to the LV plate.

For higher voltage applications using SiC MOSFET transistors, instead of GaN HEMT, a different CMOS technology is chosen. The reasons for the choice will be detailed in chapter 3. For GaN HEMT, the AGD is made using the technology CMOS AMS0.18. (**Figure 2.3**). For SiC MOSFET, the chosen technology is XFAB0.18SOI. In that case, the on-chip sensing capacitors are designed to withstand a higher breakdown voltage. **Figure 2.4** shows the capacitors designed using the XFAB0.18SOI technology.

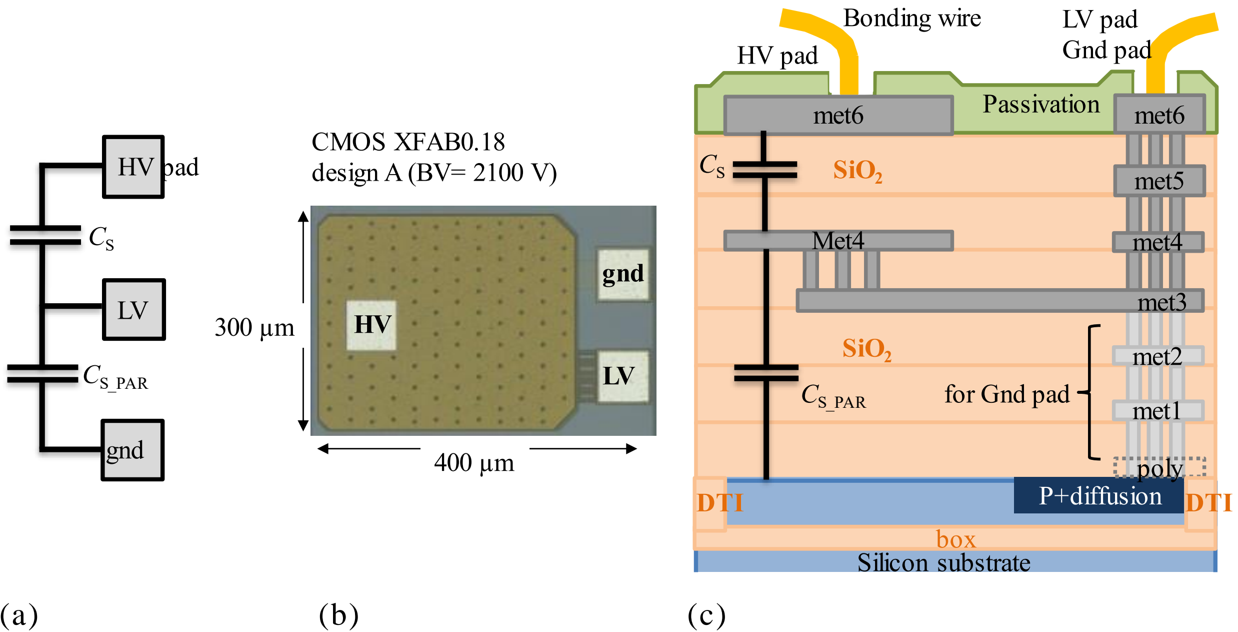


Figure 2.4. The high voltage sensing capacitor C_S. (a) Schematic, (b) photo of the capacitor implemented in XFAB0.18 technology and (c) cross-section view.

2.3.1 Density vs. breakdown voltage level trade-off

Using a vertical structure for the implementation of the sensing capacitor, it should be noted that there is a trade-off between the obtained capacitance density and its breakdown voltage level.

In one hand, the value of the capacitor is inversely proportional to the distance *d* of the plates and is given by the classical two-plate capacitor equation:

$$C = \frac{\varepsilon_r \cdot \varepsilon_0 \cdot A}{d_{ox}} \tag{2.1}$$

where ε_r is the dielectric constant of the insulator material ($\varepsilon_r = 3.8$), ε_0 is the vacuum dielectric constant, A is the area of the two metal plates and d_{OX} is the distance between the metal plates. The fringe-effect capacitor is neglected, which is relevant with the large-area two-plate capacitor.

The dielectric material of the capacitors is not pure SiO_2 ($\varepsilon_r = 3.45$) because silicon nanocrystals (nc-Si) are embedded in the process. A generic CMOS fabrication process uses Si ion implantation followed by high temperature annealing to accurately control the amount of insulating material deposited during fabrication [112]. The effective dielectric constant is not uniform and should vary with the depth of the deposited material. The dielectric constant is either 3.45 or 11.9 respectively

for pure SiO_2 and pure bulk crystalline silicon. Therefore, depending on the depth of the insulator implementation, the ε_r can change from 3.5 to 3.9 (see Fig. 4 of [112]). Related to the capacitance per unit area and dielectric strength values provided in [112], (Fig. 4) the dielectric constant of the material composed by SiO_2 and nanocrystal (nc-Si) for the isolating thickness in the proposed capacitors is very close to 3.8. In practice, it should be noted that the insulator thickness values present between two adjacent metal layers are provided by the foundry, i.e. indicated in the design-kit related to the used CMOS technology.

On the other hand, the breakdown voltage depends on the insulator material thickness and is therefore proportional to the distance *d* of the two plates. [113] describes how the dielectric strength of the oxide is a function of the oxide thickness. The theoretical values of dielectric strength for pure SiO_2 are within a range of values spread over a decade and is shown in **Figure 2.5**.

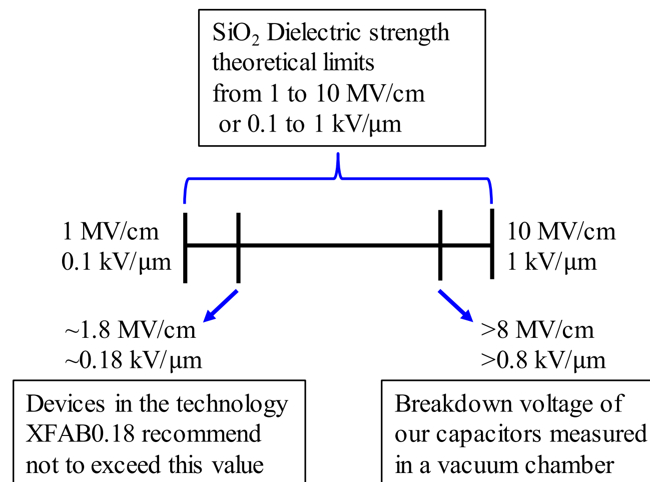


Figure 2.5. The theoretical dielectric strength of the SiO_2 compared with values recommended by the technology and the breakdown voltage measured in a vacuum chamber (2.4×10^{-6} mbar).

2.3.2 Preliminary measurements

Breakdown voltage tests consist of placing the bare die in a round metal chuck (connected to the ground potential) and applying a high voltage with needle probes mechanically controlled in motion with micrometric precision. An optical microscope with 1000× amplification factor is used to place the probes. See **Figure 2.6.**

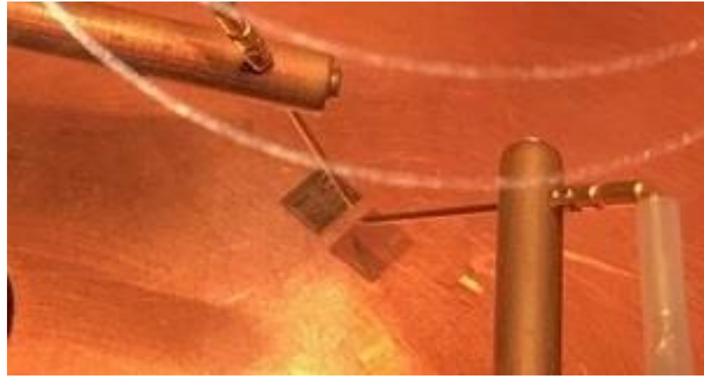


Figure 2.6. The high voltage is applied with probes to the bare die inside a high vacuum chamber that uses two air pumps to achieve the pressure of 2.4×10^{-6} mbar.

The applied voltage is slowly increased and when a destructive breakdown voltage occurs, a lamp is turned on indicating that the current is crossing a threshold value in the high voltage generator. A resistor is placed in series to limit this current. The high vacuum probe station available in the dielectric (MDCE) research group at LAPLACE was used for the experiments. The damage in the insulator material in the capacitor can be seen in **Figure 2.7** comparing (a) and (b).

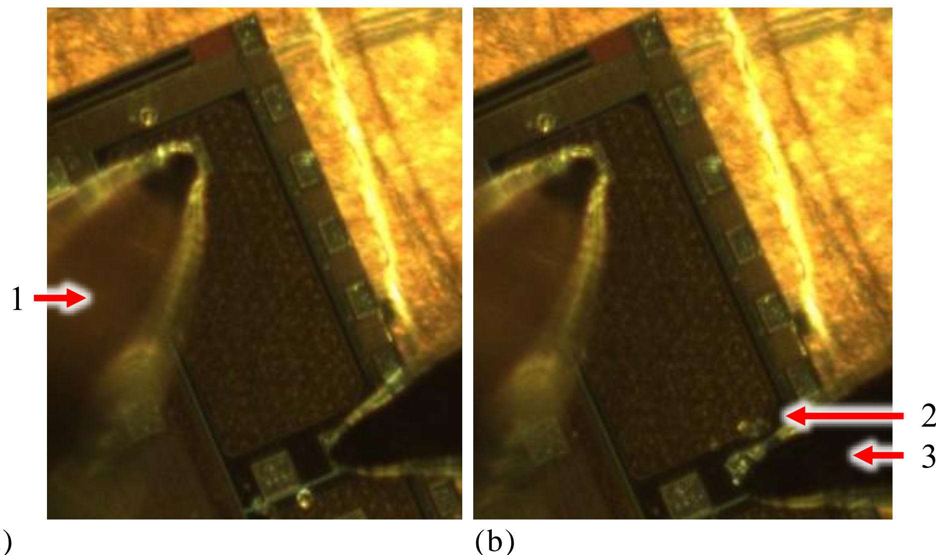
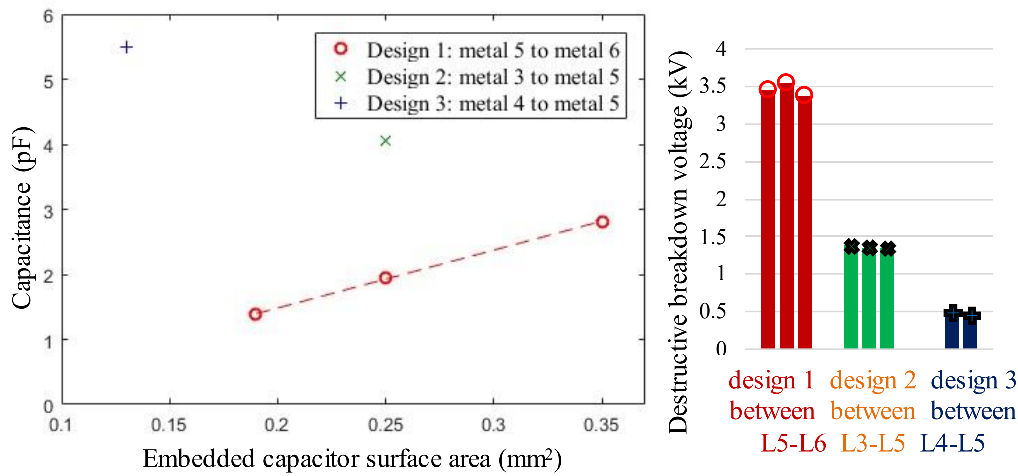


Figure 2.7. The microscope image of the on-chip high voltage capacitor during the test. (a) Before and (b) after the destructive breakdown voltage event. 1: high voltage (HV) needle probe; 2: the damage can be seen after the dielectric breakdown; 3: low voltage (LV) needle probe.

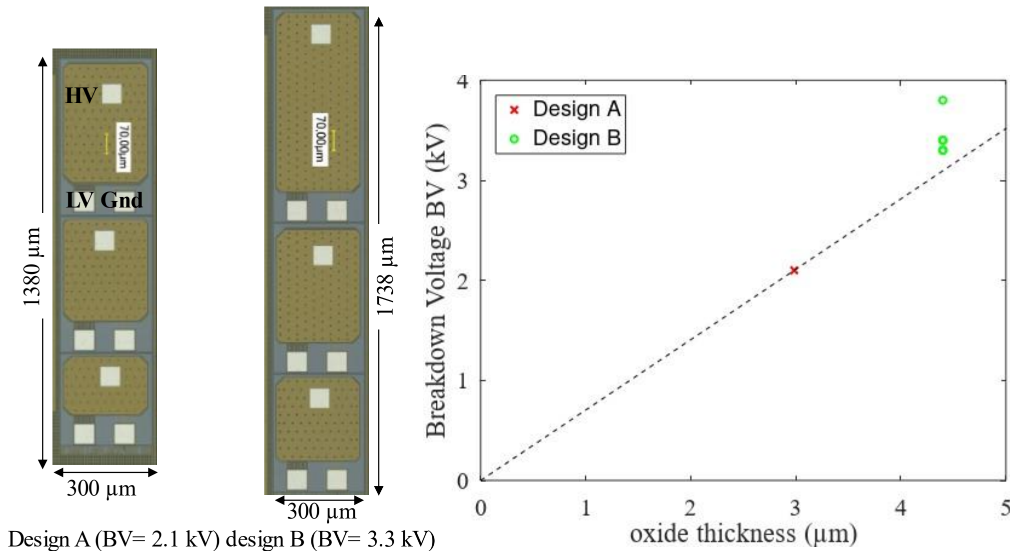
The values accurately obtained inside this range of possible values is related to the amount of nanocrystal (nc-Si) contained in the SiO_2 which constitutes the insulator, as discussed before. The capacitance values measured at 1 MHz using the impedance analyzer HIOKI IM3570 and the breakdown voltage values obtained with AMS0.18 technology are shown in **Figure 2.8** and published in [114].



(a) (b)

Figure 2.8. (a) Measured capacitance values for all capacitors in AMS0.18. (b) Measured destructive breakdown voltage for the 3 different capacitor involving different metal layers.

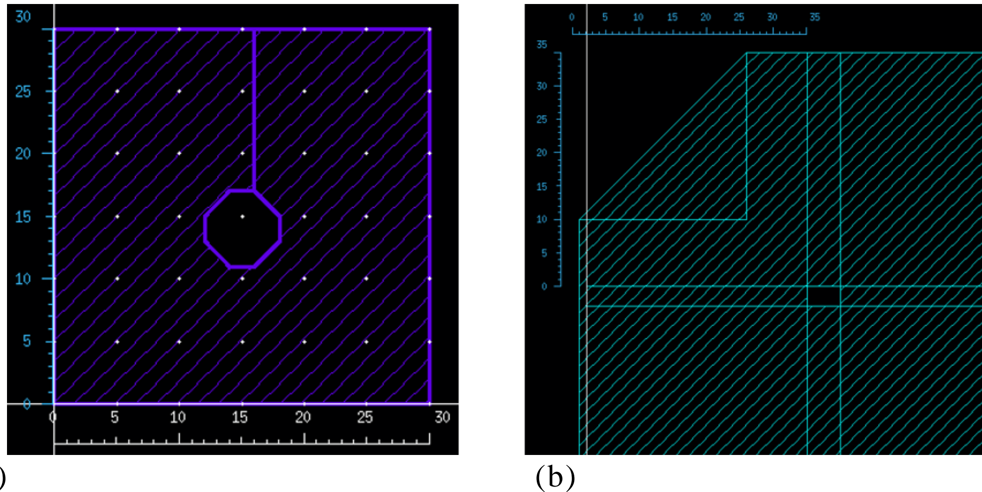
Figure 2.9 (a) shows a microscope photo of the HV capacitors designed using the technology XFAB0.18SOI and in (c) the obtained breakdown voltage measurement. The design A has an insulator thickness of around 3 µm. It should be noted that the number of metal layers used to obtain such a thickness is kept confidential. The design B has 4.4 µm of insulator thickness. A line is extrapolated from zero thickness and drawn in **Figure 2.9** (c).



(a) (b) (c)

Figure 2.9. Photo of the high voltage MOMs (metal oxide metal) capacitor in XFAB0.18SOI technology for design (a) A and (b) B. (c) Measured breakdown voltage values and extrapolation to the thickness equal to zero.

When designing with AMS technology, the maximum metal density rule is not a problem to create large square areas with metal layers. When designing with XFAB technology, a maximum surface rule applies. To avoid DRC (Design Rules Check) issues, an elementary structure involving a void space is drawn. This structure is shown in **Figure 2.10** (a). The corners have to be cut with triangular shape to avoid accumulation of electric field and edge or corner effects that could reduce the dielectric strength of the capacitors. **Figure 2.10** (b) shows the resulting corners.



(a) (b)

Figure 2.10. (a) Structure designed to avoid maximum metal density rule. (b) Triangular corners to avoid tip effect in the electric field that could decrease the dielectric strength.

2.4 Sizing M1 and M2

Considering the circuit shown in **Figure 2.2**, the first element of the feedback loop to be sized is the transistor M1. Because it is connected as a diode-connected transistor, the equivalent circuit is shown in **Figure 2.11**. In the technology reference documents, three different threshold values are provided for each type of transistor. The first value is for long channel transistor (L=W=5 µm). The second value is for short channel transistor (W×L=5 µm×0.7 µm) operating in saturation region. The third value is for short-channel transistor operating in linear region. It is recommended to use the short channel value since transistors are made using the minimum channel length L possible to withstand 5 V, which is 0.7 µm for AMS technology and 0.5 µm for XFAB SOI technology.

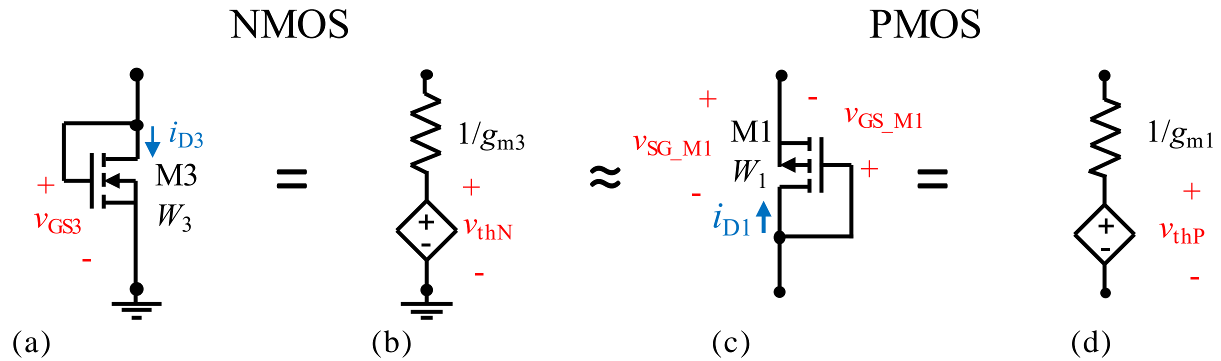


Figure 2.11. (a) NMOS diode-connected transistor. (b) Equivalent circuit. (c) PMOS diode-connected transistor and its (d) equivalent circuit.

For a given current i_D, through the CMOS transistor channel, the resulting gate-to-source voltage present at the terminals of the transistor is a function of the width W of its channel. Depending on the application, increasing the current i_D should be interesting to increase accordingly the width of the transistor in order to keep the v_{GS} voltage at a safe and predefined value. Using parametric simulations, at v_{GS} constant and equal to 4.5 V, corresponding to the supply voltage 5 V including a safety margin of 0.5 V, it is observed a constant current per width ratio over a wide range of values for W_1 (**Figure 2.12**).

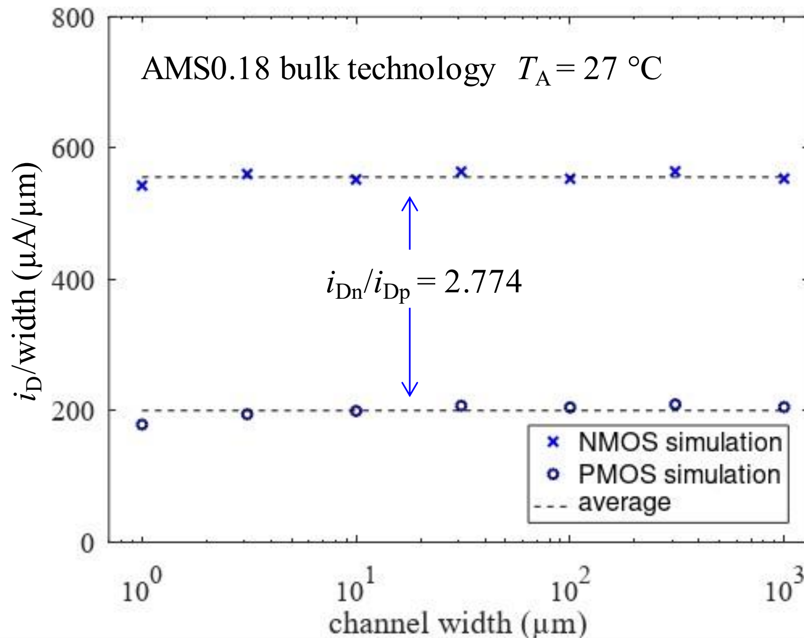


Figure 2.12. Room-temperature simulated current per channel width of the diode-connected transistor M1 and M3 with v_{GS}=4.5 V (technologies AMS0.18). It is observed a constant value of current per width ratio over a wide range of values for W.

Considering the minimum value for the length L of the transistor channel and for a given admissible v_{GS} signal excursion, this constant i_D/W ratio is very useful to determine the value of W for a current i_{Cs} coming from C_S capacitor. For example, an abacus similar to the one shown in **Figure 2.13** could be used to define the value of W.

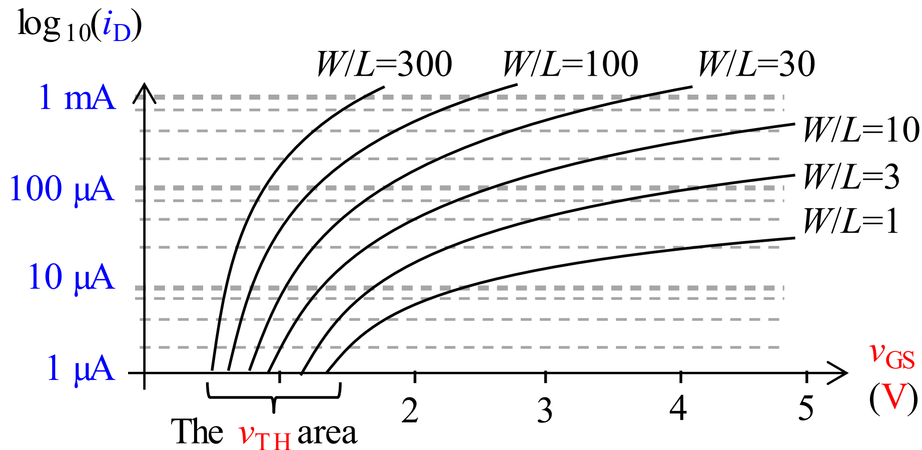


Figure 2.13. Abacus to help design scale factor of the transistor based on the required I-V characteristics. Values are approximate in this figure. Normally used to size one PMOS transistor a similar approach can also be used for a diode-connected PMOS.

Figure 2.14 shows the static I-V characteristic of a diode-connected PMOS transistor. Due to short channel effect observed in submicron CMOS technologies [115], two different operating zones may be distinguished: a low current and a high current zone [116]. At low current level, the classic well-known square law has to be considered first. At high current level, this square law is no longer valid and a direct proportionality between drain current and gate-to-source voltage is observed. Then, the relationship is linearized and an effective admittance coefficient is deduced as indicated in **Figure 2.14**.

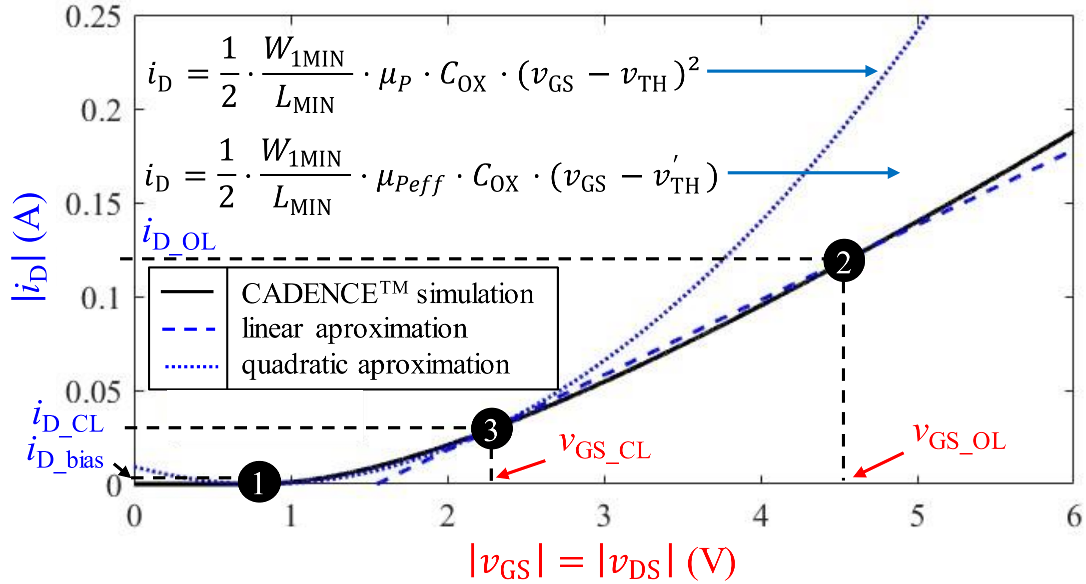


Figure 2.14. Diode-connected transistor PMOS characteristic and 1st order model parameter extraction. The operating point 1, 2 and 3 are described also in **Figure 2.15**.

During the turn-on sequence of the power transistor, the transistor M1 will operate at the operating points 1, 2 and 3 indicated in **Figure 2.14** and **Figure 2.15**. At the beginning, when no switching event occurs, i_D=0 A. At first, slightly before a turn-on order, a pre-biasing current i_{bias} (**Figure 2.2**) of about 50 µA is generated biasing M1 at the point 1. Then, when a switching event occurs, transistor M1 reaches the point 2 during a short transient less than 1ns. Just after a short delay, the feedback loop acts to reduce dv_{DS}/dt, the current i_{Cs} decreases and M1 reaches the point 3. Then, it remains in this biasing point 3 for the rest of the switching, assuming a perfect trapezoidal v_{DS} waveform for the drain-to-source voltage of the power transistor. If v_{DS} is not perfectly trapezoidal, M1 will still operate between points 1 and 3. The variable μ_P is the electron mobility and μ_{Peff} is an approximate value of μ_P but considering the linearization in **Figure 2.14**.

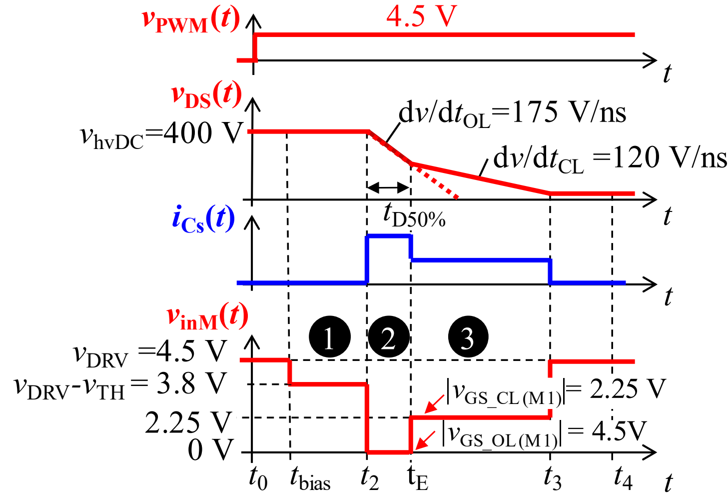


Figure 2.15. Representation of the biasing points 1, 2 and 3 defined in the previous **Figure 2.14**.

Figure 2.14 and **Figure 2.15** also show that the temporary operating point 2 should not exceed the maximum voltage v_{DVR} + 0.6 V otherwise the protection diode D_P may conduct and clamp the v_{inM} voltage to - 0.6 V. The minimum width of M1 is calculated to place point 3 at v_{GS_CL}=v_{DRV}/2 and it is verified that point 2 will operate under safe operation area. Finally, considering the linear law, the expression of the width W_1 of M1, is:

$$W_{1MIN} = \frac{i_{D_CL} \cdot L_{MIN}}{\mu_{Peff} \cdot C_{ox}/2(v_{GS_CL} - v'_{TH})} \tag{2.2}$$

Transistor M2 is a multiple of M1 depending on the gain G_P of the 1st-stage current mirror. In order to implement the desired current gain for the current mirror, W_2 is simply chosen so that:

$$W_2 = G_P \cdot W_{1MIN} \tag{2.3}$$

Note that the determination of G_P will be explained in a next section.
In order to ensure a good matching between M1 and M2, if an integer value should be considered for G_P, M2 will be made by placing several transistors identical to M1 in parallel.

2.5 Sizing M3 as a function of M2

Transistor M3 is a diode-connected transistor. It receives the current $i_{D3} = G_P i_{C_S}$ provided by M2. Sizing M3 to operate at v_{DS3}=V_{DRV}/2 will make M2 always operate in its saturation region. Moreover, M2 is a multiple of M1 whose W_{1MIN} has

been established to operate at $v_{DS1}=V_{DRV}/2$. Then, to guarantee the appropriate biasing of M3, the ratio between W_2 and W_3 has to be equal to the ratio δ of the effective mobility of the PMOS (μ_{Peff}) and NMOS (μ_{Neff}) transistors. In our case, a ratio equal to 2.5 is obtained.

$$W_3 = \frac{W_2}{\delta} \quad \text{with} \quad \delta = \frac{\mu_{Neff}}{\mu_{Peff}} \tag{2.4}$$

Another way to explain the ratio of these two transistors is made by graphical analysis. **Figure 2.16** shows the schematics and theoretical I-V characteristics for both PMOS and NMOS transistors.

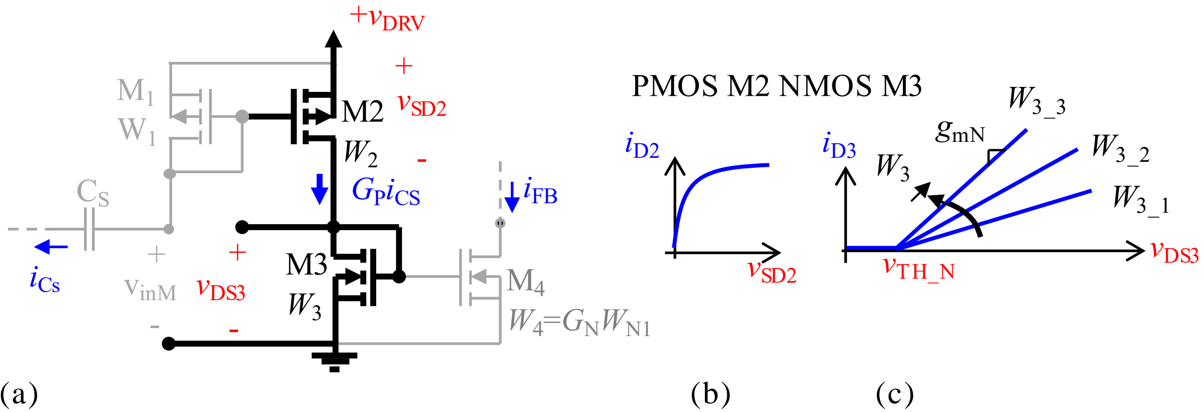


Figure 2.16. (a) Schematics for the graphical analysis of the calculation of W_3 as a function of W_2. (b) The I-V characteristic of a fixed sized transistor M2 and (c) I-V characteristics of M3 for 3 different widths.

Because both transistors share the same current and are connected in series to v_{DRV}, it is possible to write (2.5). A graphical analysis ([115], [117]) is performed by taking the upper device M2 I-V curve, reflecting it, and placing v_{DRV} at its zero as shown in **Figure 2.17**.

$$|i_{D2}| = |i_{D3}| \quad \text{and} \quad v_{SD2} + v_{DS3} = v_{DRV} \tag{2.5}$$

Figure 2.17 shows the graphical analysis, also named load line [115], [117]. Let's assume W_2 is sized to 1200 µm for instance. When there is no current i_{Cs} in the input of the current mirrors, both I-V characteristics (the load line) intersects at point Q_1, which represents the operating point of the circuit if W_3 is sized to W_{3_3}. If now a strong input current i_{Cs} is applied, i_{D3} reaches 100 mA for instance and the resulting voltage v_{DS3} depends on the considered width W_3. With $W_3 = W_{3_1}$, M2 will operate in its linear region, what has to be avoided. If $W_3 = W_{3_2}$, M2 transistor will operate

at the limit between the linear and saturation region. Finally, if $W_3 = W_{3_3}$, the voltages $v_{DS3} = v_{DS2} = v_{DRV}/2$ and M2 will operate in the saturation region as expected.

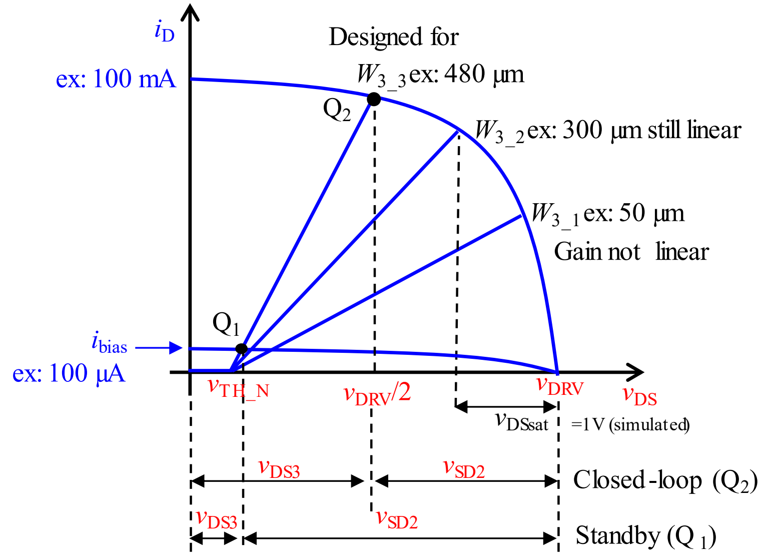


Figure 2.17. Graphical analysis of the circuit in **Figure 2.16**. Point Q will move from Q_1 to Q_2 when the power device is in the dv/dt phase. To make M3 always operate in its saturation region, W_3/W_2=1/2.5, which makes v_{DS3} always less than $v_{DRV}/2$.

Concerning the last transistor M4, it is a multiple of M3 depending on the gain G_N of the 2nd-stage current mirror. In order to implement the desired current gain for the second current mirror, W_4 is simply chosen so that:

$$W_4 = G_N \cdot W_3 = G_P \cdot G_N \cdot W_{1MIN} = G \cdot W_{1MIN} \quad (2.6)$$

2.6 Optimization of CMOS Area

Now that the method to size the transistors M1 to M4 was described, it is important to determine how the total current gain G must be split between the two current mirrors and what the optimized values for the gains G_P and G_N are. It can be noticed that M2, M3 and M4 sizes depend on M1. Transistor M1 can be considered as an elementary building block so the others are multiple of it.

A minimum size for M1 has to be computed in order to reduce the overall surface of the current mirror circuit. In one hand, its size depends on the amplitude of current i_{CS} which in turn depends on the size of the sensing capacitor C_S. On the other hand, the product $G \cdot C_S$ is imposed by the application, i.e. the targeted closed-

loop dv/dt value for a given power transistor. The main goal of this study is to determine the silicon area required depending on the choice of the C_S capacitor value.

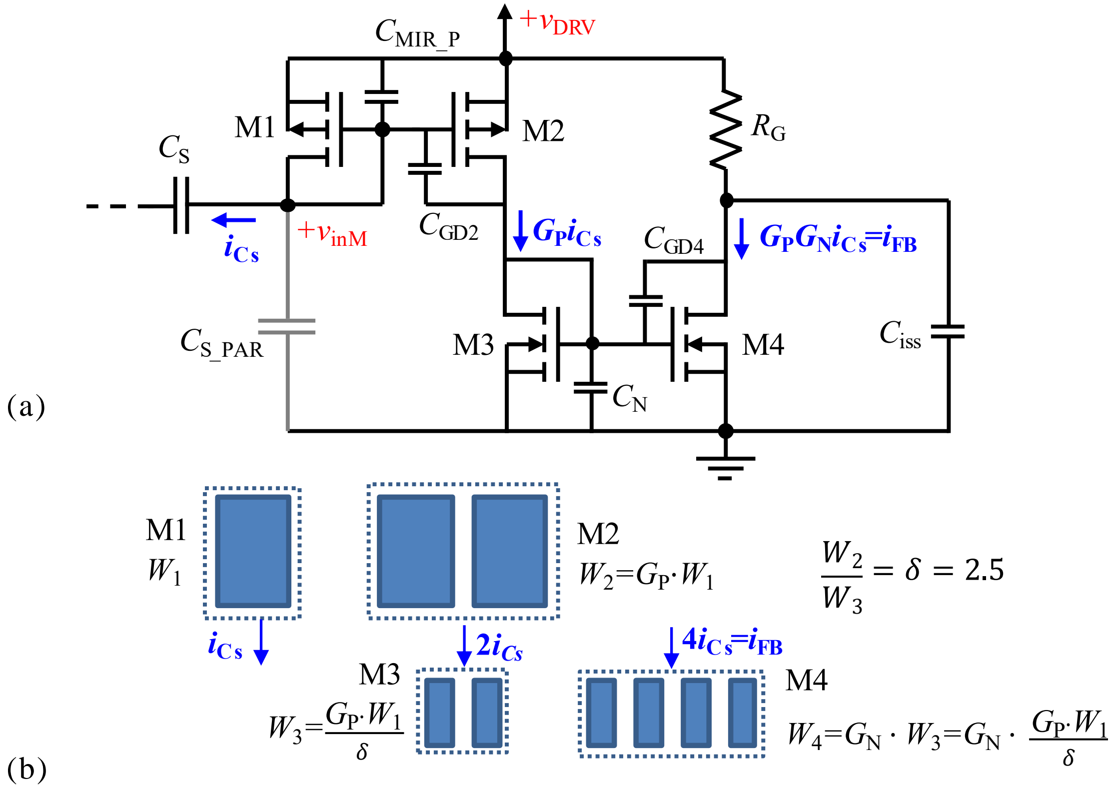


Figure 2.18. (a) Two-stage current mirror with its parasitic capacitances, (b) Circuit layout assuming an area factor of 2.5 between NMOS and PMOS transistors (example with G_P=2 and G_N=2).

To obtain an expression of the silicon area (or also called surface), the reasoning can be done considering **Figure 2.18** (b). Neglecting the effect of lateral diffusion of the source and drain under the gate [118], the surfaces S_{Mp} and S_{Mn} of the PMOS and NMOS current mirrors can be expressed respectively by:

$$S_{M_P} = (1 + G_P) \cdot \alpha \cdot W_{1MIN} \cdot L_{MIN} \tag{2.7}$$

$$\begin{aligned} S_{M_n} &= G_P \cdot (1 + G_N) \cdot \alpha \cdot W_{3MIN} \cdot L_{MIN} \\ S_{M_n} &= (G_P + G) \cdot \frac{\alpha}{\delta} \cdot L_{MIN} \cdot W_{1MIN} \end{aligned} \tag{2.8}$$

where α is the “swell” factor, i.e. the ratio between the active areas and the actual total area required by the transistors.

It should be noted that W_{1MIN} is a function of the size of C_S due to the increase of the current i_{D_CL} when C_S increases. According to (2.2) it is possible to write:

$$W_{1\mathrm{MIN}}(C_S) = \frac{2L_{\mathrm{MIN}}}{\mu_{\mathrm{Peff}} \cdot C_{\mathrm{ox}} \cdot \left(v_{\mathrm{GS_{CL}}} - v'_{\mathrm{TH}}\right)} \cdot \left.\frac{dv_{DS}}{dt}\right|_{CL} C_S$$
$$W_{1\mathrm{MIN}}(C_{\mathrm{S}}) = \frac{1}{J_{\mathrm{P}} \cdot L_{\mathrm{MIN}}} \cdot \left.\frac{\mathrm{d}v_{\mathrm{DS}}}{\mathrm{d}t}\right|_{\mathrm{CL}} \cdot C_{\mathrm{S}} \tag{2.9}$$

$$\text{with} \quad J_{\mathrm{P}} = \frac{\mu_{\mathrm{Peff}} \cdot C_{\mathrm{ox}} \cdot \left(v_{\mathrm{GS_{CL}}} - v'_{\mathrm{TH}}\right)}{2 \cdot L_{\mathrm{MIN}}^2} = \frac{i_{C_{\mathrm{S}}}}{L_{\mathrm{MIN}} \cdot W_{1\mathrm{MIN}}} \tag{2.10}$$

where J_P is a current density factor related to the technology and the choice of the biasing point, i.e. v_{GS_CL}, $dv_{DS}/dt_{(CL)}$ is the targeted closed-loop turn-on dv/dt value.

Therefore, for both PMOS and NMOS current mirror areas, the total value is the sum of the previous values that can be written as:

$$\frac{\mathrm{d}v_{\mathrm{DS}}}{\mathrm{d}t} = -\frac{v_{\mathrm{DRV}} - v_{\mathrm{M}}}{R_{\mathrm{GTOT}} \cdot C_{\mathrm{rss}}} + \frac{i_{\mathrm{FB}}}{C_{\mathrm{rss}}} = -\frac{(v_{\mathrm{DRV}} - v_{\mathrm{M}})}{R_{\mathrm{GTOT}} \cdot (C_{\mathrm{rss}} + G \cdot C_{\mathrm{S}})} \tag{2.11}$$

$$S_{\mathrm{M}} = S_{\mathrm{M_P}} + S_{\mathrm{M_N}} = \left((1 + G_{\mathrm{P}}) + G_{\mathrm{P}}(1 + G_{\mathrm{N}})\frac{\mu_{\mathrm{Peff}}}{\mu_{\mathrm{Neff}}}\right)\alpha \cdot W_{1\mathrm{MIN}} \cdot L_{\mathrm{MIN}} \tag{2.12}$$

In the case the sensing capacitor C_S is also embedded in silicon, the area S_{C_S} required to implement it can be expressed as:

$$S_{C_{\mathrm{S}}} = \frac{C_{\mathrm{S}}}{C'_{\mathrm{S}}} \tag{2.13}$$

where C_S' is the capacitance per surface unit [116] depending on the CMOS technology parameters and the desired breakdown voltage.

In the case the sensing capacitor C_S is also embedded in the silicon, the total surface is the surface of both current mirrors and the added capacitor:

$$S_{\mathrm{tot}} = S_{C_{\mathrm{S}}} + S_{\mathrm{M}} \tag{2.14}$$

Replacing W_{1MIN} from (2.2) in the expression (2.12) it is possible to obtain:

$$S_{\mathrm{tot}}(C_{\mathrm{S}}) = \underbrace{\frac{1}{\delta}\frac{\alpha}{J_{\mathrm{P}}}\left.\frac{\mathrm{d}v_{\mathrm{DS}}}{\mathrm{d}t}\right|_{\mathrm{CL}} C_{\mathrm{GDeq}}}_{\text{Plateau}} + \underbrace{\left(\left(1 + G_{\mathrm{P}}\left(1 + \frac{1}{\delta}\right)\right)\frac{\alpha}{J_{\mathrm{P}}}\left.\frac{\mathrm{d}v_{\mathrm{DS}}}{\mathrm{d}t}\right|_{\mathrm{CL}} + \frac{1}{C'_{\mathrm{S}}}\right) C_{\mathrm{S}}}_{\text{Proportional to } C_{\mathrm{S}}} \tag{2.15}$$

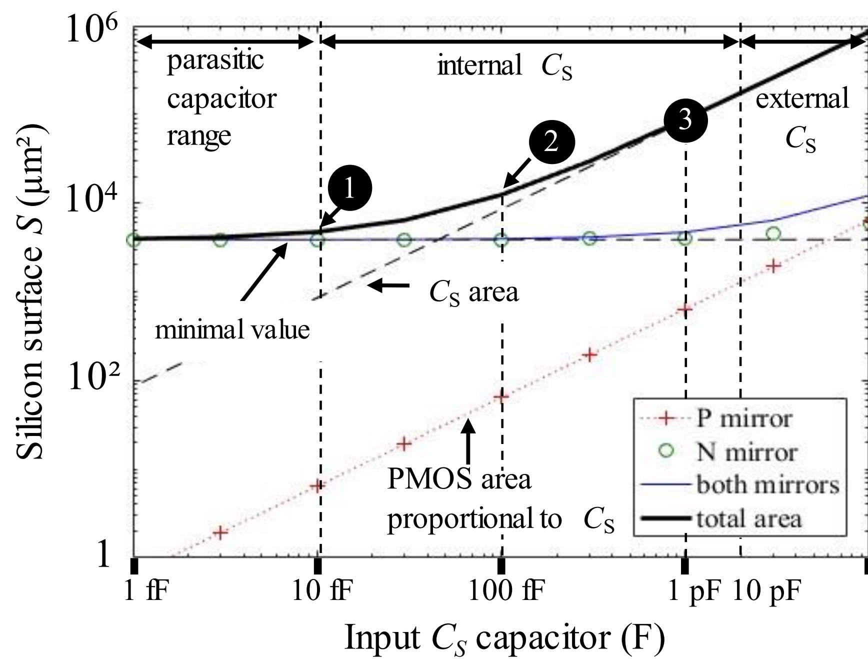
where C_{GDeq} is the virtual gate-to-drain capacitor added to the power transistor, i.e. $G \cdot C_S$.

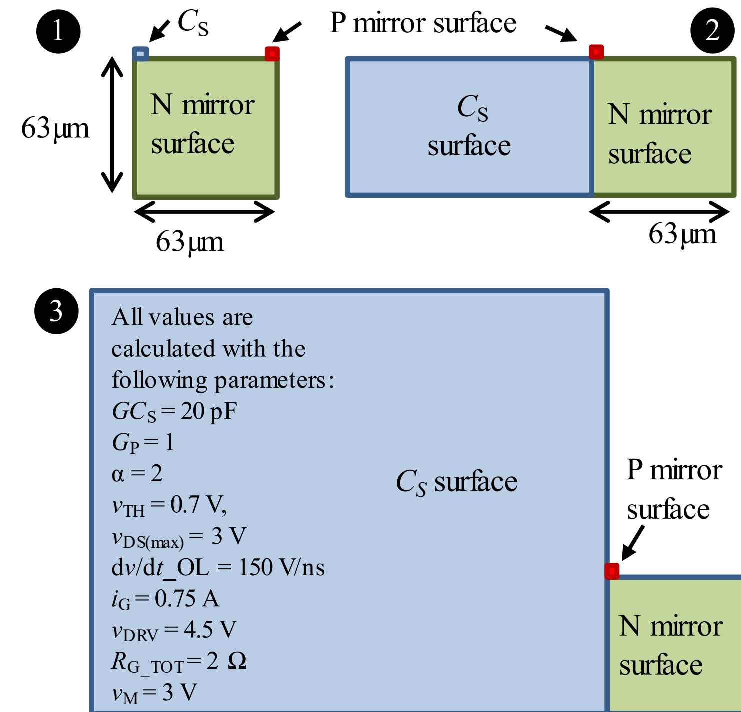
The resulting expression (2.15) shows how the total silicon area is linked with the different parameters involved in the system: the technology, the application, the

capacitor C_S and the current gain G split among the two stages of the control loop. A minimum value is reached at low C_S values and is only related to the technology and the application parameters. The second term is proportional to the value of C_S.

Figure 2.19 shows the silicon area required depending on the capacitor C_S values for a given product $G \cdot C_S$=20 pF. This figure is obtained using MATLAB™ computation. It should be noted that only C_S values higher than 10 fF have to be considered, the other values being lower than the parasitic capacitors of the integrated circuit. Three points are illustrated. Points 1 and 2 are low and middle C_S values providing smaller silicon area for the circuit. Point 3, for high C_S value, clearly shows that no benefit for the mirror area is obtained.

Figure 2.20 shows the surfaces extracted from CADENCE™ Layout for the three points considered. The CADENCE™ results are very close to the surface values computed with our equation (2.15).





(a) (b)

Figure 2.19. (a) Total silicon area as a function of the sensing capacitor C_S. The product $G{\cdot}C_S$ is kept constant and represents a given attenuation in dv/dt. (b) Visual representation of the points 1, 2 and 3 showing the total area depends predominantly on the N Mirror area for point 1, and for the sensing capacitor area for point 3.

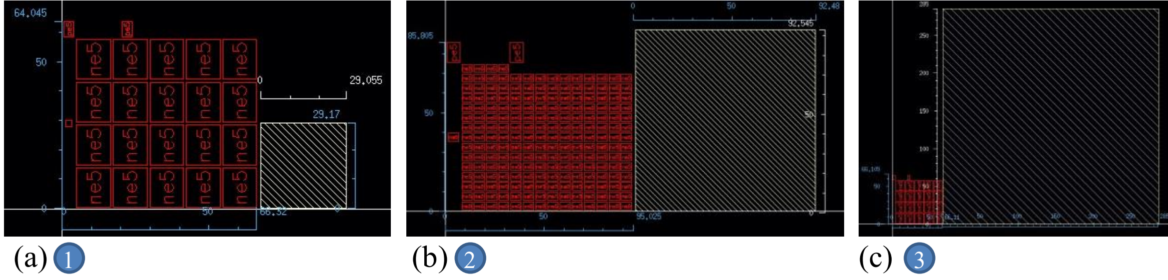


Figure 2.20. Surface extracted from CADENCE™ Layout for the points (a) 1, (b) 2 and (c) 3. The resulting surface value is the surface of the automatically generated transistors plus the estimated surface of the sensing capacitor C_S. In practice it will be required more surface for the routing with metal layers to interconnect the transistors.

Minimum surface plateau:

As previously mentioned, it is observed a minimum value of surface for low values of sensing capacitor C_S. Its expression is the following:

$$S_{\text{tot}}(C_S)_{(\min)} = \frac{1}{\delta} \cdot \frac{\alpha}{J_P} \cdot \left.\frac{\mathrm{d}v_{\text{DS}}}{\mathrm{d}t}\right|_{\text{CL}} \cdot C_{\text{GDeq}} \qquad (2.16)$$

Because the dv/dt in closed-loop is dependent on the value of $G \cdot C_S$, which is the virtual added capacitance to the drain-to-gate connections of the power transistor, it should be interesting to provide also the expression of this plateau (in eq. (2.15)) with the parameters related to the GD itself. The value of dv/dt is related to the application by the equation:

$$\left.\frac{\mathrm{d}v_{\text{DS}}}{\mathrm{d}t}\right|_{\text{CL}} \cdot C_{\text{GDeq}} = \frac{i_{R_G}}{C_{\text{GD}} + G \cdot C_S} \cdot G \cdot C_S \qquad (2.17)$$

where i_{R_G} is the current provided by the driver and C_{GD} is its intrinsic gate-to-drain capacitor of the power transistor.
The value of i_{R_G} is expressed by:

$$i_{R_G} = \frac{(v_{\text{DRV}} - v_{\text{M}})}{R_{\text{GTOT}}} \qquad (2.18)$$

An attenuation factor can be defined as follows:

$$A_{tt} = \frac{\left.\frac{\mathrm{d}v_{\mathrm{DS}}}{\mathrm{d}t}\right|_{\mathrm{OL}}}{\left.\frac{\mathrm{d}v_{\mathrm{DS}}}{\mathrm{d}t}\right|_{\mathrm{CL}}} = 1 + \frac{G \cdot C_{\mathrm{S}}}{C_{\mathrm{rss}}} \tag{2.19}$$

Therefore the main equation of the minimum surface plateau become:

$$S_{\mathrm{tot}}(C_{\mathrm{S}})_{(min)} = \frac{1}{\delta}\frac{\alpha}{J_{\mathrm{P}}} i_{\mathrm{R_G}} \frac{1}{1 + \frac{C_{\mathrm{rss}}}{G \cdot C_{\mathrm{s}}}} \tag{2.20}$$

This expression is plotted in **Figure 2.21**. It clearly shows that when the term $G \cdot C_{\mathrm{S}}$ is higher than the intrinsic gate-to-drain capacitor C_{rss} of the power transistor, the plateau reaches a maximum level that only depends on the effective mobility δ ratio, the swell factor α, the PMOS current density J_{P} and the current $i_{\mathrm{R_G}}$ provided by the driver.

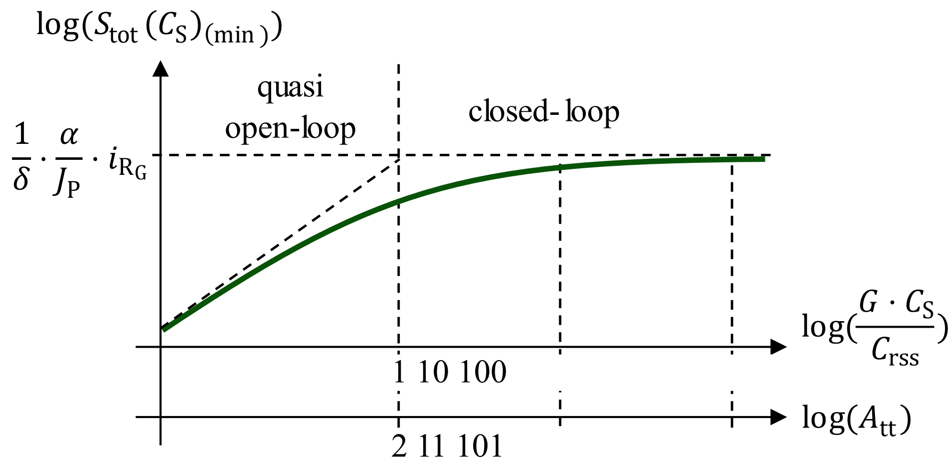


Figure 2.21. The minimum surface presents a plateau that can be analyzed as a function of the gain G and capacitance C_{S} or the desired dv/dt attenuation.

Table 2.1 provides several values obtained with $C_{\mathrm{rss}} = 6$ pF and $C_{\mathrm{S}} = 1$ pF, for different choices of dv/dt attenuation factor, where Max indicates the maximum possible value for the surface plateau. Using AMS0.35 CMOS technology, the value of Max is 4.8×10^{3} µm².

TABLE 2.1. THEORETICAL EXPECTED D*V*/D*T* ATTENUATION

Attenuation factor (A_{tt})	dv/dt attenuation	$G{\cdot}C_S/C_{rss}$	$G{\cdot}C_S$ (C_{rss}=2 pF) For SiC transistor	G (C_S=1 pF) if r_p=1*	$S_{tot}(C_S)_{(min)}$
1	0%	0	0	0	
4/3	25%	1/3	2/3 pF	2	Max×1/4
2	50%	1	2 pF	6	Max×1/2
4	75%	3	6 pF	18	Max×3/4
5	80%	4	8 pF	24	Max×4/5

*Parameter r_p is defined in chapter 3 section 3.4.2 (Feedback Loop Performance Ratio)

2.7 Bandwidth optimization

In order to address very fast transient response, the feedback control loop should provide the highest bandwidth possible. In order to correctly size the transistors M1 to M4, an expression of the bandwidth as a function of the gain G and the capacitor C_S has to be determined. For a given dv/dt attenuation, the product $G.C_S$ has to be considered constant. We will see that the bandwidth value depends on the gains G_P, G_N and on the value of the sensing capacitor C_S.

2.7.1 One stage current mirror

To determine the bandwidth of the feedback loop, it is important to consider a small-signal variation around a biasing point. In our case, we want to study the loop during a dv/dt turn-on event, so we should consider first that a current i_{Cs} is already established in the sensing capacitor C_S and an output feedback loop current equal to $G{\cdot}i_{Cs}$ is sunk by the transistor M4.

Before analyzing the complete system with all its complexity, we propose to study in a first step a simple current mirror. The circuit is shown in **Figure 2.22**.

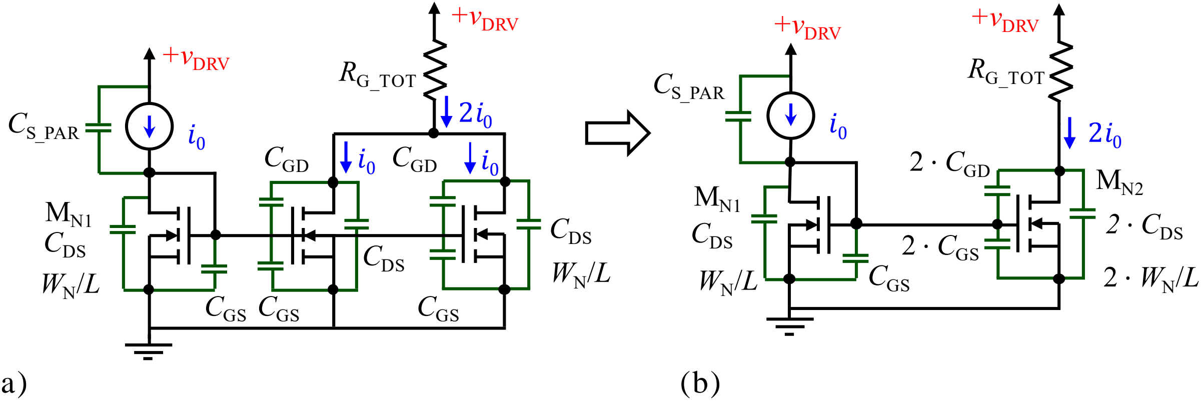


Figure 2.22. (a) A simple current mirror with a gain G=2. (b) The resulting equivalent circuit with the capacitances C_{GD}, C_{GS} and C_{DS} are multiplied by the gain of the current mirror, 2 in this example.

This figure shows the different transistors used and the several intrinsic capacitances that have to be taken into account in our analysis. The impedance of the gate node and the total capacitor connected to this node have to be considered. If one current mirror copies 2 times its input current, it will present on the common gate node of the transistors 3 times the intrinsic capacitance C_{GS} of one elementary transistor with size $W_N \times L$.

Using this reasoning, if the current mirror gain become G_N, the total capacitance seen at the gate node [102] of the NMOS transistors is expressed by (2.21).

$$C_N = (1 + G_N) \cdot C_{GS} + G_N \cdot C_{GD}(1 - |a_v|) + C_{DS} + C_{S_{PAR}} \tag{2.21}$$

where a_v is the small-signal voltage gain of the common-source stage made by M_{N2} (the second NMOS).

$$a_v = -\frac{g_{m_{N2}}}{G_{DS2} + \frac{1}{R_{G_TOT}}} = -\frac{G_N \cdot g_{m_{N1}}}{G_N \cdot \lambda \cdot i_0 + \frac{1}{R_{G_TOT}}} \tag{2.22}$$

where g_{mN} is the transconductance of the transistor, G_{DS} is the drain-to-source admittance, λ is the channel-length modulation parameter and i_0 is the input current of the current mirror.

Assuming R small and in the same order of magnitude as $1/g_{mN2}$, parameter a_v value can be considered close to -1.

2.7.2 The intrinsic capacitances of the CMOS transistors.

Capacitors C_{GS}, C_{GD} and C_{DS}, are the intrinsic capacitances of the CMOS transistors [119]. Their values can be found in the confidential documents of a given technology design kit and are accurately computed using the CADENCE™ simulator. They are expressed either per unit of area or per length, and the dimensions that they depend on are shown in **Figure 2.23** below.

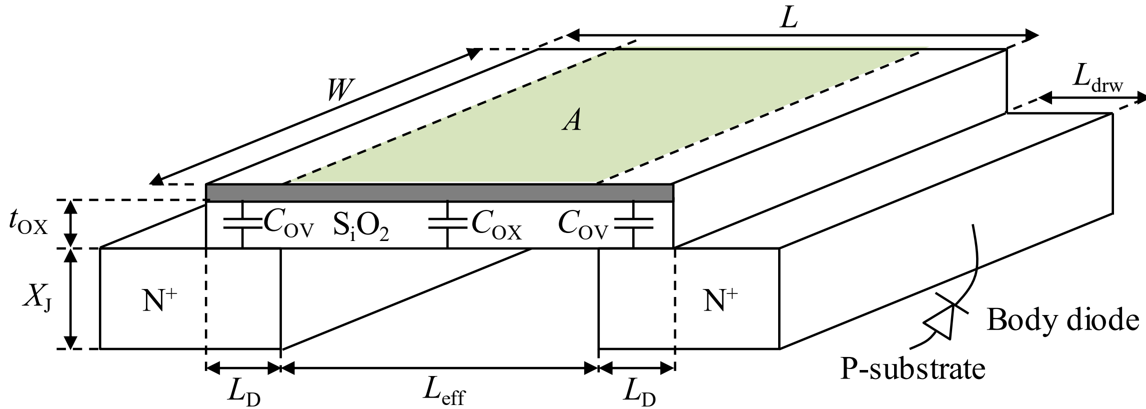


Figure 2.23. Sectional view of a lateral MOSFET showing the various capacitors to consider.

The capacitances C_{GS} of NMOS and PMOS are related to C_{OX} and computed using equations (2.23) . Parameter C_{OX}, which depends on the oxide thickness t_{OX}, is always expressed per unit of surface (µF/µm^2).

$$\begin{cases} C_{GS_N} = k \cdot C_{OX_N} \cdot W_N \cdot L_{eff} \\ C_{GS_P} = k \cdot C_{OX_P} \cdot W_P \cdot L_{eff} \end{cases} \quad \text{and} \quad \begin{cases} C_{OX_N} = \dfrac{\varepsilon_{SiO_2}}{t_{OX_N}} \\ C_{OX_P} = \dfrac{\varepsilon_{SiO_2}}{t_{OX_P}} \end{cases} \qquad (2.23)$$

where k is a parameter dependent on the shape of the channel, i.e. equal to ½ if the transistor operates in its ohmic region and 2/3 in its pinched-off region.

The capacitances C_{GD} of NMOS and PMOS are related to C_{OV} and computed using equations (2.24). Parameter C_{OV}, which depends both on the oxide thickness t_{OX} and the lateral diffusion L_D, is always expressed per unit of length (µF/µm).

$$\begin{cases} C_{GD_N} = C_{OV_N} \cdot W_N \\ C_{GD_P} = C_{OV_P} \cdot W_P \end{cases} \qquad (2.24)$$

Regarding the capacitance C_{DS}, it is related to the reverse-biased body diode of the transistor and is composed of 5 elements displayed in **Figure 2.24**. Notice that

there is no capacitance to consider between the source and the substrate because these two pins are always connected together in our circuit.

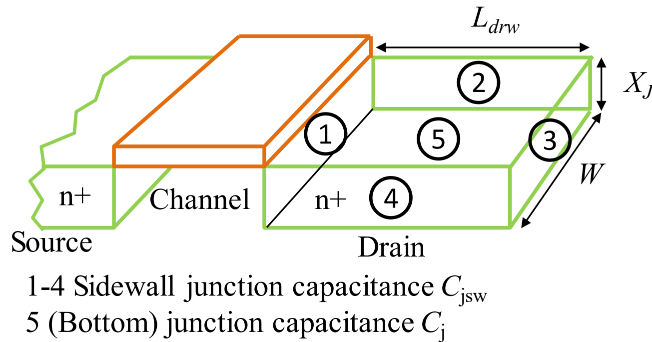


Figure 2.24 The intrinsic capacitance C_{DS} is made of 5 elements.

It should be noted that the contributions of the two surfaces 2 and 4 are neglected because the shape factor W/L in this project is in the order of magnitude of 1000.

Considering the bottom and sidewall capacitances shown in **Figure 2.24**, one can obtain the following expressions:

$$\begin{cases} C_{DS_N} = C_{J_N} \cdot W_N \cdot L_{drw} + C_{JSW_N} \cdot 2 \cdot (W_N + L_{drv}) \approx C_{D_N} \cdot W_N \\ C_{DS_P} = C_{J_P} \cdot W_P \cdot L_{drw} + C_{JSW_{NP}} \cdot 2 \cdot (W_P + L_{drv}) \approx C_{D_P} \cdot W_P \end{cases} \quad (2.25)$$

where C_D represents the equivalent linear voltage-dependent drain-to-source capacitance of the transistor (µF/µm).

Notice that these values of capacitance are voltage dependent. This dependency is shown in **Figure 2.25**.

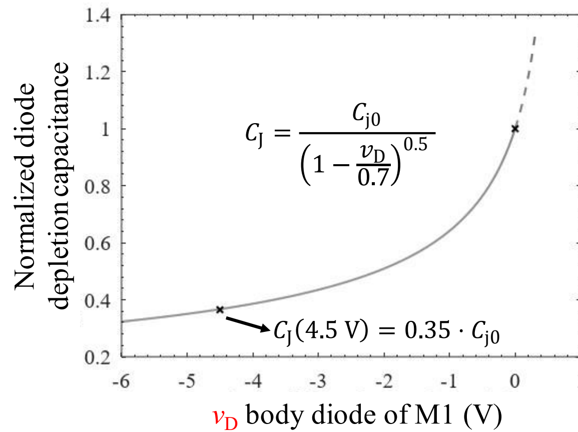


Figure 2.25. Diode junction capacitance vs. its reverse voltage biasing. It can be noted that it falls to 35% of its 0 V value when it is reversely biased to the power supply v_{DRV} voltage of 4.5V.

The reverse-biased diode capacitance depends on the applied voltage. In the case of this work, if the voltage node v_{inM} is biased to operate at maximum excursion, i.e. $v_{inM}=v_{DRV}=4.5$ V, this capacitance value is reduced to 35% of its 0V-biased value.

After some pages regarding the intrinsic capacitances of the CMOS transistors, it will follow the calculation of the bandwidth of the feedback loop.

A transfer function of only one stage current mirror is therefore

$$\frac{i_{\mathrm{DMn2}}}{i_{\mathrm{DMn2}}} = G_N \cdot \frac{\frac{C_{\mathrm{GD_P}}}{g_{\mathrm{mP}}} \cdot s}{1 + \tau_{\mathrm{P}} \cdot s} \tag{2.26}$$

Where it is possible to identify one zero in high frequency where the current could pass trough C_{GD_P} and one pole with time-constant associated to τ_P.

The main time-constant of the circuit τ_P is provided by the product of the total capacitance C_N seen at the gates of the transistors with the impedance presented by this node. Due to the diode-connected transistor, it is obvious to demonstrate that this impedance is equal to $1/g_{mN1}$. Therefore, the time-constant of the NMOS current mirror is provided by the following equation:

$$\tau_{\mathrm{N}} = \frac{C_{\mathrm{N}}}{g_{\mathrm{m_{N1}}}} \tag{2.27}$$

The bandwidth of the NMOS current mirror is then defined by:

$$f_{\mathrm{c_N}} = \frac{1}{2 \cdot \pi \cdot \tau_{\mathrm{N}}} \tag{2.28}$$

Replacing C_N in (2.27) by (2.21) we obtain:

$$\tau_{\mathrm{N}} = \frac{(1+G_{\mathrm{N}}) \cdot k \cdot C_{\mathrm{OX_N}} \cdot W_{\mathrm{N}} \cdot L_{\mathrm{eff}} + G_{\mathrm{N}} \cdot C_{\mathrm{OV_N}} \cdot W_{\mathrm{N}} \cdot (1-a_{\mathrm{v}}) + C_{\mathrm{D_N}} \cdot W_{\mathrm{N}} + C_{\mathrm{in}}}{g_{\mathrm{m_{N1}}}} \tag{2.29}$$

2.7.3 Bandwidth related to transition frequency of a technology

The definition of transition frequency (f_T) is provided in [115] (page 715 from 7th edition, or chapter 10.2) or [116] (page 34 from 5th edition or chapter 1.7.2). Or also [102] (chapter 1.2 page 38 from 2nd edition).

$$f_T = \frac{g_{\mathrm{m}}}{2\pi \cdot (C_{\mathrm{GS}} + C_{\mathrm{GD}})} \tag{2.30}$$

There is a link between the bandwidth of the current mirror and the parameters of the technology. We want to find an expression giving the dependency of the bandwidth with the transition frequency (f_T) of the technology which is a very convenient parameter to characterize the dynamic performances of a technology.

Assuming that the transistor operates at a high drain current and neglecting the input parasitic capacitance $C_{S_{PAR}}$, the expression (2.29) can be rewritten as:

$$\tau_N = \frac{\left((1+G_N)k \cdot C_{OX_N} \cdot W_N \cdot L_{eff} + G_N \cdot C_{OV_N} \cdot W_N(1-a_v) + C_{D_N} \cdot W_N\right)}{\frac{W_N}{2L_{eff}} \cdot \mu_{effN} \cdot C_{OX_N}} \quad (2.31)$$

Factoring and simplifying the term W_N in the numerator and denominator yields to:

$$\tau_N = \left((1+G_N)kC_{OX_N}L_{eff} + G_N C_{OV_N}(1-a_v) + C_{D_N}W_N\right)\frac{2L_{eff}}{2\mu_{effN}C_{OX_N}} \quad (2.32)$$

The time-constant is no longer related to the width W_N of the transistors. Its expression can be rewritten as:

$$\tau_N = \frac{1}{2 \cdot \pi \cdot f_{T_N}} \frac{\left((1+G_N) \cdot k \cdot C_{OX_N} \cdot L_{eff} + G_N \cdot C_{OV_N} \cdot (1-a_v) + C_{D_N}\right)}{k \cdot C_{OX_N} \cdot L_{eff} + C_{OV}} \quad (2.33)$$

$$\text{with } f_{T_N} = \frac{g_{m_N}}{2\pi \cdot (C_{GS}+C_{GD})} \quad (2.34)$$

where f_{T_N} is the transition frequency of the technology for the transistors NMOS and represents the maximum frequency that can be reached with an active NMOS transistor.

Considering $C_{OX} >> C_D$ and C_{OV}, it is possible to neglect the two right-hand terms of the expression, which leads to:

$$\tau_N \approx \frac{1}{2 \cdot \pi \cdot f_{T_N}}\left((1+G_N) + \frac{C_{OV_N}}{k \cdot C_{OX_N} \cdot L_{eff}} \cdot G_N \cdot (1-a_v)\right) \quad (2.35)$$

Again, neglecting the effect of the C_{OV} capacitance, it is possible to simplify and obtain:

$$\tau_N \approx \frac{1+G_N}{2 \cdot \pi \cdot f_{T_N}} \quad (2.36)$$

Finally, a relatively simple but very meaningful expression is obtained relating the transition frequency of a technology (f_T) with the cutoff frequency of one mirror current (f_{c_N}) composed by 1+G_N NMOS transistors. A good estimation of the resulting bandwidth is provided by the following expression:

$$f_{c_{N_{est}}} = \frac{f_{T_N}}{1 + G_N} \tag{2.37}$$

Figure 2.26 shows the good correlation existing between the simulated points obtained using CADENCE™ and the estimation of the bandwidth expressed by (2.37) for different values of current gain G_N.

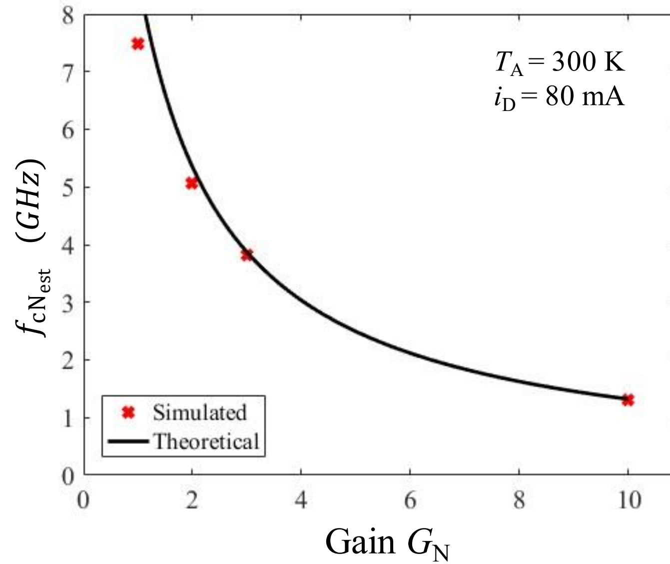


Figure 2.26. The current transfer function bandwidth of one stage current mirror as a function of its gain.

As a conclusion, the dynamic performances of one stage current mirror is directly linked with the technology parameters. For a targeted application, the choice of the technology to implement the driver circuit should be made accordingly.

The current mirrors could be implemented using $L_{\mathrm{MIN}} = 0.18$ µm for the transistors M1 to M3 but M4 needs to withstand the v_{DRV} voltage. But those studies were not carried out. See **Figure 2.27** for the values of cutoff frequency for the technologies GaAs, InP and silicon as a function of gate length published in 2008 by [120]. The values marked correspond to $L_{\mathrm{MIN}} = 0.18$ µm for the transistors with $v_{\mathrm{DSMAX}} = 1.8$ V and $L_{\mathrm{MIN}} = 0.5$ µm for $v_{\mathrm{DSMAX}} = 5$ V. For $L_{\mathrm{MIN}} = 0.5$ µm the transition frequency in this paper is 25 GHz, a value not different from the simulated values from XFAB0.18 design kit with 18.9 GHz.

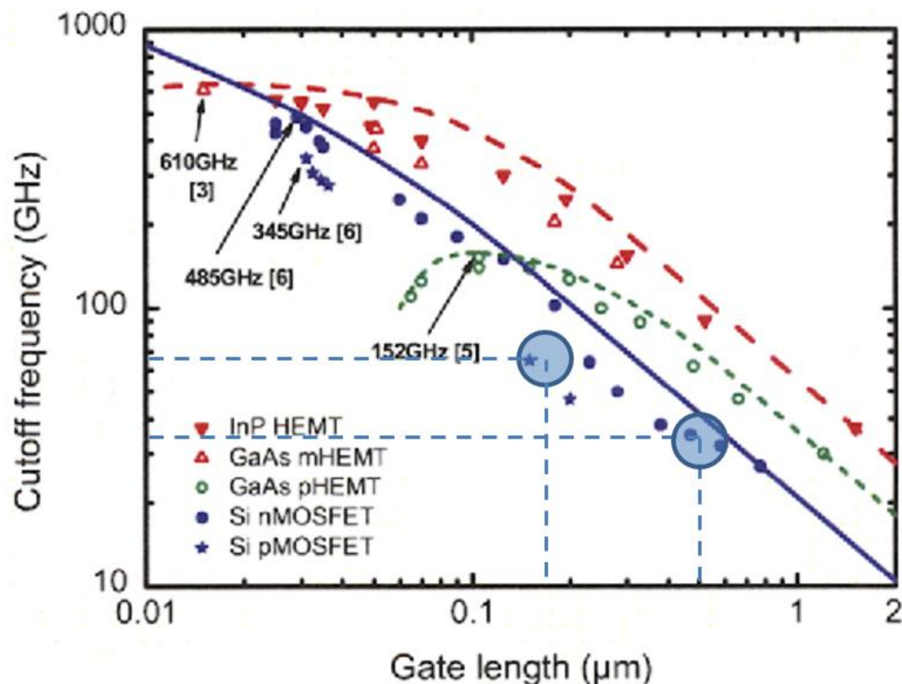


Figure 2.27. Cutoff frequency vs gate length *L* of experimental GaAs pHEMTs, GaAs mHEMTs, InP HEMTs, and Si MOSFETs (n-channel and p-channel) [120].

2.7.4 Two stage current mirror

The complete circuit of the current feedback loop involving two current mirror stages has to be considered now. We know that the value of the bandwidth depends on the values of the gains G_P and G_N of the two current mirrors. These two gains are also dependent on the value of the sensing capacitor C_S. Indeed, for a given d*v*/d*t* attenuation, the product $G \cdot C$s has to be considered constant. In order to correctly size the transistors to address very fast transient response, one expression of the bandwidth as a function of the current mirror gains and C_S has to be determined.

From a one stage current mirror small-signal representation [102], (chapter 4.2.1: High Frequency MOS Small-Signal Model, page 165 from 2nd edition) a similar analysis can be done for two stages of current mirrors. A small-signal model is represented in **Figure 2.28** below. It is useful to carry out the feedback loop analysis which has been published in [114].

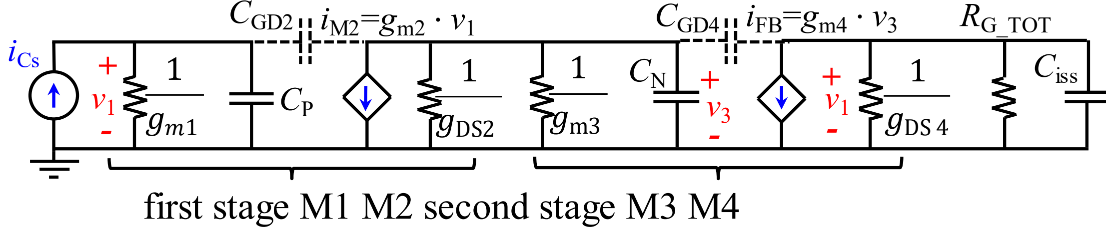


Figure 2.28. Small-signal model of two stages of current mirrors neglecting source-to-bulk capacitance (sources of NMOSs are connected to the lowest potential gnd).

The total intrinsic capacitances at the gate of the PMOS and NMOS current mirrors are respectively given by (2.38) and (2.39).

$$C_{\mathrm{P}} = (1 + G_{\mathrm{P}}) \cdot C_{\mathrm{GS_P}} + G_{\mathrm{P}} \cdot C_{\mathrm{GD_P}} \cdot (1 - a_{\mathrm{v}}) + C_{\mathrm{DS_P}} + C_{\mathrm{S_{PAR}}}$$
$$C_{\mathrm{P}} \cong (1 + G_{\mathrm{P}}) \cdot C_{\mathrm{GS_P}} + C_{\mathrm{S_{PAR}}} \tag{2.38}$$

$$C_{\mathrm{N}} = (1 + G_{\mathrm{N}}) \cdot C_{\mathrm{GS_N}} + G_{\mathrm{N}} \cdot C_{\mathrm{GD_N}} \cdot (1 - a_{\mathrm{v}}) + G_{\mathrm{P}} \cdot C_{\mathrm{DS_N}} + G_{\mathrm{P}} \cdot C_{\mathrm{DS_P}}$$
$$C_{\mathrm{N}} \cong (1 + G_{\mathrm{N}}) \cdot G_{\mathrm{P}} \cdot C_{\mathrm{GS_N}} + G_{\mathrm{P}} \cdot C_{\mathrm{DS_P}} \tag{2.39}$$

where $C_{\mathrm{S_PAR}}$ represents the parasitic capacitance present at the LV plate of the sensing capacitor C_{S}, a_{v} is the small-signal voltage gains of the common-source stages made by M2 and M4 respectively, the value close to one.

The current gain transfer function is expressed by:

$$\frac{i_{\mathrm{FB}}(s)}{i_{\mathrm{Cs}}(s)} = G_{\mathrm{P}} \cdot G_{\mathrm{N}} \cdot \frac{1 - \frac{C_{\mathrm{GD2}}}{g_{\mathrm{m2}}} \cdot s}{1 + \tau_{21} \cdot s} \cdot \frac{1 - \frac{C_{\mathrm{GD4}}}{g_{\mathrm{m2}}} \cdot s}{1 + \tau_{43} \cdot s} \tag{2.40}$$

where g_{mi} and g_{DSi} are respectively the transconductances and the drain-to-source admittances of transistors M1 to M4, τ_{21} and τ_{43} are the time-constants of the two current mirrors.

Fortunately, the expressions of the total capacitances C_{P} and C_{N} shown by the gate nodes of the PMOS and NMOS transistors can be drastically simplified.

To calculate the bandwidth, knowing the capacitances of the circuit, the associated dynamic impedances have to be computed. Mainly, the impedances seen at the gate nodes are provided by the diode-connected transistors M1 and M3. Their values are related to the transconductances g_{m}. The time-constants τ can be written as follows:

$$\tau_{\mathrm{P}} = \frac{C_{\mathrm{P}}}{g_{\mathrm{m1}}} \quad \text{and} \quad \tau_{\mathrm{N}} = \frac{C_{\mathrm{N}}}{g_{\mathrm{DS2}} + g_{\mathrm{m3}}} \tag{2.41}$$

where g_{m1} and g_{m3} are M1 and M3 transconductances and g_{DS2} is the drain-to-source admittance of M2.

It should be noted that the admittances g_{DS1} and g_{DS3} of transistors M1 and M3 are not mentioned in the study because they are negligible compared to g_{m1} and g_{m3}, respectively. Then, the cutoff frequencies for the PMOS and NMOS current mirrors are expressed by:

$$f_{c_P} = \frac{1}{2\pi\tau_P} \quad \text{and} \quad f_{c_N} = \frac{1}{2\pi\tau_N} \tag{2.42}$$

It should be noted that increasing the width W of the transistor increases both g_m and the intrinsic capacitor values. Then, for a given length L, the transition frequency is a constant term. It has been previously shown that the cutoff frequency of the current mirrors can be related to this transition frequency. Because M1 and M3 are diode-connected transistors, they always work in their saturation regime therefore C_{GD} can be neglected compared to C_{GS}. Now, neglecting the contributions of C_{S_PAR} and C_{DSp} in (2.41) and (2.42), one can estimate:

$$f_{c_N} \cong \frac{f_{T_N}}{1 + G_N} = f_{c_{N_{est}}} \tag{2.43}$$

$$f_{c_P} \cong \frac{1}{\delta} \cdot \frac{f_{T_P}}{1 + G_P} = f_{c_{P_{est}}} \tag{2.44}$$

Because the two 1st-order stages are cascaded, we can assume that the global time-constant of the feedback control loop can be computed with the following equation:

$$\tau_{tot} = \sqrt{\tau_N^2 + \tau_P^2} \tag{2.45}$$

Thus, an expression of the bandwidth using a geometrical averaging of the two-time-constants is proposed:

$$\frac{1}{f_{c_{est}}} = \sqrt{\frac{1}{f_{cN_{est}}^2} + \frac{1}{f_{cP_{est}}^2}} \tag{2.46}$$

The resulting estimated bandwidth $f_{c_{est}}$ of the circuit becomes:

$$f_{c_{est}} = \frac{f_{T_N}}{\sqrt{\delta^2 \cdot (1 + G_P)^2 + \left(1 + \frac{G}{G_P}\right)^2}} \quad (2.47)$$

It is observed that this parameter is related to the transition frequency f_{T_N} and, depending on the distribution of the gain G among the two current mirror gains G_P and G_N, the overall feedback loop bandwidth f_c changes. An optimal distribution can be identified. **Figure 2.29** shows the optimal choice of G_P depending on the value of G. Note that the higher the value of G, the lower the bandwidth.

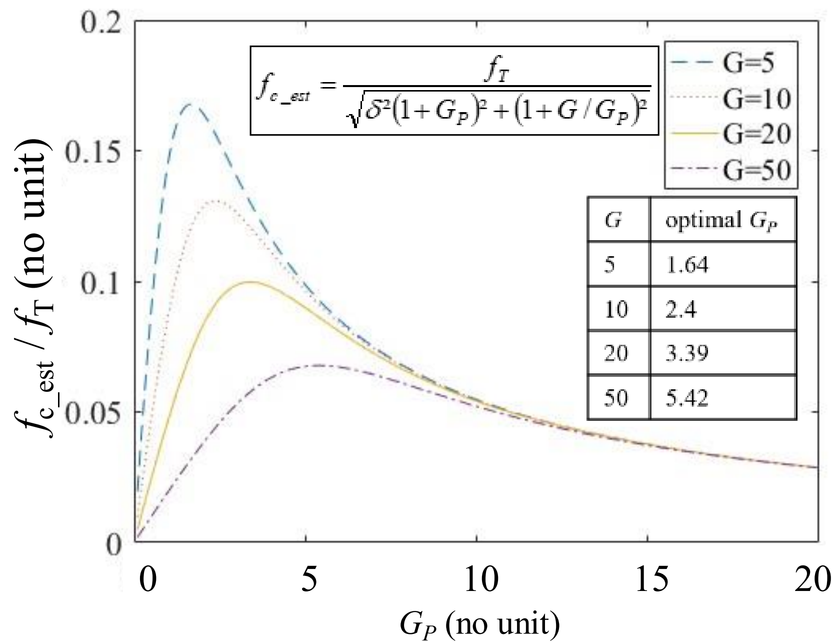


Figure 2.29. Normalized cutoff frequency of the feedback loop as a function of the PMOS mirror gain G_P for several values of G.

Now, in order to accurately compute f_c without any assumption, all the intrinsic capacitances present in (2.38) and (2.39) and the parasitic capacitance introduced by C_S are taken into account. **Figure 2.30** shows Matlab™/Octave™ computations using the appropriate technology parameters with $G{\cdot}C_S$ equals to 10 pF. Simulation results using C_S=100 fF, 300 fF and 1 pF confirm the theoretical projections.

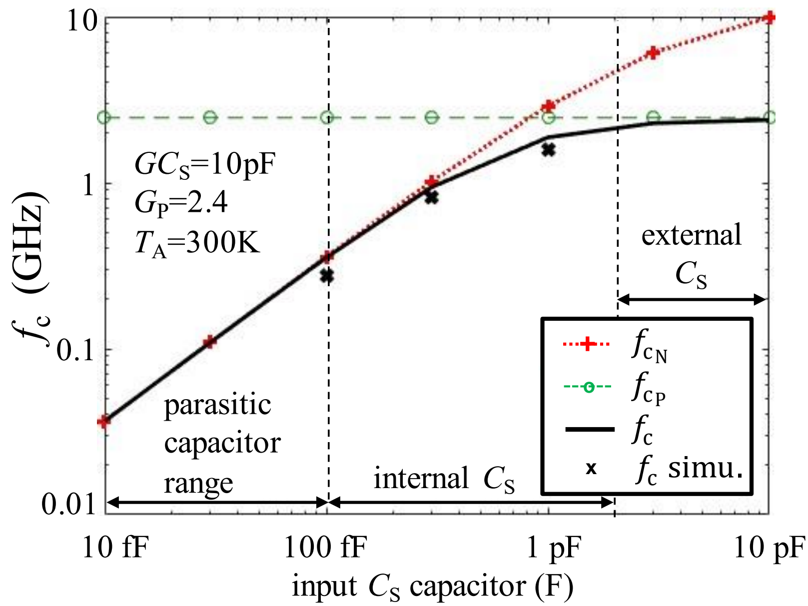


Figure 2.30. Feedback loop bandwidth as a function of C_S for a constant $G{\cdot}C_S$ = 10pF.

One can note that the higher the sensing capacitor C_S, the higher the bandwidth for the feedback loop. At high C_S values a plateau is reached, and no benefit is obtained increasing the value of the d*v*/d*t* sensing capacitor. A trade-off between the required silicon surface and the dynamic performances has to be considered. The input capacitor can have any value, however, no more than 2 pF were integrated in the chip so the external capacitor range of more than 2 pF is suggested (**Figure 2.30**) and tests with higher value uses external high voltage capacitors for the d*v*/d*t* sensing.

With CMOS AMS 0.18µm technology, a CADENCE™ small-signal simulation, shown in **Figure 2.31**, demonstrates a bandwidth close to 550 MHz (-3 dB gain) for the two-step current mirror with a current gain G = 20 and considering an input current made of a biasing current i_{bias} = 2 mA and a i_{Cs} current of 12 mA generated by a constant 6 V/ns d*v*/d*t* imposed to the HV plate of the sensing capacitor C_S = 2 pF.

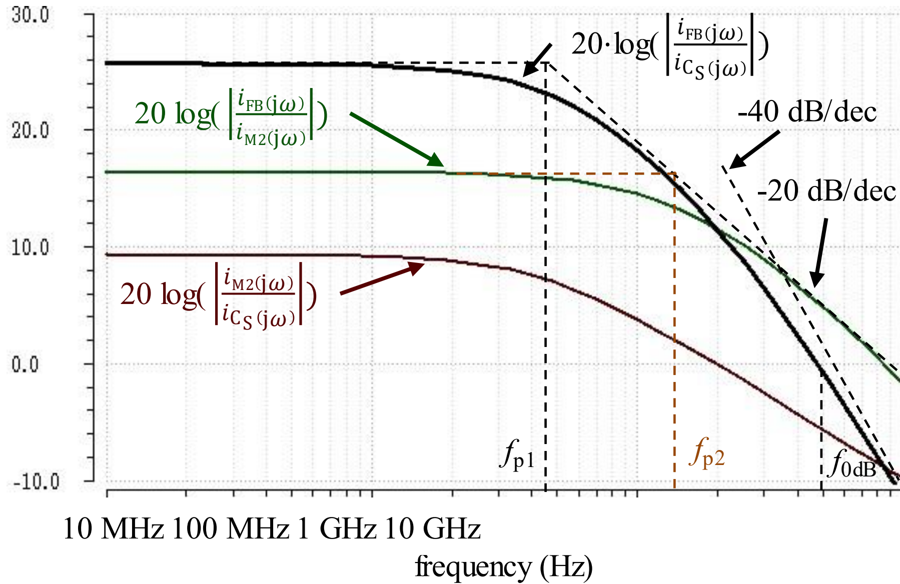


Figure 2.31. CADENCE™ simulation of the two-step current mirror transfer function (i_{bias} = 2 mA, dv/dt = 6 V/ns, G = 20, C_S = 2pF, CMOS AMS0.18 µm technology).

We will see later on, that thanks to this large bandwidth, the step response of the cascaded mirror feedback loop demonstrates a settling time equal to $(t_E\text{-}t_D)_{50\%}$ = 220 ps, that is close to the result expected and provided in **Table 2.2**.

2.8 Large-Signal Modelling – Settling time computation

In order to characterize the circuit dynamic performances, the settling time required to activate the feedback control loop when a turn-on event occurs has to be carefully studied. Indeed, the shorter the settling time of the feedback loop, the faster the switching that can be handled with our dv/dt control method. To determine the timing performances of the circuit, now a large-signal analysis has to be performed.

Observing the waveforms of the main signals of the circuit, it should be observed that the settling time, or total delay of the feedback loop, can be divided in 5 periods of time. The duration of the periods are defined by the times t_2, t_B, t_C, t_D and t_E in the **Figure 2.32** below. Notice that this study has been published in [69].

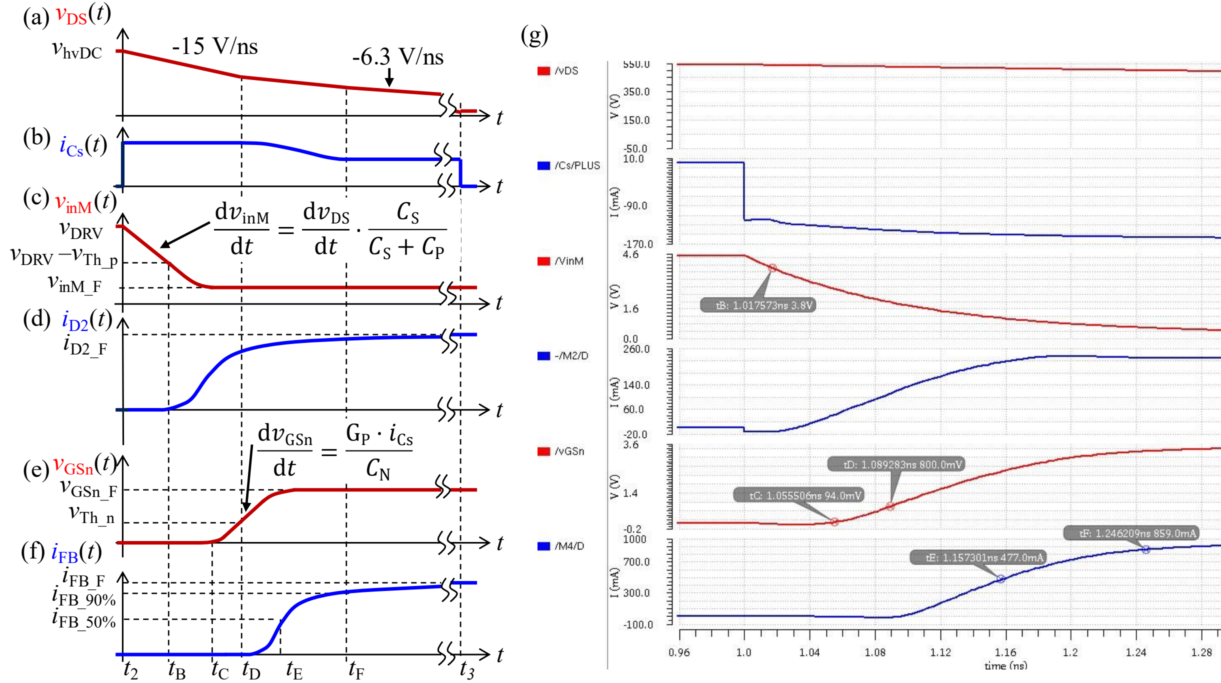


Figure 2.32. (a) to (f) Waveforms of the feedback loop voltages and currents during a turn-on dv/dt sequence. (g) CMOS AMS 0.18µm simulation results using CADENCE™ Virtuoso™.

This figure shows the voltage and current waveforms of the current mirrors between times t_2 and t_3 corresponding respectively to the start and the end of the turn-on dv/dt sequence. Capacitors C_P and C_N, mentioned in the equations present in the figure, are respectively the total amount of parasitic capacitors viewed at the gates of M1 and M3 as previously defined. The settling time, or feedback loop time delay, is shown and expressed as $t_{D50\%}=t_E-t_2$.

This time delay results from a succession of several events. During the turn-on of the power transistor and the dv/dt sequence, the voltage v_{DS} drops down from the voltage of the DC bus to a value close to zero. This transient is shown in **Figure 2.32**(a). This signal, $v_{DS}(t)$, is the input signal of the feedback loop. Because the terminal v_{inM} of the sensing capacitor C_S is at a quasi-constant voltage with respect to the voltage range of v_{DS}, the derivative of $v_{DS}(t)$ will generate a proportional quasi-constant current flowing through C_S, the $i_{Cs}(t)$ current, as shown in the second waveform **Figure 2.32**(b). This current will charge the parasitic capacitor C_{GP} present on node v_{inM}, involving the gates of the PMOS transistors M1 and M2, and change the biasing-voltage of the first current mirror, as shown in **Figure 2.32**(c). As soon as this voltage crosses the PMOS threshold voltage v_{Th_p}, a current will start to flow through the channel of M2, as shown in **Figure 2.32**(d). This current charges the gates of the transistors M3 and M4, leading to an increase in the voltage $v_{GSn}(t)$,

as shown in **Figure 2.32**(e). Finally, when v_{GSn} reaches the NMOS threshold voltage v_{th_n}, the output current i_{FB} of the second current mirror starts to rise, as shown in **Figure 2.32**(f). As soon as this current i_{FB} is no longer equal to zero, after time t_D, the feedback loop starts to operate and dv/dt starts to decrease and to be controlled.

In order to quantify the time delay of the feedback loop, it is observed that two time periods involve a slew rate mechanism. These two time periods are t_B-t_2, related to the biasing of the first current mirror, and t_D-t_C, related to the biasing of the second current mirror. The two slew rate mechanisms involved sequentially are named SR_1 and SR_2 and are developed hereafter.

2.8.1 Slew Rate 1

During the time period t_B-t_2, the voltage v_{inM} decreases with a constant rate. The parameter SR_1 is then defined using the following expression:

$$|SR_1| = \left.\frac{\mathrm{d}v_{\mathrm{inM}}}{\mathrm{d}t}\right|_{\max} \quad (2.48)$$

Because during this period of time the transistor M1 operates in its cut-off region ($v_{SG1}<v_{th_p}$), no drain current i_{D1} exists. The total amount of current sank by the sensing capacitor C_S is required to charge (or discharge) the total capacitor seen on the node v_{inM}, the gates of transistors M1 and M2. The circuit shown in **Figure 2.33** is an equivalent circuit of the input of the first current mirror during the time period t_B-t_2. Before the transistor M1 achieves threshold voltage (v_{THp}) all the current flowing through the sensing capacitor C_S is charging the capacitances (C_{MIR_P} + C_{S_PAR}). It can be assumed that this current is split in two parts, one to charge the capacitor C_{MIR_P} and the other part to discharge the parasitic capacitor C_{S_PAR}.

$$i_{C_S} = i_{C_{MIR_P}} + i_{C_{S_{PAR}}} \quad (2.49)$$

$$SR_1 = \left|\frac{\mathrm{d}v_{\mathrm{inM}}}{\mathrm{d}t}\right|_{(\max)} = \frac{i_{C_S}}{C_P + C_{S_{PAR}}} \quad (2.50)$$

The current i_{C_S} is proportional to the derivative of the voltage present across the nodes of the capacitor C_S.

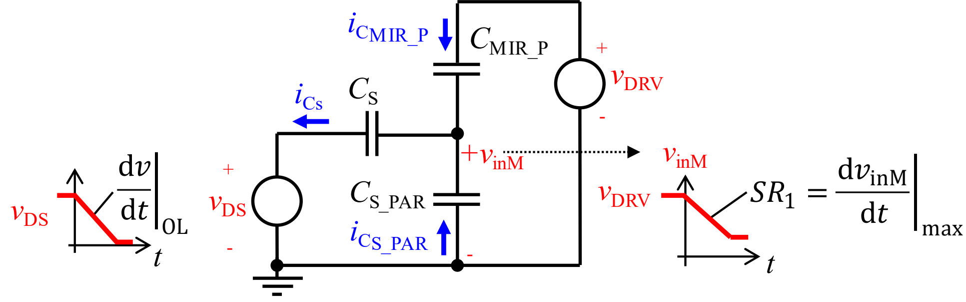


Figure 2.33. Equivalent circuit of the input of the first current mirror during the time period t_B-t_2. Before the transistor M1 achieves threshold voltage (v_{THp}) all the current passing by the sensing capacitor C_S is charging the capacitances ($C_{\text{MIR_P}} + C_{\text{S_PAR}}$).

The effect of a capacitive voltage divider is then observed at the input of the first current mirror. A second expression of SR_1 can be derived from this equivalent circuit.

$$SR_1 = \left|\frac{dv_{\text{inM}}}{dt}\right|_{(\max)} = \frac{C_S}{C_S + C_{\text{MIR_P}} + C_{S_{\text{PAR}}}} \cdot \left.\frac{dv}{dt}\right|_{\text{OL}} \tag{2.51}$$

where $dv/dt|_{\text{OL}}$ represent the drain-to-source voltage variation rate of the power transistor in open-loop operation (i_{FB}=0 A).

Considering first:

$$C_{\text{MIR_P}} = ((1 + G_{\text{P}}) \cdot k \cdot C_{\text{OXp}} \cdot L_{\text{eff}} + 2 \cdot G_{\text{P}} \cdot C_{\text{GDp}} + C_{\text{DSp}}) \cdot W_{1\text{MIN}} \tag{2.52}$$

with the minimum width $W_{1\text{MIN}}$ of PMOS transistor is C_S dependent:

$$W_{1\text{MIN}}(C_S) = \frac{L_{\text{eff}}}{\mu_{\text{Peff}} \cdot C_{\text{ox}_\text{p}} \cdot (v_{\text{GS}_{\text{CL}}} - v'_{\text{TH}})} \cdot \left.\frac{dv_{DS}}{dt}\right|_{CL} C_S = \frac{1}{J_{\text{P}} \cdot L_{\text{MIN}}} \cdot \left.\frac{dv_{\text{DS}}}{dt}\right|_{\text{CL}} \cdot C_S \tag{2.53}$$

and the expression of the parasitic capacitor $C_{S_{PAR}}$:

$$C_{S_{\text{PAR}}} = \frac{\gamma}{\gamma_{\text{P}}} \cdot C_S \tag{2.54}$$

where γ is the distance between the metal plates of the sensing capacitor C_S and γ_P is the distance between the LV (low voltage) plate and the substrate.
The equation (2.51) can also be rewritten as:

$$SR_1 = SR_{v_{\text{inM}}} = \left|\frac{dv_{\text{inM}}}{dt}\right|_{(\max)} = \left.\frac{dv}{dt}\right|_{\text{OL}} \frac{1}{1 + \frac{\gamma}{\gamma_{\text{P}}} + \frac{C'_{\text{MIR}_\text{P}}}{J_{\text{P}} L_{\text{eff}}} \left.\frac{dv}{dt}\right|_{\text{CL}}} \tag{2.55}$$

where $C'_{\mathrm{MIR_P}}$ is the total capacitance per width (F/µm) presented by the gates of the PMOS transistors.

Using (2.19), equation (2.55) can also be rewritten as:

$$SR_1 = \left.\frac{\mathrm{d}v}{\mathrm{d}t}\right|_{\mathrm{OL}} \frac{1}{\underbrace{1 + \frac{\gamma}{\gamma_{\mathrm{P}}} + (1 + G_{\mathrm{P}})}_{\text{Design choice}} + \underbrace{\frac{2kL_{\mathrm{eff}}^2}{\mu_{\mathrm{eff_P}} \cdot \left(v_{\mathrm{GS_{MAX}}} - v'_{\mathrm{TH}}\right)}}_{\text{Technology}} \cdot \underbrace{\frac{1}{A_{\mathrm{tt}}} \cdot \left.\frac{\mathrm{d}v}{\mathrm{d}t}\right|_{\mathrm{OL}}}_{\text{Appli.}}} \tag{2.56}$$

This last expression demonstrates the first slew rate SR_1 depends mainly on the design parameter G_{P}, the technology parameters and on the application inputs, i.e. the targeted closed-loop dv/dt for a given power transistor. The A_{tt} parameter is the desired attenuation of the open-loop dv/dt, it could be 50% for example, defined in equation (2.19).

Notice that the value of this first slew rate does not depend on the C_{S} value. Considering a constant product $G \cdot C_{\mathrm{S}}$, only the technology parameters and the choice of the gain G_{P} will affect the value of SR_1. In practice, a higher value for SR_1 is desired in order to reduce the activation time (or delay) of the feedback loop.

This last expression explains the first slew rate depends on the gain G_{P}, on the choice of the technology and on the numerical calculation. The numerical calculation is the desired attenuation in dv/dt, it could be 50% for example. Notice that this first value of slew rate does not depend on the C_{S} value for a constant product of $G \cdot C_{\mathrm{S}}$.

2.8.2 Slew Rate 2

The second slew rate for this large-signal analysis is called SR_2. It characterizes the maximum value of the derivative of the NMOS transistors gate voltage (v_{GSn}) versus time. It is defined as:

$$SR_2 = SR_{\mathrm{v_{GSn}}} = \left|\frac{\mathrm{d}v_{\mathrm{GSn}}}{\mathrm{d}t}\right|_{(\mathrm{max})} \tag{2.57}$$

Considering the typical equation of the capacitor $i_{\mathrm{C}} = C.\frac{\mathrm{d}vc}{\mathrm{d}t}$, the slew rate SR_2 is the total amount of current charging the intrinsic capacitance seen at the NMOS transistors (M3 and M4) gate node. This charging current depends on the sensing capacitor C_{S}, the dv/dt in open-loop (dv/d$t|_{\mathrm{OL}}$) and the gain of the PMOS current

mirror G_P. The total capacitance seen at the gates of the NMOS transistors is noted C_N.

$$SR_2 = SR_{\mathrm{v_{GS_N}}} = \frac{G_P C_S}{C_N} \cdot \left.\frac{\mathrm{d}v}{\mathrm{d}t}\right|_{\mathrm{OL}} \tag{2.58}$$

Considering equations (2.9) (2.19) (2.21) (2.23) (2.39), the capacitor C_N can be expressed as follows:

$$C_N = \frac{(1+G_N)\cdot G_P \cdot C_{GSn} + G_P \cdot G_N \cdot C_{GDn}(1-a_v) + G_P \cdot C_{DSn} + G_P \cdot C_{DSp})}{K_{linP}} \cdot \frac{L_{min}}{\left(v_{GS_{CL}} - v'_{TH}\right)} \cdot \left.\frac{\mathrm{d}v_{DS}}{\mathrm{d}t}\right|_{\mathrm{CL}} \cdot C_S \tag{2.59}$$

Now, neglecting the contributions of capacitors C_{GDN}, C_{DSN} and C_{DSP}, it follows:

$$C_N = (1+G_N)\cdot G_{P.} \frac{2\cdot k \cdot L_{min}^2}{\left(v_{GS_{CL}} - v'_{TH}\right)} \cdot \frac{1}{A_{tt}} \cdot \left.\frac{\mathrm{d}v_{DS}}{\mathrm{d}t}\right|_{\mathrm{OL}} \cdot C_S \tag{2.60}$$

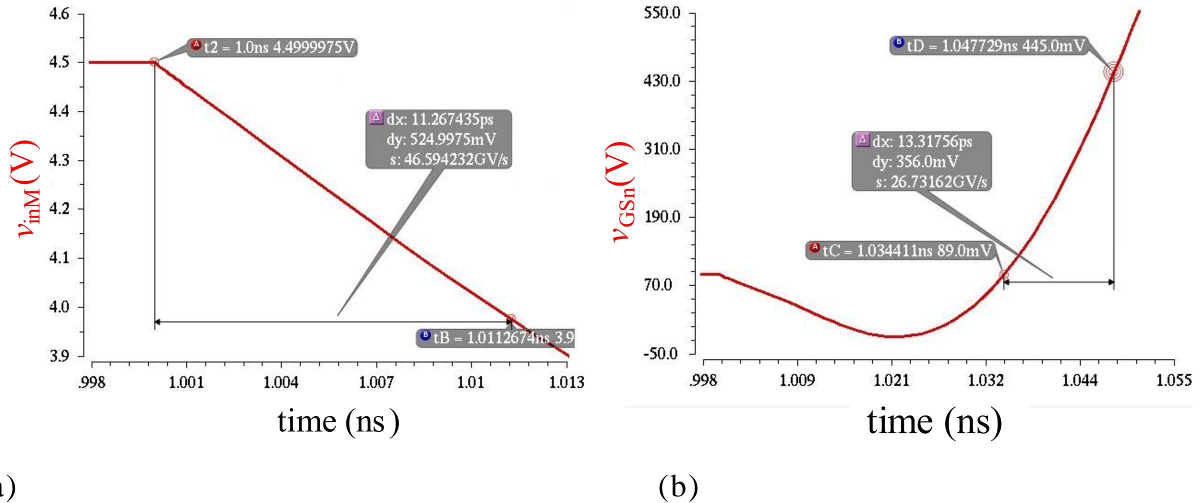
Then, SR_2 can be rewritten:

$$SR_{\mathrm{v_{GS_N}}} = \frac{1}{\underbrace{(1+G_N)}_{G_N} + \underbrace{\frac{2\cdot k \cdot L_{eff}^2}{\mu_{eff_N}\cdot\left(v_{GS_{MAX}} - v'_{TH}\right)}}_{\text{Techno. parameters}} \cdot \underbrace{\frac{1}{A_{tt}}}_{\text{Application}}} \tag{2.61}$$

In this expression it is possible to observe three different terms related to either the gain of the current mirror, the parameters of the technology or the dv/dt attenuation target. For a targeted attenuation, SR_2 is only dependent on the technology parameters and the value of G_N. It can be concluded that for a constant product $G{\cdot}C_S$ and a constant gain G_P determined for the 1st current mirror stage, this slew-rate will be dependent and proportional to the value of C_S.

It should be noted that, for both SR_1 and SR_2, many parameters depend on the choice of the CMOS technology. It can be expected that the higher the technology transition frequency (f_T), the faster the slew rates during the transient and the shorter the delay of the feedback control loop.

The two values of slew-rates SR_1 and SR_2 are extracted from CADENCE™ Virtuoso™ simulations. The extraction method of these values is shown below in **Figure 2.34**. These values (for slew rate) are calculated between the points t_2, t_B for SR_1 and t_C and t_D for SR_2 respectively. These points were defined in **Figure 2.32**.



(a) (b)

Figure 2.34. Zoom – extraction method of the SR_1 and SR_2 values from CADENCE™. (a) SR_1 extraction at the gate of the PMOS transistors (b) SR_2 extraction at the gate of the NMOS transistors.

Note that the simulated waveforms show a quasi-constant derivate for v_{GS} ranging from 0 V to the transistor threshold voltage v_{TH}.

Figure 2.35 shows the comparison of the values extracted from simulations performed with CADENCE™ Virtuoso™ and the theoretical ones calculated with accuracy with Octave™/Matlab (please refer to the Annex to the code in Annex 2: **MatlabTM/OctaveTM code for precise calculation of capacitances and bandwidth**). The equations used to calculate SR_1 and SR_2 are respectively (2.51) and (2.58). The theoretical values of C_P and C_N respectively are calculated with expressions (2.38) and (2.39) respectively. The technology considered is XFAB0.18 SOI.

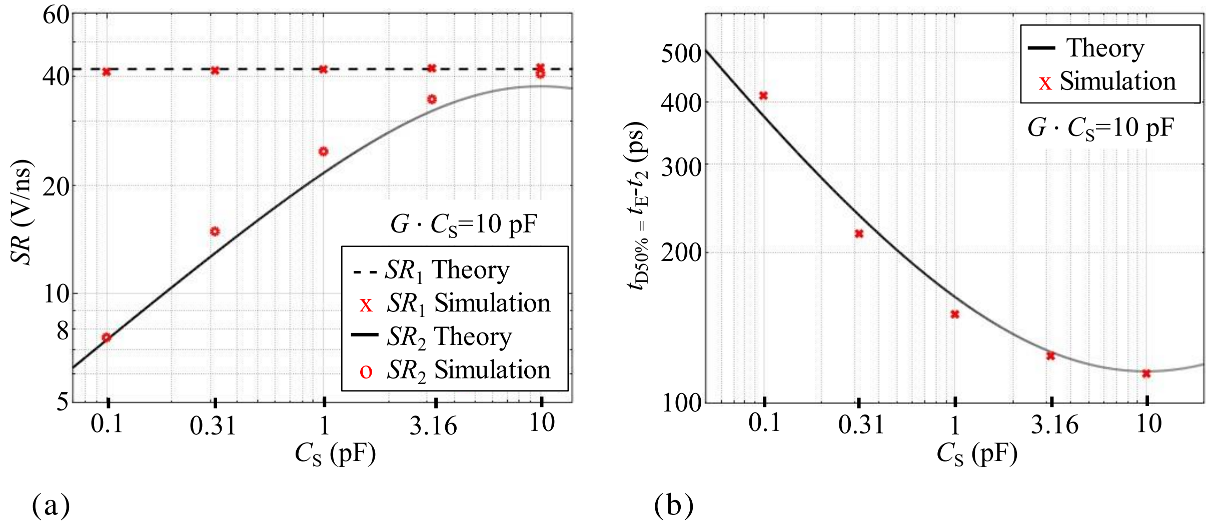


Figure 2.35. (a) Slew-rates SR_1 and SR_2 as a function of C_S for a constant $G{\cdot}C_S$; (b) the feedback loop delay, i.e. the settling time to reach 50% of the final value of the current i_{FB}, as a function of C_S capacitor.

It is interesting to notice that the value of total delay $t_{D50\%}$ is inversely proportional to the value of C_S while the slew rate SR_2 is directly proportional to C_S as predicted by (2.58). Note also the slew-rate SR_1 remains constant for any value of C_S as predicted by equation (2.51).

The value of settling time $t_{D50\%}$ is obviously linked to the circuit speed, i.e. the values of the slew-rates. It can be approximated by the expression below:

$$t_{D50\%} \approx \underbrace{a \cdot \frac{v_{TH_P}}{SR_{v_{inM}}}}_{t_C - t_2} + \underbrace{c \cdot \frac{v_{th_N}}{SR_{v_{GSn}}}}_{t_E - t_C} \tag{2.62}$$

where a and c are coefficients that can be adjusted to fit the results of future simulations and measurements. Notice that t_2, t_C and t_E are time parameters previously defined in **Figure 2.32**.

Now, if we consider the settling time (delay) $t_{D1\%}$ required to reach 1% of the final value of i_{FB}, a second approximation can be proposed:

$$t_{D1\%} \approx \underbrace{a \cdot \frac{v_{TH_P}}{SR_{v_{inM}}}}_{t_C - t_2} + \underbrace{b \cdot \frac{v_{th_N}}{SR_{v_{GSn}}}}_{t_D - t_C} \tag{2.63}$$

where b is a third dedicated parameter that can be also extracted and adjusted after simulations and measurements.

The coefficients of these two approximations after extraction from CADENCE™ simulations are a = 2.71, b = 1 and c = 3 with XFAB0.18 SOI technology and a = 4.5, b = 1 and c = 4.5 with AMS0.18 bulk technology. Using these values, theoretical settling times are calculated and their dependences on capacitor C_S are analyzed. **Figure 2.35** (b) and **Figure 2.36** show the comparison between theory and simulation for respectively the cases of $t_{D50\%}$ and $t_{D1\%}$ with AMS0.18 technology for the last one.

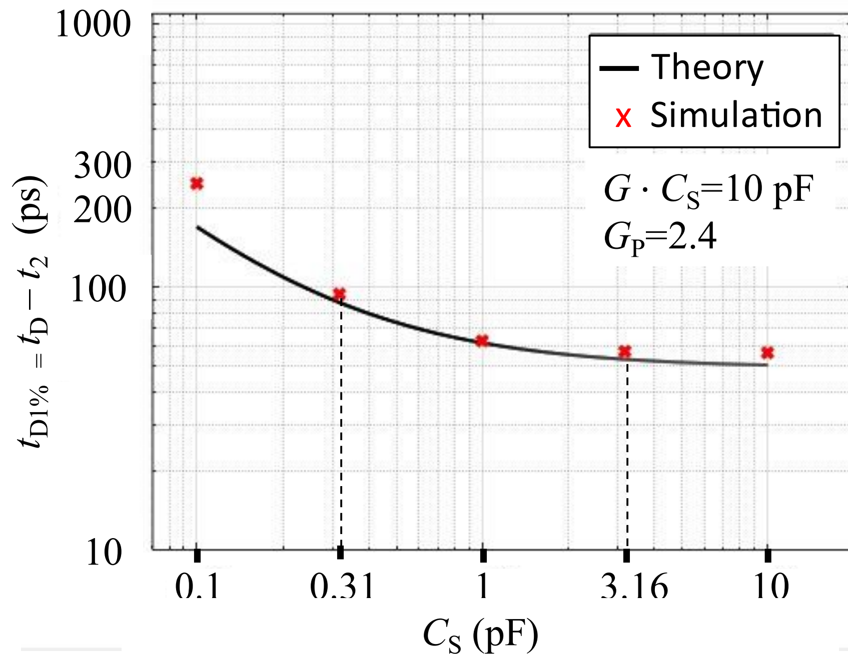


Figure 2.36. Delay $t_{D1\%}$ as a function of capacitor C_S with a constant product $G{\cdot}C_S$.

These values of $t_{D50\%}$ and $t_{D1\%}$ can be considerably reduced using a pre-biasing current technique which will be explained in the next section.

Both for $t_{D50\%}$ and $t_{D1\%}$ the tendency is similar. Increasing the value of C_S will reduce the delay of the feedback loop. Furthermore, also with constant extracted values for parameters a, b and c, the settling times estimations can accurately predict their dependency on capacitor C_S.

Observing **Figure 2.30** and **Figure 2.35** (b) it can be concluded that "the higher the values of C_S, the larger the bandwidth and the shorter the total delay $t_{D50\%}$".

Therefore, a quasi-constant value is observed for the product of the bandwidth f_C and the delay $t_{D50\%}$. Figure below shows the behavior of this product for a large range of C_S values:

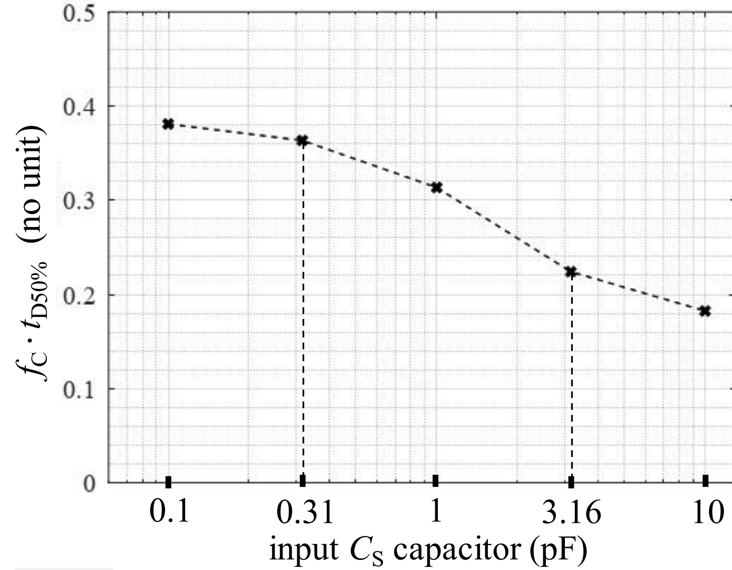


Figure 2.37. Product of the bandwidth f_C and the delay $t_{D50\%}$ as a function of capacitor C_S with $G \cdot C_S$=10 pF.

It is observed the product $f_C \cdot t_{D50\%}$ varies from 0.38 to 0.18 with C_S ranging from 100 fF to 10 pF (2 decades). It indeed represents a variation of 57% around the level 0.35 which is a well-known value for a 1st order low-pass filter ($f_C \cdot t_R$=0.35).

It can be concluded the dynamic performance of the feedback loop depends on the transition frequency of a technology (f_T). To obtain the lowest possible delay, i.e. the best performance for a feedback loop, a technology with the highest transition frequency should be chosen. Depending on the application, this technology should also offer the possibility to isolate either 5 V for GaN transistor or more than 25 V for SiC transistor. More details about the choice of the technology are discussed in next subchapter and in Chapter 3.

2.9 Comparison of technologies AMS0.18 (used for GaN applications) and XFAB0.18 SOI (used for SiC applications)

With the previous theoretical studies, two CMOS technologies have been studied. Most of the calculations have been performed using XFAB0.18 SOI technology parameters. The technology XFAB is studied for SiC devices but the values of Miller plateau are the same for GaN because the analysis and comparison of theory and simulation are already complicate to validate. For the same reason the transistor M4 is a 5V transistor even for the SiC AGD when in the design it is used a 40V transistor. Some calculations related to C_S dependencies have been also

performed with AMS0.18 bulk technology. To compare both technology, comparative simulations are made. The two schematics of the feedback loop system implemented in CADENCE™ are shown in **Figure 2.38** below. In order to perform simulations with constant product $G.C_S$, the width of the transistors is considered as a simulation variable. Then, the values of C_S, which is an input data, and the transistor widths are automatically modified to keep the product $G{\cdot}C_S$ constant.

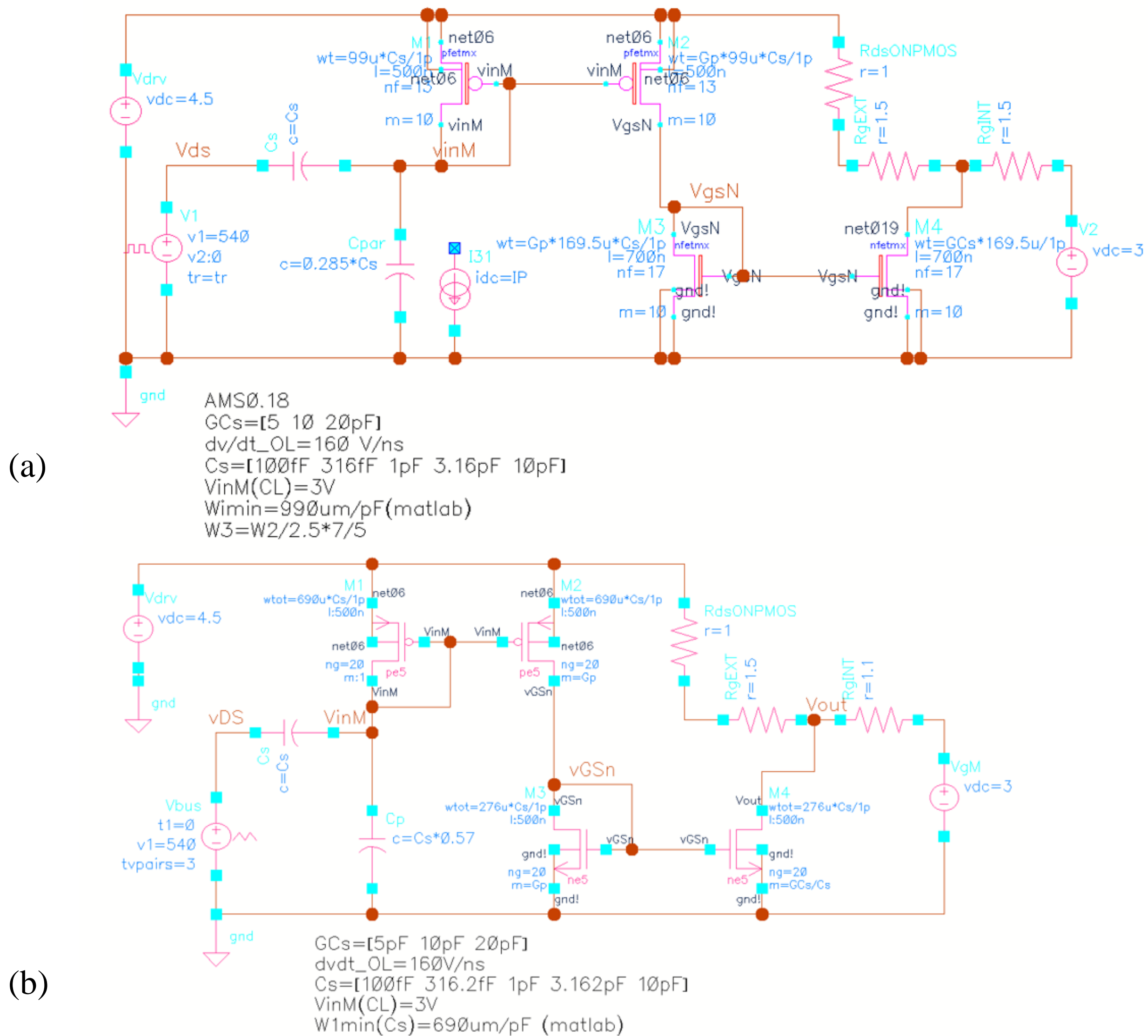


Figure 2.38. Schematic in CADENCE™ for the simulated values in the technologies (a) AMS0.18 and (b) XFAB0.18SOI. The size of the transistors are parametrized as a function of C_S for a constant product $G.C_S$.

We first compare the sizing of transistors according to the drain current amplitude, i.e. depending on the value of the capacitor C_S. **Figure 2.39** shows the

drain current of transistor M1 per width unit as a function of the width for two technologies both for the PMOS and the NMOS transistors. These results are obtained using a simple diode-connected circuit ensuring the operation of the transistor in its saturation region (**Figure 2.11**).

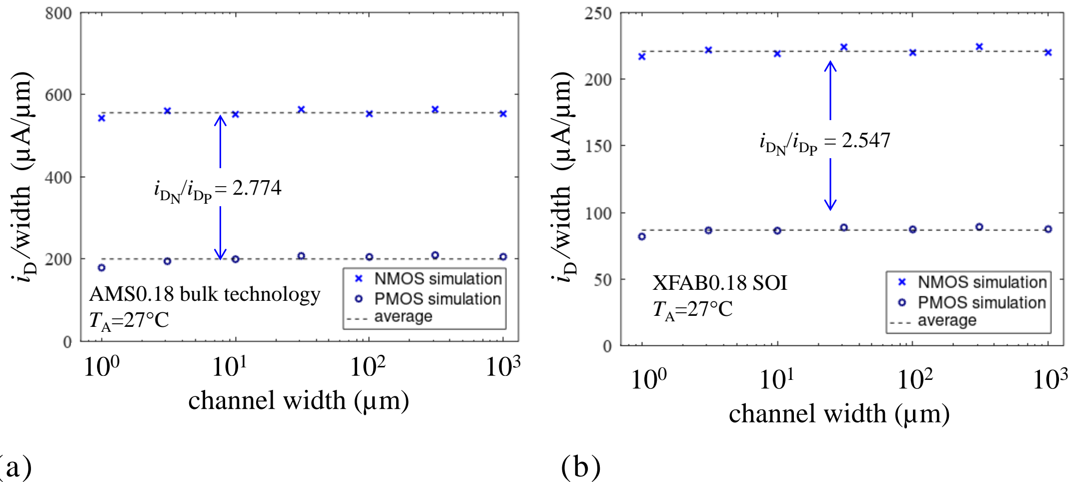


Figure 2.39. Comparison between the current per width unit as a function of the width for technologies (a) AMS0.18 and (b) XFAB0.18SOI. For the same W/L ratio the bulk technology has 2.77 times higher current, but their capacitance value is also increased.

It is first observed that, for the same W/L ratio, AMS0.18 bulk technology has 2.77 times higher current than XFAB0.18SOI.

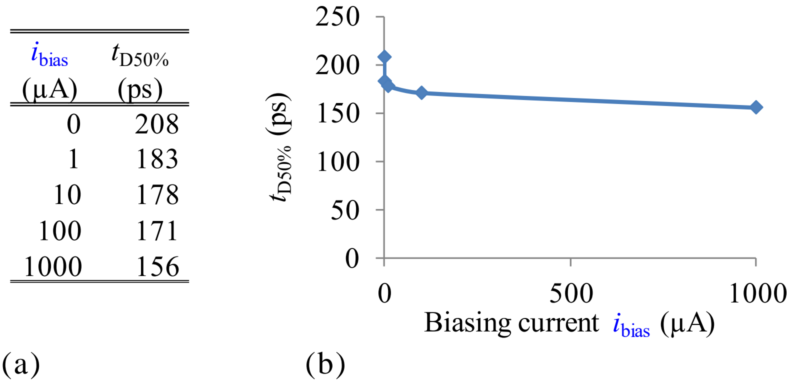
Then, the second major difference, not shown in the figure, are the values of the overlap capacitance per width (C_{OV}), the body diode junction capacitance (C_{jsw}) and (C_j). They are different between the two technologies in the same ratio. The exact values are extracted from documents under NDA (non-disclosure agreement) and used in the calculation. Therefore, the values cannot be published in this manuscript but the overlapping capacitance from the bulk technology is around 5 times higher than the similar SOI technology.

Then, the capacitance difference seems to compensate the difference of the current levels that results in a transition frequency similar for both technologies (f_t=18.2 GHz and 18.9 GHz for AMS and XFAB respectively).

More details about the choice of the technology are given in chapter 3.

2.10 Biasing current generator

The current mirrors can work properly without any biasing current applied at the input of the feedback loop circuit. Nevertheless, pre-biasing transistors M1 to M4 by sinking a small current at node v_{inM} can significantly reduce the delay $t_{D50\%}$ previously defined between the times intervals (t_D-t$_2$) and therefore improve the system performance.



i_{bias} (µA)	$t_{D50\%}$ (ps)
0	208
1	183
10	178
100	171
1000	156

Figure 2.40. (a) Table and (b) plot of the CADENCE™ simulation of settling time $t_{D50\%}$ (settling time to 50% of i_{FB_F}) as a function of the biasing current i_{bias}. Few µA is enough to significantly reduce the total delay.

Notice that the delay depends on the biasing current and also on the total gain G. Table 2.2 shows the results obtained with CADENCE™-Spectre™ transient simulations to determine the value of the delay defined in **Figure 2.1** for different biasing currents i_{bias}. Different total gain values (5, 10, 20 and 50) for the current mirrors are simulated and implemented within the prototype. One has to note that all transistors M1-M4 are designed differently for each case of total gain G value. If different gain modifies the dv/dt in closed-loop and consequently the input current i_{Cs}, it also implies different parasitic capacitance values what impacts the overall response time. In these simulations, for comparison purpose, a constant dv/dt equal to 15 V/ns with a sense capacitor of 2 pF is considered. The design must be done carefully, splitting the total gain G into two different gains G_P and G_N to minimize the parasitic capacitors of the transistors, leading to an optimized size reducing the time-constant values of the feedback loop.

TABLE 2.2. SIMULATED RESPONSE TIME FOR DIFFERENT VALUES OF BIASING CURRENT WITH THREE DIFFERENT GAINS

	G10 pre-biased		**G20 pre-biased**		**G50 pre-biased**	
bias current	Time delay ($t_{D1\%}$)	1-50% settling time	Time delay ($t_{D1\%}$)	1-50% settling time	Time delay ($t_{D1\%}$)	1-50% settling time
i_{bias}	t_D - t_2	t_E - t_D	t_D - t_2	t_E - t_D	t_D - t_2	t_E - t_D
0	218ps	214ps	244ps	279ps	351ps	503ps
20μA	80ps	256ps	83ps	337ps	102ps	608ps
2mA	27ps	251ps	28ps*	330ps*	31ps	589ps

* shown in **Figure 2.41**. Published in [114] by the same author of this manuscript.

In **Figure 2.41** the time intervals t_D–t_2 and t_E–t_D are determined by simulation of the time response with the current mirror G = 20 pre-biased with a 2 mA i_{bias} current. The input current (i_{Cs}) is set to 26 mA that corresponds to a dv/dt equal to either 26 V/ns with C_S = 1 pF or 13 V/ns with C_S = 2 pF.

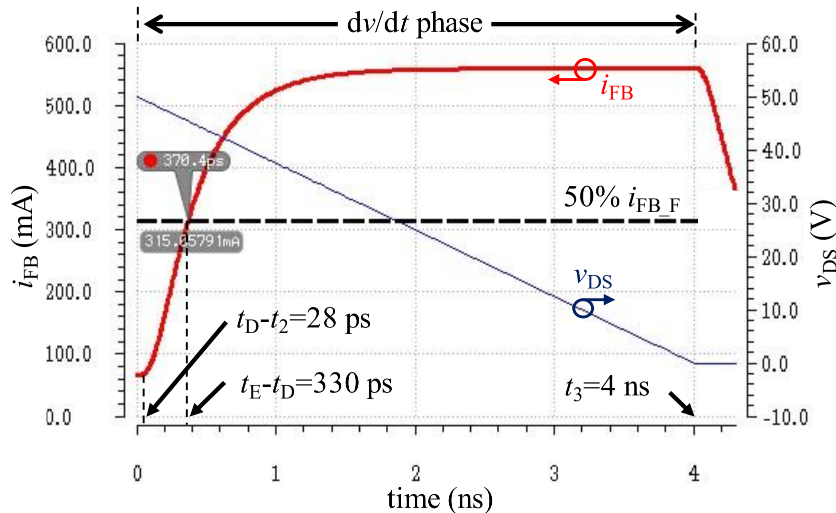


Figure 2.41. Simulation of the transient response time with G = 20 (v_{DRV}=4 V, i_{bias}=2 mA, i_{Cs}=30 mA).

After tens of picoseconds the feedback loop provides a current at the output (i_{FB}) and therefore is already acting and affecting the dv/dt.

The delay decreases as the bias current i_{bias} increases. This improvement is at the expense of an additional power consumption. Indeed, using a pre-bias current, extra losses in transistors M1 to M4 are generated, which can reach high levels due to the high value of gain G_P. It should be noted that this biasing current can be provided only during the switching. Then, a trade-off between extra losses due to

additional current consumption in the AGD during turn-on and bandwidth improvement has to be considered. Please refer to the next section for more details.

If the biasing current is higher than few milliamps not only the power consumption is increased to tens of milliamps (example G50, i_{FB}=50 mA with i_{bias}=1 mA) but it can also affect the dv/dt_OL. Indeed, a pre-biased constant current i_{FB} is sunk from the gate node and subtracted from the current i_{RG} provided by the output stage of the GD (transistors M5). The level of this current must be kept low, i.e. lower than $i_{RG}/10$ to minimize its impact on the system. To summarize, a good tradeoff between performance and consumption is achieved choosing low values for i_{bias}.

Because biasing a circuit in current requires more surface and power consumption comparing to voltage biasing [102], a simple circuit to generate i_{bias} has been chosen. This biasing circuit is shown in **Figure 2.42**.

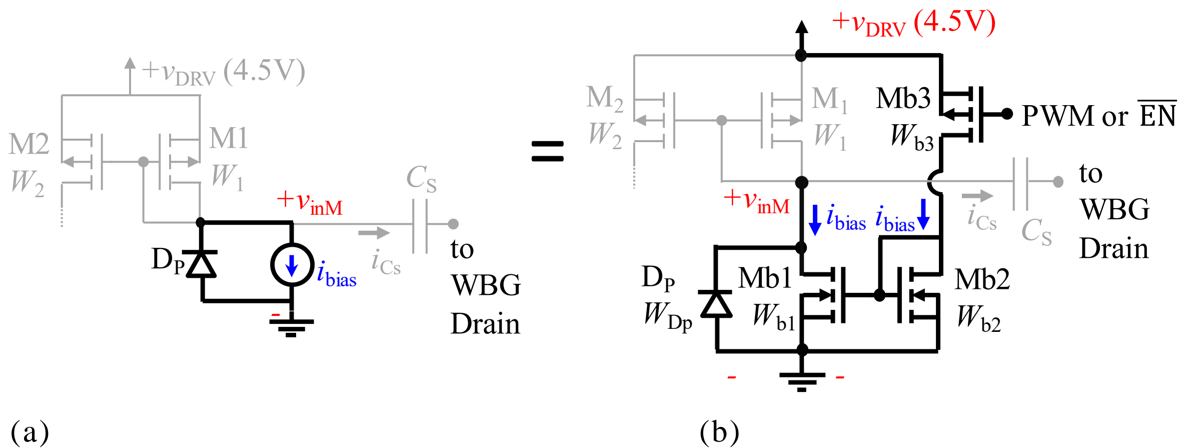


Figure 2.42. (a) Location of the biasing current generator. (b) Biasing circuit made of 3 transistors Mb1 to Mb3.

To activate the biasing circuit, the gate of Mb3 has to be set to 0V. Then a current i_{bias} proportional to the width W_{b3} of Mb3 is mirrored by the Mb1-Mb2 current mirror stage and sunk from the input node v_{inM}. If necessary, the value of this current i_{bias} can be lowered and controlled by the voltage applied to the gate of Mb3. It should be noted that the transistor sizes are set to minimum values because just few µA are necessary to significantly reduce the feedback loop delay.

The maximum possible current for the biasing generator in the SiC-application chip is around 95 µA (when the gate of Mb3 is set 0V). The values of the widths W_{b1}, W_{b2} and W_{b3} are identical and equal to 0.5 µm. For the GaN-application, the widths are respectively 0.7 µm, 0.7 µm and 1 µm. With this 95 µA biasing current, the resulting settling time is reduced by 18%. More details of the implementation and layout of the biasing circuit can be found in the chapter 3.

2.11 Impact of the proposed method and sensitivity to dispersions

2.11.1 Impact on the total gate charge

The emulated gate-to-drain capacitor (C_{rss}+G·C_S) leads to an extended Miller plateau. Since charges are subtracted during a turn-on event through transistor M4, the amount of charge required to turn-on the power device increases. This has a strong impact on the total amount of charge provided by the AGD to the gate node of the power device. Indeed, with the proposed improved AGD, the amount of charge subtracted by the feedback loop has to be provided by the driver power supply v_{DRV}.

For each switching period, the total amount of energy provided by the driver power supply is:

$$E_{\mathrm{DRV}_{SUP}} = v_{\mathrm{DRV}} \cdot Q_{\mathrm{RG}} = v_{\mathrm{DRV}} \cdot (C_{\mathrm{rss}} + G \cdot C_{\mathrm{S}}) \cdot v_{\mathrm{hvDC}} \quad (2.64)$$

where v_{hvDC} is the bus voltage of the application.

Then, the additional amount of energy $E_{\mathrm{DRV}_{SUP}}$ provided by the power-supply v_{DRV} is given by:

$$E_{\mathrm{DRV}_{\mathrm{SUP}}} = v_{\mathrm{DRV}} \cdot G \cdot C_{\mathrm{S}} \cdot v_{\mathrm{hvDC}} \quad (2.65)$$

Eq. (2.65) shows that the extra energy supplied by the driver will increase proportionally with the gain G of the internal current feedback circuit [69]. A decrease of 58% (from -15 V/ns to -6.3 V/ns) in dv_{DS}/dt will produce an increase of 58% in the energy provided by the driver E_{DRV_SUP}. Since the switching energy of the power device is considerably higher than the energy required by the driver, this increase in driver energy has a limited impact. For the 400 V application for instance, the total losses are increased by 28% from point A to point C (**Figure 1.31**). This leads to an increase of 80 nJ in the driver part compare to 12 µJ in the power device. One can note that this additional GD energy is inherent to the proposed closed-loop control, and other previously demonstrated approaches are also subject to such an energy increase [121] [63].

2.11.2 Dispersion effects caused by DC bus voltage

Due to its closed-loop nature, the attenuation factor provided by the feedback control loop is independent of external parameters, other than the C_{rss} capacitor of the power device (see equation (2.19)). Simulation of the effects of DC bus voltage variations on dv/dt attenuation shows that the closed-loop system is not affected.

In order to validate this assumption, simulations in LTSpice™ are performed and results both for dv/dt in open-loop (without the proposed method) and in closed-loop (with the proposed method) are compared. It is observed that the attenuation does not significantly change for a wide range of values of v_{busDC} voltage. **Figure 2.43**.

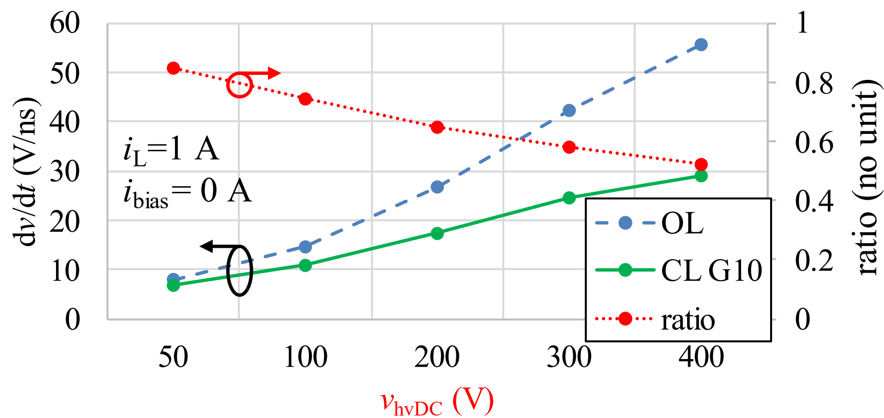


Figure 2.43. dv/dt as a function of the DC bus voltage. Notice that the closed-loop system is able to maintain a quasi-constant dv/dt attenuation for a wide range of values of v_{busDC}.

2.11.3 Dispersion effects caused by temperature

Regarding thermal effects, performances can be susceptible to changes in temperature. Both carrier mobility and threshold values decrease when the temperature increases in the CMOS transistors [118]. Notice that the current mirrors placed in an integrated circuit with the main stage driver and close to the power device might be susceptible to the same increase in temperature as those devices. Using correctly matched transistors for M1 to M4, the gain G may be very slightly impacted over the full range of temperature values. However, the integrated capacitor C_S is more susceptible to change in a large proportion. An increase in temperature might affect the product $G{\cdot}C_S$ of the feedback loop but it will affect also the main

stage buffer capability and therefore the combined effects should balance one another. This study was not carried out during the thesis.

2.12 Chapter Conclusion

In this chapter, a theoretical analysis is conducted to determine the best trade-off between the sensing capacitor C_S value and the gain G of the two current mirror stages.

After an introduction dedicated to methods used to integrate the sensing capacitor into the chip using metal layers, the sizing of the transistors involved in the feedback loop is explained in detail.

A first study on the silicon surface occupied by the circuit is performed. Depending on the chosen parameters C_S and G, it is demonstrated that the die size of the circuit varies in a large range of values proportionally to C_S.

A second study focusing on the bandwidth of the feedback loop is developed. It is shown that the circuit bandwidth is directly linked with the transition frequency of the technology which is a good indicator of the maximum frequency performances that can be reached. Once again, the dependency of the circuit performance with parameters C_S and G is demonstrated.

At last, a third study dedicated to the settling time of the feedback loop is provided. Slew-rates and time delays versus C_S are analyzed in detail. A strong correlation between settling time, bandwidth and transition frequency is highlighted.

It is important to mention that for the three studies, the theoretical results computed with mathematical software (Matlab™/Octave™) are systematically compared with CADENCE™ simulations both for AMS0.18 and XFAB.18 SOI technologies. Very good correlations are observed in all cases and confirm the validity of the theoretical approach.

As a main conclusion for this chapter, it is observed that increasing the value of C_S increases the bandwidth, reduces the settling time, but consumes more silicon surface if the sensing capacitor is integrated. Therefore, a more expensive solution can demonstrate a higher dynamic performance and be able to control dv/dt's in the order of hundreds of volts per nanosecond (1.6 GHz bandwidth, 220 ps rise time with $C_S = 1$pF and $G = 10$ in CMOS 0.18 µm technology).

Chapter 3 will demonstrate these predictions match with experimental results.

3 Design of Active Gate Drivers for GaN HEMTs and SiC MOSFETs

In this chapter, the design, the characterization, and implementations of the proposed method to control dv/dt are detailed. The proposed method was presented in the previous chapters and this chapter will focus the design specifications, simulations, measurements and performance comparisons. The required hardware for the tests and PCB specifications will also be detailed.

3.1 Introduction – Differences Between GaN and SiC

From all different technology of power devices possible for medium voltage applications [122], this work focus in the normally-off GaN and SiC devices. The first difference between GaN and SiC transistors from a GD design perspective is the gate-to-source voltage to be applied and the total gate charge. For normally-off GaN transistors, 0 to 5 V is possible [123, 124, 125, 126, 127], and it is technology dependent. For SiC MOSFETs the negative gate-to-source to turn-off the component can be as low as -5V, and the positive v_{GS}, depending on the technology is around 20 V. [128, 129, 130, 131, 132, 133].

Other differences between GaN and SiC for GDs are charge trapping effects and leakage current. Normally-off GaN devices have a relatively high DC gate current during on-state (in the µA/mm range) compared to SiC or Si power MOSFETs (usually in the nA/mm range) [134].

More comparative analysis of GaN and SiC for GD design perspective can be found in [135] [136] [137] [138] [139] [140]. **Table 3.1** compares the main parameters for GD design of 2 GaN devices and 2 SiC devices. The gate voltage during the Miller's plateau v_{M} is calculated using the expression (3.1).

$$v_{\mathrm{M}} = v_{\mathrm{TH}} + \frac{i_{\mathrm{D}}}{g_{\mathrm{fs}}} \tag{3.1}$$

TABLE 3.1: COMPARISON OF MAIN PARAMETERS FOR GATE DRIVER DESIGN FOR GAN AND SIC

Parameter	GaN EPC2001C	GaN GS66508P	SiC C3M0075120K	SiC C3M0016120K
	Tests at 50 V	Tests at 400 V	1st option	2nd option
Breakdown v_{DS} (V)	100	650	1200	1200
Rated i_D (A)	25	30	30	115
R_{DS_ON} (mΩ)	7	50	75	16
v_{GS} (V)	-5/6	-10/7	-4/15	-4/15
v_{TH} (V)	1.5	1.3	2.5	2.5
R_{G_INT} (Ω)	0.6	1.5	10.5	2.6
g_{fs}^{*}(S)	80	9	83	47
i_{gMAX}(A)	18	11	1.8	7.3
i_{Miller}^{**} (A)	4.5	0.25	0.85	3.88
v_M @ i_{D_NOM} (V)	1.8	4.6	6	4.9

* g_{fs} values considered at T_J=150°C **calculated for R_{G_EXT}=0Ω, neglecting R_{rsON} of M5 transistor and i_L=1 A.

3.2 Specifications of Active Gate Drivers for GaN and SiC

As introduced in the previous section, the CMOS technology and specifications for SiC and GaN GDs are different. GaN transistors can use negative voltage or an architecture using only 5 V CMOS transistors. In this last choice, a larger safety margin for the power device is achieved. However, using a lower voltage amplitude in the output, a lower switching speed is obtained. To compensate and increase the switching speed, lower values of external gate resistors (R_{G_EXT}) can be used for lower switching energy consumption.

Regarding SiC transistors either a cascading topology is required to generate the higher voltage amplitude in the GD output (-5 V to 20 V) or higher voltage CMOS transistors should be used. From the possible topologies of GD, the choice has been made to use 40 V CMOS transistors in the output of the GD. Those transistors can withstand 40 V between drain and source but only 5 V between gate and source. A level shifter is used to control the PMOS M5 transistor with the same PWM signal from 0 to 5 V to control the NMOS M6 transistor. More details of these specifications, the schematics and all the calculations, are presented in **section 3.4**.

As already discussed in chapter 2, parameters that will be sized in this project are the following: capacitance value of the sensing capacitor C_S, the width of the four transistors in the current mirrors W_1 to W_4, and the width of the main stage buffer W_5 and W_6.

3.2.1 100V and 650V GaN HEMTs choice

Before this work, a CMOS AGD for GaN has been developed in Laplace laboratory. To reduce the development time and cost, a first design of an AGD was based only on 5 V CMOS devices. It was further integrated with other analog and digital functions in a 0.18 µm CMOS platform. Hence, this first proof of concept is most suited to drive EPC GaN devices (breakdown voltages from 15 V to 200 V, with typical gate driving voltages between 0 V and 5 V [124, 141]), due to their low total gate charge, small gate current and low driving voltages. This CMOS design uses the previously developed 5 V output buffer by D. Colin [142], which exhibits a +/-3 A current capability and 5 V/ns output buffer slew rate. This current capability was chosen as a good tradeoff between CMOS area and power converter applications in the context of low power and high-speed power switching.

To be able to modify the gate current during experiments without soldering, the output buffer is segmented in 2 branches, with 2 enabling bits and integrated logic [143], which allows switching between 4 gate current values for both gate sourcing and sinking (0A high impedance, +/-1 A, +/-2 A, +/-3 A). This option offers the possibility to change the gate current during experiments, and therefore the dv_{DS}/dt (also called in this manuscript $dv/dt_{_OL}$) which is an important parameter for the dv/dt control loop.

Based on these specifications and previous developments in 48 V applications, the 100 V-7 mΩ EPC2001C has been chosen as a preferred candidate to implement the active gate driving technique for the first proof of concept. With a 5 V output buffer in the CMOS GD, it is also possible to address 400 V applications, given the 650 V GaN devices fabricated by GaN Systems [125, 144, 145]. However, these devices are typically driven between negative v_{GS} (e.g. -2 V, -5 V or up to -10 V) to increase their cross-talk immunity (also called self-turn-on failure), and 6 V to reduce the ON-state resistance. Consequently, the ideal output buffer to drive such devices should have a breakdown voltage of at least 20 V. It is still possible to drive such GaN devices with the previous 5 V buffer, albeit requiring a smaller external gate resistor to achieve high switching speeds. The main drawback of using the previously developed 5 V output buffer with 650 V GaN systems devices will be to have increased GaN conduction losses, which is not a problem to demonstrate the active gate driving concept. Nonetheless, high power switching speeds are offered with a 5 V output buffer driving 650 V.

Based on previous applications and developments, the active gate driving will be applied to GS66508T from GaN Systems (650 V 50 mΩ). This reference is a good

candidate to be driven by the 5 V output buffer, to exhibit high dv_{DS}/dt values and to be implemented in key 400 V applications.

These GaN devices (EPC2001C and GS66508T) were chosen as good candidates to have extremely low switching times, in the order of a few nanoseconds, to challenge the CMOS AGD in both 48 V and 400 V applications. Indeed, with these devices, the feedback loop must have a response time below 1 nanosecond to be able to effectively control the switching transient. The response time of the feedback loop should be inferior to one tenth of the switching rising or falling time [64].

3.2.2 1200V SiC MOSFET Transistor Choice

The first thing to adapt a AGD project to another technology is the choice of the target device to be controlled. A closed-loop system could be adapted to a wide range of SiC devices available in the market, however three devices are selected to simulate the behavior of the proposed system.

The focus of this thesis is the dv/dt control for WBG transistors. Therefore, the main stage buffer is adapted from a previously developed block in the lab, [146]. This previously developed buffer was studied to be compatible with a wide range of SiC transistor choices, including those shown in **Table 3.2** which are transistors for different rated current from the 2nd and 3rd generation of WofspeedCree™. The main stage buffer is compatible with any of the transistors in the table, albeit limited to a maximum peak gate current of 4 A.

For the feedback loop design, the value of dv/dt (as a function of R_{G_EXT}, v_{bus_DC} and i_L) has to be estimated. Therefore at least one power device should be chosen to simulate the effect of the feedback loop. The table shows a comparative study of different SiC power devices from WofspeedCree™ with the important parameters for the main stage buffer design and the consequent dv/dt feedback loop design.

TABLE 3.2: SIC COMPARISON FOR TRANSISTOR CHOICE

Transistor	**C3M0120090J**	**C3M0075120K**	**C3M003120K**	**C3M0016120K**	**C2M0025120D**	**C2M0040120D**
Parameter		1st option		2nd option		
v_{DS} (V)	900	1200	1200	1200	1200	1200
i_D (A)	22	30	63	115	90	63
R_{DS_ON} (mΩ)	120	75	32	16	25	40
v_{GS} (V)	-4/15	-4/15	-4/15	-4/15	-5/20	-5/20
v_{TH} (V)	2.1	2.5	2.5	2.5	2.6	2.6
R_{G_INT} (Ω)	16	10.5	1.7	2.6	1.1	1.8
R_{G_EXT} (Ω)	2.5 to 20	0 to 20	2.5 to 20	0 to 20	2.5 to 20	2.5 to 20
Q_G (nC)	17.3	51	118	211	161	115
C_{iss} (pF)	350	1350	3357	6085	2788	1893
C_{rss} (pF)	3	3	8	13	15	10
i_{gMAX} (A)	3.2	1.15	3.57	5.77	5.5	4.5

In a similar way as for GaN HEMTs, the feedback loop is made to be compatible with more than one power device, and to be associated with fast power devices. At first, a 3rd generation low power device is chosen: C3M0075120K, which has low intrinsic capacitance (C_{iss}, C_{rss}) and therefore high switching speed. Another power device with higher power capability is chosen as a second option: C3M0016120K. With these two options, a wide range of load currents can be demonstrated with the active tuning of dv/dt in different applications. Both transistors will be simulated in section 3.4.4.

A second variable to design (after considering the v_{DS_MAX} of the transistors in the output of the buffer) is the peak current the main buffer can provide to the power device. For the first option, the power device C3M0075120K, the peak current required will be limited by the R_{G_INT} which is 10.5 Ω. Since the recommended V_{GS} is -5 to 15 V therefore the peak gate current will never be higher than 20 V/10.5 Ω =1.9 A. Neglecting the effect of R_{DS_ON} of M5 compared to R_{G_INT} and R_{G_EXT} the following analysis can be simplified. If the main stage buffer (transistor M5) has a capability of supplying more than 1.9 A, there will be no change in the di/dt or the turn-on or off delay times ($t_{d(on)}$ and $t_{d(off)}$). In other words, neglecting the R_{DS_ON} of M5, a driver capable to providing 2 A or 10 A will have the same effect on the dv/dt, di/dt and turn-on delay time for the transistor C3M0075120K. In practice the R_{DS_ON} is not negligible compared to the value of the R_{G_INT} and R_{G_EXT} and a GD capable to provide high current will cause a higher dv/dt in the power device.

The 2nd option device (C3M0016120K) has a lower R_{G_INT} and therefore a higher i_{gMAX} value as presented in **Table 3.3** below.

TABLE 3.3: PARAMETERS RELATED TO D*V*/D*T* FOR SIC TRANSISTOR CHOICE

Parameter	C3M0075120K	C3M0016120K
	1st option	2st option
v_{TH}	2.5V	2.5V
R_{G_INT}	10.5Ω	2.6Ω
R_{G_EXT}	0 to 20Ω	0 to 20Ω
Q_G	51nC	211nC
C_{iss}	1350pF	6085pF
C_{rss}	3pF	13pF
i_{gMAX}	1.9A	7.7A
d*v*/d*t*_ON datasheet (10-90%)	50V/ns @20A	30V/ns @75A
d*v*/d*t*_ON datasheet (peak = 2×(10-90%))	100V/ns @20A	60V/ns @75A

3.2.3 Expected Reduction in E_{ON}

The expected reduction in *Eon* values due to the AGD and feedback loop are presented in **Table 3.4** below. On the left half of the table, simulation values are presented for the GaN EPC2001C device and on the right part, for the device GS66508.

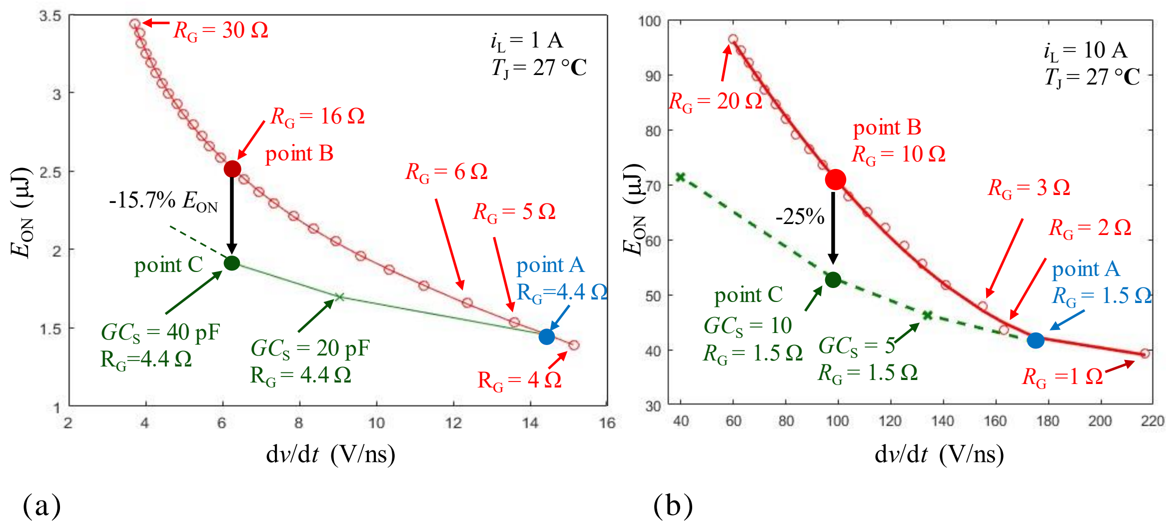
TABLE 3.4: SIMULATED EON IN OPEN AND CLOSED-LOOP FOR TWO DIFFERENT GAN VOLTAGE-RANGE APPLICATIONS

	GaN EPC2001C simulations at 48V *G·Cs*=20 pF			**GaN GS66508 simulations at 400V *G·Cs*=20 pF**		
			i_L=1 A			
Point*	**R_{G_EXT} (Ω)**	**E_{ON} (μJ)**	**|d*v*/d*t*| (V/ns)**	**R_{G_EXT} (Ω)**	**E_{ON} (μJ)**	**|d*v*/d*t*| (V/ns)**
A	4.4	1.42	15	1.5	18.18	175
B	22	1.845(+30%)	4.715 (-68%)	10	19.62(+7.9%)	97 (-44%)
C	4.4	1.62(+16.1%)	4.67 (-68%)	1.5	18.81(+3.4%)	97 (-44%)
			i_L=20 A			
Point*	**R_{G_EXT} (Ω)**	**E_{ON} (μJ)**	**|d*v*/d*t*| (V/ns)**	**R_{G_EXT} (Ω)**	**E_{ON} (μJ)**	**|d*v*/d*t*| (V/ns)**
A	4.4	5.48	14	1.5	60.88	119
B	16	12.42(+126%)	5.189(-63%)	13	122.2(+100%)	46 (-61%)
C	4.4	11.51(+110%)	5.163(-63%)	1.5	89.14(+46%)	46 (-61%)

*Similar points as defined in **Figure 3.1** for peak d*v*/d*t* values.

In the upper half of the table, values for low load current (where higher values of dv/dt are expected) are presented. In the bottom half of the table, values with a higher load current are presented where the difference in E_{on} can be significantly higher.

It is interesting to note here that latter on, most of the extracted experimental data are for a low load current. This point is interesting because it is when the highest dv/dt can be achieved during turn-on transients. If the system is demonstrated working with the highest possible dv/dt, it should then work fine for lower values of dv/dt as well. Therefore, low load current corresponds to the worst-case scenario for the feedback loop. After demonstrating that the system is working for low load currents, higher values of load currents are interesting because it is when the highest amount of switching energy E_{on} can be saved with an independent control of dv/dt from the di/dt. We can see in **Figure 3.1** a comparison between points A, B and C for both GaN 48 V application and 400 V.



(a) (b)

Figure 3.1: Simulated reduction in E_{ON} for points A, B and C corresponding to the ones in **Table 3.4**. for GaN Transistors. (a) 48 V application (EPC2001C). (b) 400 V application (GS66508).

3.3 Chip 1 – Brief Overview of Previous Design for GaN

As previously mentioned, a past AGD design for GaN has been made in LAPLACE lab. It uses AMS0.18 technology with 6 metal layers. The chip dimensions are 2650 µm × 1900 µm. It is packaged in QFN24 with 24 pins. The dimensions of the packaging are 6 mm × 6 mm. **Figure 3.2** shows the chip in the (a) packaging and (b) bare die from an optical microscope picture. The preliminary characterization was done during my Master research project [147] and further

implementations and additional characterizations in power converters were done during this thesis. This CMOS AGD was designed based on numerical Design of Experiments in CADENCE™, to identify the best transistor sizes. The detailed analysis presented in chapter 2 was obviously not available back then. However, this prototype was used as an initial set of parameters to model and further optimize the ultra-fast feedback loop.

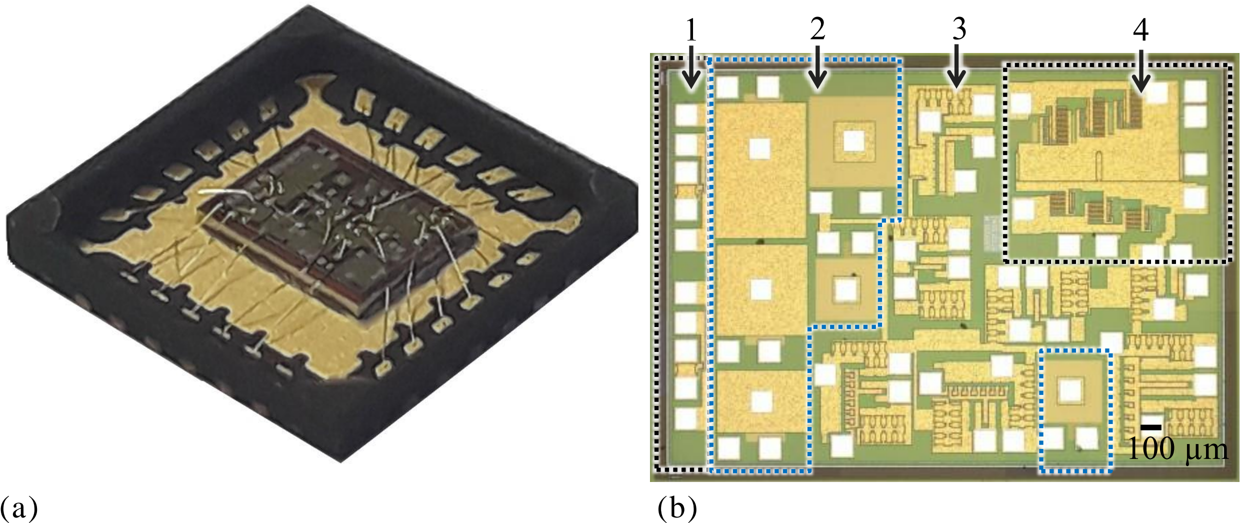
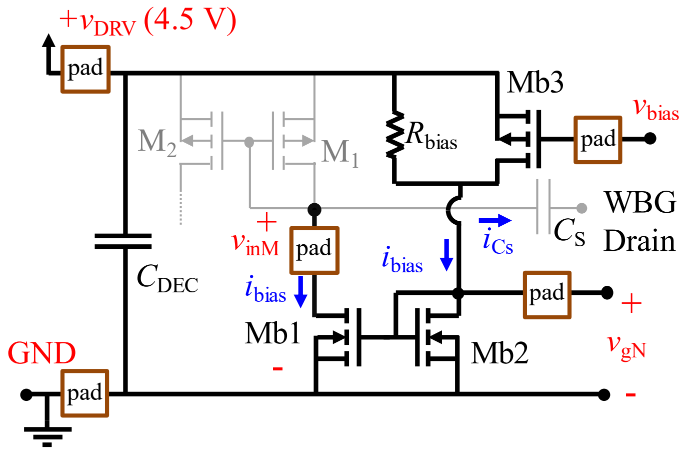
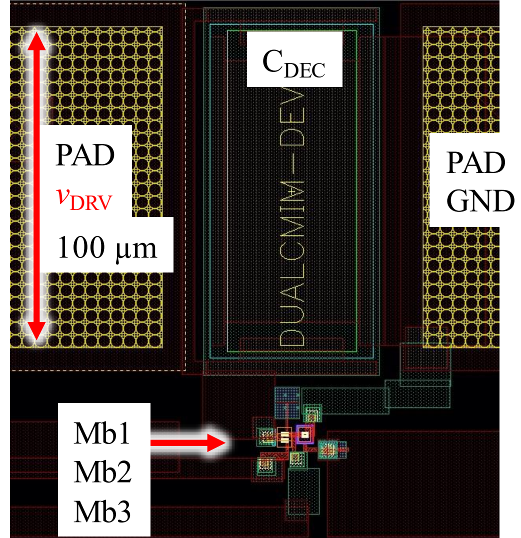


Figure 3.2: AGD previously developed at LAPLACE lab for GaN Transistors. (a) Packaged in 6 mm × 6 mm QFN24. (b) Microscope picture of the silicon bare die. Different blocs are 1: biasing current generator; 2: high voltage capacitors; 3: current mirrors; 4: main stage buffer.

The test chip is composed of different blocs, which are main stage driver, current mirror, embedded high voltage capacitors and biasing circuits.

The biasing circuit (**Figure 3.3**) was designed to operate from 1 µA to 10 µA and this current can be adjusted either with an external resistor R_{bias} or a voltage (v_{bias}) applied to the gate of Mb3 PMOS ranging from 3.5 V to 4.5 V. It is recommended not to exceed a drain current of 10 µA or a gate voltage less than 3.5 V to avoid excessive supply current consumption. Also, as already discussed in Chapter 2, if the biasing value is high, (1 mA for example) multiplied by a gain of 50, will have a i_{FB} current that will undesirably affect the switching speed during the pre-biasing phase of the current mirror. The width of transistors Mb1 to Mb3 are sized to the minimum value of 0.7 µm for a 5 V transistor with 0.7 µm of length.





(a) (b)

Figure 3.3: Biasing circuit placed in the input of the current mirror (a) schematic and (b) layout.

In this chip, the high voltage sensing capacitors (C_S) are designed between different metal layers. One design is between metal 5 and metal 6. Another design is between metal 3 and 5 and one last design between metal 4 and 5.

The other parts of this test chip (marked as number 3 in **Figure 3.2**) are 7 different current mirrors. The main idea was to use two different strategies one consists of smaller transistor M1 for a small value of sensing capacitor C_S that are the first three current mirrors in **Table 3.5**. The second strategy consists in using a higher value of W1 to be used with a biasing current. The sizes of each transistor for each current mirror are given in **Table 3.5**. To illustrate one line of this table, **Figure 3.4** is the current mirror called G20bias.

TABLE 3.5: WIDTH OF EACH TRANSISTOR OF THE AGD FOR GAN

Current mirror	W_1	W_2	W_3	W_4	Surface S	i_{FB} output current
	(µm)				(mm^2)	(mA)
G5	152	228	292	972	0.15	185
G10	133	265	340	1696	0.19	320
G20	106	317	405	2700	0.19	520
G5bias	1130	1697	292	972	0.23	185
G10bias	990	1975	340	1696	0.26	320
G20bias	789	2367	405	2700	0.26	520
G50bias	789	3450	608	6790	0.35	800

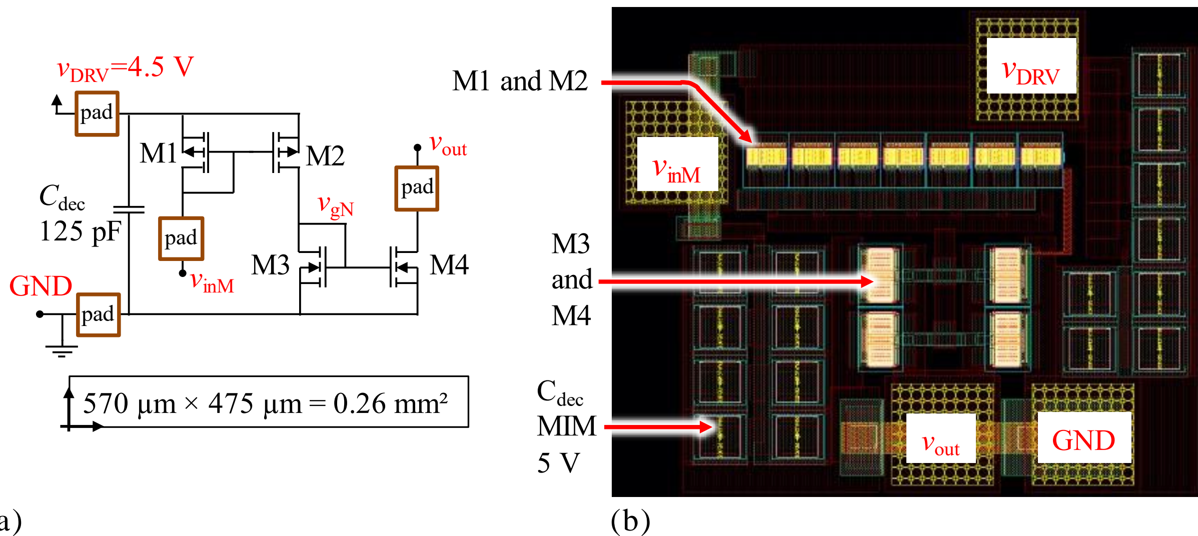


Figure 3.4: Current mirror G20bias (a) schematic and (b) layout. Block dimensions are 440 µm × 580 µm = 0.26 mm^2. It is designed to have i_{Cs} = 26 mA for v_{inM} = 3 V and i_{FB} = 520 mA for v_{out} = 3 V. Pads dimensions are 114 µm × 144 µm and parasitic CM capacitance is 300 fF.

3.4 Chip 2 – AGD for SiC

One possible circuit topology for the dv/dt feedback control loop to drive a SiC transistor is similar to that of the AGD developed for GaN HEMT (see **Figure 3.5**). The only difference in this topology is that the main stage buffer (transistors M5 and M6) and transistor M4 must withstand higher voltages (v_{DSmax}). Based on the specifications of SiC MOSFETs (i.e. v_{GS} recommended and absolute range values), the maximum drain-to-source breakdown voltages of M5 and M6 must be higher than 30 V. In the chosen CMOS technology (XFAB XT018), the more appropriate transistors have a 40 V drain-to-source breakdown voltage, to be driven by the 5 V core (5 V typical gate-to-source voltage driving of transistors M5 and M6). As previously discussed in **section 3.2.1**, transistors M1 to M3 can be designed similarly to the GaN application using 5 V transistors, only M4 must be a higher voltage transistor with a similar drain-to-source breakdown voltage capability as transistors M5-M6. Similarly to M5 and M6, M4 gate oxide is compatible with a 5 V gate-to-source driving which allows it to be associated with the 5 V M3 transistor.

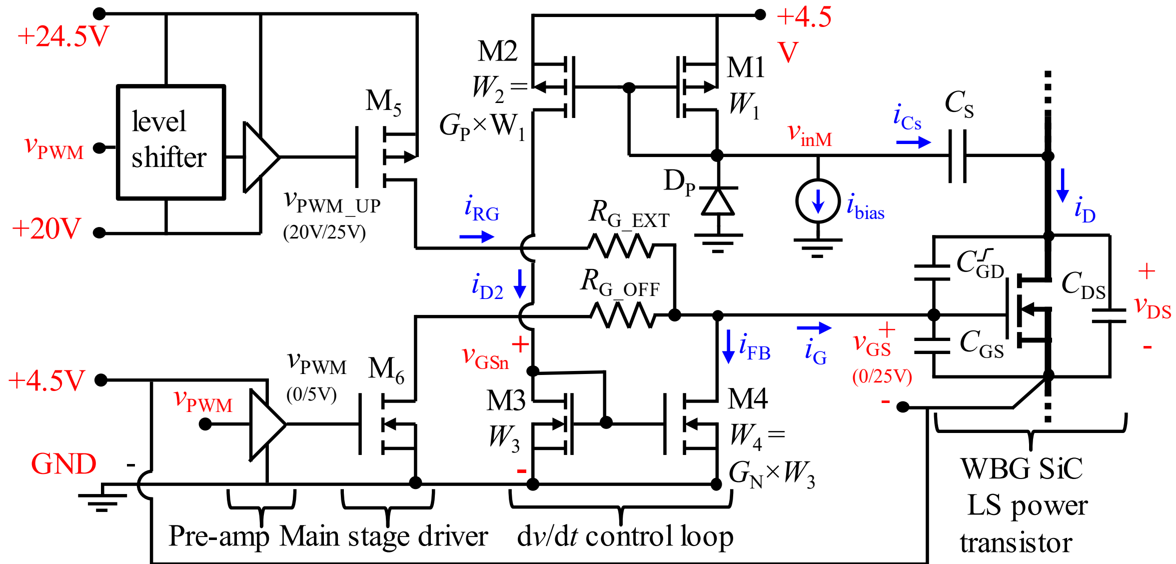


Figure 3.5: Overall schematic of the AGD for SiC WBG transistors. Transistors M1 to M3 are 5V transistors and M4 to M6 are high voltage transistors (v_{DSmax} = 40V and v_{GSmax} = 5V). The lowest potential in the chip is called GND but could be seen as -5 V from the power device point of view.

Figure 3.6 shows the order of magnitude of expected d*v*/d*t* values as a first design specification. An example of this work's objective is to experimentally obtain the waveforms in this figure due to the designed AGD. This objective is to experimentally measure in the oscilloscope the fall time (defined as 90% to 10%) that corresponds to t_R in the datasheet of the SiC power devices, change from the value in open-loop (t_{R_OL}) to the value in closed-loop (t_{R_CL}). The v_{bus_DC} HV DC bus voltage is specified to the typical value of 540 V used in aircraft applications, instead of 400 V for the GaN AGD. In order to show the good performance of the system and a low delay, R_{G_EXT} value will be chosen to be 2.5 Ω or 0 Ω and therefore the value of d*v*/d*t* will be around 54 V/ns (see **Table 3.3**). The total time to switch the voltage will increase from 10 ns to 19 ns from open to close-loop control. The fall time (90% to 10%) will increase from around 8 ns to around 17 ns. Similarly to GaN devices, one of the key constraints is to actively control the d*v*/d*t* within the first nanosecond to allow a precise control of the turn-on sequence, switching losses and EMI spectrum.

Closed-loop feedback system can be developed to impose a targeted value to d*v*/d*t*. SiC devices can achieve many tens of V/ns and a feedback system could limit these values to a constant target, 27 V/ns see **Figure 3.6** for this example. The desired attenuation of around 2 is targeted in a first step and more detailed after.

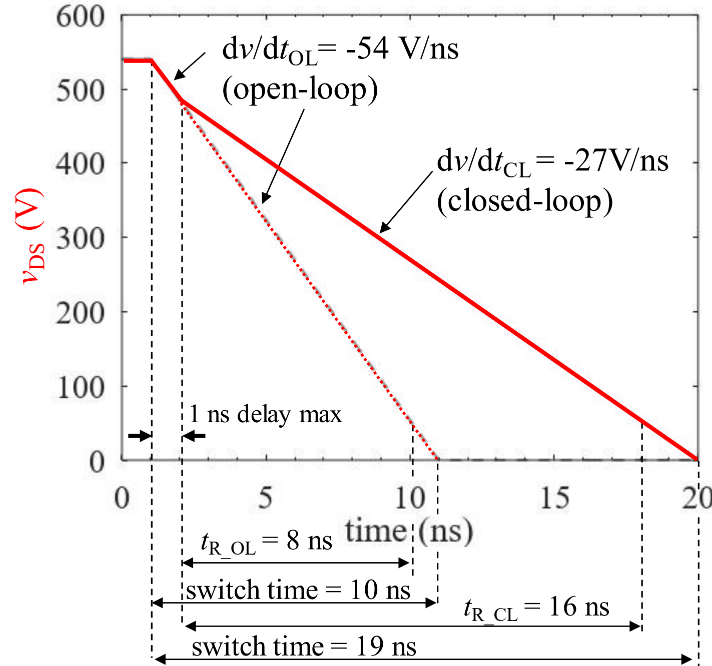


Figure 3.6: Example of expected waveforms at turn-on, to be measured by the designed CMOS AGD for SiC MOSFETs. It is desired to obtain 50% attenuation in dv/dt from -54 V/ns to -27 V/ns using the feedback loop. Therefore, the fall time in the oscilloscope screen (from 90% to 10%) should change from t_{R_OL} = 8 ns to t_{R_CL} = 16 ns.

One of the objectives of this work is to model and optimize the feedback loop (as presented in chapter 2), to investigate its application with GaN power devices and to design an adapted solution for SiC MOSFETs. "Chip 2" in the next sections refers to the developed AGD to work with SiC MOSFETs, typically for the devices C3M0075120K and C3M0016120K. One first step in the project is to import the model of the power device provided by the manufacturer to the CMOS design environment CADENCE™ Virtuoso™. (Please refer to **Annex 3: Translating Spice Simulations File (.lib) into CADENCETM (.scs)**).

It is important to import the transistor model into Cadence because parameters of the power WBG transistor should be taken into account to obtain the value of the dv/dt in open-loop configuration with the appropriate size of M5. If the value of dv/dt in open-loop changes, all the project specifications would change.

3.4.1 Simulating d*v*/d*t* in Open-loop Configuration

After the SiC power transistor is successfully imported in CADENCE™ (Please refer to **Annex 3: Translating Spice Simulations File (.lib) into CADENCETM (.scs)**), some simulations are conducted to obtain the value of dv/dt

in open-loop to be compared with the analytical values. The open-loop d*v*/d*t* represents a typical turn-on without the AGD controlling the switching speed. A low value of R_G is chosen so the d*i*/d*t* value can be maximized for a lower switching energy. A low value of load current is set to be able to have the highest possible d*v*/d*t* in open-loop, as discussed hereinbefore. If the AGD circuits are designed for the highest open-loop value of d*v*/d*t* with the highest possible attenuation, the system should work for all other operating points. Increasing load current or gate resistance should not affect the capability to control d*v*/d*t* of the circuit.

To make the same AGD work with a wide range of SiC power devices, at least two different power devices of two different values of current capability are considered. One power device for low current C3M0075120K (30A) and another one with higher current capability C3M0016120K (120A). Both simulations are made with low load current of 1 A for the reason explained in the previous paragraph. A simple assumption is that if the system is designed for both a high and low load current devices, the entire system should work for a wide range of components available in the market with specifications between those two values of current.

Combining the imported model of the power devices with the adapted main stage buffer designed in LAPLACE, values of d*v*/d*t* in open-loop are obtained. These values depend on the model of the power device imported in Cadence™ and the size of M5, the PMOS output transistor of the main stage buffer. The d*v*/d*t* in open-loop values are shown in **Table 3.6** below. The last column i_{G_OL} is the gate current observed during Miller's plateau. Resistor R_G is considered from 0 to 20 **Ω** with one point in the middle for 10 **Ω**, which covers the range of values recommended by the manufacturer.

TABLE 3.6: SIMULATED VALUE OF D*V*/D*T* IN OPEN-LOOP CONFIGURATION

Device	R_{G_INT} (Ω)	C_{rss} @200V (pF)	R_{G_EXT} (Ω)	d*v*/d*t* peak OL (V/ns)	i_{G_OL} (mA)
C3M0075120k	10.5	6	0	51	390
C3M0075120k			10	38	276
C3M0075120k			20	30	210
C3M0016120k	2.6	20	0	47	670
C3M0016120k			10	33	470
C3M0016120k			20	24	335

Simulated with T_A=27°C and v_{GS}=0/20 V

Notice that the two SiC power devices have a ratio between C_{rss} of around 3. Therefore, using a C_S value 3 times higher, the same values of gain should provide

the same controllability in dv/dt for these two power devices. The maximum value of current should not be exceeded for the transistor M1. In other words, the minimum value of voltage in the input of the current mirrors (v_{inM}) should not exceed the maximum excursion during a turn-on transient.

The next part of the project specifies values of gain to be implemented in the chip to be experimentally tested. Those values are calculated from (2.19).

The expected dv/dt attenuation by the dv/dt control loop is shown in the **Table 3.7** below for the device C3M0075120k. These values would be the same in case the device C3M0016120k is used with a sensing capacitor Cs = 3 pF instead of 1 pF.

TABLE 3.7: THEORETICAL EXPECTED DV/DT ATTENUATION

Attenuation factor (A_{tt})	dv/dt attenuation	$G{\cdot}C_S/\ C_{\mathrm{rss}}$	$G{\cdot}C_S$ (C_{rss}=6 pF) For SiC transistors	G (C_S=1 pF) if r_{p}=1*
1	0%	0	0	0
4/3	25%	1/3	2 pF	2
2	50%	1	6 pF	6
4	75%	3	18 pF	18
5	80%	4	24 pF	24

*The parameter r_{p} will be defined and explained in the next section.

As already discussed in the previous chapters, the dv/dt as a function of gain or $G{\cdot}C_{\mathrm{S}}$ is expressed by (3.2).

$$\frac{\mathrm{d}v_{\mathrm{DS}}}{\mathrm{d}t} = \left|\frac{v_{\mathrm{DRV}} - v_{\mathrm{M}}}{R_{\mathrm{G}}\left(C_{\mathrm{rss}} + r_{\mathrm{p}} G C_{\mathrm{S}}\right)}\right| \tag{3.2}$$

where v_{DRV} is the power supply voltage of the driver, v_{M} is the Miller plateau voltage, R_{G} is the total resistance to access the gate, C_{rss} the reverse transfer capacitance of the WBG power device, G the total gain of the current mirrors, Cs the sensing capacitor and r_{p} the performance parameter to be defined and explained in the next section.

After the open-loop values are obtained and some values of gain suggested in **Table 3.7**, the theoretical expected attenuation in dv/dt is plotted in **Figure 3.7** using Matlab™. Notice that those functions are plotted from (3.2) and can also be seen in **Figure 3.7** (a). Values of dv/dt for G10 with Cs = 2 pF correspond to the values of G = 20 and Cs = 1 pF. Therefore the 12 points marked in **Figure 3.7** (a) are the same as just 8 points in **Figure 3.7** (b).

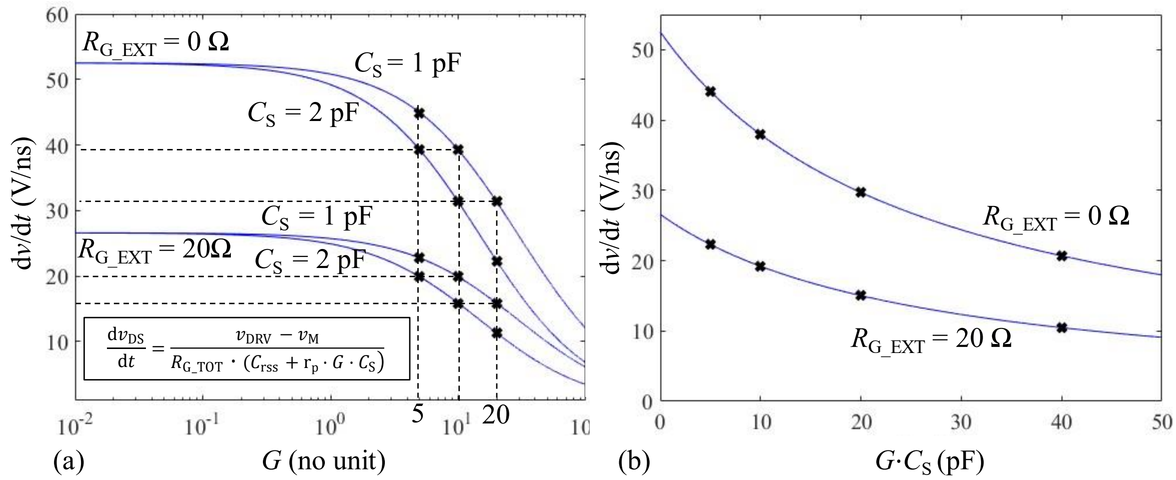


Figure 3.7: Expected d*v*/d*t* reduction as a function of (a) gain G and (b) the product of the gain by the sensing capacitor C_S, for the SiC power device C3M0016120K. Increasing the gain will decrease the d*v*/d*t*. Points marked with × are the current mirrors designed with G=5, 10 and 20.

Each point in this figure represents one choice of the total gain G for the current mirrors. It is constructed and implemented in the chip current mirrors with gain 5, 10 and 20. All those values are analytically calculated and represent an ideal behavior of the system. In practice a higher feedback current is required to have this ideal attenuation in d*v*/d*t* from **Table 3.7**. The reason for this difference of ideal behavior and the performance of the feedback loop is explained in next section.

3.4.2 Feedback Loop Performance

The feedback loop can have a different performance according to the operating point and design specifications of the main stage PMOS transistor M5 during a switch-on event. To understand the relationship between the performance of the feedback loop and the operating point of the transistor M5, the gate node of the power device is shown below in **Figure 3.8**.

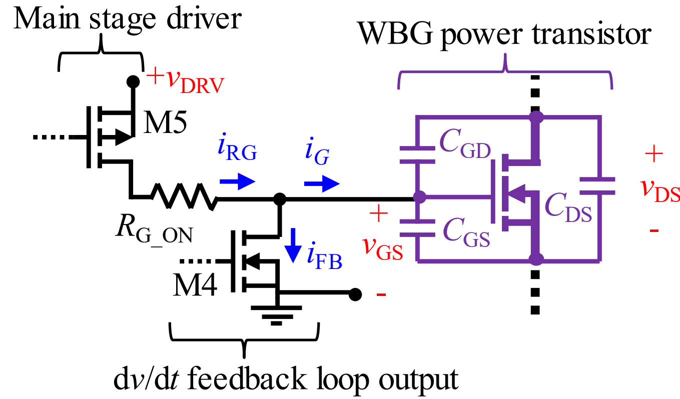


Figure 3.8. The gate node of the power device and the three currents to control the d*v*/d*t* during the Miller's plateau.

Kirchhoff law can be applied and the resulting current going to the gate of the power device is expressed as:

$$i_G = i_{R_G} - i_{FB} \tag{3.3}$$

Transistor M4 is always operating in saturation mode, therefore its behavior can be simplified to a current source. The same does not occur to the transistor M5 as the operating point depends on the sizing of width of M5. When a current is subtracted from the gate node i_{FB}, transistor M5 will behave in three different cases. The first case, called case A in **Figure 3.9**, is the ideal behavior of the method. The ideal behavior is when a subtracted current by the feedback loop will directly affect the current going to the gate of the power device. For example, subtracting 0.5 A in the feedback loop (i_{FB}) from 1 A being provided by the main stage buffer M5 (i_{RG}) will result in a reduction from 1 A to 0.5 A going to the gate of the power device (i_G). In simulation, cases different than this ideal situation have been observed. It has been observed in simulation that the 1 A current flowing through M5 (i_{RG}) would not stay constant when the feedback loop subtracts a current from the gate node. In the worst-case scenario (case C in **Figure 3.9**), a current (i_{FB}) subtracted of 0.5 A from 1 A (i_{RG}) results in no change in d*v*/d*t* value. There was no change because the main stage buffer M5 (i_{RG}) just provided 1.5 A and the resulting current going to the gate of the power device (i_G) did not change from 1A.

The three cases with three different performances for the feedback loop are shown in **Figure 3.9**.

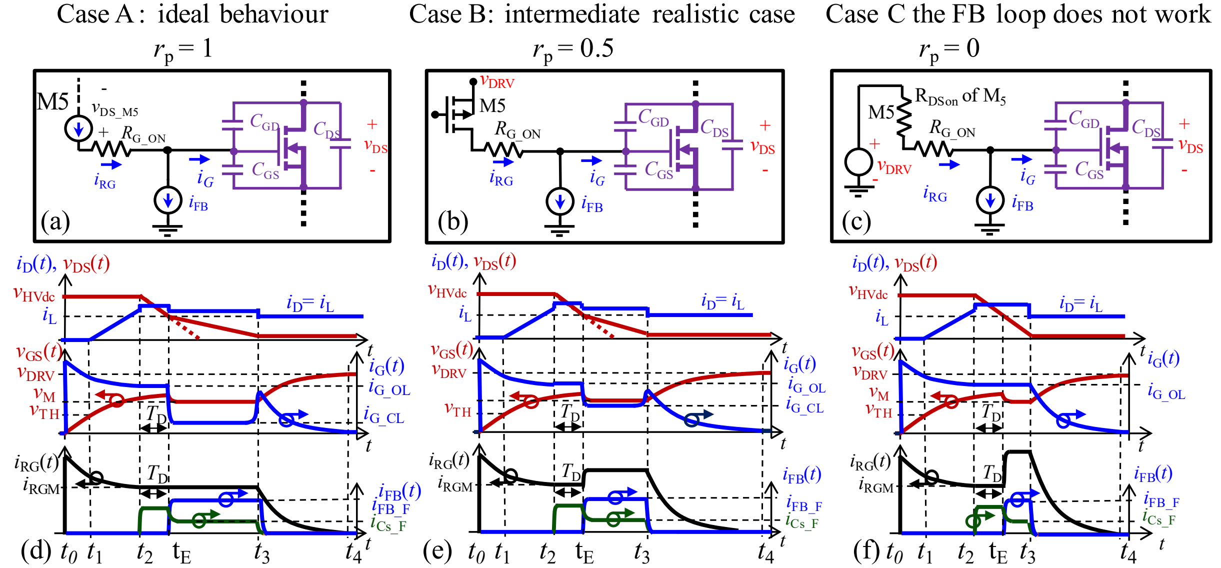


Figure 3.9: The three different cases with three different performance values r_p. (a) The ideal behavior. (b) The realistic intermediate case. (c) The worse-case scenario where all the current being pulled from the gate node i_{FB} is not affecting i_G because the main stage PMOS M5 is providing an additional amount of current to all the subtracted current (i_{RG}).

Notice that case C is a worst-case scenario where even pulling a current from gate node i_{FB} will not affect the current i_G. In this case C, the feedback loop will not work at all. The case B is a realistic scenario seen in simulations where some current is needed to put M5 in saturation regime before the loop act to control and reduce the dv/dt. The performance parameter r_p is defined in equation (3.4) as the amount of current being useful to control the dv/dt divided by all the current being sunk by the feedback loop.

$$r_p = \frac{i_{G_{OL}} - i_{G_{CL}}}{i_{FB_F}} \tag{3.4}$$

Another easy way to understand this concept is just look at the current i_{RG} when the feed-back loop becomes active. The more it changes the worse is the performance of the feedback loop to try to control the current going to the gate of the power device. Notice in **Figure 3.9** that the performance parameter r_p for the case A is 100%. It can be explained because all the feedback current i_{FB_F} is useful and it is the same as the difference between the current flowing to the gate of the power device before (i_{G_OL}) and after (i_{G_CL}) the feedback loop is active. For case C (**Figure 3.9**), the worst case is 0% and for case B it is illustrated 50% of feedback loop performance. The worst case is when transistor M5 will simply provide an incremental current (i_{G_CL} - i_{G_OL}) with exactly the value of i_{FB_F}. In this case,

transistor M5 is behaving similarly as a voltage source, simply providing more current when more current is being sunk.

Different simulations were conducted to assess r_p as a function of external gate resistor R_G or load current. It was observed that it is necessary to adapt the main stage driver (W_5 the width of M5 transistor) to have a saturation current (i_{Dsat}) close to the value of current during the Miller plateau (i_{G_OL}). Notice that smaller the value of the transistor, the better the performance of the feedback loop but it will represent a slower turn-on event in open-loop (without the method). The best point in this trade-off is if the designed transistor M5 has a saturation current (i_{Dsat}) close to the Miller's plateau current (i_{G_OL}).

Therefore, as a conclusion of this observed issue, the main stage buffer was designed to have a saturation current (i_{Dsat}) value close to the values of the current during the Miller's plateau (i_{G_OL}). See **Table 3.6** for the values of current during Miller's plateau (i_{G_OL}) for the two SiC transistor chosen. For this reason, the main stage buffer is calculated to have the saturation current i_{Dsat} = 660 mA, (see **Figure 3.10**).

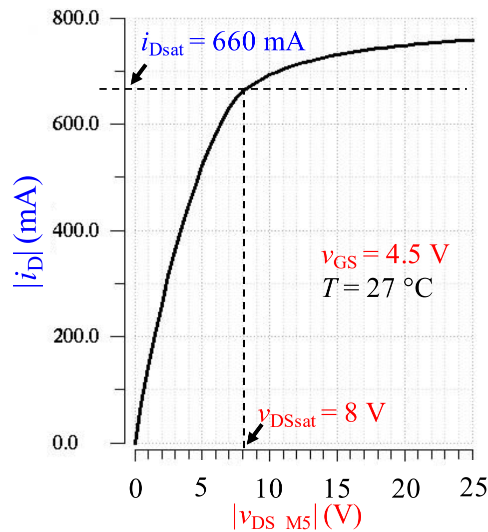


Figure 3.10: i_D–v_{DS} characteristic for the transistor PMOS M5 of the main stage buffer for width W_5=4.32 mm. It is designed to have i_{Dsat} close to the value of i_{RG_OL} to be compatible with the power devices C3M0016120K and C3M0075120K (and therefore a wide range of devices).

Notice that to control the dv/dt without using the feedback loop, the case C can also be used. Therefore, the 3 cases when sizing the main stage driver transistor M5 can be obtained as illustrated in **Figure 3.11**.

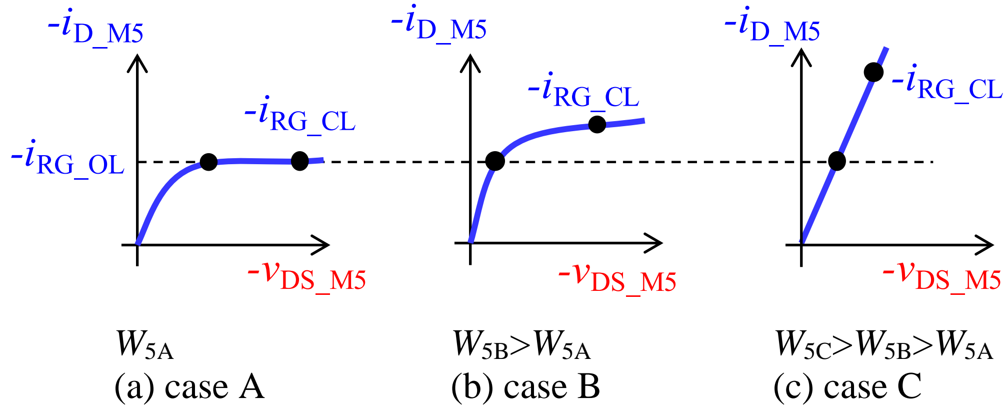


Figure 3.11. The three cases corresponding to different values of W_5. (a) The ideal case where the saturation current of M5 i_{Dsat_M5} is equal to the open-loop current (i_{G_OL}) and ideally the transistor M5 does not supply more current when the feedback loop is closed. (b) The realistic case where an (acceptable) increase in i_{D5} is observed when closing the loop. (c) The worst-case scenario where the feedback loop does not work but the dv/dt could be controlled by other methods.

Case A: The width of M5, W_5 correspond to sizing W_5 to match $i_{Dsat_M5} = i_{G_OL}$ of the power device. The saturation current of M5, i_{Dsat_M5}, is equal to the open-loop current (i_{G_OL}) and ideally the transistor M5 does not supply more current when the feedback loop is closed. The advantages of this sizing for Case A are:

1. The current i_G can be tuned if the driver has a split PMOS output. No need to add R_{G_EXT} resistors to control the dv/dt
2. When using the feedback loop the i_{G_OL} cannot exceed i_{Dsat_M5}
3. The gate current can be controlled enabling more or less transistors M5 in parallel or it can be set by changing the voltage applied to v_{SG} in M5.

The disadvantages of this case are:

1. The thermal losses that should be dissipated outside the GD are all dissipated inside the chip. Thus, the maximum allowed switching frequency of a converter using this method is reduced.
2. The i_G current being dependent on this saturation current means the dv/dt is much more sensitive to parameter dispersion. Parameter values that depends on temperature, power supply voltage, process variations and v_{GS} variation will affect the dv/dt.
3. The GD is designed for only one specific power device.

Case C: The width of M5, (W_5) is such that the saturation current of M5 (i_{Dsat_M5}) is much higher than the gate current during the Miller's plateau ($i_{Dsat_M5} >> i_{G_OL}$). The advantages of this case to control dv/dt is:

1. Thermal losses $v_{DS} \times i_D$ in the PMOS M5 are lower than in case A. Less thermal dissipation means higher values of switching frequency can be achieved.
2. The designer can control the dv/dt with an external resistor R_{G_EXT} in a wide range of values, the current during Miller's plateau i_G can be set between i_{Dsat_M5} and 0.

Disadvantages:

1. The proposed feedback loop does not work to control the dv/dt. It has to be controlled by one or more external gate resistor $R_{G_EXT.}$
2. To change the values of R_{G_EXT}, the resistor should be soldered. Otherwise, a split output PMOS M5 should have as many outputs as desired values of dv/dt.

Case B: Represents the realistic intermediate case between case A and C, where most of the simulation results are obtained. The performance parameter r_p ranges from 0.2 to 0.9 depending on values of W_5, load current, temperature, and R_{G_EXT}.

More details can be seen in the simulations in **section 3.4.4**.

3.4.3 Schematic of the Main Stage Buffer for SiC Devices

Transistors M5 and M6 are relatively complex to design because of the pre-amp and digital logic required. The main stage buffer was developed in the thesis of Yazan Barazi [146] in LAPLACE lab and for this work, this buffer has been adapted. The buffer designed for another thesis in LAPLACE has a soft shut-down, active Miller clamping and high impedance output mode [148]. Those functions were simplified and deleted for this work in order to concentrate in the active feedback loop. This buffer has split PMOS and split NMOS architectures. It is possible to control different values of current to provide the power device gate charges. The split PMOS makes it possible to control the initial dv/dt with different values of external gate resistors R_{G1} and R_{G2}. Therefore, three values of gate current can be achieved (i_{G3}, i_{G2}, i_{G1}). Those values can be also set to zero and the dv/dt would be controlled by the maximum current the PMOS transistors (M5) are capable to provide. A segmented driver makes it possible to control dv/dt, di/dt and propagation delay [93]

[149] [150] [95] [151] [152] [153] [154] [155] [156]. In the case of an application with a switching leg with two SiC power devices for HS (high side) and LS (low-side), the dead-time adaptation should be taken into consideration [157] [158] [159] [160] [161] [162] [163].

A proposed strategy to be used with the segmented output is presented in **Figure 3.12** above. This strategy combines both segmented driver with the active closed-loop to control the d*v*/d*t*. The idea is flattening the d*v*/d*t* curve as a function of load current. The closed-loop control is used for a higher level of load current in **Figure 3.12** when the i_G is also suggested to be higher (i_{G4}).

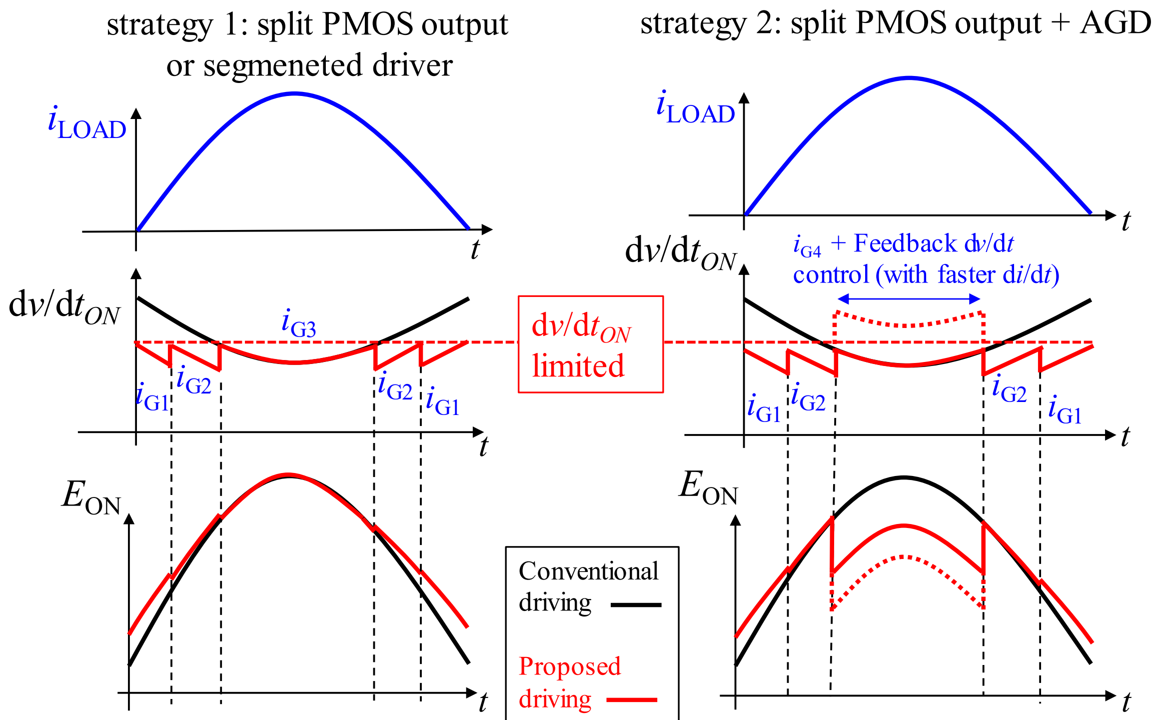


Figure 3.12. Suggested strategy to be used with segmented driver and active feedback control loop. Notice that the gate current can be controlled with either segmented driver topology or the feedback loop and also that $i_{G4} > i_{G3} > i_{G2} > i_{G1}$.

This buffer is copied and simplified and the value of W_5 is adapted. The simplified buffer shown in **Figure 3.13** has two multiplexer blocs to enable or not the two transistors in parallel named M5a and M5b (PMOS) or M6a and M6b (NMOS). For example, if the bits EnP1 and EnP2 are set to "00", the buffer will not provide any current in the event of PWM input in high state. If this binary information is set to "01", the current provided by the PMOS M5a output transistors could be up to 0.7 A (temperature and voltage dependent as previously discussed in **Figure 3.10**). If the binary information in the bits EnP1 and EnP2 are set to "11" the

maximum current the buffer can provide is with M5a and M5b in parallel is equal to 3.5 A (temperature and voltage depending). The value of 0.7A is obtained after parametric simulation changing the width of M5 to obtain a better performance parameter r_p for the power devices C3M0016120K and C3M0075120K. The open-loop Miller currents (i_M) are 670 mA and 390 mA respectively.

The optimal number of stages for the buffer regarding the propagation delay is around 3 from the mathematical analysis first presented in [164] and also commented in the textbook [165]. Thus, the designed buffer has 3 current amplification stages.

Notice that the main stage buffer needs a level shifter to shift up the logic signal from [0 to 5 V] to [20 V to 25 V] because M5 is controlled applying a voltage referenced to v_{DRV}=25 V. This block Buffer also needs a dead-time delay to avoid the PMOS (represented by M5) to turn-on at the same time as the NMOS transistors (represented by M6), avoiding a short circuit. If those transistors switch at same time it would represent a small short circuit condition and the power consumption of this block would be higher.

Regarding routing in CADENCE™, **Figure 3.13** shows in blue high current paths that are placed close to the edges of the chip to avoid resistive path. In red, 5 signal pads for digital signals that does not carry high current. The layout of this buffer is presented in section **3.4.5** and **Figure 3.16**.

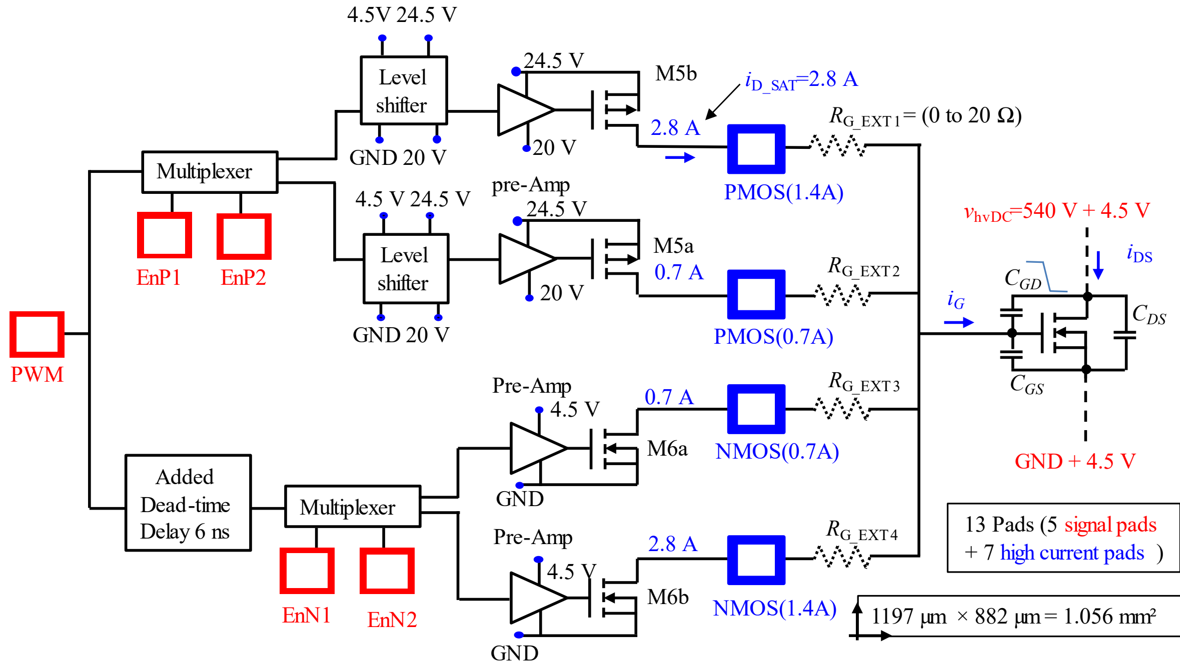


Figure 3.13: Main stage buffer developed in the thesis of Yazan Barazi [146] and adapted to have a saturation current (i_{Dsat} = 660 mA) close to the value of Miller's plateau current during a turn-on event to avoid the problem described in previous section 3.4.2.

3.4.4 Simulation of the Expected Behavior of the AGD SiC

After the theoretical study showing the optimal distribution between $G \cdot C_S$ in chapter 2, **Table 3.8** shows all the current mirrors designed in the CMOS AGD prototype for SiC MOSFETs. Each line of the table represents one different feedback loop made of two current mirrors. The selected values of total gain are 5, 10 and 20. First 3 current mirrors are designed to operate with C_S = 2 pF and the highest attenuation in dv/dt are expected at G = 20. Simulation corresponding to this point are given in **Figure 3.14**. The value of 2 pF is chosen to demonstrate the best performance possible in a prototype because optimization studies in chapter 2 demonstrate the feedback loop delay ($t_{D50\%}$) is smaller for higher values of C_S. Values above 2 pF would consume too much silicon surface.

The following 3 current mirrors (numbers 4, 5 and 6) are designed to operate with a sensing capacitor C_S = 1 pF. The objective of having these dimensions is to be able to compare experimentally the behavior of different values of C_S with the same product $G{\cdot}C_S$ to be able to validate the theoretical tendencies studied in chapter 2. The same product $G{\cdot}C_S$ doesn't give the same attenuation in the simulations because the performance parameter also changes.

The last four current mirrors (number 7 to 10) are designed to operate with different biasing points in order to experimentally verify the theoretical predictions that the first 6 current mirrors will have a lower delay time. A lower delay time in a step response corresponds to a higher bandwidth that is the most important performance parameter of the project.

TABLE 3.8: WIDTH OF THE FOUR TRANSISTORS W1 TO W4 FOR EACH CURRENT MIRROR CONSTRUCTED IN THE CHIP AGD SIC.

Name CM#	C_S (pF)	G	G_P (no unit)	G_N	W_1	W_2	W_3 (µm)	W_4	S (µm²)	dv/dt att.
1	2	5	1.64	3.05	1200	1968	787	4800	630215	25%
2	2	10	2.4	4.17	1000	2400	960	8000	110047	>25%
3	2	20	3.39	5.9	776	2630	1052	12416	116425	50%
4	1	5	1.64	3.05	776	1272	509	3104	51807	<25%
5	1	10	2.4	4.17	582	1397	559	4656	64855	25%
6	1	20	3.39	5.9	388	1315	526	6208	82545	>25%
7	1	20	1	20	388	388	155	6208	73154	50%
8	1	20	5	4	388	1940	776	6208	76580	50%
9	1	20	3.39	5.9	388	1315	52	3513	56744	50%
10	1	20	3.39	5.9	388	1315	305	5000	72040	50%

Table 3.8 shows all the devices designed and constructed in the chip. A simulation is performed for each of the current mirrors with a double pulse setup, using the diode E4D05120A in the HS (high-side) to obtain a faster dv/dt. For the current mirror number 3 (CM#3), the third line in **Table 3.8**, the expected reduction in dv/dt is shown in **Figure 3.14**. On the left, (a) is for the power device C3M0075120K and (b) for C3M0016120K. The high-side has a SiC diode E4D05120A, the AGD is connected to the low-side the switching waveform is a double pulse. The load is simulated with a current source.

The first plot shows the desired impact in the switching node v_{DS}. Blue lines correspond to results in open-loop (or without the closed-loop active method) and green lines for closed-loop behavior (or with the method). The second plot shows the current in the sensing capacitor of 2 pF. This current corresponds to the time derivative of v_{DS}. The following 3 curves are the currents in the gate node of the power device. For the 115 A SiC device C3M0016120K the attenuation is slightly lower with the same value of Cs = 2 pF but the feedback loop performance is better. It can be seen that the current in R_G does not significantly change because the saturation current of M5 (i_{Dsat_M5}=660 mA) is closer to the value of Miller's plateau

for this device. Assuming R_{G_EXT}=0 Ω, the open-loop currents are 670 mA and 390 mA respectively for C3M0016120K and C3M0075120K, see **Table 3.6**.

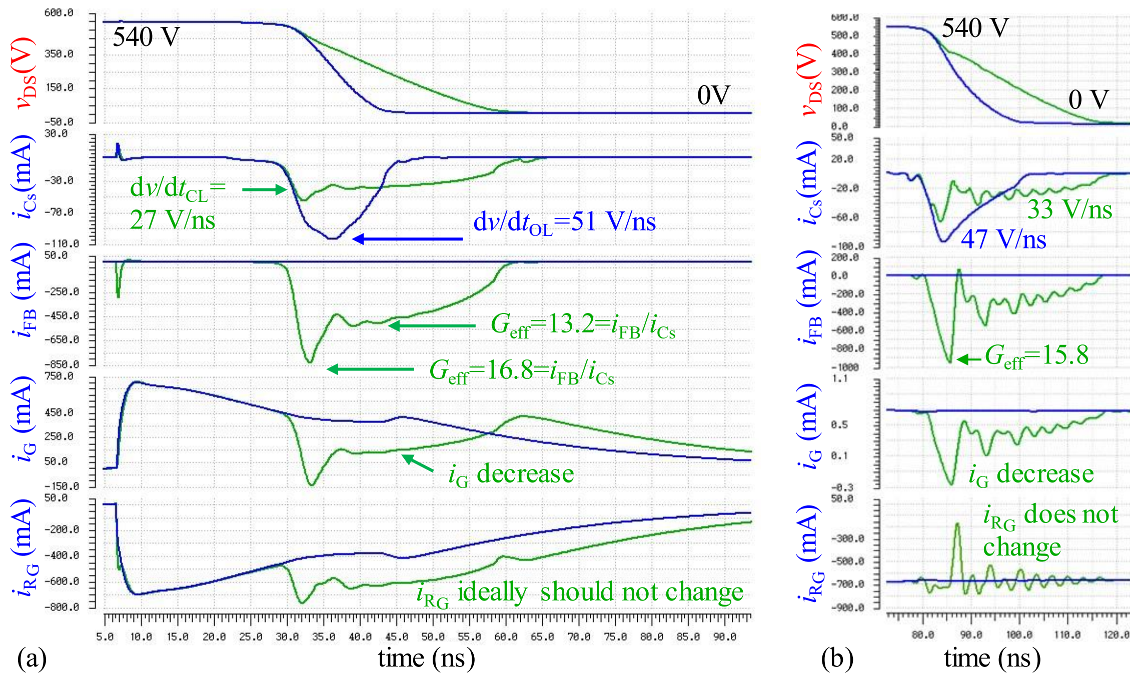


Figure 3.14: Simulated waveforms for gain G=20 (CM#3) and for (a) C3M0075120K and (b) C3M0016120K power device. Conditions for the simulation are i_L = 1 A, R_{G_EXT} = 1 mΩ, C_S = 2 pF and T_A=27°C.

3.4.5 Layout of the CMOS AGD for SiC

The overall image of the AGD layout for SiC in CADENCE™ can be seen in **Figure 3.15**. The following images in this section are a zoom at different sections of the chip. The overall silicon area for the AGD is 7.5 mm^2, with additional area used for test functions designed in other projects (those extra blocks can be seen in the top part of **Figure 3.15** marked as 5) to reach a total area of 9.9 mm². The functions have been designed during the second and third year of this PhD, and the final files were submitted for fabrication in March 2020. At the time of writing, these functions are still being fabricated by the foundry, and should back from fabrication (XFAB) and packaging (IMEC) in November 2020. The price is given per square millimeter but 10 mm^2 is the minimum for this technology for an academic project. The price for the fabrication of a prototype for the technology XFAB XT018 HV SOI is 1555 €/mm^2 through Europractice [166]. The price includes 50 bare dies, but additional dies can be bought for 10 €/extra die with a maximum of 50 extra units.

The number of requested prototypes is 70 chips. There will be 3 different bonding diagrams with 10 each, because the number of total pads is 80 and the packaging has 40 pins. Therefore 30 chips will arrive packaged in QFN40 pins (6 per 6 millimeters) and 40 chips will arrive in bare die for wafer probes tests.

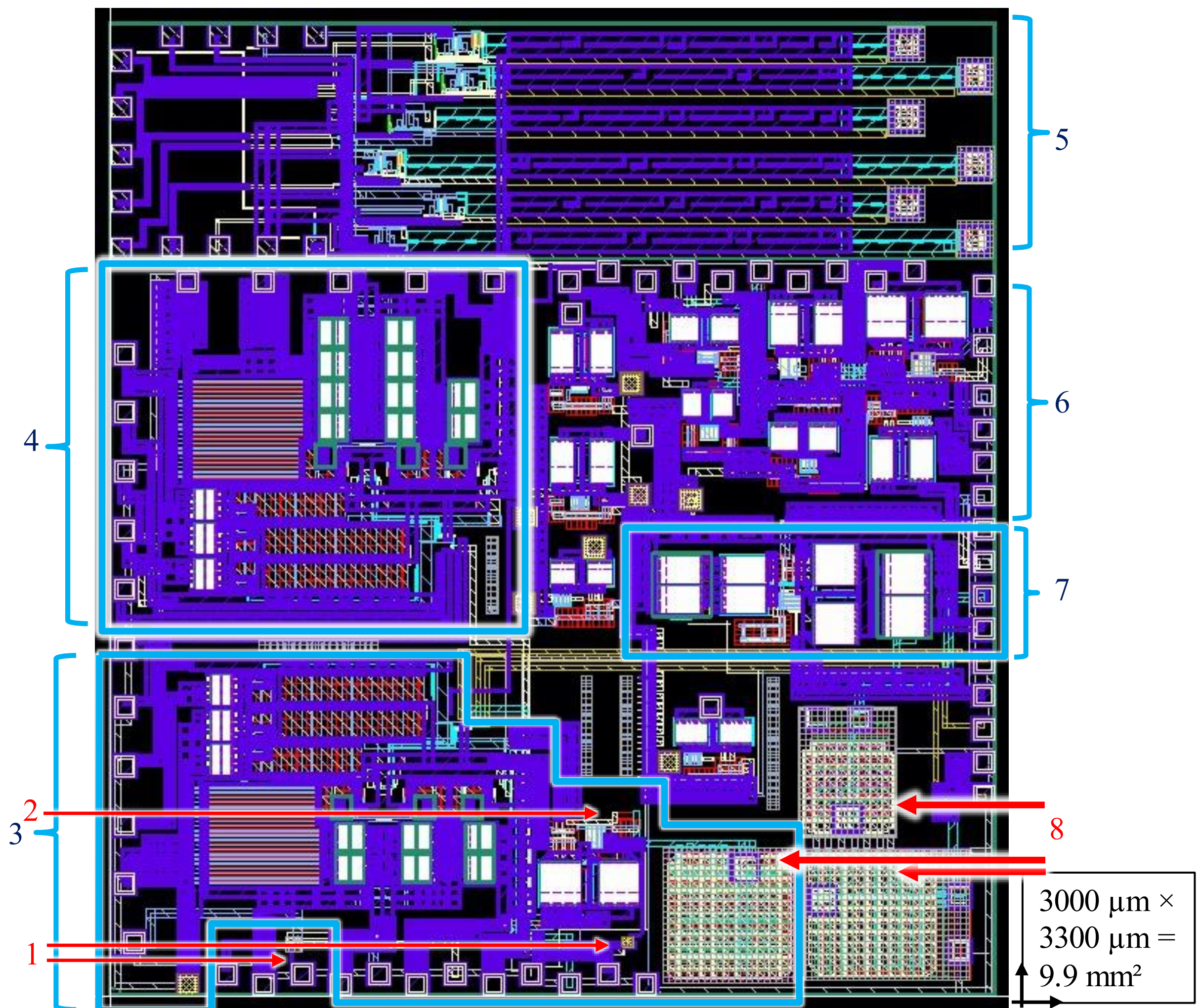


Figure 3.15: Layout of the AGD CMOS chip for SiC. Dimensions are 3 × 3.3 mm = 9.9 mm^2. 1: biasing current generators; 2: protection diode D_P; 3: Solution entirely integrated with main buffer, sensing capacitor, current mirror and biasing circuit connected; 4: main stage driver 5: other testing blocks about short circuit detection; 6: 10 different current mirrors containing M1 to M4 transistors; 7: binary gain circuit 8: high voltage sensing capacitors (C_S).

The test chip is designed to have different blocks. Some tests can be performed using wafer probe tests (blocks 6 and 8 in **Figure 3.15**) and others require the chip to be packaged and a PCB to connect the parts. All the current mirrors (number 6 in **Figure 3.15**) and the high voltage capacitors (number 8) can be tested using wafer probes test in the chip. The main stage buffer will only be tested in the packaged

solution. After individual blocks are tested separately, a more integrated solution can also be tested.

A more integrated solution is represented by the number 3 in **Figure 3.15**. A better performance could be achieved if the current mirrors, buffer and sensing capacitor are all in the same silicon die. The signal has less parasitic elements and a higher bandwidth can show a faster closed-loop response.

Figure 3.16 is a zoom in the main stage buffer previously noted as number 4 in **Figure 3.15**. The purple color is the top metal, the 6th metal layer. It has the lower series resistance per square (the exact value is under Non-Disclosure Agreement), therefore for a lower series parasitic resistance all the high current routing preferably uses this layer. Also, since it is the most distant layer from the substrate, it has less parasitic capacitance with ground potential.

One strategy for routing this main stage buffer consists in placing all the high current pads close to the chip edges where the connection pads are located. The low current pads are placed as far as possible from the chip edges and can be seen in the bottom right part represented by 8 in **Figure 3.16**. In this point, some diodes are also added connected using metal 1 layer to avoid antenna problems during fabrication.

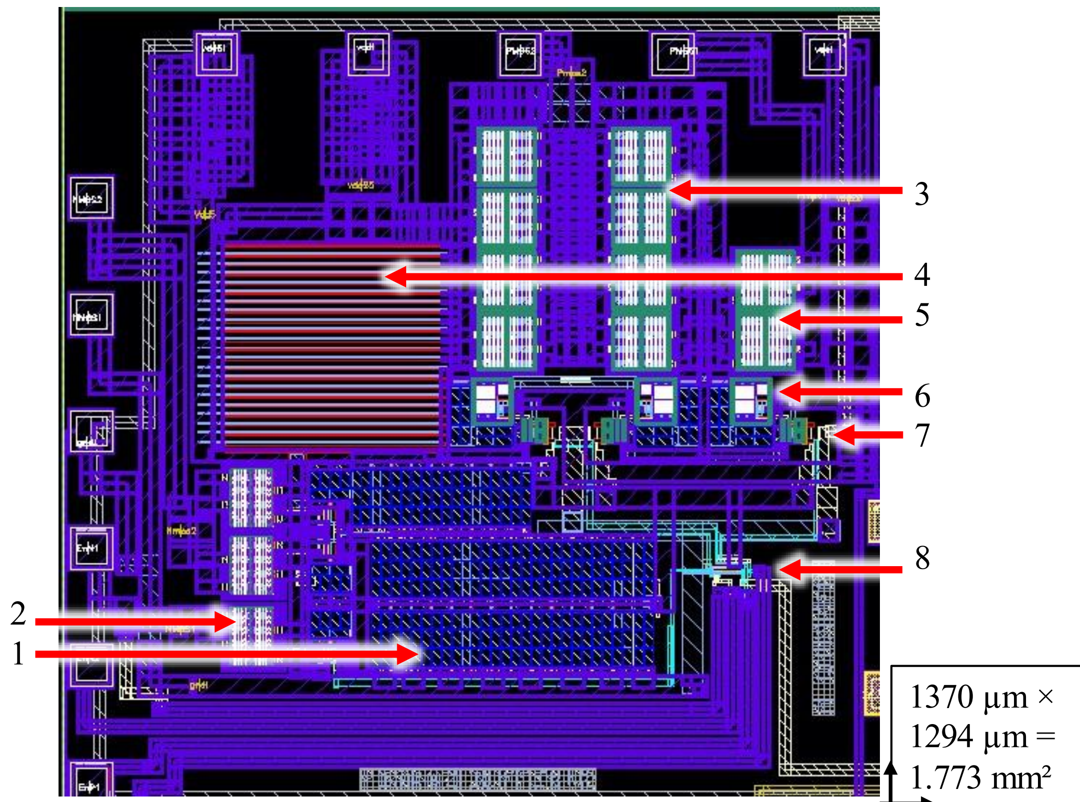


Figure 3.16: Detail to the main stage current buffer. 1: Decoupling capacitors 5V MIM. 2: NMOS called M6 in the main schematic (**Figure 3.5**). 3: PMOS M5b 4: Decoupling capacitors 40 V MIM,

5: PMOS M5a adjusted to i_{Dsat} = 0.7 A; 6: Pre-amplification stage; 7: level shifter; 8: digital blocs with the enable's logic.

Figure 3.17 is a zoom in one current mirror, noted as part 6 in **Figure 3.15**. Each transistor from M1 to M4 is represented in both schematic and layout in this figure. Decoupling capacitors are required to reduce voltage drop during operation. These on-chip decoupling capacitors will prevent voltage drop when high current will flow in the output of the current mirror during a dv/dt event. 30 pF of capacitance will reduce the voltage drop but decoupling capacitors of at least 50 nF (preferably 1 µF) will still be required in the testing PCB.

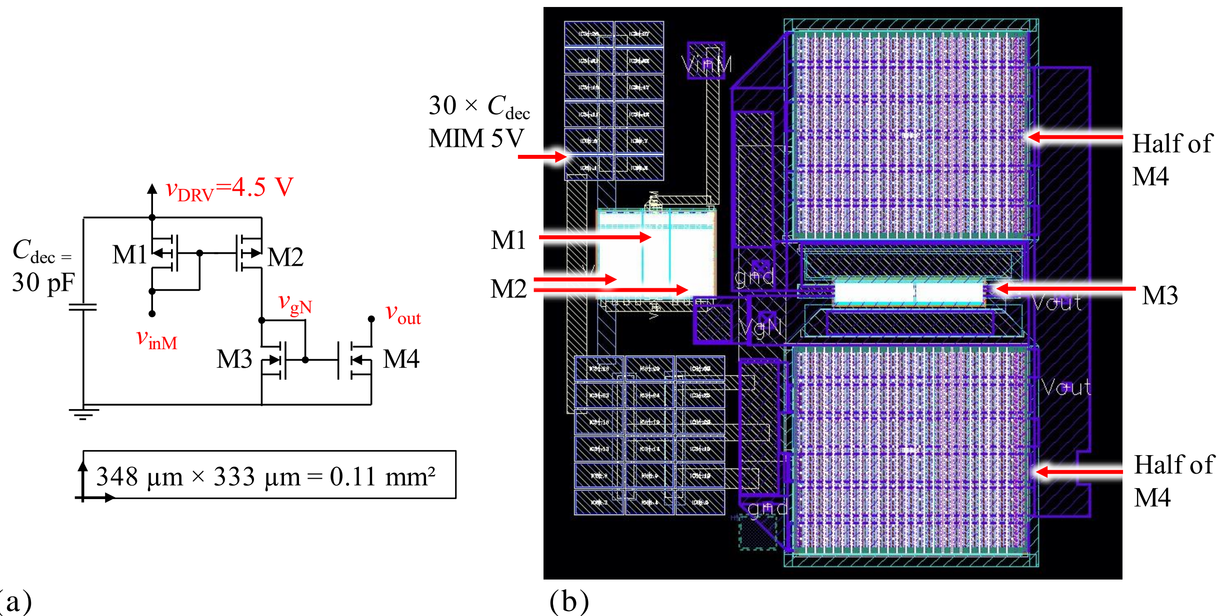
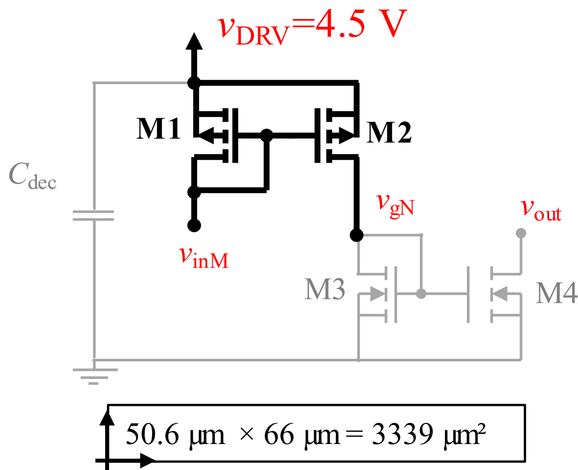
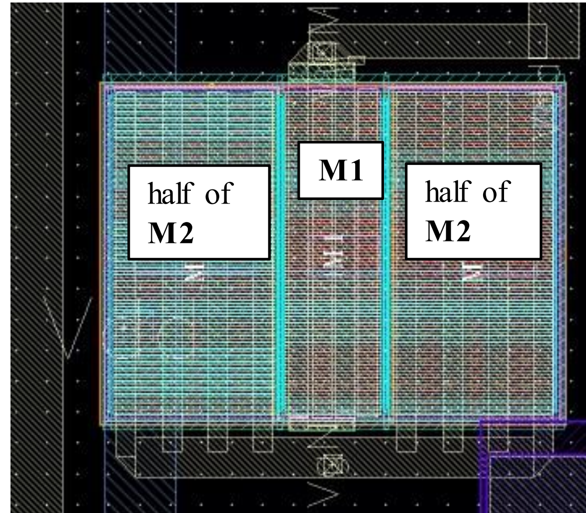


Figure 3.17: Current mirror G20 (designed to have a gain 20) and to operate with C_S=2pF. (a) Schematic corresponding to the (b) layout image from CADENCE™.

Figure 3.18 is a zoom in the connection of transistors M1 and M2. The files in the software CADENCE™ are made using many layers of hierarchical blocks. This connection shows a low-level block in the design. It can be noticed that transistor M2 is split in half to better distribute the current using fewer metal paths as possible since metal paths represents parasitic elements that degrade bandwidth.

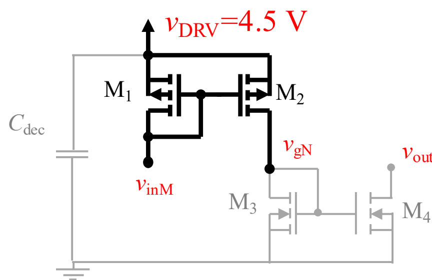


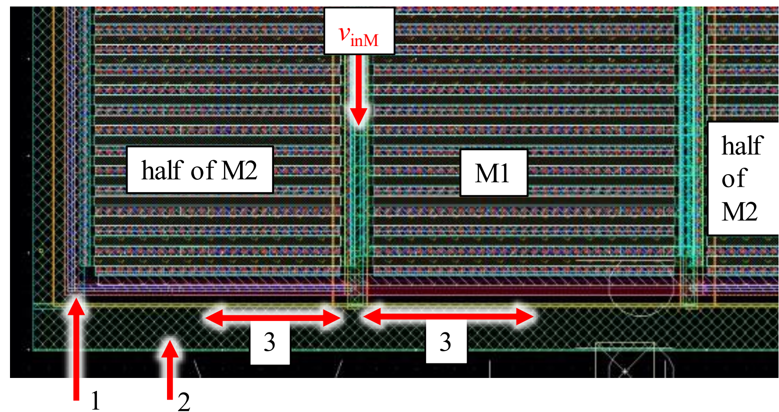


(a) (b)

Figure 3.18: Detail of a current mirror of gain 5. (a) Schematic with highlighted part corresponding to the (b) layout of the connection between transistors M1 and M2.

The routing strategy consist in connecting the gates of M1 and M2 using the polysilicon layer and the most underneath metal 1 layer. This strategy is presented also in **Figure 3.19**. In order to avoid a long path in highly resistive polysilicon, a connection ring goes around the transistor M2. The polysilicon is 4000 times more resistive than metal one layer when comparing values per square.





(a) (b)

Figure 3.19: Detail of a current mirror of gain 5. (a) Highlighted schematic corresponding to the (b) layout of the connection between transistors M1 and M2. 1: Guard-ring to prevent latch-up effect. 2: Connection ring around M2 to have the better 3: maximum distance the current has to go through highly resistive polysilicon 6 μm and 9 μm.

Regarding the biasing circuit for the AGD for SiC chip, a 3D view extruded from the exported GDS files is represented in **Figure 3.20** below.

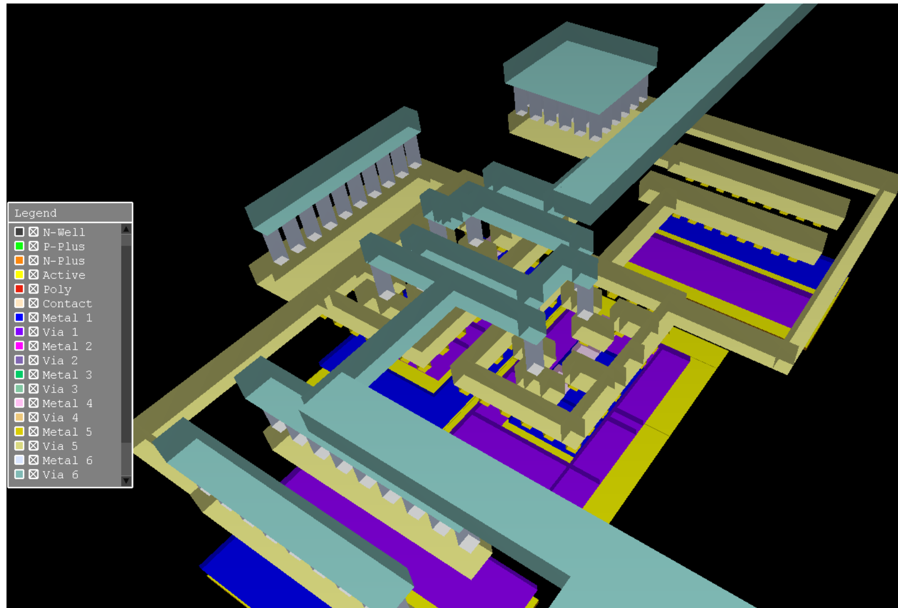


Figure 3.20. A 3D view extruded from the GDS files. The biasing current generator is made using 6 metal layers for the chip AGD for SiC.

3.4.6 d*v*/d*t* controllable by two bits

In the previous solution (number 6 in **Figure 3.15**), it is not possible to change the value of the gain. A solution that can have the values of gain controlled electronically by a binary word is therefore desired.

Connecting current mirrors with gain 20 and 10 the following circuit is created. The approach is to connect current mirrors together and adapt the architecture to be able to actively control the d*v*/d*t* with a binary word of two bits. The following topology is first described in [167], and implemented here as a first test circuit. Using the topology in **Figure 3.21** (a) the binary information is referenced to GND and not to the source of the transistors M6 or M8. Notice that the bulk of the transistors M6 and M8 are connected to the source of those transistors and this is possible by using a DTI layer around those transistors. The binary information is referenced between the node b_1 and GND. Notice that v_{out} node is connected to the gate of the power device and it will change from 0 to 25 V (equivalent to -5 V to 20 V). Therefore, transistors connecting to the potential v_{out} are 40 V transistors. Those transistors cannot exceed 5 V in the gate to source voltage. Simulation are performed to verify that using this topology the potential will not exceed 5 V in the gate of any of the transistors.

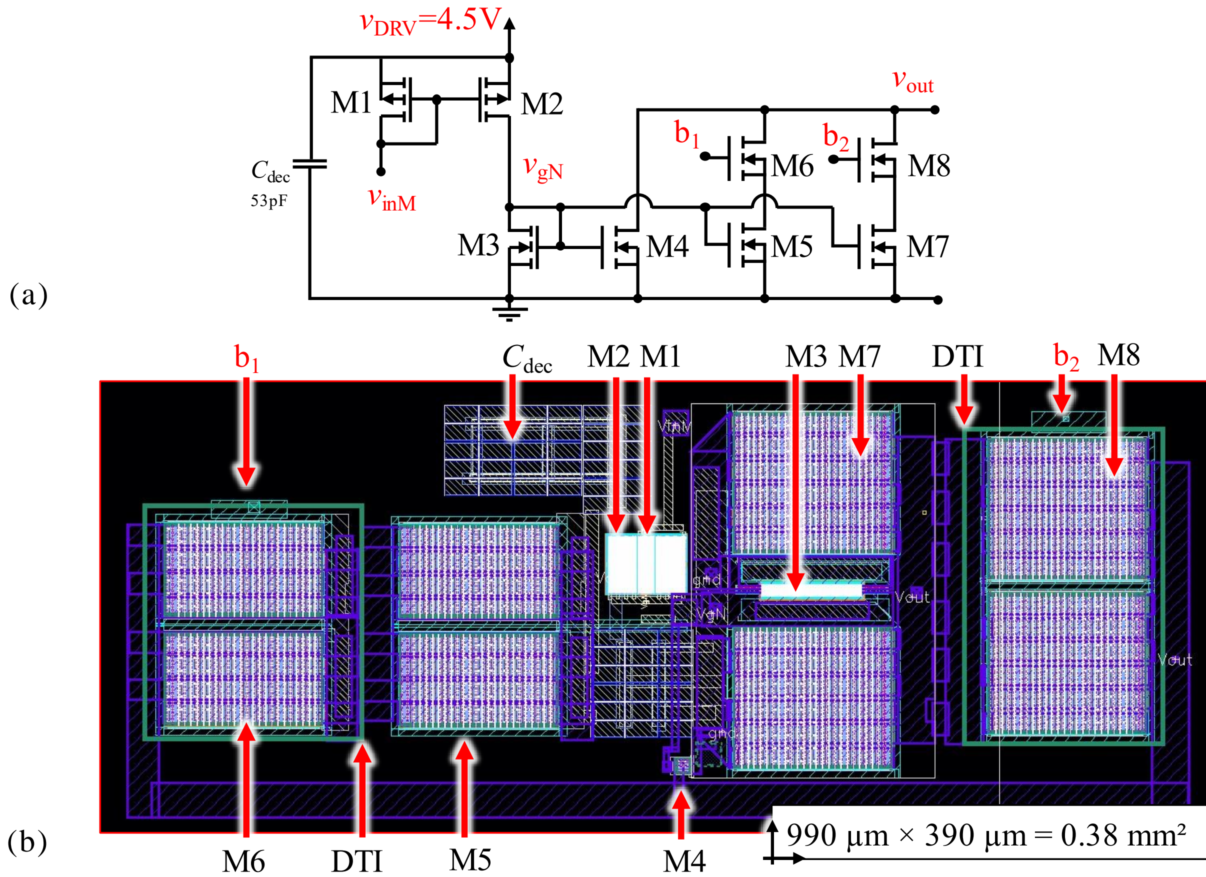


Figure 3.21: dv/dt controllable by two bits. (a) Schematics and (b) layout. Transistors M1 to M3 are 5V transistors and M4 to M8 are 40V transistors (v_{DSMAX} = 40 V, v_{GSMAX} = 5 V). Due to the DTI layer (green color) around M6 and M8, it is possible to isolate the bulk of those transistors and connect to the source of M5 and M7 and not to GND.

TABLE 3.9: SIMULATED BEHAVIOR OF THE BINARY GAIN CIRCUIT

Binary word (b_2b_1)	Gain G	$G \cdot C_S$ (pF)	Simulated dv/dt(V/ns)	Simulated Fall Time (ns))	Simulated dv/dt A_{tt} (%)
00	0.1	0.2	49.72	8.687	0
01	10	20	25.85	16.71	51.98
10	20	40	18.72	23.07	72.43
11	30	60	14.42	29.95	77.02

The widths of all transistors are: W_1 = 776 µm, W_2 = 2630 µm, W_3 = 1052 µm, W_4 = 40 µm, W_5 = 8000 µm, W_6 = 8000 µm, W_7 = 12416 µm, W_8 = 12416 µm. The performance in simulation changes the dv/dt from around 50 V/ns to 14 V/ns which corresponds to an attenuation of 77%. Intermediate values of attenuation are achieved for different values of the binary word. **Table 3.9** shows the expected attenuation and values of dv/dt for each configuration of the binary word.

3.4.7 Pads

Connection to the packaging of the chip is made with bonding wires soldered in the connection pads. The connection pads were designed with diode underneath to work as ESD (electrostatic discharge) protection. Electrostatic discharge subject the I/O pins of a chip to high-current, high voltage stress [168] [169] [117]. Superior ESD robustness can be achieved in SOI compared to bulk CMOS in less design area [170]. The diode called dpp6 in the design kit is a Zener diode of 6 V and will clamp undesired ESD transients as demonstrated in **Figure 3.22**. Simulation results shows a diode with 4 parts of 50 µm making a total of 200 µm which will be able to sink 90 mA at 6 V or 665 mA at 7 V (v_{DS} absolute max = 7 V for the 5 V transistors). In the third quadrant, for negative transient voltage, it should be able to sink 80 mA at -1 V or 968 mA at -2 V. The junction diode capacitance is 190 fF at normal operating condition of 4.5 V (reverse biasing) and the higher value of 400 fF at 0 V. In case it is forwarded biased it would have slightly more than 400 fF but it would represent a negative voltage applied to the pad. The diode leakage current is simulated from 120 µA at -40°C to 249 µA at 175°C

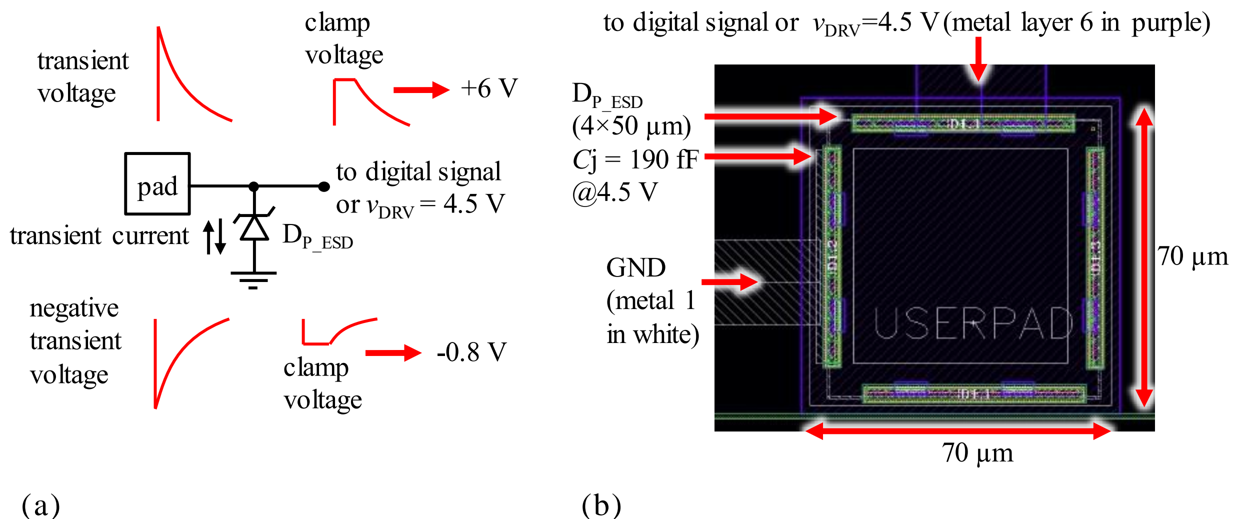


Figure 3.22: Design of protection diode D_P (a) operating principle (b) layout image. Protection diode D_P will prevent ESD (electrostatic discharge) and prevents damage to M1 transistor in case i_{Cs} current is too high.

Notice that the metal paths inside the chip contains parasitic resistance, inductance and capacitance values associated to it. **Figure 3.23** below represents the parasitic values of resistance and inductance respectively as R_{met} and L_{met} from the power supply to the blocks in the chip.

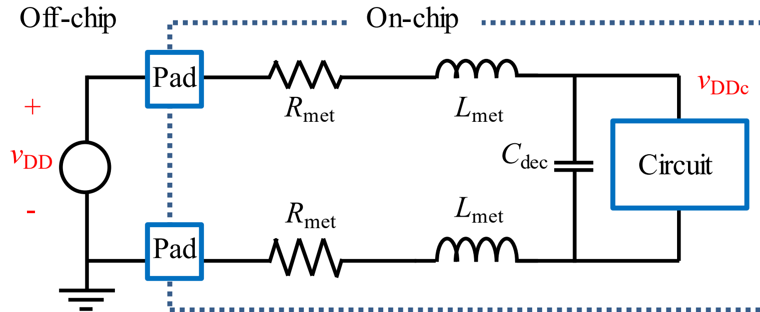


Figure 3.23. The parasitic values of resistance and inductance associated to the metal path in the chip are considered during routing. The conductors are non-ideal, attention is made to calculate those values to become negligible compared to the values in the chip.

3.5 Preliminary Characterization (Wafer Probe Tests)

This section is related to the chip AGD for GaN with AMS0.18 technology.

In order to verify the overall chip, blocks are separately tested. The current mirrors can be tested by applying a sequence of pulse of currents using a source measure unit (SMU) Keithley 2612B. The source meter is connected to wafer probes to execute the tests directly into the silicon bare die. The connection diagram is represented in **Figure 3.24** below. Pulses are short in duration, 1 ms with period of 5 ms to avoid a significant increase in temperature, which could change significantly the expected behavior when compared to the behavior from ambient temperature of 27 degrees Celsius (simulation default value in Cadence^{TM}).

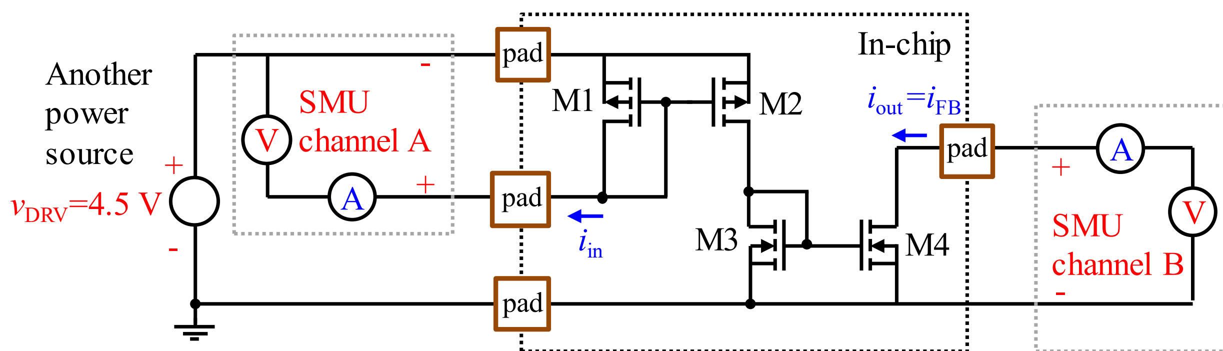


Figure 3.24. Characterization of the current mirrors with connections to the SMU (source measure unit) and power source. In each pad a wafer probe connects the measuring device to the silicon bare die.

26 sequential current pulses are generated in ascending order ranging from 0 to 25 mA. Each pulse will stay during 1 ms in the desired value and goes OFF for 4

ms, to complete a period of 5 ms. The output current (i_{out}) as a function of input current for all current mirror is measured and plotted in the same image in **Figure 3.25**

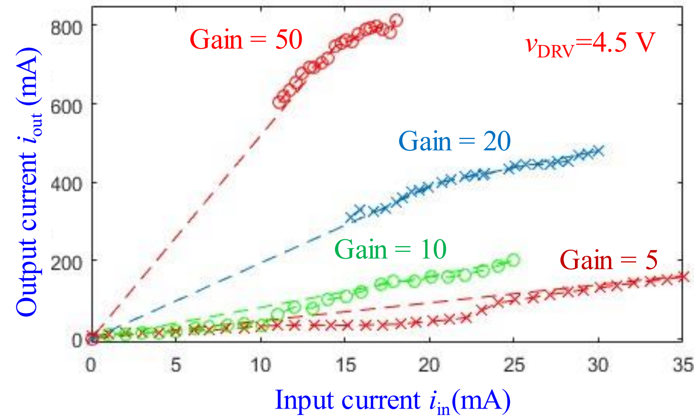


Figure 3.25: Measured current using waver probe in the bare die. Each independent current mirror from gains 5 to 50 for the AGD GaN Chip 1.

Some differences between analytically expected values and obtained experimentally are observed (see **Figure 3.26**). These differences can be attributed to parameters dispersion during fabrication, wafer probes contact resistance, junction temperature and parasitic series resistance in the 6 metal layers inside the chip. For example, for the current mirror of gain 10, with an input current of 25 mA, the output current is measured 205 mA instead of 250 mA. Notice that this is a difference of 18% and is considered acceptable.

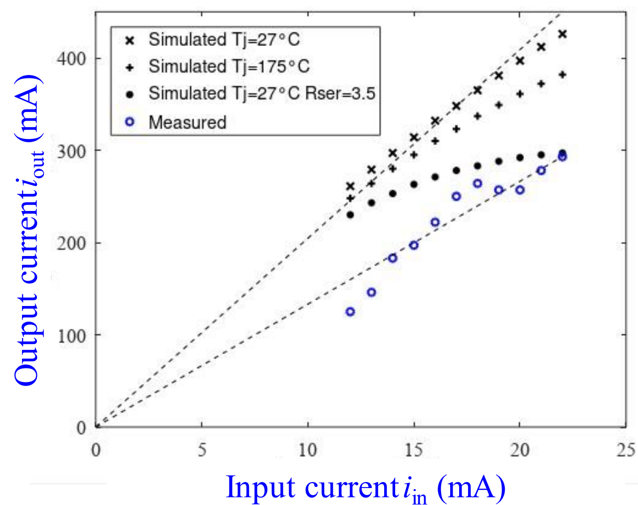


Figure 3.26. Characterization of the current mirror of gain 20. Comparing measured and simulated results. Notice that the wafer probe tip adds some series resistance in the measure, the value of *R*ser=3.5 Ω is added to the simulated model in each one of the four probes.

3.6 PCB Design and Implementation

The chip presented in section **3.3** will now be tested in a double pulse setup to measure the effect of the feedback loop in controlling the d*v*/d*t*. The CMOS GD chip 1 was connected to the low-side power transistor, while the gate of the high-side transistor was shorted to its source in order to obtain symmetrical elements and similar values of intrinsic capacitance (C_{oss}) for the power devices. The output power load is an air inductor with a low parasitic capacitance (C_{PAR}=160 pF) measured at 1 MHz. The schematic is presented below in **Figure 3.27**. The reason for having two external gate resistors in parallel is achieve a better controllability and solder easily the SMD discrete resistor with dimensions 0603.

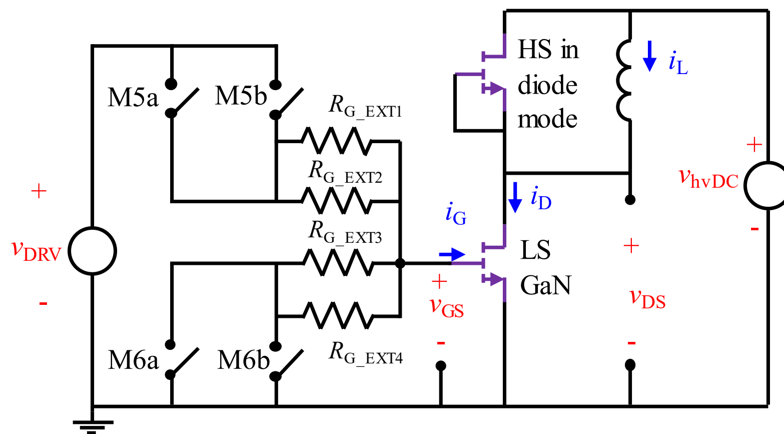


Figure 3.27. Schematic of the double pulse setup board for the applications with GaN power transistors.

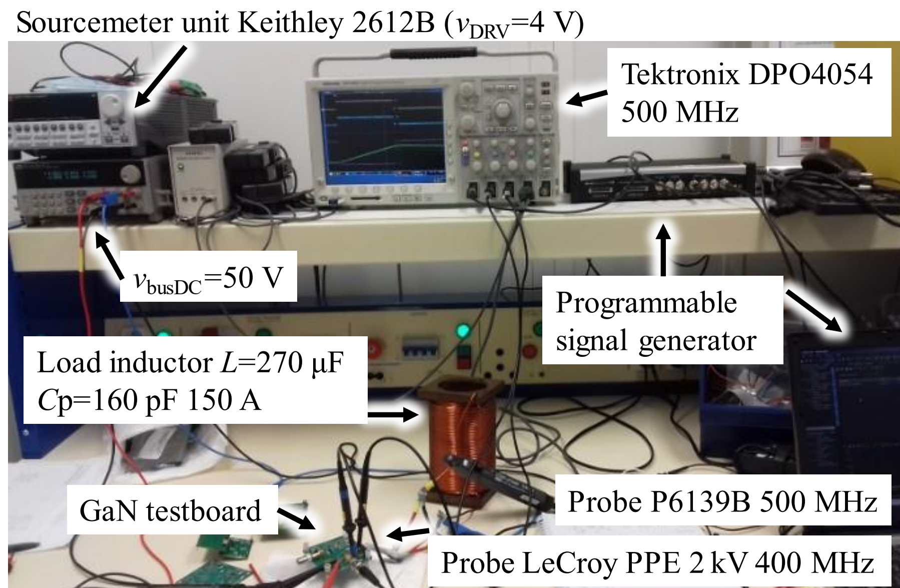


Figure 3.28. AGD high d*v*/d*t* measurement Testbench.

Tests are carried out using the parameters shown in **Figure 3.28** and in **Table 3.10**. The printed circuit boards are routed and assembled. For soldering the GaN with µm precision, a machine called Zevac is used.

TABLE 3.10: TEST BENCH AND MEASUREMENT SETUP FOR EPC2001C AND FOR GS66508T

Name	PARAMETER	
v_{hvDC}	48 V	400 V
Power transistor	GaN EPC2001C 100 V 36 A 7 mΩ	GaN GS66508T 650 V 30 A 50 mΩ
C_{rss}	20 pF - 150 pF	2 pF - 60 pF
v_{DRV}	4 V	3 V
C_S sensing capacitor	2 pF ceramic external capacitor MC0805N2R0C500CT	1 pF ceramic external (MC0805N1R0C501CT) or integrated (Met6-4) capacitors
R_G (ON)	4.4 Ω	1.5 Ω (and 4.4 Ω)
Load inductor	L=270 µF C_{PAR}=160 pF 150 A	L=270 µF C_{PAR}=160 pF 150 A
T_A	22°C	22°C
Oscilloscope	Tektronix DPO4054 500 MHz	Tektronix DPO4054 500 MHz
Probes	P6139B 500 MHz (max 300V)	LeCroy PPE 2 kV 400 MHz
i_L	1.3 A	2.5 A
PCB dielectric thickness between L1 and L2	288 µm	123 µm

3.6.1 48V Application

For the 48 V application, 6 PCB (**Figure 3.29**) were built with layout considerations to minimize the parasitic inductances of both the power and control loops of the power transistor [125], [171]. Each PCB uses 4 layers, for this reason. The dielectric thickness is 288 µm between metal layers 1 and 2 to reduce the inductance of the power loop. Two low-voltage decoupling capacitors with a capacitance of 1 µF are placed close to the GD to supply the peak current required during the switching transients, in addition to decoupling the capacitors integrated on-chip. The sensing capacitor C_S was integrated either on-chip or externally.

Attention is also paid to minimize the PCB parasitic capacitance between drain and source of the power device.

Consequently, this PCB is only used for double pulse tests with our CMOS AGD driving EPC GaN HEMTs or GaN System devices, with the active control implemented at the low-side transistor. Neither the drain nor the gate currents are probed to comply with extremely low parasitics both for the power loop and the driving loop. Parameters are summarized in **Table 3.10**.

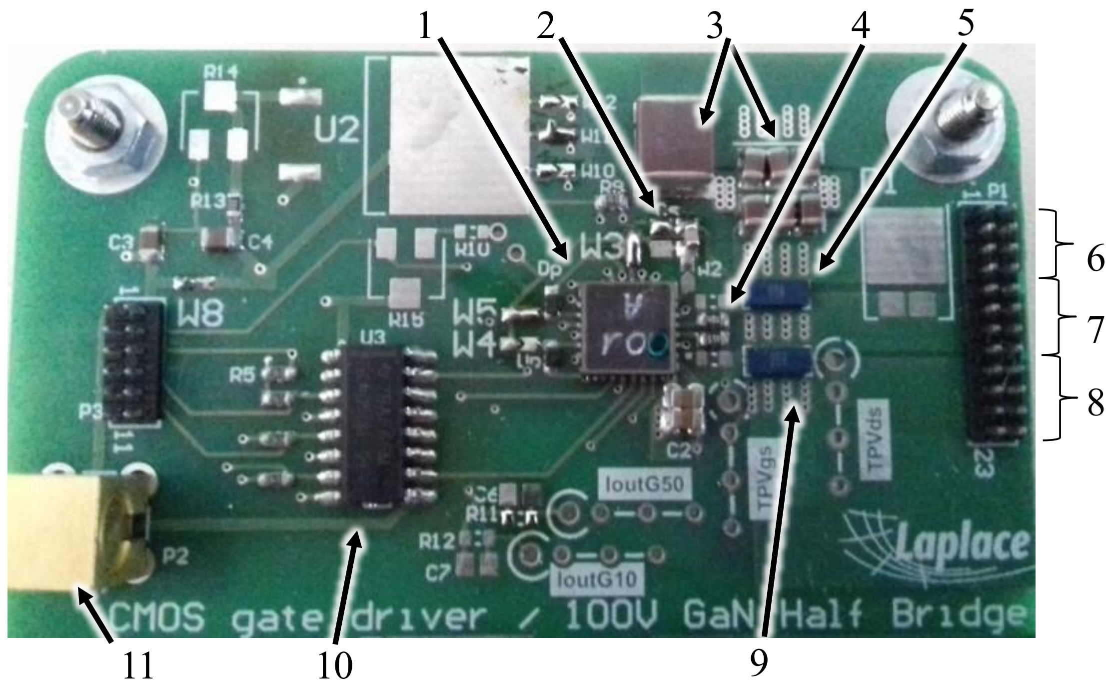
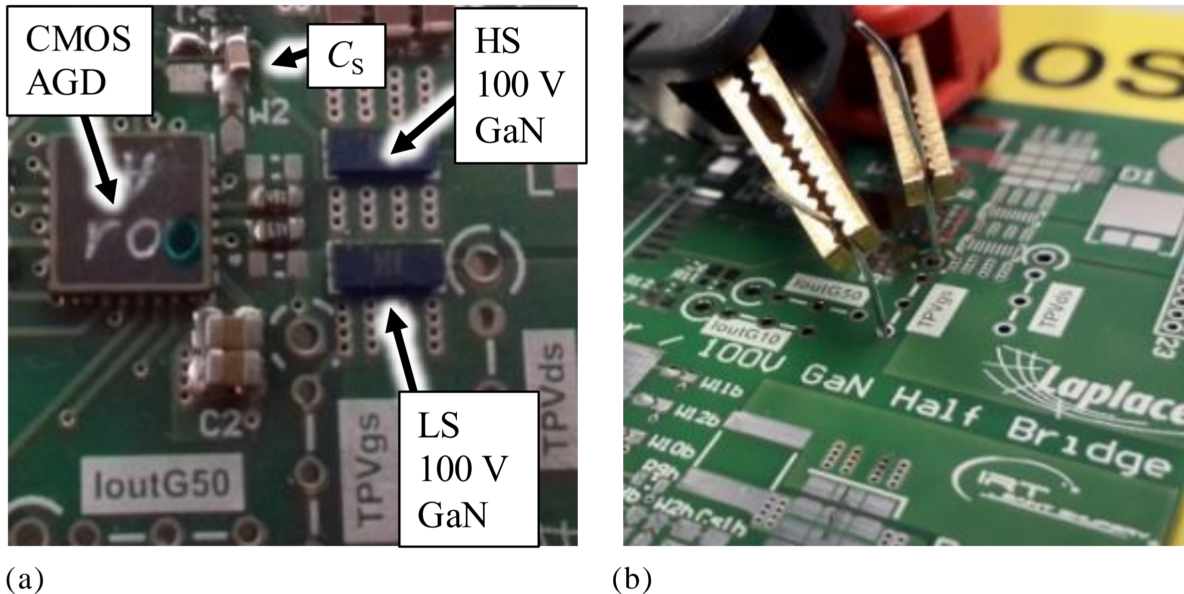


Figure 3.29: 4-metal layers PCB for 48 V application measuring 80 mm × 50 mm. 1: Designed AGD for GaN packaged in QFN24 (6 mm × 6 mm); 2: high voltage external sensing capacitor; 3: decoupling capacitors 10 µF+6×1 µF; 4: R_{Gon} and R_{Goff}; 5: High side GaN EPC2001C; 6: v_{hvDC} ;7: switching node called v_{DS}; 8: GND; 9: low side GaN; 10: protection buffers CD4050; 11: v_{PWM}

Figure 3.30 (a) shows a zoom of the AGD connection to the power device GaN EPC2001C. **Figure 3.30** (b) shows how the impedance analyzer HIOKI IM3570 is connected to the PCB to measure parasitic capacitance values that can affect switching speed. The measured values are $C_{GSmes} \approx C_{GDmes} \approx 3.4$ pF at 1 MHz. The impedance analyzer also plots the value of capacitance and it is verified that for a wide range of frequencies (1kHz to 5MHz) the measured values are the same. This value of 3.4 pF is in fact two capacitances in parallel. The capacitance between two points excluding the equivalent circuit is half of this value and therefore $C_{GS} \approx C_{GSmes}/2 = 1.7$ pF. The same for $C_{DS} \approx C_{DSmes}/2 = 1.7$ pF.



(a) (b)

Figure 3.30: (a) Detail to the gate drive and power loops. (b) Measuring parasitic capacitance between gate and source and gate and drain tracks using the impedance analyzer Hioki IM3570. $C_{GSmes} \approx C_{GDmes} \approx 3.4$ pF at 1 MHz.

Using the fabricated CMOS AGD with the integrated buffer, **Figure 3.31** shows experimental waveforms obtained during the turn-on with and without the closed-loop control, with the same gate resistor and driving voltages for the same test parameters as previously described in **Table 3.10**. For the closed-loop, a pre-biasing current of 20 µA was applied at the input of the current mirror (v_{inM} node) using a SMU (source measure unit) Keithley 2612B. Without the closed-loop control, the fall time is 4.36 ns (90%-10% $v_{DS}(t)$), with peak dv/dt of -15 V/ns. Even with this fast switching event, the AGD is able to actively control the dv/dt sequence from the beginning, without modifying the di/dt. It is possible to see the di/dt sequence in the v_{GS} signals because it is the interval between v_{TH} (around 1.7 V from the datasheet) and the beginning of the dv/dt phase, the second line marked in **Figure 3.31**. However, the $v_{GS}(t)$ signal with and without the closed-loop control clearly shows that the di/dt sequence remains almost identical in both cases (**Figure 3.31** and **Figure 3.32** marked as di/dt sequence). One can also note that the reduced dv/dt with the closed-loop feedback allows the reduction in the drain current overshoot and subsequent gate overvoltage before the Miller's plateau. Due to the AGD, the fall time is increased from 4.36 ns to 7.37 ns (90%-10% v_{DS}) without affecting the gate charge before the Miller's plateau. This increase in fall time corresponds to the reduction in peak dv_{DS}/dt from -15 V/ns to -6.3 V/ns as shown in **Figure 3.1**. One must note that all the analog circuits are integrated within the CMOS AGD; only the driver supply decoupling capacitors, HV-sensing capacitor (for some tests) and gate

resistors are external devices. It should also be emphasized that due to the high speed and large gain of the integrated current mirrors, the HV-sensing capacitor C_S is designed in the pF range, allowing its further integration within the CMOS chip (please see **Table 3.10** for values).

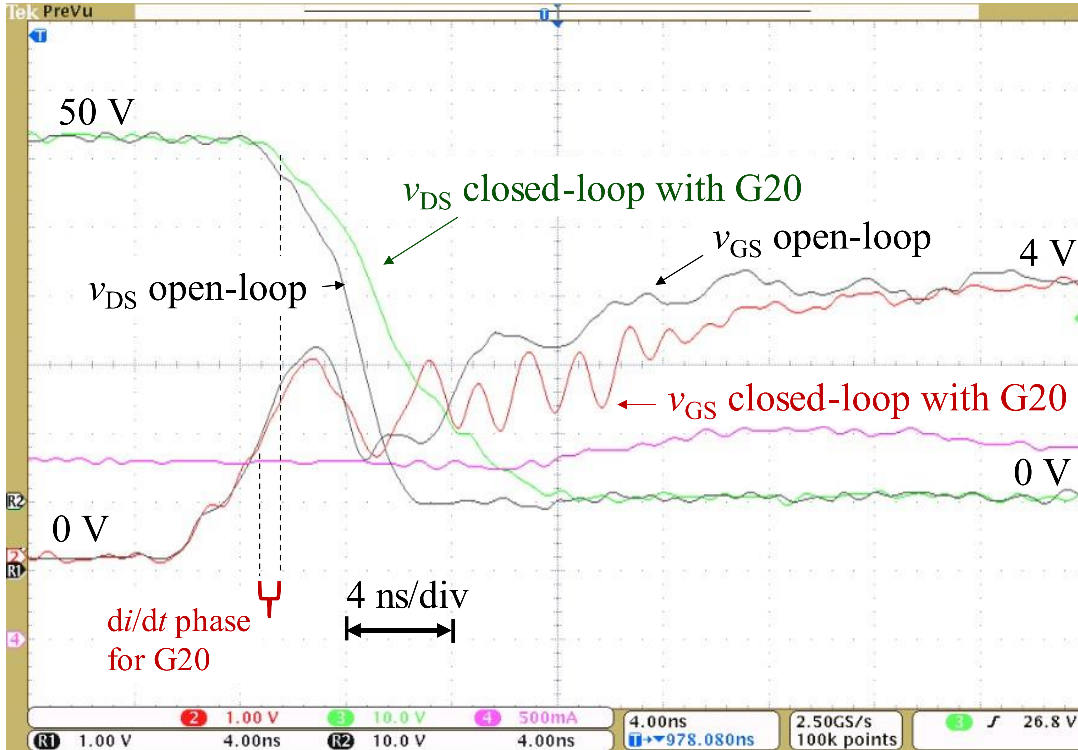


Figure 3.31: Measured signals for v_{DS} and v_{GS} with and without the proposed method to control dv/dt. Gain 20 and i_{bias} = 4 µA. Published also in [69], from the same author of this manuscript.

Figure 3.32 shows the measured v_{GS} waveforms in open-loop and in closed-loop with gains of 10 and 50 for the same value of sensing capacitor C_S = 2pF (external). The duration of the Miller's plateau is successfully increased with higher feedback gain values ("effect 1" in **Figure 3.32**). It is also clear that the di_D/dt phase is not affected by the closed-loop control. The di/dt value is estimated to be approximately 1A/ns, since the v_{GS} signal changes from v_{TH} to v_M in approximately 1 ns. Please note that measurements are carried out with i_L=2 A to obtain higher values of dv/dt to explore the speed limits of the method. In addition to the reduction of the dv_{DS}/dt with higher closed-loop gains, the drain overcurrent during turn-on is also reduced. This effect can be seen in **Figure 3.32** ("effect 2") where $i_D(t)$ and $v_{GS}(t)$ are linked by the transconductance of the GaN transistor in this operating state. Reducing the drain overcurrent and gate overvoltage before the Miller's plateau is a clear proof of the ultrafast closed-loop control. Due to the AGD, the classical design trade-offs in operating conditions and reliability issues are clearly pushed forward.

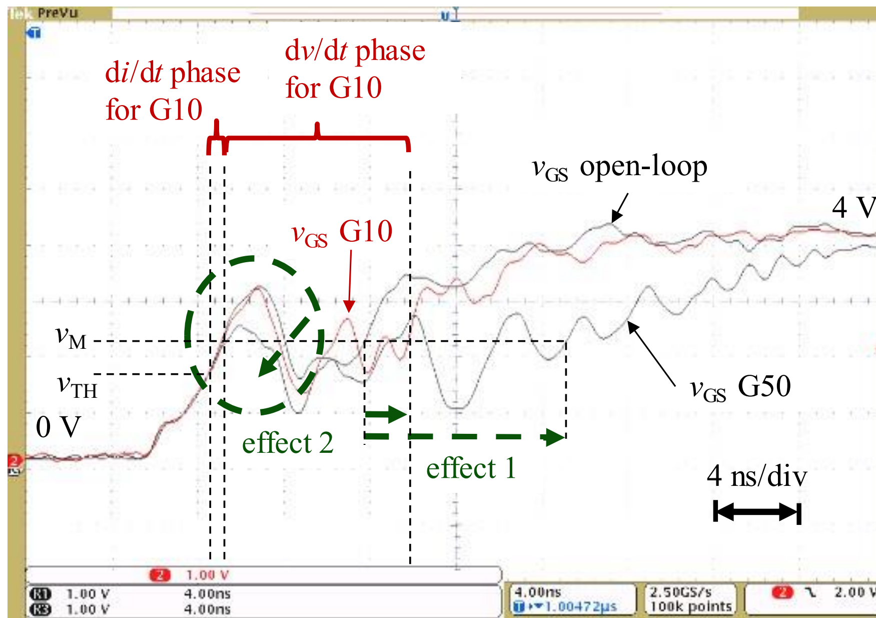


Figure 3.32: Measured v_{GS}(t) for open-loop (without the proposed method) and closed-loop controls with mirror gains equal to 10 and 50.

To compare the implementation of the AGD with a gain of 50, **Figure 3.33** shows a comparison between the experimental results and simulated waveforms. Increasing the feedback gain of the current mirrors decreases dv_{DS}/dt while maintaining an identical di/dt.

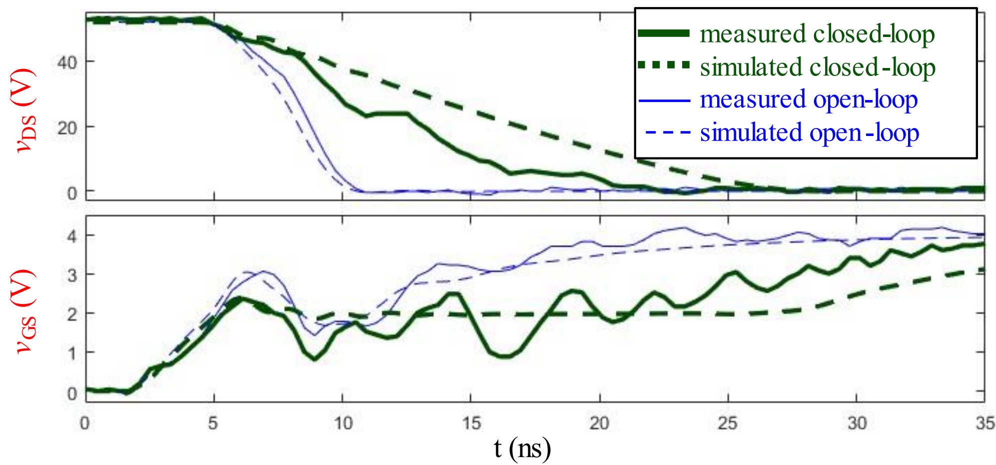


Figure 3.33: Measured and simulated waveforms v_{DS}(t) and v_{GS}(t) for open-loop and closed-loop controls using a current mirror with gain of G = 50. A pre-biasing current of 150 µA is used in this measurement. Cs = 1 pF.

It is possible to see that with a high value of gain G, the switching transient might become instable and the waveform can become oscillatory as can be seen in **Figure 3.33**. It can be explained because a high current being sunk from the gate

node during a turn-on event might contribute to discharge the gate and make the power device turn-off. If i_{FB} current is too high either because C_S or G are too high, an oscillatory behavior can be observed. The oscillations are more prohibitive in experimental results then in simulation probably because of non-simulated parasitic elements and other non-idealities.

In a similar way as in **Figure 3.33**, for a lower value of gain G = 10, **Figure 3.34** demonstrates a similar comparison between measured and simulated waveforms. Notice that the derivative of v_{DS} changes less because the Miller's plateau is less affected by a lower i_{FB} current.

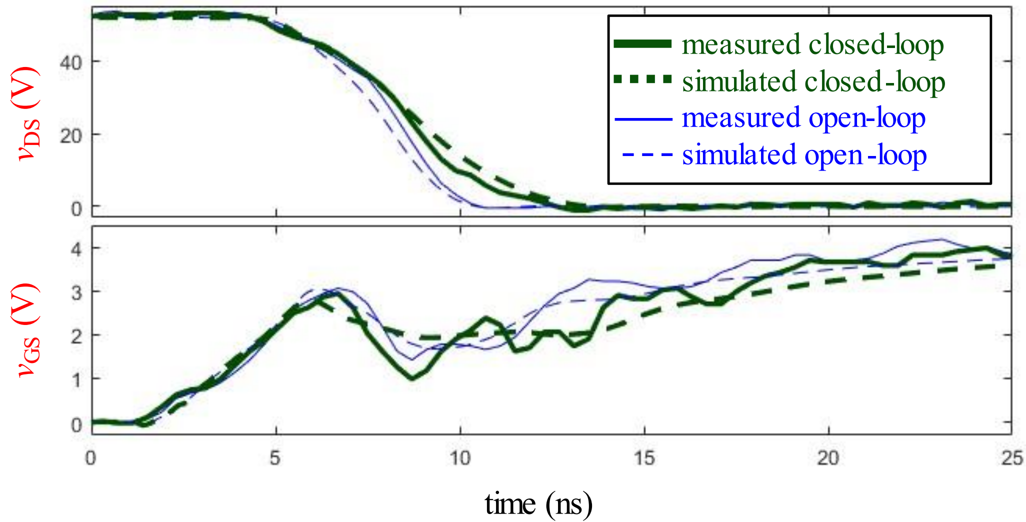


Figure 3.34: Measured and simulated waveforms $v_{DS}(t)$ and $v_{GS}(t)$ for open-loop and closed-loop controls using a current mirror with gain of G=10.

Peak value of dv/dt is calculated from experimental data calculating the difference between two consecutive points of acquired data from oscilloscope. **Figure 3.35** shows the data processed in this way. Notice that the instantaneous derivative value should be directly proportional to the current in the sensing capacitor C_S. For a capacitor C_S = 1 pF, 10 V/ns correspond to 10 mA of current.

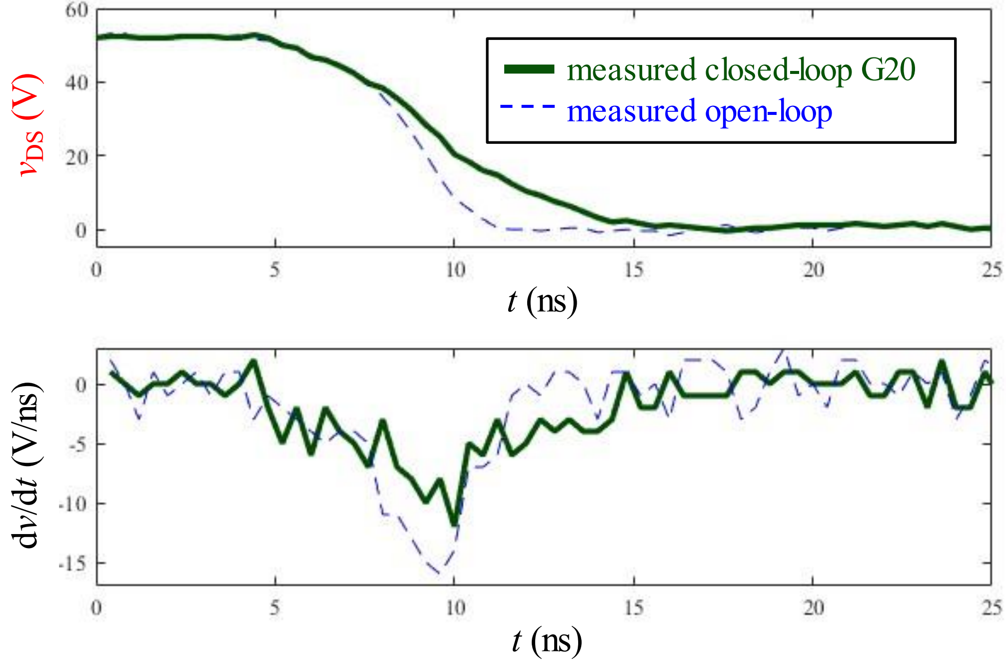


Figure 3.35: Measured waveform $v_{DS}(t)$ and its derivative calculated from 2 consecutive data points from the acquired data from oscilloscope.

The experimental data for $v_{DS}(t)$ for the turn-on, turn-off, ON and OFF-states measured with the double pulse method are merged into a periodic signal, with a 1 MHz switching frequency and a duty cycle of 0.5. In other words, the data processing consisted in simply erasing the 50000 data points between turn-on and off transients to bring those dv/dt phases closer. Those points correspond to the time when the signal v_{DS} is around 0 V during the double pulse. The Fourier transform of such a $v_{DS}(t)$ signal is shown in **Figure 3.36** for both the open-loop and closed-loop controls. An analytical expression for the expected attenuation $K_{dB(G20)}$ at high frequency is provided by (3.5). Consequently, for the reduction in the peak dv/dt during turn-on with the closed-loop control, the v_{DS} spectrum is reduced at high frequency, e.g., 13 dBµV lower at 100 MHz (**Figure 3.36**). This is a clear advantage of the AGD for reducing the high-frequency voltage content of the switching nodes with fewer switching losses compared to a classical adjustment of the gate resistor. The theoretical reduction in spectrum content is expressed by (3.5).

$$K_{\mathrm{dB(G20)}} = 40 \cdot \log \left(\frac{\mathrm{d}v \backslash \mathrm{d}t|_{\mathrm{G20}}}{\mathrm{d}v \backslash \mathrm{d}t|_{\mathrm{OL}}}\right) \tag{3.5}$$

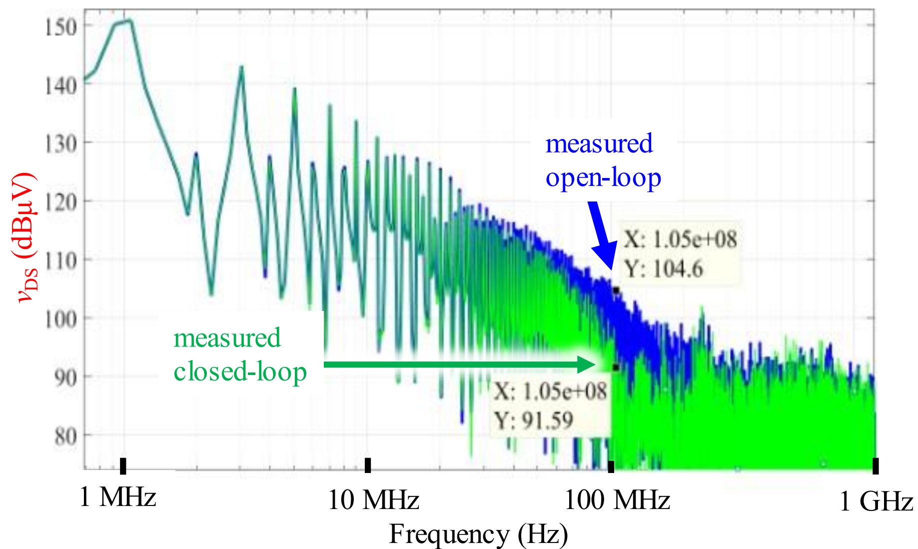


Figure 3.36: v_{DS} spectrum with open and closed-loop during turn-on calculated from data measured for the EPC transistor with all the parameters in **Table 3.10**.

3.6.2 400V Application

For a 400 V application, 650 V GaN should be used. The same chip presented in section **3.3** will now be tested in a double pulse setup for this higher value of bus voltage v_{hvDC}. Similarly, as for the 48V application, a PCB is made taking into consideration the parasitic inductance value of both control and power loops of a switching arm. The PCB has 6 layers and the dielectric thickness is 123 µm between metal layers 1 and 2 to reduce the inductance of the power loop. The upper device is connected in diode mode with gate and source short circuited to have to simulate the effect of a switching leg with the same transistor. Measured values of parasitic capacitance are the following: $C_{GS} \approx C_{GD} \approx 3.6$ pF at 1 MHz and once again verified the value for the full range of the impedance analyzer from 1 kHz to 5 MHz. It has more capacitance compared to the previous board because since it has 6 layers, the distance between two metal layers is smaller. **Figure 3.38** (a) is the PCB assembled for GaN GS66508T power device and (b) is a zoom to the AGD and GaN connection.

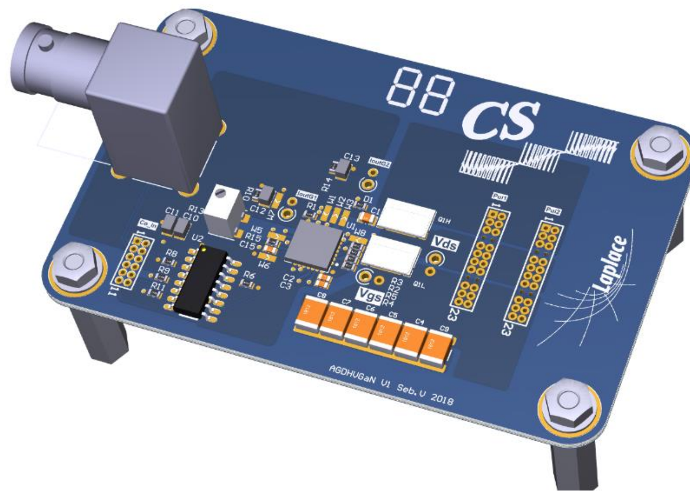
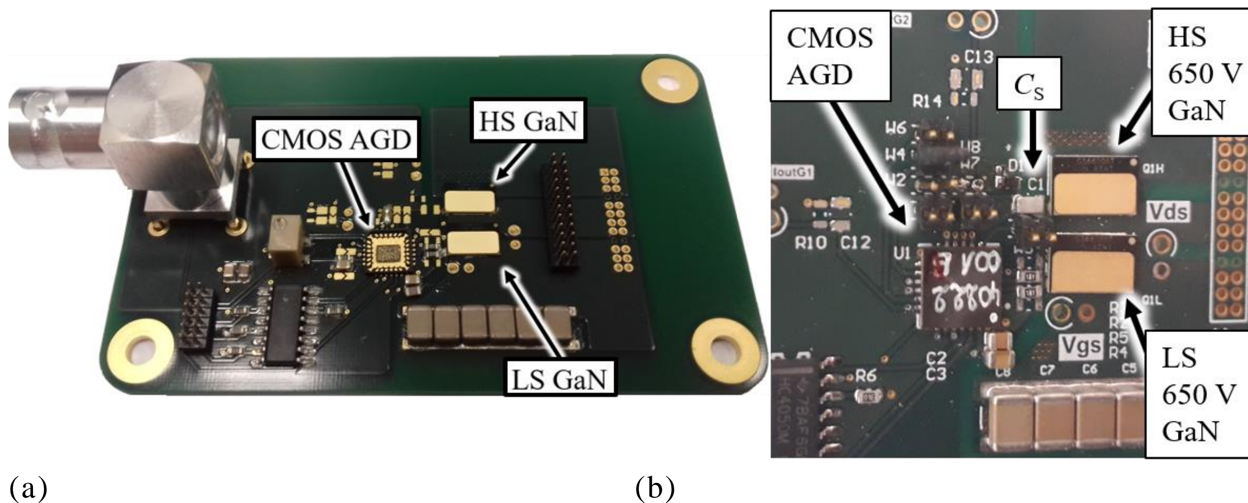


Figure 3.37: 3D representation in Altium Design™ of the PCB for 400V application.



(a) (b)

Figure 3.38: 6-metal layers PCB for 400V application showing (a) AGD with open hood. (b) Zoom to the AGD and GaN. The PCB dimensions are 80 mm × 50 mm.

Figure 3.39 shows the implementation of the AGD with a GaN System transistor GS66508T for gain G = 10 and C_S = 1 pF. The fall-time during turn-on (v_{DS}, 90% to 10%) is increased from 3.3 ns (open-loop) to 8 ns (closed-loop). The peak dv/dt value of -175 V/ns is therefore reduced to -120 V/ns with our CMOS AGD. A biasing current of 320 µA is applied, and one can observe that dv/dt starts to be attenuated in less than 1 ns. All the parameters for the results are described in **Table 3.10**. Without an integrated analog feedback loop, such a result would not be possible. This experimental result shows, for the first time, the active control of 650 V GaN devices with extremely high switching speeds, both in open- and closed-loops. **Figure 3.40** shows a similar result, where the high-voltage capacitor is

integrated on the same CMOS chip as the GD (1 pF, 3.5 kV breakdown, see section **2.3**). The small differences in switching speeds between **Figure 3.39** and **Figure 3.40** can be explained by the use of a different PCB board, albeit from the same design (typical dispersion in power devices, CMOS GD and PCB parasitics). Nonetheless, this result clearly shows that the AGD can be fully functional, even with the high-voltage sense capacitor C_S monolithically integrated within the CMOS AGD.

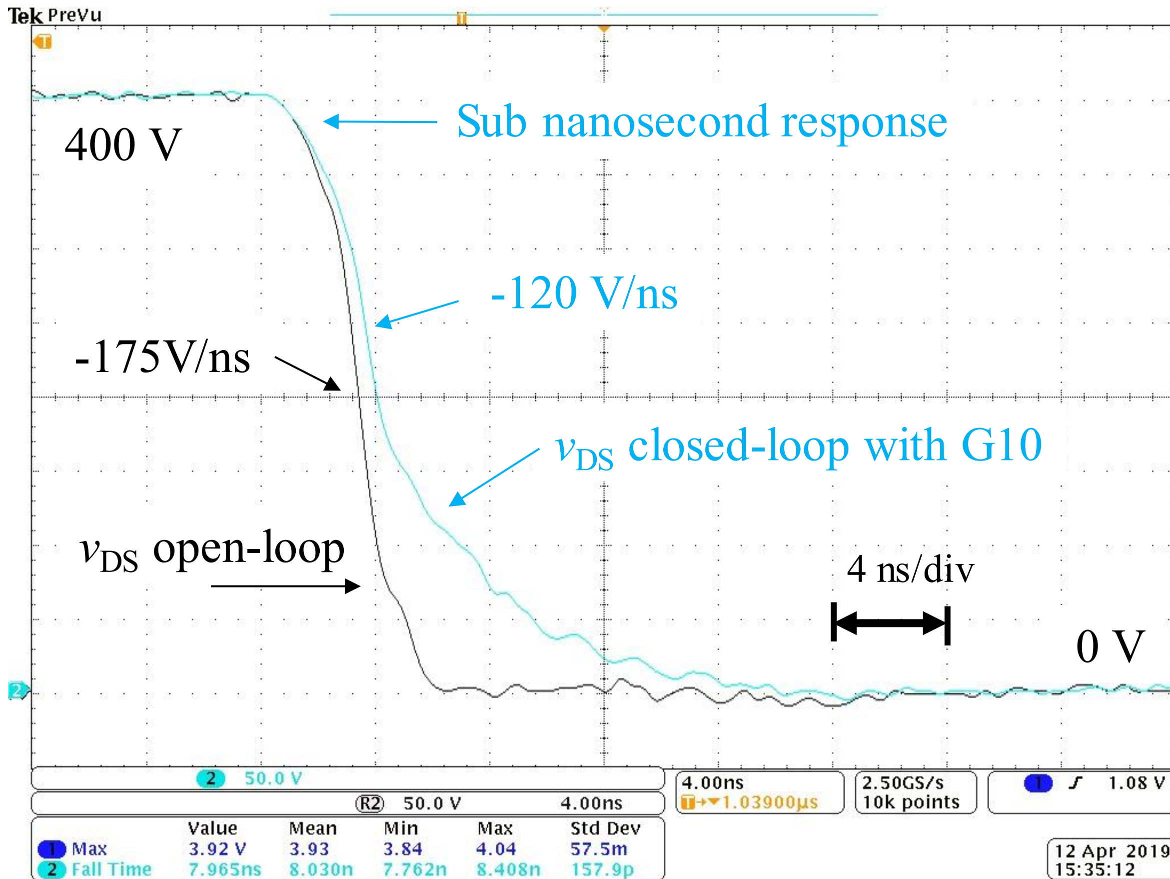


Figure 3.39: Measured v_{DS}(t) waveforms for open-loop (without the proposed method) and closed-loop (with the proposed method) controls for 650 V GS66508T GaN transistors. i_{bias}=320 µA.

Please note that the effect of a biasing current improving the feedback response time can be seen comparing **Figure 3.39** (i_{bias} = 320 µA) and **Figure 3.40** without biasing current. The attenuation in dv/dt occurs latter in **Figure 3.40** when compared to **Figure 3.39**, as predicted and discussed before. All the other parameters are the same for both figures.

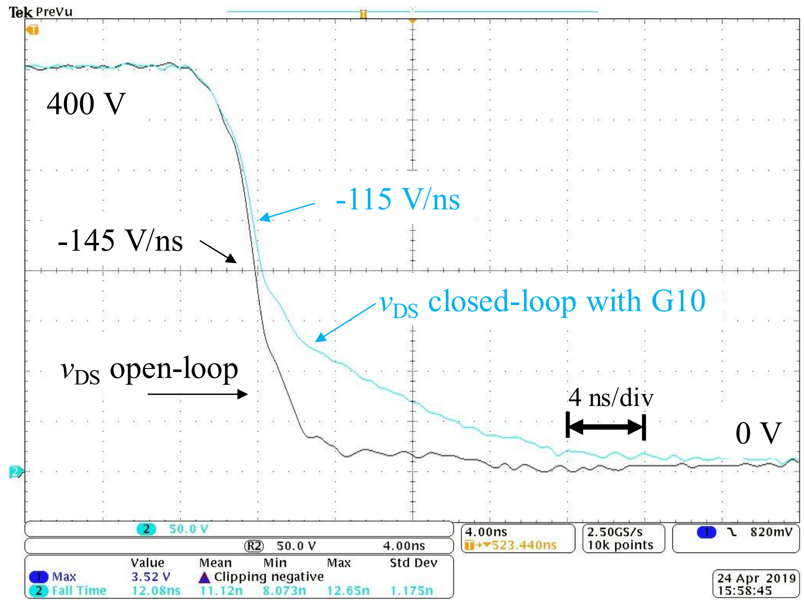


Figure 3.40: Measured $v_{DS}(t)$ waveforms with an embedded sensing capacitor C_S and without an i_{bias} current for this measurement.

Since the tests for the GaN in 48V application had R_G value of 4.4 Ω, some experiments are also conducted with this value of R_G for the 400V application for comparison analysis. The acquired data is shown in **Figure 3.41**. Notice that the value of gain 20 with C_S = 2 pF makes the switching event critically stable. The feedback current is higher than the current being provided by the main stage buffer and power device tends to turn-off during a turn-on event, resulting in this oscillatory behavior.

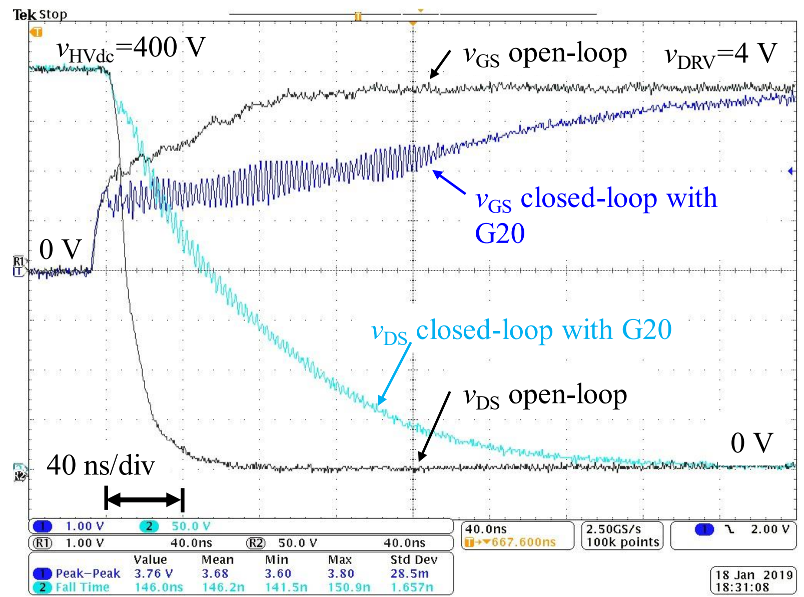


Figure 3.41: Experimental results with the CMOS AGD in the 400V DC bus voltage. With the closed-loop, the dv/dt is attenuated from -45 V/ns to -6.6 V/ns. R_G = 4.4 Ω.

In a similar way as for the 48 V application, the data from experimental results is processed to calculate the frequency spectrum of v_{DS} signal. The data processed into a periodic signal and the FFT calculated and demonstrated in **Figure 3.42**. For this 400 V application, the reduction is 7.6 dBμV at 100 MHz. This data corresponds to experimental results shown in **Figure 3.39**, where is observed a reduction in dv/dt from 175 V/ns to 120 V/ns. Equation (3.5) also applies.

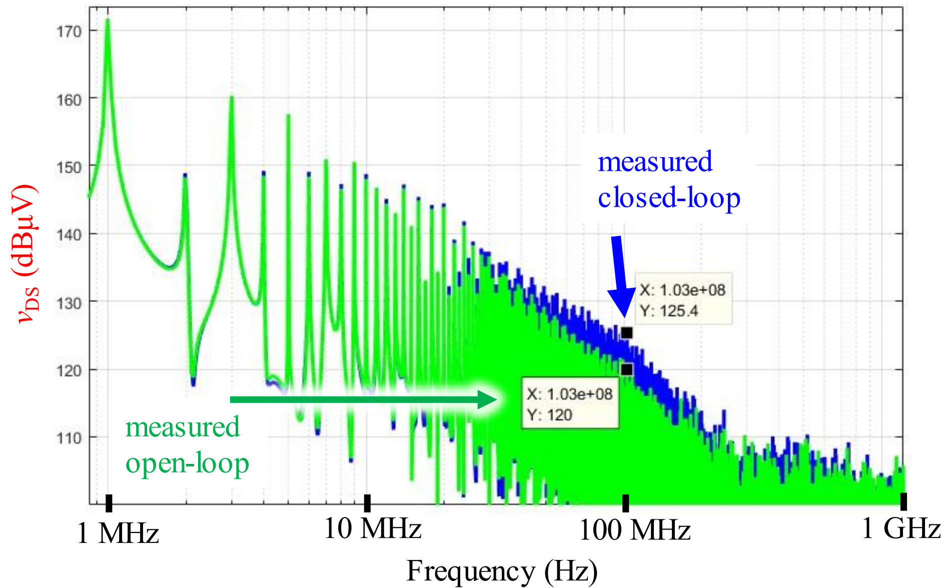
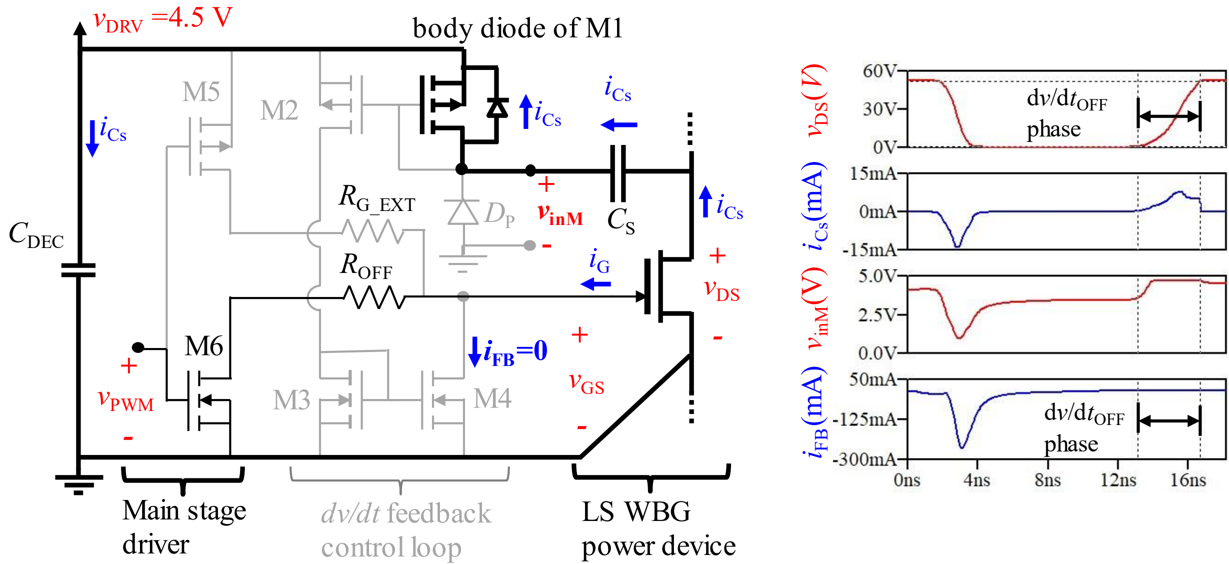


Figure 3.42: v_{DS} spectrum with open and closed-loop during turn-on calculated from data measured for the GaN Systems 650 V transistor with all the parameters in **Table 3.10**.

3.6.3 The turn-off behavior of the turn-on feedback loop

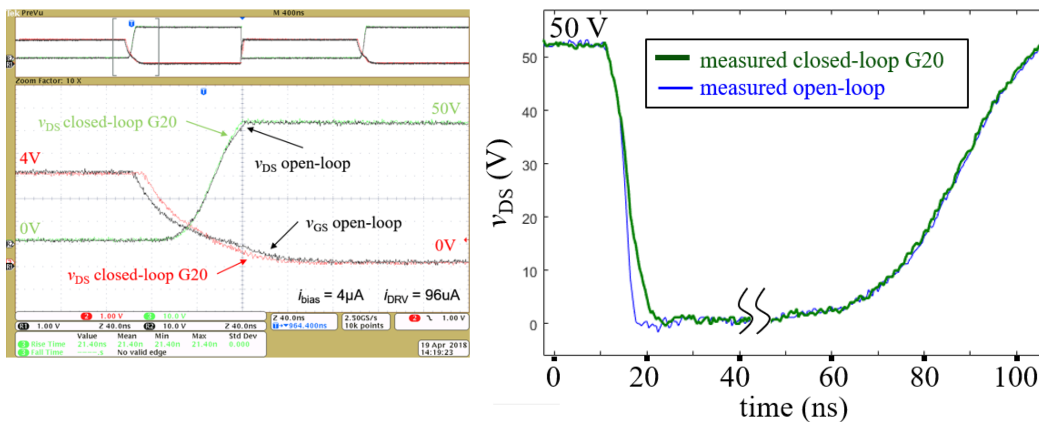
The proposed topology to control dv/dt should not affect the turn-off behavior. In order to control both, turn-on and off events, a symmetrical circuit should be adapted [63]. In this work, a prototype is built to actively control only the turn-on. Therefore, it is important to demonstrate that the proposed method is not affecting the turn-off behavior. The discharge path of C_S during a turn-off event is shown in **Figure 3.43** below.



(a) (b)

Figure 3.43: Turn-off transient behavior explained. The discharge path of C_S is highlighted in the (a) schematic. (b) Simulation results showing that during the turn-off, the current i_{FB} will not be affected comparing to the turn-on transient, even if v_{inM} changes.

A current will flow through the body diode of M1 which will simply cause an increase in voltage in the node v_{inM} of only 0.7 V. This increase in voltage will not affect the output of the current mirror. Notice that D_P is a Zener diode that can also protect the node from an excessive increase in v_{inM} voltage in case v_{DRV} also increases. The experimental curve for this behavior is shown in **Figure 3.44** below. It is possible to see in **Figure 3.44 (a)** that the method affects the v_{GS} waveform but not v_{DS} during turn-off event.

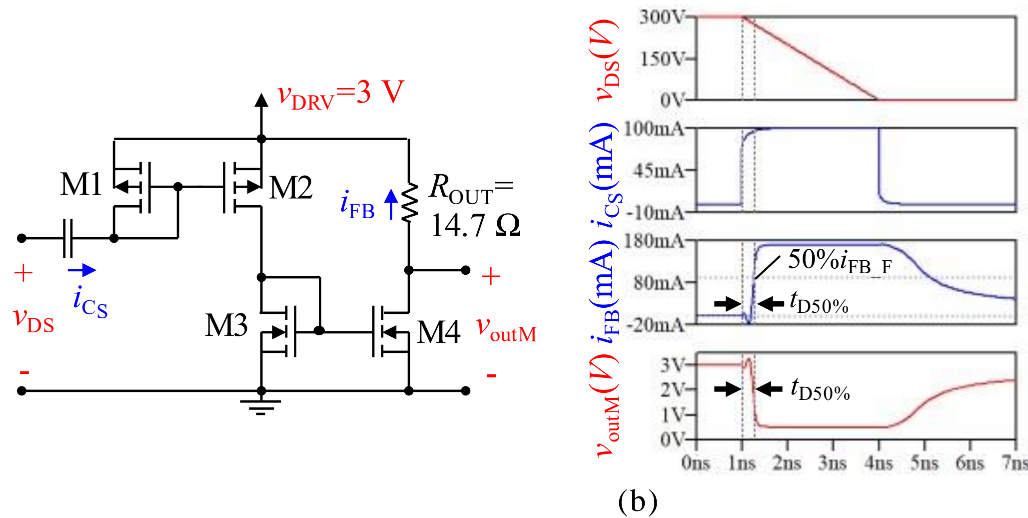


(a) (b)

Figure 3.44: Measured turn-off behavior. (a) Oscilloscope screen capture. (b) Measured data between turn-on and off are subtracted so both turn-on and off are visible close to each other for a better comparison.

3.6.4 Sub-nanosecond response demonstration (control loop measured response to a resistive load)

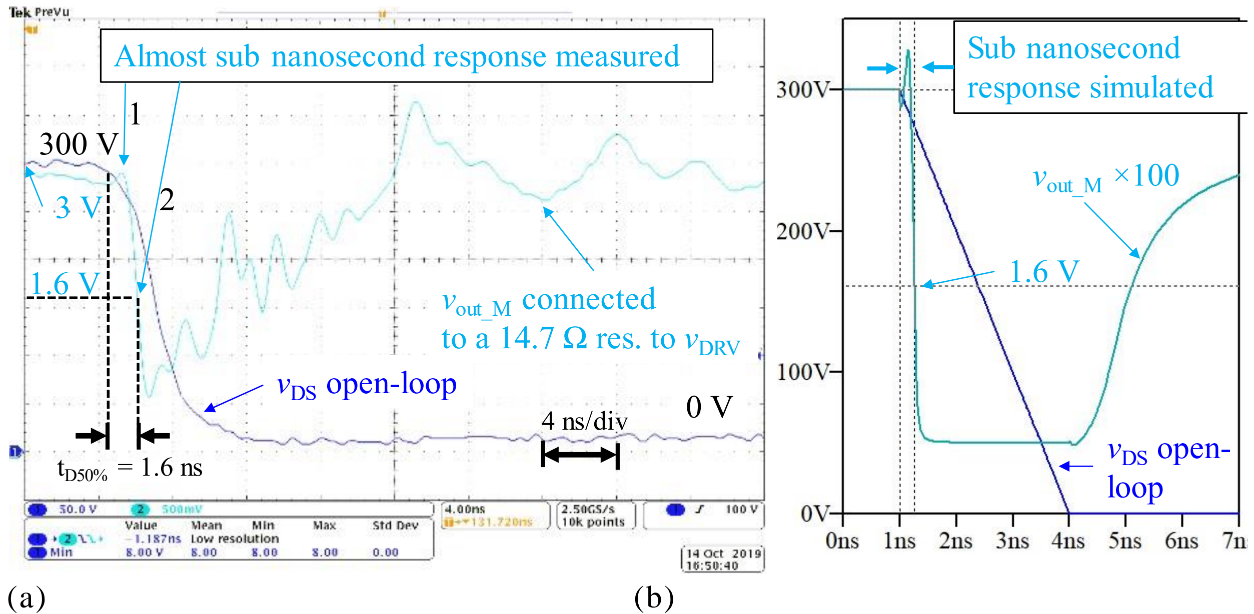
In order to experimentally measure a sub-nanosecond response of the control loop, we can connect the output of the current mirrors to a resistive load without the closed-loop system (**Figure 3.45** (a)) and measure the delay in the voltage signal using a simulation to actually measure a delay in current signals. Simulation values for the point where the current reaches 50% of its final value ($t_{D50\%}$) correspond to a point of 1.6 V for v_{outM} (see **Figure 3.45** (b)).



(a) (b)

Figure 3.45: The d*v*/d*t* feedback loop output is connected to a resistive load to measure the delay in the voltage signal (v_{DS} and v_{outM}) that correspond and correlate to the delay in the currents (i_{Cs} and i_{FB}). (a)Schematic and (b)simulation.

The value of R_{out} = 14.7 Ω is an impedance match with M5 (R_{DS_ON} on M5) to show the maximum excursion in v_{outM}. If the value of the resistance is lower, (e.g. 1 Ω) the signal will change less, only 0.3 V, 10% of v_{DRV}. If it is higher (e.g. 1 k Ω) M4 may work in its ohmic region. Measurements are made in 300 V instead of 400 V because of the limitation of probes P6139B 500 MHz are 300 V. To compare two signals, two probes P6139B are first calibrated. To verify this simple calibration procedure, an identical 300 V step signal is measured with both probes and they match in the screen with full zoom applied to time axis. Then, the measurement is performed and shown in **Figure 3.46**.



(a) (b)

Figure 3.46: Measured input and output voltage signal of the current mirror connected to a resistive load R_{OUT} = 14.7 Ω. Voltage signals correspond to the respective current signals. The (a) measure is compared to the (b) simulation with an ideally trapezoidal waveform to prove the system is responding in less than 1 ns. The current mirror is G10bias. No biasing current is applied to the input of the current mirror.

The last thing to verify is the time between points 1 and 2 in **Figure 3.46** (a). Point 1 (pointed by the arrow marked as 1) correspond to the first point in the oscilloscope under 298 V after a long series of points between 298 V and 306 V in the CSV data file. This point indicates the start of the d*v*/d*t* phase. Point 2 in **Figure 3.46** (a) is the closest point to 1.6 V of v_{outM}. In simulation of **Figure 3.45** (b) this point is reached when i_{FB} achieves 50% of its final value. In the oscilloscope capture, the time distance between these points 1 and 2 corresponds to precisely 4 points of data with a step of 0.4 ns between each point. Consequently, it is 1.6 ns observed experimentally. Notice that the feedback loop was already sinking current before 1.6 ns to raise the current to 50% of its final value in this point.

The measured delay between the voltage signals is around 1.6 ns, compared to 260 ps in simulation. Simulation are made with LTspice™ with intrinsic capacitances added in the model (values of perimeter and area of each transistor are included). However parasitic values of the PCB are not included in the simulation. The oscilloscope probe capacitance is also not taken into consideration into the simulation.

3.7 Chapter conclusion

This chapter focused in three subjects:

1 - Adaptation of the AGD firstly created for GaN devices into a high performance AGD for SiC technology. This adaptation takes into consideration the optimization studies from chapter 2.

2 - Presentation of AGD layout and design choice for best performance of the AGD chip.

3 - Experimental results of AGD for GaN devices verifying the AGD design and the ultrafast feedback loop allowing us to significantly reduce d*v*/d*t* of GaN devices.

When adapting the method for SiC devices, it has been observed some simulation curves were generating a feedback current, but the main stage buffer was simply providing higher current, therefore the d*v*/d*t* was not changing. It has been observed that the operating point of transistor M5 (main stage buffer PMOS) is important in the feedback loop performance. For the feedback loop works properly, the buffer (transistor M5) should be sized accordingly to place saturation current (i_{Dsat}) close to the value of Miller's plateau current (i_{G_OL}).

Concerning subject 2, one of the big layout challenges is to find a good balance in the tradeoff between parasitic capacitance and series resistance. During routing, the more metal is used, the less series resistance the connections will have, but the higher the parasitic capacitance with the substrate which can degrade performance. For this reason, every time it is possible to route using the most top metal layer it is preferred.

Finally, some interesting results are experimentally demonstrated for GaN applications, up to the date this thesis is written, no closed-loop system was able to control a switching transient of a few nanoseconds in WBG power devices. Experimental results also show that increasing the gain *G* too much may lead to instability in the control loop. Another result also shows the turn-on control does not affect the turn-off behavior as expected.

General conclusion and perspectives

Contributions to closed-loop dv/dt control is given in this thesis because a good level of controllability is experimentally demonstrated for high values of dv/dt. A method to control dv/dt independently from di/dt using high voltage on-chip capacitors is presented. The objective is improving the tradeoff between switching energy and switching speed (dv/dt). A challenge in this work is to use low voltage CMOS technology in 5V for GaN and 40V transistors for SiC transistors to achieve waveform controllability for higher voltages WBG power devices in higher voltage applications. For example, for aeronautical applications, high efficiency power converters are being designed to work with each time higher levels of DC voltage.

In chapter 1, applications in power electronics for AGDs have been briefly commented. One brief overview of the switching waveform analysis is performed. It has been presented the methods to control the dv/dt, the state-of-the-art of AGDs. In the end of chapter 1, a method to control dv/dt independently from the di/dt is presented to be more detailed in the next chapters.

In chapter 2 surface and bandwidth are optimized for different values of gain G and C_S and in each of the two stages of the current mirrors G_P and G_N. A major conclusion in this study is that choosing a higher value for the capacitor C_S for a same given attenuation in dv/dt and therefore the gain G is lowered to compensate, will consumes more surface but the bandwidth increases. It has also been observed a minimum theoretical value of surface. For small values of sensing capacitor C_S a minimum value is achieved. Another important conclusion is the link between the dynamic performance of the feedback loop and the transition frequency of a given technology. Equations relating the transition frequency is established as a function of the sensing capacitor C_S for a constant product between the variables $G \cdot C_S$. The study clearly indicates the bandwidth obtained with a 0.18µm CMOS technology is enough to the required performances to control a modern wide band-gap transistor GaN or SiC.

In chapter 3 the design procedure and main specifications are more detailed, a performance parameter has been defined and discussed. In this third chapter also, it has been experimentally demonstrated a controllability of the dv/dt from 175V/ns to 120V/ns. The layout images and simulations are presented for another AGD developed for SiC applications.

Perspectives

Using the methodology presented in this thesis regarding CMOS design, many other ideas could be developed to explore possibilities to achieve high values of efficiency in switching cells. Regarding specifically the d*v*/d*t* in closed-loop architecture the following ideas could be applied in other projects:

- To speed up instead of slowing down v_{DS} transition. By injecting more current in the gate of the power device after the external gate resistance, a switching waveform could speed up to decrease the switching losses.
- To apply the method to also control the turn-off. A symmetrical topology could be easily adapted to control the d*v*/d*t* during the turn-off for high values of load current.
- To apply the method to control the d*i*/d*t* sequences with a similar circuit topology, such as current mirrors to control the d*i*/d*t* as well.
- To study other topologies to have a continuously variable gain. By applying different values of voltages and currents using analog design techniques the non-linearities of the Miller capacitance C_{rss} could be compensate for a more optimal switching waveform.
- To add another loop to control the value of gain automatically. By combining different feedback loops of different values of gain, an enable signal could be used to enable more or less value of gain electronically. By adding another feedback loop this could be done automatically.
- Instead of sinking a current after the external gate resistance another idea that provides more stability is to provide less current by the transistor M5 during the d*v*/d*t* phase. In this case only a sensing capacitor can be placed from the drain of the power device to the gate of M5, if it is correctly sized it will limit the d*v*/d*t* to a certain value.

More generally, the application of this active gate driving must be investigated with SiC MOSFETs, in a close relationship with power module and integrated power module packaging techniques. This work offers new perspectives for a better trade-off in switching losses and electromagnetic perturbation sources.

Abbreviations

AC	Alternating Current
ADC	Analog-to-Digital Converter
AGD	Active Gate Driver
BJT	Bipolar Junction Transistor
CGD	Conventional Gate Driver
CM	Common-Mode
CMOS	Complementary Metal Oxide Semiconductor
D	Diode
DAC	Digital-to-Analog Converter
DC	Direct Current
DM	Differential-Mode
DRC	Design Rules Check
FB	Feedback
GaN	Gallium Nitride
GD	Gate Driver
HEMT	High Electron Mobility Transistor
HS	High Side Power Transistor
LS	Low Side Power Transistor
LVS	Layout Versus Schematic
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
NMOS	N-type Metal-Oxide Semiconductor
PMOS	P-type Metal-Oxide Semiconductor
SMD	Surface Mount Device
Si	Silicon
SiC	Silicon Carbide
SiO_2	Silicon Dioxide
SMU	Source Measure Unit
SOA	Safe Operation Area

Variables

C_S	Sensing Capacitor
BV	Breakdown voltage of a dielectric
C_{DS}	Drain-to-source capacitance
C_{GD}	Gate-to-drain capacitance
C_{GS}	Gate-to-source capacitance
C_{iss}	Input capacitance
C_{oss}	Output capacitance
C_{PAR}	Parasitic capacitance
C_{rss}	Reverse transfer capacitance
f_c	Cut-off frequency
i_{Cs}	Sensing capacitor current
i_{FB}	Feedback loop output current
i_G	Gate current
i_{Rg}	Current in the gate resistor R_g
S	Surface (or Area) of the CMOS circuits
$t_{D1\%}$	Settling time to achieve 1% of final value of current i_{FB}
$t_{D50\%}$	Settling time to achieve 50% of final value of current i_{FB}
v_{DS}	Drain-source voltage
v_{GS}	Gate-to-source voltage
v_{GSn}	Gate-to-source voltage of the NMOS' transistors
v_{GSp}	Gate-to-source voltage of the PMOS' transistors
v_{inM}	Voltage at the input of the PMOS current mirror

List of publications

Journal Papers

P. Bau, M. Cousineau, B. Cougo, F. Richardeau and N. Rouger, "CMOS Active Gate Driver for Closed-Loop dv/dt Control of GaN Transistors," in *IEEE Transactions on Power Electronics*, vol. 35, no. 12, pp. 13322-13332, Dec. 2020, doi: 10.1109/TPEL.2020.2995531.

Conference Papers

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Annex 1: Main academic teams publishing about AGD worldwide

The main research groups from academic institutes working with AGD worldwide can be seen in the **Figure 0.1** below.

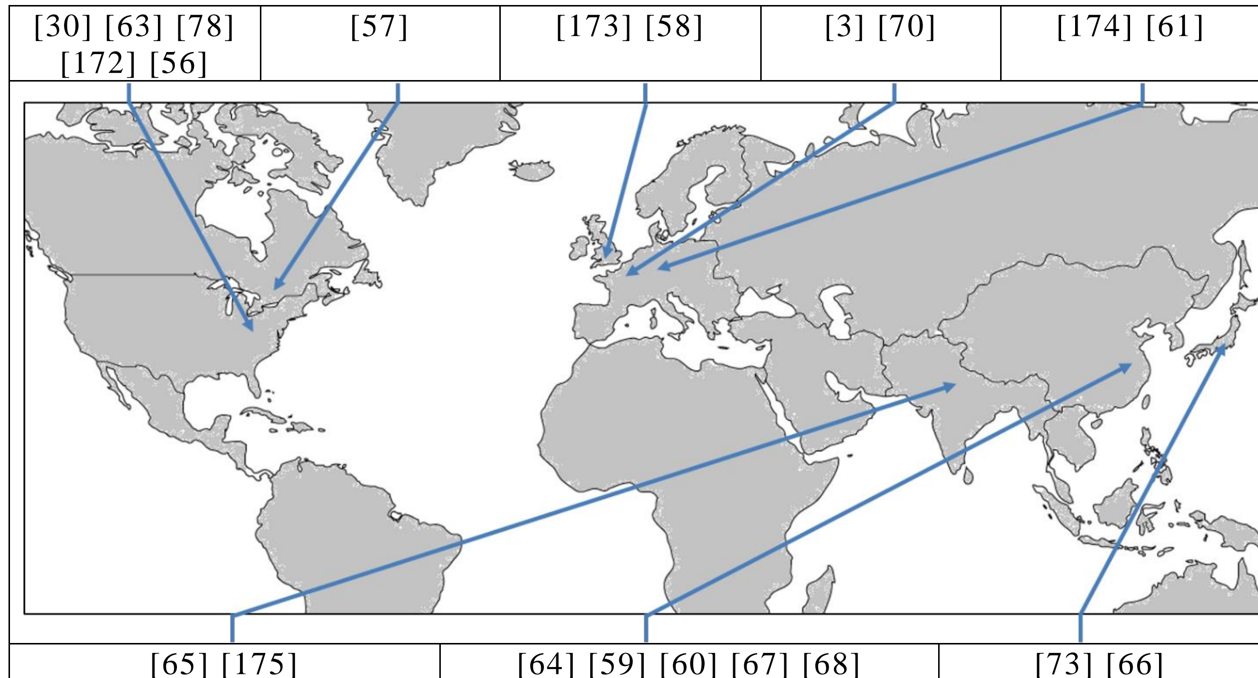

Figure 0.1. Some of the main academic groups working with AGD (Active Gate Drivers) worldwide. In ascending chronological order for each country pointed.

In Canada, the University of Toronto have been publishing many articles regarding power IC for WBG power devices. Many papers are from different places in the USA also, with a highlight to CPES a laboratory attached to Virginia Tech in the state of Virginia, dedicated to power electronic. In United Kingdom, the University of Bristol has also good papers regarding AGD. France and Germany have several other papers regarding AGD and power IC for WBG transistors. In recent years, after 2017, a big number of academic publications are from first authors from Asia, especially China.

Annex 2: Matlab™/Octave™ code for precise calculation of capacitances and bandwidth

To calculate precisely the capacitance seen in nodes of the PMOS' and NMOS' transistors, the code for Matlab™/Octave™ is demonstrated. The equation used to calculate the SL_1 (line 29 below) is (2.51). The slew rate 2, SR_2 in line 32 below is calculated with equation (2.58):

NDA data. Confidential values

```
delta   paisseur inter-couches metalliques pour capa Cs
delta   sseur couche du bas de la capa Cs avec substra
k=0.6   en régime saturé
CoxN=   capacité d'oxyde surfacique (F/m²) - 1fF/µm²=1mF/m²
CoxP=
CovN=   ité débordement de Grille sur Drain (F/m)
CjN=0   capacité de la jonction drain-source en inverse du bas (F/m)
CjP=0
CjSWn   pacité des murs de la jonction drain-source en inverse du bas
CjSWp
Lptot   e-6; Lp=Lptot-DeltaLp;
Lntot   5e-6; Ln= Lntot-DeltaLn;% (m) longueur de grille minimale, rés

Vth=0.5;
dvdt_OL=160e9;
GCs=10e-12;
Cs=0.1e-12:0.01e-12:10e-12; Cs2=1e-12*[0.1 0.215 0.464 1 2.15 4.64 10];
Gp=2;  G=GCs./Cs;  Gn=G./Gp;
Cin_parasite=1/2*delta_ox/deltap.*Cs;
W1=7*133e-6.*Cs./1e-12; W3=3*113.22e-6.*Cs./1e-12;
CgsN=CoxN.*W3.*k.*Ln;
CdsN=(CjN.*W3.*Ln)+2.*(W3.*CjSWn);
CgdN=CovN.*W3;
CdsP=(CjP.*W1.*Lp)+2.*(W1.*CjSWp);
Kexp=1; Kpw=1; %kexp1pF=1.0927

CmirP=(1+Gp).*(k.*CoxP.*W1.*Lp)+CdsP;
Cp=CmirP+Cin_parasite;
SR1=dvdt_OL.*(Cs./(Cs+Cp));

Cn=((1+Gn).*Gp.*CgsN)+(Gp.*CdsN)+(Gp.*CdsP)+Gp*Gn.*CgdN*(11);
SR2=(dvdt_OL.*Gp./Cn).*Kexp.*Cs.^Kpw;

SL1_10p_Cadence=1e9*[50.51 49.76 50.89 56.6 76.26 95.13 101.1];
SL2_10p_Cadence=1e9*[11.52 17.74 26.19 36.84 46.56 44.94 30.55];
%figure;
set(gcf,'color','white'); set(gca, 'FontName', 'Times New Roman','FontSize', 20);

loglog (Cs,SR1,'--','Color',[0,0,0],'LineWidth',2); set(gca, 'FontName', 'Times New Roma
loglog(Cs2,SL1_10p_Cadence,'x','Color',[1,0,0],'LineWidth',3); hold on;
loglog(Cs,SR2,'Color',[0,0,0],'LineWidth',2); hold on;
loglog(Cs2,SL2_10p_Cadence,'o','Color',[1,0,0],'LineWidth',3); hold on;

legend('SR1 Theory','SR1 Simulation','SR2 Theory','SR2 Simulation','Location','southeast
xlabel('Input Cs capacitor (pF)'); ylabel('SR (V/s)');
set (gca, "ygrid", "on");
grid minor on
axis ([0.7e-12 2e-12 0.7e10 1.3e11])
```

Regarding the feedback loop delay to achieve 50% of the final value of current, ($t_{D50\%}$) delay, the Matlab™/Octave™ code is demonstrated below. Notice that for this technology AMS0.18, the approximation coefficients a, and c (in equation (2.62)) are calculated as a=4.5 and c=4.5 and can be seen in line 30 below.

Please notice that the numerical values of the capacitance per surface unit are imported from the documents from the foundry that the authors signed a non-disclosure agreement. These confidential data is hidden in the code in this annexes.

NDA data. Confidential values

```
1  delta_                        sseur inter-couches metalliques pour capa Cs
2  deltap                        ur couche du bas de la capa Cs avec substra
3  k=0.55                        régime saturé
4  CoxN=2                        pacité d'oxyde surfacique (F/m²) - 1fF/µm²=1mF/m²
5  CoxP=3
6  CovN=0                        débordement de Grille sur Drain (F/m)
7  CjN=0.                        acité de la jonction drain-source en inverse du bas (F/m)
8  CjP=0.
9  CjSWn=                        té des murs de la jonction drain-source en inverse du ba
10 CjSWp=
11 Lptot=                          Lp=Lptot-DeltaLp;
12 Lntot=                        ; Ln= Lntot-DeltaLn;% (m) longueur de grille minimale, re
13
14 dvdt_OL=160e9; GCs=10e-12;
15 Cs=0.1e-12:0.01e-12:10e-12; Cs2=1e-12*[0.1 0.316 1 3.16 10];
16 Gp=2.4;  G=GCs./Cs;  Gn=G./Gp;
17 Cin_parasite=1/2*delta_ox/deltap.*Cs;
18 W1=1000e-6.*Cs./1e-12; W3=W1/2.4;
19 CgsN=CoxN.*W3.*k.*Ln; CdsN=(CjN.*W3.*Ln)+2.*(W3.*CjSWn); CgdN=CovN.*W3;
20 CdsP=(CjP.*W1.*Lp)+2.*(W1.*CjSWp); CgsP=k.*CoxP.*W1.*Lp;
21 Kexp=1; Kpw=1; %kexp1pF=1.0927
22
23 CmirP=(1+Gp).*CgsP+CdsP;
24 Cp=CmirP+Cin_parasite;
25 SR1=dvdt_OL.*(Cs./(Cs+Cp));
26 %SL1_10p_CadM=1e9*[54.36 54.46 54.75 54.93 54.96];%
27 Cn=((1+Gn).*Gp.*CgsN)+(Gp.*CdsN)+(Gp.*CdsP)+Gp*Gn.*CgdN*(2);%avn=0.9999993
28 SR2=(dvdt_OL.*Gp./Cn).*Kexp.*Cs.^Kpw;SL2_10p_CadM=1e9*[3.178 13.45 32.91 42.96 44.58];
29 td50_CadM=1e-12*[956.1 201.2 108.4 97.19 96.93];
30 te_t2=(4.5*0.525./SR1+4.5*0.445./SR2);
31 %figure; set(gcf,'color','white');
32 loglog(Cs,te_t2,'Color',[0,0,0],'LineWidth',2); hold on;
33 set(gca, 'FontName', 'Times New Roman','FontSize', 18);
34 loglog(Cs2,td50_CadM,'x','Color',[1,0,0],'LineWidth',3); hold on;
35
36 legend('te-t2 Theory','te-t2 Simulation','Location','northeast')
37 xlabel('Input Cs capacitor (pF)'); ylabel('t_{50%} = te-t2 (ps)');
38 set (gca, "ygrid", "on");
39 grid minor on
40 axis ([0.7e-12 2e-12 3e-10 4e-10])
```

Annex 3: Translating Spice Simulations File (.lib) into CADENCE™ (.scs)

To be able to simulate the behavior of the AGD, one environment of simulation is required. In microelectronic one very consolidated software in industry is CADENCE™ Virtuoso SPECTRE™. For power electronics applications, the manufacturer provides files in format .lib that can be used in LTSpice™ for example. To have one simulation environment with AGD and a power transistor device, either the microelectronic models must be imported in LTSpice™ or the power device model (.lib) file must be translated to other format (.scs) to be used in CADENCE™. In order to convert the files provided by the manufacturer WolfspeedCree™ website to CADENCE™, some procedures are required. First the schematic of one netlist file .lib is drawn and can be seen in **Figure 0.1** below.

After the netlist file is drawn, some adjustments from a Spice file to a CADENCE™ Spectrum™ environment is necessary to translate the file. All the necessary adaptions required to translate from FileName.lib to FileName.scs are listed below:

1. Translating syntax. See **Table A** for examples.
2. Add first line: “simulator lang=spectre”.
3. subcircuits (subckt) put inside the main part of the file to not declare more than 1 subcircuit in the same file to make unique node names for better understanding of the code. The author doesn’t know if a CADENCE™ file can have subcircuits declared and how to do so. The proposed solution doesn’t declare more than one subcircuit in the file and worked fine.
4. The subcircuit name must match the file name.
5. When placed outside a subcircuit, some elements must change name to avoid conflict with the name inside the subcircuits (Rg to Rg1 and Rd to Rd1).
6. Creation of one IF function to replace the function limit.
7. Replace another limit function with (max value) as a parameter of a current source.

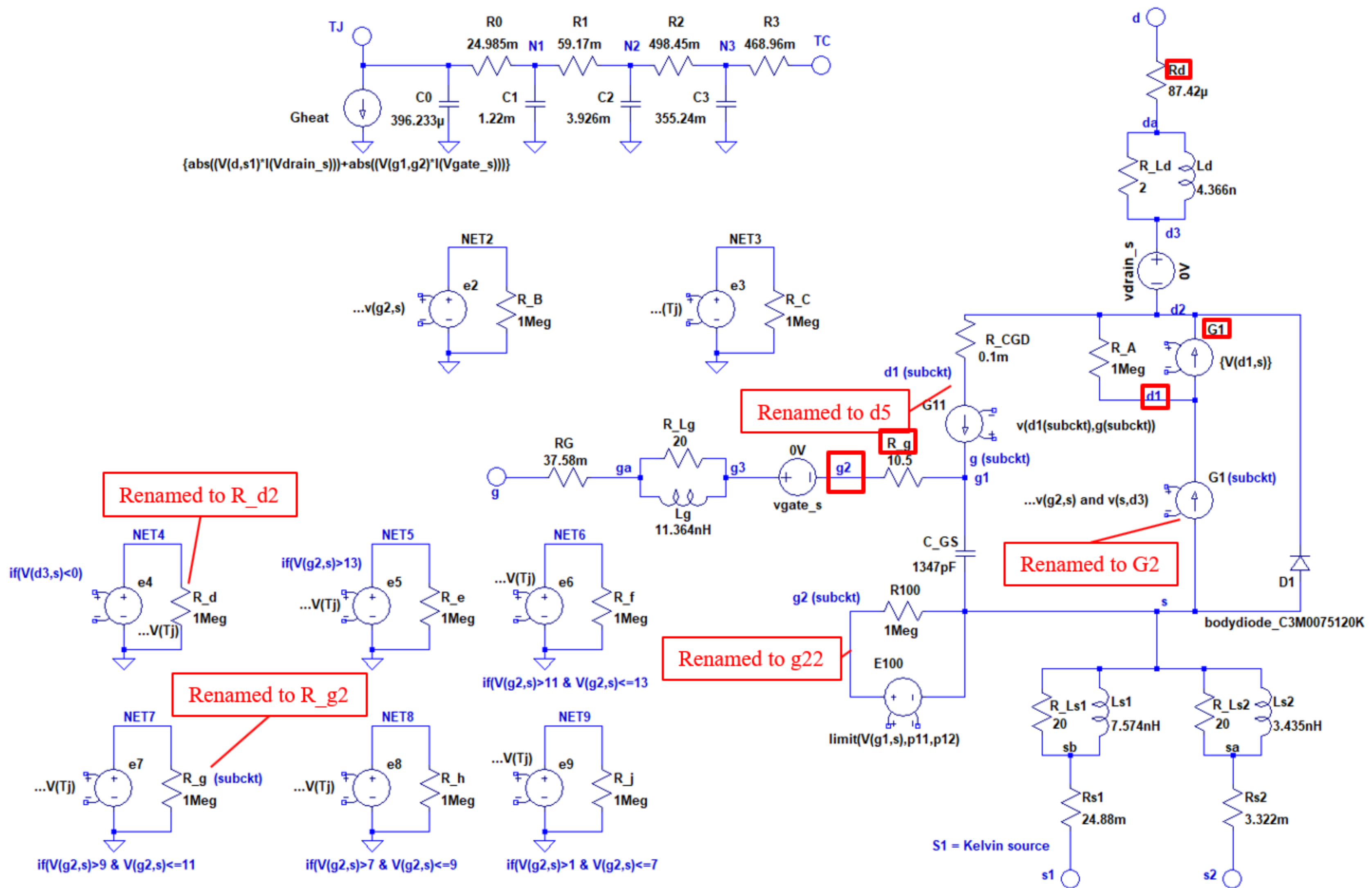

Figure 0.1: Translating and adapting the netlist file ".lib" to ".scs" provided by the manufacturer Wolfspeed CREE™ for the SiC power transistor C3M0075120K. Some elements are renamed to avoid conflict with names inside subcircuits.

TABLE A: SYNTAX TRANSLATION

LTSpice™ file (.lib)	CADENCE™ Spectrum™ file (.scs)	find and replace
{	(	yes
.param	parameters	yes
.ends	ends (subcircuit name)	yes
TANH(…)	tanh(…)	yes
If	?	no
*	//	no
, (=ELSE inside the if loop)	: (=ELSE inside the if loop)	no
Rth_1 T11 TJ {0.011}	Rth_1 (T11 TJ) resistor r=(0.011)	no
Cth_1 0 TJ {4.25e-5}	Cth_1 (T11 TJ) capacitor c=(4.25e-5)	no
G1 d2 d1 Value {V(d1,s)}	G1 (d2 d1) bsource i=(v(d1,s))	no
Example of one device		
.model bodydiode_C3M0016120K d(is=158.89n cjo=1119p)	bodydiode_C3M0016120K (s d2) d01 model d01 diode is=158.89e-9 cjo=1119e-12	no

After all this adaption is done, the power device model behavior is verified in many different simulations. All simulations are done to plot the same images of the datasheet. The curves plotted to verify are: i_D vs v_{DS} for different $v_{GS,}$ i_D vs $v_{GS,}$ the third quadrant operation, gate charge, switching times as a function of external gate resistor $R_{G.}$ **Figure 0** below is the classical i_D-v_{DS} characteristic.

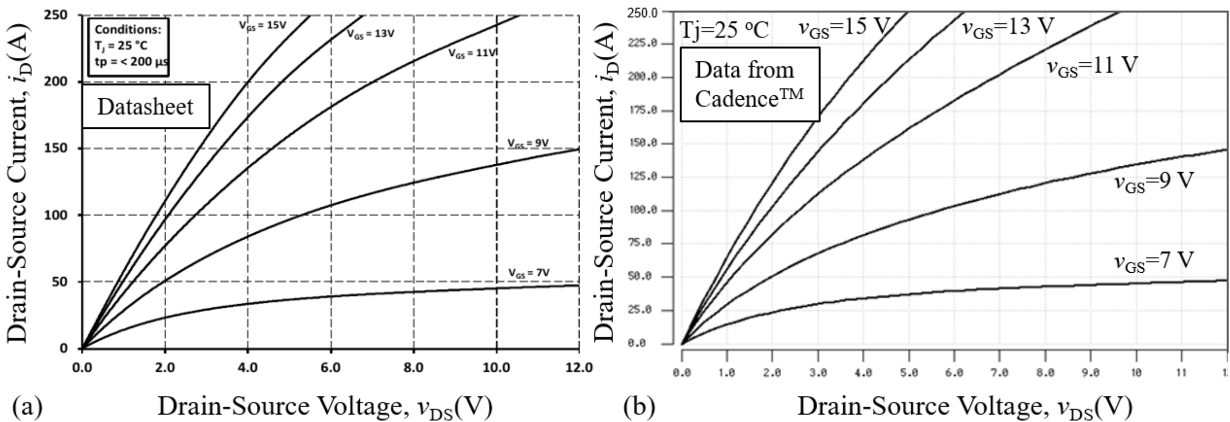

Figure 0: Comparing device's C3M0016120K (a) datasheet with (b) CADENCE™ Simulation to prove the imported and adapted model of the SiC power transistor is working as expected despites adaptations in the code.

The thermal model is verified working when imposing a junction temperature of 175 °C in CADENCE™ simulation, the curves are compared to the datasheet. All the other curves are not shown to keep this manuscript not excessively long.

Some difference has been observed in the 3rd quadrant operation. When the device did not match so well with the datasheet, a 3rd quadrant simulation is performed in LTSpice^{TM}. It is observed the manufacturer provided model has the same behavior, therefore excepting the error from the alterations during the translation of the file.

Annex 4: Preliminary Datasheet of AGD for SiC

Features

- Compatible with 1200V SiC Power MOSFETs
- i_{gMAX}=3.5 A
- Fast and controllable fall and rise times
- Split output with 3 NMOS and 3 PMOS in parallel
- Low inductance QFN40 package
- Simulated for C3M0075120K (30A) C3M0016120K (115A) devices
- Small 6 × 6 mm footprint
- High voltage dv/dt sensing capacitor C_S (2.3kV)
- Made with XFAB0.18 SOI CMOS technology

Applications

- Research application to demonstrate controllability of dv/dt in the order of 50 V/ns or higher for SiC power MOSFETs
- Characterization
- Test of sub-systems inside the chip

Description

The AGD is a gate driver with split output and dv/dt control with feedback loop that made different degrees of freedom to the designer to control the dv/dt of high voltage power devices SiC.

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This information is about a prototype built.

Absolute Maximum Range values (Tcase = 27 °C except as noted)

Parameter	Symbol	Value	Unit
PMOS high supply voltage	Vdd25V	25	V
PMOS low supply voltage	Vdd20V	20	V
NMOS high supply voltage	Vdd5V	5	V
NMOS low supply voltage	GND	0	V
Storage temperature Range	Ts	-55 to +150	°C
Operating Junction Temperature	TJ	-55 to +150	°C

Prototypes Production Information

EuroPractice Run Number	**Package type**	**Qty packaged A chips**	**Qty packaged B chips**	**Qty packaged C chips**	**Qty bare die**
7148	QFN40 6×6mm	10	10	10	40
Dim_x	**Dim_y**	**Area**	**FTP Password**	**CAD software**	**DRC/PVS software**
3000 µm	3300 µm	9.9 mm^2	dvdtG5****	CADENCE IC v6.1.6	6.0.2/ 15.23
Technology	**Service-Center**	**Ref_number**	**Layout format**	**Process cost**	**Package cost**
X-FABXT018 0.18µ SOI CMOS MET3/4/ MID/THK	IMEC	79148/A36410/01	gdsii	15550.00€	2580.00€

Electrical and Design Characteristics (Typical values at TJ = 27 °C, unless otherwise noted)

Parameter	Symbol	Min.	Typical	Max.	Unit	Conditions
PMOS high supply voltage	Vdd25V		24.5	25	V	
PMOS low supply voltage	Vdd20V		20		V	

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NMOS low supply voltage	Vdd5V		4.5	5	V	
Recommended R_{gEXT}		0	0	20	Ω	
Decoupling capacitance on-chip for Vdd5V	Cdec5V		236		pF	Between Vdd5V and GND
Decoupling capacitance on-chip for Vdd20V	Cdec20V		10.6		pF	Between Vdd20V and Vdd25V
Decoupling capacitance on-chip			45.7		pF	Between Vdd5V and Vdd25V
Bonding Wire gold (Au)			50		µm	

(1) Simulated value for a steady state with typical values.

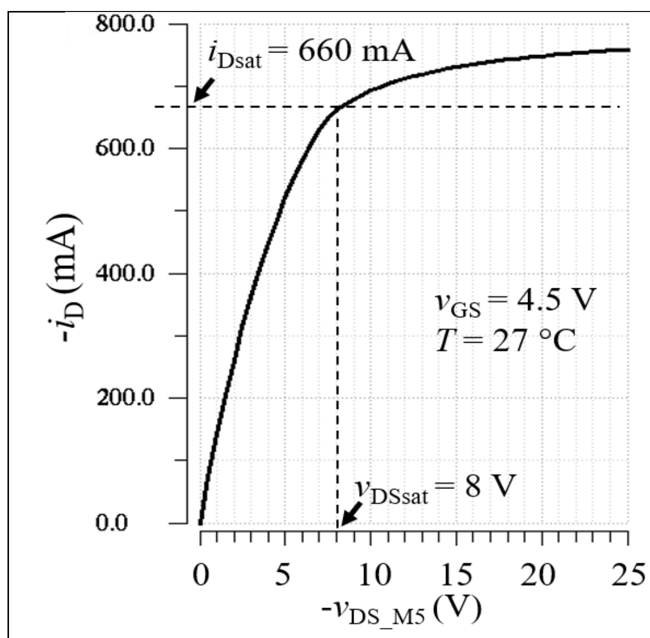

Figure 0.1. i_D–v_{DS} characteristic for the transistor PMOS M5 of the main stage buffer for width W_5=4.32 mm. It is designed to have i_{Dsat} close to the value of i_{RG_OL} to be compatible with the power devices C3M0075120K 30A and C3M0016120K 115A (and therefore a wide range of devices) @ 27°C.

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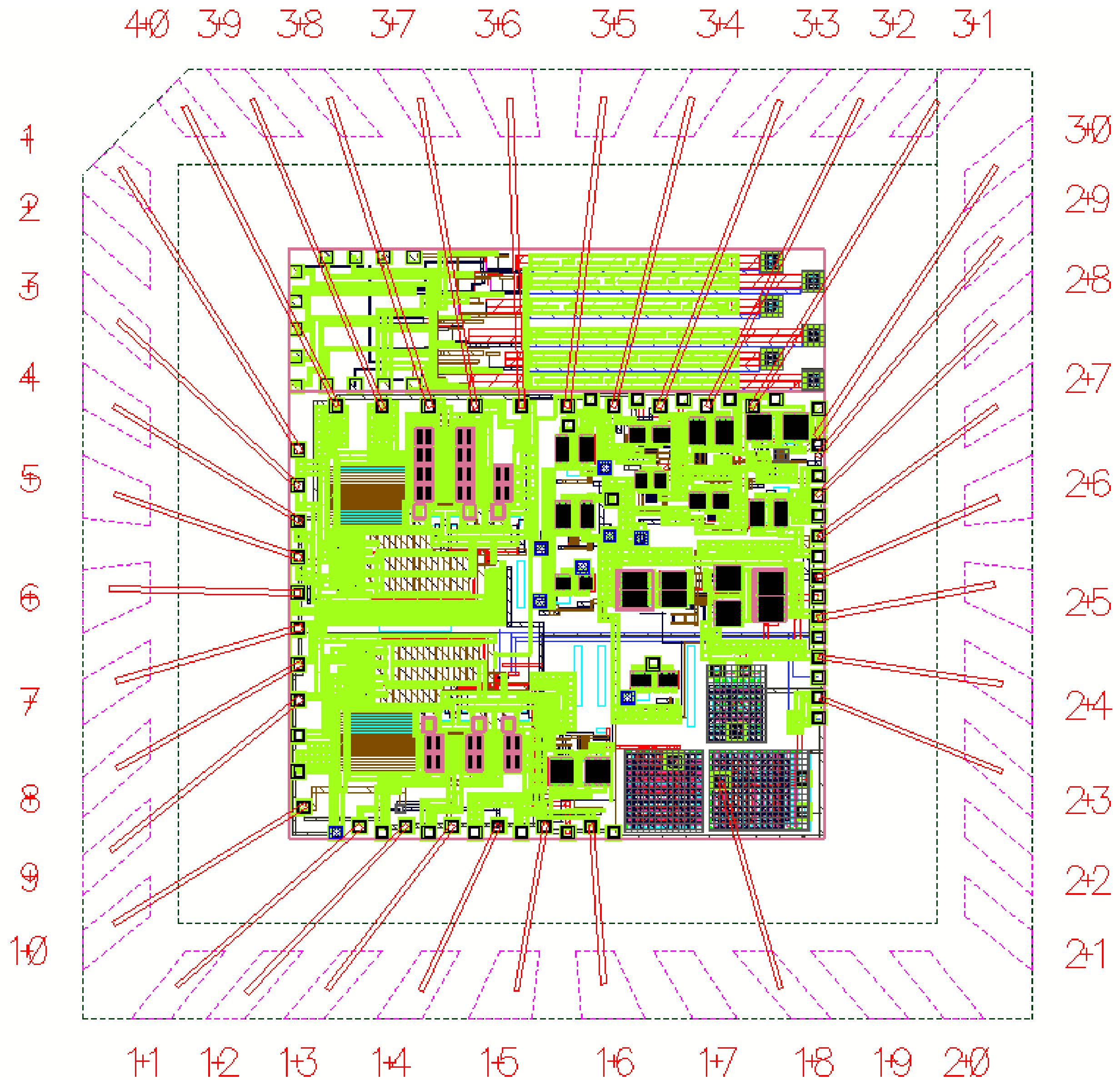

Figure A. Wire bonding A. It is expected 10 prototype units with this cabling diagram. Lid glued.

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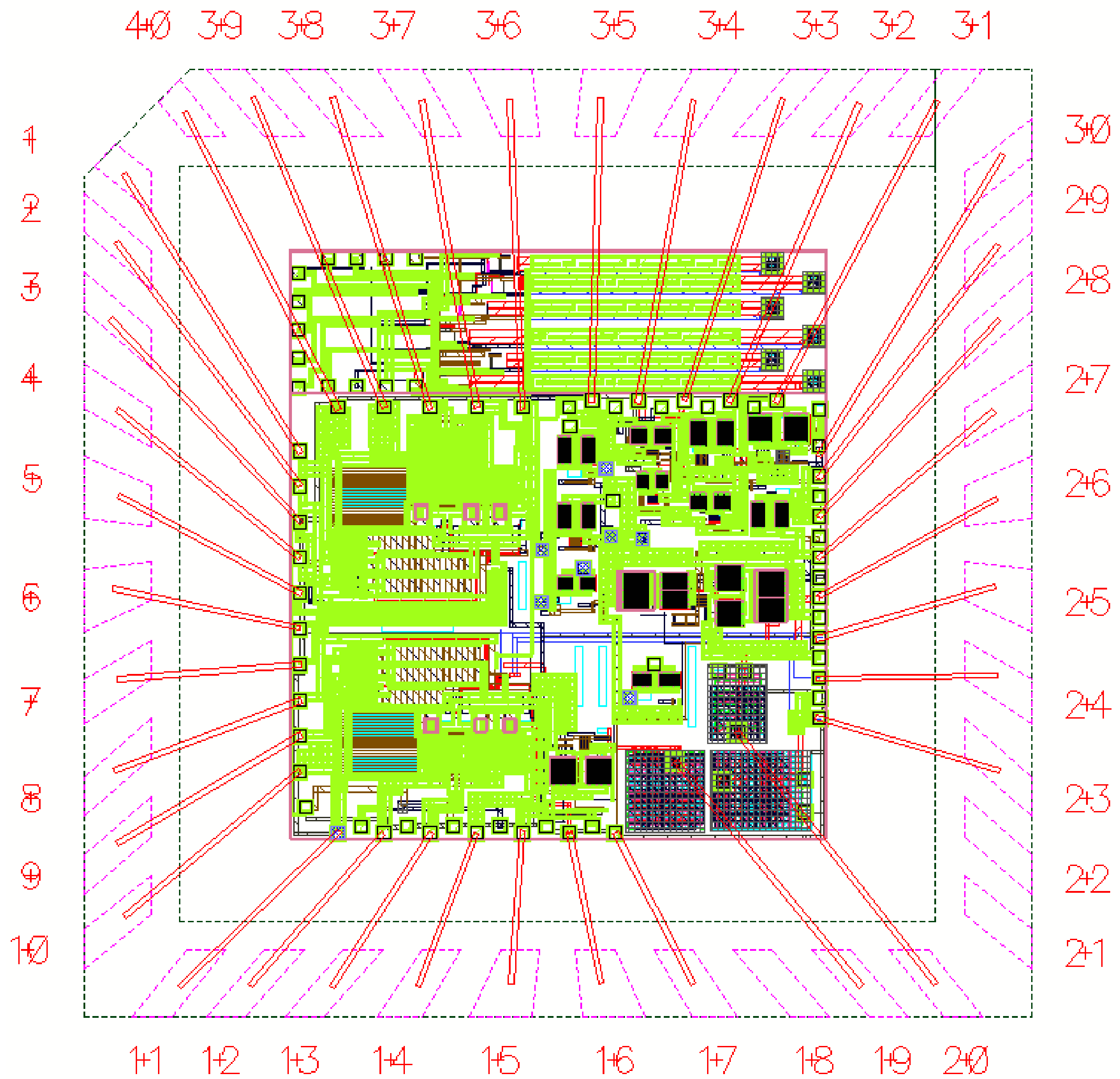

Figure B. Wire bonding B. It is expected 10 prototype units with this cabling diagram. Lid glued.

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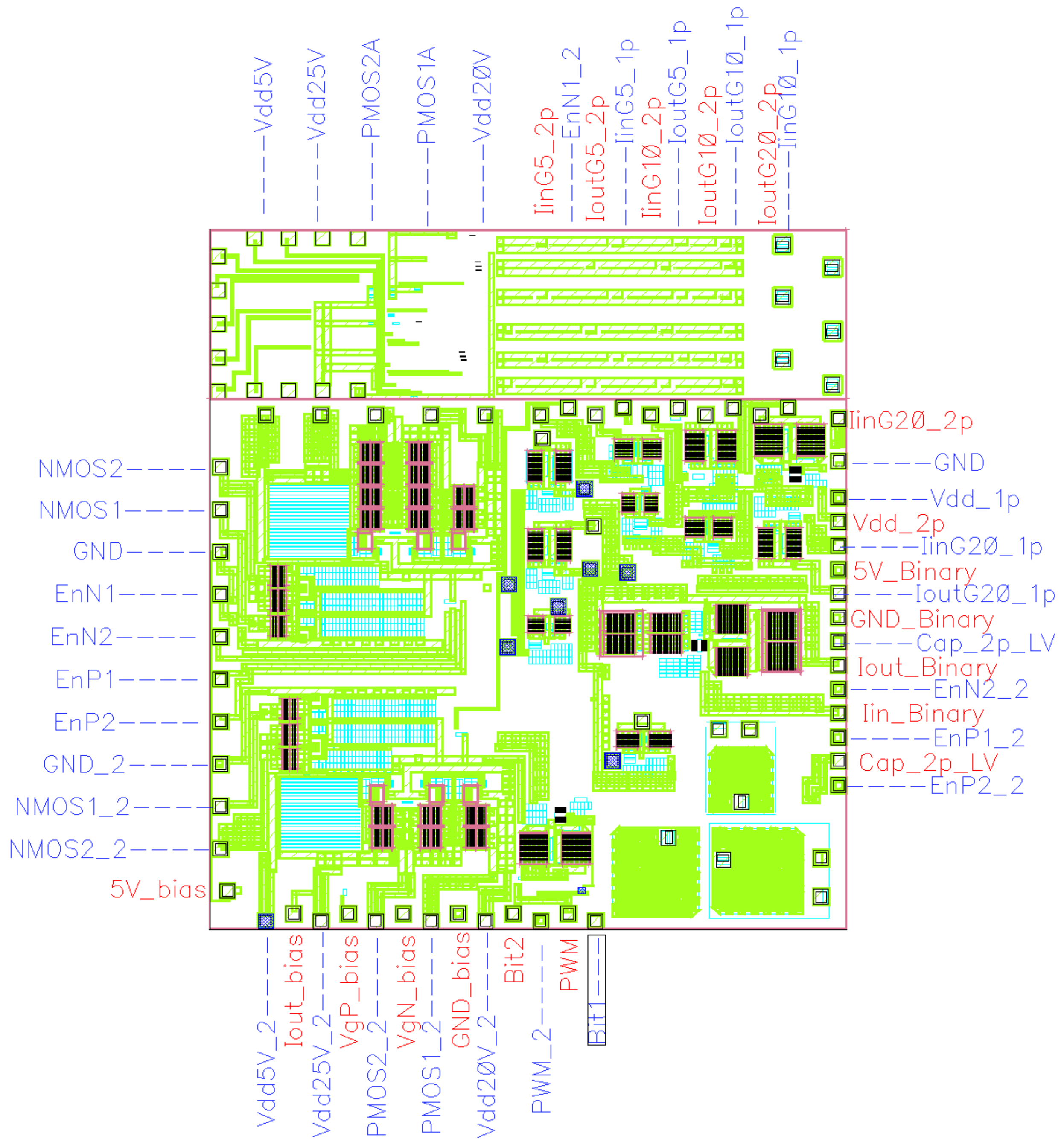

Figure C. Pads names

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Abstract

Title of the thesis: CMOS Active Gate Driver for Closed-Loop d*v*/d*t* Control of Wide Bandgap Power Transistors

Abstract. Wide bandgap (WBG) power transistors such as SiC MOSFETs and GaN HEMTs are a real breakthrough in power electronics. These power semiconductor devices have lower conduction and switching losses than their Silicon competitors. However, the fast switching transients can be an issue in terms of Electromagnetic Interferences (EMI). Consequently, one must slow down the switching speeds of WBG transistors to comply with EMI limitations, which reduces their advantages in terms of higher switching frequencies and lower total losses. In this work, an active gate driver is proposed to control the switching speed of wide bandgap semiconductor power transistors. An innovative closed-loop control circuit makes it possible to adjust separately the dv/dt and di/dt during the switching sequences. Overall, the dv/dt values can be reduced to comply with system-level limits of EMI, with less switching losses than existing methods. The proposed method is thoroughly investigated, with analytic and numerical models to assess the key performances: feedback loop bandwidth, optimal circuit design, area consumption. Selected and optimal designs are implemented in two integrated circuits in CMOS technology which demonstrate delay times below the nanosecond. With such performances, it has been shown experimentally that it is possible to actively control switching speeds higher than 100 V/ns under voltages of 400 V.

Keywords: Active Gate Driver, Switching Speed, Wide Bandgap Semiconductor, d*v*/d*t*, Closed-loop Systems, EMI (electromagnetic interference).