National Science Foundation's Industry/University Cooperative Research (I/UCRC) Program

STP-H7-CASPR: A Transition from Mission Concept to Launch

Mission-Critical Computing
NSF CENTER FOR SPACE, HIGH-PERFORMANCE, AND RESILIENT COMPUTING (SHREC)

35th Annual Small Satellite Conference

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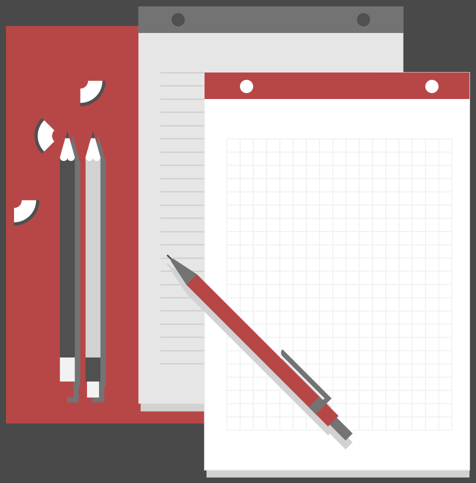
Outline

- **Acknowledgements and Programs**
- **Hybrid Space Computing**
- **Mission Design and Architecture**
  - **Goals and Objectives**
  - **Prophesee Sisley and SATLANTIS iSIM-90**
  - **Hardware and Software**
- **Development, Integration, and Testing**
  - **Design and Development**
  - **Integration and Testing**
- **Conclusions**

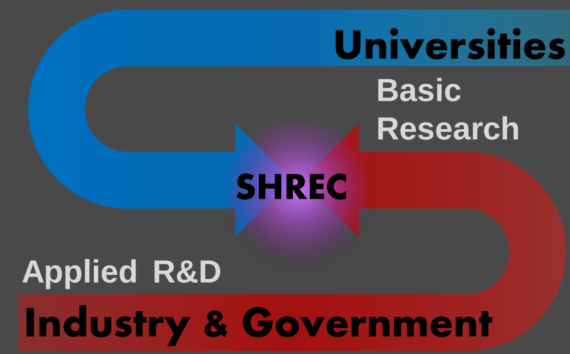


Acknowledgements and Programs

Acknowledgements

- CASPR is a research mission at Pittsburgh SHREC site
  - NSF Center for Space, High-performance, and Resilient Computing (SHREC)
    - Founded in 2017
    - Formerly NSF Center for High-performance Reconfigurable Computing (CHREC) (2007-2017)
    - Comprises 4 university sites and over 30 industry and government partners
- CASPR was collaborative effort
  - Builds on success and experience of STP-H5-CSP and STP-H6-SSIVP experiments
  - Key development partners:
    - DoD Space Test Program
    - University of Pittsburgh
    - SHREC Members
    - Renesas, Infineon, Texas Instruments

National Science Foundation
WHERE DISCOVERIES BEGIN



See **www.nsf-shrec.org** for more info

Space Test Program

Space Test Program – Houston

- Provides sole interface to NASA for all DoD payloads on International Space Station (ISS)
- Provides economic and efficient process to enable spaceflight opportunities for DoD space science and technology community

History of Mission Success

- Build upon successes of HREP, MISSE 6/7/8, STP-H3, STP-H4, STP-H5, STP-H6 while incorporating valuable lessons learned
- STP in-house contractor (MEI Technologies) expertise allows for aggressive 2-year build/integration schedule
- Aerospace Corp provides assistance to Houston team with leadership and mission assurance roles

Image Courtesy DoD Space Test Program

Hybrid Space Computing

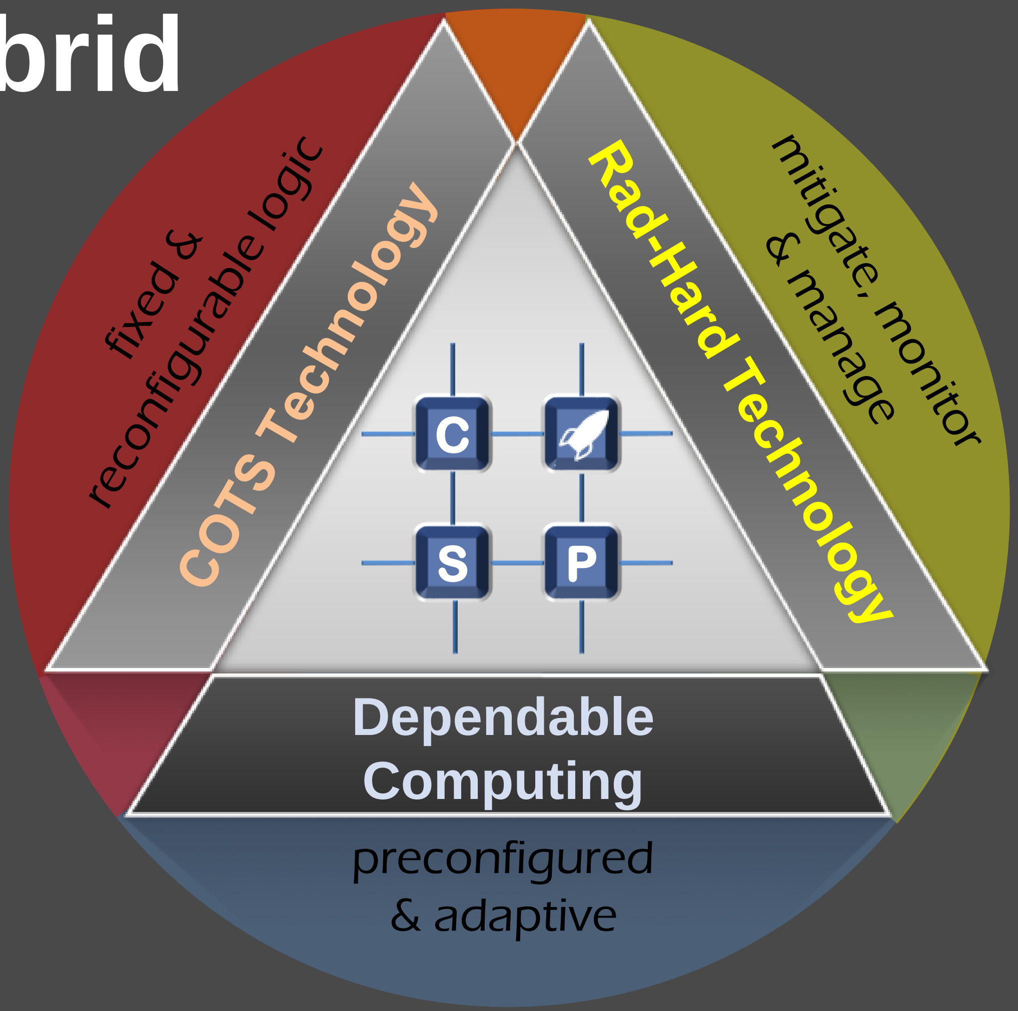
Hybrid Space-Computing Concept

Multifaceted Hybrid
Space Computing

Hybrid processor
(multicore CPU + FPGA subsystem)

Hybrid system
(commercial + rad-hard)

Robust Design
(Novel mix of COTS, rad-hard, & DCA)



CHREC Space Processor (CSP)

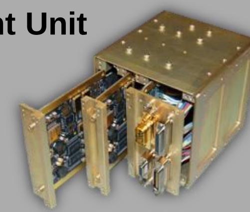
Easy Development with CSP

- Selective component population scheme supports Engineering Model (EM) and Flight Model (FM)
- Rapid and cost-effective design prototyping using evaluation kit or Zedboard / Zybo / Pynq board
- Downloadable example software designs and configurations (Linux/RTEMs, cFE, etc.)

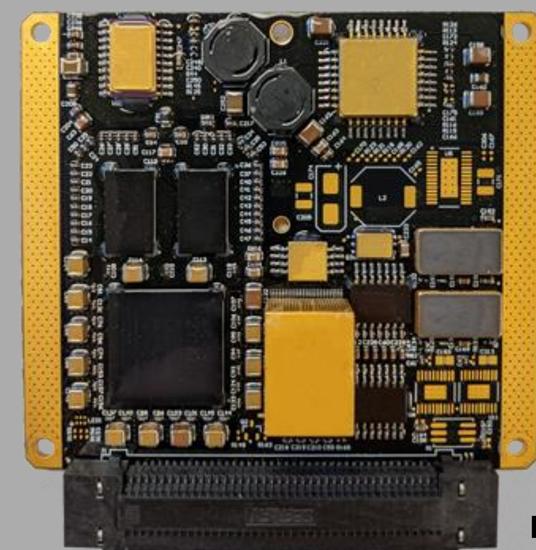
Specifications:

- Xilinx Zynq 7020 (ARM dual-core Cortex-A9 + Artix-7 FPGA)
- (1-4) GB NAND Flash
- (256 MB–1 GB) DDR3
- Dedicated Watchdog Unit
- Internal Power Regulation
- 26 Configurable ARM GPIO Pins
- 12 Single-Ended FPGA I/O Pins
- 24 High-Speed Differential Pairs

STP-H5 Flight Unit



STP-H6 Flight Unit



CSP Rev. C Flight Model

Flight Heritage on STP-H5/6
Radiation & Env. Tested

Order at spacemicro.com

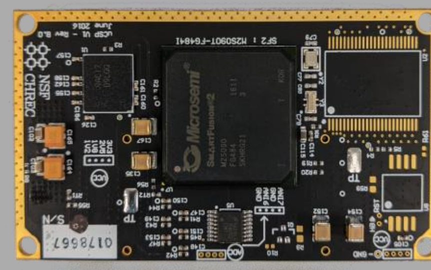
µCSP Smart Module

Even Smaller Solutions…

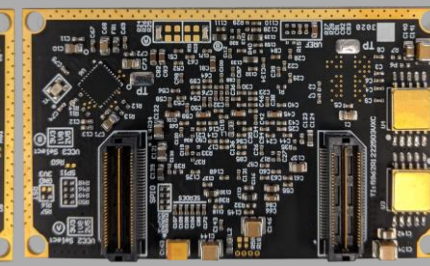
- Multifaceted hybrid processor at center of CSP Concept
- Even lower SWaP-C profile than CSP for small spacecraft missions
- Provided template for "Smart Module" designs

Specifications:

- SmartFusion 2 (ARM Cortex-M3 + FPGA)
- 64 Mb NOR Flash
- 1 Gb LPDDR3
- Dedicated Watchdog Unit
- ADC for board temp and 2 channels for flyleaded measurements



µCSP Top View



µCSP Bottom View

µCSP Smart Module

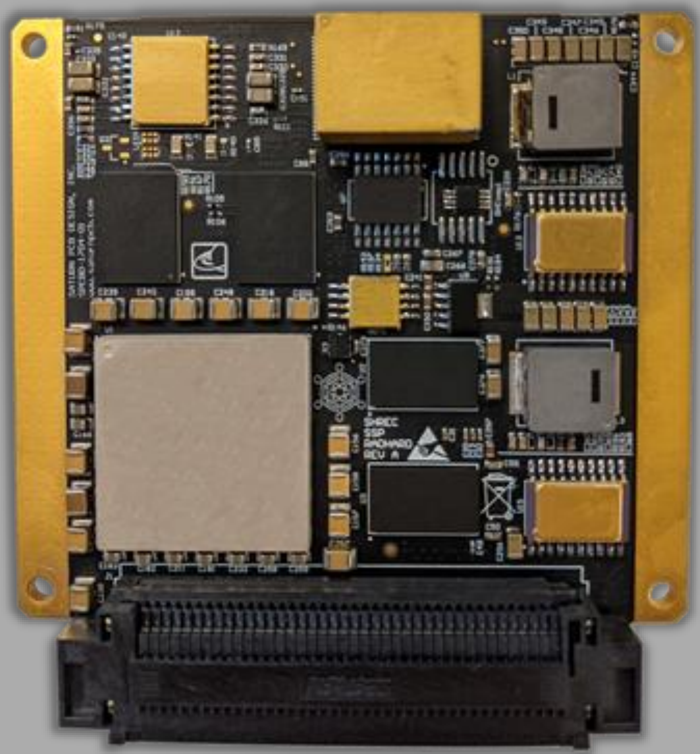
SHREC Space Processor (SSP)

Next-Generation SSP

- Builds upon CSP to create new platform with improved computational, memory, and communication capabilities
- Supports Engineering Model (EM) and Flight Model (FM) configurations

Specifications:

- Xilinx Zynq 7030/35/45 (ARM dual-core Cortex-A9 + Kintex-7 FPGA)
- (1-4) GB NAND Flash
- 1GB PS-DDR3L and 4GB PL-DDR3L Memory
- Dedicated Watchdog Unit
- Internal Power Regulation
- 28 Configurable ARM GPIO Pins
- 31 High-Speed Differential Pairs
- 8 MGT Lanes for High-speed Communication



SSP FM

Mission-Critical Computing
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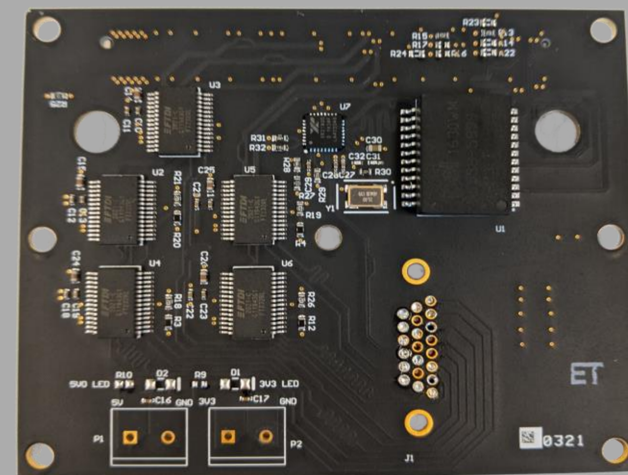
AMD Space GPU (SGPU)

AMD Embedded GX-216HC SoC

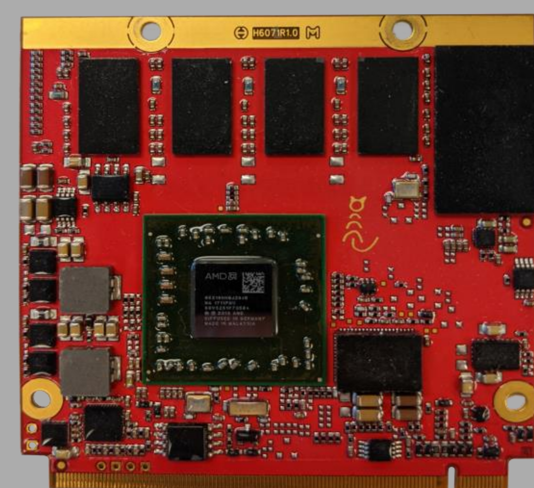
- Commercially purchased Qseven Module
- Sub-1U SoM card with application-specific carrier card
- Allows for on-board execution of deep-learning applications

Specifications:

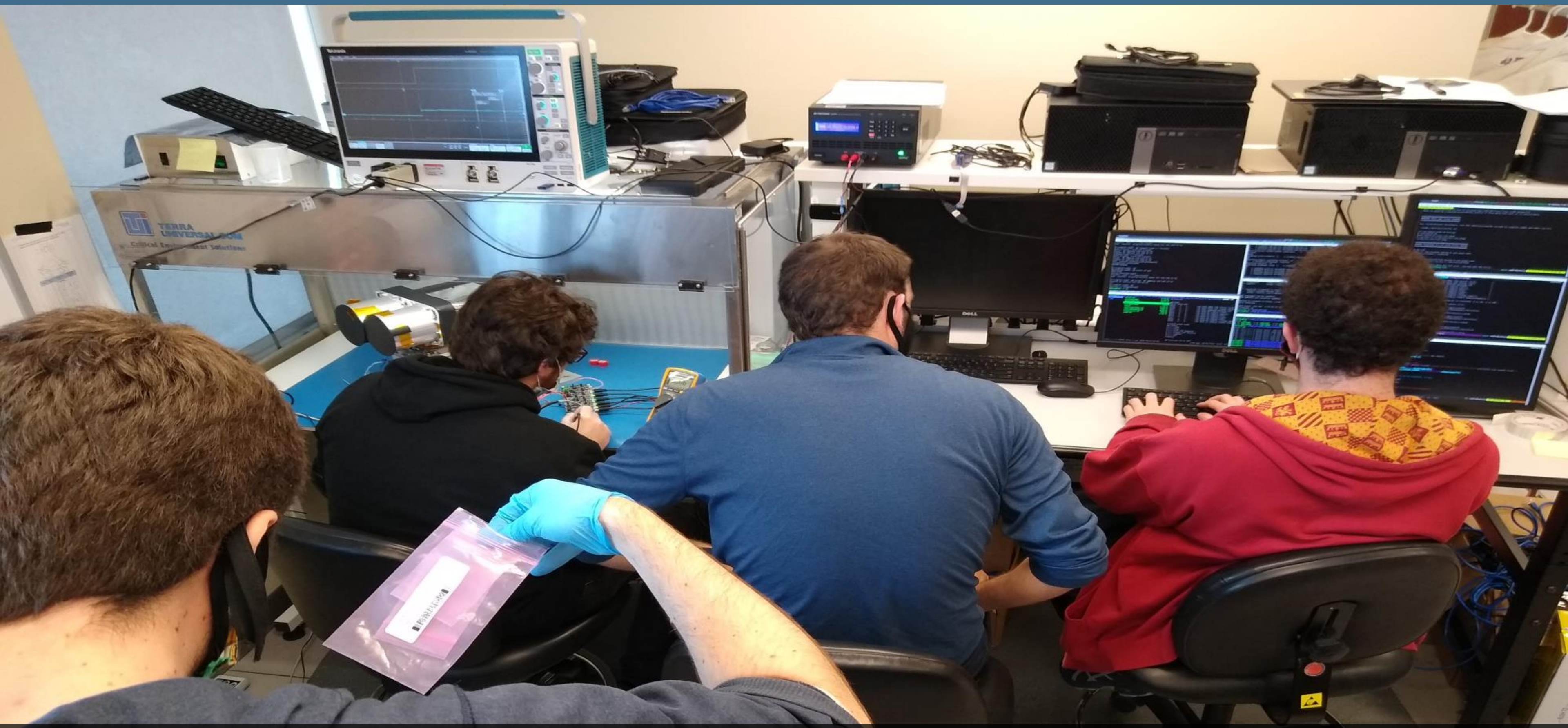
- 16GB non-volatile, onboard memory
- 4GB DDR3 memory
- Lubuntu 18.04 OS
- 100 Mbps Ethernet
- 12W power limit
- Custom carrier card



Carrier Card



AMD GPU Qseven Module



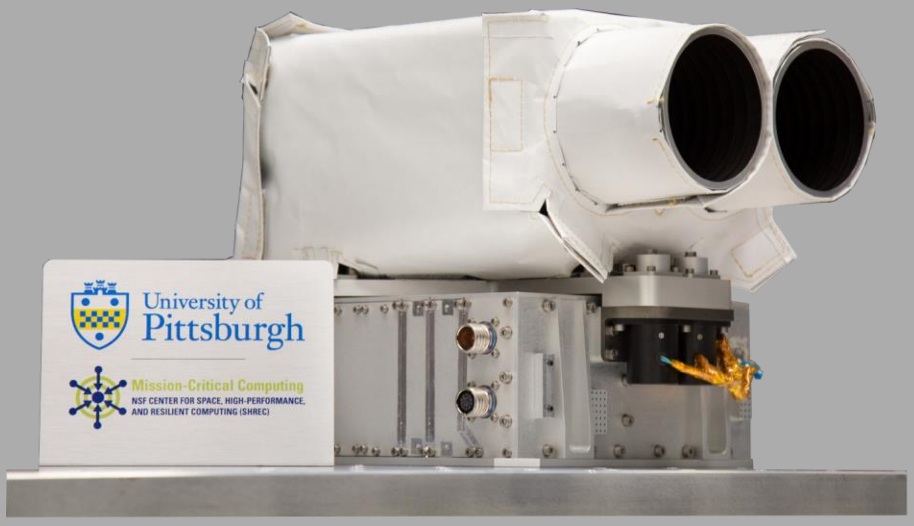
Mission Design and Architecture

CASPR Introduction

Motivation

Study and evaluate new technologies in sensors, computer systems, and deep-learning apps for space-based sensing with autonomous sensor processing

- Run onboard autonomous sensor processing apps in machine-learning and computer-vision
- 6U computing payload (2 SSPs, CSP, µCSP Smart Module, Power Card, SGPU, Backplane)
- Prophesee Sisley neuromorphic, event-driven sensor and SATLANTIS iSIM-90 optical imager



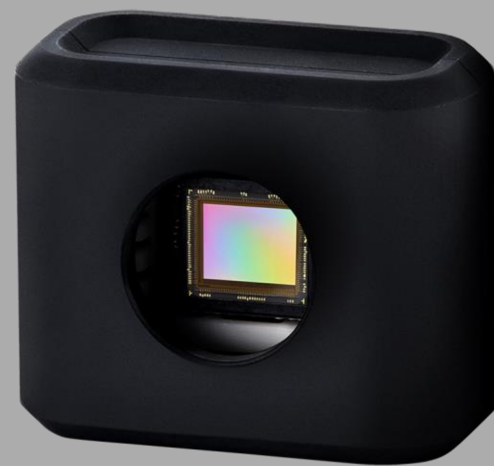
Prophesee Sisley

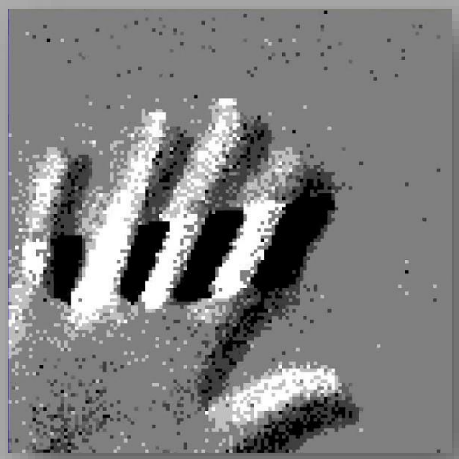
Event-driven Neuromorphic Sensor

- Developed by Prophesee
- Composed of independent pixels sensitive to events in their field-of-view (FoV)
- Captures in time domain and generates asynchronous stream of events
- Reports only dynamic changes in light intensity
- Records at low temporal resolutions while maintaining low data rate

Specifications:

- $30 \times 30\ \mu m$ pixel size
- 640 x 480 pixel resolution
- 66 mega-events per second





SATLANTIS iSIM-90

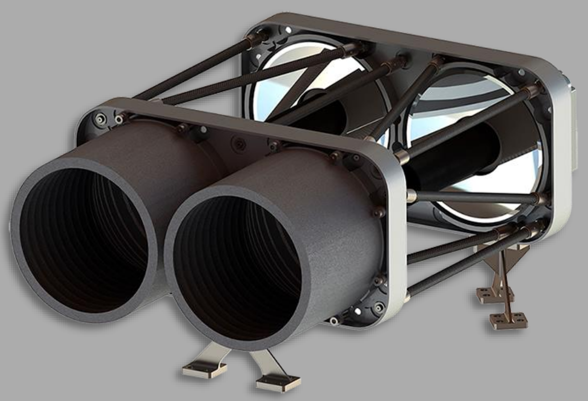
Binocular Camera System

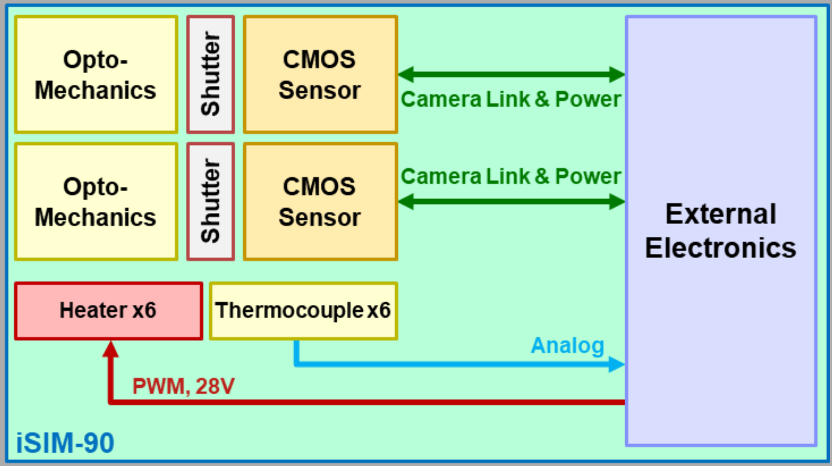
- Collaboration with SATLANTIS
- Next-generation, multispectral, high-resolution optical imager for Earth observation
- Combines class-leading performance via use of cutting-edge technologies
- Provides diffraction-limited images from blue band to near-infrared (NIR) band

Specifications:

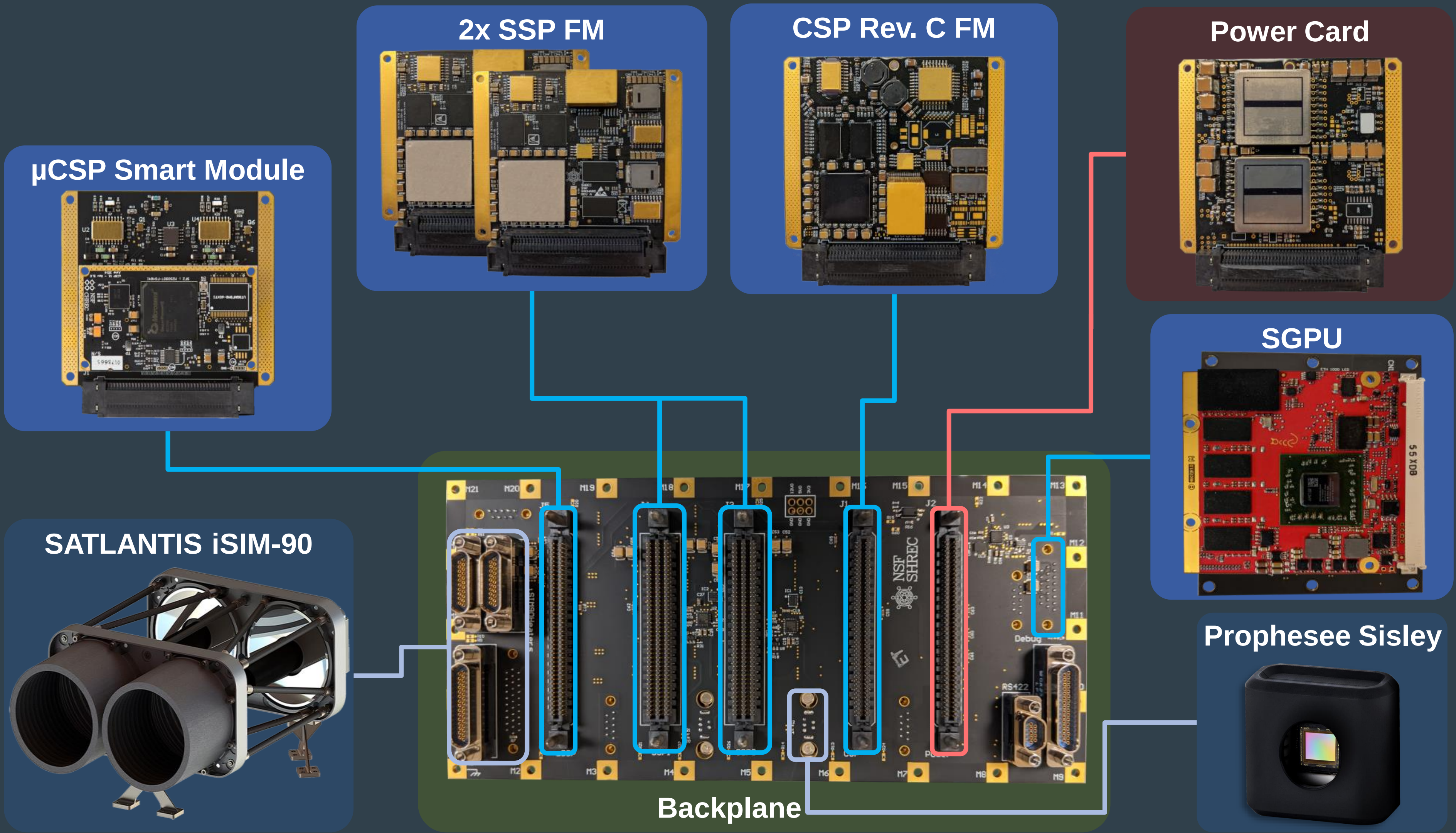
- GRD @ $400km$: $3.7m$
- GSD @ $400km$: $2.2m$
- Ideal operating temperatures: $23 \pm 3\ °C$
- Multi-spectral super-resolution algorithms
- 12MP @ 6.3 FPS

iSIM-90 Optics

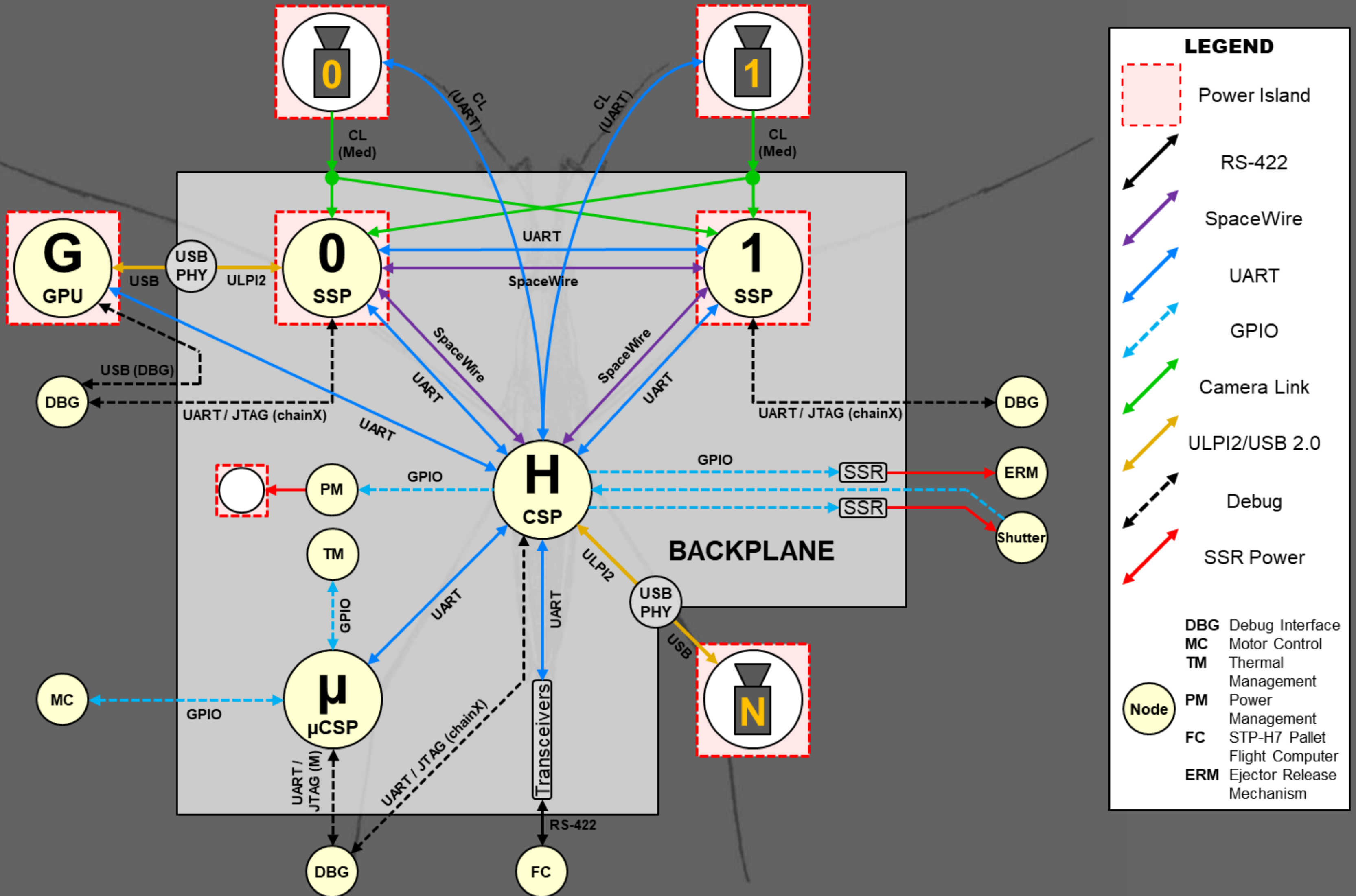




Flight Electronics



System Architecture



Flight Software

Software Architecture

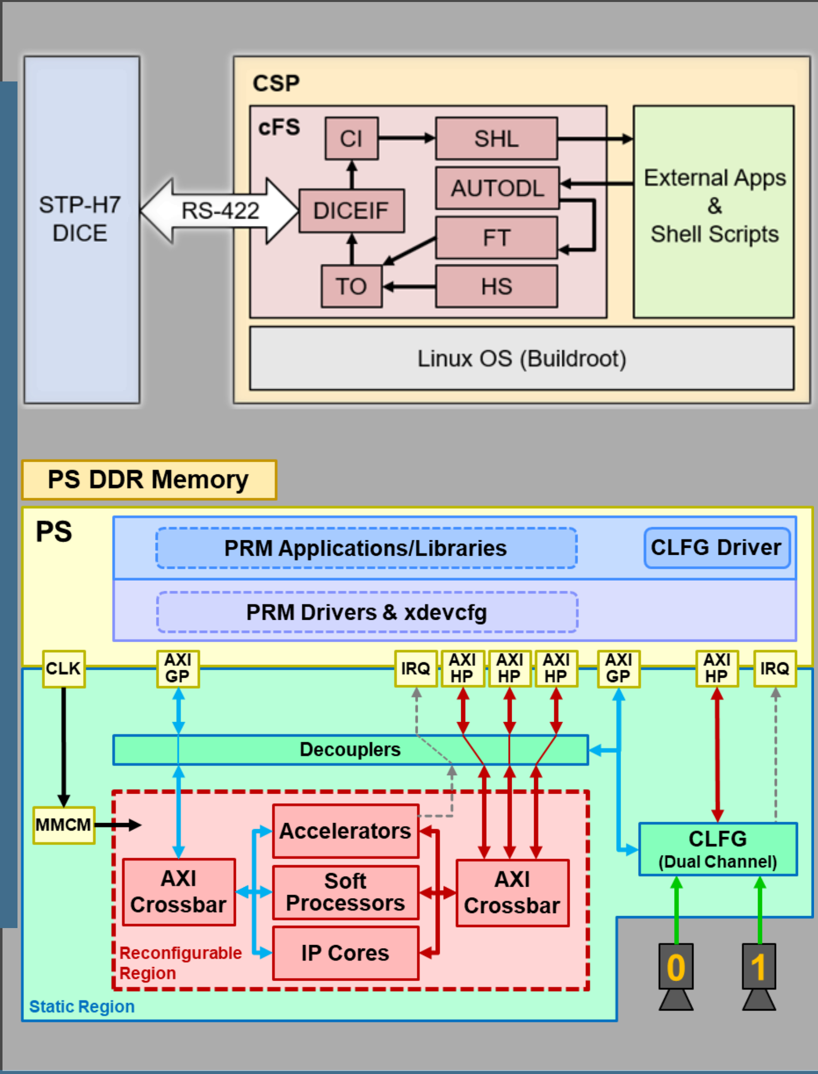
- Includes Linux operating system and core Flight Software supplemented by drivers, services, and applications
- CSP and SSP run Wumbo Linux
- SGPU runs Lubuntu 18.04 LTS

Services and Applications

- Core Flight Executive (cFE)
  - Mission-independent software services
- Core Flight System (cFS)
  - Applications and libraries running on cFE

FPGA Management

- CSP and SSP feature complete hardware/software stacks to facilitate high-throughput imaging and FPGA acceleration



Development, Integration, and Testing

Design and Development

Initial Design and Development

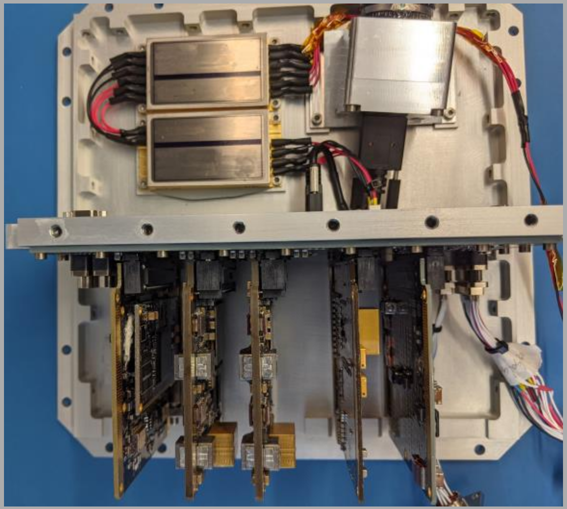
- Mission objective formulated and architecture designed using modular and iterative approach
- Network topology designed iteratively to connect all modules into one system architecture

Preliminary Testing

- Testing performed on available development kits prior to FlatSat
- FlatSat designed to integrate flight cards with connections to peripherals for validation

Design for Flight

- Parts on flight cards epoxied for stability and to survive launch conditions
- Each flight card conformally coated to survive harsh environment of space



Integration and Testing

Assembly

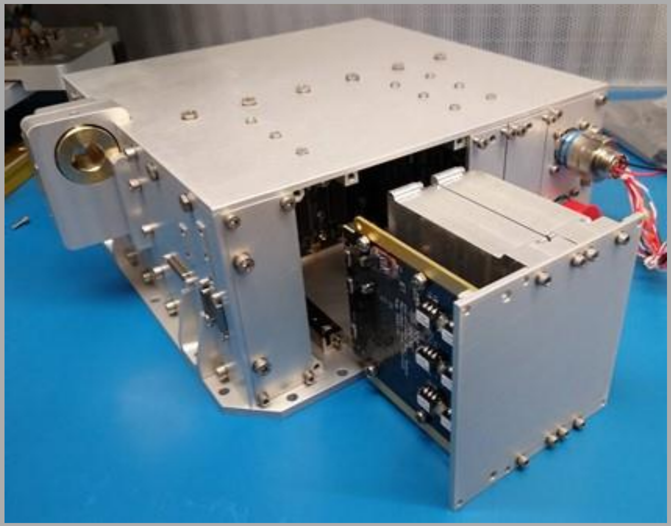
- All flight cards assembled in chassis and integrated with custom flight harnesses
- Sisley encased using custom aluminum enclosure
- iSIM-90 mounted atop gimbal-actuated platform

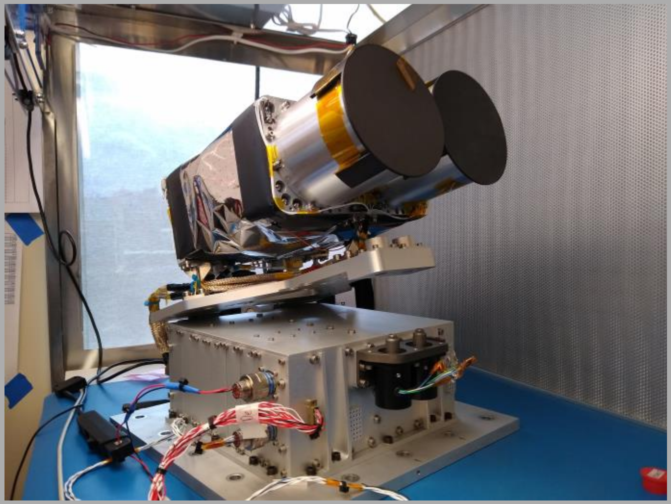
Testing and Validation

- Software iteratively installed, verified, and adapted throughout assembly process
- Scripts prepared to properly initialize and configure hardware for functional verification

Environmental Testing

- Workmanship vibration and thermal-vacuum testing performed at Naval Research Lab to ensure system survival





Conclusions

- **Advancements in sensor technologies**
  - Introduces big-data challenges due to massive datasets and limitations in downlink
  - Escalates app demands for autonomous sensor processing
  - Tightens constraints in size, weight, power, and cost
- **Autonomous sensor processing on STP-H7**
  - Focuses on evaluating new sensor technologies
    - Prophesee Sisley neuromorphic sensor and SATLANTIS iSIM-90 optical imager
  - Expands computing capabilities
    - Combines novel sensor technologies with innovative computing techniques on resilient and high-performance flight hardware
- **CASPR was successfully delivered to STP at NASA Johnson Space Center to be integrated onto STP-H7 pallet**

More Information?

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Questions?
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