IN-FLIGHT RECONFIGURATION WITH SYSTEM-ON-MODULE BASED ARCHITECTURES FOR SCIENCE INSTRUMENTS ON NANOSATELLITES

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Heritage in remote sensing instrumention at airborne, balloon and satellites

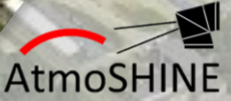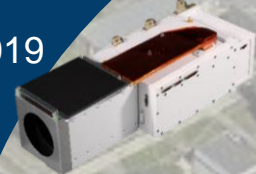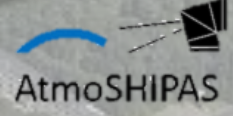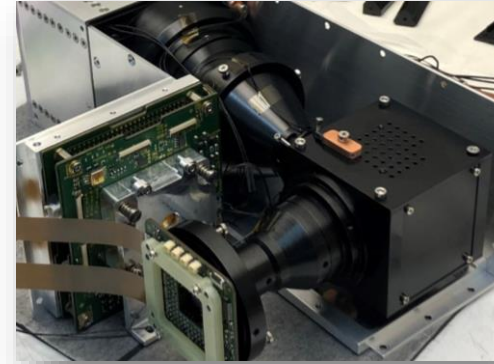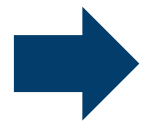# MINIATURIZED CLIMATE RESEARCH INSTRUMENTS

Objectives and Challenges

- standardized sublevel components available (power, communication, altitude control, deorbiting,…)

- customize **science payload electronics** needed

SHI spectrometer for atmospheric temperature measurements

➡ **flexibility, (re)programmability, modularity, reusability**

SPIE-JARS 05/2019

- novel science "standardized" payload electronics based on our "system on module" approach with heritage from precursor instruments (AtmoHIT & AtmoSHINE) on sounding rocket and in space

- long-term measurements with custom mitigation techniques using COTS components

- focus is on imaging sensors in combination with integrated System-on-Chip (SoC) solutions
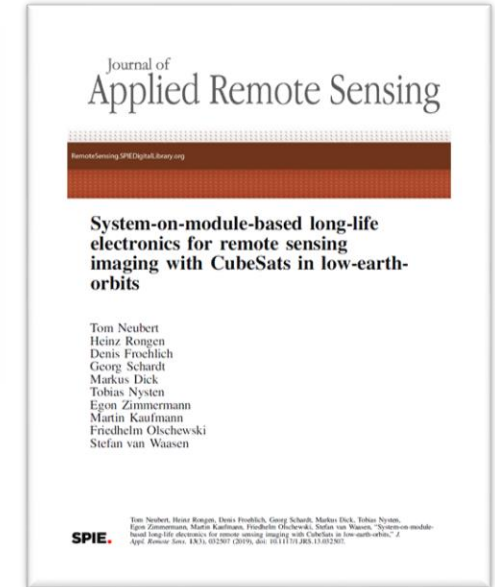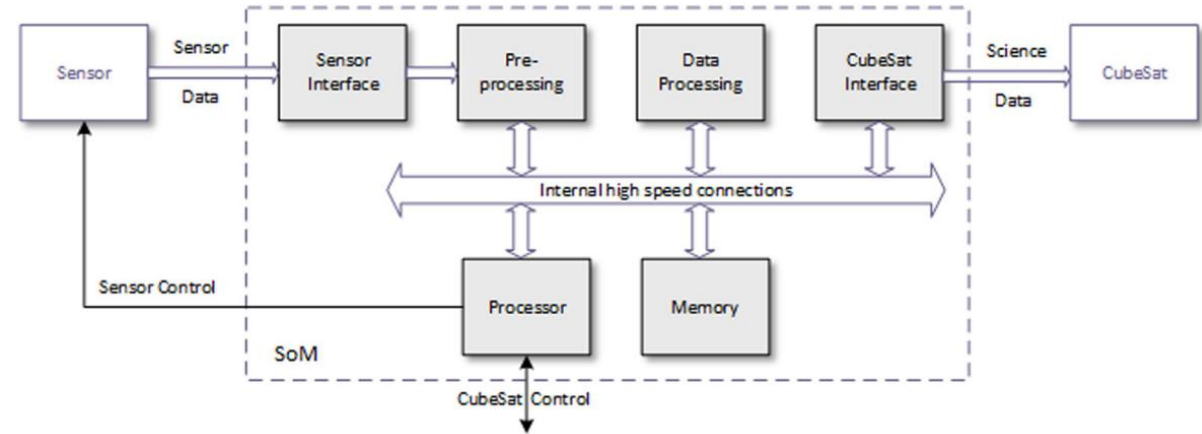
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SYSTEM-ON-MODULE APPROACH

Features

- Pin compatible modules with processing units, memory and power conversion

- Several processing capabilities (CPLD, FPGAs, µC, SoC, MPSoC)

- Short development time, 'low' design expertise needed (universities)

Challenge

- Radiation environment, system reliability

- Size, power consumption, limited data bandwidth and costs
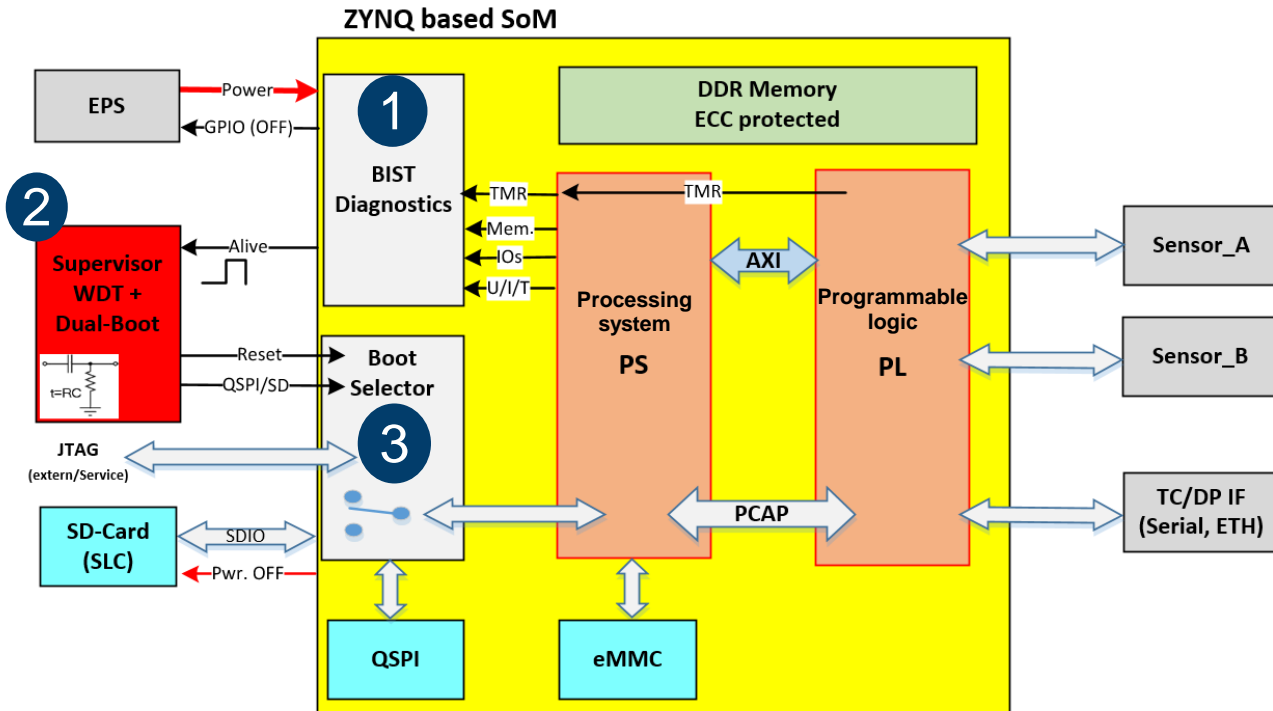
Solution approach

- SRAM-based XILINX System-on-Chip (SoC) architectures contains processing units (PS) and reconfigurable logic (PL)

- Mitigation techniques, protection circuits and **reconfiguration** for long-term measurements

Source: https://shop.trenz-electronic.de

A RECONFIGURABLE SCIENCE ELECTRONICS

Blockdiagram


Firmware storage devices
- QSPI   nominal (primary) boot device
- SD-Card   redundant (secondary) boot device
- eMMC   Transfer memory and 'Golden image'

Reconfiguration strategy

1 **Built-In-Self-Test (BIST)**: Detection and monitoring of failure
- Diagnostics for all vital functions
- Classification in
  - Minor   → Warning
  - Major errors   → Reconfiguration
  - Critical situations → Shutdown

2 **Save reconfiguration**
- on Software crash
- compensate for SEU and SEFI induced errors
- safe shutdown at SEL events

3 **Highly secured boot process**
- Redundant boot devices
  - Automatic switch between Nominal/Redundant
- 'Golden Image' in third device
- BIST and automatic correction of invalid FW image

video
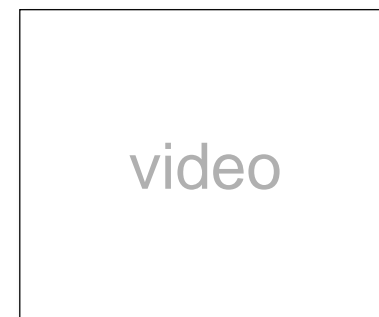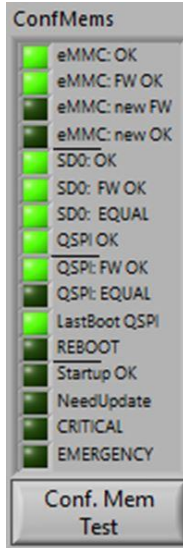
SUPERVISOR CIRCUIT

Simple watchdog IC with two functional blocks

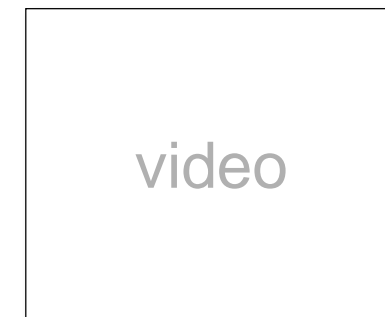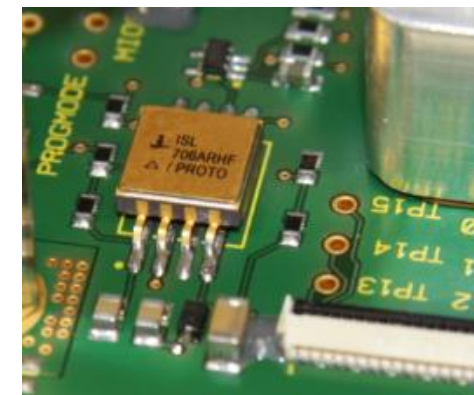**1** **Triggering the Reconfiguration**

- 'alive' signal is a combined signal by software task at PS and logic block inside PL
- when PS or PL stops working (crash), WDT resets the system
- at major risks 'alive' trigger signal will suppressed by BIST
  - SEU events occur inside TMR (PL)
  - Cyclic memory pattern checks fails (PS)
  - TM/TC and HK packages inconsistent
  - Error at peripheral interfaces (I^2C, SPI, DMA)
  - Discrepancies in configuration memories

2 **Dual Boot Functionality**

- using time delay at PFI input during power up to start from nominal boot device
- corrupted configuration will force a reset **1** due to missing 'alive' signal and PFI output (BootSelect) has inverted after this time
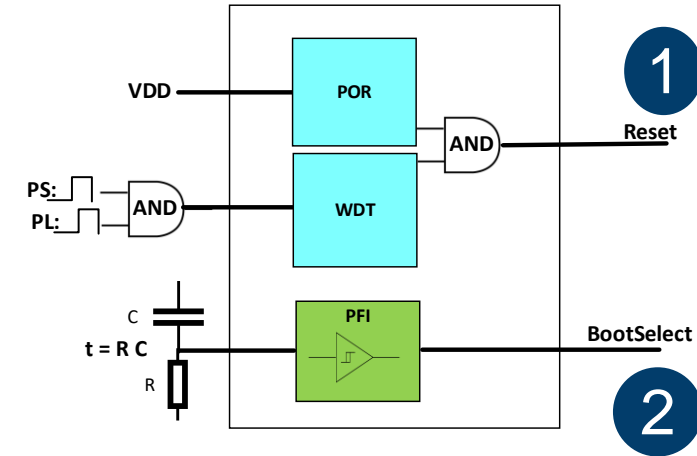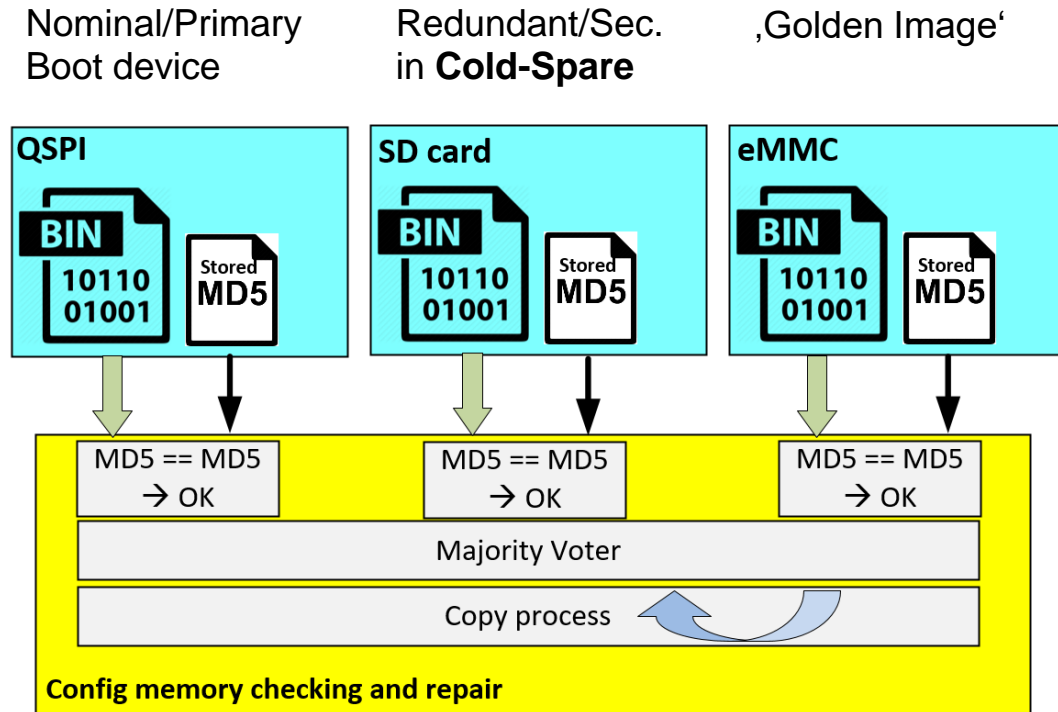

- ISL706ARH (5962R1121304VXC)
- QML qualified per MIL-PRF-38535
- High dose rate   100krad(Si)
- SEL LET$_{TH}$ 86MeV•cm2/mg

FIRMWARE CHECK AND ‚SELF-REPAIR'

TMR like behavior of the three configuration memories

Nominal/Primary Boot device — QSPI

Redundant/Sec. in **Cold-Spare** — SD card

‚Golden Image' — eMMC

Each configuration memory holds the binary boot image and the correct MD5 hash tag in a separate file.

1) BIST

- At power-up time 'System-checker' process
- Firmware and stored MD5# are checked
  → FW OK marker for each device
- MD5# tags are compared to each other's
  → Discrepancy of memory content

2) Self-Repair, in case of a discrepancy
  - consistent memory is copied to the faulty one

video

IN-FLIGHT RECONFIGURATION

Communication Concept
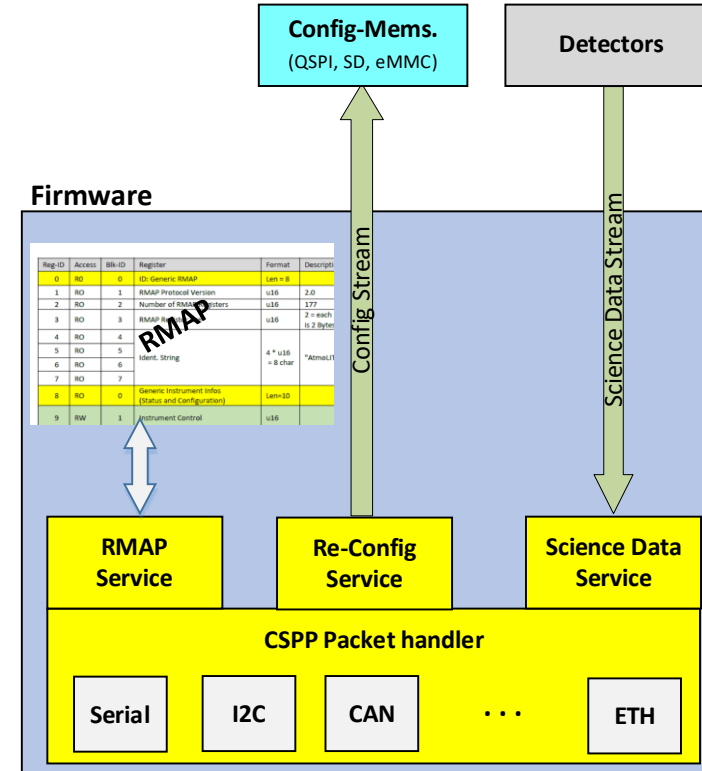
- OBC handles all ground communication via radio (S-, X- Band)
- Ground testing via direct network link
- Multiple physical interfaces
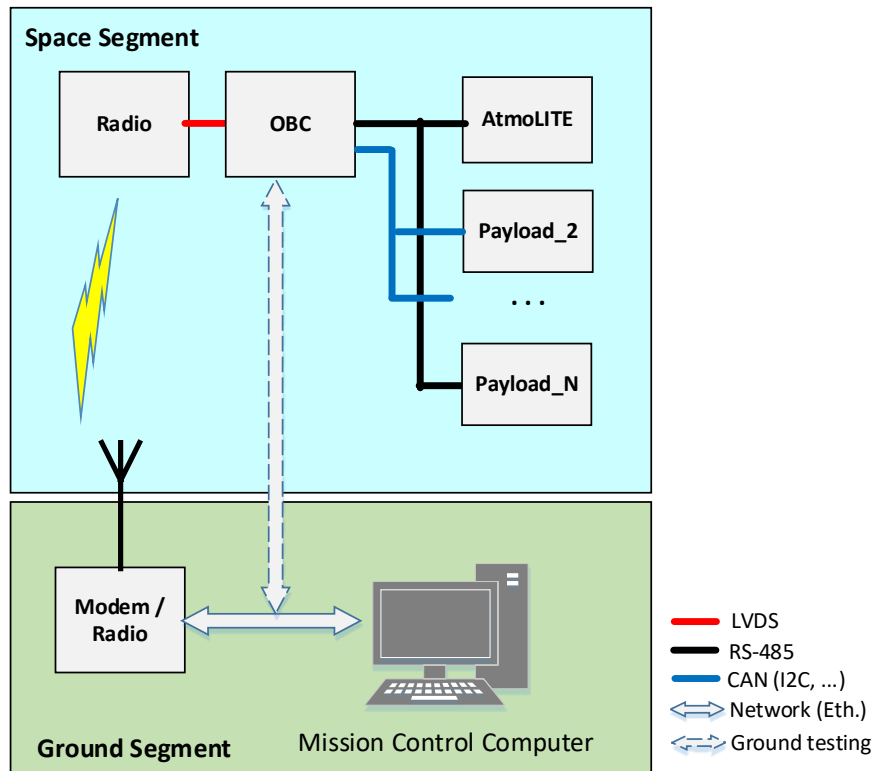
CubeSat Space Packet Protocol*(CSPP)

- CSPP supports multiple interfaces (physical layer)
- 16 Byte Header,
  - Protocol and Routing information
  - Parameter and Data block, CRC secured

* Source: Git repository: https://github.com/libcsp/libcsp
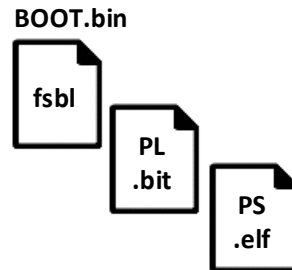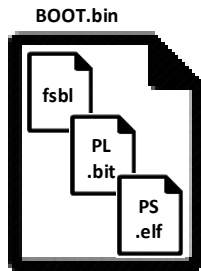
IN-FLIGHT FIRMWARE UPLOAD

Firmware

Firmware consists of **three** parts:
- First-Stage-Bootloader (fsbl)   ~ 100 KB
- PL configuration bit stream (.bit)   1.8 … 4 MB
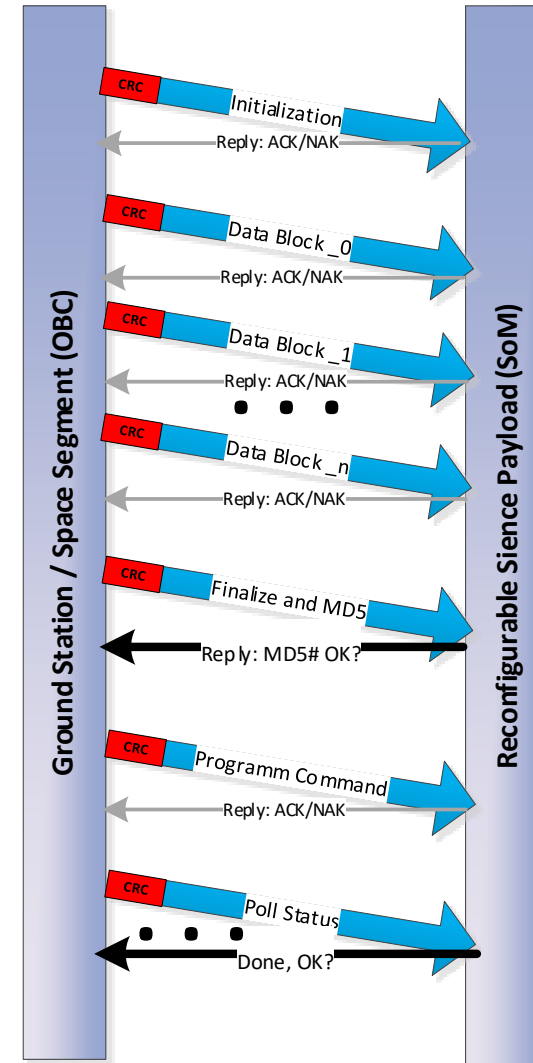- PS application code (.elf).   ~ 1 MB (FreeRTOS)

→ BOOT.BIN   or as single files

BOOT.bin

fsbl

PL .bit

PS .elf

BOOT.bin

fsbl

PL .bit

PS .elf

- Files can be compressed in Xilinx Vivado toolchain, to reduce uplink capacity

Upload process

Ground Station / Space Segment (OBC)

Reconfigurable Sience Payload (SoM)

CRC Initialization
Reply: ACK/NAK

CRC Data Block_0
Reply: ACK/NAK

CRC Data Block_1
Reply: ACK/NAK
• • •

CRC Data Block_n
Reply: ACK/NAK

CRC Finalize and MD5
Reply: MD5# OK?

CRC Programm Command
Reply: ACK/NAK

CRC Poll Status
• • •
Done, OK?

Initialization information
- Total size of Configuration

Upload Data blocks:
- block size in parameters
- Data-CRC secured
- Reply ACK/NAK
- on NAK: resend block

Validation
- Send MD5#
- Generate local MD5#
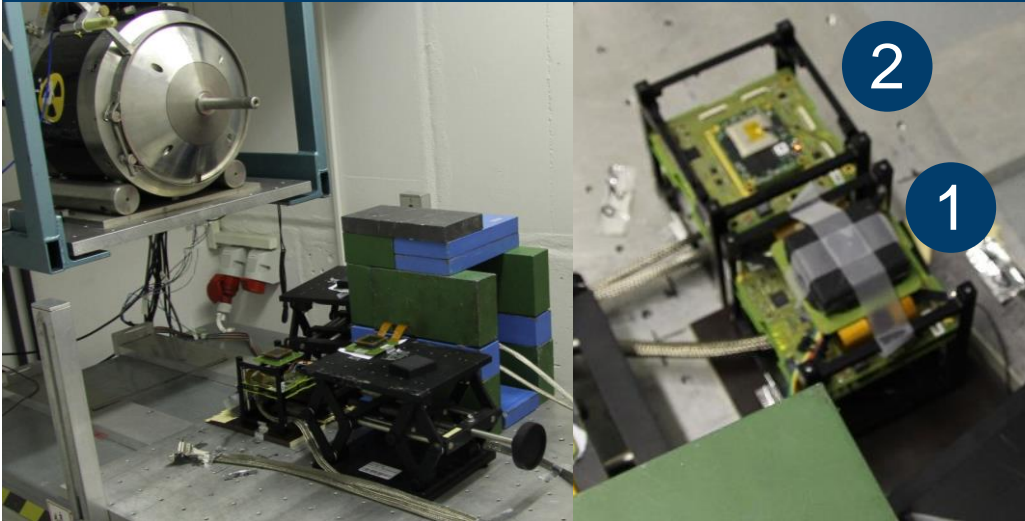- Compare MD5's#
- Reply ACK / NAK

Program Operation

video

FIRST IMPLEMENTATION RESULTS


Radiation Test

				ZYNQ - 7000 TE720-ECC (S/N: 609088)			ULTRASCALE + TE820 (S/N: 527320)		
reconfiguration cycle	meas_time	dose rate in krad/h	TID / kRad	QSPI	SD_Card	EMMC	QSPI	SD_Card	EMMC
1	18:44:00	1	0.00	pass	pass	pass	pass	pass	pass
2	19:40:00	1	0.93	pass	pass	pass	pass	pass	pass
3	22:05:00	1	3.35	pass	pass	pass	pass	pass	pass
4	23:50:00	1	5.10	pass	pass	pass	pass	pass	pass
5	05:30:00	1	10.76	pass	pass	pass	pass	pass	pass
6	08:30:00	1	13.76	pass	pass	pass			
7	09:15:00	1	14.51	fail	pass	pass			
8	10:50:00	0	14.51	fail	pass	pass			
9	12:14:00	3	18.71	fail	pass	pass			
10	12:29:00	3	19.40	fail	pass	pass			

Thermal Cycling Tests


temperature cycling test
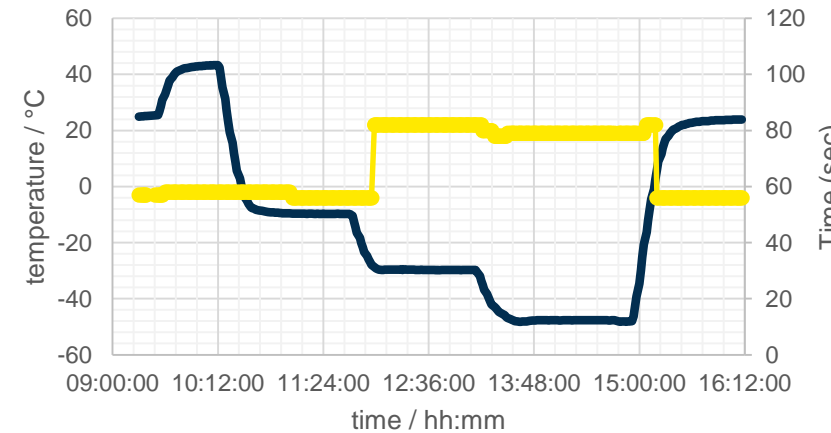
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SUMMARY

- Reconfiguration strategy using BIST classify hazards into different risk levels leads to interact on demand
- With additional memory devices available at SoM a highly secured boot process are demonstrated
- Dual boot functionality with a simple supervisor chip increases reliability
- Implementation of on-board firmware self check and repair is secured based on MD5 checksum
- In-flight reconfiguration using packet based protocol (CSP) is independent from physical layer interfaces (CAN, I²C, UART, LAN,…)
- Firmware can be partly uploaded and compressed to safe uplink time
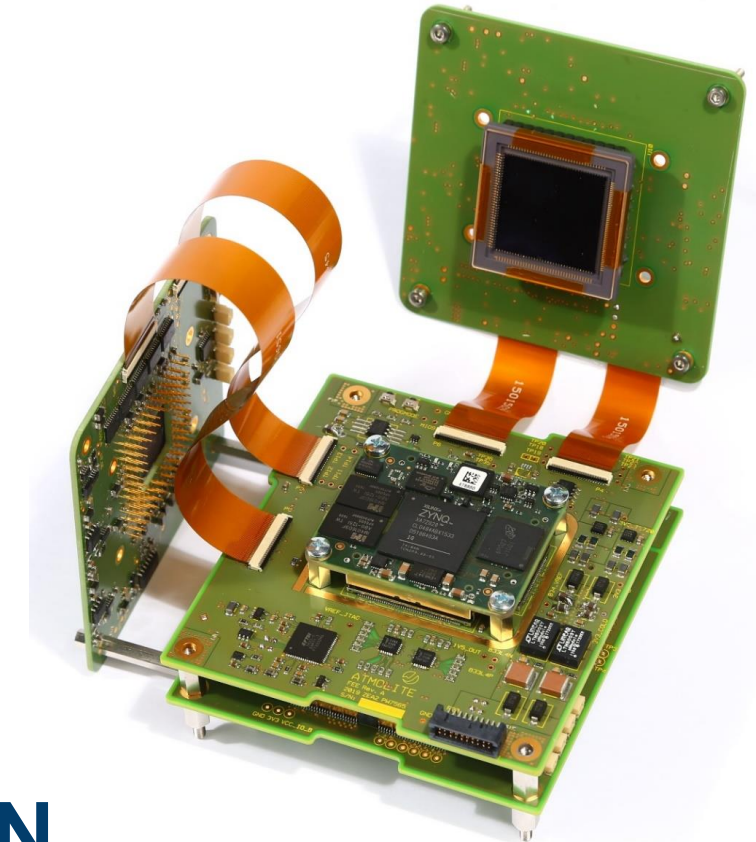
THANK YOU FOR YOUR ATTENTION

Please join the Q&A WEBINAR (Aug. 11th).
Further information in conference proceeding paper (SSC21-VIII-08).

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