National Aeronautics and Space Administration

NASA SpaceCube

Edge TPU SmallSat Card for Autonomous Operations and Onboard Science-Data Analysis

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SpaceCube

www.nasa.gov

Outline

1. Introduction to SpaceCube and AI
2. SpaceCube Low-power Edge AI Node (SC-LEARN)
3. STP-H9 SCENIC AI Demonstration
4. Accuracy and Execution Results
5. Conclusions and Cross-Cutting Capabilities

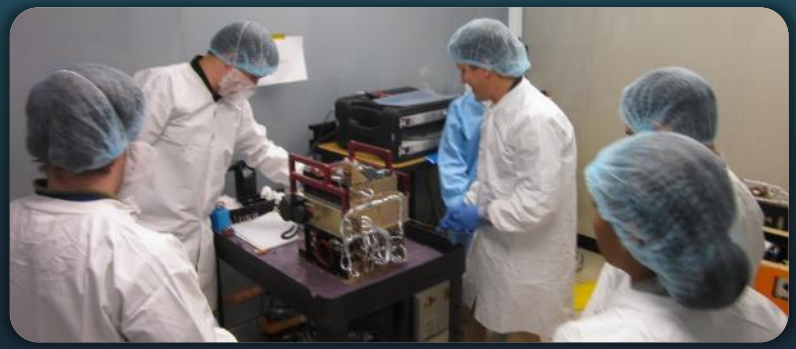
Who are we?

Science Data Processing Branch: Embedded Processing Group (EPG) Specializes in Embedded Development

- Hardware acceleration of algorithms and applications
- Intelligence, autonomy, and novel architectures
- Flight software integration for development platforms
- Advanced architectures and research platforms

Advanced Platforms for Spaceflight

- SpaceCube v2.0 and v2.0 Mini
- SpaceCube v3.0 and v3.0 Mini
- SpaceCube Mini-Z and Mini-Z45
- SC-LEARN and supporting interface cards



Key Tools and Skills

- **Flight Software**: core Flight System (cFS)[1], driver integration, flight algorithms
- **Ground Support Equipment (GSE)**: COSMOS, GMSEC, system testbeds
- **FPGA Design**: Hardware acceleration, fault-tolerant structures
- **Mission Support**: Supporting flight cards, algorithm development
- **On-board Autonomy and Analysis**: deep-learning and machine-learning frameworks, unique architectures

SpaceCube v2.0[2]

[1]2020 NASA Software of the Year (https://github.com/nasa/cFS)
[2]2020 NASA Government Invention of the Year Runner-Up

What is SpaceCube?

NASA SpaceCube

A family of NASA developed space processors that established a hybrid-processing approach that provides a **blend of the best advantages** of both commercial and radiation-hardened technologies to yield unparalleled next-generation systems

Merits of approach recognized by peers with Award for **2020 NASA Government Invention of the Year Runner-Up** for SpaceCube v2.0

Flown 11 systems in space to date

Heritage

SpaceCube v1.0

STS-125, MISSE-7, STP-H4, STP-H5, STP-H6

SpaceCube v1.5

SMART (ORS)

SpaceCube v2.0-EM

STP-H4, STP-H5

SpaceCube v2.0-FLT

RRM3, STP-H6 (NavCube)

SpaceCube v2.0 Mini

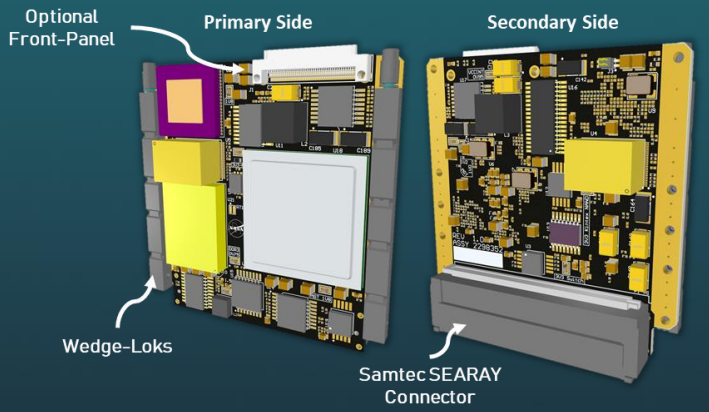
STP-H5, UVSC-GEO

What is CubeSat Card Specification (CS^2)?

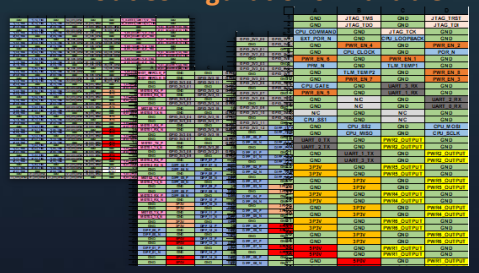
- **Motivations**: Standard or Template is suggested for new designs to allow for **flexibility and interoperability** enabling engineers to **mix-and-match** varying designs to construct new system

- **Challenge**: Reduce constant mission-specific **redesign of one-off cards**, establish baseline configurations to allow compatible 1U-type cards across multiple programs, and address concerns not met by existing card standards

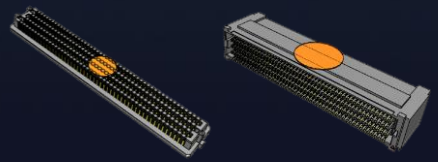
- **Solution**: CS^2 establishes common interface between CubeSat cards, encourages design reuse, and provides **convenient reference** to integrate with mechanical structures supported by SpaceCube family of designs



200-pin and 400-pin Connector Pinout Configurations Available



Example Wedge-Lok
(courtesy nVent SCHROFF)



Model of 400 Pin Connectors Backplane (Left) / Card (Right)
(courtesy Samtec)

What is the Google Coral Edge TPU?

- Edge TPU is a small, **low-power ASIC** designed to provide high-performance neural-net inferencing developed by Google Research
- Edge TPU is flexible design that supports general-purpose AI applications using the **open-source TensorFlow Lite API**, making it widely accessible for application development
- Includes **built-in safety features** such as automated frequency throttling at high temperatures, which is necessary for survival of the device in space environment
- Edge TPU has **extended operating** temperature range (– 20˚C to 70˚C)
- Systolic array architecture

Edge TPU Accelerator Module

Images Courtesy Coral.AI

https://coral.ai/products/accelerator-module/

Motivations, Challenges, Goals

Motivations

Substantial commercial investment of applied AI is demonstrated in **numerous terrestrial applications**

Advances in AI algorithms and custom accelerator electronics can also be harnessed in **space domain**

Small, low-power **AI microchip architectures** are attractive for space missions

Challenges

For terrestrial applications, datacenters with server-grade CPUs and GPUs **are available** for advanced deep learning

Using state-of-the-art artificial intelligence (AI) frameworks onboard spacecraft is challenging because common **spacecraft processors are performance limited**

Goals

Harness application-specific AI chips for high-performance and power-efficient AI applications

Enable breakthrough capabilities including autonomous constellation management, reactive health and status monitoring, and responsive, **onboard data analysis**

AI for Science and Defense

Broad applications and needs for BOTH Science and Defense missions highlighted in guiding documents and studies

Science

- NASA 2017 Strategic Technology Investment Plan
- NASA Technology Taxonomy 2020
- 2015 NASA Technology Roadmaps
- Visions into Voyages (Planetary Science decadal survey)
- Thriving on Our Changing Planet (Earth science decadal survey)

Onboard Intelligence For Space Missions!

Defense

- DARPA Blackjack
- Air Force Space Command Long-Term Science and Technology Challenges
- National Geospatial-Intelligence Agency SmallSat Keynote

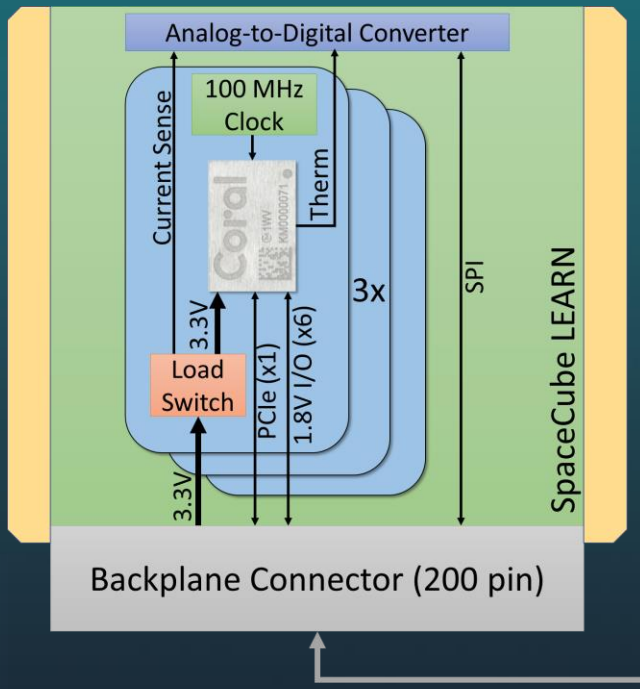
SpaceCube LEARN

SC-LEARN is designed to act as a **co-processor** to expand capabilities of NASA's existing high-performance space processors

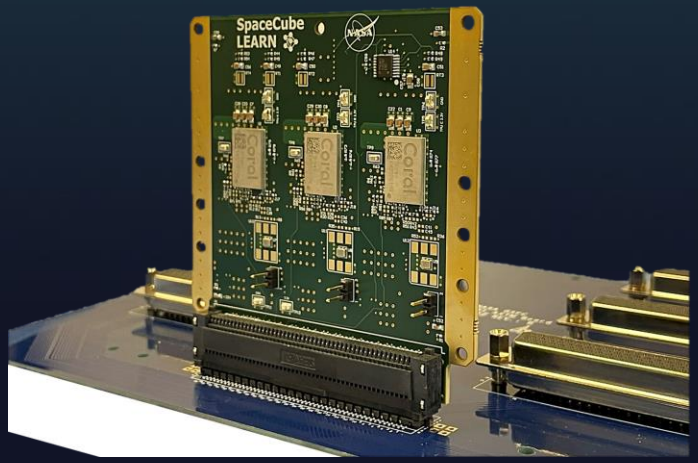
SC-LEARN features **three** Edge TPU Accelerator Modules in 1U CubeSat form-factor

Accelerator Modules are powered by three **independent rad-hard load switches**, which are controlled by host processor

Load switches incorporate **current sense amplifiers** whose output is monitored by onboard rad-hard analog-to-digital (ADC) converter



SpaceCube v3.0 MINI



Operational Modes

High-Performance Mode

Multiple Accelerator Modules can be used cooperatively to execute operations in parallel to dramatically improve performance over single-node design

Fault-Tolerant Design Mode

- Use of physical-hardware Triple-Modular-Redundancy (TMR)
- Mode in which output of three replicas of device are run through majority voter for fault masking

Power-saving Mode

- SC-LEARN design benefits from individual load switches for each Edge TPU accelerator
- Can operate in lower power mode state when two of three Edge TPUs are depowered allowing for cold sparing of system

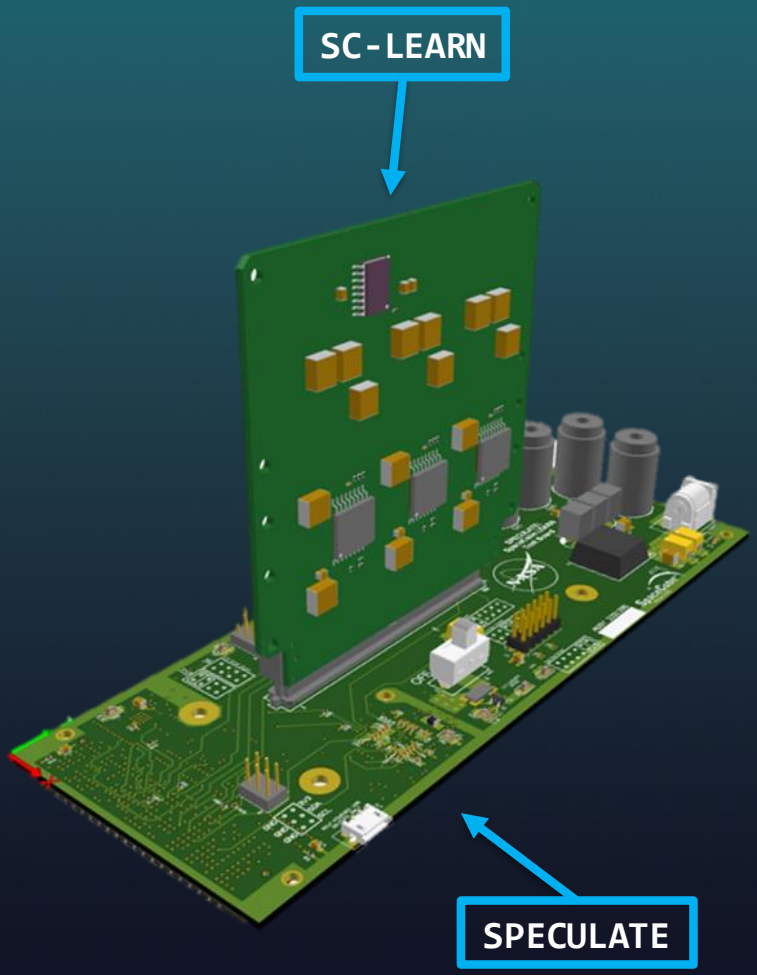
SC-LEARN Evaluation Board (SPECULATE)

For ground-based testing, SC-LEARN connects to SPECULATE (SPacE CUbe LeArn TEst) board with standard interfaces for **rapid desktop prototyping**

SPECULATE provides power to SC-LEARN and interfaces to **multiple host FPGA processors**, most notably SpaceCube v3.0 Mini

FMC connector is main interface to host FPGA board, including PCIe, USB 2.0, and multiple IO control signals for Edge TPUs on SC-LEARN

SPECULATE can be powered through **several options** including FMC card, banana jacks, or standard 12V wall wart connection



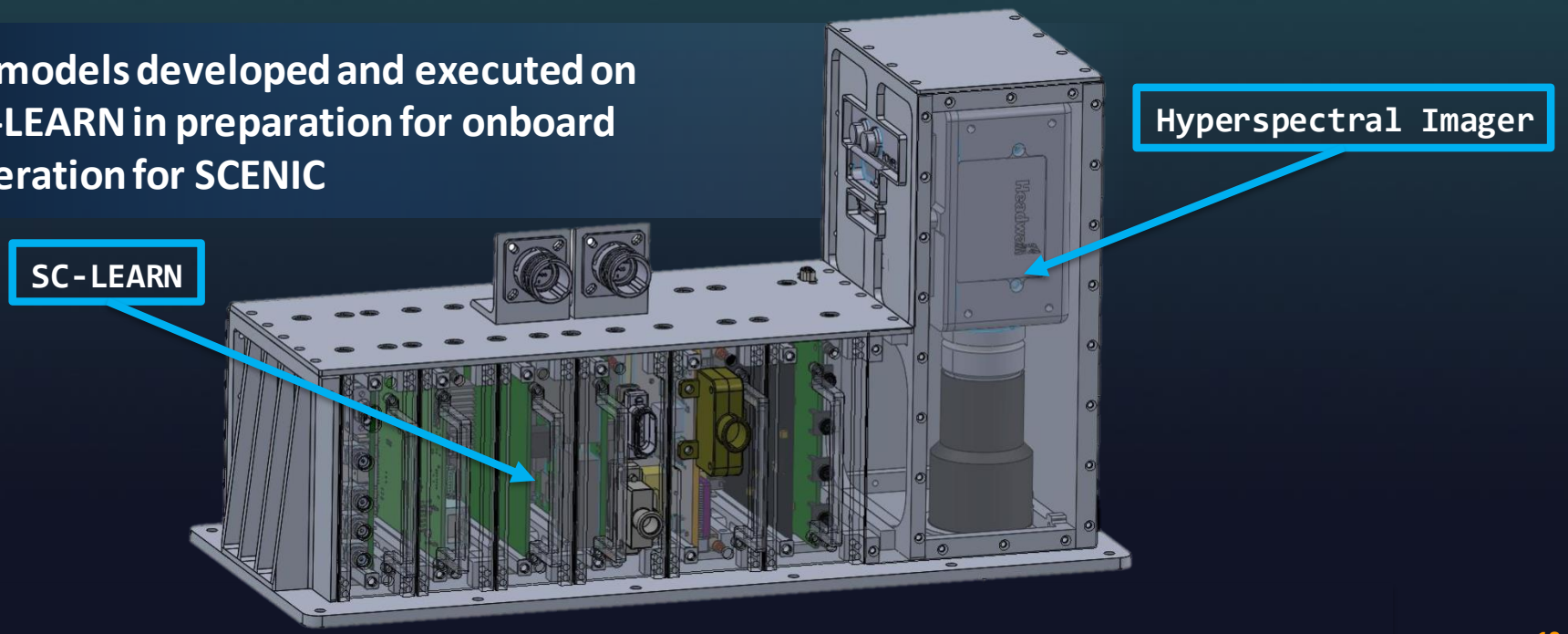
Flight Demo: STP-H9-SCENIC

Space Test Program – Houston 9 (STP-H9)
SpaceCube Edge Node Intelligent Collaboration (SCENIC)

ISS-based testbed to evaluate AI/machine learning technology on FPGA and custom AI microchip platforms in space (TPU, DPU, Myriad X)

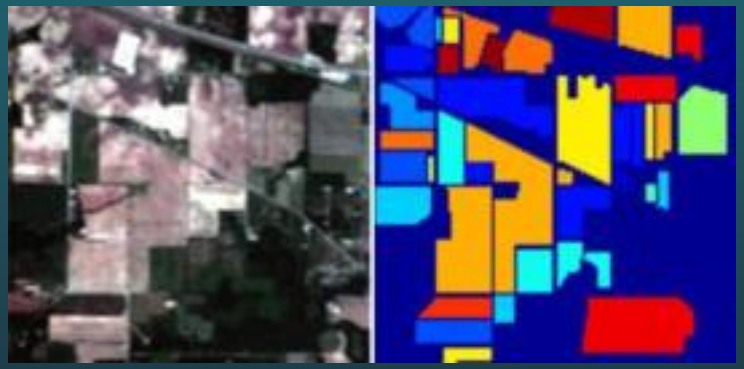
Collaboration w/ AFRL & Aerospace Corp.

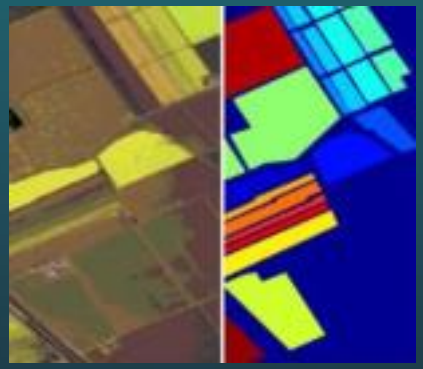
AI models developed and executed on SC-LEARN in preparation for onboard operation for SCENIC



Datasets and Test Vectors

Indian Pines | Salinas | Pavia University



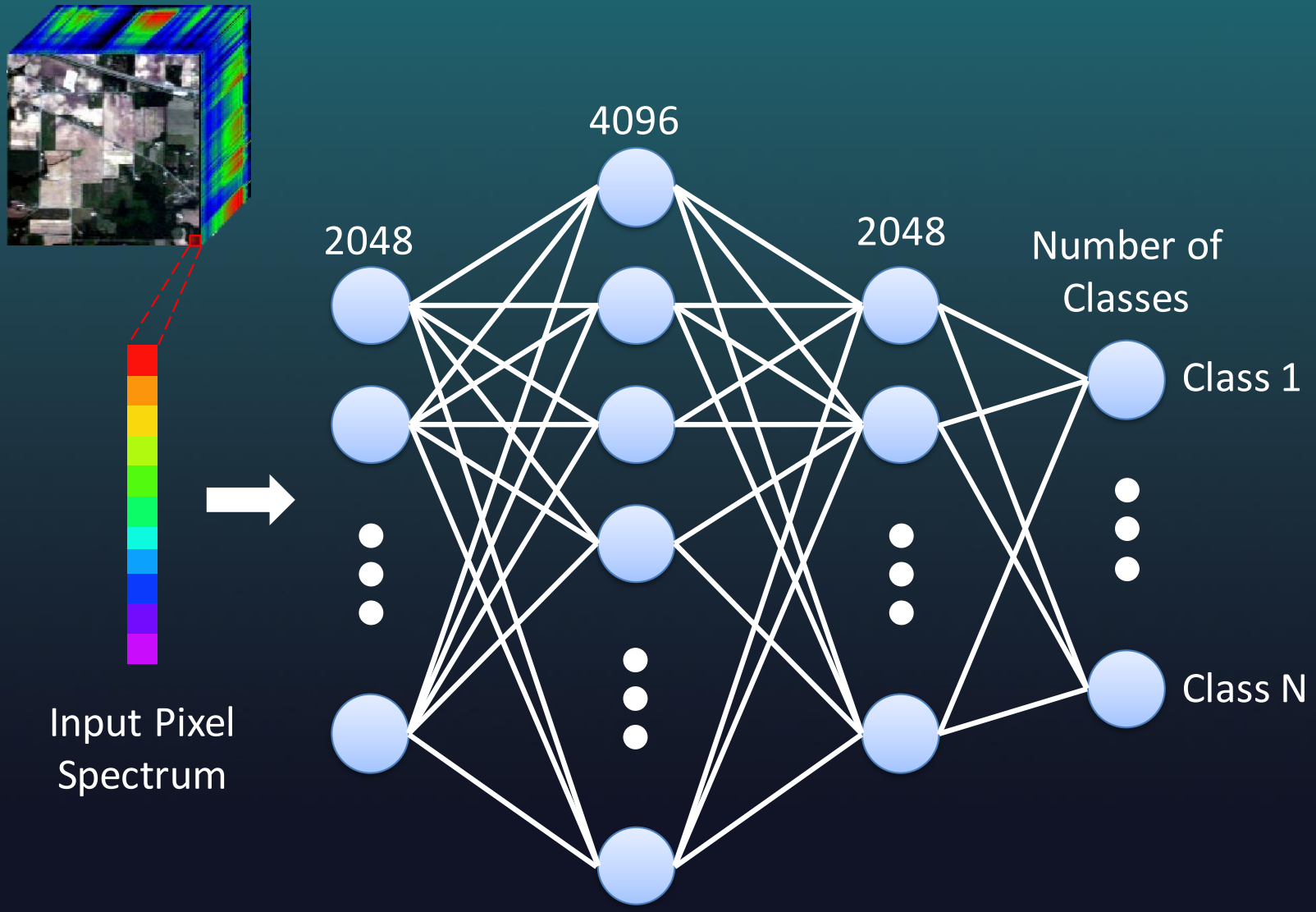


- Normalized on per-band basis: $I_{norm} = \frac{I - \min(I)}{\max(I) - \min(I)}$

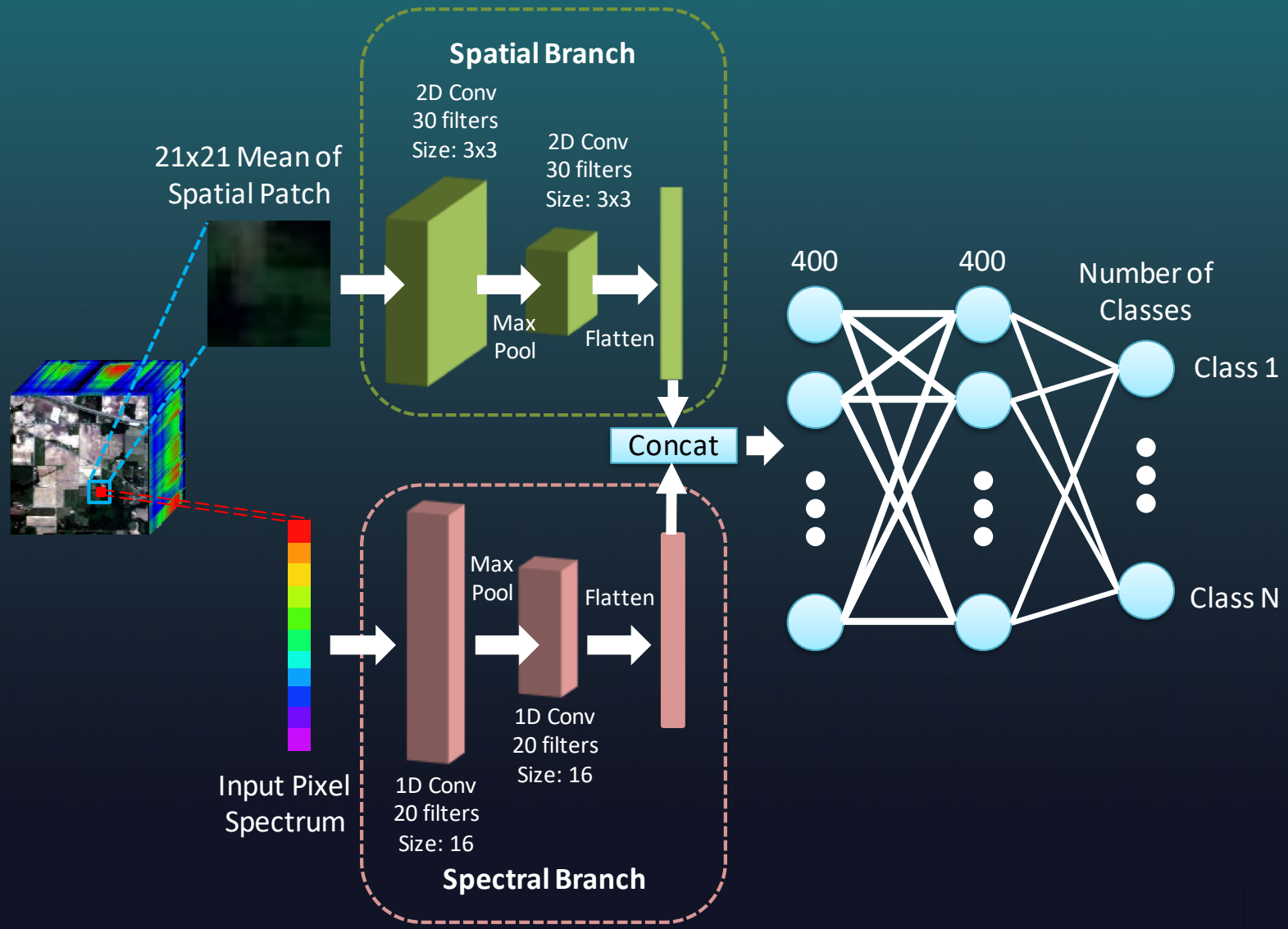
Dataset	Sensor	Spatial Dimensions	Spectral Bands	Sensitive Wavelengths	Classes	Labeled Pixels	GSD
Indian Pines	AVIRIS	145x145	224	0.4-2.5 µm	16	10,249	20 m
Salinas	AVIRIS	512x217	224	0.4-2.5 µm	16	54,129	3.7 m
Pavia University	ROSIS	610x610	103	0.43-0.85 µm	9	50,232	1.3 m

Datasets available online and images provided courtesy: http://www.ehu.eus/ccwintco/index.php/Hyperspectral_Remote_Sensing_Scenes

Hyperspectral Models: Multi-Layer Perceptron (MLP)



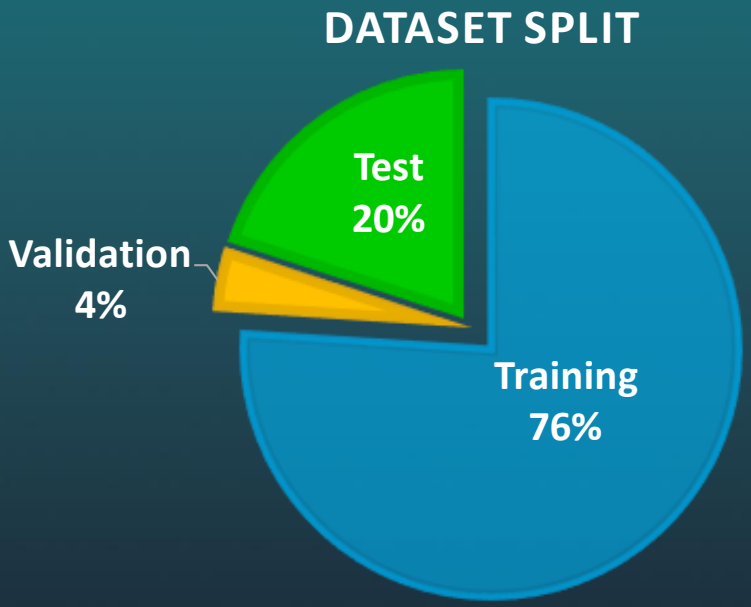
Hyperspectral Models: Spectral Spatial Convolutional Neural Network (SS-CNN)



Training and Quantization Methods

Training

Both MLP and SS-CNN models were trained on the Salinas, Indian Pines, and Pavia University datasets using **Adam optimizer** in **TensorFlow/Keras** framework



Quantization

While training process used 32-bit floating-point (FP32) data types for all weights and tensors, Edge TPU can only operate on quantized **8-bit integer (INT8)** weights and tensors

TensorFlow Lite converter quantizes weights and tensors, converting FP32 to INT8 values, and vice versa, via:

$$Value_{FP32} = (Value_{INT8} - z_0) * s$$

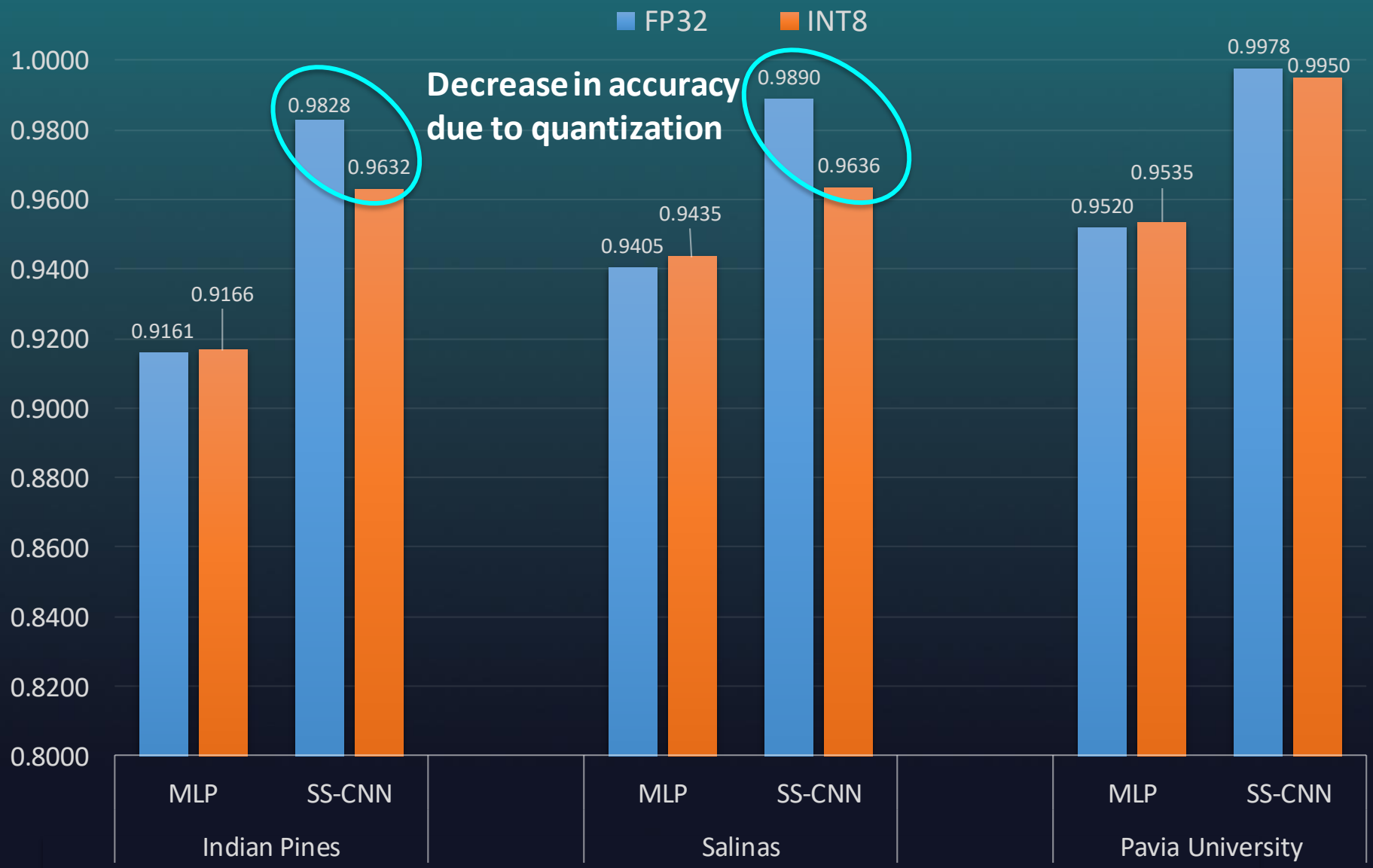
Must provide **representative dataset** to optimize z_0 and s to limit accuracy degradation

Comparison of Model Complexity

Model	Dataset	# trainable parameters	On-Chip Memory for Caching Parameters	Off-Chip Memory for Streamed Parameters
MLP	Indian Pines	17,244,176	536.25KiB	16.02MiB
MLP	Salinas	17,244,176	536.25KiB	16.02MiB
MLP	Pavia U	17,031,177	344.25KiB	16.02MiB
SS-CNN	Indian Pines	948,106	3.27MiB	320.00B
SS-CNN	Salinas	948,106	3.27MiB	320.00B
SS-CNN	Pavia U	785,299	3.14MiB	320.00B

SS-CNN parameters can fit in on-chip Edge TPU cache, while MLP parameters must be streamed from off-chip memory on host

Training and Quantization Results



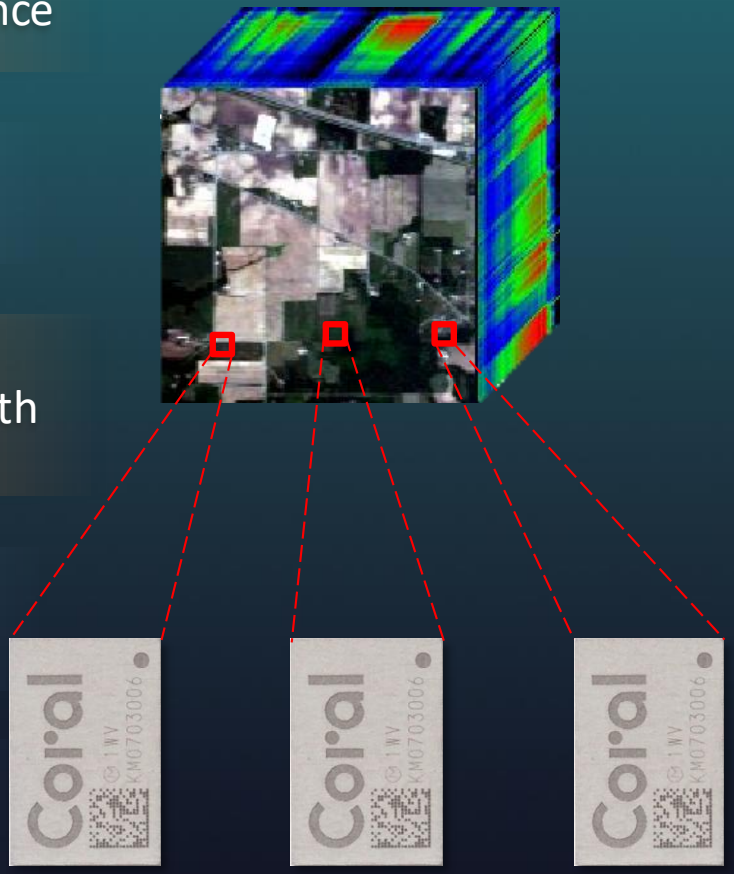
Execution Study Overview

SC-LEARN Parallel-processing Configuration Performance

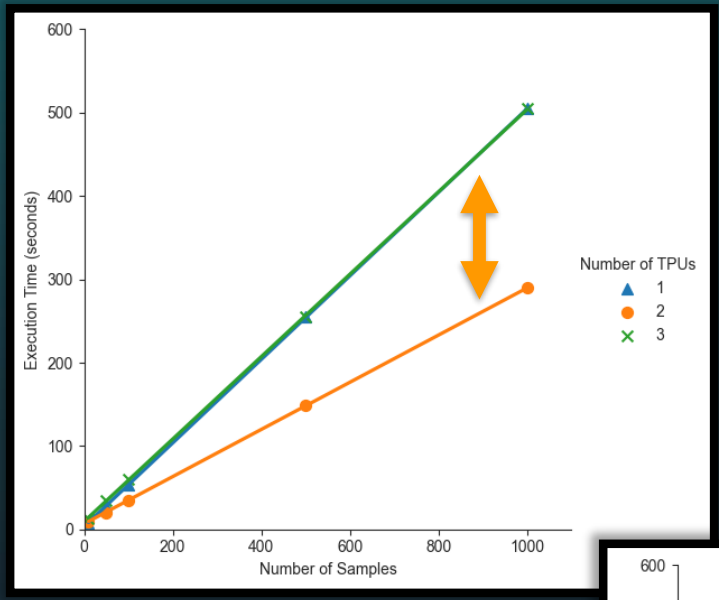
- Multi-threaded application was developed to perform inference on varying number of Edge TPUs

Application was executed on increasing number of samples to examine how the execution time scaled with expanding amounts of data

- **Single Edge TPU case**: Inference was performed on samples for a baseline comparison
- **Multiple Edge TPU case:** Threads spawned corresponding to number of available Edge TPUs with samples split evenly across them for inference

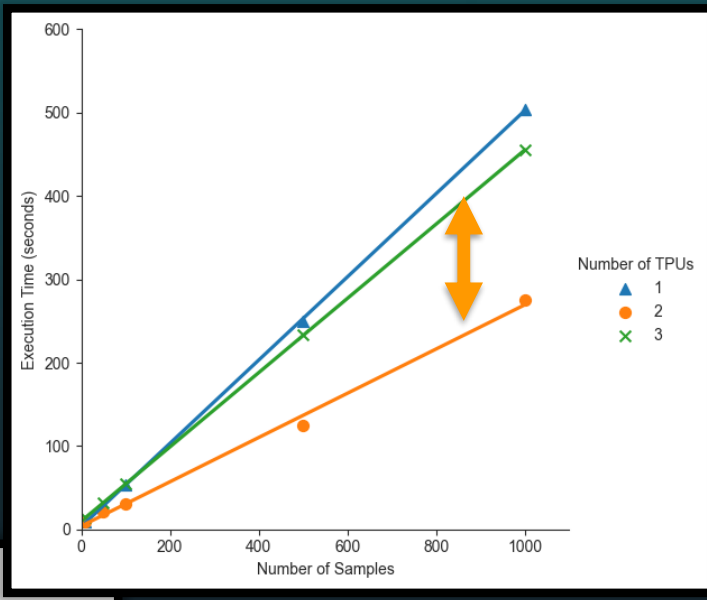


Execution Study: MLP Results



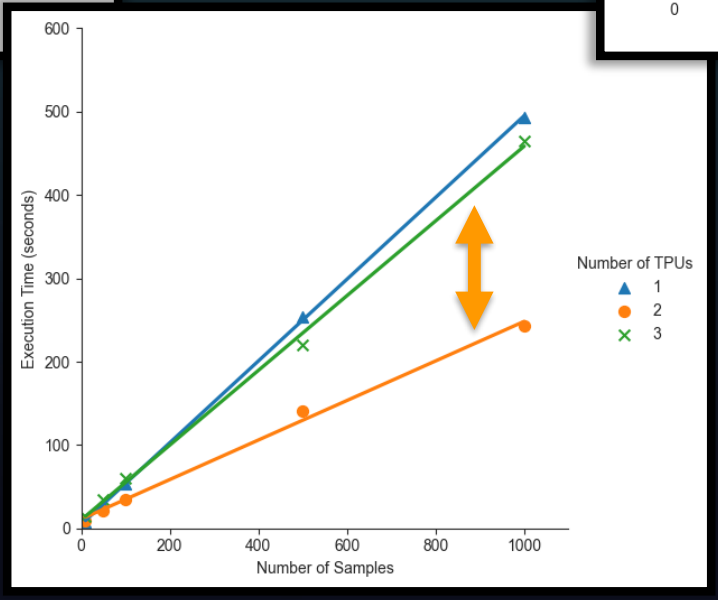
Indian Pines

Use of two Edge TPUs is only slightly slower than one Edge TPU for small number (<50) of samples



Salinas

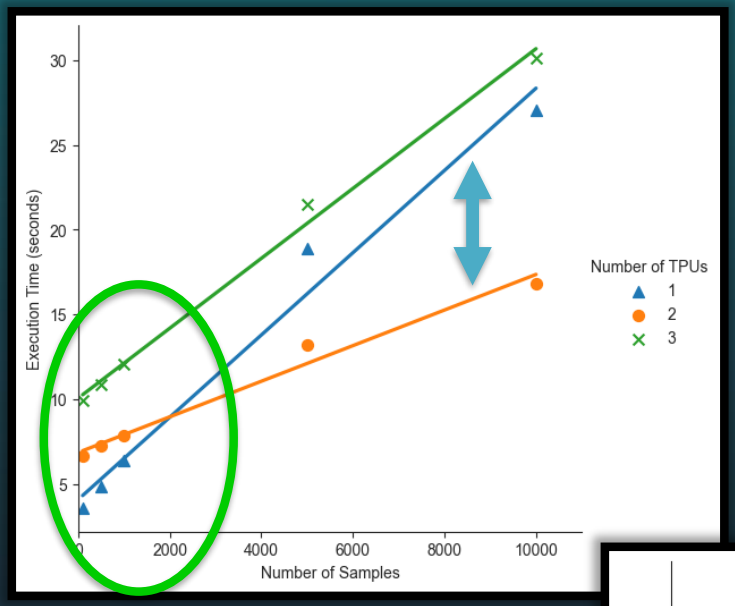
As number of samples increases beyond 500, speedup approaches near linear scaling, executing around twice as fast using two Edge TPUs compared to one



Pavia University

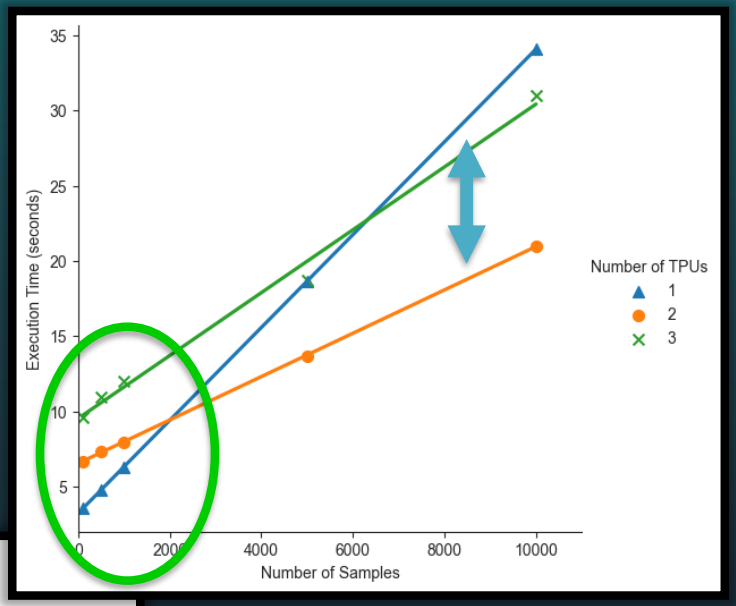
Upon adding third Edge TPU, dramatic decrease in performance is observed

Execution Study: SS-CNN Results



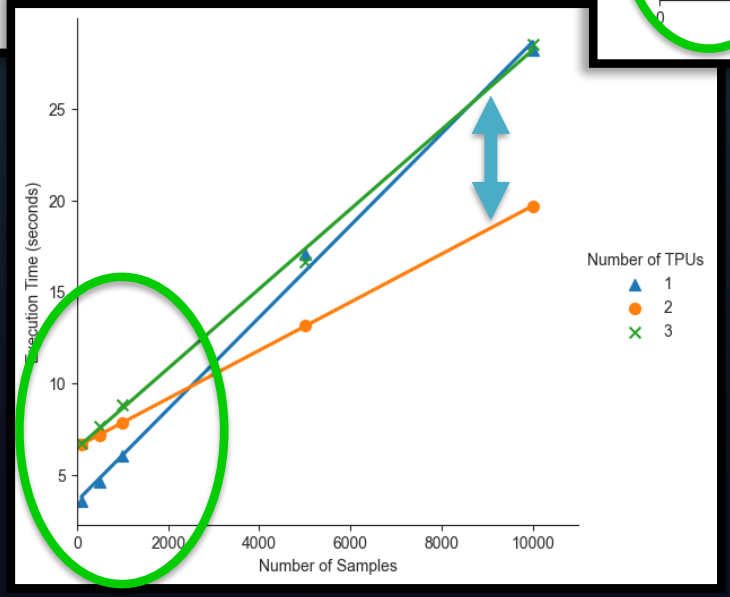
Indian Pines

SS-CNN executes faster than MLP model, since SS-CNN parameters can fit in Edge TPU's cache while MLP parameters cannot



Salinas

One Edge TPU is substantially faster than two Edge TPUs for smaller number of samples (less than approximately 2000)



Pavia University

As number of samples increases beyond ~2000, benefit from distributing the data across two Edge TPUs outweighs overhead associated with spawning two threads

Future Work

Radiation testing in collaboration with NASA Electronic Parts and Packaging Program (NEPP)

Perform power characterization of SC-LEARN for different AI models

Quantization-aware Training

- Quantization nodes are inserted into training graph of AI model to simulate noise effects of quantization
- Model can learn to be resilient to quantization noise

Fault-aware Training

- Mitigate the radiation effects of the space environment

Transfer Learning

- Use knowledge learned from training on one task with large dataset to solve task on target dataset with limited training data

Future Opportunity: DAVINCI+/CUVIS

Deep Atmosphere Venus Investigation of Noble-gases, Chemistry and Imaging
Compact Ultraviolet to Visible Imaging Spectrometer (CUVIS)

CUVIS will employ advanced optical systems and innovative artificial intelligence/deep learning (AI/DL) hardware and software for on-board data processing for rapid identification of science results (Edge AI)

Modified SC-LEARN to Enable NASA Science!

Conclusion

*SC-LEARN is a **MISSION ENABLING** technology*

Delivers exceptional AI computational capabilities in small, low-power form factor

CubeSat Card Standard (CS^2) provides flexibility and interoperability to mix-and-match varying designs to construct new system

Multiple operational modes allows system designers to meet performance and reliability requirements

STP-H9-SCENIC will allow for deployment of hyperspectral models for onboard data processing in realistic mission scenario

Thank you! Questions?

Contact Us

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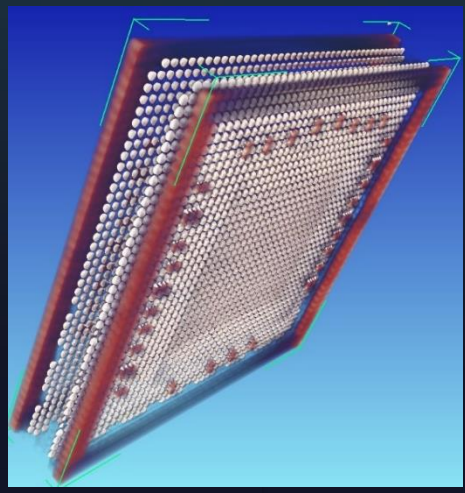
CATALOG APPENDIX

SpaceCube v2.0 Processor Card

Overview

- TRL9 flight-proven processing system with unique Virtex **back-to-back** installed design methodology
- **3U cPCI** (190 mm × 100 mm) size
- Typical power draw: 8-10W
- 22-layer, via-in-pad, board design
- IPC 6012B Class 3/A compliant

Back-to-Back FPGA Design



High-Level Specifications

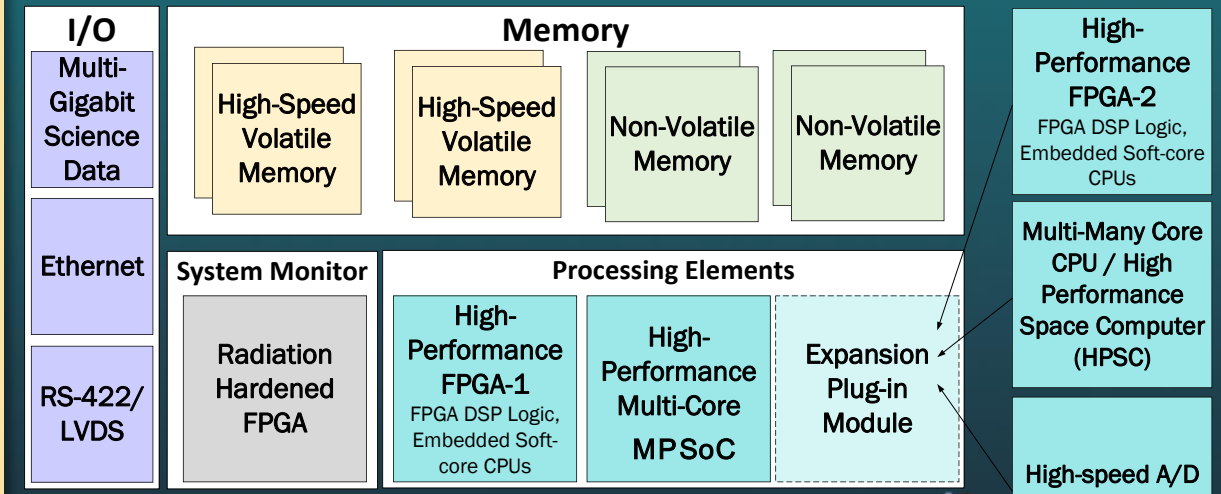
- 2x Xilinx Virtex-5 (QR) FX130T FPGAs (FX200T Compatible)
- 1x Aeroflex CCGA FPGA
  - Xilinx Configuration, Watchdog, Timers
  - Auxiliary Command/Telemetry port
- 4x 512 MB DDR SDRAM
- 2x 4GB NAND Flash
- 1x 128Mb PROM, contains initial Xilinx configuration files
- 1x 16MB SRAM, rad-hard with auto EDAC/scrub feature
- 16-channel Analog/Digital circuit for system health
- Mechanical support for heat pipes and stiffener for Xilinx devices
- External Interfaces
  - Gigabit interfaces: 4x external, 2x on backplane
  - 12x Full-Duplex dedicated differential channels
  - 88 GPIO/LVDS channels directly to Xilinx FPGAs
- Debug Interfaces
  - Optional 10/100 Ethernet interface

SpaceCube v3.0 Processor Card

Overview

- **Next-Generation** SpaceCube Design
- **3U SpaceVPX** Form-Factor
- Ultimate goal of using High-Performance Spaceflight Computing (**HPSC**) paired with the high-performance FPGA
  - HPSC will not be ready in time for the prototype design
  - Special FMC+ Expansion Slot

SpaceCube v3.0 Architecture



High-Level Specifications

1x Xilinx Kintex UltraScale

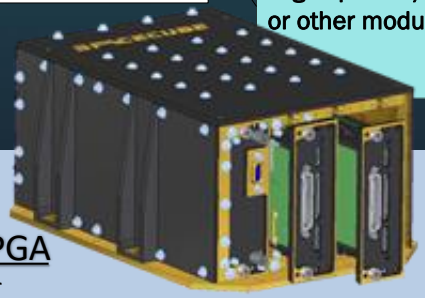
- 2x 2GB DDR3 SDRAM (x72 wide)
- 1x 16GB NAND Flash
- External Interfaces
  - 24x Multi-Gigabit Transceivers
  - 75x LVDS pairs or 150x 1.8V single-ended I/O
  - 38x 3.3V single-ended I/O,
  - 4x RS-422/LVDS/SPW
- Debug Interfaces
  - 2x RS-422 UART / JTAG

1x Xilinx Zynq MPSoC

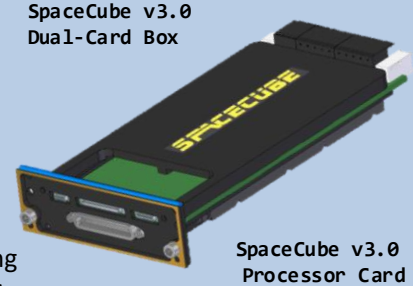
- Quad-core Arm Cortex-A53 processor (1.3GHz)
- Dual Arm R5 processor (533MHz)
- 1x 2GB DDR3 SDRAM (x72 wide)
- 1x 16GB NAND Flash
- External Interfaces
  - I2C/CAN/GigE/SPIO/GPIO/SPW
  - 12x Multi-Gigabit Transceivers
- Debug Interfaces
  - 10/100/1000 Ethernet (non-flight)
  - 2x RS-422 UART / JTAG

Rad-Hard Monitor FPGA

- Internal SpaceWire router between Xilinx FPGAs
- 1x 16GB NAND Flash
- Scrubbing/configuration of Kintex FPGA
- Power sequencing
- External Interfaces
  - SpaceWire
- 2x 8-channel housekeeping A/D with current monitoring



SpaceCube v3.0 Dual-Card Box



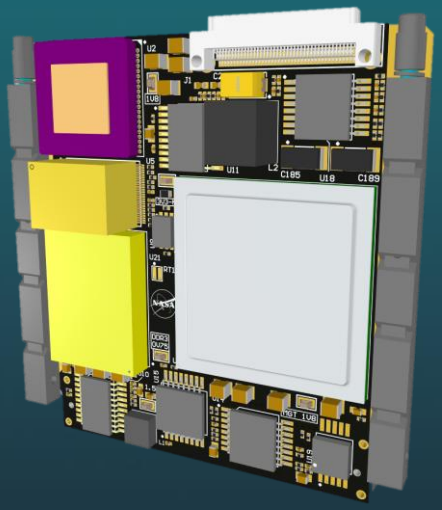
SpaceCube v3.0 Processor Card

SpaceCube v3.0 Mini Specification

Overview

- Apply **SpaceCube design approach** to provide next-generation processor in **CubeSat form-factor**
- Maintain compatibility with SpaceCube v3.0
- High-performance processor of Goddard's modular CubeSat spacecraft bus MARES
- Evaluation board available with common interfaces for rapid prototyping and debug
- Conforms to CubeSat Card Standard (CS^2)

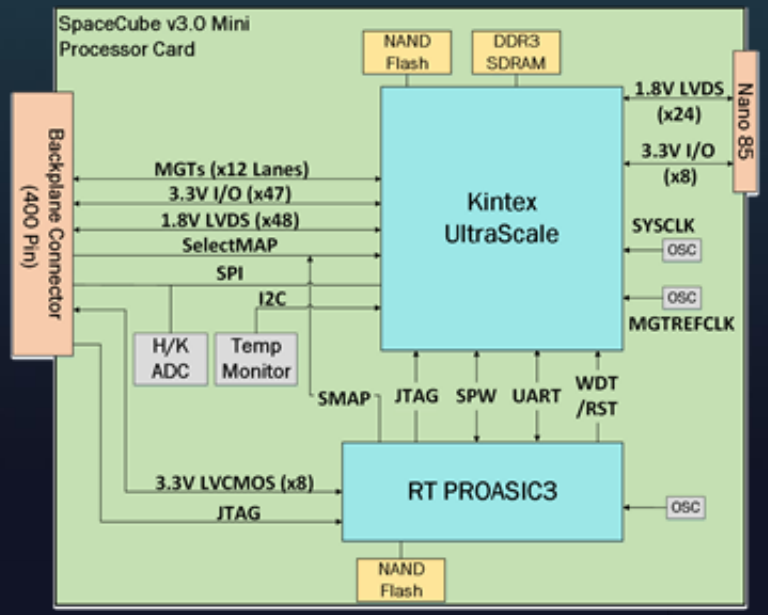
[CS]²



High-Level Specifications

Xilinx Kintex UltraScale

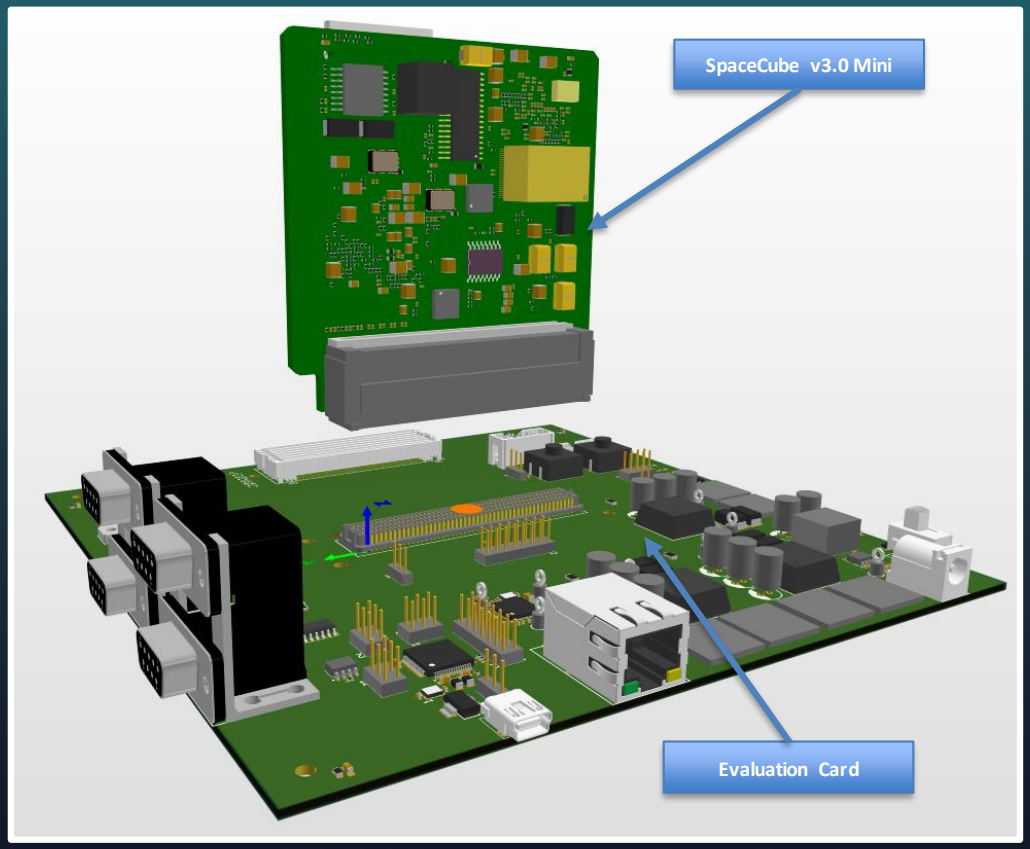
- 1x 2GB DDR3 SDRAM (x72 wide)
- 2x 16GB NAND Flash
- Radiation-Hardened Monitor
- External Interfaces
  - 12x Multi-Gigabit Transceivers
  - 48x LVDS pairs or 96x 1.8V single-ended I/O
  - 48x 3.3V GPIO
  - SelectMAP Interface
  - (Front Panel) 24x LVDS pairs or 48x 1.8V single-ended I/O
  - (Front Panel) 8x 3.3V GPIO
- Debug Interfaces
  - 2x RS-422 UART (external transceivers)
  - JTAG



SpaceCube Mini Active Eval Kit

Overview

- Provides **easy development platform** to support SpaceCube v3.0 Mini rapid prototyping and design
- Includes several common interfaces for programming and debug
- Incorporates FMC+ Connector to support future Mezzanine and commercial vendor designs



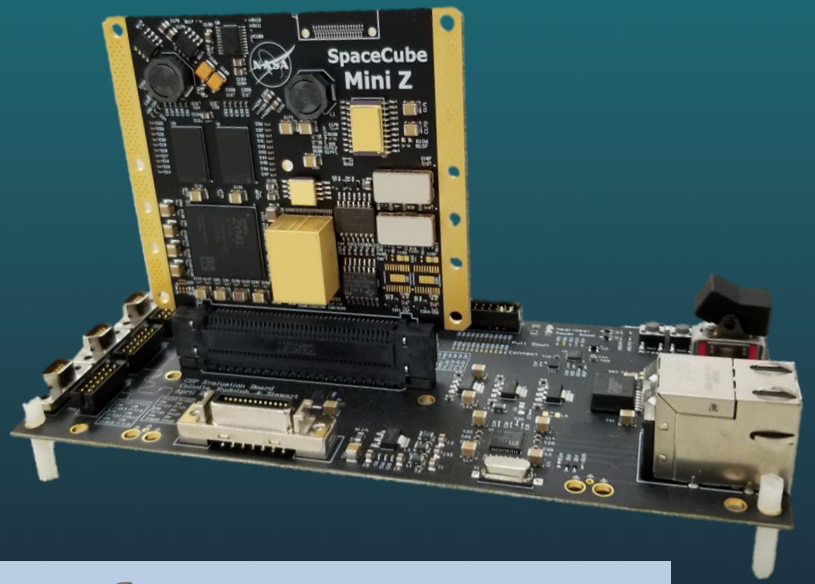
High-Level Specifications

- Gigabit Ethernet (RJ45/SGMII)
- USB Debug / JTAG
- JTAG headers - Xilinx and Microsemi
- SelectMAP programming header
- 2 SpaceWire ports
- 4 RS422 ports
- FMC+ Connector
  - 11 Multi-Gigabit Transceivers
  - 46x LVDS or 92x 1.8V GPIO
  - 22x 3.3V GPIO

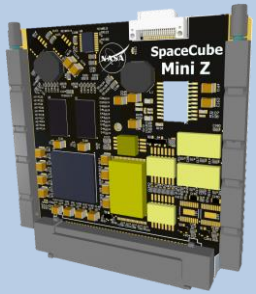
SpaceCube Mini-Z Specification

Overview

- **Re-envisioned and upgraded** version of popular CSPv1 design collaboratively developed between NASA GSFC and NSF CHREC
- Supports additional IO and form-factor changes to maintain compliance with MARES (GSFC's SmallSat bus) architecture



High-Level Specifications



Processing Capability

- Processing System (PS)
  - Xilinx Zynq-7020 SoC with Dual-Core ARM Cortex-A9 up to 667 MHz
  - 32KB I/D L1 Cache per core
  - 512KB L2 Cache
  - 256KB OCM
  - NEON SIMD Single/Double Floating Point Unit per core
- Programmable Logic (PL)
  - 85K Logic Cells
  - 53,200 LUTS /106,400 FF
  - 220 DSPs
  - 4.9Mb BRAM

Storage

- 1GB DDR3 SDRAM
- 4GB NAND Flash

IO

- MIO
  - 26 single-ended configurable IO into common interfaces such as UART, SPI, CAN, and I2C
- EMIO
  - 24 differential pairs and 12 single-ended IO
- Front Panel
  - 12 differential pairs

Dev. Tools

- CSP Evaluation Board
  - JTAG programming support
  - 10/100 Ethernet
  - MIO and EMIO breakout
  - 3 SpaceWire breakouts
  - Camera Link breakout
- USB-UART Board
  - USB to UART Converter

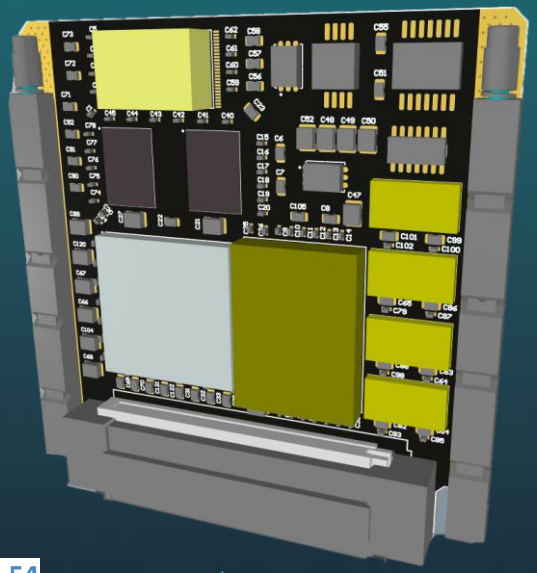
Physical Dimensions

- ~82g, 620 mil thick
- <1U CubeSat form factor
- 1.6-3.6W (FPGA load dependent)

SpaceCube Mini-Z45 Specification

Overview

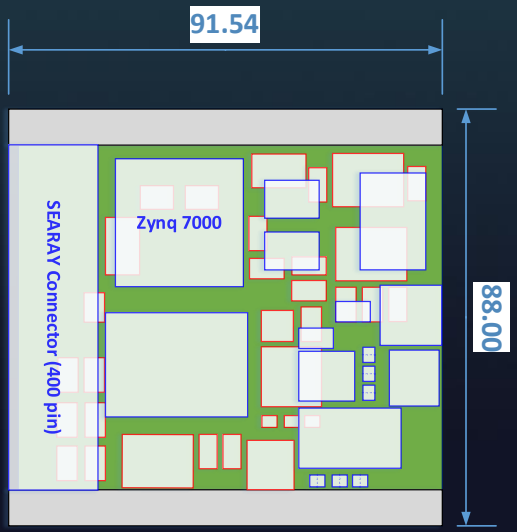
- Apply **SpaceCube design approach** to provide next-generation processor in **CubeSat form-factor**
- Maintain compatibility with SpaceCube v3.0 Mini and Mini-Z designs
- **Upgrade** capabilities of Mini-Z (CSPv1) to provide MGTs, more FPGA resources and more memory



High-Level Specifications

<u>1x Xilinx Zynq 7000 System-on-Chip</u>

- 1GB DDR3 SDRAM for ARM Processors
- 2GB DDR3 SDRAM for Programmable Logic
- 16GB NAND Flash
- Radiation-Hardened Watchdog
- External Interfaces
  - 8x Multi-Gigabit Transceivers
  - 31x LVDS pairs or 62x single-ended I/O (voltage selectable)
  - 28x Single-ended PS MIO
- Debug Interfaces
  - 1x RS-422 UART (external transceivers)
  - JTAG



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Acronyms

Acronym	Definition
AXI	Advanced eXtensible Interface
cFS	Core Flight System
CGND	Chassis Ground
cPCI	Compact PCI
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check
CS2	CubeSat Card Standard
DSP	Digital Signal Processor
DTN	Disruption Tolerant Network
EM	Engineering Model
EPG	Embedded Processing Group
FF	Flip Flop
FLT	Flight
FMC	FPGA Mezzanine Card
FPGA	Field Programmable Gate Array
FSM	Finite State Machine
GEO	Geostationary Earth Orbit
GMSEC	Goddard Mission Services Evolution Center
GND	Ground
GOPS	Giga-operations per second
GPIO	General Purpose IO
GSE	Ground Support Equipment
IMPS	Intelligent Multi-purpose System
LEO	Low Earth Orbit
LVDS	Low-voltage differential signaling
LVPC	Low-Voltage Power Converter
MGT	Multi-Gigabt Transciever
MPSoC	Multiprocessor system on a chip
ORS	Operationally Responsive Space
PCB	Printed Circuit Board
RST	Reset
SC	Spaceube
SMAP	Select Map
SoC	System on Chip
STP	Space Test Program
TMR	Triple Modular Redundancy
TTE	Time Triggered Ethernet
UVSC	Ultraviolet Spectro-Coronagraph
WDT	Watchdog Timer