Ultra-low Power ADCs for Space Sensors and Instruments

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***Abstract*—A 28nm 0.1V 10-bit 2kS/s time domain ADC design is proposed. This design opens the doors to both low supply and low power space sensors and instruments. Due to the stringent voltage supply, unique challenges arise that are met with innovation in the sample switch and the quantizer design. These components of the ADC architecture are optimized to perform successfully at a 0.1V supply with a sample rate suitable for most sensor applications.**

***Index Terms*—ADC, TDC, Sub-threshold, low-power, low-voltage, wireless sensor networks**

I. Introduction

A. Space Sensors and Instruments

As technology improves it becomes more viable to connect devices and understand the world better. As data communication technology improves, an increasing number of devices will become connected to satisfy the demands for data [1]. Many large and costly sensors can now be replaced with smaller, more cost effective sensors that communicate as a network. Each smaller sensor can gather data and collaborate with neighboring devices to complete a dataset of any environment [2]. These sensors are usually created using a microcontroller, an energy source, a transmitter, and sensing electronics that can interface with the environment that surrounds them.

These small sensor networks can be deployed in a variety of conditions. In Earth's atmosphere, an entire network can monitor global weather conditions to update a ground station. On exploration missions, a planet's surface could be monitored in multiple locations to provide a clearer picture of a planet's condition as shown in Fig. 1 [5]. Any way they're deployed, they can help paint a better picture of places out of reach.

Small, low power sensors can also be used in other space instruments that require great power efficiency. These types of sensors have already been successfully used to monitor body vital conditions and could easily be incorporated into space suits, rover equipment, or other reconnaissance devices [3], [4]. Information on long range missions is crucial, and the instruments that provide this data should be used wherever possible to make the most of costly exploration and surveillance missions.

Each of these applications benefit from a system's ability to use power efficiently while providing needed information. Existing systems need to have their components optimized to preserve power and operate for as long as possible with a given energy source.

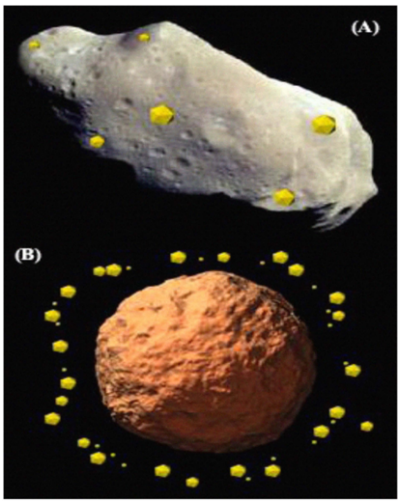

Fig. 1: Two methods of low-power sensor deployment, on surface and in orbit [5].

B. ADCs in Sensors and Instruments

Every sensor that interfaces with the natural world needs to have an Analog-to-Digital converter (ADC) to quantize the element that is being monitored. This device needs to translate an analog element, such as temperature, pressure, or light intensity, into a digital output that represents the original analog quantity. This data can then be transmitted to a receiver to be processed and analyzed.

The energy source for these small sensors is commonly an energy harvester or limited battery [6]. In either case,

the power consumption requirements are very strict. Whether the energy source is a battery or a low voltage energy harvester, it is crucial that the ADC's power consumption is as low as possible. The ADC also needs to have a sample rate of around 1-2kHz to properly function for sensing applications. We propose a 10-bit ADC that can operate at an ultra-low supply voltage of 0.1V with a sample rate that meets the requirements for space sensors and their applications.

II. ADC Design

To meet the needs for low power consumption and high resolution we chose to use a time domain based ADC. This architecture is simple and very power efficient. It has many variations and we will leverage it's strengths to meet our design requirements. The subsequent section describes its basic operation.

A. Standard Time Domain based ADC Architecture

A time domain ADC is constructed using four main components. First, a switch samples the input and holds its value for evaluation. This sampled value acts as an input to a time based circuit. This process models a voltage-to-time converter (VTC). In our case, we use a ring oscillator which repeatedly swings from rail to rail. This period of oscillation is influenced by the sampled voltage, which allows the ADC to have distinct states that can be detected. These oscillations are then converted to a digital code using a time-to-digital converter (TDC).

For our ADC, this is done by keeping track of the number of times that the ring oscillator fully returns to its original phase. The phase is also tracked by recording the initial and final states of the ring oscillator. A 10 phase example of this phase tracking is shown in Fig. 2. Here, the full rotations from 0 to 2π make up our counting resolution. Then, the progression within a full phase rotation accounts for the difference between initial and final phase. These two metrics define the resolution of states that can be tracked using this ADC topology. Finally, the digital code is translated and serialized to be processed off chip.

B. Proposed SAR Architecture

For this ADC, we plan to take advantage of the scalability of a time domain ADC. As the supply is lowered in a chip design, often the needed sizing of transistors outpaces targeted performance. However, when metrics are moved from the voltage domain to the time domain, scaling becomes much more manageable. For this reason we chose to design a 10-bit differential ADC with time domain interpolation. In order to have high enough

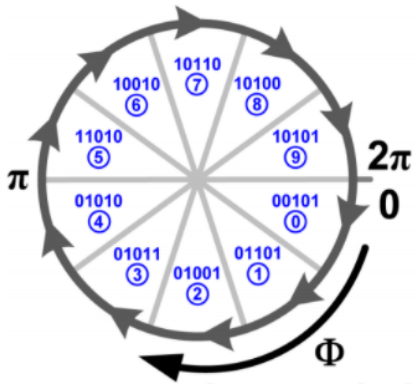

Fig. 2: Phase diagram of a ring oscillator's output.

resolution for sensing applications, we felt that 10-bits would be a appropriate size. The ADC proposed is differential to improve noise performance at the cost of added complexity and size. The ADC will consist of a quadruple bootstrapped sample switch, a VTC, TDC logic, and digital translation logic. Like most recent time domain architectures, clocks will need to be generated for the sample switch and for the TDC/output logic.

C. 0.1V Supply Voltage

As stated before, the time domain based ADC is simple by design and many have successfully lowered the needed supply voltage below the nominal level of 1.8V [7]–[11]. However, in the best of these designs, the supply was lowered to 0.3V. To push these designs even further and in order to reduce power consumption and enable operation of low supply devices we intend to reduce the power supply voltage to 0.1V. This requires an unprecedented design that takes full advantage of modern process technologies such as 28nm fabrication.

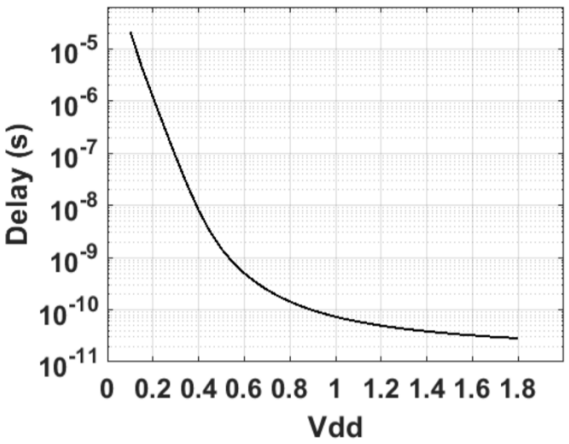

Fig. 3: Inverter delay vs. power supply voltage.

D. Challenges of a Low Power Supply Voltage

Designing an ADC that operates at 0.1V comes with unique problems. At this supply level, transistors conduct very little current. A simple way to illustrate this is to look at inverter delay vs. supply voltage. As seen in Fig. 3, the delay increases exponentially with reduced supply. This creates challenges with the digital logic's rise and fall time. It also creates problems in the sample and hold circuit, making it difficult to charge up the switched-capacitor DAC within the allotted sample time. Simply using an existing design with a 0.1V supply is sure to fail.

Another important consideration is noise power. With the proposed supply voltage and a 10-bit ADC, the least significant bit (LSB) voltage is given by

$$\frac{V_{ref}}{2^{NoB}} = \Delta$$

For our design, that equates to an LSB of 0.195mV. We need to ensure that our noise voltage doesn't surpass the voltage of our LSB, or else our accuracy will be severely reduced. In the subsequent section we will explain several methods that will mitigate aforementioned problems and allow our ADC to operate accurately at 0.1V.

III. Circuit Design

A. Quadruple Bootstrapped Switch

Typically, the sample and hold circuit is implemented using a bootstrapped switch as seen in Fig. 4. This helps tackle problems with linearity and transistor conduction by minimizing changes in resistance of the sampling transistor. During the sample phase, transistors are switched on so that the gate voltage remains constant. During the hold phase, the capacitor is recharged to VDD. For most applications this provides enough linearity to track inputs correctly without introducing unwanted harmonics in the frequency output.

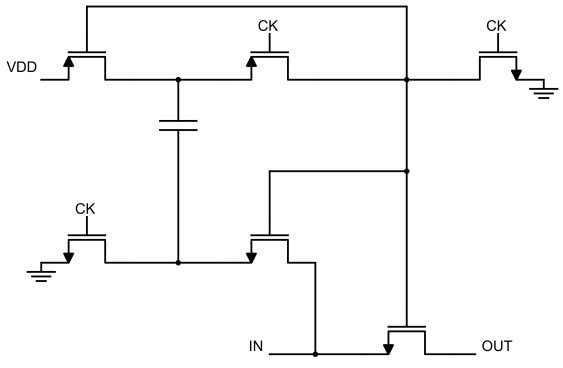

Fig. 4: Design of a typical bootstrapped switch.

For a 10-bit ADC, a conservative target spurious free dynamic range (SFDR) is 73dB. However, with such low conductance at 0.1V a single bootstrap switch is not enough to meet this target. For our design, we have a 12.5% to 87.5% sample to hold duty cycle, respectively. With a sample rate of 2kHz, this leaves us with little time to fully track the input during our sample stage. To improve transistor conductance, the number of bootstrap capacitor boost stages needs to be increased. In fact, after running various simulations and trying new designs the optimal approach was to cascade the bootstrap topology four times over. In this layout, diagramed in Fig. 5, four smaller capacitors are charged during the hold phase then linked in series. This not only allowed us to use relatively small internal capacitors for the bootstrap switch, but it also boosted the gate voltage on the sample transistor to 0.4V + Vin. After size optimization of the capacitors and transistors, the target SFDR of 73dB was met as seen in Fig. 6.

In order for a quadruple bootstrap switch to function, some parts of the reset circuitry had to be altered. Traditional bootstrap switches use a PMOS to pull the capacitor top plate high to VDD. For our design, this causes a leakage issue across the PMOS since it experiences a relatively large voltage drop across the drain to source. To prevent this, a huge gate voltage would need to be generated to ensure a negative source to gate voltage. To circumvent this issue, NMOS pullup transistors were used alongside a 2VDD charge pump to be able to correctly pull the top plate voltages to VDD. This process eliminates leakage in the pullup transistors while also enabling the 4VDD boost needed for good tracking.

In addition to simply cascading the bootstrap architecture, and resolving pullup leakage several key changes had to be made to prevent leakage current from the pulldown/hold transistors. This is because the design is done in 28nm technology, which is faster than more common technologies like 180nm. However, in 28nm technology the transistors leak small amounts of current from their drain to source. With a larger supply voltage this leakage is negligible but for a 0.1V supply it is significant. To prevent this leakage the NMOS transistors had to be switched to have a negative gate to source voltage as opposed to a gate to source voltage of zero. This leakage lock circuit is shown in Fig. 7, where an intermediate voltage between an NMOS pair is pulled high during the NMOS off state to ensure very little leakage current during the hold/reset phase.

One final change that needed to be made to the sample switch, was the addition of leakage prevention circuitry for the top plate of the sampling capacitor. The previous

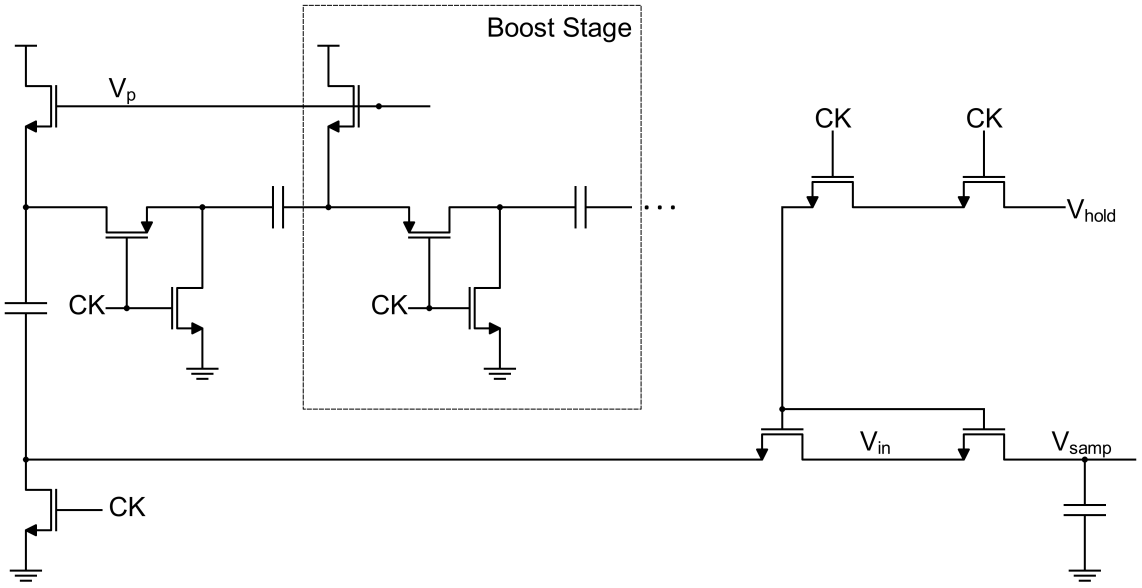

Fig. 5: Design of quadruple bootstrapped switch.

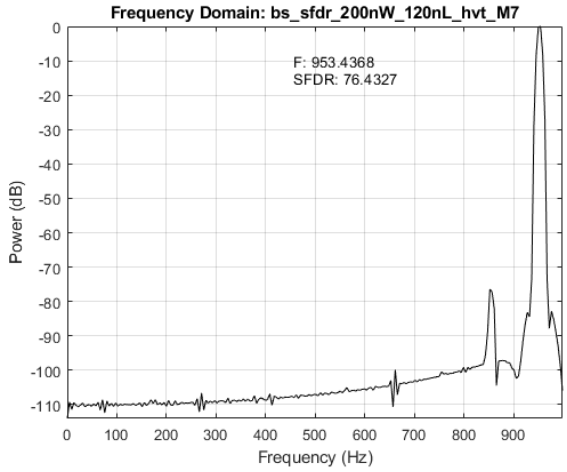

Fig. 6: SFDR of our quadruple bootstrapped switch at Nyquist Frequency

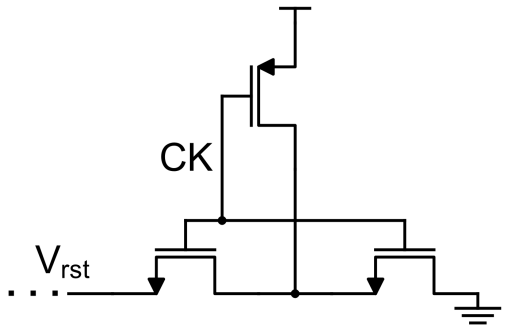

Fig. 7: Leakage lock circuit added to NMOS reset switches.

modification tackled leakage on the boosting capacitors. However, since the input continues to change during a hold phase, the top plate of the sampling capacitor can leak from drain to source on the sampling transistor. As discussed before, if this sampled voltage changes more than the LSB voltage during our voltage-to-time conversion we introduce error in our quantization. To prevent this from happening, V_{hold}, as seen back in Fig. 5, is generated using a simple driver and capacitor shown in Fig. 8. This voltage is switched between zero and -VDD so that our sample transistor sees the 4VDD boost voltage during sample phase and -VDD during the hold phase. This -VDD gate voltage puts the transistor in a state of strong inversion, which ensures that there is very little leakage on the top plate of the sampling capacitor.

B. Time Domain Conversion

Voltage domain comparators are commonly used in ADCs. In order to meet quantization noise requirements, the transistors in a voltage domain comparator need to be sized according to the noise to LSB relationship given by

$$\sigma^2 \leq \frac{\Delta^2}{12}$$

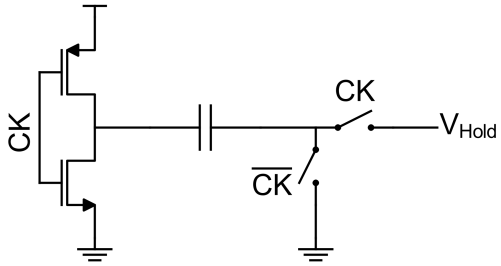

Fig. 8: Negative voltage generator for the sample transistor.

where sigma squared is the standard of deviation of the input referred noise power probability density function with respect to comparator input voltage difference. With an LSB voltage of 0.195mV transistors in a voltage domain comparator would need to be sized unreasonably high.

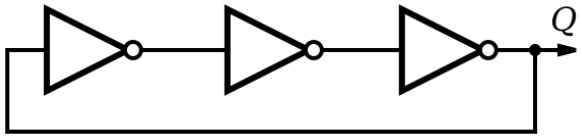

Fig. 9: A 3-stage ring oscillator.

To mitigate this problem, we have designed this ADC with a VTC and TDC. By moving the quantization to the time domain, the transistors no longer run into scaling issues that come with lowering the supply voltage. For the VTC, we wanted to keep the circuit simple and well controlled. A basic ring oscillator (Fig. 9) oscillates at different frequencies depending on various metrics given in the equation below from [13], where f_{fr} is the oscillation frequency, I_v is the current drawn by a single stage, and M_i is the number of stages.

$$f_{fr} = \frac{I_v}{M_i V_{DD} C_{Load}}$$

In order to use this in our design we had to modify the layout of the inverters used in the ring so that we could manipulate one of these variables. To do this, each inverter, as shown in Fig. 10, was modified with a stacked PMOS and NMOS pair which allows us to control the amount of current conducted. This in turn, varies the speed at which they oscillate. this modification allows us to use the previously sampled voltage as a control voltage for the voltage controlled oscillator (VCO) ring.

To ensure that this control voltage would remain robust at various temperature corners of design, we designed a common-source current mirror to generate the header

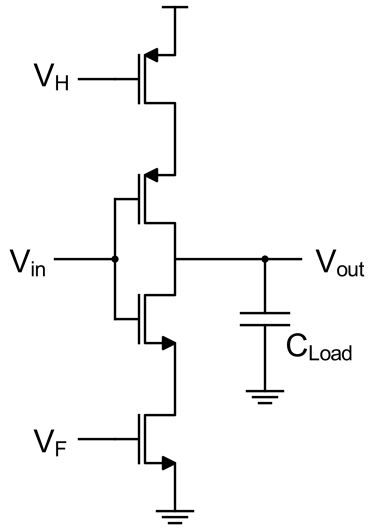

Fig. 10: Current-starved inverter.

and footer voltages, V_H and V_F respectively. This design is shown in Fig. 11. Here, the sampled voltage drives two stacked current mirrors that generate gate voltages to mirror the appropriate current to the VCO units. An NMOS is also added at the input to ensure that there is some offset level of conduction even when the control voltage is near zero.

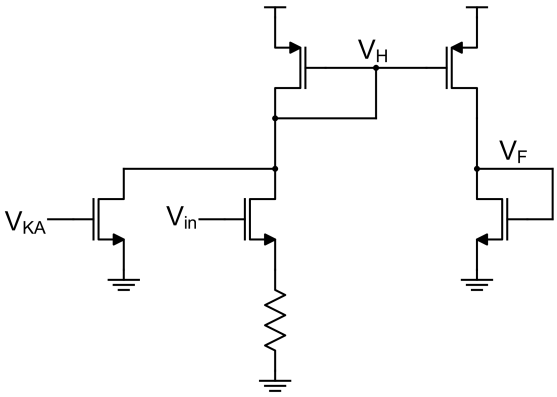

Fig. 11: Common-source current mirror VCO unit driver.

Now that the sampled voltage directly and consistently influences the VCO oscillation frequency, we can begin to quantize the frequency. To do this, we implemented a 5-bit counter on one node of the VCO ring to keep track of every 2π rotation. To track the phase change within 2π, D flip-flops are connected to each node of the VCO and clocked at the beginning of each sample. Each time they are clocked, they load their previous value into another D flip-flop. This way, we can track the state

at the beginning and the end of the sample. These two values are evaluated by a difference operator which result is our total interior phase change.

A big challenge with using a time domain component is metastability. A metastability event is encountered when the TDC logic fails to reach a decision within a given amount of time, i.e., the VCOs are still oscillating. Metastability detection is crucial in a TDC design since it is always updating its own inputs to complete the next comparisons. One way to detect metastability is to use simple binary counters to understand the depth level of metastability. As seen in Fig. 12, as Vin decreases oscillation counts also increase. A larger number indicates deeper levels of metastability and all cases where metastability is past a predetermined threshold need to be thrown out and re-measured.

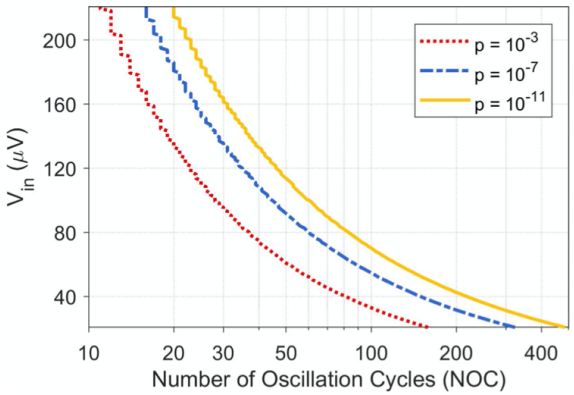

Fig. 12: Oscillation count vs. Vin [12].

IV. Conclusion

In this paper we discussed the design of a 28nm 0.1V 10-bit 2kS/s time domain based ADC. By using innovative design choices in the sample and hold circuit, along with the use of a time domain conversion circuitry, the system is expected to operate correctly at 0.1V supply. With further design and testing, we feel confident that the ADC will be able to perform with a reasonable sample rate of 2kHz.

Our future work consists of finalizing design elements and completing physical layout. In order to successfully detect a signal, the input needs to be oversampled due to the inherit first order noise shaping of the VTC. A final oversampling rate needs to be determined by evaluating the needed resolution for 10 bits. An exact number of VCO stages needs to be determined as well by evaluating power/speed as a function of stages. The static properties of the ADC (INL and DNL) need to be measured and evaluated. The signal-to-noise ratio (SNR) needs to be optimized to reach within 3dB of the ideal SNR of 62 dB for a 10-bit ADC. Finally, the chip must go through tape-out and fabrication to be tested and verified. After all of this is completed, we are confident that this ADC will push the limits of technology in space to its next level. We anticipate finalizing the design in Spring of 2021, and finishing tape-out at the end of the Summer of 2021. The chip will then be tested and verified.

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