NEW PROCESSES FOR HETEROGENEOUS INTEGRATION OF III-NITRIDE OPTOELECTRONIC DEVICES: APPLICATION TO INGAN-BASED LIGHT EMITTING DIODES AND SOLAR CELLS GROWN ON 2D H-BN

A Dissertation
Presented to
The Academic Faculty

by

Soufiane Karrakchou

In Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy in the
School of Electrical and Computer Engineering

Georgia Institute of Technology
June 2021

Approved by:

Dr. Jean Paul Salvestrini, Advisor
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Shyh-Chiang Shen
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Abdallah Ougazzaden
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Nico Declercq
The George W. Woodruff School of Mechanical Engineering
Georgia Institute of Technology

Dr. Paul L. Voss
School of Electrical and Computer Engineering
Georgia Institute of Technology

Date Approved: June 1st, 2021

ACKNOWLEDGEMENTS

I would like to begin by expressing my sincere gratitude to my advisor, Prof. Jean Paul Salvestrini for his continuous guidance, encouragement, patience and support all over this thesis journey. His knowledge and expertise have led me to grow as a research engineer and young scientist. I am also grateful to Prof. Abdallah Ougazzaden who brought me through his enthousiasm for research to this wonderful and leading-edge world of semiconductors, and for giving me the opportunity to be part of his research team. I'm also deeply grateful for all his necessary guidance and feedback throughout this thesis.

I would like to express my gratitude to Prof. Paul L. Voss for his valuable support and the insightful scientific discussions we had throughout these years. My sincere thanks also go to Dr. Suresh Sundaram for his contribution to this work, through the epitaxial growth and supervision of all samples used in this thesis.

I would like to express my gratitude to the committee members for taking the time to read this thesis and for offering helpful comments and suggestions.

My sincere appreciation is extended to my research group's colleagues: Taha Ayari for his contribution to the fabrication process of devices, Walid El-Huni and Rajat Gujrati for their contribution to the simulation study, Adama Mballo for his contribution to the epitaxial growth, Yacine Halfaya for his contribution through the deep characterization of the solar cells structures, Renaud Puybaret and Youssef El Gmili for their important contribution to the nanolithography process, Prof. Ali Ahaitouf and Olivier Konne for their help with the design of the measurement setups.

I would also like to thank the Institut Lafayette's scientists: Yves Sama, Simon Gautier, Hafsa Bouhnane, Karim Bouzid, Tarik Moudakir and Chris Bishop for their productive and fruitful collaboration on the fabrication process and characterization as well as for the precious suggestions they provided for my research work.

My thanks also go to my fellow labmates and friends Ashutoch Srivastava, Hibat E. Adjmi, Iktiham Bin Taher and Vishnu Ottapilakkal. It was a real pleasure to work with them and I wish them good luck for their research work.

Lastly, I would like to give a special thanks to my parents for their support and sacrifices all over the years. They have nurtured my curiosity and critical thinking skills since I was young and have always encouraged me to study science. This thesis is dedicated to them.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

SUMMARY

Mechanical release and transfer of GaN-based heterostructures using 2D h-BN have undergone considerable development with the invention of van der Waals epitaxy of III-Nitride thin-films along with device fabrication and transfer onto various flexible and rigid substrates. The technique consists of mechanical peeling-off of the epilayers from the native substrate, which allows a dry and fast release and transfer of optoelectronic and electronic III-N devices to arbitrary substrates. However, during the epitaxial growth and device fabrication of the epilayers, delaminations and cracks arise in the structures, which limits the size of crack-free devices to only a few hundreds of squared microns.

The goal of this thesis is to develop efficient, large-scale and low-cost new processes for heterogeneous integration of III-Nitride optoelectronic devices onto arbitrary rigid and flexible substrates. These developed processes were used to fabricate lateral and vertical InGaN-based LEDs as well as nanopyramid-based InGaN solar cells grown on 2D h-BN.

The outcomes of this thesis represent progress towards efficient, robust and low-cost 2D-hBN-assisted lift-off technology for heterogeneous integration of optoelectronic and electronic III-N devices.

In Chapter 1, we introduce the motivations and the scope of this thesis. In Chapter 2, we present the state of the art of lift-off and transfer methods for heterogeneous integration of optoelectronic and electronic layers and devices. In Chapter 3, we introduce the basic principle of van der Waals epitaxy of 3D III-N epilayers on 2D h-BN and we give an overview of the main results achieved by our group at IRL 2958 GT-CNRS Lab (prior to the beginning of this thesis), for the growth of 2D layered h-BN as well as the

InGaN/GaN epilayers on top of h-BN/sapphire substrates by vdWs epitaxy. These results are essential to the development of the advanced fabrication processes achieved during this thesis. In Chapter 4, we present the main results achieved on the fabrication and transfer of LEDs grown on h-BN through the selective area van der Waals epitaxy (SAVWE) and the self-lift-off and transfer (SLOT) while in Chapter 5 we present the main results obtained for the design and the fabrication of nanopyramid-based InGaN solar cells on 2D h-BN for the next generation of high-efficiency flexible solar cells.

CHAPTER 1. INTRODUCTION

The demand for advanced electronic and optoelectronic devices has triggered the development of epitaxial growth methods for single-crystalline semiconductors. However, the lattice and thermal expansion coefficient mismatches between the epilayers and substrate materials limit the possibility for monolithic integration of tailored electronic and optoelectronic devices. Meanwhile, the heterogeneous integration of dissimilar components has attracted considerable attention. It consists of assembling devices fabricated separately, using different materials and processes, into a single die to achieve a heterogeneous system[1].

One interesting way to achieve this heterogeneous integration is to lift-off the epitaxially-grown layers and to transfer them to a receiving substrate. It also allows the expensive native substrate to be reused for other epitaxial runs. Several lift-off methods have been developed for this purpose, such as mechanical spalling[2], laser lift-off[3] and chemical etching[4] of a sacrificial layer. However, these techniques have several limitations, notably high cost, a time consuming process, surface contamination and limitations in the size of the released layers and reusability of the substrate. Recently, a promising transfer approach based on two-dimensional (2D) crystals, namely graphene[5] and hexagonal boron nitride (h-BN)[6] has emerged as an effective technology for the release and transfer of III-nitride epilayers. It consists of a mechanical peeling-off of the epilayers from the substrate via handling materials, which allows a dry and fast (instantaneous) release and transfer to arbitrary substrates.

2D layered h-BN can be grown by metal organic vapor phase epitaxy (MOCVD) in the same run and same growth conditions as the GaN-based structures, which is a very important characteristic. Accordingly, 2D layered h-BN-based assisted lift-off and transfer techniques have been accelerated through recent progress in the epitaxial growth of layered h-BN and the subsequent van der Waals (vdWs) epitaxy of III-Nitride materials by MOCVD[7], [8] and the subsequent fabrication of electronic and photonic devices such as HEMTs[9], LEDs[10] and solar cells[11]. All of these experiments showed the large potential of the 2D layered h-BN-based mechanical transfer technique on rigid and flexible substrates.

On the other hand, these reported experiments reveal two critical weaknesses of wafer scale vdWs h-BN for device transfer purpose. The first one is related to the delamination of the h-BN and 3D structures during the cooling process after the epitaxial growth or during the device fabrication steps. The second issue is the cracks which appear in the devices and are induced during the lift-off and transfer steps, leading to a low fabrication yield which further decreases with the size of the transferred devices. This effect is mostly caused by the mechanical damage resulting from the lift-off and transfer that required delicate manipulation. As a result, transferred layers came with a high crack density randomly distributed over the surface which limited the size of crack-free devices to only a few hundreds of squared microns.

However, using this technology in high-throughput industrial scale requires the development of large-scale, reproducible and highly-controlled release techniques.

The goal of this thesis is to develop efficient, large-scale and low-cost processes for heterogeneous integration of III-Nitride optoelectronic devices, namely InGaN-based LEDs and solar cells grown on 2D layered h-BN. In this context, we focus on the improvement of (i) the material quality (ii) the optical and electrical performance and (iii) the transfer yield of large-scale crack-free devices to flexible and rigid substrates, as compared to the state of the art. In the case of solar cells, these processes can even pave the way to an efficient fabrication of tandem cells by transferring the InGaN cells on top of a silicon solar cell or InGaN multi-junctions by stacking solar cells with different indium incorporations.

This document consists of 5 chapters. The ”Introduction Chapter” is followed by :

- Chapter 2, where we present the main lift-off and transfer methods for heterointegration by giving a critical analysis of advantages and disadvantages of these main transfer techniques and we discuss their applications on a broad range of materials and devices.
- Chapter 3, where we introduce the basic properties of 2D hexagonal boron nitride (h-BN) and the van der Waals epitaxy of 3D III-N epilayers on top of it.
- Chapter 4, where we present the main results achieved on the fabrication and transfer of LEDs grown on h-BN through newly developed processes : selective area van der Waals epitaxy (SAVWE) and the self-lift-off and transfer (SLOT).
- Chapter 5, where we present the main results obtained on the design and the fabrication of nanopyramid-based InGaN solar cells on 2D h-BN for the next generation of high-efficiency flexible solar cells.

CHAPTER 2. LIFT-OFF AND TRANSFER TECHNIQUES FOR HETEROGENEOUS INTEGRATION

Epitaxial growth has been a key technology in the development of high-quality semiconductor layers on different inorganic substrates. These layers led to the fabrication of efficient electronic and photonic devices such as transistors, LEDs, solar cells, etc. The epitaxial growth can be homogeneous (growth on a substrate of the same material) or heterogeneous (growth on a substrate of a different material). Homogeneous epitaxy allows to achieve high-crystalline quality layers but usually requires expensive substrates, while heterogeneous epitaxy is limited by the lattice and thermal expansion coefficient mismatches between the epilayers and the growth substrate, which generates a high-density of defects in the epilayers. This mismatch limits the potential for monolithic fabrication and integration of high-quality devices on dissimilar substrates. Subsequently, advanced epitaxial growth and transfer techniques have been developed to allow the heterogeneous integration of highly mismatched materials through the release of layers and devices from the native substrate and the transfer onto another receiving substrate.

Besides the possibility for integrating dissimilar materials on the same platform, removing the growth substrate can allow (i) the expensive substrate to be reused to grow other epilayers, which drastically reduces the production costs [12], [13] and (ii) the performance of the transferred devices to be boosted. One example is GaN-based power LEDs for automotive lighting that need a high thermal dissipation capability to sustain injection of high currents, thus, these devices are often transferred to metallic substrates such as copper [14], [15].

Several methods offer solutions for the fabrication of transferrable III-N semiconductor devices. These epitaxial layer separation approaches include chemical lift-off (CLO) - also referred as epitaxial liftoff or ELO-, laser lift-off (LLO), mechanical spalling and 2D-layer assisted lift-off (Figure 1).

In this chapter, we give a critical analysis of advantages and disadvantages of these main transfer techniques and we discuss their application to a broad range of materials and devices.

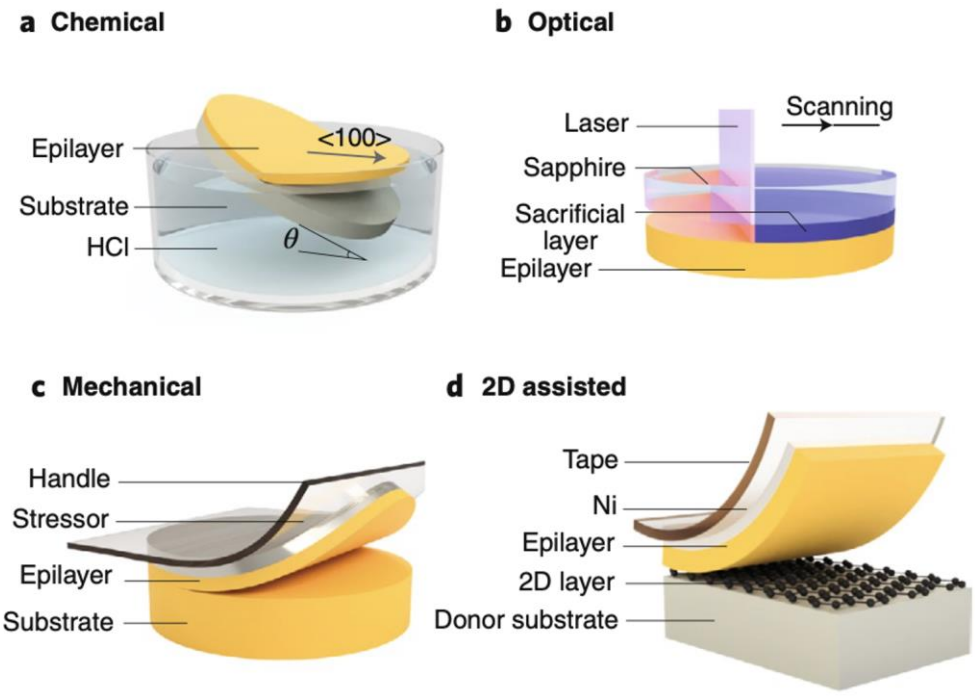

Figure 1 - Schematics of different lift-off and transfer techniques described in this chapter. Adapted from [1].

2.1 Transfer by Chemical Lift-Off

Chemical lift-off (CLO) is based on the removal of a sacrificial layer inserted in between the functional epilayers and the substrate [4], [16], [17]. The removal of the substrate is achieved by a selective etching of the sacrificial layer while preserving the native substrate. For this purpose, this method needs to allow the growth of a high-quality epilayers on top of the sacrificial layer and show high etch selectivity of this layers. Thus, selecting the releasing layer depends on the subsequent epilayers and the selectivity of the chemical etchants.

The etching of the releasing layer can be relatively fast for small pieces but the scalability of this technique can be time-consuming (several hours to even days), which limits the possibility of high-throughput production. Accordingly, different variants have been developed to accelerate this process.

2.1.1 Chemical Lift-Off by Lattice-Matched Sacrificial Layers

Since the epitaxial growth of high-quality epilayers is easier on lattice-matched layers, first investigations of CLO were mainly based on this technique. For instance, AlAs is known to be lattice-matched with GaAs substrates and can be etched by hydrofluoric acid (HF) whereas GaAs-based layers are resistant to HF[18]. This combination led to the fabrication of freestanding GaAs-based membranes for LEDs, solar cells and photodetectors[19], [20]. However, etching of AlAs by HF induces some material residues and increases the roughness of both the epilayers and the substrate which deteriorates the epilayers quality and limits the possibility of substrate reuse[21]. Accordingly, surface tension assisted CLO

by lattice-matching AlInP (etched by hydrochloric acid) was introduced to overcome this issue and offers a smother detached surfaces of both the epilayers and the substrate[21].

2.1.2 Chemical Lift-Off by Heterogeneous Sacrificial Layers

Since III-N materials are resistant to most of the chemical etchants, using a lattice-matched III-N sacrificial layer for CLO is challenging. For this purpose, the use of a heterogeneous sacrificial layer was investigated. Although the growth of III-N films on dissimilar layers is also challenging and can led to the degradation of the material quality, several dissimilar materials were used for the epitaxial growth and release of GaN-based thin-films, such as SiO_2[22], Ga_2O_3[16], CrN[17] and ZnO[4]. For example, Ha et al.[17] have shown successful release of GaN LEDs by depositing CrN by sputtering and growth of GaN-based films on CrN/sapphire by low-pressure hydride organometallic vapor phase epitaxy

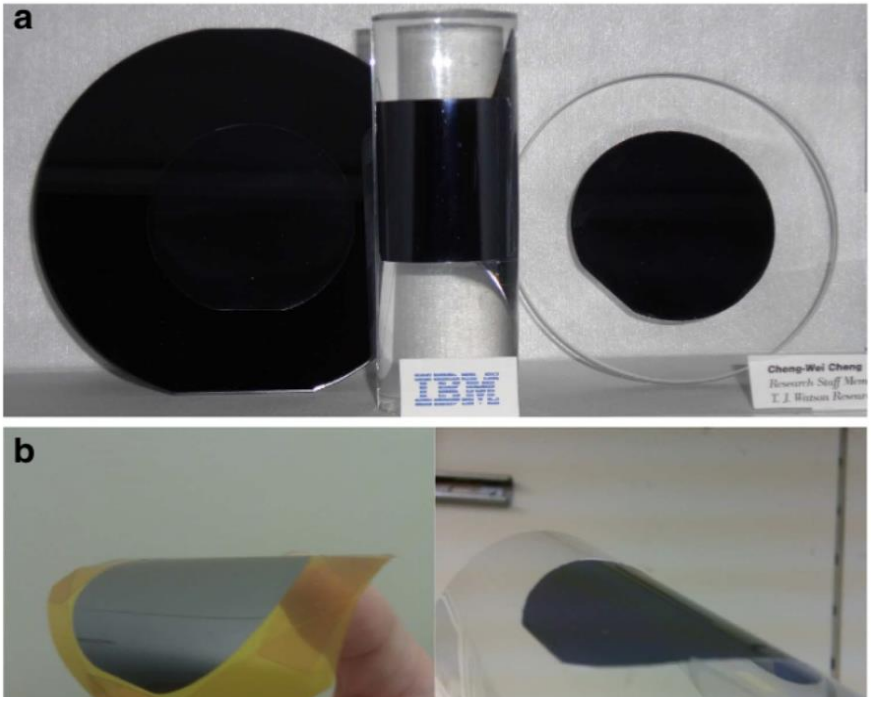

Figure 2 - Photographs of a transferred GaAs layers to a (a) rigid and (b) flexible substrate by HCl etching of AlInP sacrificial layer. Adapted from [31].

(HOVPE). After a selective etching of CrN sacrificial layer, high-quality vertical LEDs with low threshold voltage and low series resistance have been achieved. However, this process was demonstrated only on centimeter-sized area and the possibility of its scalability is not proven.

2.1.3 Photoelectrochemical or Electrochemical Lift-Off

The above mentioned challenges of chemical etching of III-N materials also led to the development of photoelectrochemical (PEC) etching of III-N sacrificial layers. This method is based on the light absorption in the sacrificial layers that generates electrons and holes and thus the oxidation and dissolution of this releasing layer. For example, by selectively etching InGaN layers, large-area lift-off of GaN membranes was demonstrated[23]. However, one disadvantage of PEC is that it requires an external illumination source, for this purpose, the electrochemical (EC) doping-selective etching was developed[24]. This methods allows a fast etch of n-doped GaN while being inert to p-doped and undoped GaN.

The variant chemical lift-off methods presented above allows achievement of good quality of transferred layers and devices in some particular configurations. However, challenges remain in the choice of the sacrificial layer and the selective etchant. Moreover, this method offers (i) a slow etch rate (ii) surface contamination by etching residues (iii) expensive safety precautions to avoid leaks and evaporation of the extremely hazardous etchants (e.g., hydrogen fluoride, etc.). For this purpose, other dry transfer techniques were developed such as laser lift-off (LLO).

2.2 Transfer by Laser Lift-Off

LLO is based on high-power excimer laser irradiation that separates epitaxial layers from transparent substrates such as sapphire. For example, for GaN LEDs on sapphire, the short wavelengths of the laser are transparent to the sapphire and are absorbed in GaN, inducing decomposition of the GaN/substrate interface to metallic Ga (which becomes liquid at about 30°C) and N_2 gas, thereby separating GaN from sapphire[25]. Damage-free release of GaN-based films has been demonstrated using a 248 nm laser at around 500 mJ cm^{-2}[12]. During this process, the wafer is bonded to an intermediate or final substrates by adhesive bonding (wax) or wafer bonding[26], [27]. Wang et al.[27] achieved a stable transfer of GaN films grown on sapphire via a Ni/Au bonding layer onto a molybdenum substrate. 2-inch and 4-inch GaN wafer transfer has been demonstrated, and results in robust, versatile and fast process especially thought the recently enabled femtosecond lasers[28], [29]. However, because of the thermal strain relaxation and shock waves induced by laser excitation, damage to GaN films could be induced[26]. Moreover, the plasma induced at the interface can result in a roughness ranging from 60 to 90 nm[30], which requires a chemical and mechanical polishing of the substrate before reuse. The high cost of LLO equipment is another disadvantage that limits its availability for regular users.

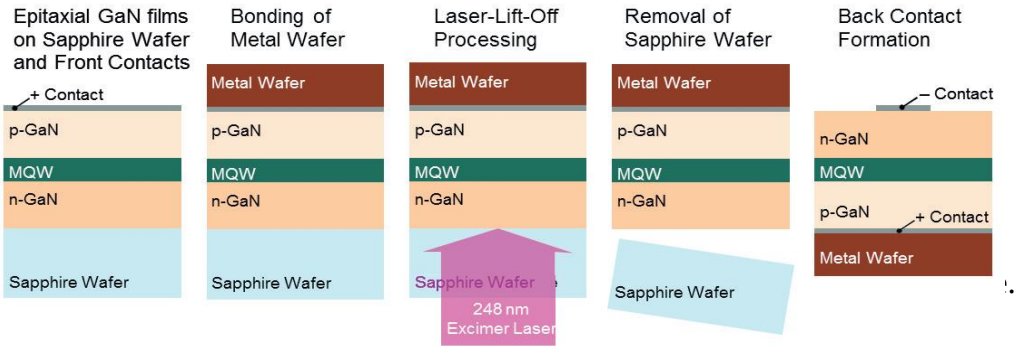

Fig
Ad

2.3 Transfer by Mechanical Spalling

Mechanically controlled spalling is fracture-based transfer method of creating semiconductor thin films. It is based on the deposition of a tensile stressor film on the surface of the epilayers followed by a tape handler as shown in Figure 4[31]. A crack is initiated and propagates horizontally in a controllable way through the entire functional layer. It has been demonstrated on a wafer-scale at IBM on several materials such as silicon[32], GaAs [33] and GaN[34], [35] to produce different flexible electronic and optoelectronic components such as CMOS transistors,[2] LEDs[34] and solar cells[33], [36].

When compared with CLO and LLO, mechanical spalling is much simpler since it does not require the use of a sacrificial layer or an expensive equipment. However, spalling crack propagation is difficult to control because it depends on many factors such as the stress amplitude and the substrate material and orientation[37]. Thus, accurate control of the thickness of the released layer is very complicated. Moreover, this process induces residual stress and curvature of the released layers on the handler tape. Another disadvantage is the high roughness of the released layers that can be as large as 500 nm as reported by Bedell et al.[38] for GaN films.

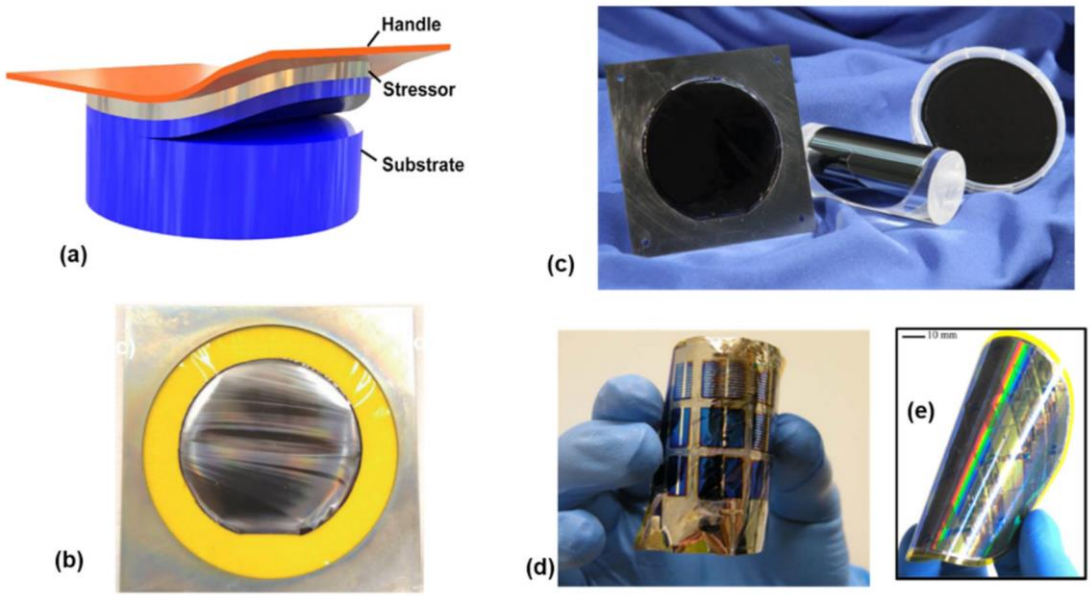

Figure 4 - (a) Schematics of the mechanical spalling process. (b) Optical image of the released GaN film. (c) Optical images of Si on plastic. (d) Transferred solar cells. (e) flexible CMOS circuits fabricated by spalling techniques. Adapted from [31].

2.4 Transfer by 2D-Layer Assisted Lift-Off

2D-layer assisted lift-off utilizes the weak van der Waals (vdWs) bonds of the single-crystalline epilayers grown on 2D materials by advanced epitaxy methods, namely vdWs epitaxy and remote epitaxy. The 2D materials layer has two functions. First, it acts as a buffer layer for the subsequent epilayers despite the large lattice mismatch. Second, due to the weak vdWs bonds, only a weak mechanical force on the epilayers is needed for the release from the native substrate. This technology has been accelerated through recent progress in the epitaxial growth of high quality III-N materials on graphene [5] and h-BN[6], [39]. Recent reports have been made on the transfer of some key opto-electronic devices (HEMTs, LEDs and solar cells) to flexible and rigid substrates [9], [40], [41].

In contrast with conventional LLO and CLO methods, the release of functional layers using 2D materials is fast (within few seconds) and requires no expensive equipment and no chemical etchants. Compared to the mechanical spalling, this techniques allows a reduced stress needed for transfer as well as an accurate control of the layer thickness which is defined by the epitaxial growth. Moreover, the released surfaces are atomically flat due to the 2D buffer layer allowing no covalent bonds between the epilayers and the substrate[1]. Thus, no chemical and mechanical polishing is needed for the reuse of the substrate.

Here two different approaches are possible. The first is a liquid-phase exfoliation by ultra-sonification, which is based on exposing the wafer, in an ultrasonic bath, to a liquid having a surface tension comparable to the surface energy of the 2D material[42]. However, this technique has a production yield lower than 10 % and is therefore unsuitable for industrial applications due to (i) defects and cracks caused by the local high temperatures due to the ultra-sonification process, (ii) difficulties of handling released layers in the liquid and (iii) time consuming process that can take until hundreds of hours.

The second method in this category is the mechanical release of layered materials. It consists on a mechanical peeling-off the epilayers from the substrate via a handling tape which allows a dry and fast release. Using a 2D layered h-BN buffer, several authors reported MOCVD growth of GaN-based structures associated with a simple release of these layers. Moreover, Ayari et al.[9] demonstrated the fabrication and transfer of GaN-based high mobility electron transistors (HEMT) gas sensors grown on layered h-BN, with higher sensitivity to NO_2 gas and a response time 6 times faster than before transfer. Besides, Glavin et al.[40] achieved flexible high-frequency RF HEMTs with cut-off frequencies greater than 42 Ghz and maximum oscillation frequencies greater than 74 GHz.

Concerning optoelectronics applications, the 2D-h-BN assisted mechanical lift-off allowed the fabrication and transfer of InGaN/GaN LEDs and solar cells with enhanced performances to rigid and flexible substrates[6], [11].

All of these experiments showed the large potential of the layered h-BN-based mechanical transfer technique on different host substrates in terms of (i) thermal dissipation that improve the efficiency of HEMT transistors when using a SiC substrate[41], (ii) thermal confinement that allows for higher sensitivity and shorter time-response HEMT-based gas sensor when using copper tape as substrate[9] (iii) device flexibility when using plastic substrate[10].

On the other hand, these reported experiments revealed two critical weaknesses of wafer-scale h-BN for device transfer. The first one is related to the delamination of the h-BN and 3D structures after epi-growth. This could be explained by the fact that for large area substrates the difference between the thermal expansion coefficients between the 3D heterostructures and the BN/sapphire substrate doesn't result in the creation of a wafer bow as in the case of GaN grown on sapphire substrate[43] but on spontaneous and sporadic delamination of the heterostructure from the substrate during the cooling process after the epitaxial growth or during the device fabrication steps[11], [43], [44]. The second issue is the cracks which appear in the devices and are induced during the lift-off and transfer process, leading to a low fabrication yield which further decreases with the size of the transferred devices[6], [41]. This effect is mostly caused by the mechanical damages resulting from the lift-off and transfer process that required delicate manipulation. As a result, transferred layers came with a high crack density randomly distributed over the surface which limited the size of crack-free devices to only a few hundreds of squared

microns. Figure 5a shows a schematic of the spontaneous delamination mechanism of 2D layered h-BN layer from sapphire substrate during immersion in water and Figure 5b shows an example of cracks generated in GaN-based LEDs during transfer via water-soluble tape. Thus, using this technology in high-throughput industrial scale requires the development of large-scale, reproducible and highly-controlled release techniques.

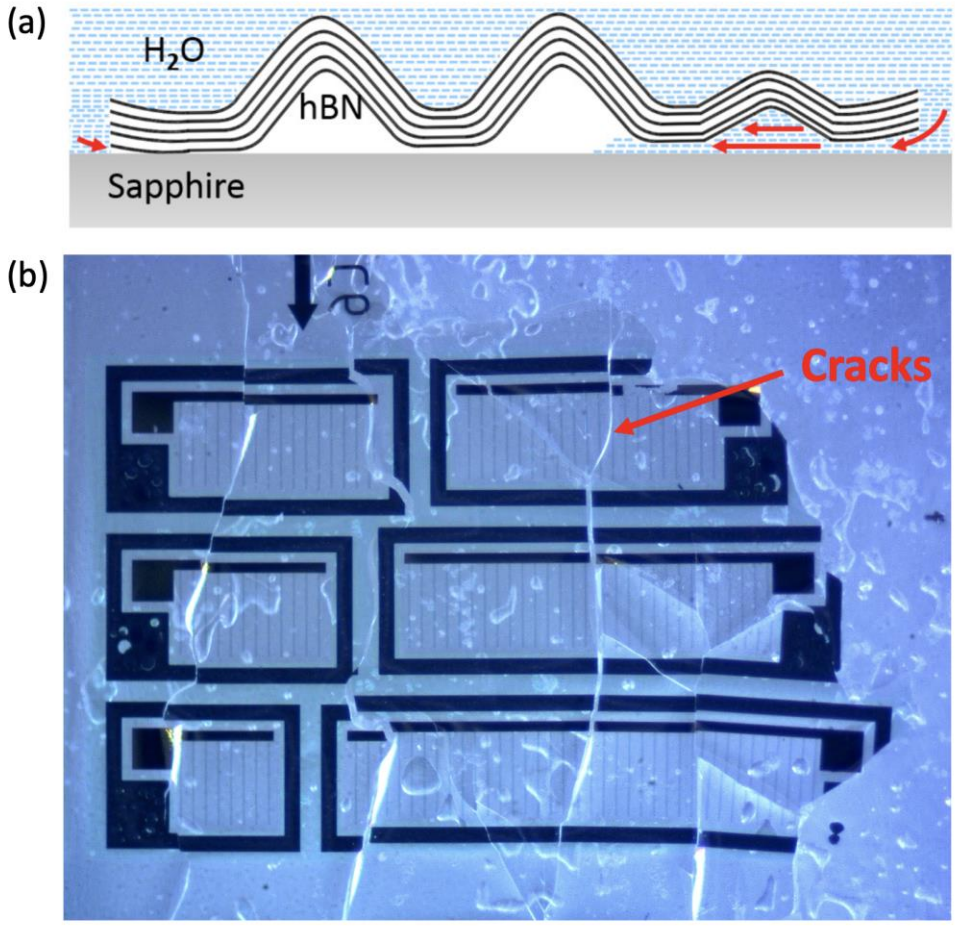

Figure 5 - (a) Schematic illustrating the spontaneous delamination of 2D layered h-BN layer from sapphire substrate during immersion in water. Adapted from [43]. (b) Example of cracks generated in GaN-based LEDs during transfer via water-soluble tape.

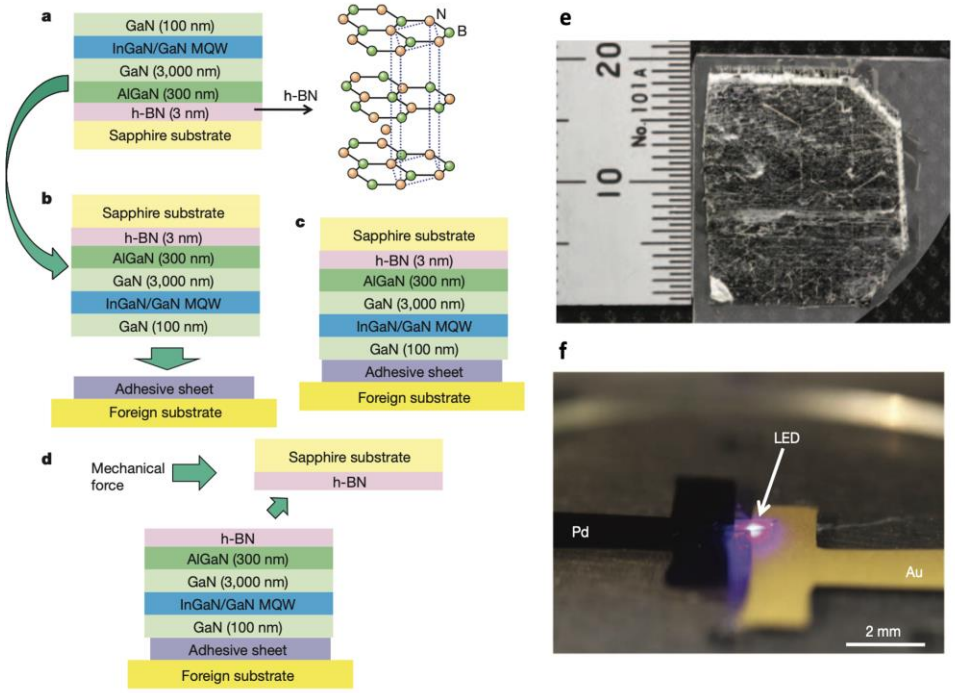

Figure 6 - (a-d) Schematics illustrations of an LED structure grown on h-BN/sapphire and transferred onto a foreign substrate. (e) Photograph of a released membrane and (f) prototype of a fabricated LED. Adapted from [6].

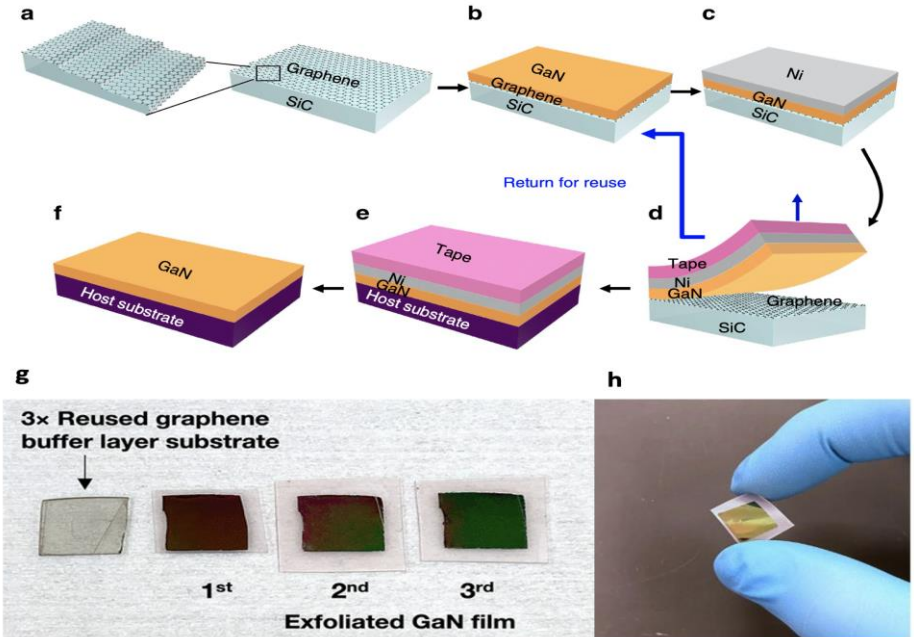

Figure 7 - (a-f) Schematic of the growth and graphene-assisted mechanical lift-off of single-crystalline thin films using nickel stressor and handling tape. Adapted from [5]. (g,h) Photographs of released GaN films from graphene buffer layer enabling substrate reuse by repeated growth and release Adapted from [13].

Figure 6 shows schematics and photographs of the first LED structures grown on h-BN/sapphire and transferred onto a foreign substrate [6] whereas Figure 7 shows the transfer process for GaN-based epilayers grown directly on graphene [5], [13].

In the next chapter, we discuss the material properties of h-BN. Then, we give an overview of the main results achieved by our group at IRL 2958 GT-CNRS laboratory (prior to the beginning of this thesis), for the growth of 2D layered h-BN as well as the InGaN/GaN epilayers on top of h-BN/sapphire substrates by vdWs epitaxy. These results are essential to the further development of advanced fabrication processes that are extensively presented in Chapter 4 and Chapter 5.

CHAPTER 3. VAN DER WAALS EPITAXY ON 2D H-BN

3.1 2D Hexagonal Boron Nitride : Material and Growth

3.1.1 Properties of 2D h-BN

Two-dimensional (2D) materials constitute a new class of nanomaterials exhibiting exceptional physical and functional properties including high electron mobility, high mechanical strength, high surface-to-volume ratio and mono-layered structure that makes this type of materials a key to the development of next-generation of high-performance 2D heterostructure devices, flexible electronics/optoelectronics as well as the heterogeneous integration of dissimilar components onto a common electronic and photonic integrated circuit. Two-dimensional hexagonal boron nitride (2D h-BN) is one of these materials and has an atomic structure quite similar to graphene, with a honeycomb configuration where nitrogen (N) and boron (B) are covalently sp^2-bonded with a lattice constant of 2.504 Å

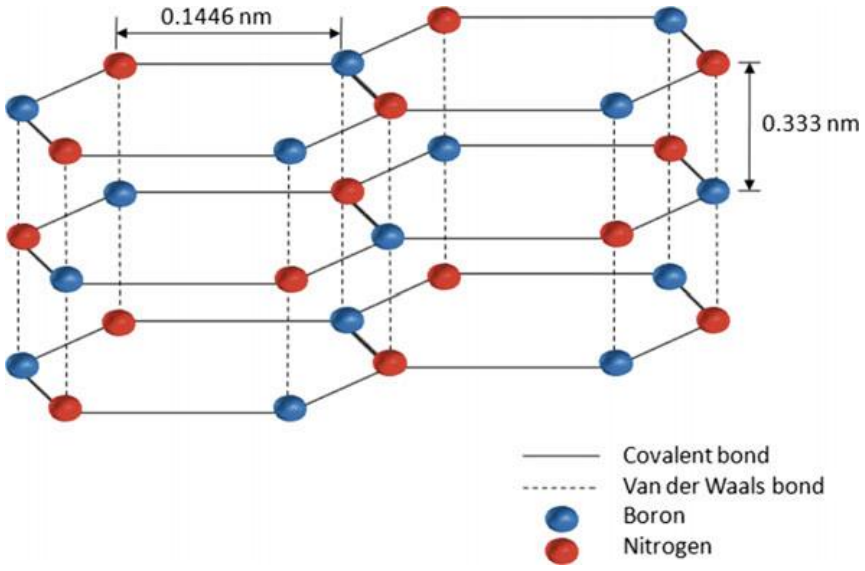

Figure 8 - Schematic diagram of the atomic structure of 2D layered h-BN. Adapted from [45].

and stacked through weak vdWs forces with an interlayer distance of 3.33 Å. It has an atomically flat surface with no dangling bonds and a roughness of around 0.1 nm. Owing to its strong covalent bonds, 2D h-BN has a very high mechanical strength (breaking strength of 15.7 Nm^{-1}) and thermal conductivity (~ 1700 – 2000 W mK^{-1}). It is also mechanically inert and thermally stable. Moreover, h-BN is a wide bandgap semiconductor (~ 6.5 eV) which makes it inherently electrically insulating[45].

3.1.2 Growth of 2D Layered h-BN on Sapphire by MOCVD

Two-dimensional hexagonal boron nitride has been obtained through different methods. First, mechanical exfoliation of bulk crystals was introduced, where a scotch tape has been used to create boron nitride nanosheets that can be transferred onto other materials or devices[46], [47]. However, with this method the scalability is significantly limited. Other methods were introduced, ranging from chemical vapor deposition on metal foils[48] or by molecular beam epitaxy (MBE)[49] and flakes synthesized by polymer derived ceramics (PDC) have also been used[50]. Nevertheless, the surface areas obtained were limited to few microns. Subsequently, several reports of large-area h-BN layers with high crystalline quality by metalorganic chemical vapor deposition (MOCVD) on sapphire, SiC, and AlN, have been reported[7], [51], [52].

Recently, our group at IRL 2958 Georgia Tech – CNRS reported 2-inch wafer growth of 2D h-BN on sapphire by MOCVD with continuous and uniform morphology over the surface[53]. The growth was performed in an Aixtron MOCVD close coupled showerhead (CCS) 3 x 2″ reactor using triethylboron (TEB) and ammonia (NH3) as B and N precursors, respectively. The layers were grown at 1280 °C in hydrogen ambient at 85 mbar, with

NH_3/TEB ratio of 1000. BN layers were grown directly on the 2-in. sapphire substrates with pre-flow of TEB but without any buffers. The BN growth was achieved using hydrogen as carrier gas. The total flow rate was 20 SLPM (standard litre per minute) and the total thickness of the layers varies according to the growth time from 3 to 60 nm for different samples based on the cross-section STEM characterizations.

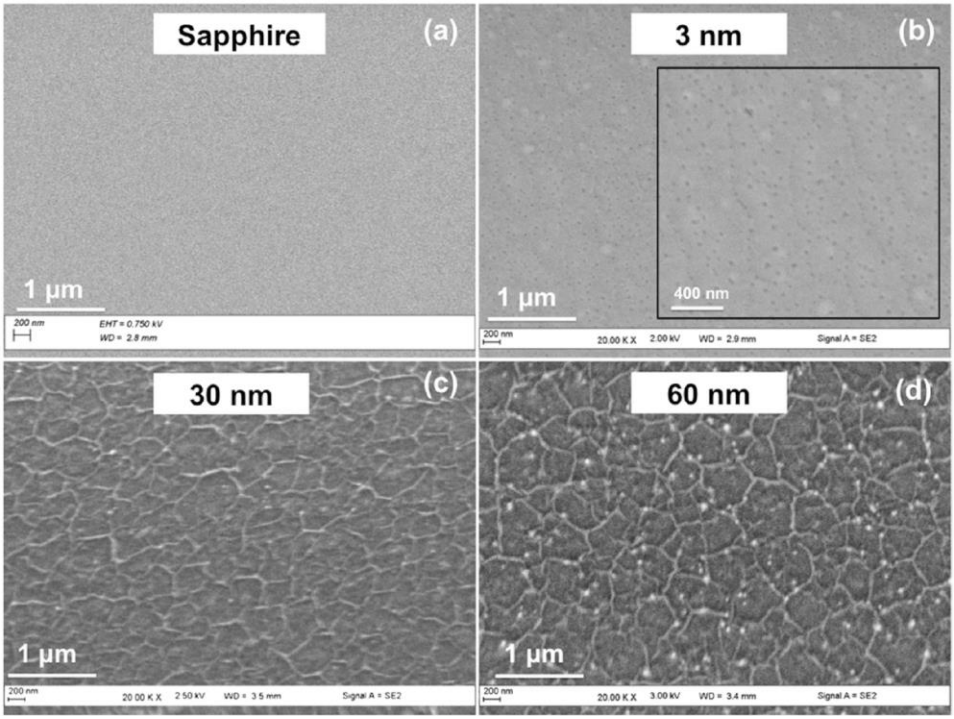

Figure 9 - SEM images of the sapphire substrate and 2D BN layers with different thicknesses. Adapted from[53].

The morphology change of the h-BN layers according to their thickness is shown in Figure 9. The crystal structure of 30 nm-thick h-BN was examined by high resolution X-ray diffraction (HR-XRD) scans, as shown in Figure 10. A clear symmetric diffraction peak is located at 26.0° that relates to hexagonal boron nitride (0002) crystal planes. The (0004) plane diffraction peak is also observed at 53.7°. The crystal lattice "c" is calculated to be 6.85 Å, which is in a good agreement with reported values[54]. The left inset of Figure 10 is the HR-XRD ω-scan in the triple-axis mode, which measures the mosaic spread. The

full-width at half-maximum (FWHM) is around 684 arcsec showing a highly oriented crystal structure along the c-axis. Raman measurement is shown in the right inset of the Figure 10. The spectrum of the thin BN film fitted with Cauchy−Lorentz distribution shows a peak at 1370 cm^{-1} that is attributed to the h-BN first-order Raman E_{2g} vibrational mode. The FWHM of the peak is 45 cm^{-1} which is comparable with what has been observed for single-crystal BN flakes fabricated by MBE and by CVD.

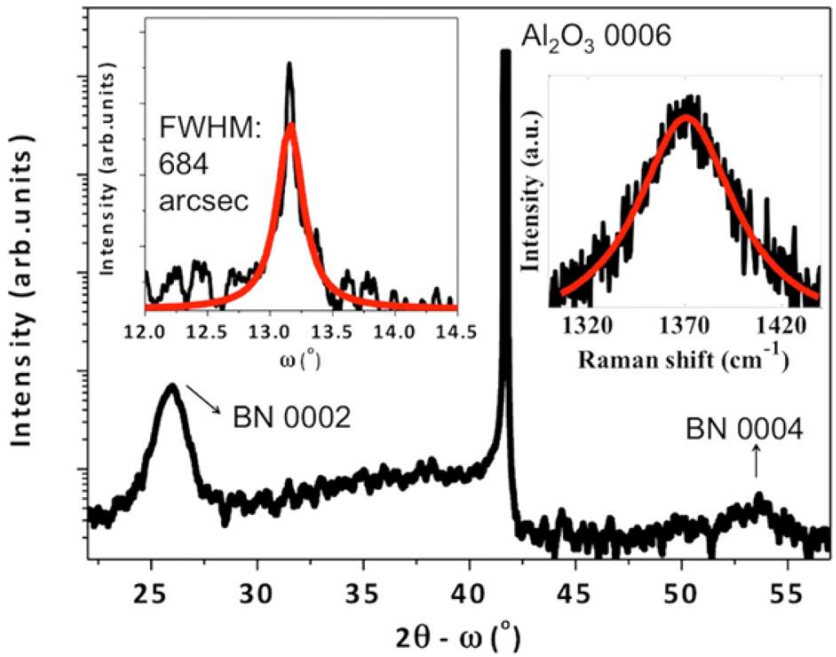

Figure 10 - High-resolution triple axis 2θ−ω scan of the 30 nm thick h-BN layer grown on sapphire; left inset shows the triple axis ω-scan along with Lorentz fit (red line) of the BN (0002) reflection. Right inset shows Raman spectrum. Adapted from[53].

This successful epitaxial growth of atomically flat 2D layered h-BN on sapphire paves the way to the development of flexible electronic and optoelectronic III-N components and their heterogeneous integration onto other platforms. These high-quality layers can also be used in a broad range of applications including vdWs heterostructures (2D-2D layered structures), graphene electronics (where h-BN is used as a substrate, protection, passivation and gate dielectric).

3.2 Van der Waals Epitaxy of InGaN/GaN Structures on 2D h-BN

3.2.1 Van der Waals Epitaxy of 3D Single-Crystals on 2D Materials

VdWs epitaxy is a 2D material-assisted growth method that recently received strong research interest owing to the ability to grow 2D and 3D single crystals on top of 2D materials having no dangling bonds and stacked via weak vdWs forces. This technique was first introduced by Koma et al.[55]–[58] in 1985 and recently renewed attention owing to the novel breakthroughs of research on 2D materials[46], [59].

It permits the growth of high-quality 3D crystals on 2D buffer layers with lattice mismatch greater than 60 %[1]. Moreover, since most 2D materials have a hexagonal lattice, the growth of III-N semiconductors having the same hexagonal lattice have been successfully demonstrated with high crystal quality. Chung et al.[60] reported GaN thin films on graphene-layered sheets using ZnO nanowalls as an intermediate layer while Kim et al.[5] demonstrated direct vdWs epitaxy of single-crystalline GaN layers on epitaxial graphene on SiC substrates. Furthermore, Kobayashi et al.[6] demonstrated the potential versatility of this approach by growing AlGaN/GaN heterostructures and InGaN/GaN multi-quantum well structures on h-BN in spite of the large lattice mismatch between h-BN and GaN (> 25 %), by adding a thin AlN buffer layer. Besides, this buffer layer works as a dislocation filter, decreasing the density of threading dislocations in the GaN to 8.6 x 10^9 cm^{-2}.

In this thesis, we have chosen 2D layered h-BN as a buffer layer to grow GaN-based LEDs instead of graphene because h-BN can be grown by MOCVD in the same run and same growth conditions as the LEDs structures which is very important for achieving high-throughput and low-cost industrial manufacturing.

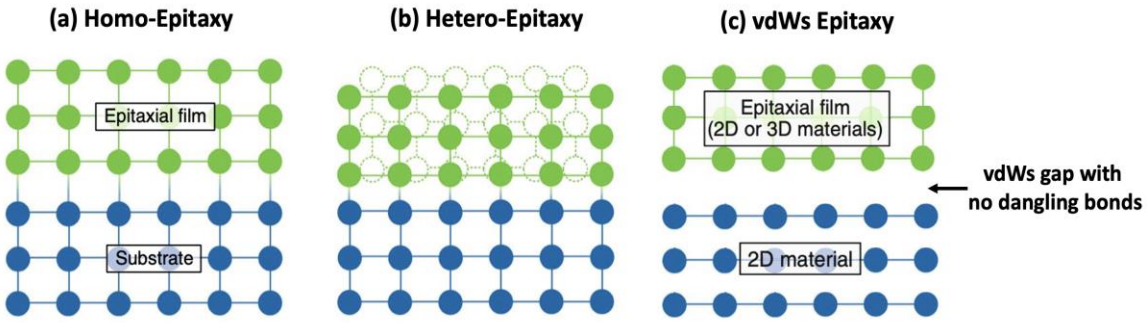

Figure 11 - Illustration of the two conventional (a) homo-epitaxy and (b) hetero-epitaxy together with (c) vdWs epitaxy of 2D or 3D materials on 2D substrates. Adapted from [1].

3.2.2 Van der Waals Epitaxy of InGaN/GaN Structures on 2D h-BN

The III-N research group at IRL 2958 GT-CNRS also recently reported the growth of InGaN/GaN MQW structures on h-BN/sapphire by MOCVD [11], [39]. The growth was performed in an Aixtron MOCVD CCS 3 x 2 in. system on the (0001) sapphire substrate. Triethylboron (TEB), trimethylgallium/triethylgallium (TMGa/TEG), trime-thylindium (TMIn), trimethylaluminum (TMAl), and ammonia (NH3) were used as B, Ga, In, Al, and N sources, respectively. Silane (SiH4) and Cp_2Mg were used as n-type and p-type doping sources, respectively. First, an h-BN layer (5 nm) was grown on the sapphire substrate at 1300°C. Then, an intermediate Si-doped AlGaN layer (250nm) with an Al mole fraction of 14% was grown at 1100°C. This layer acts as an interfacial buffer between sp^3-bonded 3D epitaxial films and 2D h-BN and promotes nucleation. The InGaN/GaN MQW structure consists of a Si-doped GaN layer (500 nm), 5-periods of InGaN/GaN multi-quantum wells

(MQWs), and a Mg-doped GaN layer (250 nm). The MQW structure consists of a 12-nm-thick GaN barrier layer and a 2.5-nm-thick InGaN quantum well layer with an In mole fraction of 15%. The electron and hole carrier concentrations in the Si- and Mg-doped GaN layers are 5 x 10^{18} and 1 x 10^{17} cm^{-3}, respectively. Figures 12a and 12b show the schematic of the grown structure and the wafer photograph after growth, respectively.

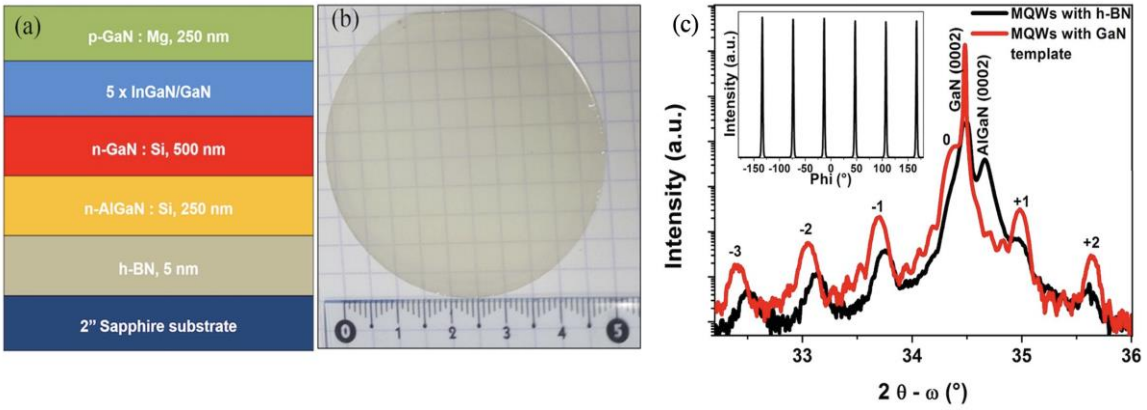

Figure 12 - Schematic illustration of the grown structure and (b) the resulting transparent wafer photograph after epi-growth. (c) HR-XRD $2\theta - \omega$ of the MQW structure on the h-BN and the same structure using conventional GaN template. The inset shows the HR-XRD azimuthal off-axis phi scan of GaN (102) on AlGaN/h-BN. Adapted from [39].

The growth of the GaN-based layers on the ultra-thin h-BN is governed by vdWs epitaxy. As discussed in the previous sub-section, in contrast with conventional homo- and hetero-epitaxy, vdWs epitaxy does not involve strong chemical bonds between the epilayer and the substrate; instead, it only requires either the substrate or the overlayer to have a surface free of active dangling bonds[56] such as layered materials[61] which is the case for h-BN. In this study, an AlGaN interfacial buffer is used between h-BN and GaN. In situ reflectance clearly indicates uniform nucleation and subsequent coalescence of AlGaN islands with a 250 nm thick growth. This can be explained by the high sticking coefficient of Al on h-BN at high temperatures. Complete recovery to 2D surfaces is achieved with further GaN growth. The phi scan for a (102) plane of GaN on AlGaN/h-BN was performed

and is shown in the inset of Figure 12c. The six-fold symmetry of the diffraction peaks of GaN (102) planes with 60° intervals. Subsequently, an MQW structure was grown. The crystallographic properties of the MQW structure on h-BN in comparison with the MQW structure on a conventional GaN template were analyzed by high resolution X-ray diffraction (HR-XRD) using $2\theta - \omega$ configuration and the scans are shown in Figure 12c. In the case of the MQW structure on the conventional GaN template, one can observe the intense GaN peak and satellite peaks from the MQWs up to the third order with pendellosung fringes, indicating good periodicity and abrupt interfaces in the quantum wells. For the MQWs sample with an h-BN layer, the satellite peaks from the MQWs up to the third order were also observed, along with the GaN (0002) and AlGaN (0002) diffraction planes. Figure 13a shows TEM image of the grown structure on h-BN/sapphire and Figure 13b shows photoluminescence (PL) mapping over the entire 2-inches wafer. The average emission wavelength is 475 nm and the standard deviation of the peak wavelength is 0.8%.

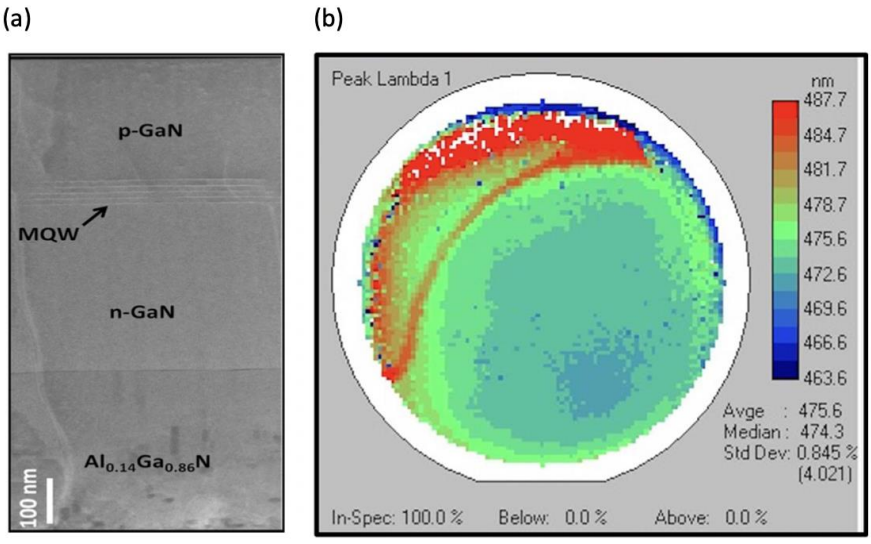

Figure 13 - (a) TEM image of the grown structure. (b) Wavelength distribution of photoluminescence mapping performed at room temperature. Adapted from [11].

This series of structural and optical characterizations demonstrate the ability to grow epitaxial InGaN-based structures on h-BN with good quality that can operate as photovoltaic devices LEDs. Subsequently, devices were fabricated on native substrate and transferred to foreign substrates such as glass (Figure 14).

These promising results opened up the way to the fabrication of highly efficient III-N electronic and photonic devices on hBN/sapphire for heterogeneous integration and flexible electronics. However, further improvement to the overall wafer-scale lift-off process is needed in order to obtain wafer-scale crack-free surfaces. During this thesis, advanced processes were developed for this purpose and are extensively presented in the next chapters.

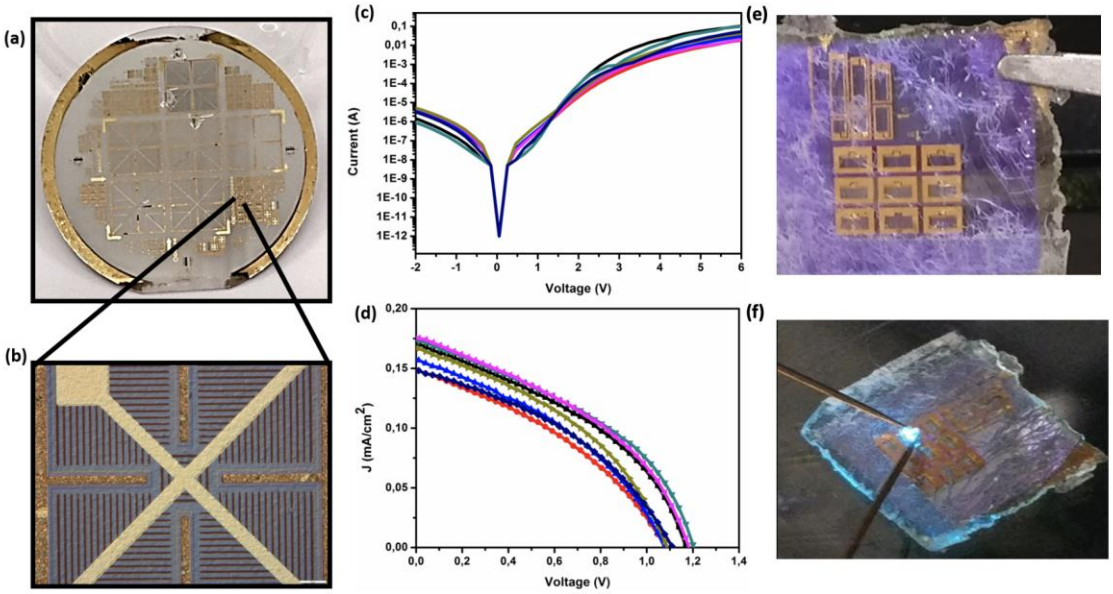

Figure 14 - (a) Photograph of the fabricated solar cells on 2 in. h-BN/sapphire. (b) Optical microscopy image of a ~1 mm^2 solar cell. (c) Dark I−V curves of devices in different locations on the wafer and their corresponding illuminated J−V curves under AM 1.5 condition in (d). (e) Photograph of solar cells on the release tape and (f) photograph of solar cells on the receiving glass substrate during I-V measurements. Adapted from [11].

CHAPTER 4. FABRICATION AND TRANSFER OF INGAN LEDS GROWN ON 2D H-BN

In the recent years, innovation in heterogeneous integration of functional III-N layers and devices has received considerable attention and has opened a world of new applications for electronic and opto-electronic systems through novel lift-off and transfer technologies.

One of the goals of this thesis is to develop efficient, large-scale and low-cost processes for heterogeneous integration of InGaN-based LEDs grown on 2D layered h-BN. In the state of the art of this type of devices reported in Chapter 2, we mentioned two critical weaknesses of existing processes that are (i) the delamination of the h-BN and GaN-based epilayers grown of top of it and (ii) the high number of cracks that are introduced during the lift-off and transfer steps. In order to reach industrial manufacturing maturity, innovative solutions are needed. In this chapter, we present the results of novel fabrication methods we developed to overcome the above-mentioned issues. These advanced processes were named (1) selective area van der Waals epitaxy (SAVWE) and (2) self-lift-off and transfer (SLOT).

In Section 4.1 we demonstrate the capabilities of SAVWE to limit delamination and cracks in the 2-inches wafer and to enable a reliable pick-and-place of selected lateral LED devices whereas in Section 4.2 we undergo a side-by-side comparison of lateral LEDs grown on layered h-BN with and without SAVWE. A benchmarking and testing of all the process steps from epitaxy, to device fabrication, lift-off, and transfer of devices has been

performed. In Section 4.3 we introduce the SLOT process for an efficient fabrication of large-area crack-free free-standing LED membranes. As a proof of concept, vertical thin-film (VTF) LEDs are fabricated on these membranes and electro-optically characterized and compared to lateral LEDs.

4.1 Selective Area van der Waals Epitaxy (SAVWE)

In order to avoid delamination and cracks of h-BN on large diameter substrate one solution could rely on making the h-BN regions smaller and physically separated by a selective mask. This selective area van der Waals epitaxy (SAVWE) would also enable a pre-die separation before the growth since the growth wafer surface is subdivided into delimited areas chosen for device locations. This would facilitate the device-by-device pick-and-place without the need for a dicing step. In addition, the selective area growth of h-BN and the subsequent GaN-based epilayers could allow to improve the material quality by reducing the density of threading dislocations.

To achieve these structures a 2-inches diameter wafer surface is subdivided into small areas ranging from 1 mm^2 to 1 cm^2 by means of a SiO_2 mask, as illustrated in Figure 15. After the growth of a 3 nm h-BN layer, the InGaN-based epilayers are then selectively grown. Figure 15 [62] shows a schematic of several devices separated by the SiO_2 mask. After fabrication, the devices can be released individually and placed on a specific carrier position in an integrated circuit for example, as illustrated in Figure 15c and 15d.

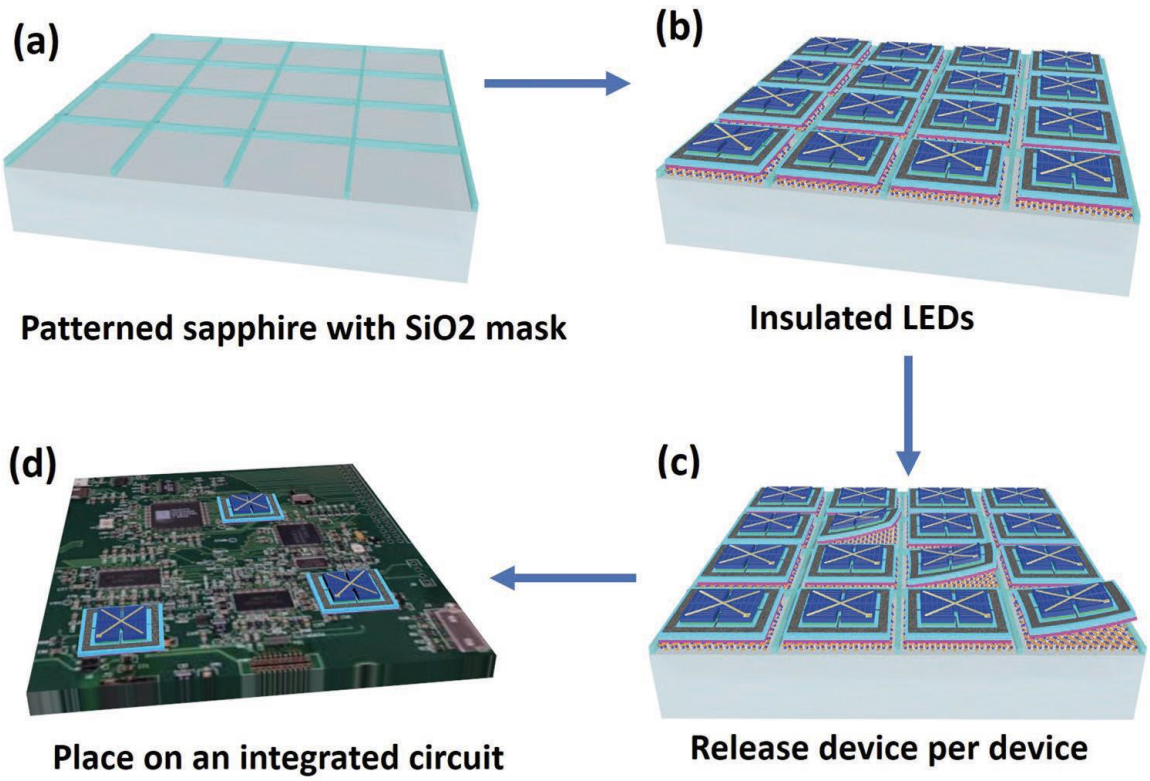

Figure 15 - (a) A large-surface sapphire wafer patterned into small areas using a SiO_2 mask (b) Insulated grown and fabricated devices on h-BN (c) The devices can be released from the sapphire one by one and (d) placed on an integrated circuit [62].

4.1.1 Growth of LED Structures on 2D Layered h-BN

Since h-BN is of key importance for the transfer method, we first investigated its growth using a patterned wafer. A-400-nm-thick SiO_2 mask has been fabricated on a sapphire substrate and then we have performed the growth of 20 nm h-BN. As shown in Figure 16, high resolution X-ray diffraction (HR-XRD) scans give a clear symmetric diffraction peak located at 25.8° that relates to hexagonal boron nitride (0 0 0 2) crystal planes. The quality of the localized h-BN on sapphire is similar to the one on unpatterned substrate as it can be seen by the wrinkles in the left inset scanning electron microscope (SEM) images of Figure 16, which are characteristic of the 2D layered h-BN. The h-BN

growth is very localized with no visible connection between the BN layers on the mask and on the sapphire surface, as confirmed by the tilted SEM image showing the mask sidewall with isolated BN crystallites. On the SiO_2, randomly oriented BN has been grown showing a radical difference in quality between BN on dielectric SiO_2 and on sapphire substrates.

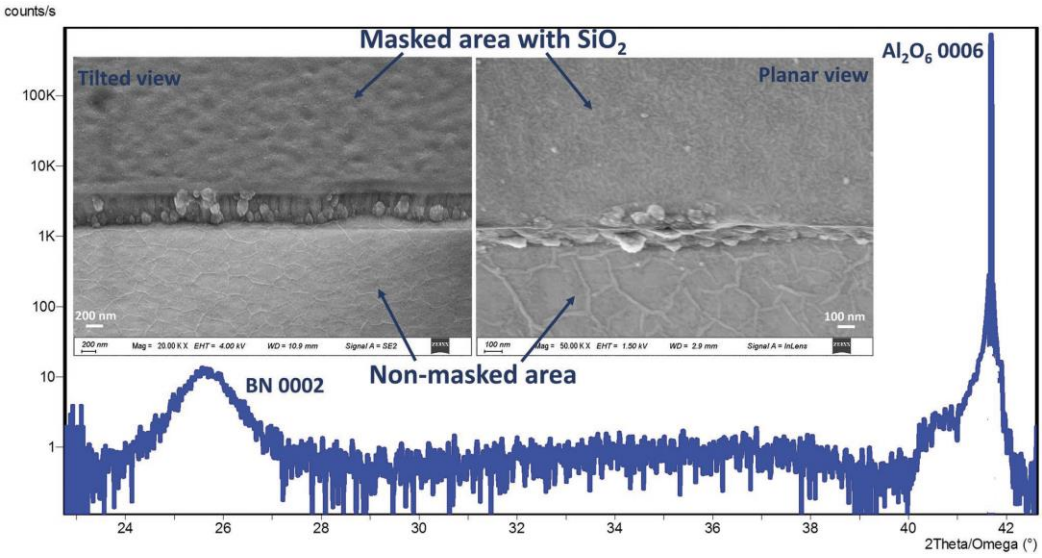

Figure 16 - High-resolution triple axis $2\theta - \omega$ scan of the 20 nm thick h-BN layer grown on a patterned sapphire. Left and right inset show a 45° tilted SEM image of the 20 nm h-BN layer grown on a patterned sapphire, and a planar SEM image, respectively [62].

After studying the growth of the h-BN layer using patterned sapphire, we have performed a series of runs to grow InGaN-based LEDs using h-BN/patterned sapphire substrates. The LED structure, shown in the inset of Figure 17d, consists of five InGaN/GaN quantum wells sandwiched between 0.5 μm n-GaN and 0.25 μm p-GaN layers. This structure is grown on 3 nm h-BN using a 250 nm $Al_{0.14}Ga_{0.86}N$ nucleation layer. The SEM images in Figure 17c show the selective growth of the LED structure in regions where layered h-BN is deposited, avoiding the growth on randomly oriented BN on SiO_2. The inset image shows very sharp sidewalls of the LEDs structure in each side of the mask which is required to guarantee the separation between the devices after process fabrication. To avoid the

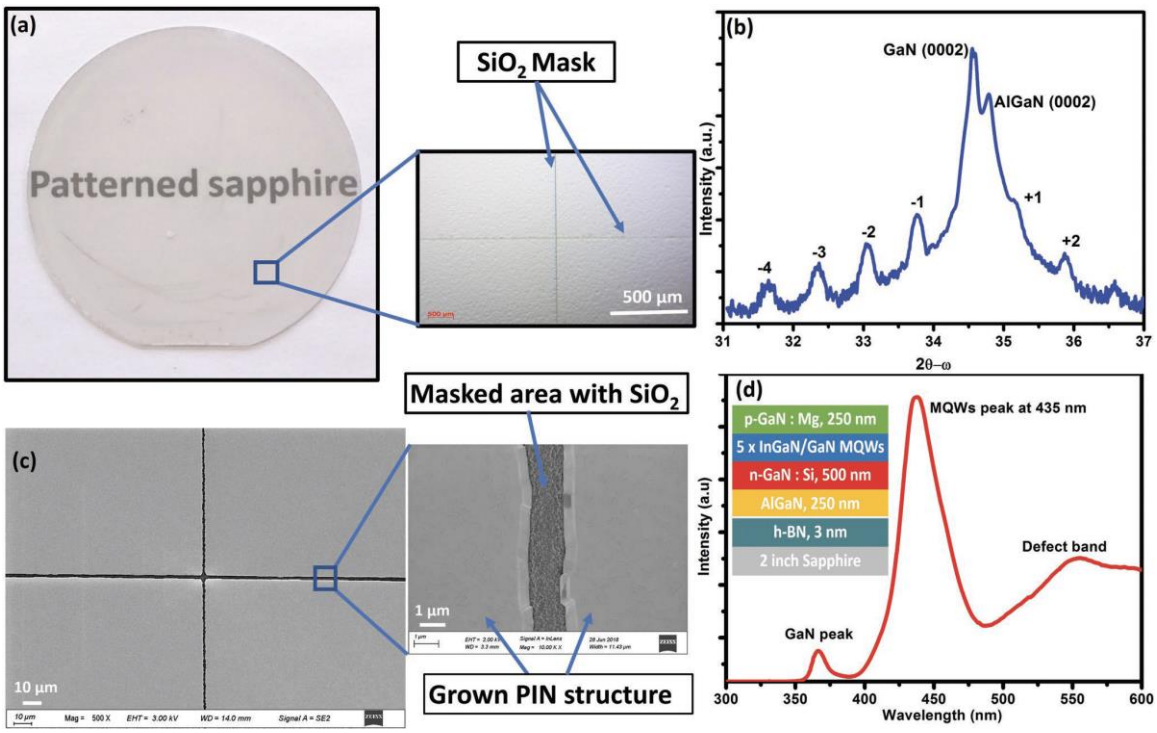

Figure 17 - (a) As-grown LED structure on 2 in. patterned sapphire, inset: optical microscope image showing separated growth areas (b) High resolution X-ray diffraction $2\theta - \omega$ scans of the grown structure (c) SEM images of the locally grown LEDs structure (d) CL spectrum recorded at room temperature under excitation of 5 keV, the inset shows the grown structure [62].

coalescence of the approximately 1-µm-thick grown structure due to the lateral growth, the SiO_2 mask thickness was chosen to be 400 nm. The high-resolution X-ray diffraction $2\theta - \omega$ scan around the (002) of the grown structure on the patterned sapphire is shown in Figure 17b. The scan clearly delineates the InGaN satellite peaks up to the fourth order as well as the peaks from the GaN and $Al_{0.14}Ga_{0.86}N$ layers. Optical characteristics of the multi-quantum well (MQW) structure have been investigated, as shown in Figure 17d. Depth resolved cathodoluminescence (CL) spectrum for the MQW structure are recorded at room temperature with an electron beam excitation energy of 5 keV. A MQW emission peak around 435 nm has been obtained which corresponds to 14% In content in the quantum wells. These series of characterizations demonstrate the ability to selectively grow InGaN-

based structures on a localized 2D layered h-BN with good quality using a 2-inches patterned sapphire wafer.

4.1.2 Fabrication and Transfer of LEDs on 2D Layered h-BN

Several LEDs with various chip designs and sizes were fabricated using a 2-inches grown sample, as shown in Figure 18b. Figure 18a shows a set of eight devices with a 1 mm^2 area and different designs that are insulated by the SiO_2 mask. The use of sacrificial h-BN for wafer-scale fabrication poses a processing challenge because spontaneous delamination of the grown structure can occur during device fabrication. In our experiment,

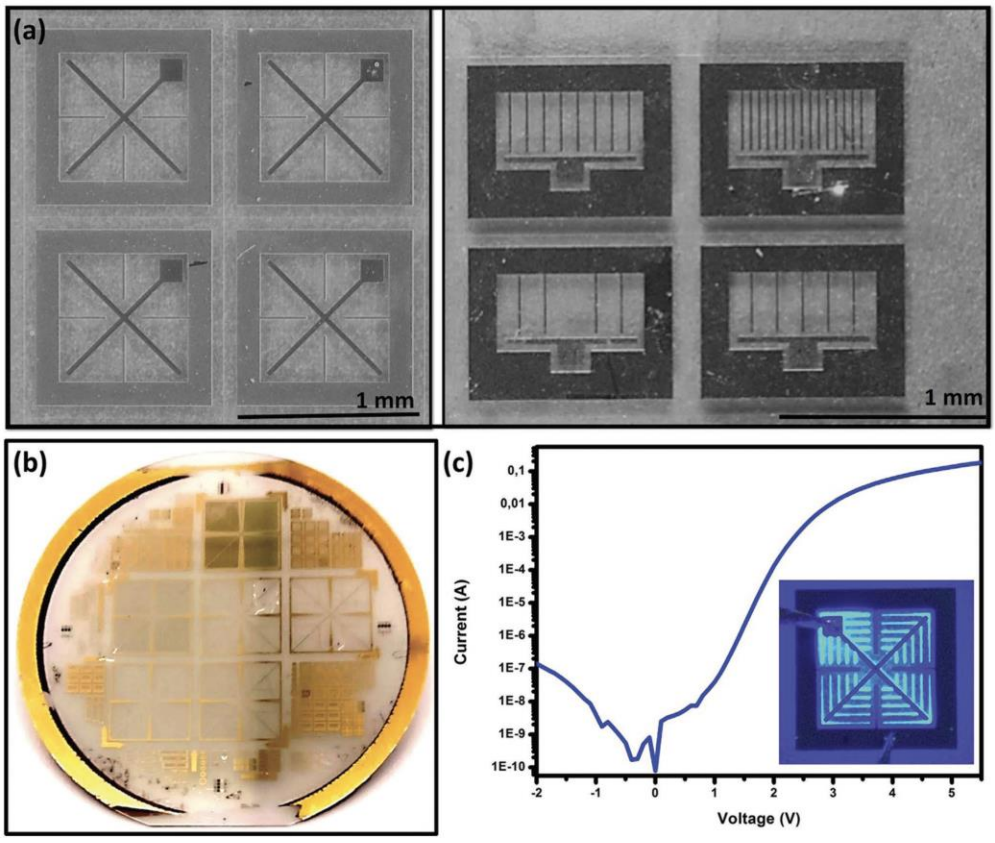

Figure 18 - (a) Optical microscope images of eight devices with 1 mm^2 area and different designs, separated by the SiO_2 mask (white lines around the devices) and ready for pick-and-place (b) Photograph of the wafer-scale processed discrete LEDs (c) I–V characteristic of a fabricated device emitting blue light shown in the inset [62].

a standard photolithography-based process has been applied while contact with liquids was limited and no ultrasonic cleaning was used. After fabrication, I–V measurements were performed as shown in Figure 18c with an inset exhibiting blue light emission from a LED device. Thanks to the patterning with the SiO_2 mask, the fabricated devices are already physically insulated from each other. The discrete LEDs can be released and transferred individually without the need for a dicing step. In this work, a selected set of devices has been released by means of a water-dissolvable tape and transferred to a flexible aluminium tape. The tape is attached to a carrier for release. Then, once the device is placed on the final substrate, the tape is simply removed by dissolving it in water for around 1 min. The pick-and-place capability is demonstrated in Figure 19a where we clearly see that some devices have been lifted off from sapphire leaving their locations empty while other LEDs were kept on the growth wafer. During the transfer process, device structures remained completely intact and free from cracks and metallic contact damage. This crack-free transfer has been achieved primarily thanks to the optimized vertical lift-off of the devices. A setup has been adapted to only enable a vertical movement during the device release step and avoid peeling off which induces strains on the surface and therefore cracks. Figure 19b shows an LED after its release from the growth wafer and its transfer to an aluminium tape, respectively. I–V measurements for a same LED were performed before and after its transfer to confirm the preservation of the device functionality, as shown in Fig 19c with an inset exhibiting blue light emission from the device on the aluminum tape. In this work, the LEDs have been placed on the flexible final substrate with the p-side on top which is appropriate for this type of application. We should note that the proposed pick-and-place process could be adapted for other application like displays where the LEDs need to be

placed up-side down in contact with an IC driver. For this case, one more transfer step after devices release is needed and can be easily implemented.

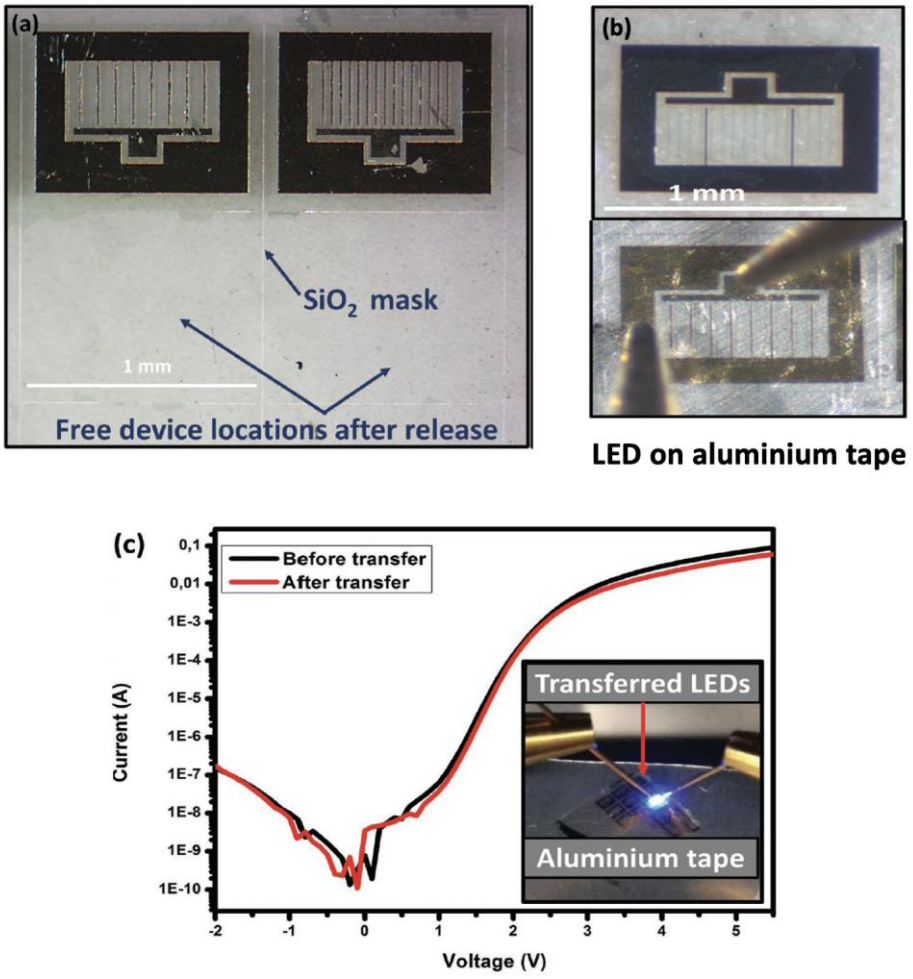

Figure 19 - (a) Optical microscope image showing empty locations of two lifted off LEDs and two other LEDs kept on the patterned sapphire (b) Microscope images from the backside of an LED on a water dissolvable tape after release and an LED after its crack-free transfer on a flexible aluminium tape (c) I–V characteristics of a same device before and after its transfer with its blue light emission shown in the inset [62].

In summary, this work demonstrates a wafer-level mass manufacturable approach for the heterogeneous integration of III-nitride devices using 2D h-BN, which is robust and facilitate a simple device-level pick-and-place. The key step in the proposed solution is the patterning of the sapphire wafer to laterally control the h-BN quality and separate the device locations. Discrete blue LEDs have been fabricated on 2 in. patterned sapphire wafer

with a SiO_2 mask. Subsequently, a set of devices have been mechanically released from the growth substrate thanks to the 2D layered h-BN and transferred on a flexible aluminum tape without damage.

The results presented here provide viable routes to the development of advanced III-N-based integrated devices at industrial scale. However, more detailed study is needed to understand the effect of this selective area growth on material quality, device transfer efficiency and device performances before and after transfer. For this purpose, we have performed a side-by-side study of LEDs grown on layered h-BN with and without SAVWE. A benchmarking and testing of all the process steps from epitaxy, to device fabrication, lift-off, and transfer of devices have been performed. Millimetric-size LEDs were fabricated on patterned and unpatterned sapphire substrates and then released from their native substrates and transferred to different host substrates.

4.2 Comparison of Patterned and Unpatterned LEDs on h-BN

4.2.1 Growth of Patterned and Unpatterned LEDs on 2D Layered h-BN

Two sets of LEDs heterostructures have been grown by MOCVD. The epilayers were grown in an Aixtron MOCVD CCS 3x2'' reactor on (0001) 2-inches sapphire wafers. A 3 nm thick h-BN layer was first grown at 1300°C. Then, an intermediate 200 nm thick AlGaN layer with an Al mole fraction of 14% was grown at 1100°C. This layer acts as an interfacial buffer between sp^3-bonded epitaxial films and layered h-BN and promotes nucleation. The LED structure comprises a 300 nm thick Si-doped GaN layer, 5-periods of InGaN/GaN multi-quantum wells (MQWs), and a 175 nm thick Mg-doped GaN layer. The 5 QWs structure consists of a 12-nm-thick GaN barrier layer and a 2.5-nm-thick InGaN QW layer with an In mole fraction of 15%. The electron and hole carrier concentrations in the Si- and Mg-doped GaN layers are 5×10^{18} and 1×10^{17} cm^{-3}, respectively. For the patterned substrate, an SiO_2 mask was achieved by a photolithography-based process on an epi-ready sapphire substrate. 400 nm-thick SiO_2 layer was deposited by plasma-enhanced chemical vapor deposition (PECVD) on a 2-inches sapphire wafer and the patterns were defined by optical lithography. The devices locations were opened by etching SiO_2 by buffered oxide etch solution. Then, hBN and subsequent layers were grown similarly to the unpatterned substrate. The schematic of the 2 epitaxial structures grown on unpatterned and patterned sapphire substrates are shown on Figure 20 [63]. Both sets of structures were grown in the same runs.

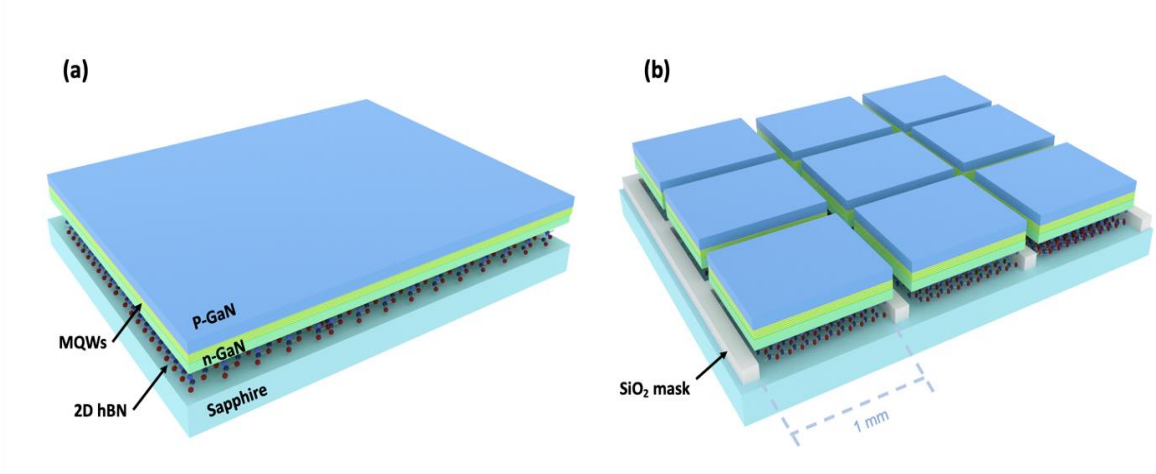

Figure 20 - Schematics of the two grown structures: (a) LEDs on h-BN/unpatterned sapphire, (b) LEDs on h-BN/patterned sapphire with SiO_2 mask [63].

In-depth structural characterizations have been conducted after the growth. Figure 21a shows HR-XRD 2θ - ω scans of the two heterostructures. Both X-ray diffraction spectra are comparable. One can observe an intense GaN peak and several satellite peaks from the MQWs up to the fifth order with Pendellosung fringes indicating good periodicity and abrupt interfaces in the quantum wells. GaN (0002) and AlGaN (0002) diffraction peaks are also observed. Interestingly, the GaN (0002) ω-scans, depicted in Figure 21b, shows smaller full-width at half-maximum (FWHM) for the patterned structure (1044 arcsec) than the one of the unpatterned heterostructure (1584 arcsec) indicating better overall crystalline quality since in wurtzite GaN films the broadness of symmetric (0002) ω-scan spectra is mainly related to the presence of dislocations. This is confirmed by the TEM analysis of both types of structures. As shown in Figure 22a and 22b, a significant reduction of the threading dislocation density is observed in the patterned structure in an area close to the SiO_2 mask (few tens of microns) compared to the unpatterned structure. These can be explained by the mechanism of the growth of 3D layers on 2D crystals. Indeed, since both structures were grown on h-BN surface having no dangling bonds, the threading

dislocations are mostly originating from the AlGaN islands formation during the nucleation layer on h-BN. SAVWE likely promotes the growth of large AlGaN and h-BN islands close to the mask leading to the lateral coalescence with less generation of stacking faults and dislocations than in the case of the growth on unpatterned substrate.

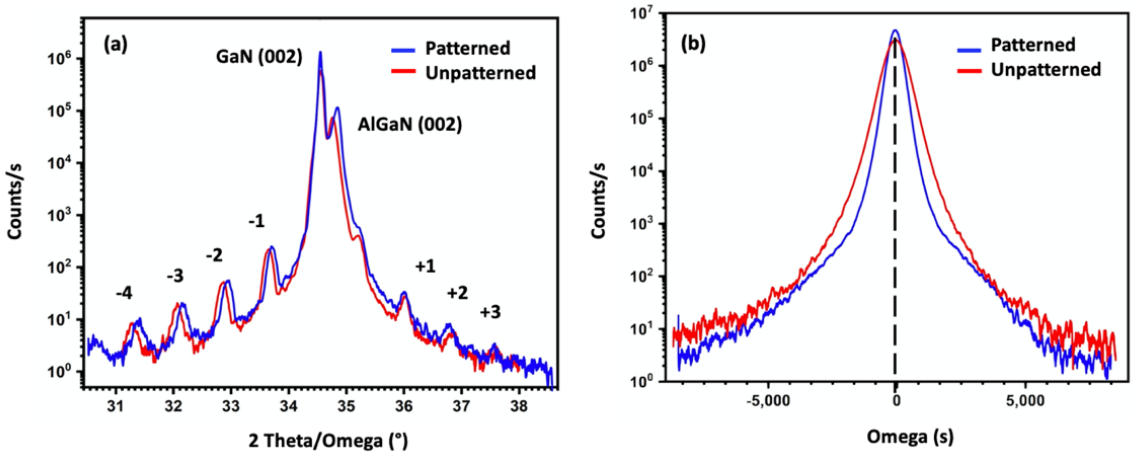

Figure 21 - (a) High resolution X-ray diffraction 2θ - ω scans of the two grown samples. (b) High resolution X-ray diffraction ω-scans of the two grown samples along the GaN (0002) reflections [63].

Optical characteristics of the MQW structures have been investigated, as shown in Figure 22c. For that, cathodoluminescence (CL) spectra of both structures were recorded at room temperature with an electron beam excitation energy of 8 keV and normalized with respect to the GaN CL peak intensity. For both structures a MQW emission peak around 445 nm has been obtained which corresponds to 14 % In content in the quantum wells. The corresponding peak intensity is significantly higher for the patterned structure (x1.5) than the one of the unpatterned structures. This result is in good agreement with TEM and X-ray diffraction data and can be expected since the threading dislocations act as nonradiative recombination centers and impact the luminescence.

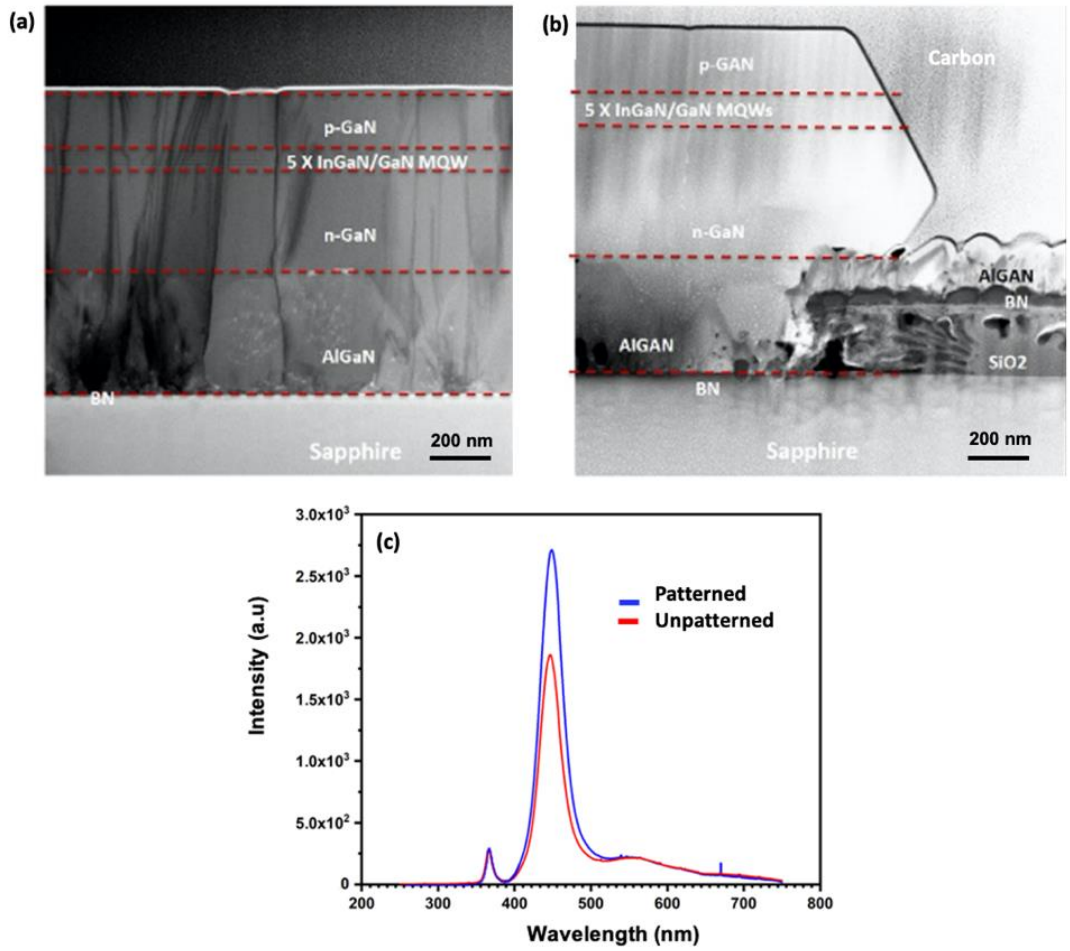

Figure 22 - (a) TEM image of the unpatterned sample, (b) TEM image of the patterned sample, (c) Cathodoluminescence spectra at 8 kV recorded on both structures at room temperature. Both spectra have been normalized with respect to their GaN peak intensity [63].

High resolution X-ray diffraction (HRXRD) scans were performed in Panalytical X'pert Pro MRD system with Cu Kα radiation. The samples were prepared for STEM using focused ion beam (FIB) thinning and ion milling. 100-nm-thick carbon was deposited before FIB in order to protect the surface. Then, the high-angle Annular Dark Field Scanning Transmission Electron Microscopy (HAADF-STEM) was performed on an aberration-corrected JEOL 2200FS electron transmission microscope. Depth resolved cathodoluminescence (CL) spectra were measured with Horiba HR-320 system.

4.2.2 Fabrication and transfer of LEDs to arbitrary substrates

The fabrication of the LEDs was based on a standard photolithography process whereas contact with liquids was limited and no ultrasonic cleaning was used to avoid delamination. Dry etching was accomplished by Cl_2/Ar inductively coupled plasma (ICP). Ti/Al/Ni/Au and Ni/Au layers, deposited by e-beam evaporation, were used for the n-contact and p-contact, respectively. The n-contact was annealed at 850 °C for 30s under N_2 and the p-contact was annealed at 600 °C for 60s under O_2.

The fabricated LEDs had an area of 1 mm x 0.5 mm with n-contact surrounding the device and 16 fingers for the p-contact. After fabrication of LEDs on both structures, few mm^2 surface areas containing four LEDs were released by mean of water-soluble tape through a vertical lift-off that minimizes induced shear strains in the device layers and transferred from the two structures to an aluminum tape containing a 5-µm-thick acrylic adhesive layer. Figure 23a and 23b show microscope images of transferred unpatterned and

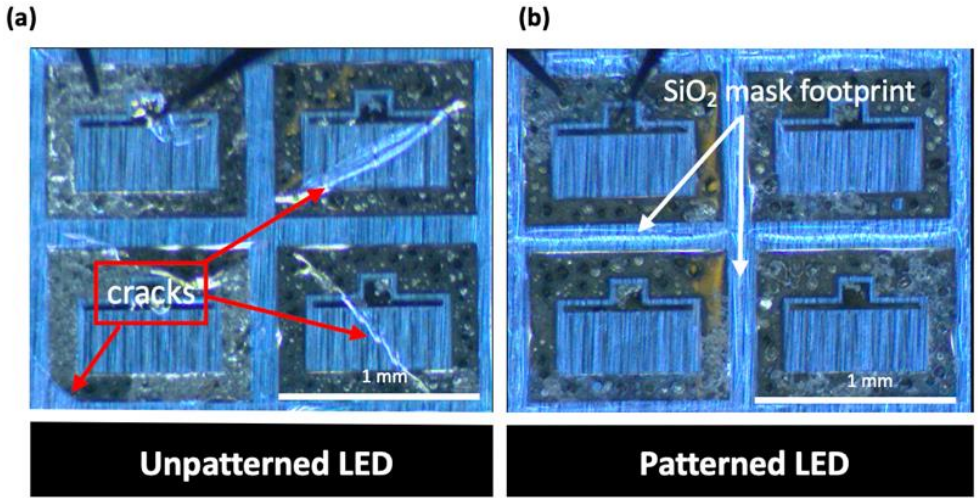

Figure 23 - Optical microscope images of large area LEDs released and transferred to aluminum tape from (a) unpatterned and (b) patterned structures. Several cracks are observed for devices released from the unpatterned structure [63].

patterned LEDs, respectively. The transferred LEDs from the patterned structure were crack-free while those transferred from the unpatterned structure showed large cracks crossing half of the devices. Analysis was conducted on 20 released LED devices from each sample. 18 functional devices without cracks were obtained on patterned devices while 6 crack-free LEDs were obtained on unpatterned devices. This results correspond to a yield increase from 30% to 90% and are another proof of efficiency of SAVWE approach.

Subsequently, device transfer to silicon rigid substrate was attempted. For efficient comparison, slightly smaller (1 mm x 0.5 mm) LEDs were considered to avoid too many cracks in devices transferred from the unpatterned structure. This transfer on rigid and non-sticking substrates was achieved using water capillary force and without the use of an intermediary adhesive layer. First, a small droplet of water was deposited on the host substrate, then the mechanically released LEDs were applied on the receiving substrate. As

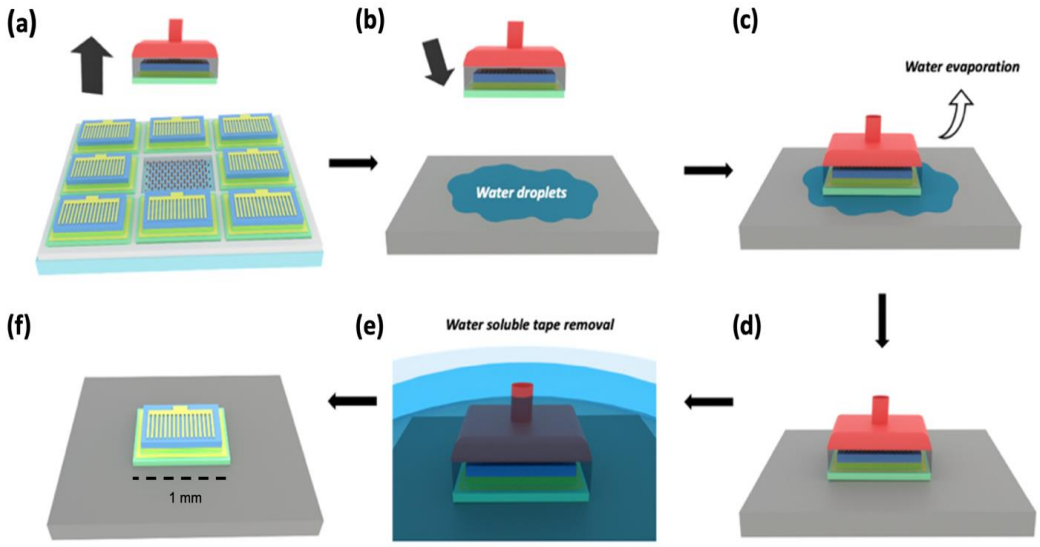

Figure 24 - Schematics of the lift-off and van der Waals bonding transfer on rigid substrate. (a) Vertical release from h-BN/sapphire native substrate (b) water droplets deposition of silicon (c) deposition of released LEDs onto silicon (d) vdWs bonding on silicon after water evaporation (e) water soluble tape removal (f) LED transferred to silicon [63].

the water evaporates, it pulled the surfaces together by capillary action until a robust and uniform vdWs bonding was obtained. The top tape was then dissolved in water and the transferred devices were cleaned by a flow of acetone and isopropanol to remove any remaining residues. The process flow illustration of this transfer is given in Figure 24.

Figure 25 shows representative microscope images of the devices taken at the different steps of the transfer process for both unpatterned and patterned structures: after the fabrication process, lift-off, and transfer on aluminum tape and silicon substrate. As it can be seen, the lift-off step is achieved without any cracks whatever the structures. It is also

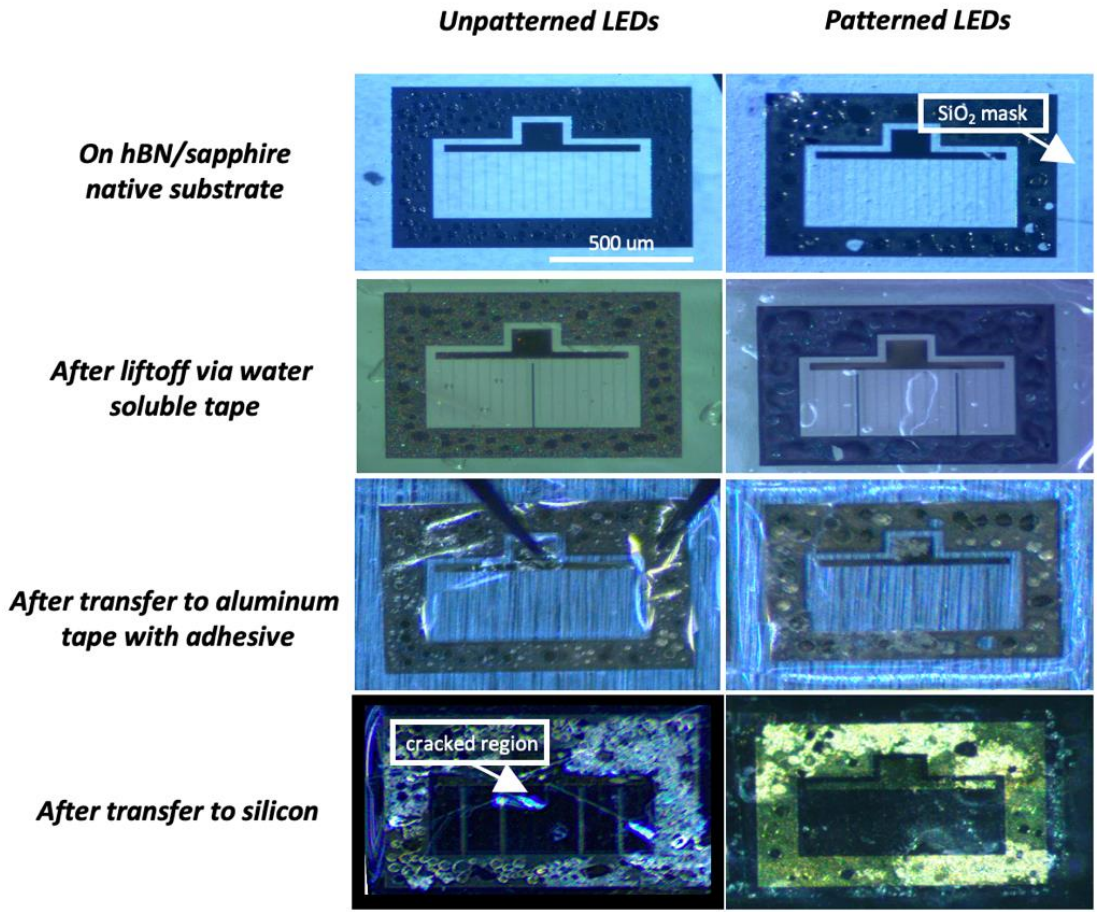

Figure 25 - Microscope images of the devices taken at the different steps of the transfer process for both unpatterned and patterned structures: after the fabrication process, lift-off, and transfer on aluminum tape and silicon substrate [63].

the case for the transfer to aluminum tape, even if the yield is a bit higher for the devices transferred from the patterned structure. Surprisingly, we were not able to transfer crack-free devices on silicon substrate from the unpatterned structure while we achieved systematically crack-free transfer from the patterned one.

4.2.3 Electro-Optical Characterization of LEDs Before and After Transfer

Figure 26a shows electro-luminescence images of the LEDs from both structures recorded, for a pulsed (15 ms duration, duty cycle of 0.5) electric current of 100 mA, before and after the fabrication process and transfer on aluminum tape (for reference) and silicon substrate. Electroluminescence images were taken by a CCD camera and optical emission versus time measurements were performed using a silicon photodiode connected to an oscilloscope. Figure 26b is a photograph of light emission from an LED on silicon. In Figure 26a, one can see that for devices transferred to aluminum tape, the luminescence is relatively higher in the case of the patterned LEDs. Moreover, in both structures the center of the LEDs looks darker than the edges. We attributed this attenuation to the current induced heating and poor thermal dissipation due to the acrylic layer of the tape which has a low thermal conductivity. It is to be noticed that this effect is more pronounced in the case of the unpatterned LEDs. This could be related to the high density of dislocations in the unpatterned structures as it is well known that the threading dislocation lines have an adversely effect on the thermal conductivity of III-N semiconductors because of the phonon-dislocation scattering mechanism. Also it has been reported that micro-cracks in the materials reduces significantly the thermal conductivity because the heat transfer by radiation or convection across the cracks is completely absent.

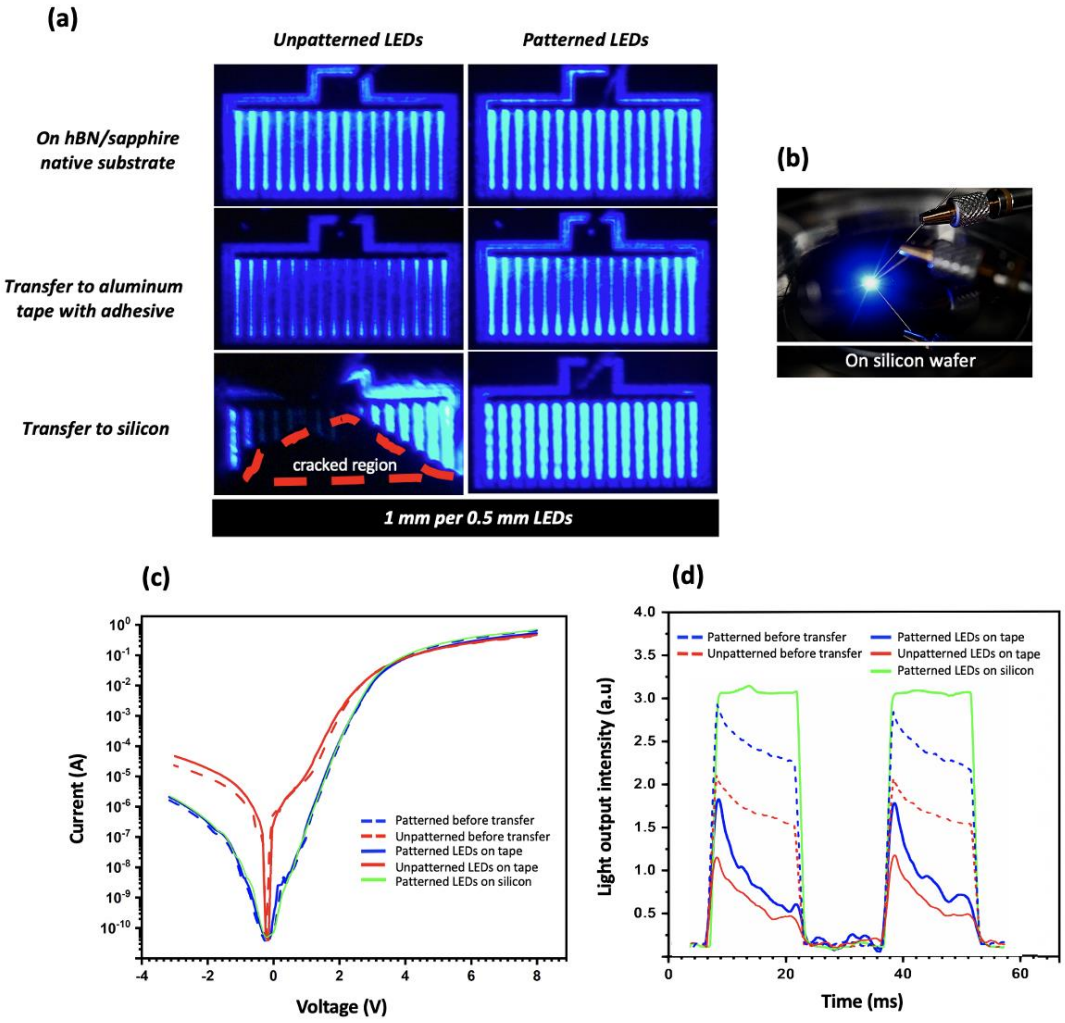

Figure 26 - (a) EL images of LEDs before and after transfer to different substrates (b) Photograph of light emission from an LED on silicon (c) I–V characteristics of LEDs before and after transfer to aluminum tape and silicon (d) Light output versus operation time of patterned and unpatterned devices before and after transfer to aluminum tape and silicon [63].

Homogenous and more intense electro-luminescence was obtained for patterned LEDs transferred to silicon substrate. This is a clear evidence of the good vdW bonding between the device and the silicon substrate which allows for an efficient thermal dissipation thanks to the relatively high thermal conduction of the silicon. Electro-luminescence was obtained also in the unpatterned device transferred on silicon substrate. Nevertheless, due to the

cracks in the devices, current was able to flow only in a small part of the device, leading to high local current density and electro-luminescence.–In addition, quantitative electro-optical characterization was conducted through pulsed current-voltage measurements on LEDs before and after transfer. Results are shown in Figure 26c. I-V measurements were achieved by an automated probe station. The data of the unpatterned LED on silicon were not reported because of its leaky behavior likely due to the cracked area. All the other devices exhibited a turn-on voltage around 3V. Clearly, unpatterned LEDs showed degraded behavior with reverse leakage current more than one order of magnitude larger than in the case of patterned LEDs. Forward current below the turn-on voltage due to recombination in the depletion region is also two order of magnitude higher. It is also to be noticed that patterned LEDs showed very little variation of their I-V before transfer and after transfer on either aluminum tape or silicon substrate. On the contrary, unpatterned LEDs came with larger alteration, such as higher reverse leakage and lower forward current of the I-V behavior.

The role of the thermal dissipation in the inhomogeneity of the electro-luminescence of the different LEDs is clearly evidenced in Figure 26d showing the time dependence of the emitted optical power of the patterned and unpatterned LEDs before and after transfer and recorded for a pulsed (15 ms duration, duty cycle of 0.5) electric current of 100 mA. These data confirmed what was qualitatively observed on Figure 26a. First, the LEDs transferred on aluminum tape show some degradation of the output optical power which is even more pronounced in the case of the unpatterned LEDs. Second, except for the patterned LEDs transferred on silicon for which the optical power showed a plateau-like behavior during the full duration of the current impulse, the other LEDs before and after transfer exhibited

a decay of the optical power after a few hundred of μs and a significantly reduced peak intensity for the LEDs transferred on tape when compared to LEDs on h-BN/sapphire and transferred on silicon. This indicates that thermal effects occur during the first microseconds of operation. This is clearly due to a lack of thermal dissipation induced by the host substrate since the decay is faster for LEDs transferred on aluminum tape than for LEDs before transfer and for LEDs transferred to silicon for which no decay is observed. The decay observed for the LEDs before transfer is a bit surprising because one can expect a large thermal dissipation of the sapphire substrate. The thermal dissipation efficiency in that case is likely degraded by the presence of the thin AlGaN buffer and h-BN layers which could introduce large thermal resistance at their interfaces.

The results obtained in this study show that the SAVWE of III-N device coupled with the h-BN based mechanical lift-off and transfer on a host substrate lead to an overall improvement of the crystalline quality of the active layers by a reduction of the threading dislocation density and thus an enhancement of the electrical and optical device performance. Moreover, the yield of the transfer of large-size crack-free devices on host substrates is higher when using SAVWE. The technique developed in the frame of this study is also very useful for the efficient heterogeneous integration of III-N devices on CMOS compatible substrates. It can be easily extended to the transfer of other devices especially electronic devices and solar cells where the dimension of the devices could be quite large. Another application of such a process is the realization of waveguiding in III-N films which requires cladding layers of lower refractive index to confine light to the III-N layer. This could be achieved, much more easily than, for instance, the technique developed by C. Xiong et al.[64], by transferring III-N layers to a SOI substrate where the

silicon dioxide on top of the silicon wafer serves as one of this cladding layer. As a of concept and as shown in Figure 27, we successfully transferred a crack-free patterned LED on a thick glass plate. One can notice that the back-side light-emission is guided in the glass plate owing to the perfect transparency of silica glass at the considered wavelength. Last, SAVWE could be very useful for the fabrication of devices with engineered shape such as triangle LEDs that allows for a better light-extraction, this without any complicated dicing process.

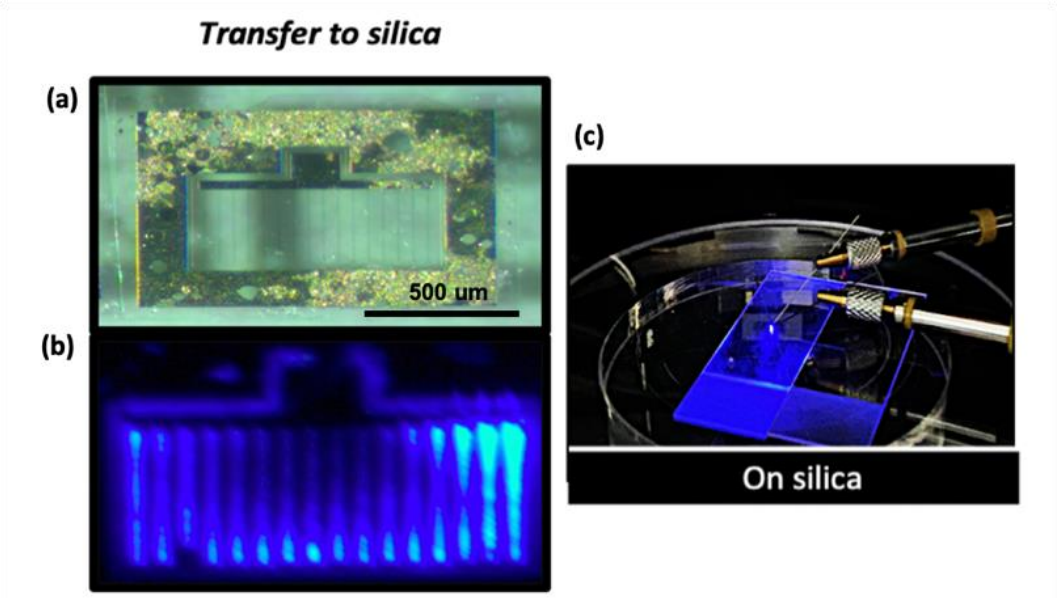

Figure 27 - (a) Optical microscope image of a patterned LED transferred on a silica plate. (b) Corresponding electro-luminescence when a pulsed current is applied to the device. (c) Photograph showing the backside emission, guiding and decoupling of the light in the rough surface region of the plate [63].

4.3 Self-Lift-Off and Transfer (SLOT) Process for Vertical Thin-Film LEDs

Besides the SAVWE process we developed for the fabrication of crack-free lateral LEDs, we also achieved monolithic free-standing large-area vertical thin-film (VTF) III-N LED arrays fabricated through a novel h-BN-based thermo-mechanical self-lift-off and transfer (SLOT). In this sub-section, we present results of the fabrication of vertical InGaN LEDs on large-area free-standing membranes, using the thermo-mechanical lift-off technique newly enabled by 2D layered h-BN. The fabricated vertical LEDs are electro-optically characterized and compared to lateral LEDs.

4.3.1 Motivations of Vertical Thin -Film LEDs

In the recent years, innovation in high-brightness GaN-based light-emitting diodes (LEDs) has enabled the next-generation solid-state lighting, displays and visible light communication systems[65]. However, conventional laterally contacted LEDs grown on insulating sapphire substrates suffer from (i) high series resistance caused by lateral current path and by current crowding near the edge of the contact[66], [67], (ii) poor heat dissipation when operated at high current density due to the low thermal conductivity of the substrate[68], and (iii) limited top surface emission owing to the extensive coupling of light in the thick transparent sapphire substrate[69], [70]. To overcome these issues, vertical thin-film LEDs (VTF-LEDs), where the sapphire substrate is removed and the LED structure is transferred to an electrically conductive host substrate, have been widely investigated. In this configuration, electrical contacts are deposited on both sides of the functional epilayers. VTF-LEDs where shown to exhibit lower series resistance and operation voltage due to the vertical current injection[71], [72]. Moreover, transfer to

metallic substrates allows for efficient heat extraction when LEDs are driven at high current density as well as for enhanced light extraction efficiency due to their high optical reflectivity[73]. Furthermore, after removing the native substrate, the luminescence efficiency of these vertical-cavity LEDs can be improved by thinning the optical cavity length through a backside etching process[74].

Separating the epilayers from the native substrate is a key step in the fabrication process of VTF-LEDs. As discussed in Chapter 2, this can be achieved through different methods such as laser lift-off and chemical etching of a sacrificial layer or 2D h-BN-based mechanical lift-off. In this context, we developed a new h-BN enabled approach which allows for the monolithic fabrication of crack-free vertical LED arrays on large-area free-standing membranes. This process is enabled by the use of a thick layer of electroplated copper deposited on top of the LED structure which (i) adds rigidity to the structure to prevent crack generation, (ii) acts as back mirror and heat sink, and (iii) enables, when combined with moderate thermal treatment, the self-lift-off and transfer (SLOT) of LED structures from sapphire.

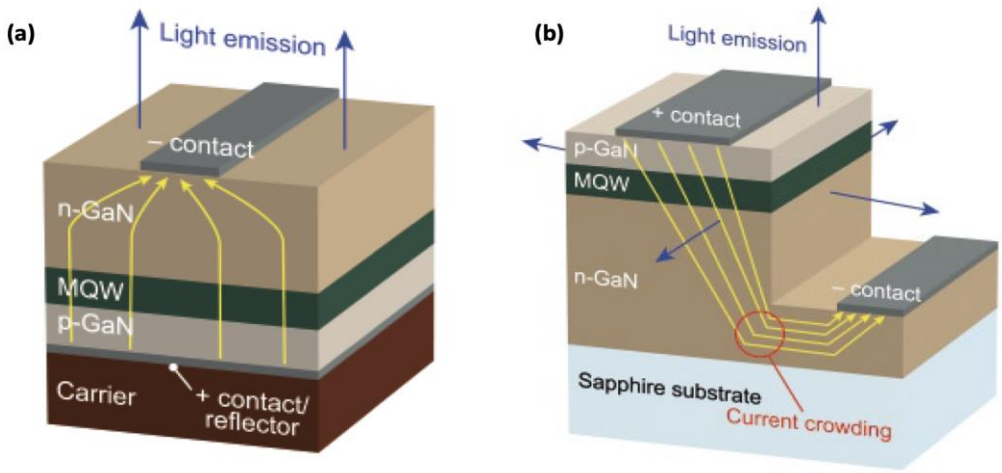

Figure 28 - (a) Schematic of a VTF LED (b) Schematic of a lateral LED showing the current crowding issue [69].

4.3.2 Materials and Methods for the SLOT Process

After the growth of a 3-nm-thick h-BN layer on 2-inch sapphire substrate, an intermediate layer of n-AlGaN (0.3 μm) with an Al mole fraction of 14% was grown to act as a nucleation layer, followed by a GaN-based LED heterostructure consisting of a silicon-doped n-GaN (0.3 μm), 5 InGaN/GaN MQWs and a magnesium doped p-GaN region (0.2 μm). The 5 MQWs structure consists of 12-nm-thick GaN barrier layers and 2.5-nm-thick InGaN QW layers with an In mole fraction of 15% to get light emission in the blue (targeted wavelength is around 460 nm and has been confirmed with cathodoluminescence).

The electron and hole carrier concentrations in the Si- and Mg-doped GaN layers are 5 x 10^{18} and 1 x 10^{17} cm^{-3}, respectively. The LED structures before and after the SLOT fabrication process are given in Figure 29a and 29b [75], respectively, and the SLOT fabrication process of VTF-LEDs is schematically summarized in Figure 29c. First, a Ni (20 nm)/Au (20 nm) bilayer is deposited on top of the LED epilayer to act as a p-type electrical contact. This contact is then annealed at 600°C under O_2 atmosphere for 60 s and an additional Ti (5 nm)/Au (20 nm) bilayer is deposited. The Ti layer helps to improve the adhesion of the subsequent metal layers while the Au layer acts as a seed for subsequent copper deposition as well as back mirror to enhance the reflection of the light emitted by the quantum wells. These metal layers are deposited by e-beam evaporation. Then, a few cm2 area is patterned by a photoresist (SPR 220-3) via a standard photolithography-based

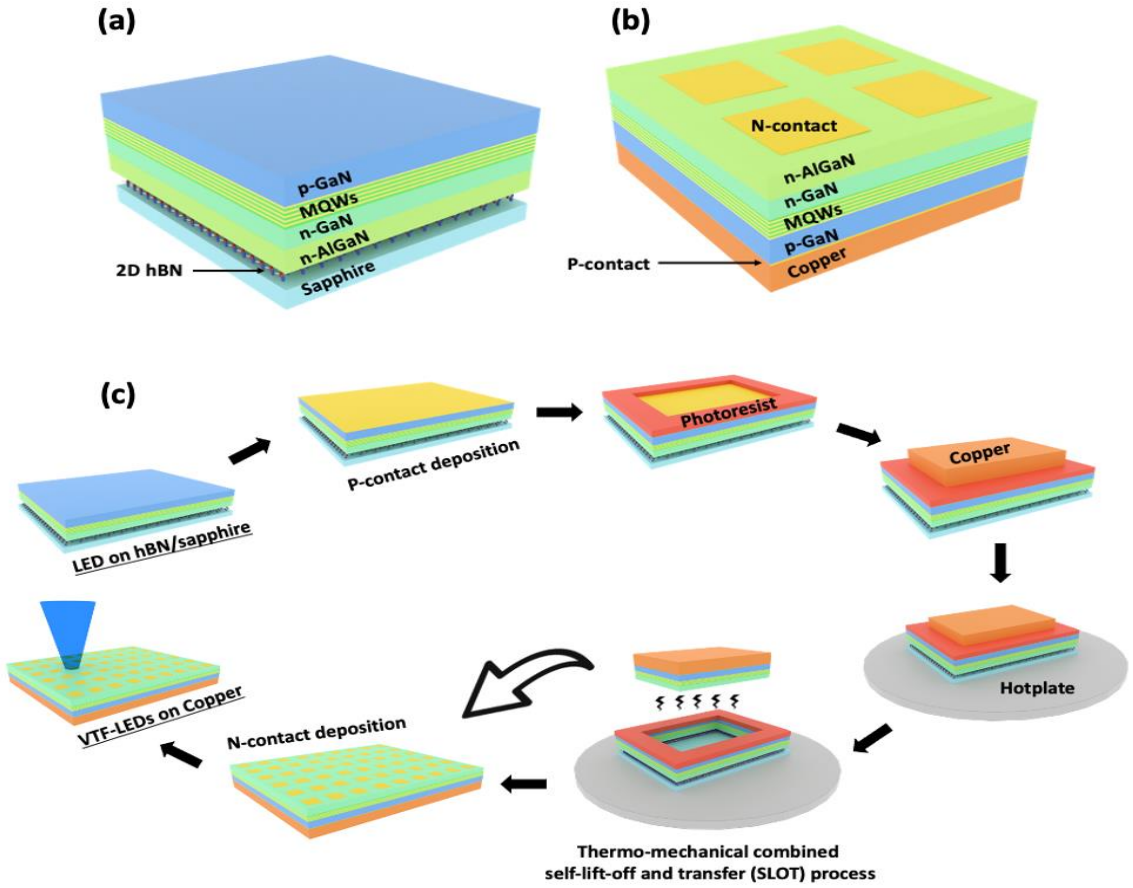

Figure 29 - Schematics of (a) LEDs structure grown on h-BN/sapphire, (b) VTF-LEDs on copper fabricated by SLOT process and (c) different steps of the SLOT process for fabrication of VTF-LEDs [75].

process, followed by an O_2 plasma cleaning to remove any remaining traces of photoresist from the developed area. Then, a 30-µm-thick layer of copper is electroplated using an acid-free solution containing dilute $CuSO_4$ to avoid delamination of the epilayers grown on h-BN.

Thinner layers of Cu resulted in the free-membrane wrapping around itself generating cracks and making it hard to manipulate for further process steps. 30-µm-thick Cu layer was shown to be thick enough to rigidify the structure while maintaining it flexible and result in reproducible flat and crack-free flexible membranes. The sheet resistance of the 30-µm-thick electroplated copper was found equal to 3 mΩ per square. This value is one

order of magnitude larger than values reported in the literature[76]. This could be explained by the fact that we used a sulfuric acid-free solution for the electroplating which generally lead to higher resistivity of the copper layer due to the formation of CuOH complexes.

The release of the LED structure from the sapphire native substrate is achieved with a thermal treatment at 100°C for 1 hour. During this step, the whole few cm^2 targeted area of the functional layers is spontaneously released from the sapphire substrate owing to shear stress at the interface between the copper layer and the III-N epilayers due to the difference of thermal expansion coefficients. This shear stress is large enough to break the vdWs bonding of h-BN to sapphire. Extended analysis of thermal stresses generated in the layers and experimental details are given in the next "*Mechanical Analysis of the SLOT Process*" sub-section.

From the atomic force microscope (AFM) image of the membrane after SLOT process (Figure 30), the resulting n-AlGaN surface is atomically flat with an r.m.s roughness of 0.65 nm obtained over a 10 x 10 μm area.

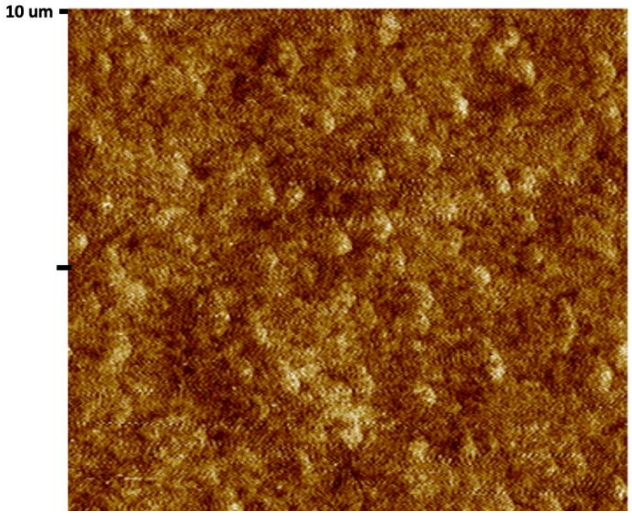

Figure 30 - AFM image of the separated surface of the LED structure after the SLOT process. The corresponding r.m.s. roughness is 0.65 nm [75].

High-angle annular dark field scanning transmission electron microscope (HAADF-STEM) images and elemental map, as deduced from energy dispersive X-ray analysis (EDX), of a VTF-LED are shown in Figures 31a and 31b, respectively. HAADF-STEM images of the LED structure before and after lift-off (Figure 31a), shows that the SLOT process does not introduce any degradation of the crystalline quality of the epilayers. These images were taken on tens of different regions and show homogeneous material quality over the 2-inch wafer. The threading dislocation density is estimated to 3 x 10^9 cm^{-2} for epilayers on hBN/sapphire native substrate and copper. These dislocations originate from the AlGaN layer and can be explained by the growth-mechanism of 3D layers on 2D crystals. Indeed, since the LED structure is grown on hBN surface having no dangling bonds, the threading dislocations are mostly originating from the grain boundaries formation during the AlGaN nucleation layer on h-BN[63]. EDX elemental map shows clearly the different epilayers as well as the deposited metal contacts. As reported by several authors[77], [78], the Ni/Au p-type ohmic contact annealed under O_2 led to diffusion of Ni atoms in the Au layer and the formation of a rough and continuous NiO layer at the top surface and a non-continuous Au layer underneath. The high roughness of the successive metal layer interfaces (Ti/Au/Cu) between metal layers is mainly attributed to the roughness of the formed NiO layer.

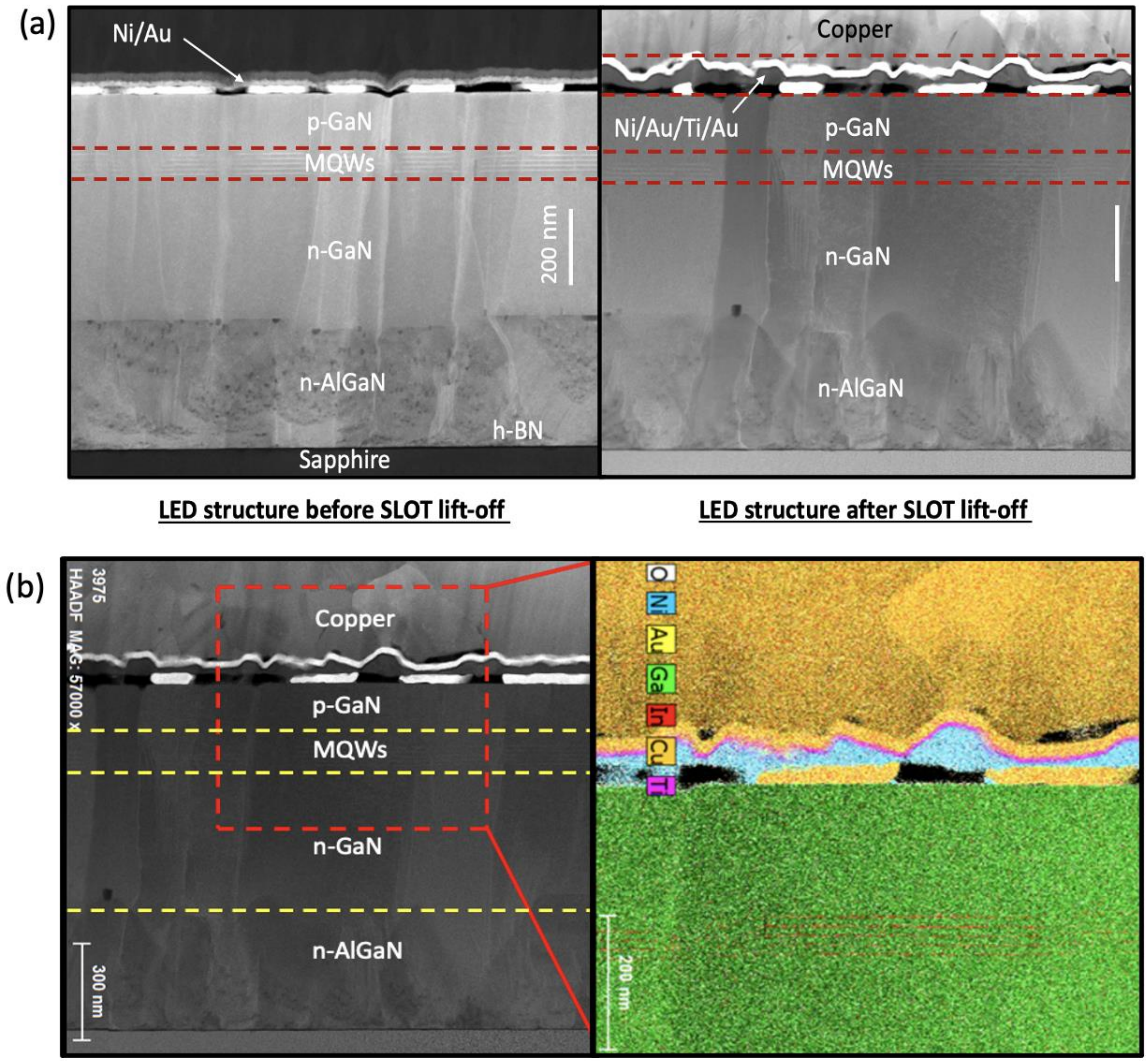

Figure 31 - (a) High-angle annular dark field scanning transmission electron microscope (HAADF-STEM) images of the LED structure before and after SLOT process showing no degradation of the epilayers after lift-off. (b) TEM image and corresponding energy dispersive X-ray spectroscopy (EDX) elemental mappings of an LED free-membrane on copper [75].

After a 10 min HCl treatment to remove native oxides from the exposed n-AlGaN layer, a 30-nm-thick Au layer is deposited by e-beam evaporation using a stainless-steel shadow mask with squares of various size (0.25 mm^2 to 4 mm^2) on the n-AlGaN layer to form the n-contact. This contact is not annealed to avoid inducing cracks in the free-standing LED

membrane due to the high thermal expansion of the copper layer. The VTF-LED membranes obtained are then bonded to a thick aluminum holder using silver paste for further electro-optical characterizations. Electrical and electro-optical characterization was conducted on the fabricated VTF-LEDs through pulsed (1 ms duration, duty cycle of 1%) current-voltage measurements. Optical power was measured by a Si photodiode placed, due to the electric probes size, 2 cm above the device under test, and thus capturing a small amount of the light emitted from the LED under test. Figure 32a shows photographs of a 4 x 3 cm^2 released LED membrane and the corresponding sapphire substrate after the membrane release using the SLOT process. Photographs of a 1-cm^2 membrane, highlighting its flexibility as well as a membrane on which an array of 24, 0.5 x 0.5 mm^2 in size, VTF-LEDs are fabricated are shown in Figure 32b and 32c, respectively.

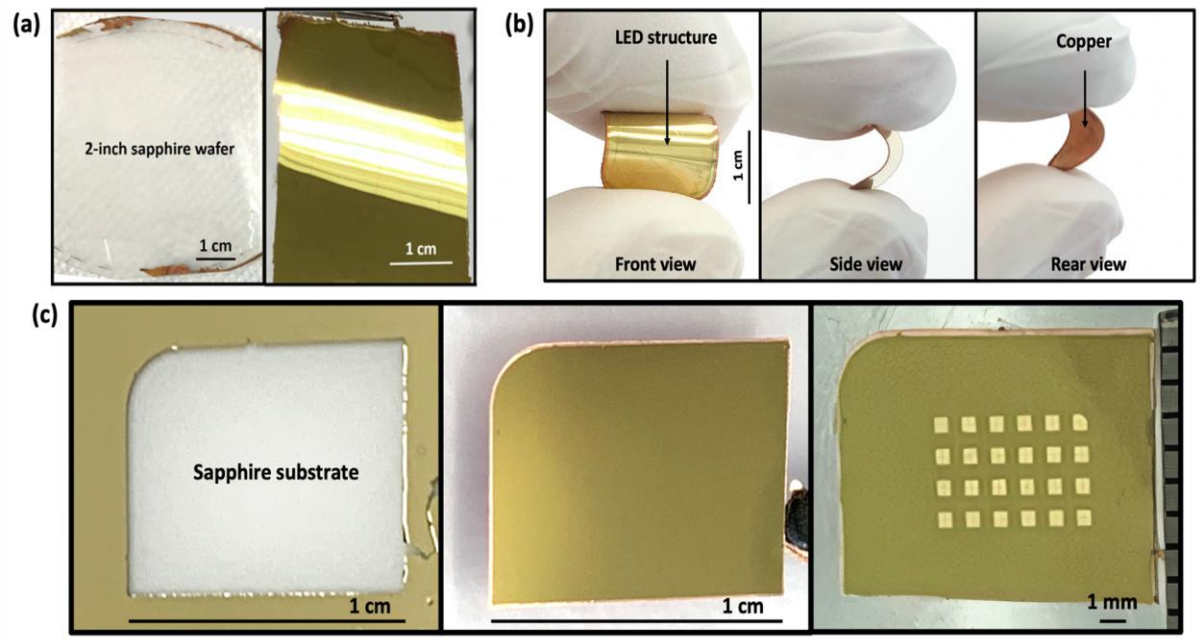

Figure 32 - (a) Photographs of 4 x 3 cm^2 LED membrane and the corresponding sapphire substrate after the membrane release using the SLOT process (the bright stripe on the membrane corresponds to the reflection of the ceiling neon lamp in the cleanroom). (b) Photographs of a 1-cm2 membrane, highlighting its bending possibility. (c) Photographs of a 1-cm^2 released membrane on which an array of 0.5 x 0.5 mm^2 VTF-LEDs is fabricated [75].

4.3.3 Electro-Optical Characterization Results

Electrical and electro-optical characterizations were carried out on more than 50 LEDs of size 500 x 500 μm^2, fabricated on different membranes. All the devices exhibited a diode-like I-V curve, with threshold voltage ranging from 5V to 10V and series resistance ranging from 5Ω to 15Ω, and light emission. We note some variation in the efficiency and homogeneity of the emission from one LED to another. As an example, Figure 33a shows a photograph image of an array of 4 VTF-LEDs connected in parallel and operated at 8V. As shown in Figure 33b, for 15 of the set of 50 VTF-LEDs, homogeneous and bright electro-luminescence was obtained, although the applied current and voltage were different for each of them. Figure 33c shows both typical current-voltage (I-V) and optical power versus current (L-I) characteristics VTF-LED, recorded in this set of 15 devices. When compared to a lateral LED fabricated on a same LED structure (Figure 34), the VTF-LED exhibits a higher threshold voltage (around 9V, against 2.5V for the lateral LED), lower series resistance (5Ω, against 12Ω for the lateral LED) and higher leakage current (1.7 mA at -3V, against 0.4 mA for the lateral LED). We also remark that the VTF-LED exhibits a linear increase of the optical power with the current injection increase up to 500 mA (limit of our equipment), without any saturation as in the case of the lateral LED for injected current larger than 200 mA for which current crowding and associated heating effect begin to degrade the LED efficiency. This heating effect is greatly reduced thanks to better current injection in the vertical structure and to the copper substrate which acts as a heat sink permitting good thermal dissipation in the case of the VTF-LED, as it has been reported by Horng et al[68].

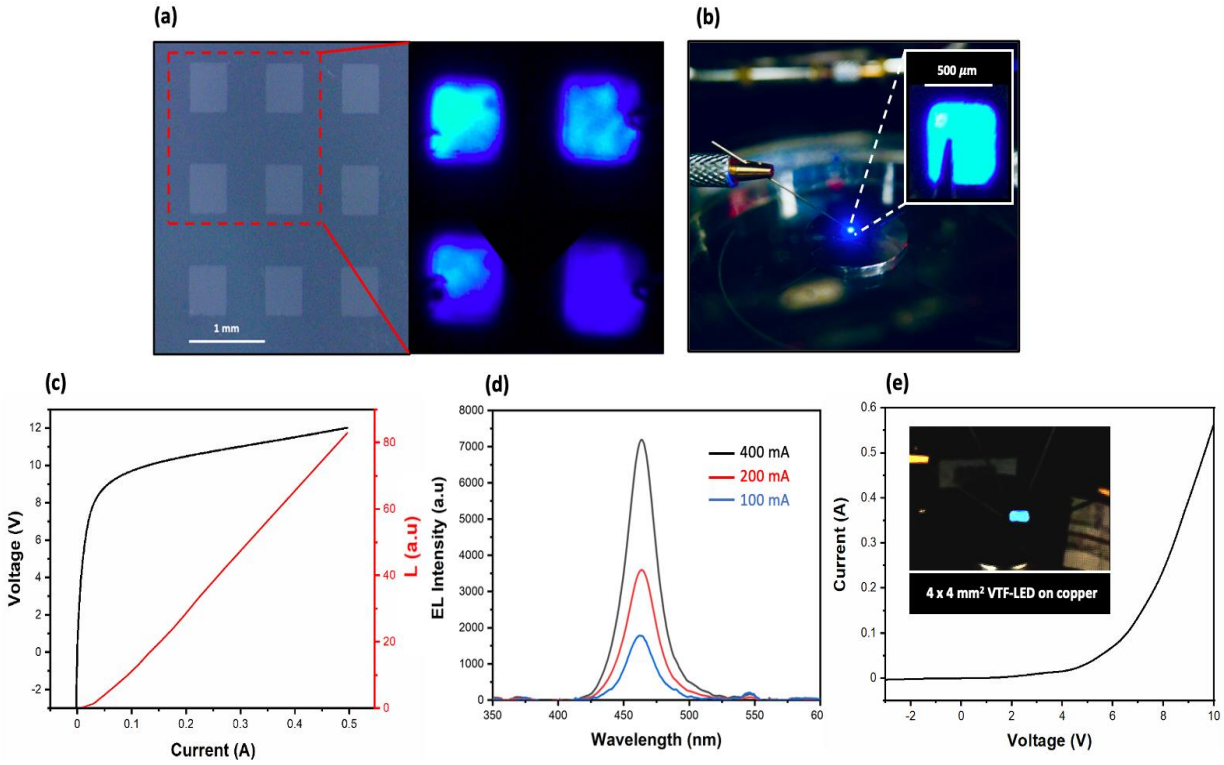

Figure 34 - (a) Electroluminescence image of 4 VTF-LEDs connected in parallel and operated at 8V. (b) Photographs of a homogeneous VTF-LED operated at 300 mA. (c) Current-voltage and optical power versus current characteristics of the VTF-LED in (b). (d) Electro-luminescence spectra of the VTF-LED for different levels of injected current. (e) Current-voltage of a large size (4 mm x 4 mm) VTF-LED. Inset is a photograph of this LED operated at 500 mA [75].

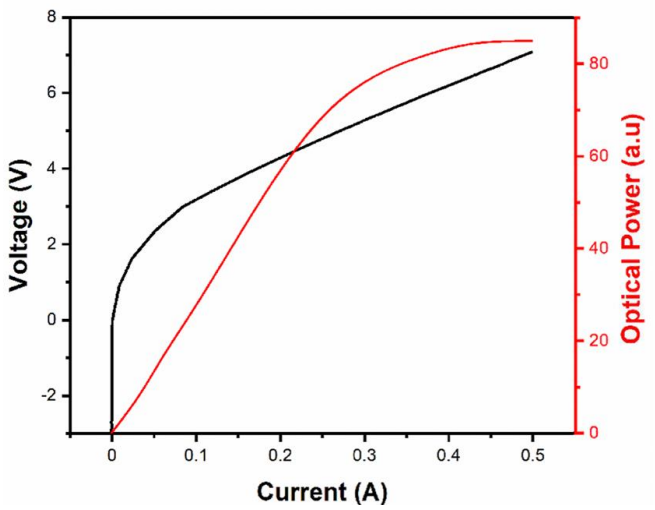

Figure 33 - Current-voltage and optical power versus current characteristics of a typical lateral LED processed on a same LED structure as VTF-LEDs [75].

Figure 33d shows the electro-luminescence spectra of the VTF-LEDs for different levels of injected current. The light-emission peaks are at a wavelength of 462 nm and are independent of the value of the injected current. As reported by Trindade et al.[79], the temperature increase due to the increase of current injection should lead to a red shift whereas the reduced quantum confined stark effect (QCSE) while increasing the current injection should lead to a blue shift. In the case of these VTF-LEDs on copper, the absence of a red shift could be attributed to the high thermal dissipation capability of the copper substrate, whereas the absence of a blue shift could be attributed to the relaxation of residual compressive strain in the GaN-based films grown on h-BN, that diminishes the QCSE in the quantum wells as reported by Liu, F et al. [80].

Concerning the wavelength shift before and after SLOT process, it is difficult to assess because the fabrication of the vertical LED is complete only at the end of the SLOT process. Thus, it is not possible to measure the electro-luminescence emission wavelength before the release of the vertical LEDs. However, by considering lateral LEDs grown on h-BN/Al2O3 template, the electro-luminescence of the quantum wells at 100mA peaked at (464 ± 1) nm before lift-off. These devices are released by water-soluble tape and transferred to an aluminum tape containing a 5-μm-thick acrylic adhesive layer as described in previous sections of this chapter.

After the transfer of the same lateral LEDs, the electro-luminescence of the quantum wells at 100mA peaked at (466 ± 1) nm. After the SLOT process done on an LED structure grown on h-BN/Al2O3 template using the same growth parameters, the electro-luminescence of the quantum wells peaked at (462 ± 1) nm. The slight red shift of around 2 nm observed in lateral LEDs before and after transfer to the acrylic-based tape could be

attributed to a temperature increase, because of the weak thermal dissipation of the tape. For vertical LEDs, it is not possible to conclude if there is a shift because we cannot have a reference vertical device before lift-off. The wavelengths obtained on each configuration are summarized in the following table.

Table 4 - The electro-luminescence wavelength (nm) of lateral and vertical LEDs at 100 mA, before and after lift-off.

	Lateral LED before transfer	**Lateral LED after transfer to tape**	**Vertical LED before transfer**	**Vertical LED**
Wavelength (nm)	464 ± 1 nm	466 ± 1 nm	Not possible	462 ± 1 nm

For the electro-luminescence spectra of the lateral LEDs for different levels of injected current, Figure 35a and 35b shows a considerable red shift of 7 nm for LEDs before lift-off and 29 nm after lift-off and transfer on flexible tape. The important 29 nm red shift in the case of lateral LEDs on tape can be seen by eyes as shown in Figure 35c, where the light is changing from blue to turquoise-green while light intensity is decreasing.

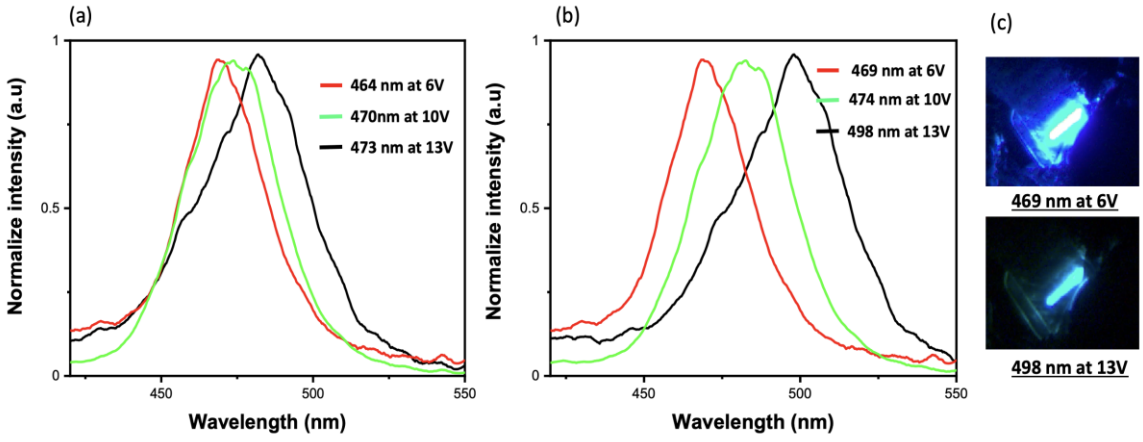

Figure 35 - Normalized electro-luminescence spectra of the lateral LEDs for different levels of operating voltage (a) before lift-off and (b) after lift-off. (c) Photographs of an LED on tape showing the observed red shift of 29 nm.

These results combined with the constant spectrum versus current of the vertical LEDs confirms the heat dissipation capability of the copper substrate and demonstrate the proof of concept of an h-BN enabled SLOT process for the fabrication of VTF-LEDs. These results show that the thermo-mechanical SLOT process allows for large-area and crack-free release of III-Nitride epilayers and fabrication of VTF-LEDs arrays. This approach based on self-detachment of the epilayer from the substrate without any external force applied by a stamp/tape simplifies a critical step of the process fabrication and hence minimize the risk of cracks generation for large surface devices leading to a highly reproducible and controllable process. Also, since the membrane is only 30-μm thick, the fabricated VTF-LEDs could be folded, cut and stuck to different surfaces.

Nevertheless, the n-contact of these structures is realized on the n-AlGaN layer on h-BN which, as shown in our previous work[63], has lower crystalline quality than the n-GaN buffer near the MQWs. Thus, strong carrier recombination process can occur at the grain boundaries of the AlGaN layer. This could explain the observed high series resistance (expected values for this kind of devices are around 1 Ω[17]) as well as the inhomogeneous light-emission from one LED to the other and within a single LED.

The rather high leakage current observed in the fabricated VTF-LEDs is likely related to the absence of mesa isolation of single vertical devices whereas their large threshold voltage are probably due to the non-ohmic n-contact which was not annealed to avoid inducing cracks in the free-standing LED membrane. The absence of mesa isolation could also lead to some current spreading in the MQWs region resulting in lower current density and thus, reduced light-emission efficiency. These points are confirmed by electrical simulations of the VTF-LEDs, carried out using SILVACO-Atlas software to study the

effect of (i) the n-AlGaN layer (considered without any defect), (ii) ohmicity of the n-contact and (iii) absence of mesa isolation. As shown in Figure 36a, the n-AlGaN layer introduces increased resistance in the structure leading to an increased series resistance of the LED, whereas, as shown in Figure 36b, the largest impact on the I-V curve comes from the non-ohmic contact which results in large increase of the threshold voltage and decrease of the current. The current spreading at the level of the quantum wells is clearly shown in Figure 36c. Thus, the AlGaN resistivity (which is probably under-estimated in the simulations which do not include the effect of low structural quality of the AlGaN layer), and the non-ohmic n-contact are the main cause of the observed high series resistance and voltage threshold whereas the current spreading due to non-symmetric contacts causes reduction of electro-luminescence. To remove electrical issues related to the AlGaN layer, a solution could lie in the etching of this layer. Either dry or wet AlGaN etch must be conducted on the free-standing membrane, which is challenging and requires further adaptation. Improvement in efficiency have been previously demonstrated on VTF-LEDs

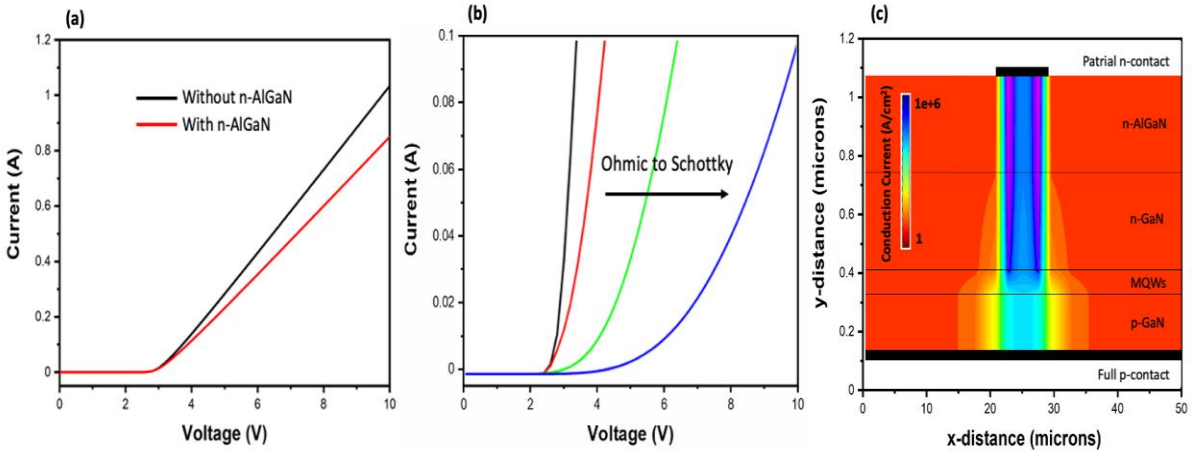

Figure 36 - (a) Simulated current-voltage characteristics of VTF-LEDs with and without the n-AlGaN layer. (b) Simulated effect of the Schottky n-contact on the current-voltage characteristic of VTF-LEDs. (c) Current distribution in a VTF-LED without mesa isolation [75].

released through laser lift-off, where the defective undoped GaN buffer layer is removed through a backside etching process[14], [74]. Work is in progress to optimize this step for the SLOT process.

Optical simulation was also conducted to investigate the effect of the n-AlGaN layer on the light extraction efficiency (LEE) and far field angular emission pattern (FFP) of the VTF-LEDs. FDTD Lumerical software was used to model the structure where a dipole source is positioned at the MQW active region. The LEE and FFP were obtained by averaging results over the source position and polarization direction of the dipole to consider the incoherent, unpolarized and isotropic emission of the QWs. Figure 37a shows the LEE as a function of the optical cavity length. The n-AlGaN layer thickness is swept from 0 to 500 nm. We can see a periodic variation of the extraction efficiency with a period of around 100 nm, originating from interference effects altering the top surface reflection according to the AlGaN layer thickness. The LEE is shown to vary between 3.3% and 6.5%. The n-AlGaN thickness of our fabricated VTF-LEDs being around 300 nm is thus not optimum since the corresponding LEE is around 4.2%. As it can be seen in Figure 37b showing the effect of the n-AlGaN layer thickness on the FFP, the quasi-flat pattern corresponding to the actual VTF-LED (300 nm thick AlGaN) is in a good agreement with the poorly defined light emission at the edges, seen in the inset of Figure 33b and could explain also the lower measured optical emission. Slightly modifying the thickness of the n-AlGaN layer (to 340 nm for instance) would increase the LEE to more than 6% and result in highly directional emission of light.

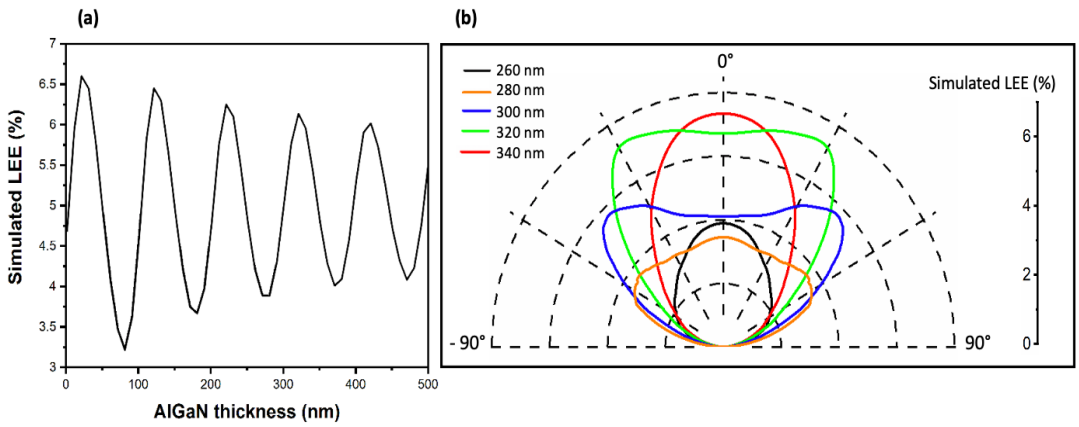

Figure 37 - Simulation of the effect of n-AlGaN thickness on (a) the LEE of the VTF-LEDs and (b) on their far-field angular pattern for an AlGaN thickness range from 260 to 340 nm [75].

The results obtained in this study show that the thermo-mechanical SLOT process allows for large-area and crack-free release of III-Nitride epilayers and fabrication of VTF-LEDs arrays based on h-BN grown in the same MOCVD growth run as the epilayers. Because the process doesn't require any external force with tape/stamps to separate the epilayers from the substrate, this approach can take its place as additional 2D material building block enabling mechanical liftoff and transfer of epilayers.

A set of ten LED membranes containing a total of 400 LEDs has been fabricated using the SLOT process and 50 LEDs have been deeply characterized in the frame of this work. Crack-free membranes on which we were able to get light emission from all of the LEDs but with dispersion in their performance have been obtained, leading to a 100 % crack-free transfer yield for the 400 tested LEDs. In addition, the SLOT process at the wafer scale is possible leading to the lift-off and transfer of the LED epilayers from a full 2-inch wafer.

Because the membrane is only 30-µm thick, the fabricated VTF-LEDs can be folded, cut and transferred onto different surfaces. Moreover, an efficient etch of the n-AlGaN buffer layer on the free-standing membranes could enhance performances of this VTF-LEDs by decreasing the electrical series resistance as well as enhancing the LEE by modifying the optical cavity length. This work also opens new ways for the fabrication of thin-film flip-chip (TFFC) LEDs where both contacts are placed on the backside of the LED (Figure 38). Such a configuration[14], [81] allows for higher light-extraction (no metal is deposited on the emitting side and there is no requirement of wire-bonding to access the n-contact). TFFC-LEDs can be achieved through the SLOT process, by introducing additional process steps while the LED structure in still on the h-BN/sapphire native substrate. Besides the expected increase of the LEE, this architecture will also allow to deposit the n-contact on the good quality n-GaN buffer instead of the low-quality n-AlGaN seed layer (as for VTF-LEDs) and thus, enhance the charge carrier transport. Moreover, since for the TFFC configuration the deposition of n-contact is done while the LED structure is still on h-BN/sapphire native substrate, this contact can be annealed, which will decrease the threshold voltage and series resistance as compared to the VTF-LEDs.

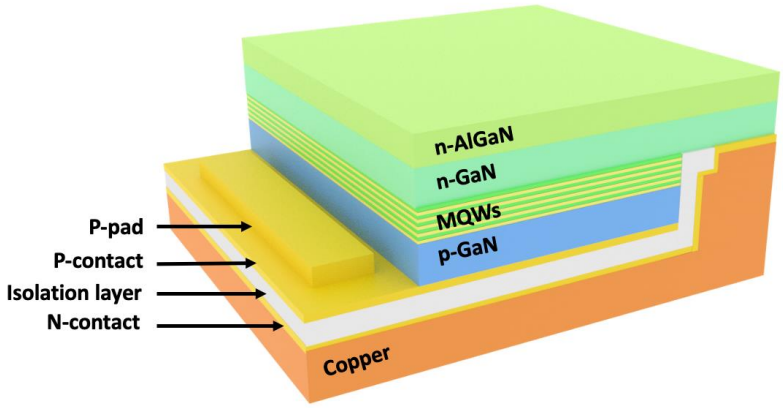

Figure 38 - Schematic of TFFC LEDs that could be realized through the SLOT process.

4.3.4 Mechanical Analysis of the SLOT Process

In the past, extensive analysis of thermal stresses generated in bilayer[82] and multilayer[83] has been performed. The increasing complexity in obtaining closed form solutions for interface stresses in bilayer requires the first order approximations and computational calculations[83]. To get more insight on what happen during the thermal lift-off process we adopted a simpler approach. The LED membrane attached to the sapphire substrate has been simplified and modeled as a copper/sapphire bilayers and a mechanical model of bending of a bilayers strip upon heating was used[82]. The LED epilayer structure was neglected in the model as the thickness of copper (30 μm) is 30 times larger than those of the LED epilayers, so major strain and stiffness condition during thermal expansion was assumed to be imposed by copper. Upon heating the bilayers, both copper and sapphire layers expand. Copper layer, owing to higher thermal coefficient of expansion than sapphire (see Table 2), expands more but is constrained by the sapphire layer. This difference in the thermal expansion coefficients causes thus compressive force in copper (F_1) and tensile force in sapphire F_2. To fulfill the equilibrium condition, these forces must be equal and opposite in direction leading to the creation of moments (M_1 and M_2) and then to a bending of the bilayers as shown in Figure 39.

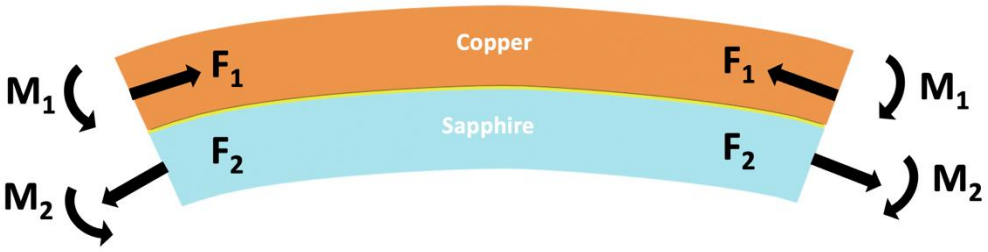

Figure 39 - Schematic showing the forces and moments on an infinitesimal element inside the bulk of the sample.

Table 5 - Values of the different parameters used in the calculation.

Property	**Copper (Cu)**	**Sapphire (Al_2O_3)**
Length x Width	1 cm x 1 cm	1 cm x 1 cm
Thickness	30 μm	350 μm
Young's Modulus (GPa)	110[83]	345[85]
Thermal Expansion Coefficient (x 10^{-6}/K)	17[84]	8.0[86]

Taking the values of the different parameters as shown in Table 2, a compressive stress of 66 MPa in the copper layer and tensile stress of 5.6 MPa in the sapphire layer, and a flexure stress (due to the moments) of 0.5 MPa in the copper layer and 18.4 MPa in the sapphire layer have been calculated. In addition, since the edges of the bilayers are free surfaces, to balance the internal stress and moment, shear and normal stresses along and perpendicular to the copper/sapphire interface, respectively, appear at the interface. This is shown schematically in Figure 40.

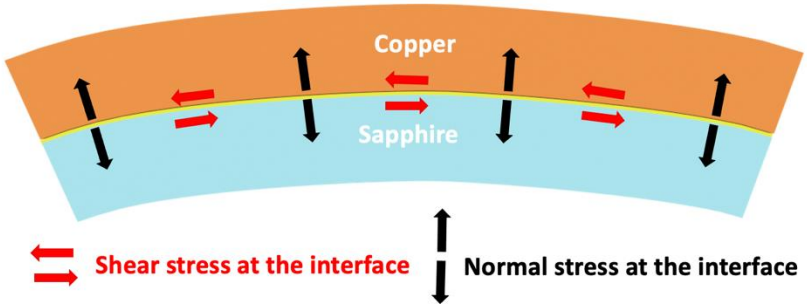

Figure 40 - Schematic showing the shear and normal stresses at the edge of the sample [75].

The magnitude of these interface shear and normal stresses is maximal at the edges of the sample and decreases down to the center of the bilayers. The dependence of the interface shear and normal stresses magnitude at the edge of the bilayers as well as the curvature

radius and maximum deflection are plotted as function of the temperature in Figure 41a and 41b, respectively.

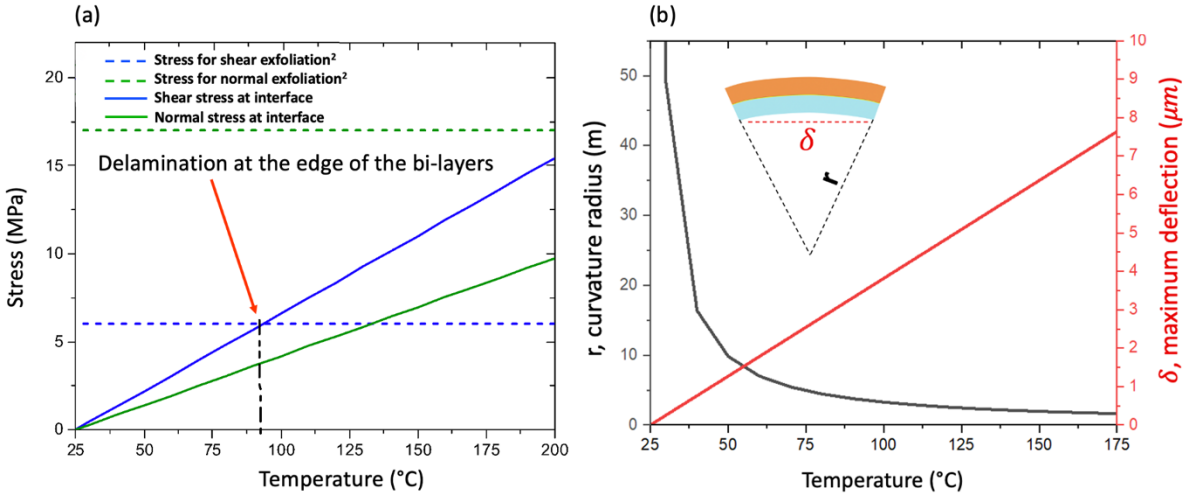

Figure 41 - (a) Variation of shear and normal stresses with temperature. The doted lines show exfoliation shear and normal stresses of h-BN2. (b) Variation of curvature radius and maximum deflection of the bilayers versus temperature [75].

As expected, both bilayers edge interface stresses increase with temperature increase. Since the adhesion between the two layers is governed by the van der Waals bonds of the BN interlayer in our case, once the interface stress becomes larger than the force required to break these bonds delamination may occur. The horizontal dotted lines in Figure 41a corresponds to the shear and normal stresses required for exfoliation of a hBN layer as measured by Rokni et al.[87]. It is clear that once the temperature reaches a value of 89°C the interface shear stress becomes larger than the force required for the exfoliation of a hBN layer leading to delamination at the edges of the bi-layers which then propagates toward the center of the bi-layer since the interface shear stress at the new edges (after partial release) is still enough to sustain the delamination process. This continuous propagation of the stress lead to the complete lift-off.

For thermal lift-off experiment, the structures were put on a hotplate set at three different temperatures: 50°C, 100°C and 200°C for an hour. At 50°C, no delamination was observed. At 100°C (same order of what we get from calculation), edge delamination started after a few minutes and the lift-off was completed after 60 min and without cracks in the epilayers. At 200°C, the complete lift-off happened faster (after 15 min), but a large number of cracks were introduced in the structure. The faster delamination could be explained by the fact that at this temperature the bending is larger inducing interface stress above the threshold on a larger length. At this temperature, the bending is probably beyond to what can be sustained by the epilayers and cracks are induced.

Figure 42 shows an example of LED membranes after a SLOT process of 100°C without cracks (left) and 200°C (right) with cracks.

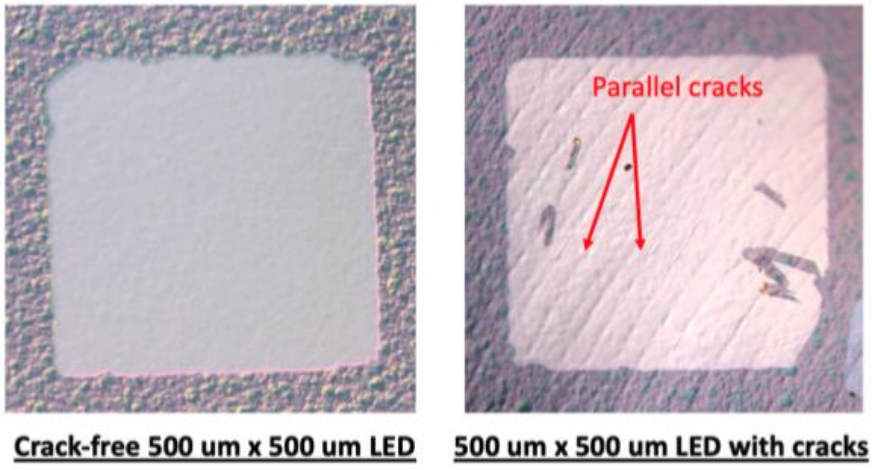

Figure 42 - LED membranes after a SLOT process of 100°C without cracks (left) and 200°C (right) with cracks.

CHAPTER 5. TOWARDS FLEXIBLE NANOPYRAMID-BASED INGAN SOLAR CELLS

5.1 Introduction

During the last century, industrialization and the growth of population leaded to a global growth of economic activities and thus, unrestricted energy consumption in a world which has limited resources. Currently, we approach the limits to growth imposed by the depletion of non-renewable resources. Moreover, the combustion of fossil fuels - such as oil, coal and gas - produce the greenhouse gases such as carbon dioxide that are mainly responsible for the global warming and climate change. Combustion of fossil fuel dominates power generation by 38 % of total world electricity supply in 2019 [88].

This constant growth in energy demand associated with global warming challenges are very motivating factors for the development of the most efficient photovoltaic (PV) cells and innovative materials and processes to replace conventional fossil fuels in the future. After decades of research and development promoted by government subsidies, the cost-per-watt of PV panel dropped form around $100 in 1975 to $3 today [88].

Silicon (Si) solar cells dominate the PV market by 92 % due to its abundance and low manufacturing costs. However, about 50 % of the cost of Si cells is related to the Si substrate [89]. Another alternative to thick Si cells is thin-film (few tens of microns) solar cells that are lightweight and low-cost. In addition, thin-film cells can be fabricated or integrated on various flexible substrates [88] with different shapes and sizes depending on specific applications such as future mobile and wearable devices, electric cars and bicycles, building integrated photovoltaics (BIPV) on curved rooftops and space engines [90].

Figure 43 - Photographs of various applications of flexible thin-film solar cells. Adapted from [89][90].

In spite of these benefits, the fabrication of thin-film solar cells on flexible substrates remains challenging since the mechanical, thermal and chemical properties of these substrates are not compatible with the processes used to fabricate the active device. For instance, polyethylene terephthalate (PET) is widely used as flexible substrate but has a melting temperature (around 250°C) below the one needed to deposit the absorber layers (300°C for amorphous Si and above 600°C for polycrystalline Si) [91]. Alternatively, the deposition temperature of amorphous Si is lowered to accommodate the substrate, leading to a lower efficiency whereas polycrystalline Si can be only deposited on substrates with higher tolerance such as glass and metals. Another solution relies on depositing the active layers and fabricating the photovoltaic cells on a compatible substrate followed by a lift-

off and transfer process for the heterogeneous integration of these devices on a substrate of interest. These method has been also successfully demonstrated on several III-V solar cell structures. For example, GaAs using the chemical etching of an AlGaAs sacrificial layer and transfer to PET substrate showed an efficiency around 20 % [92].

In this chapter, we propose to use the 2D-h-BN assisted mechanical lift-off and transfer for the heterogeneous integration of solar cells to rigid and flexible substrates. We especially focus on InGaN-based solar cells since InGaN is a III-N material that can be grown by MOCVD in the same run and same growth conditions as 2D h-BN. Thus, these transferrable solar cells could be achieved using a single material family.

In addition, recent developments on the growth of single-crystalline InGaN nanopyramids (NPs) [93] makes it possible to enhance the indium incorporation in the absorbing layer while reducing the density of structural defects and thus, to reach a power conversion efficiency beyond the state of the art of InGaN-based solar cells. Therefore, the combination of these two innovative technologies (InGaN NPs growth and 2D-hBN release and transfer) could lead to the realization of low-cost, high-efficiency and flexible photovoltaic devices.

First, we present the state of the art of InGaN-based solar cells by enhancing the motivations of the use of InGaN NPs instead of bulk InGaN as an absorber layer. Afterwards, we introduce the optical and electrical simulation results of the NP-based InGaN structures and we present the growth and fabrication of these solar cell structures through three different generations of devices. Finally, we discuss the perspectives and further work needed to achieve the high-efficiency, low-cost and transferrable InGaN solar cells on 2D h-BN.

5.2 The State of the Art of InGaN Solar Cells

The evolution of photovoltaics technologies is usually divided into three generations. The first generation is based on monocrystalline and polycrystalline silicon. The efficiency of this solar cells is mainly limited by the low bandgap of silicon. The second generation is based on thin-film materials such as CIGS, CdTe and amorphous silicon. The reduction of materials amount and the vacuum-based deposition methods needed to produce these cells make them cheaper and more efficient. However, even if CIGS and CdTe PV cells offer high efficiency at a lower cost than silicon, the future of this technology may run into difficulty due to the use of scarce and toxic materials [94], [95]. The third generation of photovoltaics is based on the investigation of new materials such as organics, dye-sensitized solar cells, quantum dot-sensitized solar cells, perovskites and multi-junction III-V semiconductors. Each of these materials has particular advantages and drawbacks concerning efficiency, stability, cost, transparency and flexibility [96].

In the last decades, the III-Nitride InGaN alloy has received a particular attention for its potential in photovoltaics applications. Due to its direct and variable bandgap -from 0.64ev (InN) to 3.4eV (GaN)-, InGaN covers the entire solar spectrum [97] (Figure 44) and enables the fabrication of high-efficiency multi-junction solar cells with a single material. In addition, InGaN has a high absorption coefficient (10^5 cm^{-1}) allowing to absorb 90% of the incident light with few hundreds nanometers thick layers, which reduces significantly the amount of the material needed and subsequently the cost of the solar cells. Moreover, its resistance to high energy radiations and high temperatures makes it a promising candidate for concentrated photovoltaics (CPV) and space applications.

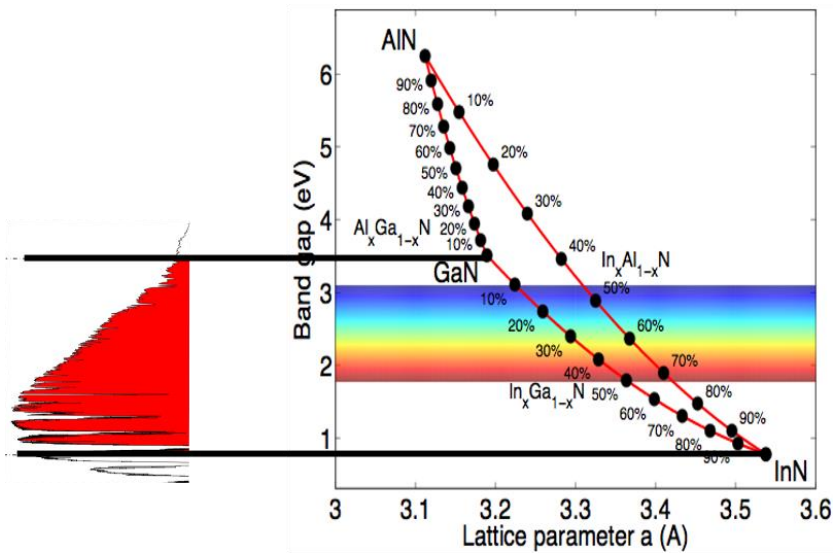

Figure 44 - Band gap energies of the InGaN alloy system covering the entire solar spectrum [97].

However, due to large lattice mismatch between GaN and InN, the growth of thick, strained and high-crystalline 2D bulk InGaN layer is technologically challenging. Lowering the bandgap of InGaN by increasing the indium incorporation results in the degradation of the epitaxial layer through a high defects and threading dislocations densities as well as phase separation of indium due to the relaxation of the epitaxial mismatch stress (Figure 45), which hindered the performances of the photovoltaics devices [98], [99]. Other issues such as high InGaN/GaN interface polarization charges [100], [101] and sensitivity of InGaN to the growth temperature of the p-type GaN top layer lower the efficiency of InGaN solar cells [102]. Various approaches have been used to realize InGaN-based solar cells including bulk InGaN homojunctions [103] and heterojunctions [104], InGaN/GaN semibulk [105] and superlattices [106], InGaN/GaN multi-quantum wells (MQWs) [107], [108]. However, the performances are hindered by the above-mentioned issues.

The highest conversion efficiency ever reported for InGaN solar cells is 5.95%, achieved with a 20-period MQW structure with 19% indium content [109].

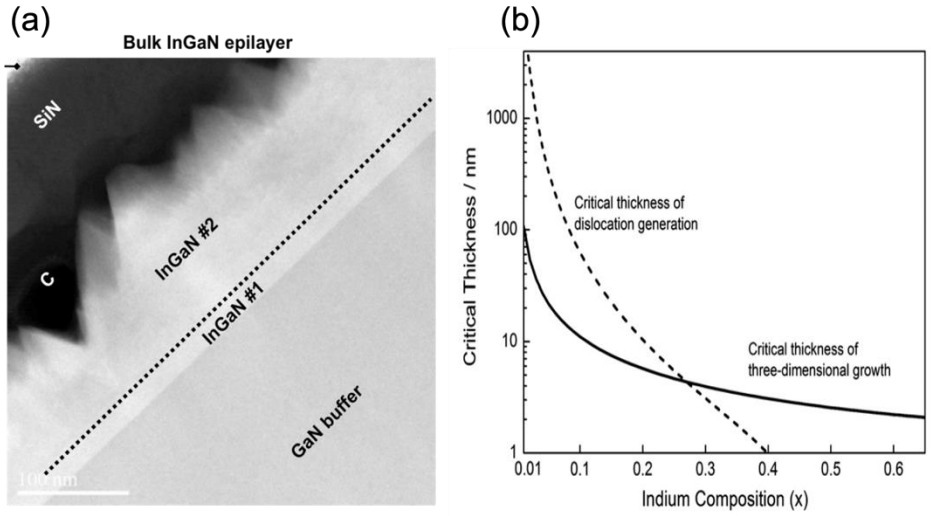

Figure 45 - Three dimensional growth of bulk InGaN[98]. (b) Critical thickness of dislocation generation and three-dimensional growth versus indium composition x ($In_xGa_{1-x}N$) [99].

High-efficiency InGaN solar cells need high indium content and high crystalline quality of the InGaN absorber layer. In this context, InGaN-based 3D nanopyramids (NPs) achieved by our group at IRL 2958 GT-CNRS with high crystalline quality and high indium content can be used [93], [110]. This approach is based on metalorganic chemical vapor deposition (MOCVD) and nano-selective area growth (NSAG). An indium incorporation of 33% on AlN buffered Si(111) was achieved, as shown in Figure 46. Moreover, owing to their three-dimensional geometry, InGaN NP-based devices could provide a unique advantage over thin films in the area of flexibility when grown on 2D layered h-BN substrates and transferred to a flexible substrate.

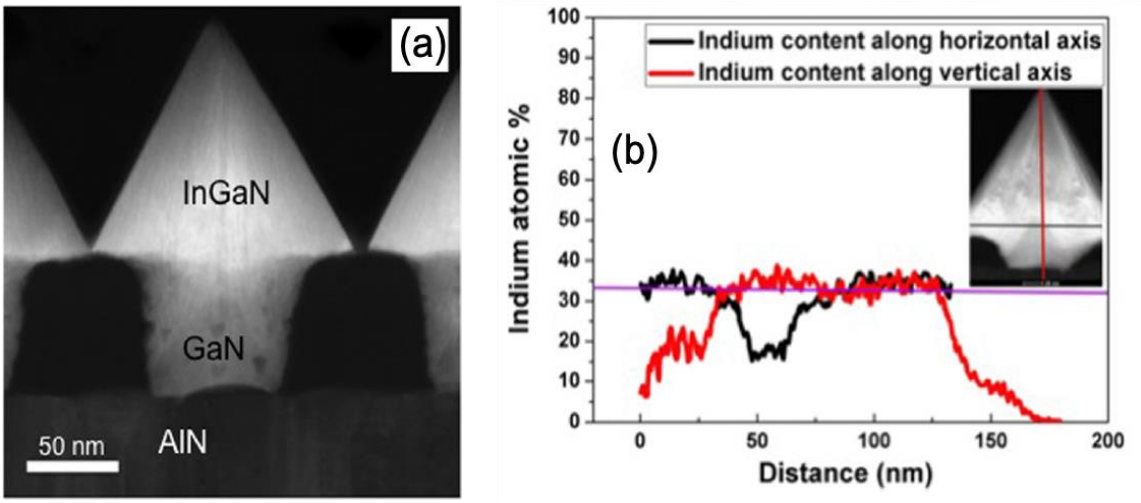

Figure 46 - (a) Cross sectional HAADF-STEM images of single InGaN NPs. (b) EDX line scans for indium in InGaN NPs along the vertical and horizontal axes of the NP [110], [93].

One of the objectives of this thesis is the realization of low-cost, high efficiency InGaN solar cells. This target is possible by combining different innovative technologies. First, recent developments of the InGaN-NP growth method makes it possible to enhance the indium incorporation in the material while reducing the density of structural defects. Then, the combination of the h-BN-based lift-off process (demonstrated for lateral and vertical LEDs in Chapter 4) can allow the implementation of low-cost and high-efficiency InGaN solar cells through (i) the transfer to flexible substrates, (ii) the fabrication of tandem cells by transferring the NP-based InGaN cells on top of a silicon solar cell and (iii) the realization of NPs InGaN multi-junctions by stacking solar cells with different indium incorporations.

5.3 Simulation of Nanopyramid-based InGaN Solar Cells

To increase the indium incorporation in the absorber layer and cover a large portion of the solar spectrum while reducing the structural density of dislocations and defects and avoiding the phase separation of indium, we propose an approach based on a three-dimensional (3D) structure, namely InGaN NPs. The nano-selective area growth of InGaN NPs have recently exhibited encouraging results. GT-CNRS group recently demonstrated NPs-based absorbers grown by MOCVD that are single-phase, defect-free, fully relaxed with high indium incorporation up to 33%, which is almost twice as high as in planar InGaN grown in the same conditions [93], [110].

In order to have a better understanding of the optical and electrical properties and to achieve a high-efficiency InGaN NP-based solar cell, we carried a modeling study by coupling optical and electrical simulation tools, FDTD Lumerical and Silvaco ATLAS, respectively. We also computed and compared the electro-optical performances of both planar and NP-based InGaN solar cells under 1.5 air-mass solar spectrum conditions.

The double hetero-junction solar cell structure studied is shown in Figure 47. It is a p-GaN/InGaN/n-GaN structure where the InGaN absorber is interposed between p- and n-GaN layers. The InGaN absorber is an array of NPs separated by an SiO_2 mask. The p- and n-regions are doped by Mg and Si respectively. For the modeling purpose, the device described by a primitive cell (Figure 47a) with periodic boundary conditions in both x- and y-axis. The parameters of the simulated cell are described in Figure 47b and the simulation flowchart is described in Figure 48. All the simulation work was done considering AM1.5G solar spectrum conditions.

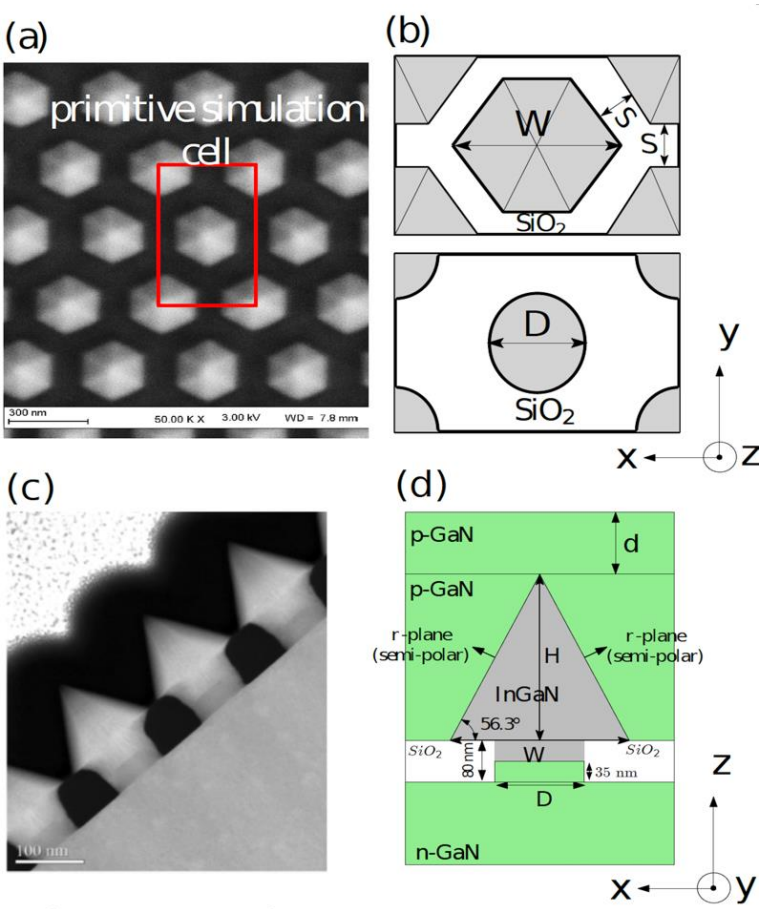

Figure 47 - (a) SEM top view image of the InGaN NP array. (b) Top view of the modeled structure. (c) SEM cross section image of the InGaN NP. (d) Cross-sectional view of the single NP modeled structure [122].

The particularity of the hexagonal pyramid-shaped structure required the use of a FDTD method to model the light-matter interaction and to compute the dependence of absorption, photo-generation rate and ideal photo-current at each node of the structure with the p-GaN layer thickness (d), width of the NP (W) and pyramid spacing (S).

The output of the optical simulation is used as the input for the electrical simulation. For that, the total photo-generation rate is averaged along the y-direction in order to provide the photo- generation rate map used for 2D Silvaco simulation of the electric transport in the device.

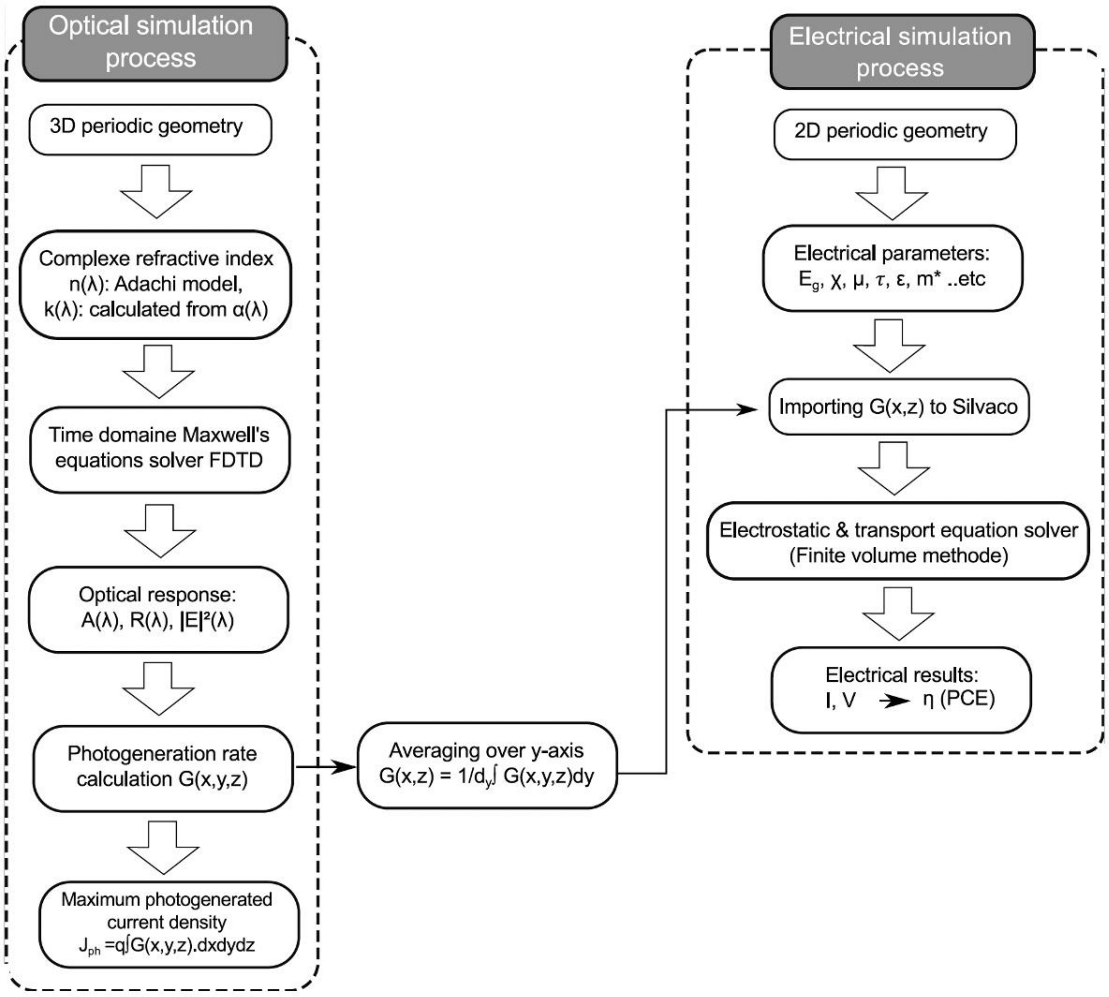

Figure 48 - Coupled optical-electrical simulation flowchart [122].

In order to find the optimized structure for our solar cells, we varied the holes diameter (D), the width and spacing of NPs (W and S, respectively) as well as the thickness of the subsequent p-GaN top layer. The important output physical quantities we focused on where the absorption, the photo-generation rate and the ideal photo-current. These results allows to determine the optimize design parameters that we will rely on for the nanolithography SiO_2 mask fabrication as well as the growth of the NPs and p-GaN top layer.

5.3.1 Optical Simulation

To model the light-matter interaction we started from the absorp- tion of light by the solar cell. The absorption coefficients α for InGaN alloys were calculated using the following equation[111]:

$$\alpha = \sqrt{a \times (E - E_g) + b \times (E - E_g)^2}$$

where a and b are setting parameters depending on the indium composition. E is the incident photon energy, E_g is the bandgap energy which is calculated using the following Vegard's law:

$$E_g = x \times E_g^{InN} + (1 - x) \times E_g^{GaN} - b \times x \times (1 - x)$$

where x is the alloy fraction and b the bowing factor. Refractive index is computed using the model developed by Adachi [112]:

$$n(\omega) = \sqrt{A(x) \times (\frac{E_g}{h\omega})^2 \times \left[2 - \sqrt{1 + \frac{h\omega}{E_g}} - \sqrt{1 - \frac{h\omega}{E_g}}\right] + B(x)}$$

where ω is the optical frequency, and $A(x)$and $B(x)$ are setting parameters depending on the alloy fraction x as:

$$A(x) = 9.827 \times (1 - x) - 53.57 \times x$$

$$B(x) = 2.736 \times (1 - x) - 9.19 \times x$$

We have considered InGaN and GaN materials as being optically isotropic. Given the sub-wavelength thickness of InGaN NP, the bi-refringence should have anyway small effect on the simulation result. The photo-generation rate is extracted by dividing the absorbed power by the photon energy:

$$g(r,\omega) = \frac{P_{abs}(r,\omega)}{\hbar\omega}$$

where $P_{abs}(r,\omega)$ is the optical power absorbed per unit volume from a monochromatic source at an angular frequency ω and position r, which is obtained by:

$$P_{abs}(r,\omega) = -0.5 \times \omega \times |E(r,\omega)|^2 \times \Im\,|\epsilon(r,\omega)|$$

where $E(r,\omega)$ is the electric field spectral density [$V^2\ m^{-2}\ Hz^{-1}$] and ϵ is the frequency dependent permittivity. The total photo-generation rate is given by the integration over the frequency:

$$G(r) = \int g(r,\omega) \times d\omega$$

The photo-generated current J_{ph}, estimated with the assumption that each absorbed photon generate an electron-hole pair collected at the electrical contacts, is given by:

$$J_{ph} = \frac{q}{A} \int G(r) \times dr$$

where q is the electron charge and A is the primitive cell surface area.

Figure 49 shows the ideal photocurrent density J_{ph} as a function of the spacing between NP varying in the range $0\,nm \leq S \leq 80\,nm$ and width of NP varying in the range $1.25 \times D\ (to\ avoid\ holes\ overlap) \leq W \leq 2 \times D$, and mapped for three different hole diameters varying between $80\,nm$ and $170\,nm$ in the SiO_2 mask (D). The p-GaN top layer thickness has been optimized for each couple of parameters (*S*, W) to get the highest possible J_{ph}. Since increasing W or decreasing *S* lead to a thicker effective planar InGaN layer then J_{ph} increases correspondingly from 3.2 mA/cm^2 (for $D = 80\,nm$, $S = 80\,nm$ and $W = 100\,nm$) up to 7.45 mA/cm^2 (for $D = 170\,nm$, $S = 0\,nm$ and $W = 340\,nm$). As expected, densely packed and large NP are preferable to obtain large J_{ph}.

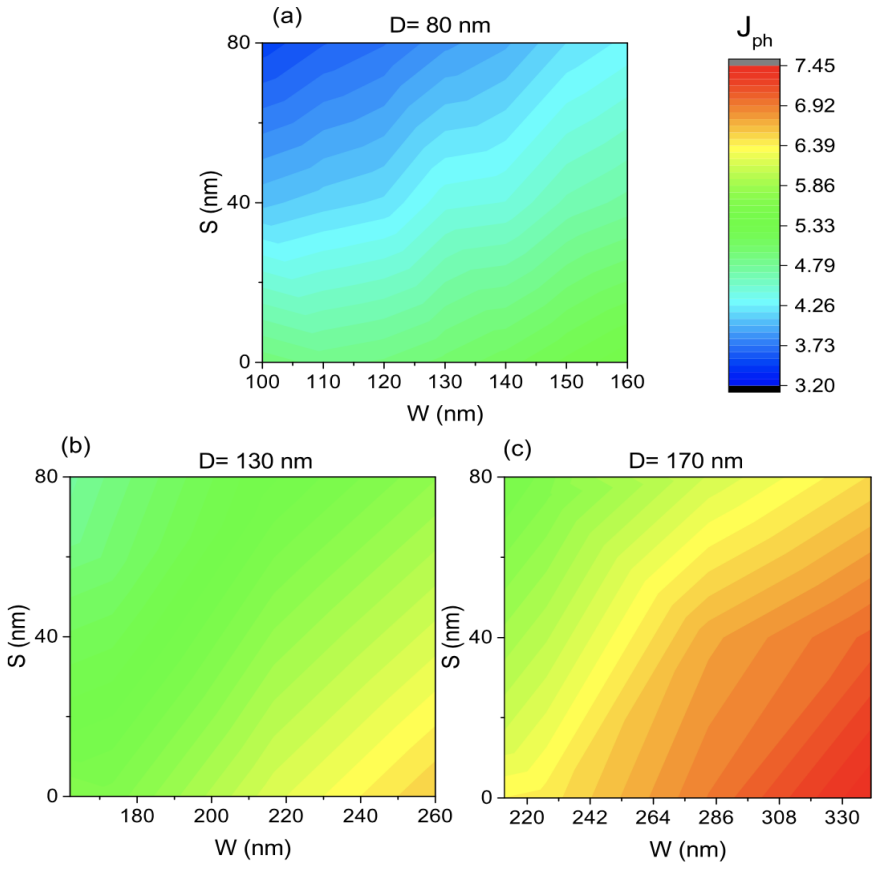

Figure 49 - Photo-current density J_{ph}(mA/cm^2) as function of the spacing between NP (S) and width of NP (W) mapped for different hole diameter in the SiO_2 mask (D = 80 nm, D = 130 nm and D = 170 nm) [122].

In order to have more insights on the role of the p-GaN thickness, Figure 50 shows the variation of J_{ph} as function of both the p-GaN top layer thickness and width of the NP for a hole diameter in the SiO_2 mask D = 170 nm and for a spacing between the NP equal to zero, which corresponds obviously to the largest InGaN absorber effective thickness (total InGaN NP volume distributed on a planar layer having the surface area of the solar cell; as there are two pyramids inside the primitive modeled cell, the calculated equivalent thickness is the sum of both the volume of InGaN hexagonal pyramid and InGaN cylinder inside the hole multiplied by 2, this volume is then divided by the primitive cell surface which can be deduced from the hexagonal pyramid dimensions and the space between these pyramids) and thus highest optical absorption and J_{ph}. The variation of J_{ph} with *d* or *W* is not monotonic. The presence of maxima and minima in the dependence of *Jph* can be explained by a modulation of the optical reflection at the top surface of the solar cell induced by the interference phenomenon between the optical waves reflected at the top surface and at the p-GaN/SiO_2 interface, respectively. This phenomenon occurs whatever the solar cell structure is.

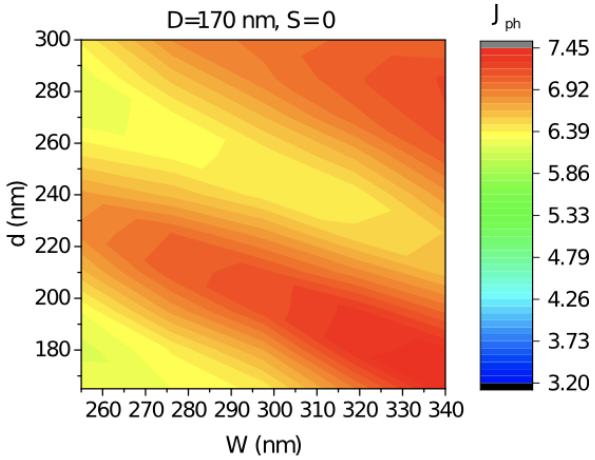

Figure 50 - Photo-current density J_{ph} (mA/cm^2) as function of the p-GaN top layer thickness and width of the NP for a hole diameter in the SiO_2 mask D = 170 nm and for spacing between the NP equal to zero [122].

To compare the performance of the InGaN NP absorber-based solar cell with those of the planar InGaN absorber-based solar cell whose absorber thickness is an effective thickness corresponding to the volume of the InGaN NP, Figure 51 shows the $J_{ph}(W, D)$ maps obtained in both cases for an optimized p-GaN top layer thickness and a zero spacing between the NPs. As expected, for both devices, J_{ph} increases with both *W* (more markedly) and *D* since this corresponds to an increase of the effective InGaN absorber thickness. Nevertheless, for a width of NP larger than 170 nm (corresponding to an effective thickness of around 55 nm), J_{ph} becomes higher in the case of the InGaN NP absorber based solar cell. It reaches, for W = 340 nm and D = 170 nm (corresponding to an effective InGaN thickness of around 95 nm), a value of about 7.4 mA/cm^2 corresponding to an increase of 9% when compared to the 95 nm thick planar InGaN solar cell (J_{ph} = 6.79 mA/cm^2).

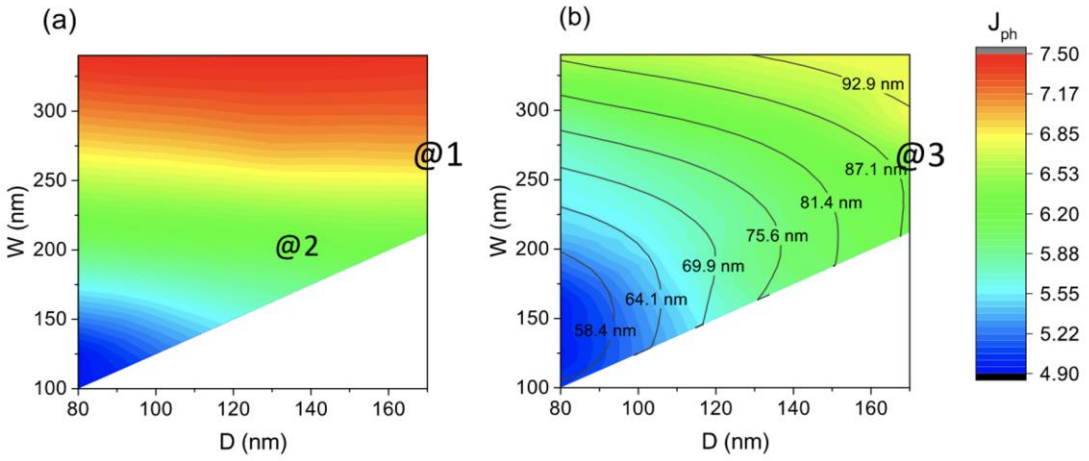

Figure 51 - $J_{ph}(D, W)$ (mA/cm^2) maps of the (a) InGaN NP absorber-based solar cell and (b) planar InGaN absorber-based solar cell whose absorber thickness is an effective thickness corresponding to the volume of the InGaN NP, for an optimized p-GaN top layer thickness and a spacing between the NP S = 0 nm. The lines in (b) indicate the corresponding effective planar InGaN layer thickness [122].

This originates from an increase of the absorption which can be explained by a light-trapping effect in the NP due to the nano-structured SiO_2 mask, as evidenced by Figure 52 which compares the cross- section maps of the optical electric field intensity, obtained (using Lu- merical software) at a wavelength equal to 525nm, for the three cases marked @1 and @2 (InGaN NP absorber-based solar cell), and @3 (planar InGaN absorber-based solar cell) in Figure 51.

A periodic vertical optical electric field intensity pattern, originating from the interference effect mentioned previously, is observed in the three cases. This pattern is more intense for the InGaN NP solar cell (Figure 52a and 52b) because of the larger refractive index contrast at the interface between the SiO_2 mask and the InGaN NP, when compared to the p-

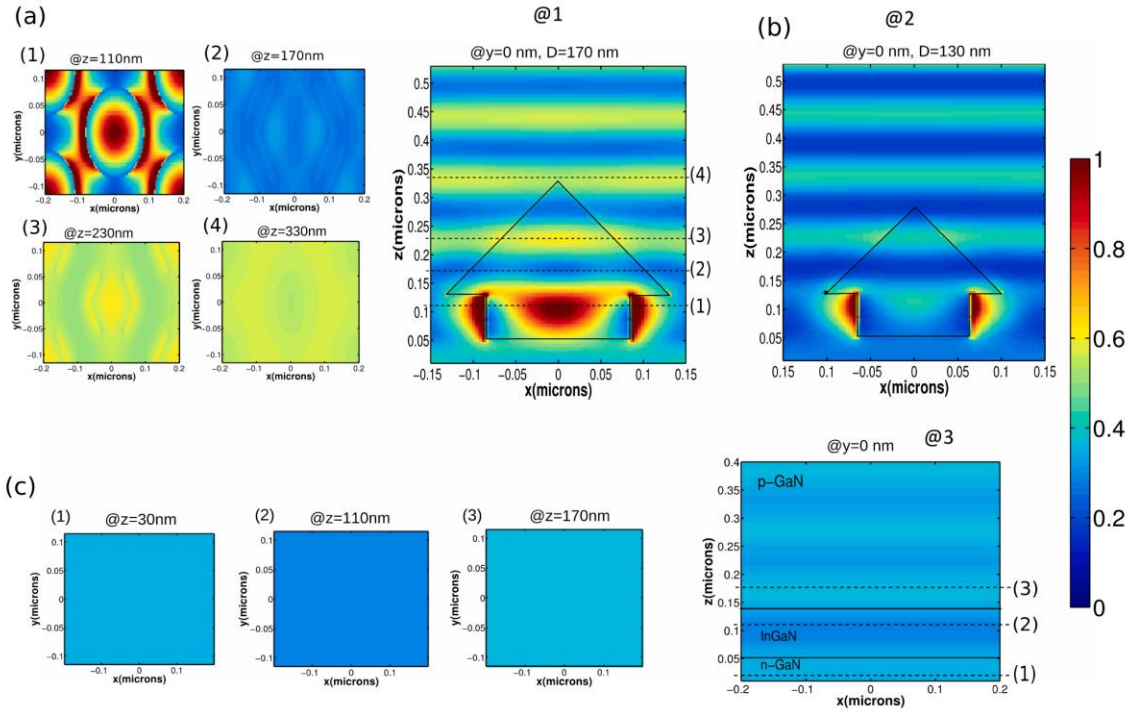

Figure 52 - Cross section (x,y) and (x,z) maps of the normalized optical electric field intensity obtained at = 525 nm for (a) @1 and (b) @2 InGaN NP absorber-based and (c) @3 planar InGaN absorber-based solar cells. See Figure 51 for the @1, @2, @3 marks. Optical absorption has not been taken into account to clearly highlight the light trapping effect [122].

GaN/InGaN interface refractive index contrast of the planar InGaN solar cell (Figure 52c). In the case of the InGaN NP solar cell, it is also more intense for large W and D because of the broader SiO_2/InGaN interface. The light trapping in the NP is clearly seen in Figure 52a showing a large optical confinement in the base of the NP and a less pronounced one in the upper part of the NP. It is to be noticed that this confinement disappears for the smaller size NP (Figure 52b) because of the wavelength of the light which is probably beyond the cut-off wavelength allowing the optical confinement. This optical confinement is probably generated by the horizontal sub-wavelength grating mirror (SiO_2 mask with holes filled by InGaN material on top of a low refractive index sub-layer (n-GaN)) [113].

Considering the band gap of the InGaN absorber with 30% of In content, a maximum photocurrent of 13mA/cm2 is expected for AM1.5G solar spectrum conditions. The difference between this value and those of 7.4 mA/cm^2 (largest value of J_{ph} obtained for an opening in the SiO_2 mask of D = 170 nmand a NP width of W = 340 nm) can be explained by either the reflection loss at the front surface which is about 20%, and partial absorption due to the limited effective thickness of the InGaN absorber which is about 95 nm in this case. Therefore, if we consider, as proposed by Dahal et al. [114], an anti-reflective coating (ARC) and a dielectric mirror (DM) on the top and bottom of the solar cell, respectively, the solar cell absorption spectrum can be tuned in such a way that the photocurrent is increased by 24% to reach 9.2 mA/cm^2 (see Figure 53a). The ARC design used in our simulation is close to those achieved by Young et al. [115], and for the DM, which is advantageous for the combination of high band gap InGaN-based solar cells with

silicon [116] we have considered two multi-layered Si_3N_4/SiO_2 and Ta_2O_5/MgF_2 stacks allowing reflection larger than 80% in the 350–620 nm wavelength range (see Figure 53b).

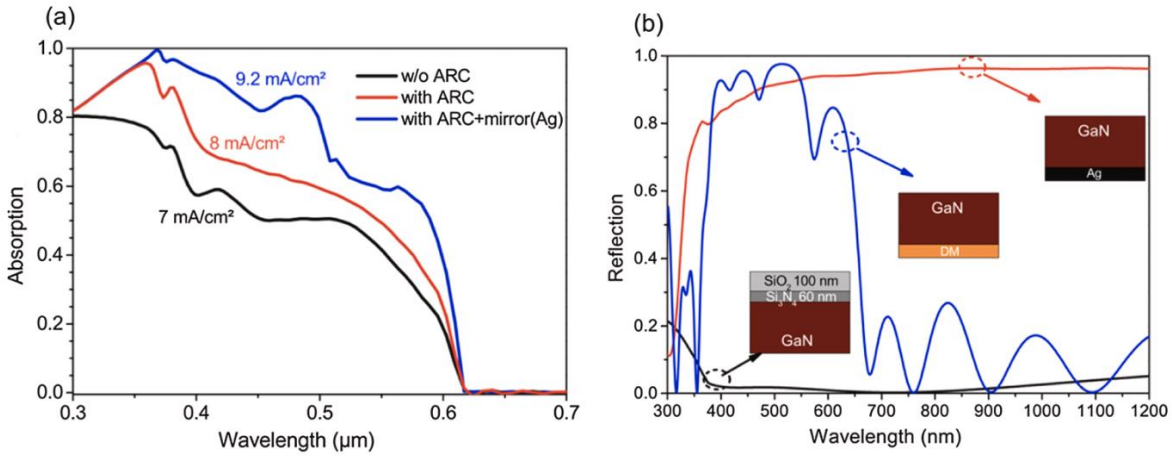

Figure 53 - Tuning solar cell (a) absorption and (b) reflection spectra using a multi-layered SiO_2/Si_3N_4 anti-reflection coating at its top and a metallic mirror (Ag) or a DM constituted of two multi-layered Si_3N_4/SiO_2 and Ta_2O_5/MgF_2 stacks at its bottom [122].

5.3.2 Electrical Simulation

To further assess the InGaN NP absorber-based solar cell performance, we have conducted 2D electrical simulation using Silvaco software which does not solve properly 3D 6-faceted pyramids. For that, we have produced a 2D photo-generation rate map from the 3D photo-generation rate map by flattening it along the y-axis using a spatial averaging which almost allows for the conservation of the total photo-generated carriers throughout the volume of the NP [117]. Then, this approximate 2D map serves as input data for 2D electrical simulations using Silvaco software. Due to the large conduc- tion band offset (ΔE_c) at the InGaN/GaN hetero-interface, we have used the thermo-ionic-field emission carrier transport model proposed by Yang et al. [118]. We have accounted for Shockley-Reed-Hall (SRH), and surface and radiative recombinations. A surface recombination velocity

of 10^4cm/s for electrons and holes is specified at the front surface. The radiative coefficient and carriers' lifetime are taken from El-Huni et al.[119]. As the NSAG NPs are considered fully relaxed [110], we have chosen a bowing factor of 2.59 eV based on the work done by Islam et al. [120] for absorption band gap of relaxed InGaN. The same bowing factor has been used to calculate the electron affinity for InGaN. This is based on the study done by Moses and Van de Walle [121] showing that the valence band maximum varies linearly with the indium composition. More details about the physical models and parameters' values can be found in Ref [119], including electric mobility and effective mass. Parameters used in the simulations can be found in Ref [122].

To take into account of the polarization-induced charge, we have adapted the model developed by Romanov et al.[100]. This model computes the polarization difference at the InGaN/GaN hetero-interface along the semipolar direction as:

$$\Delta P = P_{Lz'}^{pz} + \left(P_L^{sp} - P_T^{sp}\right) \times \cos\vartheta$$

where P_L^{sp} and P_T^{sp} are the spontaneous polarizations in the grown layer and substrate, respectively. is the inclination angle of the c-axis relative to the normal of the hetero-interface. $P_{Lz'}^{pz}$ is the strain-induced piezoelectric polarization component of the layer defined as:

$$P_{Lz'}^{pz} = e_{31}\cos\vartheta\varepsilon_{x'x'} + \left(e_{31}\cos^3\vartheta + \frac{e_{33} - e_{15}}{2}\sin\vartheta\sin2\vartheta\right)$$
$$\varepsilon_{y'y'} + \left(\frac{e_{33} + e_{15}}{2}\sin\vartheta\sin2\vartheta + e_{33}\cos^3\vartheta\right)\varepsilon_{z'z'} + ([e_{31} - e_{33}]\cos\vartheta\sin2\vartheta + e_{15}\sin\vartheta\cos2\vartheta)\varepsilon_{y'z'}$$

where e_{ij} and ϵ_{ij} are the piezoelectric and strain coefficients, respectively. Figure 54 shows the obtained hetero-interface polarization difference (P) as a function of the inclination

angle for a strained $In_{0.3}Ga_{0.7}N$ layer on top of a GaN layer (case of planar solar cell) and a strained GaN layer on top of an $In_{0.3}Ga_{0.7}N$ (case of NP solar cell). The colored regions correspond to growth planes for which polarization charges lead to an increase of the internal electric field. NP-based solar cells for which the hetero-interfaces lie on the r-plane ($\vartheta = 56.7°$) have unfavorable P much less than planar solar cells for which the hetero-interface lie on the c-plane ($\vartheta = 0°$).

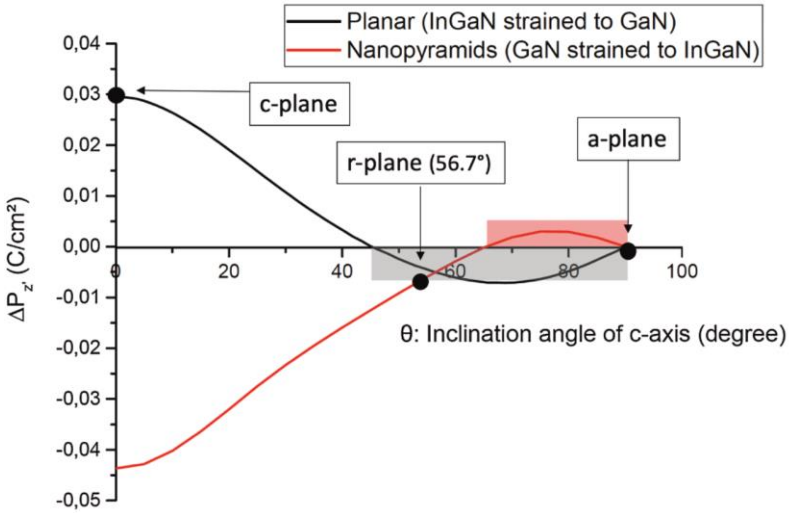

Figure 54 - Polarization difference at the hetero-interface as a function of the inclination angle of the c-axis (z) with respect to the normal at the interface (z′) for planar and NP based InGaN solar cells. The colored regions correspond to growth planes for which polarization charges lead to an increase of the internal electric field ($45° < \vartheta < 90°$ for planar solar cells and $65° < \vartheta < 90°$ for NP solar cells) [122].

Figure 55a shows an example of 2D photo-generation rate map obtained when using the optimized geometric parameters and for AM1.5 illumination conditions. The photo-generation rate is larger in the down part than in the upper part of the NP. This is due to both the larger volume and optical electric field intensity of the InGaN absorber in the down part of the NP as show in Figure 55b and 55c. This approximate 2D map serves then as input data for 2D electrical simulations using Silvaco software.

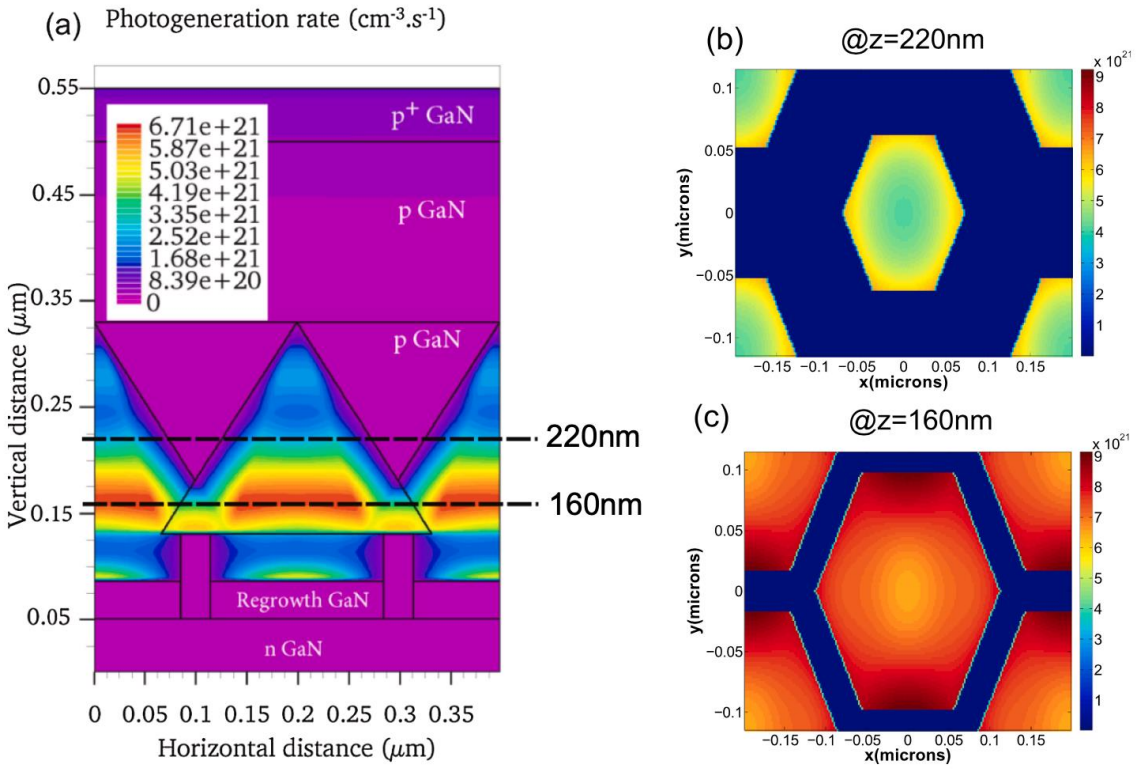

Figure 55 - (a) 2D photo-generation map calculated from the 3D photo-generation map using the optimized geometric parameters and for AM1.5 illumination con- ditions. Cross section of the 3D photo-generation map at a NP height of (b) 220 nm and (c) 160 nm [122].

To check the validity of our models and approach we have first computed the value of J_{ph} in the case of an opening in the SiO_2 mask of D = 170 nm and a NP width of W = 340 nm using Silvaco and the approximated 2D map. With these conditions, using Lumerical and 3D map, as seen before, we found J_{ph} = 9.2 mA/cm^2. The value obtained using Silvaco and considering a defect-free device (since Lumerical does not support electric transport) is equal to 9.165 mA/cm^2. The two values are in a very good agreement confirming the validity of the chosen approach for the simulation and electric models. We then have studied the role of both the p-GaN, u-InGaN and n-GaN doping on the solar cell performance. To achieve high efficiency InGaN solar cells, a high level of doping for the

p-GaN and n-GaN layers is required to limit the barrier height at the hetero-interfaces, while low u-InGaN residual doping is needed [123] to keep the width of the depletion region as large as possible. These requirements are all the more crucial as the discontinuity in spontaneous and piezoelectric polarization generates interface charges that produce supplementary and strong band bending and potential barriers as well as electric field that hinders separation of photo-generated carriers [124]. If highly doped n-GaN layer can be grown relatively easily [125], the growth of highly p-type GaN layers remains difficult [126] and the undoped InGaN typically demonstrates n-type conductivity resulting from a high background concentration [127].

Figure 56 shows the dependence of the power conversion efficiency (PCE) as function of the n-GaN and p-GaN doping concentration for both InGaN NP absorber-based and planar InGaN solar cells and for a residual donor concentration in the InGaN of $8 \times 10^{16} cm^{-3}$.

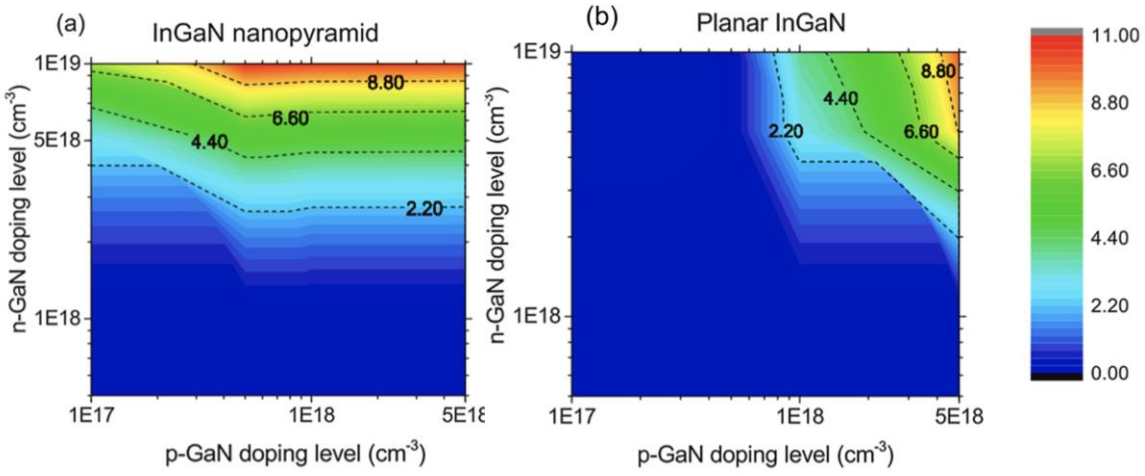

Figure 56 - Dependence of the PCE with respect to either n-GaN and p-GaN doping concentrations for both (a) InGaN NP absorber-based and (b) planar InGaN solar cells[122].

High PCE can be obtained for a n-GaN doping concentration larger than 8×10^{16}cm $^{-3}$ whatever the solar cell structure (InGaN NP or planar InGaN). As mentioned above, this is due to the large barrier in the conduction band at the n-GaN/InGaN hetero-interface which is the same for both structures, and can be lowered by increasing the n-GaN doping concentration, leading to the accumulation of a large positive charge in the n-GaN region close to the interface causing an inversion layer in the InGaN layer which in turn leads to the screening of the polarization-induced charges (see Figure 57). On the other hand, it is to be noticed that the constraint on the p-GaN doping concentration is highly relaxed in the case of the InGaN NP absorber-based solar cell when compared to the planar InGaN solar cell. Indeed, to reach the maximum PCE, the required p-GaN doping concentration is one order of magnitude less in the InGaN NP absorber-based solar cell than in the planar InGaN solar cell (5×10^{17}cm $^{-3}$ instead of 5×10^{18}cm $^{-3}$). This is due to the fact that the p-GaN/InGaN interface in the case of the InGaN NP is along the r-planes which induce much less polarization charges effect. Thus, a given p-GaN doping concentration allows for an accumulation of negative charges in the p-GaN region which is enough to create an inversion layer, and thus an electric field allowing the separation of the photo-carriers, in the InGaN layer in the case of the InGaN NP solar cell (see Figure 58). In the case of the planar InGaN solar cell, for the same accumulation of negative charges in the p-GaN region, the polarization charge effect is stronger (p-GaN/InGaN interface along the c-planes), leading to the accumulation of negative charges in the InGaN region and creation of an electric field that hinders separation of photo-generated carriers.

To conclude the study of the role of doping, Figure 59 shows the de- pendence of the PCE with the residual donor concentration of the InGaN layer for both InGaN NP absorber-

based and planar InGaN solar cells and for different p-GaN doping concentration, and with a n-GaN doping concentration of 1×10^{19}cm $^{-3}$.

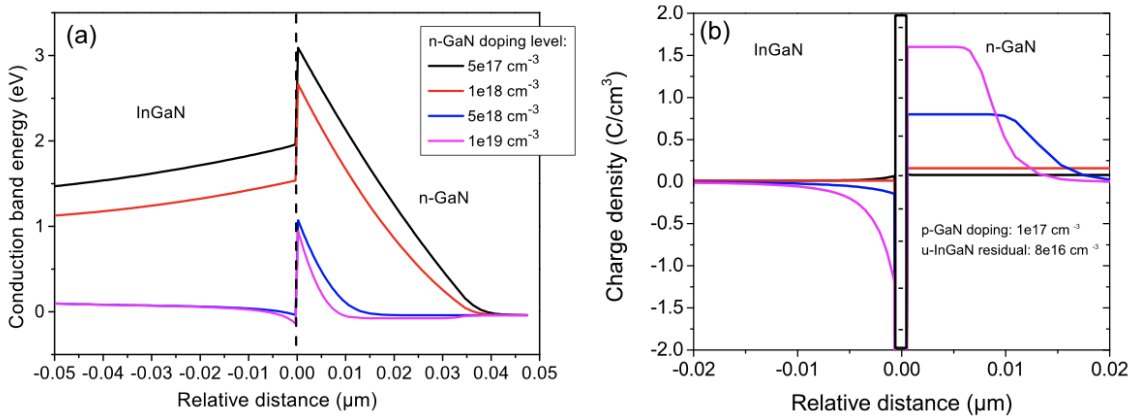

Figure 58 - (a) Conduction band and (b) charge distribution at the n-GaN/InGaN hetero-junction for different level of the n-GaN doping concentration [122].

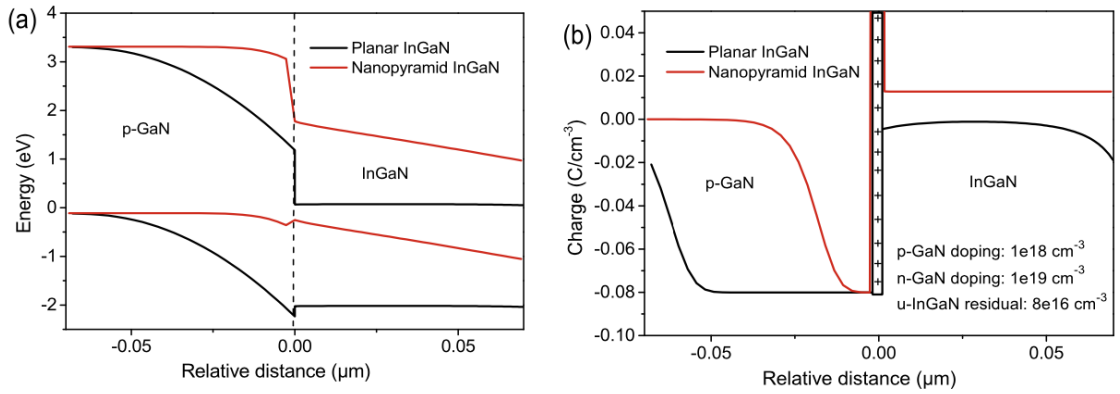

Figure 57 - (a) Energy band diagram and (b) charge distribution at the p-GaN/InGaN hetero-junction for both InGaN NP absorber and planar InGaN based solar cells [122].

For residual donor concentration of the InGaN layer up to around 1×10^{17}cm $^{-3}$, the PCE exhibits slight variations (increase or decrease) whatever are the p-GaN doping concentration and the type of solar cell. The slight increase of the PCE can be explained by the increase of the V_{oc} due to the shrinking of the space charge region while the J_{sc} remains constant (see inset of Figure 59). Beyond this residual concentration level, a decrease of the PCE can be noticed especially in the case of the InGaN NP absorber-based

solar cell with a p-GaN doping concentration of 5×10^{17}cm $^{-3}$. This can be explained by the fact that the overlap between the region where the photo-generation rate is high and the region where the drift electric field is high becomes weaker, especially for a high residual donor concentration of the InGaN layer. This phenomenon is even stronger because of the diffusion length of the photo-carriers which becomes smaller with the increase of the residual donor concentration. Finally, Figure 59 shows that InGaN NP absorber-based solar cells can tolerate a higher InGaN residual donor concentration than that of the planar InGaN solar cells.

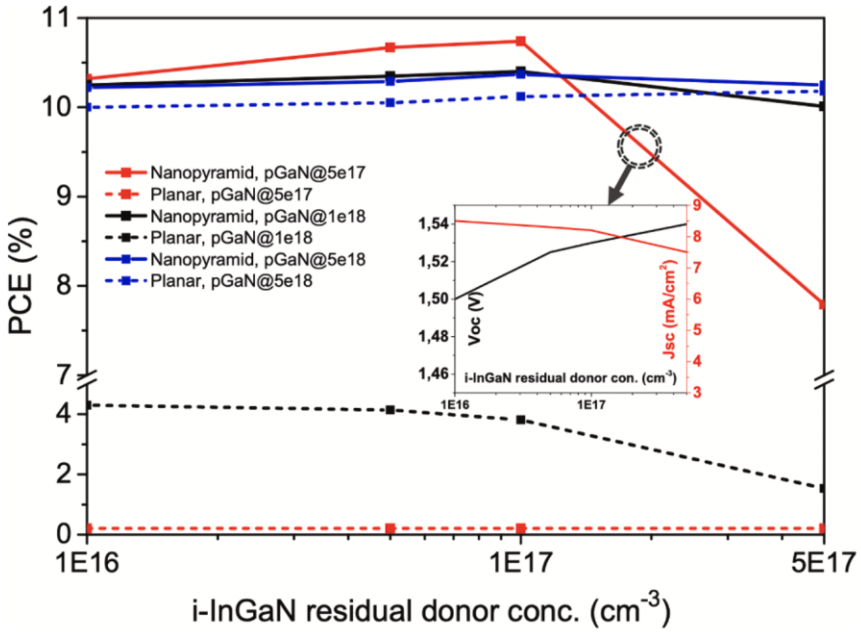

Figure 59 - Dependence of the PCE with respect to the residual donor concentration of the InGaN layer for both InGaN NP absorber-based and planar InGaN solar cells and for different p-GaN doping concentration with n-GaN doping concentration of 1×10^{19} cm^{-3}. The inset shows both the J_{sc} and V_{oc} dependence with the residual donor concentration of the InGaN layer [122].

The $In_{0.3}Ga_{0.7}N$ NP absorber-based solar cell, optimized in terms of mask opening, doping, ARC and back mirror, can reach a PCE of 10.8% using currently available technologies.

In summary, we have modeled and investigated the performances of InGaN NP-based solar cells with 30% indium content. When compared to planar InGaN solar cells, the NP-based solar cells show that the semi-polar growth planes lead to less polarization charges in the InGaN/GaN interface, which allows to handle ten times less acceptors concentration in the p-GaN top layer while maintaining the same performances. Moreover, the SiO_2 mask used in the NP-based structure showed a light trapping effect in the SiO_2/InGaN interface, leading to a higher optical absorption and thus efficiency. Last, InGaN NP-based solar cells can allow for a higher InGaN residual donor concentration than that of the planar InGaN solar cells. Overall, an optimized $In_{0.3}Ga_{0.7}N$ NP-based solar cell can lead to an efficiency twice than that of a planar InGaN-based solar cells with standard p- and n-GaN doping level.

In the next sections, we present the growth and fabrication process of these solar cell structures through three different generations of devices. In the first and second generation we achieved the growth of a complete NP-based InGaN structure on sapphire whereas for the third generation we demonstrate the first growth of InGaN NPs on 2D h-BN/sapphire substrate.

5.4 Fabrication of Nanopyramid-based InGaN Solar Cells

5.4.1 The First Generation of the NP-based Solar Cells at GT-Atlanta

The first simulation results allowed us to optimize the nanolithography fabrication of the SiO_2-like mask used for the selective area growth of the NPs. In order to fabricate the nano-patterned mask we use the hydrogen silsesquioxane (HSQ), which is a negative-tone resist. It has been used as a negative resist for nanolithography - also referred as electron beam lithography (EBL) - , nanoimprint, and extreme ultraviolet (EUV) lithography and sub-10nm resolution, high contrast, moderate sensitivity, minimum line edge roughness, good etch resistance and high degree of mechanical stability. The cross-linking via Si-H bond scission by exposure to electron beams results in an amorphous structure of HSQ similar to SiO_2 [128]. Hence, it allows a single-step process to fabricate high-resolution nano-patterns on our substrate, which compared to the standard deposit-pattern-etch process, allows a better preservation of the substrate quality since it does not expose the bottom GaN layer to ICP plasma etching. Figure 60 shows schematics of the deposit-pattern-etch photolithography-based approach and the HSQ nanolithography-based approach.

Prior to my thesis, the first version of the nano-patterned mask was performed at Georgia Institute of Technology's Institute of Electronics and Nanotechnology (IEN) cleanrooms using the JEOL JBX 9300 FS electron-beam lithography (EBL) system armed with a 100 kV. The nano-patterned mask was fabricated on n-doped c-oriented 2-µm-thick GaN on sapphire template following the procedure described in Figure 60a. First, a 100-nm-thick HSQ layer is spin-coated and exposed to a 4 nm Gaussian electron beam with 100 kV accelerating voltage under a current of 1.9 nA.

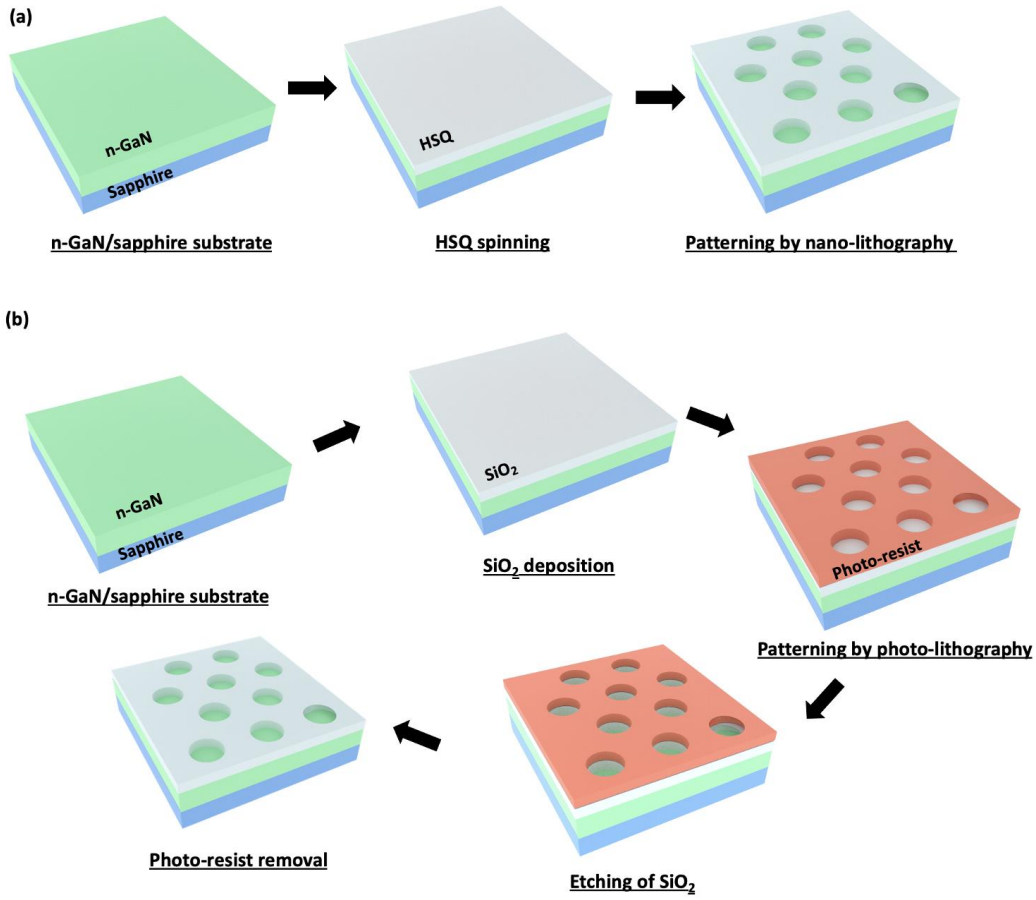

Figure 60 - Schematics of (a) the HSQ nanolithography-based approach and (b) the deposit-pattern-etch photolithography-based approach.

Then, tetramethylammonium hydroxide (TMAH) 25% developer is used to open the nano-holes that correspond to the area of HSQ not exposed to the electron beam [129]. The nano-holes are arranged in a hexagonal lattice with a diameter around 90 nm and a pitch double of their diameter as shown in Figure 61a. The optimized base dose in these conditions was found to be between 671 $\mu C/cm^2$ and 692 $\mu C/cm^2$. The fabricated glass-like masks were then sent to IRL 2958 Georgia Tech-CNRS Laboratory to perform the growth of the subsequent InGaN NPs and p-doped GaN layer by MOCVD. First, the optimized growth conditions of the InGaN layer on a ¼ of a 2-inches wafer allows a nano-selective area growth (NSAG) where the GaN nucleation layer and InGaN epitaxial NPs tends to grow

on the n-doped GaN underneath and not on the mask. High growth selectivity was obtained as shown in the Figure 61b. Details of the MOCVD growth are reported in Ref [110]. Moreover, the optimized epitaxial lateral over-growth (ELOG) conditions used to grow the subsequent p-type GaN top layer allowed to have a good coverage of the InGaN NPs as shown in Figure 62.

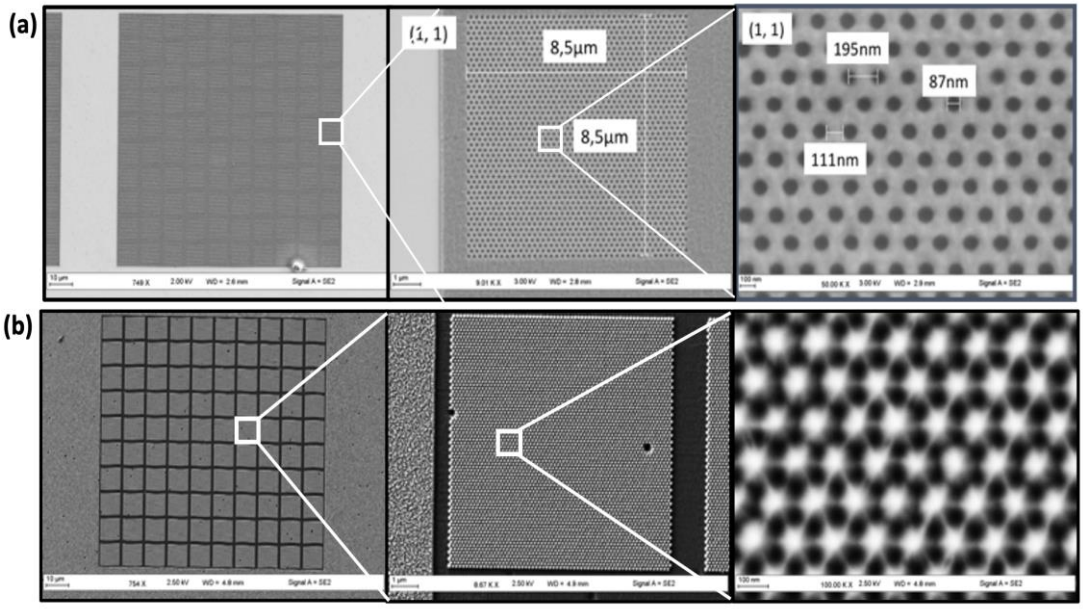

Figure 61 - SEM images of (a) thenanolithography mask on of 100 x 100 μm with squares of 8.5 x 8.5 μm achieved by Georgia Tech (Atlanta) facilities, and the (b) InGaN nanopyramids grown at IRL 2958 GT-CNRS.

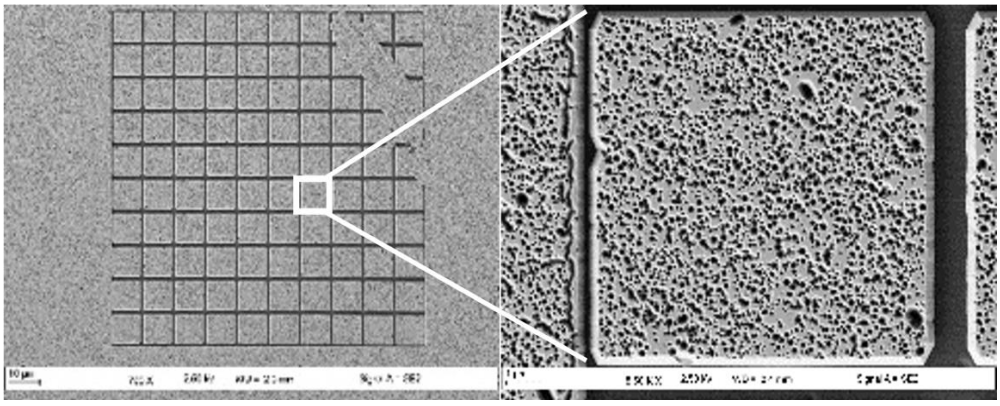

Figure 62 - SEM images of the p-type GaN top layer on InGaN nanopyramids on ¼ 2-inches wafer. Defects are due to low temperature growth of the p-GaN. Growth at higher temperatures will deteriorate the quality of the InGaN underneath.

- **Selectivity on 2-inches wafer :** When we tried to reproduce this results on a 2-inches wafer, selectivity issues during the growth of InGaN NPs emerged. High density of crystallites appeared, especially in the center of the 100 x 100 µm masks as shown in Figure 63. Moreover, the NPs were not completely covered by the p-GaN layer during the regrowth step. More investigations of the mask fabrication process and the growth conditions were needed to achieve PIN structures on 2-inches wafers.

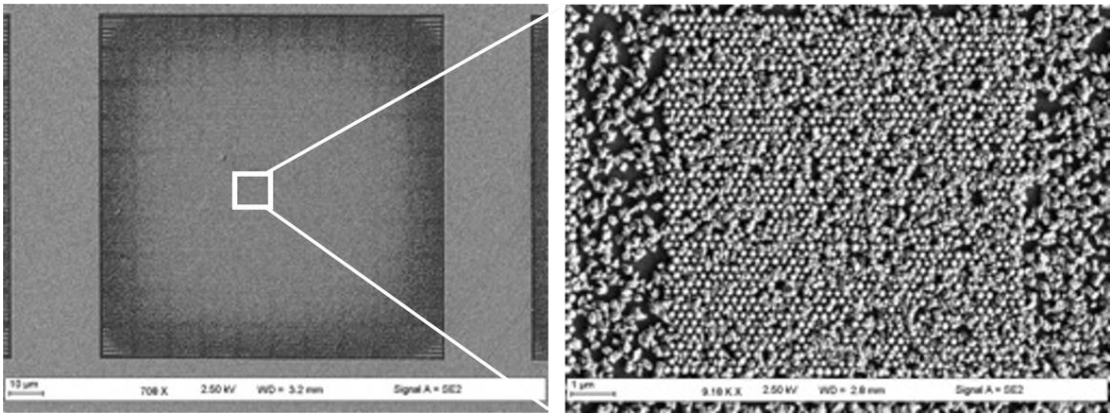

Figure 63 - SEM image after InGaN NPs growth on a full 2-inches wafer. High density of crystallites especially in the center of the 100x100 µm^2 masks.

In this period, a technology transfer of the nanolithography mask fabrication from GT-Atlanta, USA to the IRL 2958 GT-CNRS in Metz, France was decided. The optimization study of this second generation of this PIN structures is described in the following section.

5.4.2 The Second Generation of the NP-based Solar Cells at IRL GT-CNRS

In this part, the nanolithography process is operated by the RAITH eLine Plus system, which is a part of the *Institut Lafayette* cleanroom facilities. It is a versatile nanofabrication system armed with a 30 kV electron beam column and providing a Gaussian beam smaller than 2 nm. For our nano-patterns we decided to use an acceleration voltage of 25 kV, which is close to the limit of the machine and which means that the acceleration of electrons is reduced by a factor of four compared to the 100 kV exposition used before. For this purpose, the base dose of exposition needs to be re-optimized. We operated a Monte Carlo simulation by Casino software to visualize the path of electrons for a 100 kV and a 25 kV exposure. Since in e-beam lithography, most exposure occurs by secondary electrons [130] a decrease in the acceleration voltage by a certain factor should induce a decrease in the base dose by approximately the same factor in order to have the similar contrast in both cases [131]. Therefore, the Monte Carlo simulation parameters were: 100 kV and 800 $\mu C/cm^2$ versus 25 kV and 200 $\mu C/cm^2$.

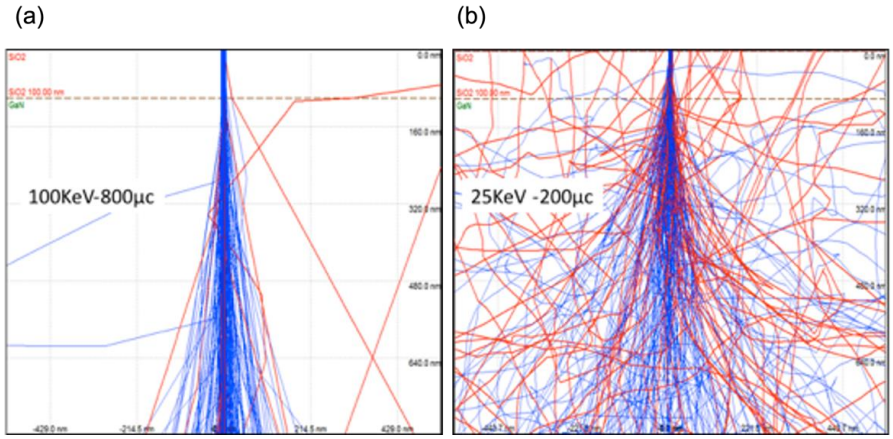

Figure 64 - Monte Carlo simulation of (a) 100 kV-800 $\mu C/cm^2$ (b) 25 kV-200 $\mu C/cm^2$. The substrate in both cases is GaN on sapphire and the HSQ layer is 100 nm thick. In blue: forward scattering path. In red: backward scattering paths.

A base dose of 200 μC/cm^2 was taken as a reference value that will be adjusted afterward through a base dose test on silicon wafers. As observed in Figure 64, forward and backward electron scattering occurs more in the 25 kV than in the 100 kV exposure. Therefore, we have more generation of secondary electrons in the 25 kV than in the 100kV exposure. Thus, since most exposure occurs by secondary electrons [130], less base dose is needed for an acceleration voltage of 25kV compared to 100kV. However, using a low acceleration voltage (25 kV) reduces the resolution of the patterned features and introduced more constraints on the size of the nano-holes we are targeting. Nano-holes of around 150 nm were then fabricated on a 2-inches n-GaN/sapphire wafers with different sizes of the mask as shown in Figure 65. The optimized base dose of electrons beam was found to be 260 μC/cm^2 for a resist thickness of 100nm.

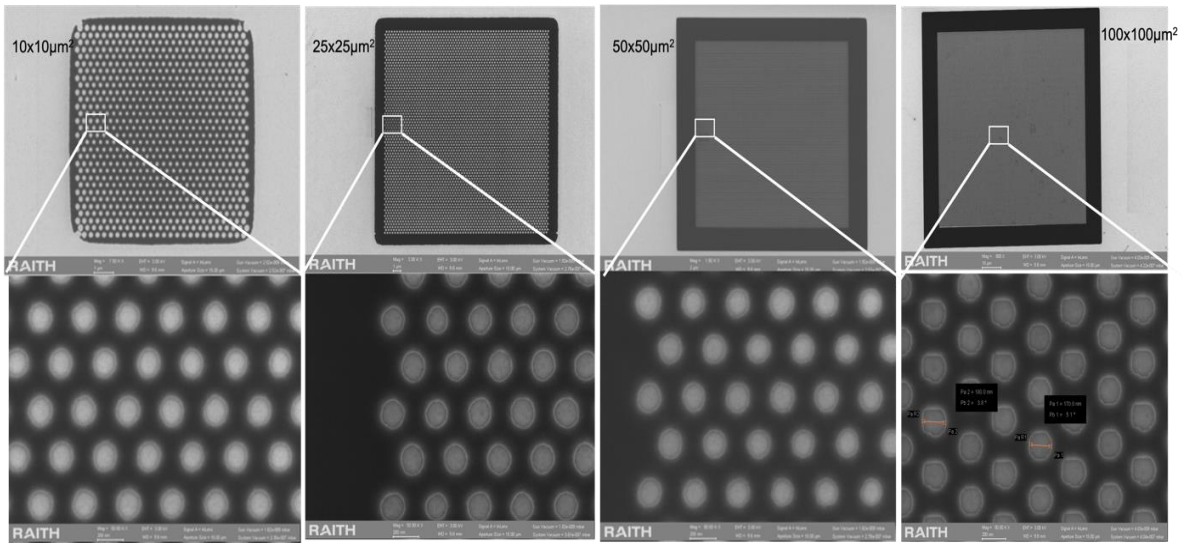

Figure 65 - SEM images of masks of the size: 10 x 10 μm^2, 25 x 25 μm^2, 50 x 50 μm^2 and 100 x 100 μm^2.

However, the growth of InGaN on this masks triggered a selectivity issue which seems to depend on two main parameters:

(i) The size of the mask.

(ii) The position of the mask in the 2-inches wafer.

Small masks of 10 x 10 μm^2 and 25 x 25 μm^2 are selective in all positions in the 2-inches wafer whereas larger masks of 50 x 50 μm^2 and 100 x 100 μm^2 are perfectly selective on the edges of the wafer, not selective near to the center and partially selective in between the center and the edges of the wafer, as illustrated by Figure 66.

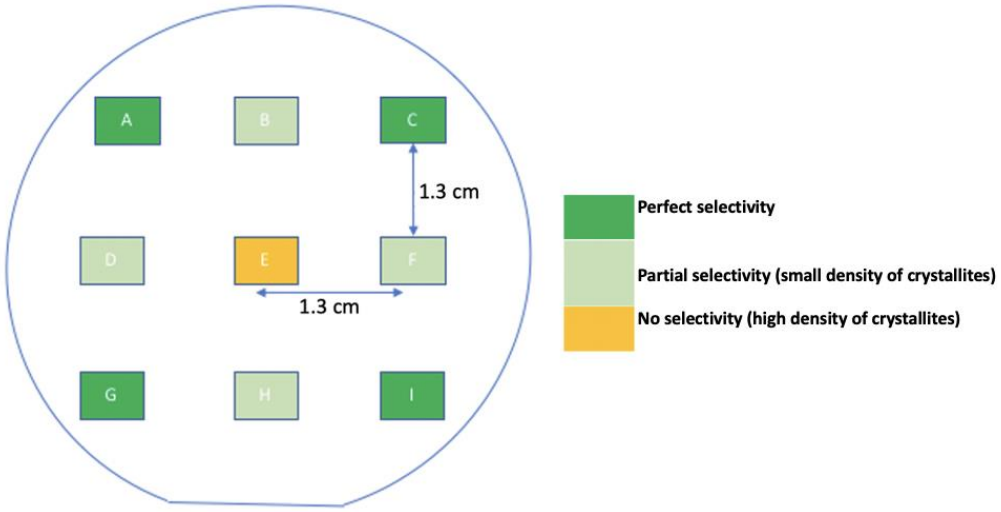

Figure 66 - A schema of a 2-inches wafer showing the dependence of selectivity on the mask position in the wafer for masks of size 50 x 50 μm^2 and 100 x 100 μm^2.

- **Optimization of the MOCVD Growth Conditions :**

An optimization flow chart was then launched. We first decided to add an *in situ* baking step under NH_3 at 1000°C and N_2 at 600°C. However, no improvement was observed on the selectivity of the mask in the center of the wafer as shown in Figure 67. Moreover, we also proceeded to a variation of the growth temperature. Three runs were launched at 815°C, 829°C and 840°C. Although we have less crystallites on the InGaN NPs at higher growth temperatures on 2-inches wafers, no perfect selectivity was obtained (Figure 68).

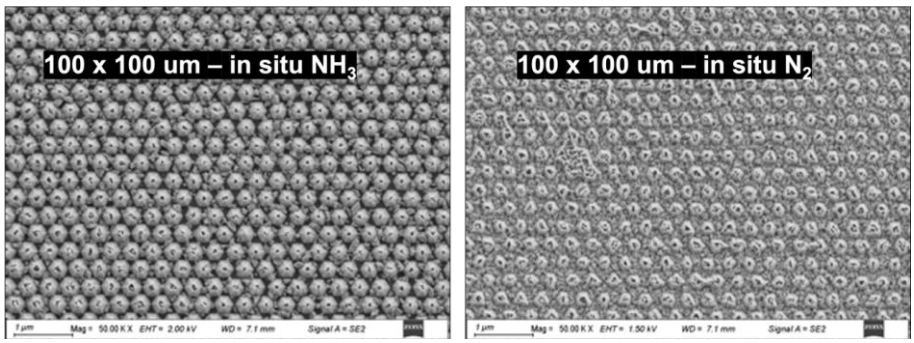

Figure 67 - InGaN growth of NPs on a 100 x 100 µm^2 mask after in situ NH_3 and after in situ N_2. High density of crystallites is observed.

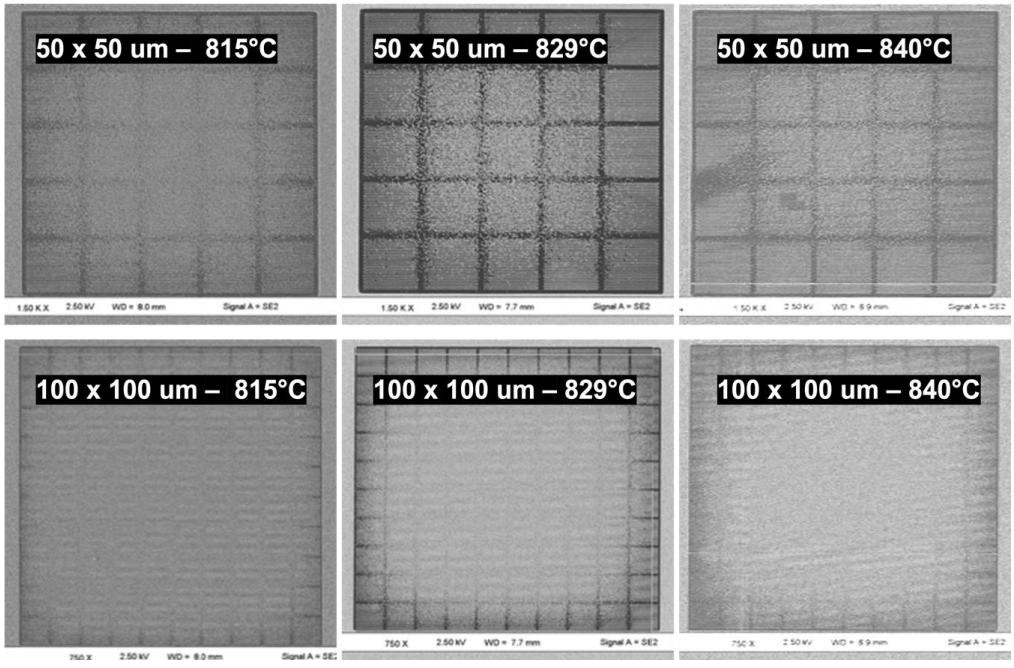

Figure 68 - InGaN growth of NPs on a 100 x 100 µm^2 by varying the growth temperature. High density of crystallites is observed.

Moreover, to reach a high indium incorporation in the NPs, growth must be proceeded at low temperature, thus, increasing the growth temperature higher than 840°C is not a relevant solution for our application. Therefore, we decided to focus on the optimization of the nanolithography mask.

- **Optimization of the Mask Fabrication Process :**

Concerning the mask fabrication process, a standard thickness of 100 nm of HSQ was used in the previous runs. A base dose of e-beam of 260 $\mu C/cm^2$ was considered to give the best resolution of nano-holes of around 150 nm. However, we hypothesized that at this base dose the cross-linking via Si-H bonds scission on HSQ was not efficient enough to produce an amorphous structure similar to SiO_2 allowing to achieve a perfect growth selectivity. To confirm this hypothesis, a Raman spectroscopy measurement was done on masks exposed to different doses, however, due to the low resolution of the measurement, no correlation between the Si-H stretching peak intensity and the base dose was observed. Energy Dispersive X-Ray Spectroscopy (EDX) is needed to achieve a higher resolution.

One solution to confirm the cross-linking hypothesis of the HSQ is to decrease the thickness of the mask. We fabricated masks of 77 nm (5500 rpm during the resist spin coating) instead of 100 nm (4000 rpm) and grew the InGaN NPs, but no improvement on the selectivity was observed as illustrated in Figure 69.

Further steps were based on post-baking the HSQ mask after the development by TMAH of the unexposed resist as suggested in Ref[132]. The mask was baked at 500°C for 1h under O_2 gas. This is supposed to dissociate the Si-H bonds and increase the number of Si-O bonds to achieve an SiO_2-like amorphous structure. However, the results of this

experiment were not as expected since after the InGaN NPs growth the density of crystallites on the mask was high, as shown in Figure 70.

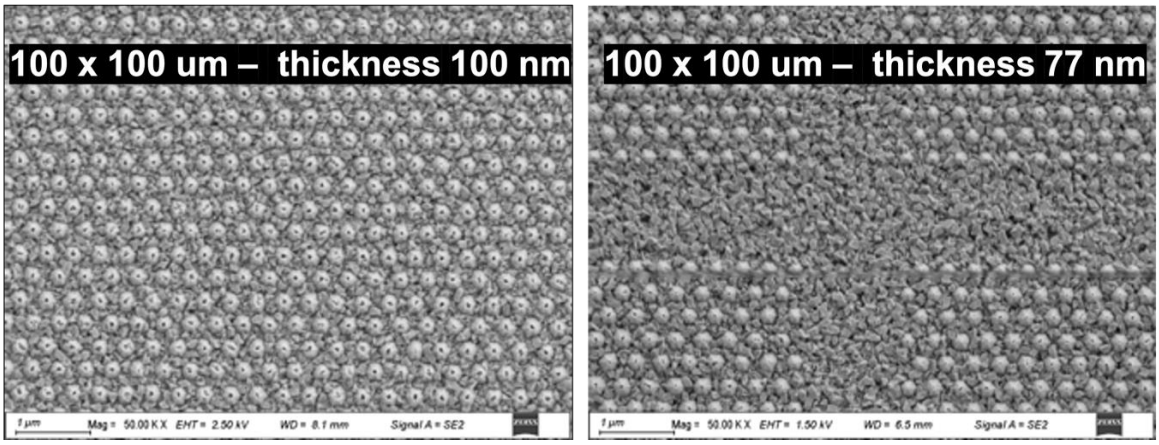

Figure 69 - InGaN growth of NPs on a 100 x 100 μm^2 masks with two different thicknesses100 nm and 77 nm. High density of crystallites is observed.

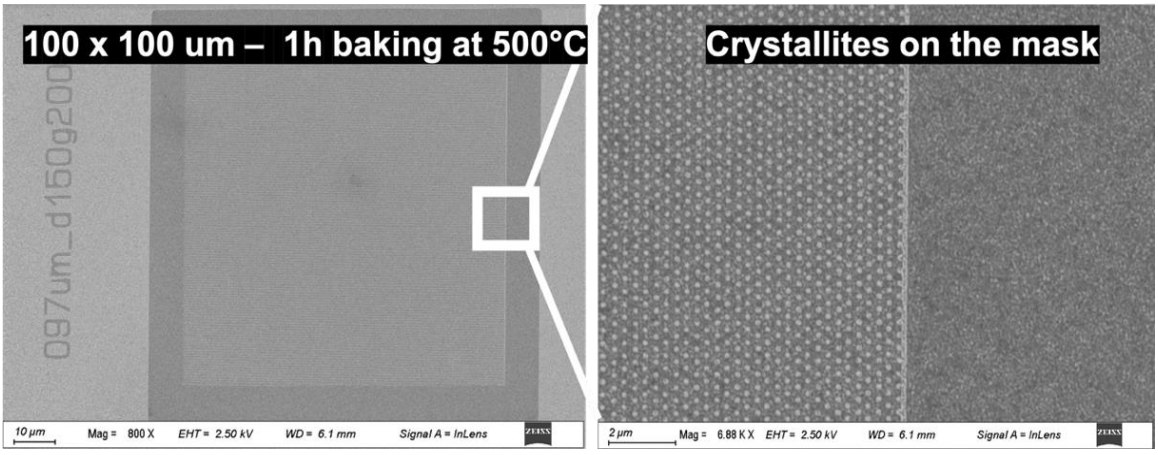

Figure 70 - InGaN growth of NPs on a 100 x 100 μm^2 mask baked for 1 hour at 500°C under O_2 . High density of crystallites is observed.

Subsequently, a post-exposure to UV was introduced. The UV exposure was done at 500 W (electrical power of the UV lamp) for various durations ranging from 15 minutes to 2 hours. In this experiment also, the results were inconclusive since after the InGaN NPs growth the density of crystallites on the mask was high (Figure 71).

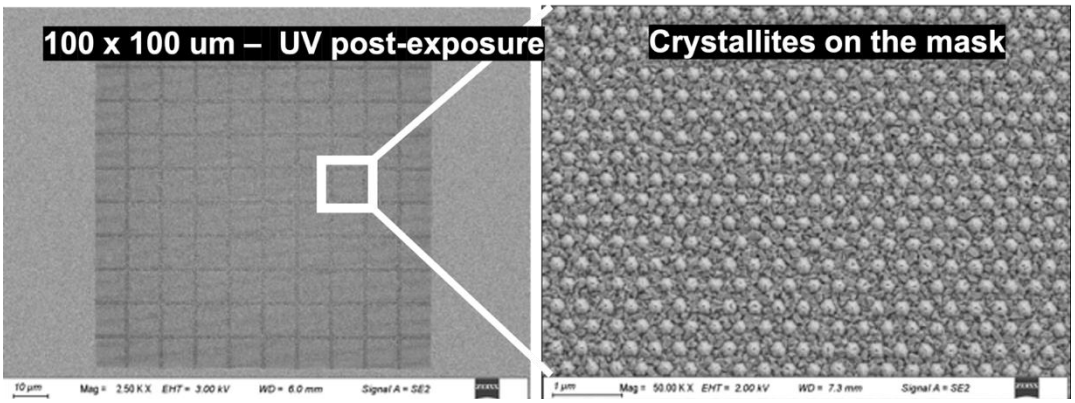

Figure 71 - InGaN growth of NPs on a 100 x 100 µm^2 mask exposed to UV irradiations after development of unexposed HSQ. High density of crystallites is observed.

The next step was to post-expose the HSQ mask to electrons beam in SEM imaging mode after the development by TMAH of the unexposed resist. The post-exposition was proceeded at a low acceleration voltage of 3kV with an aperture of 120 µm to maximize the e-beam current. Each 100 x 100 µm^2 mask was exposed for a duration ranging between 1 hour and 9 hours. The growth of InGaN NPs at 815°C was achieved afterwards, and we concluded that a post-exposure duration of 2 h 30 min was enough to have a perfect growth selectivity of InGaN NPs in the center of the wafer as shown in Figure 72.

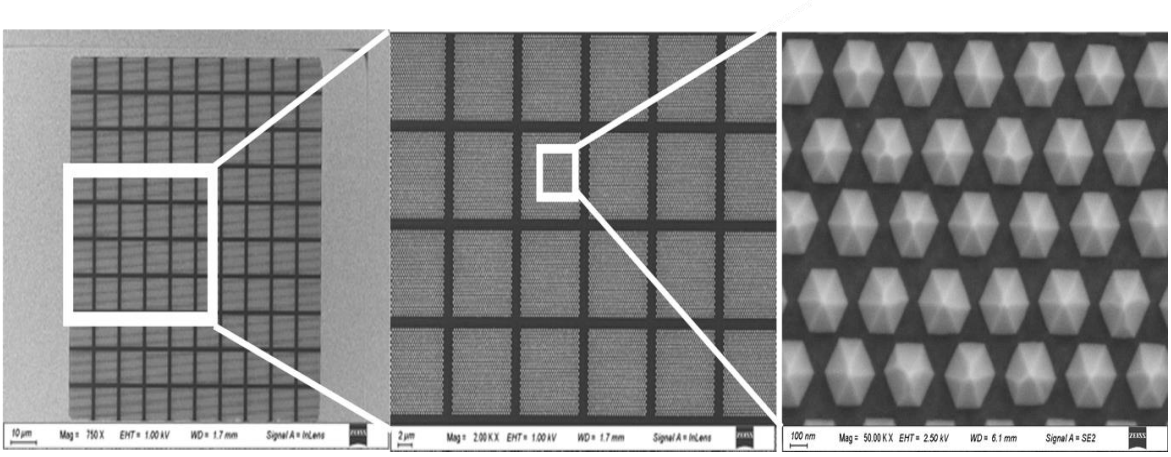

Figure 72 - InGaN growth of NPs on a 100 x 100 µm^2 mask exposed to an e-beam of 3 kV for 2 hours and 30 minutes. High selectivity of InGaN growth is observed.

The indium content in the NPs was estimated by cathodoluminescence (CL) spectra are shown in Figure 73 and CL mapping at 360 nm and 530 nm are illustrated in Figure 74.

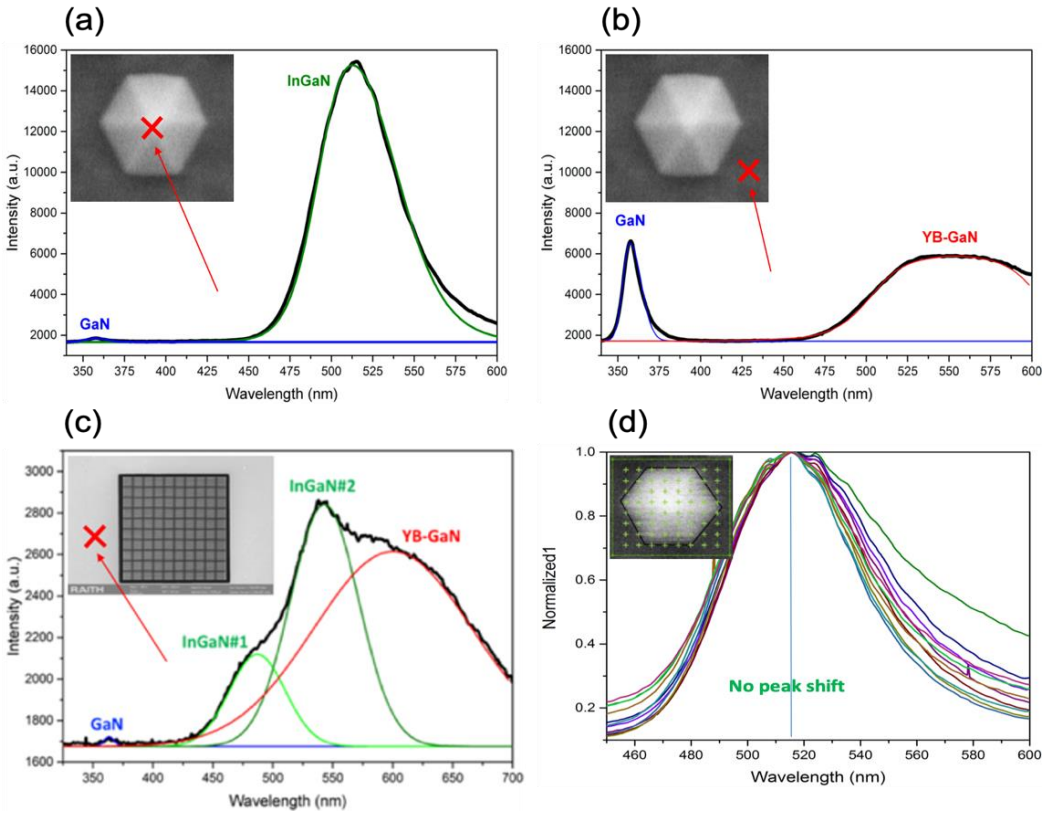

Figure 74 - Room temperature CL spectra of (a) a single InGaN NP, (b) HSQ-exposed region, (c) planar InGaN in the field, (d) mapping of different positions of the same NP.

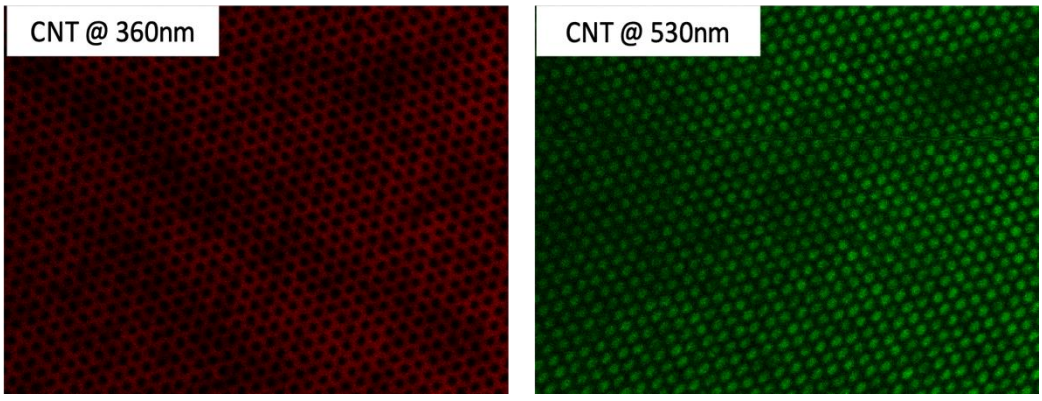

Figure 73 - CL monochromatic mappings of the InGaN NPs arrays.

The room temperature CL spectra from a single InGaN NP (Figure 73a) combined with the results of Orsal et al. [133] on the relaxation rate of InGaN and the associated bandgap bowing parameter confirmed that the In incorporation in the InGaN NPs is around 21%. The CL spectra in the nanolithography mask region (Figure 73b) shows only the peak of GaN underneath as well as the defect-related GaN emission because of the yellow luminescence of Ga vacancies. In the CL spectra of planar InGaN in the field (Figure 73c) we observe two peaks emission at 487 nm and 543 nm that should originate from the strained and relaxed InGaN sublayers, and it is found to be varied between 12% and 22% in the field which is due to phase separation in thick planar InGaN [134], [135]. This difference in the indium incorporation between the NPs and the field confirms the higher crystalline quality in the NPs compared to the planar InGaN. Finally, Figure 73d confirms the high homogeneity of indium incorporation in the pyramids since no peak shift is observed during the scanning measurement. Finally, Figure 74 shows CL monochromatic mappings of the InGaN NPs arrays. The 360 nm monochromatic CL mapping indicates that strong light emission of near band edge emission appears around the NP, and the bright region of 530 nm emission peak spreads all over the InGaN.

The p-type GaN layer on the NPs was optimized by adjusting temperature, precursor CP_2Mg flow rate and III/V ratio. We started by growing a 80 nm p-GaN planarization layer at 1000°C to cover the top of the pyramids. Then, a 150 nm thick p-type GaN with moderate Mg doping and a 50 nm contact layer with high Mg doping concentration were grown at 850°C. Figure 75 gives a top view of the whole PIN structure. We can see that the NPs are completely covered by the p-GaN layer, even if we have some hole defects on p-GaN due

relatively low temperature (850°C) of p-GaN regrowth. Using a higher temperature will deteriorate InGaN NPs underneath.

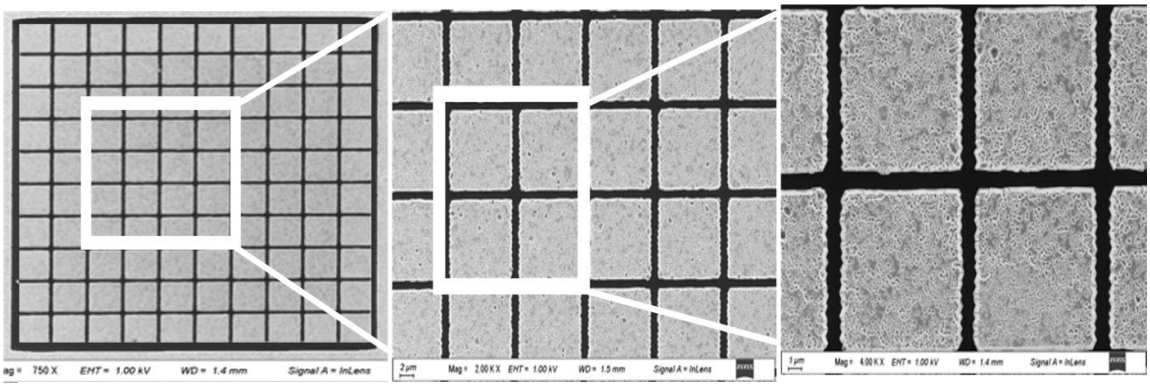

Figure 75 - Good coverage of InGaN NPs with p-GaN layer with perfect selectivity between the pixels.

However, the re-growth of p-type GaN layer was not reproducible over the runs. The hypothesis that has been put forward is a possible contamination of the mask by a hydrocarbon layer during the post-exposition step. SEM contamination patterns similar to the ones reported in literature was observed on our masks during multiple image scanning [136]. This contaminations can be deposited on the surface due to (a) oil in the vacuum pumps, (b) organic residue on the sample surface [128]. Moreover, the HSQ masks that were subject to post-exposition by electron beam were impossible to etch in the HF acid even by keeping them overnight in HF baths. This result confirmed, in some measure, the contamination hypothesis.

- **Mask contamination related to e-beam post-exposure:**

The next step was to apply a piranha etch to the HSQ-exposed mask after the perfectly selective growth of InGaN NPs. Piranha is a mixture of sulfuric acid (H_2SO_4), water, and hydrogen peroxide (H_2O_2), used to clean organic residues off substrates. The result of this experiment is illustrated in Figure 76 and showed that the whole HSQ-exposed mask is etched after an overnight bath of piranha, which was not the case when applying an HF etch. This unexpected result make us assume that the HSQ mask was not completely cross-linked after the nanolithography step, since a well cross-linked HSQ can be efficiently etched by HF acid [137].

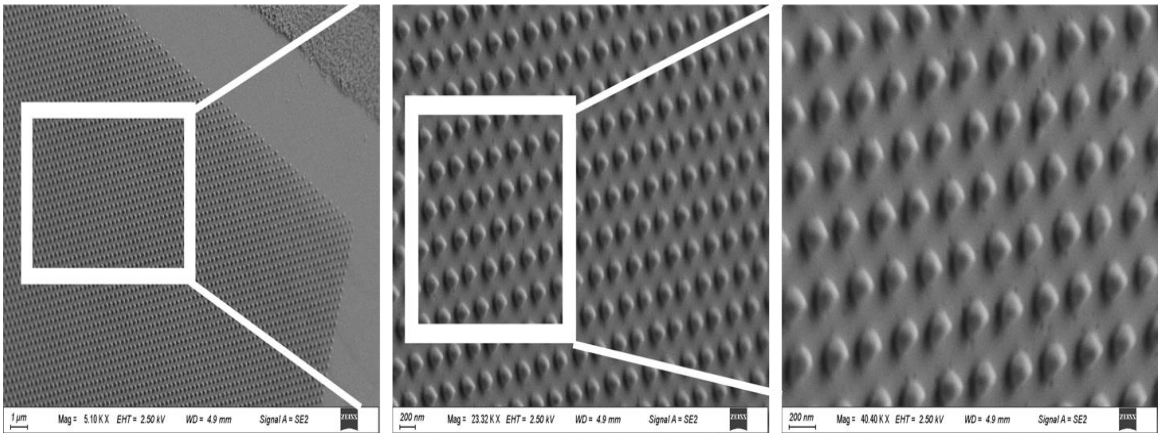

Figure 76 - SEM images of 100 x 100 µm^2. mask etched in a piranha bath. We can observe that the mask is completely etched.

After the growth of InGaN NPs and the complete etching of the HSQ-exposed mask, we proceeded to the p-type GaN regrowth. First, we started by growing a 80 nm p-GaN planarization layer at 1000°C to cover the top of the pyramids. The results are shown in Figure 77 using *Inlens* and *SE2* imaging detectors. Due to the high sensitivity to chemical compositions, the *Inlens* detector allows to observe the NPs underneath the p-type GaN top layer, whereas with *SE2* detector, the NPs we can only observe the top surface of p-GaN

due to its uniformly growth on InGaN. Subsequently, a 150 nm thick p-type GaN with moderate Mg doping and a 50 nm contact layer with high Mg doping concentration were grown at 850°C. The results are shown in Figure 78 using *Inlens* and *SE2* detectors. We observe a good coverage of the surface by p-GaN as well as some defects and v-pits on the surface related to the relatively low temperature growth of the p-type layer [102].

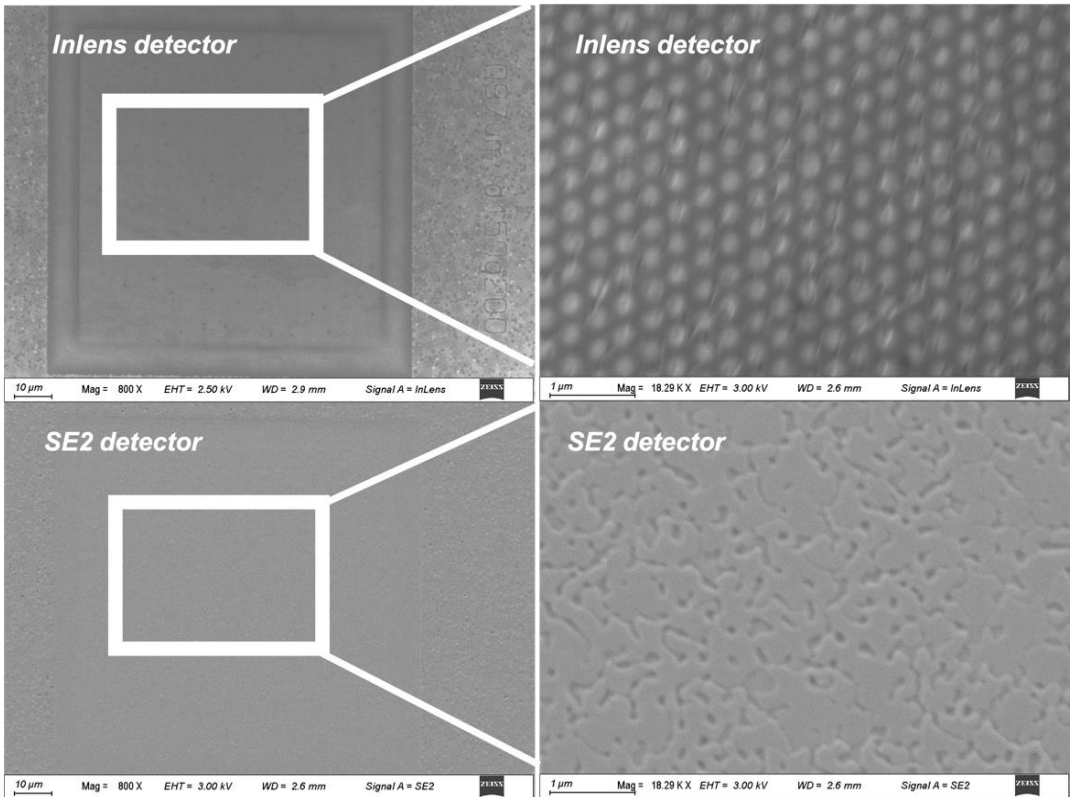

Figure 77 - SEM images (on the same mask) of the p-GaN planarization layer.

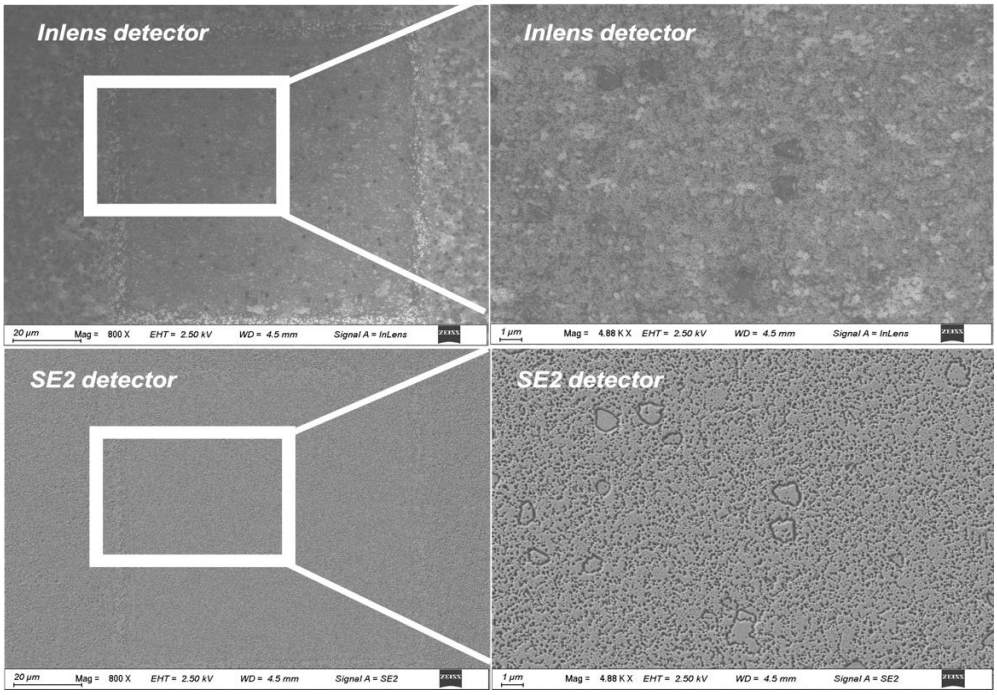

Figure 78 - SEM images (on the same mask) of the p-GaN top layer.

This concluding achievement of a complete solar cell structure paved the way to the fabrication of a first InGaN NP-based solar cell on sapphire. The next step to achieve high-efficiency transferrable InGaN solar cells is to realize a similar PIN structure on 2D h-BN/sapphire substrate. Thus, it could be possible to use the heterogeneous integration process based on mechanical lift-off of h-BN to fabrication InGaN solar cells that can be (i) transferred to flexible and rigid substrate (ii) integrated on top of a silicon solar cell to achieve a high efficiency III-N/silicon tandem cell and (iii) stacked on top of other NP-based solar cells with different indium incorporations to achieve multi-junction devices.

In this purpose, the same optimization process exposed in this section was conducted on an n-GaN/hBN/sapphire substrate. The results of this study are developed in the following section.

5.4.3 The Third Generation of the NP-based Solar Cells on 2D h-BN

To achieve HSQ-based masks for nano-selective area growth of InGaN NPs on n-GaN on h-BN/sapphire substrates, an optimization of the base dose of electrons beam as well as an adjustment of the conventional HSQ nanolithography process was needed. The growth h-BN layer (3 nm) was first grown on sapphire. Then, an intermediate n-AlGaN layer (300 nm) with an Al mole fraction of 14% was grown. This layer acts as an interfacial buffer between sp^3-bonded epitaxial films and 2D h-BN and promotes nucleation of n-type GaN. This templates introduce a processing challenge due to spontaneous delamination of 2D h-BN triggered by the originated mechanical strains. Surpass 3000 adhesion promoter and HSQ resist spin-coating step are done by minimizing exposure to liquids. The structures used and the nanolithography process flow is illustrated in Figure 79.

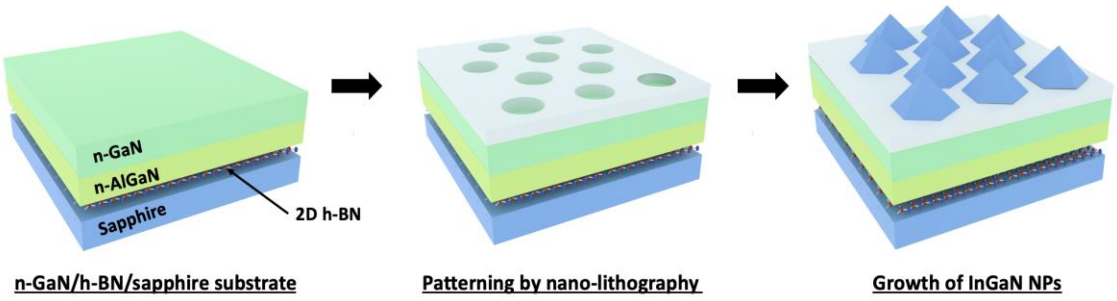

Figure 79 - Schematics of the process steps of InGaN solar cells on h-BN/sapphire.

The test dose was performed for a range between 120 μC/cm^2 and 190 μC/cm^2 and an optimized dose of 160 μC/cm^2 was obtained (Figure 80). This low value (compared to 260 μC/cm^2 used on a conventional n-GaN/sapphire template) can be explained by the higher electron scattering effect induced by n-GaN/n-AlGaN and n-AlGaN/hBN interfaces. The HSQ cross-linking reaction being mainly triggered by secondary electrons [130], lower dose of electrons beam is needed in this case.

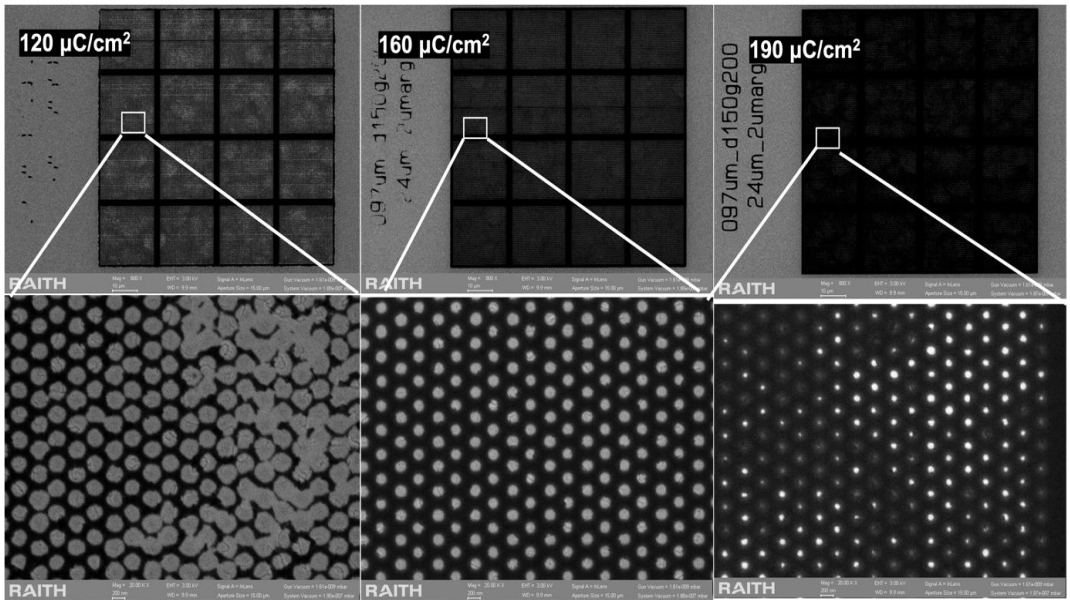

Figure 80 - HSQ masks with test doses of 120 µC/cm^2 (holes are too large), 160 µC/cm^2 (good holes of 150 nm) and 190 µC/cm^2 (holes small and not completely open). The optimized dose is 160 µC/cm^2 for holes of 150 nm diameter.

However, the homogeneity of the diameter of nano-holes between the center and the edge of the 2-inches wafer was challenging to obtain due to the growth inhomogeneities and the higher roughness of the n-GaN on n-AlGaN/h-BN/sapphire surface underneath compared to conventional n-GaN on sapphire as illustrated by AFM images of both templates (Figure 81). N-GaN-on-sapphire template has a roughness root-mean-square (RSM) of 0.3 nm whereas n-GaN-on-hBN template has a roughness RMS of 3.5 nm.

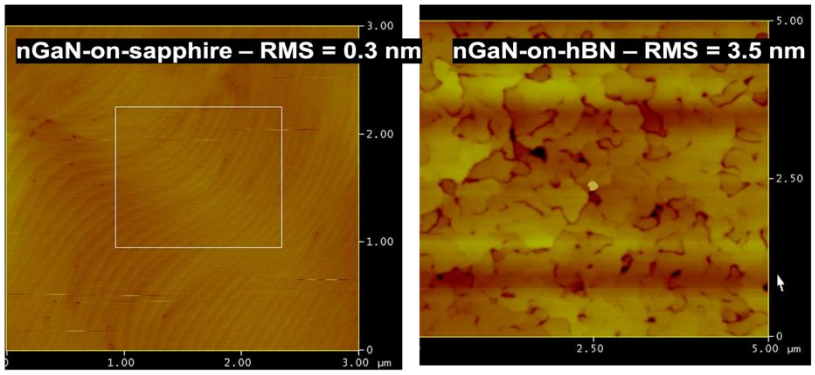

Figure 81 - AFM images of an nGaN-on-sapphire and an nGaN-on-hBN.

The next step was to post-expose the HSQ mask to electrons beam in SEM imaging mode after the development by TMAH of the unexposed resist. Different over-exposition durations was tried on different masks. The growth of InGaN nanopyramids at 815 °C was achieved afterwards, and we concluded that a post-exposure duration of 1 h 15 min was enough to have a perfect growth selectivity of InGaN nanopyramids shown in Figure 82, however, inhomogeneities in the NPs' size are observed and can be explained by the inhomogeneities in the holes' size mentioned above. No delamination of hBN was observed during the growth of InGaN NPs.

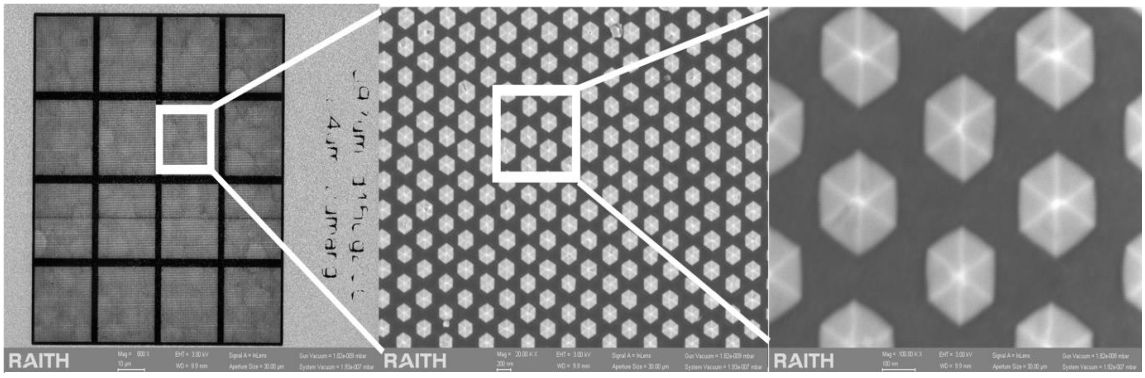

Figure 82 - Perfectly selective NSAG growth of InGaN NPs on nGaN on n-AlGaN/hBN.

Finally, to achieve a complete solar cell structure, the re-growth of p-type GaN layer was conducted but only partial coverage of the NPs by the p-GaN was obtained (Figure 83). This may be due to the possible contamination of the mask by a hydrocarbon layer during the post-exposition as discussed in the previous section. Removing the HSQ-exposed mask by piranha as it was done for nGaN-on-sapphire templates could help to have a homogeneous p-GaN regrowth. Work is in progress to optimize this step.

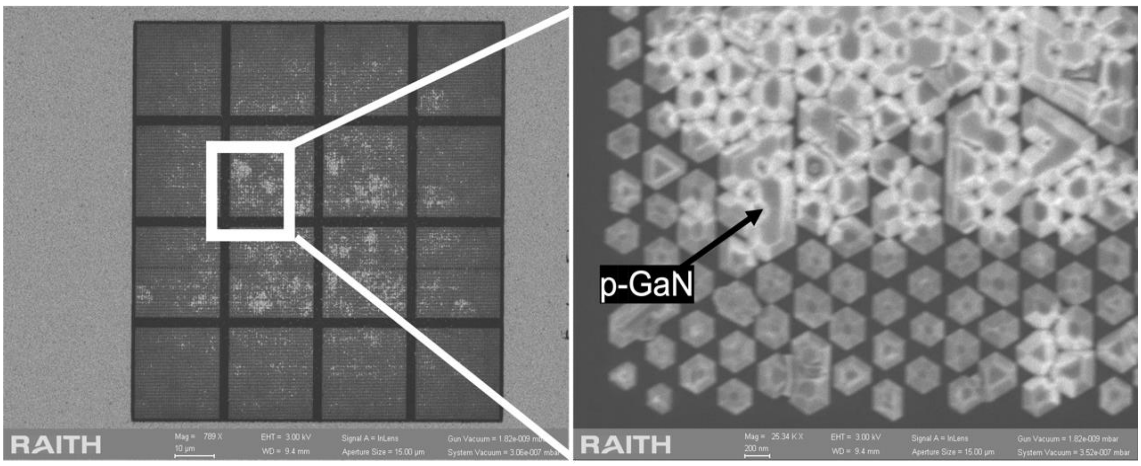

Figure 83 - SEM images after p-GaN regrowth. Only partial coverage of InGaN NPs is obtained.

After these encouraging growth results of NP-based InGaN solar cell structures on sapphire and h-BN/sapphire substrates, we focused on the fabrication process of these photovoltaic devices by optimizing the various technological blocks involved.

5.4.4 Solar Cells Fabrication Process

- **Optimization on MQW-based InGaN PIN structures**

To fabricate NP-based InGaN solar cells, a standard photolithography-based process was used. However, an optimization of different process steps was required to adapt the LED process described in Chapter 3 to the relatively small-size solar cells devices (around 100 x 100 μm). For this purpose, a conventional planar multi-quantum wells (MQWs) InGaN PIN structure was used. The mesa etching isolation is used in conjunction with a prior photolithography step and is achieved by inductively coupled plasma (ICP). Etching of GaN is accomplished using a Cl–based plasma with BCl_3/Cl_2/Ar chemistry. This step is carried out to remove p-GaN and InGaN layers from the regions that are exposed to the plasma.

Concerning electrical contacts, a transmission line measurement (TLM) was conducted to achieve a minimal contact resistance across metal-semiconductor interfaces. This step is preceded by a surface cleaning in HF acid to remove native oxides of GaN. For n-type contacts, Ti/Al/Ni/Au (20/200/25/25nm) are deposited by e-beam evaporation and annealed at 850 °C for 30 s under nitrogen. This optimized recipe allows to have an ohmic contact with a resistance of 5×10^{-6} ohm.cm^2, which corresponds to the state of the art of ohmic contacts on n-type GaN [138]. For p-type contact, Ni/Au (10/10nm) is also deposited by e-beam evaporation and annealed at 600 °C for 60s under an oxygen atmosphere. This thin layers of metals allow to have a continuous and partially transparent spreading layer with an ohmic behavior with a resistance of 1×10^{-2} ohm.cm^2. Finally, we added a p-pad of Ni/Au (20/100nm) on top for a better current collection.

The fabricated devices are then characterized as LEDs through current-voltage (I-V) measurements and electroluminescence (EL) to estimate the performances as well as the homogeneity of the process. All devices of the processed 2-inches wafers are tested by an automated probe station for a statistical process control. The I-V measurement of a 100 x 100 µm^2 processed device that indicates a leakage current at (-2V) of 10^{-11} A and a forward current (at 7V) of 100mA which corresponds to a current density of 1000 A/cm^2. The threshold voltage is between 3V and 4V. These values correspond to the state of the art of InGaN-based microLEDs [139]. Moreover, this process is well controlled and very homogeneous throughout the 2-inches wafer. More details on the photo-lithography mask and the equipment used is provided in Appendix B of this document.

- **Fabrication of NP-based InGaN solar cells structures**

After these optimizations, NP-based PIN devices were fabricated (Figure 84a and 84b). Light emission was observed during electroluminescence testing, however, the I-V curve was not corresponding to a good-quality PIN structure. This is mainly due to the quality of the p-GaN top layer which is partially covering the InGaN NPs. Therefore, during deposition and annealing of the p-contact, metals must be introduced between the pyramids and caused the high leakage current observed in Figure 84c. However, light emission was obtained for an applied voltage as high as 20 V (Figure 84d).

More optimization of the p-GaN growth is needed to achieve a high-quality NP-based InGaN solar cells with this technology.

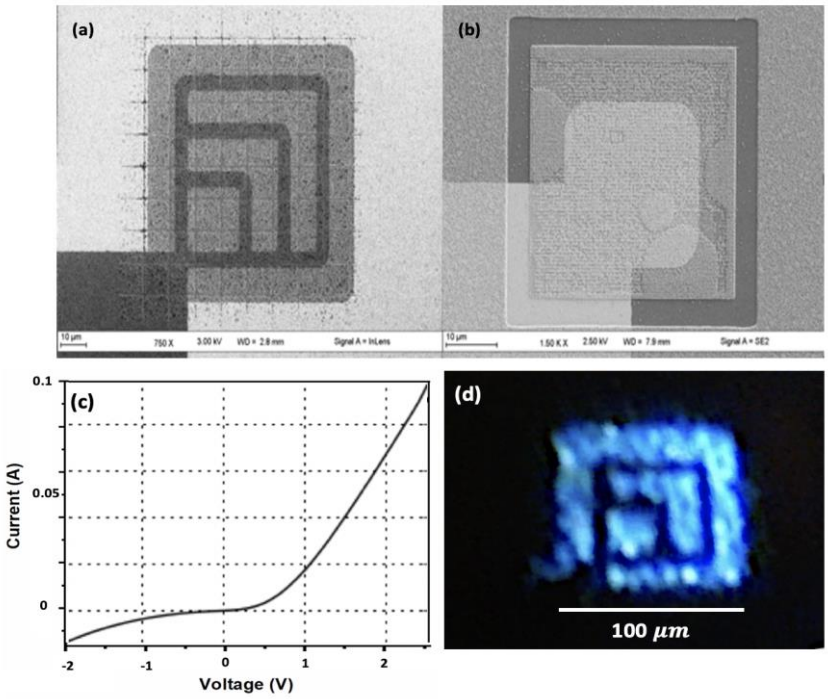

Figure 84 - SEM images of processed InGaN nanopyramid-based solar cell structures. (a) 100 x 100 μm^2 device with arrays of 10 x 10 μm^2 (b) 100 x 100 μm^2 device with no arrays.

5.5 Summary and Perspectives

The results presented for the InGaN NPs on sapphire and h-BN/sapphire templates in this chapter show that this approach can be an effective method for achieving high-efficiency InGaN-based photovoltaic devices. This new technique allows to grow high-quality InGaN absorbers with high indium content. Moreover, we have investigated, through simulation, the performances of InGaN NP-based solar cells with 30% indium content. When compared to planar InGaN solar cells, the NP-based solar cells show that the semi-polar growth planes lead to less polarization charges in the InGaN/GaN interface, which allows to handle ten times less acceptors concentration in the p-GaN top layer while maintaining the same performances. Furthermore, the SiO_2 mask used in the NP-based structure showed a light trapping effect in the SiO_2/InGaN interface, leading to a higher optical absorption and thus efficiency. Therefore, for an equivalent absorber volume, NP-based solar cells can lead to an efficiency (10.8 %) twice higher than planar InGaN solar cells. Accordingly, we have optimized the fabrication process steps of these NP-based structures by the use of a conventional MQWs-based InGaN structure through the same photo-lithography mask.

However, challenges remain for the regrowth of high-quality and uniform p-GaN layers on the NPs. By MOCVD, the low temperature (850°C) regrowth of p-GaN results in a high density of v-pits and defects that cause a high leakage current in the fabricated devices. Using a higher temperature deteriorates InGaN NPs underneath. Therefore, low-temperature molecular beam epitaxy (MBE) of the p-GaN could be a solution. Moreover, this technique allows high doping levels while preventing the problems of hydrogen passivation, polarity inversion domains and self-passivation that appear in the case of MOCVD growth[140] . Therefore, layers with high Mg (p-type dopant) concentration can

be achieved without significant degradation of the material quality [141], [142]. The combination of MOCVD and MBE techniques to overcome the problems associated to p-doping has proven successful for the fabrication of high efficiency LEDs [143] and we proposed to export such an approach for the demonstration of high-performance InGaN-based solar cells. For that, several wafers for p-GaN regrowth by MBE are currently under study. Besides the high p-doping that can result from this approach, MBE regrowth on NPs could result in conformal deposition of the p-GaN layers (Figure 85), which could reduce the top surface reflection and thus increase the light trapping in the absorber layer. Optical and electrical simulations are also in progress to investigate these effects.

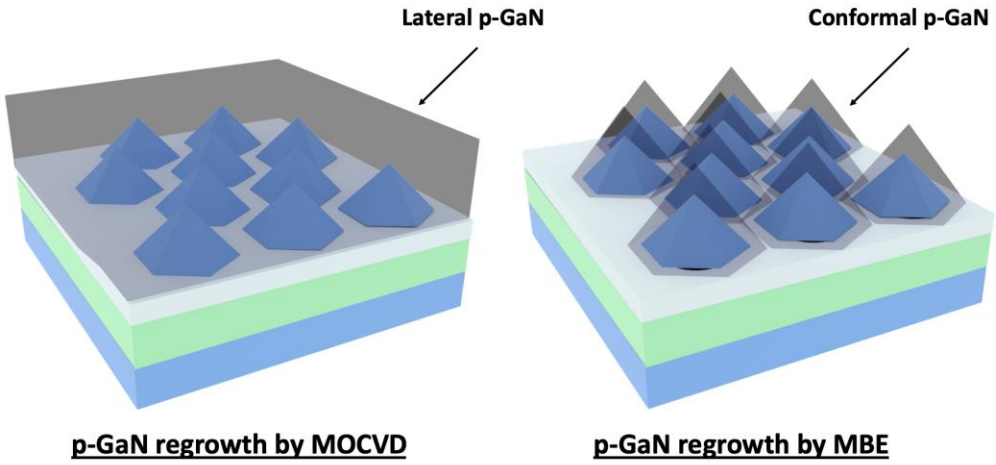

Figure 85 - Schematics of lateral and conformal p-GaN regrowth by MOCVD and MBE.

In addition, the successful growth of InGaN NPs on h-BN/sapphire templates could also pave the way for achieving flexible high-efficiency InGaN-based photovoltaic devices by transferring these devices from the h-BN/sapphire native substrate to a flexible substrate of interest as shown in Figure 86.

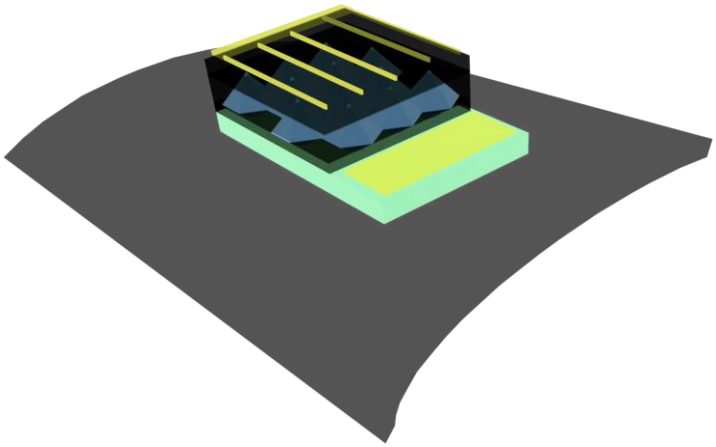

Figure 86 - Schematic of a NP-based InGaN solar cell transferred to a flexible substrate.

Moreover, the nano-selective area growth (NSAG) of InGaN NPs could also be combined to the innovative techniques presented in Chapter 4 and demonstrated for LED structures. For example, the NPs structures on h-BN/sapphire could benefit from the improvement of the crystalline quality of the n-GaN/n-AlGaN buffer layer by a reduction of the threading dislocation density and thus enhancing the efficiency. Besides, this combination will allow the simple pick-and-place crack-free transfer of devices for heterogeneous integration of these devices on silicon or glass with a back-reflector. The transferrable solar cells could also form a tandem cells by placing them on top of a silicon solar cell or InGaN multi-junctions by stacking solar cells with different indium incorporations. These configurations are schematically illustrated in Figure 87 and are also under study.

Finally, the SLOT process could also be used to achieve NP-based solar cells on copper through a one-step lift-off and transfer. This n-GaN-on-top structure could benefit from the high reflectivity and the flexibility of the metallic substrate as well as the possibility to form a bottom cell to which a pGaN-on-top NP-based cell could be transferred (Figure 88).

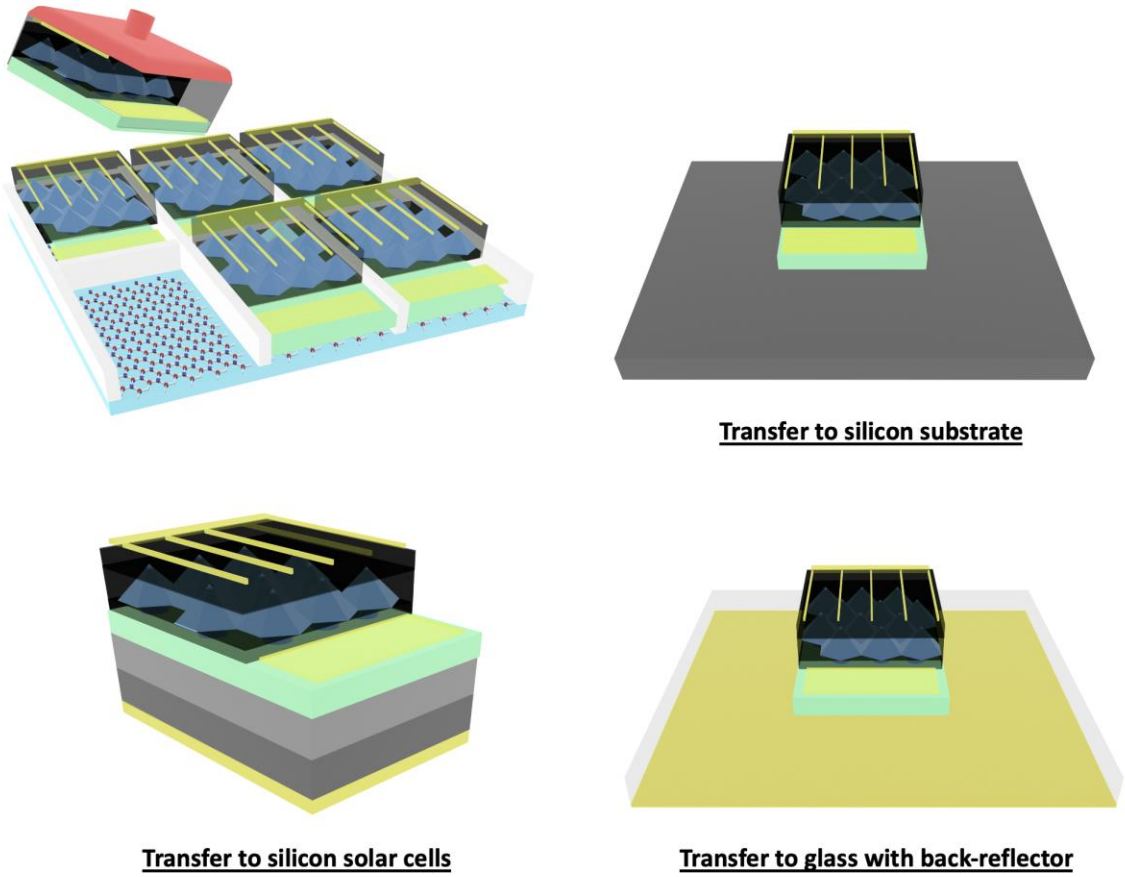

Figure 88 - Schematics illustrating the possibility of combining the NSAG and SAVWE approaches for efficient transfer of the solar cells to various substrates.

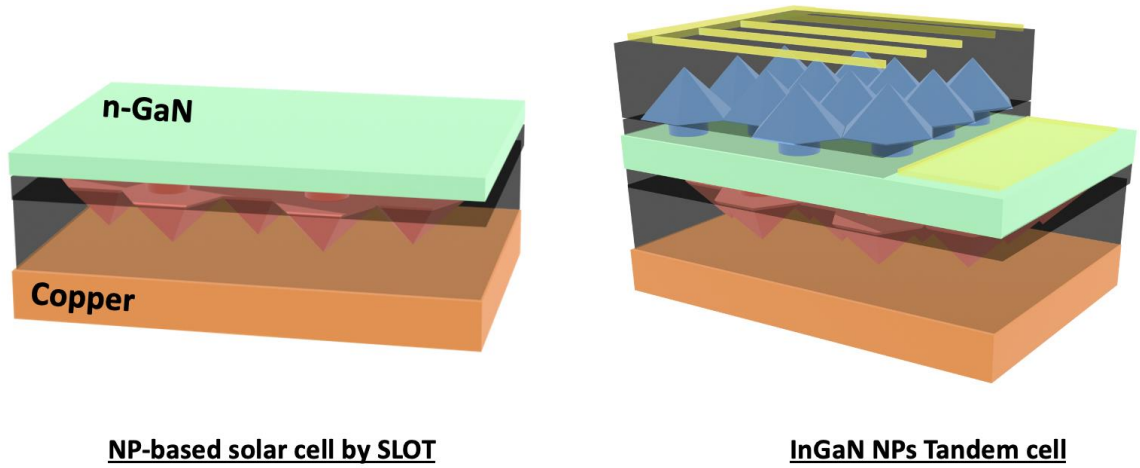

Figure 87 - Schematics illustrating the possibility of combining the NSAG and SLOT process for achieving free-standing and tandem NP-based solar cells on copper.

CHAPTER 6. CONCLUSION AND PERSPECTIVES

6.1 Conclusion

The goal of this thesis is to develop efficient, large-scale and low-cost new processes for heterogeneous integration of III-Nitride optoelectronic devices onto arbitrary rigid and flexible substrates. These processes developed were used to fabricate lateral and vertical InGaN-based LEDs as well as nanopyramid-based InGaN solar cells grown on 2D h-BN.

First, we introduced a novel fabrication method called selective area van der Waals epitaxy (SAVWE) and investigated its capability to limit delamination and cracks in the 2-inches wafer and to enable a reliable pick-and-place of selected lateral LED devices. Then, we underwent a side-by-side comparison of lateral LEDs grown on layered h-BN with and without SAVWE. We proved that the SAVWE of III-Nitrides coupled with the h-BN based mechanical lift-off and transfer lead to an overall improvement of the crystalline quality of the active layers by a reduction of the threading dislocation density and thus an enhancement of the electrical and optical device performances. In addition, transfer onto silicon and silica substrate through an efficient and robust liquid capillary van der Waals bonding (without the use of an intermediary adhesive layer) was demonstrated while the yield of the transfer of large-size crack-free devices on host substrates was three times higher when using SAVWE.

Moreover, we introduced another innovative process called thermo-mechanical self-lift-off and transfer (SLOT) for an efficient fabrication of large-area crack-free free-standing III-N membranes. Using this process, we demonstrated the fabrication of efficient vertical thin-film (VTF) InGaN light emitting diodes. This approach can provide a solution

for the fabrication of low cost, wafer scale, crack-free, and highly reproducible free-standing arrays of vertical LEDs with up to centimeter-size areas.

Finally**,** we proposed to use the 2D-h-BN assisted mechanical lift-off and transfer for the heterogeneous integration of solar cells to rigid and flexible substrates. We especially focused on InGaN-based solar cells by combining the van der Waals epitaxy of III-nitrides with the newly demonstrated nano-selective area growth of high-quality and high-indium-content InGaN nanopyramids (NPs). We performed optical and electrical simulations of the NP-based InGaN structures and proved that they can lead to an efficiency twice higher than planar InGaN solar cells. Then, we demonstate a first successful growth of the NPs InGaN structures on h-BN sapphire.

6.2 Perspectives

The perspectives of this work covers further improvements of the epitaxial growth and device fabrication, as well as the new process ideas that could arise from the combination of the different technological blocks presented in this thesis.

- **Optimization of the AlGaN buffer layer for lateral LEDs on h-BN :**

For the III-N epilayers grown on 2D h-BN, an optimization of the material quality of the AlGaN buffer layer could lead to a significant decrease in the density of threading dislocations that propagates to the InGaN MQWs. Theoretically, the vdWs epitaxy of 3D III-Nitrides on 2D h-BN should lead to defect-free epilayers owing to the absence of dangling bonds at the substrate/epilayers interface. Thus, this optimization could allow to

reach electro-optical performances of LEDs comparable or higher than conventional LEDs grown on sapphire, without the need of a thick low-temperature GaN buffer.

- **SAVWE process for micro-LEDs :**

In the context of this thesis, we demonstrated through the SAVWE process the fabrication and pick-and-place of 1 x 1 mm^2 LEDs. However, this approach could also be used for micro-LEDs and could allow an efficient assembly and integration method for micro-LED displays. Work is under progress to demonstrate this technology for LEDs as small as 50 x 50 μm^2.

- **SLOT process by etching the AlGaN buffer layer :**

As discussed in Chapter 4, the performance of the VTF-LEDs achieved by the SLOT process were limited by the n-AlGaN buffer layer on the n-contact side. An efficient etch of the this layer on the free-standing membranes could enhance performances of this VTF-LEDs by decreasing the electrical series resistance as well as enhancing the ligth extraction efficiency by modifying the optical cavity length as predicted by the simulations performed. This process step is currently under study.

- **SLOT process for TFFC-LEDs and VCSELs :**

The SLOT process also opens new ways for the fabrication of thin-film flip-chip (TFFC) LEDs where both contacts are placed on the backside of the LED. Such a configuration allows for higher light-extraction (no metal is deposited on the emitting side and there is no requirement of wire-bonding to access the n-contact). TFFC-LEDs can be achieved

through the SLOT process, by introducing additional process steps while the LED structure in still on the h-BN/sapphire native substrate.

Vertical-cavity surface-emitting lasers could also be fabricated via the SLOT process by depositing the dielectric mirrors on both sides of the epilayers. The first mirror can be deposited while the epilayers as still on the h-BN/sapphire native substrate whereas the second mirror can be deposited on the released surface of the free-standing membrane.

- **Combining SAVWE and SLOT processes :**

The two processes developed in this thesis could also be combined to achieve isolated vertical LEDs by growing the device structures selectively, depositing the thick copper layer and releasing the free-standing membranes. This combination can result in higher electro-optical performances of the LEDs by decreasing the leakage current due to the physical isolation of each single LED.

- **MBE p-GaN regrowth for NPs InGaN solar cells :**

For NPs InGaN solar cells, challenges remain for the regrowth of high-quality and uniform p-GaN layers. By MOCVD, the low temperature regrowth of p-GaN results in a high density of v-pits and defects that cause a high leakage current in the fabricated devices. Using a higher temperature deteriorates InGaN NPs underneath. Therefore, low-temperature molecular beam epitaxy (MBE) of the p-GaN could be a solution. Moreover, this technique allows high doping levels while preventing the problems of hydrogen passivation. For that, several wafers for p-GaN regrowth by MBE are currently under study.

Besides, MBE regrowth on NPs could result in conformal deposition of the p-GaN layers, which could reduce the top surface reflection and thus increase the light trapping in the absorber layer. Optical and electrical simulations are also in progress to investigate these effects.

- **Combining InGaN NPs and SLOT process :**

The SLOT process could also be used to achieve NP-based solar cells on copper through a one-step lift-off and transfer. This n-GaN-on-top structure could benefit from the high reflectivity and the flexibility of the metallic substrate as well as the possibility to form a bottom cell to which a pGaN-on-top NP-based cell could be transferred, to achieve a tandem double-junction InGaN photovoltaic device.

6.3 Publications

1. **S. Karrakchou**, S. Sundaram, R. Gujrati, P. Vuong, A. Mballo, Hibat E.Adjmi, V. Ottapilakkal, W. El Huni, K. Bouzid, G. Patriarche, A. Ahaitouf, P. L. Voss, J-P. Salvestrini & A. Ougazzaden , "Monolithic Free-Standing Large-Area Vertical III-N Light Emitting Diode Arrays by One-Step h-BN-based Thermo-Mechanical Self-Lift-Off and Transfer," *ACS Appl. Electron. Mater.*, 2021.
2. **S. Karrakchou,** S. Sundaram, T. Ayari, A. Mballo, P. Vuong, A. Srivastava, R. Gujrati, A. Ahaitouf, G. Patriarche, T. Leichlé, S. Gautier, T. Moudakir, P. L. Voss, J-P. Salvestrini & A. Ougazzaden, "Effectiveness of selective area growth using van der Waals h - BN layer for crack - free transfer of large - size III - N devices onto arbitrary substrates," *Sci. Rep.*, pp. 1–9, 2020.

3. W. El Huni, **S. Karrakchou**, Y. Halfaya, M. Arif, M.B. Jordan, R. Puybaret, T. Ayari, C. Bishop, S. Gautier, A. Ahaitouf, P. L. Voss, J-P. Salvestrini & A. Ougazzaden , "Nanopyramid-based absorber to boost the efficiency of InGaN solar cells," *Sol. Energy*, vol. 190, 2019.
4. Mballo A, Srivastava A, Sundaram S, Vuong P, **Karrakchou S**, Halfaya Y, Gautier S, Voss PL, Ahaitouf A, Salvestrini JP, Ougazzaden A. Towards P-Type Conduction in Hexagonal Boron Nitride: Doping Study and Electrical Measurements Analysis of hBN/AlGaN Heterojunctions. *Nanomaterials*. 2021; 11(1):211.
5. S. Sundaram, P. Vuong, A. Mballo, T. Ayari, **S. Karrakchou**, G. Patriarche, P. L. Voss, J-P. Salvestrini & A. Ougazzaden, "MOVPE of GaN-based mixed dimensional heterostructures on wafer-scale layered 2D hexagonal boron nitride—A key enabler of III-nitride flexible optoelectronics" APL Materials 9, 061101, (2021).
6. T. Ayari, S. Sundaram, C. Bishop, A. Mballo, P. Vuong, Y.Halfaya, **S. Karrakchou**, S. Gautier, P. L. Voss, J-P. Salvestrini & A. Ougazzaden , "Novel Scalable Transfer Approach for Discrete III-Nitride Devices Using Wafer-Scale Patterned h-BN/Sapphire Substrate for Pick-and-Place Applications," *Adv. Mater. Technol.*, vol. 4, no. 10, p. 1900164, Oct. 2019.
7. P. Vuong, A. Mballo, S. Sundaram, G. Patriarche, Y. Halfaya, **S. Karrakchou**, A. Srivastava, K. Krishnan, N. Y. Sama, T. Ayari, S. Gautier, P. L. Voss, J. P. Salvestrini, *and* A. Ougazzaden , "Single crystalline boron rich B(Al)N alloys grown by MOVPE", Applied Physics Letters 116, 042101 (2020).
8. P. Vuong, S. Sundaram, A. Mballo, G. Patriarche, S. Leon, F. Benkhelifa, **S. Karrakchou**, T. Moudakir , S. Gautier, P. L. Voss, J. P. Salvestrini, *and* A.

Ougazzaden , “Control of the Mechanical Adhesion of III–V Materials Grown on Layered h-BN”, ACS Applied Materials & Interfaces, 12, 49, 55460-55466 (2020).

9. N. Y. Sama, A. Hathcock, D. He, P. Vuong, **S. Karrakchou**, T. Ayari, A. Mballo, C. Bishop, Y. Halfaya, H. Bouhnane, S. Gautier, A. Ahaitouf, J-M Matray, J-P. Salvestrini & A. Ougazzaden , "Investigation of Sc_2O_3 Based All-Solid-State EIS Structure for AlGaN/GaN HEMT pH Sensor," *2019 IEEE SENSORS*, 2019, pp. 1-4.

APPENDIX A. III-NITRIDES FUNDAMENTALS

A.1 Properties and Growth

The III-Nitrides are wide bandgap semiconductors that enabled a revolution in modern electronic and optoelectronic applications in the few last decades, resulted in demonstration of blue, green, red, and white LEDs, blue and green laser diodes (LDs) and even more, high electron-mobility transistors (HEMTs) for sensors and power electronics, solar cells and photodetectors [144]. One advantage of III-N alloys including binary, ternaries, and quaternaries of (B, Al, Ga, In) N is their wide bandgap ranging from 0.65 eV to 6.05 eV. Except BN which is still under investigation, all other ternary and binary alloys have direct bandgap that make them the suitable for light-emitting applications. III-N semiconductors can cover a large spectral range from the near infrared to the deep ultraviolet, including the entire visible spectrum (Figure 89).

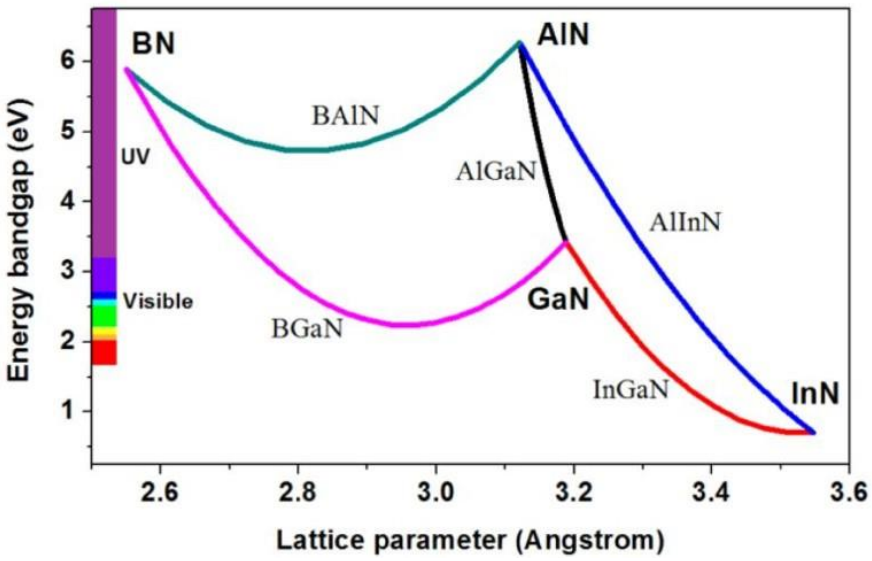

Figure 89 - Bandgap energies of different III-Nitrides and their alloys showing the suitability of light-emission from infrared to ultraviolet spectra .

III-Nitrides also display high chemical, mechanical, and thermal stabilities, high thermal conductivities, high carrier saturation drift velocities, and high radiation hardness, making devices suitable for harsh environment and long lifetime applications.

III-N semiconductors crystallize into two different structures: hexagonal wurtzite and cubic zincblende, among which the hexagonal wurtzite structure is thermodynamically stable for bulk III-Nitrides. In this thesis, the crystal structure of all the samples was of hexagonal wurtzite type. Such a crystal structure has a hexagonal unit cell and therefore is described by the lattice constants a (in- plane) and c (out-of-plane) as shown in Figure 90. Nitrogen atoms are forming a hexagonal close packed structure and group III atoms occupying half of the tetrahedral sites available in the lattices. Since there is a large disparity of electro-negativity between III-group elements and nitrogen atoms with small atomic radius, the III-group elements and nitrogen are bound by strong covalent bonds. Typical crystal orientations and planes of wurtzite III-Nitrides are illustrated in Figure 90 and Figure 91, respectively. The lattice parameters and thermal properties of the III-N binary alloys are given in Table 3. The {0001} plane is called the *c*-plane, the {1–100} plane is the *m*-plane, the {11–20} plane is the *a*-plane, and the {1–102} plane is the *r*-plane

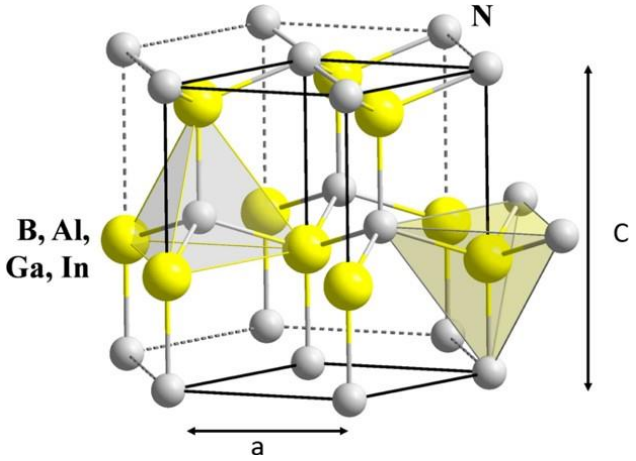

Figure 90 - Wurtzite crystalline structure of III-Nitrides

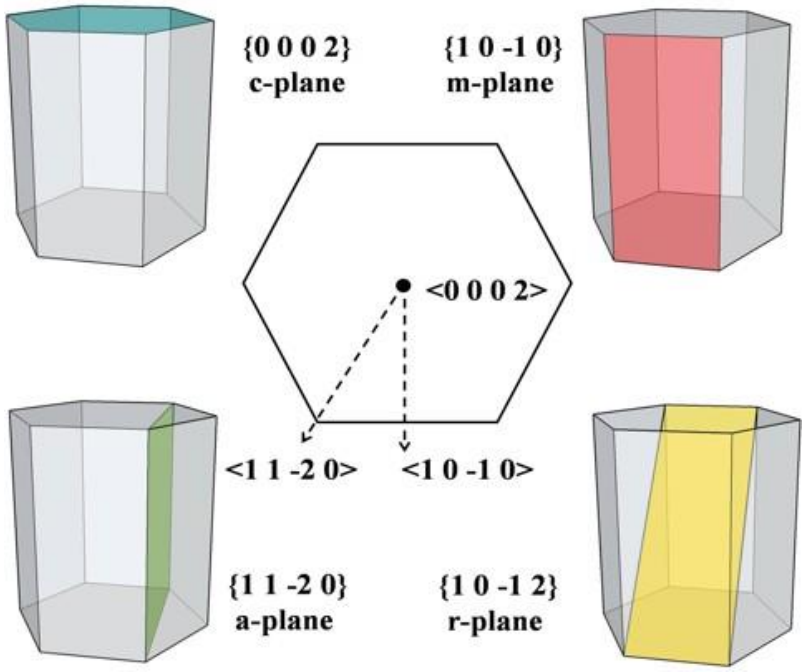

Figure 91 - Typical crystal orientations and planes of wurtzite III-Nitrides.

Table 6 - Lattice parameters, bandgap and thermal expansion coefficients of III-N binary alloys [145]–[147].

Material	In-plane lattice parameter (a)	Out-of-plane lattice parameter (c)	Bandgap at 300 K	Thermal expansion coefficient x 10^{-6} K	
				$\boldsymbol{\Delta a/a}$	$\boldsymbol{\Delta c/c}$
GaN	3.19 Å	5.19 Å	3.42 eV	5.6	3.17
InN	3.54 Å	5.70 Å	0.65 eV	2.85	2.9
AlN	3.10 Å	4.97 Å	6.2 eV	4.2	5.27
BN	2.55 Å	4.17 Å	5.9 eV	-2.7	38

The lattice parameters of the ternary alloys can be obtained from Vegard's law [148]:

$$a,c(A_xB_{1-x}N) = a,c(AN) \times\ x +\ a,c(BN) \times (\,1-x)$$

where x is the indium composition and (a, c) are the lattice parameters of the $A_xB_{1-x}N$ alloy.

Homogeneous epitaxy of III-N materials allows to achieve high-crystalline quality layers but usually requires expensive substrates, while heterogeneous epitaxy is limited by the lattice and thermal expansion coefficients mismatch between the epilayers and the growth substrate, which generates a high-density of defects and dislocations in the epilayers. These defects and dislocations results from the in-place strain that can be compressive or tensile. If the lattice parameter of the epilayer is larger than the lattice parameter of the substrate the strain is compressive, whereas it is tensile if lattice parameter of the epilayer is smaller than the lattice parameter of the substrate.

- **Spontaneous and Piezoelectric Polarizations**

Due to the lack of a center of inversion symmetry, the wurtzite structure of nitride materials are subject to polarization. In this type of structures, geometrical centers of the positive and negative charges are not at the same position, causing a polarity of the charges. This polarity depends on the direction of growth and the first element deposited. Taking GaN grown along the c-axis [0001] direction as an example, if the first element is nitrogen (N),

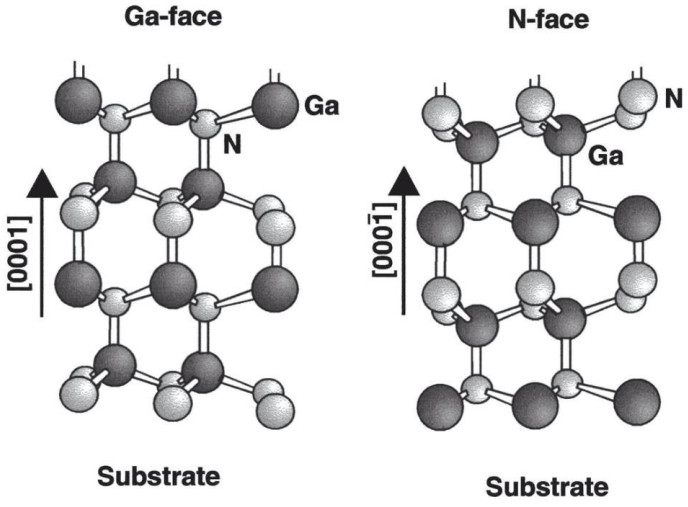

Figure 92 - Schematics of Ga-face and N-face polarity[149].

the last atomic layer will be gallium (Ga), which results in a polarity called Ga-face or metal-face. Otherwise, an N-face polarity is obtained. Schematics of these two configurations are given in Figure 92 [149]. The epitaxial growth of GaN on the sapphire substrate along the c-axis direction is a relatively mature method and results a high-crystalline quality. The most studied group III-N semiconductor devices are based on the *c*-plane Ga-polar face. In order to reduce the effect of the polarization on the performance of the device, nitride devices built on non-polar surfaces such as *a*- and *m*-plane or semi-polar *r*-plane have also been studied. Although there are still many difficulties in the quality of epitaxial crystals, many studies have reported the high-performance devices on non-polar or semi-polar crystal planes, where the performance of the devices is close to that built on polar materials [150].

The spontaneous polarization has a nonlinear dependence on the material composition and can be obtained for from the following formula:

$$P_{sp}(A_x B_{1-x} N) = x\ P_{sp}(AN) + (1-x)\, P_{sp}(BN) + b\ x\ (1-x)$$

where x is the indium composition, b is the bowing parameter [150].

In addition to the spontaneous polarization, III-N materials are also subject to a piezoelectric polarization induced by the tensile or compressive stress that modifies the atomic positions and the charge distribution in the epilayers. Polarization charges will appear at the interface of the layers and are related to the strain ε of the epilayer, expressed as the ratio between the lattice constants of the substrate and the epilayers, to the lattice constant of the substrate [150] :

$$\varepsilon = (a_{\text{subs}} - a_L) / a_L$$

The piezoelectric polarization of AlN, GaN, and InN are:

$$P_{pz}\text{AlN} = \begin{cases} -1.808\varepsilon + 5.624\varepsilon^2 \varepsilon < 0 \\ -1.808\varepsilon - 7.888\varepsilon^2 \varepsilon > 0 \end{cases}$$

$$P_{pz}(\text{GaN}) = 0.918\varepsilon + 9.541\varepsilon^2$$

$$P_{pz}(\text{InN}) = -1.373\varepsilon + 7.559\varepsilon^2$$

where P_{pz} is the piezoelectric polarization in [C/m^2]. The sum of the spontaneous and piezoelectric polarizations is the net polarization P_T.

$$P_T = P_{sp} + P_{pz}$$

- **Electron Band Structure**

In the energy band theory, the problem can be described and analyzed more clearly using the inverted lattice and the Brillouin zone of the wurtzite structure of the III-N materials is shown in Figure 93 where k_x, k_y, and k_z are three coordinate axes orthogonal to each other in the inverted lattice [151]. GaN, AlN, and InN are direct band gap semiconductor materials and are suitable as luminescent materials. In addition, the second energy valley M-L valley and the third energy valley A valley are also found in the energy band. Due to the action of the crystal field and the spin-orbit coupling, the valence band splits into a heavy hole band, a light hole band, and a spin-coupled split band.

The dependence of the energy bandgap for the wurtzite III-N semiconductors on temperature is given by:

$$E_g(T) = E_g(0) - \frac{\alpha T^2}{T + \beta}(\text{eV})$$

where $E_g(T)$ represents the band gap width when the temperature is T, $E_g(0)$ is the band gap at zero Kelvin, and α and β are the Varshni thermal coefficients.

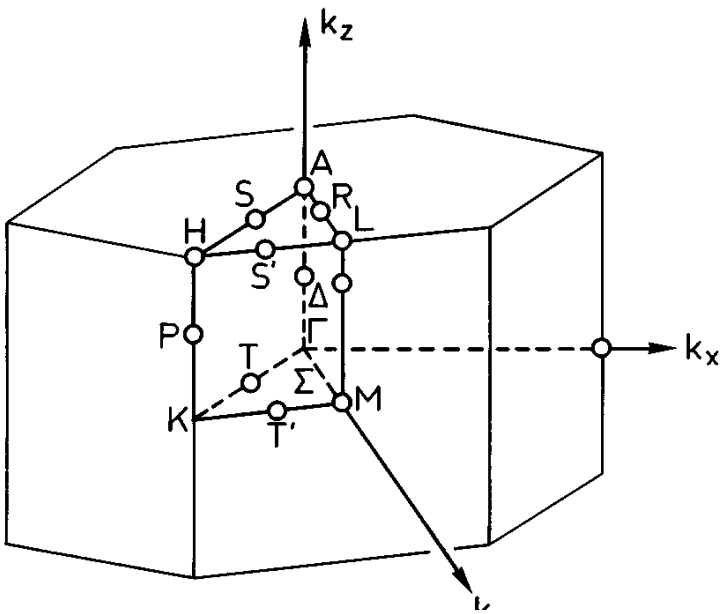

Figure 93 - The first Brillouin zone of the wurtzite crystal structure [150].

The energy bandgap for III-N unstrained ternary alloys can be calculated with simple Vegards law as following :

$$E_g(A_x B_{1-x} N) = x\ E_g(AN) + (1-x)\, E_g(BN) - b\ x\ (1-x)$$

where x is the indium composition, b is the bowing parameter [150].

Materials with different compositions and strain have different bowing parameters that are empirically calculated.

A.2 Growth of III-Nitride Materials

III-Nitrides can be grown by several techniques including molecular beam epitaxy (MBE), hydride vapor phase epitaxy (HVPE) and metalorganic chemical vapor deposition (MOCVD - also referred as metalorganic vapor-phase epitaxy (MOVPE) -.

In the MBE method, the material vapor under ultra-high vacuum conditions. The material beams are directly sprayed onto a substrate and controlled to scan the substrate. The slow growth rate allowed by this technique facilitates the precise control of thickness while the low growth temperature reduces the thermal expansion mismatch between the epilayers and the substrate. Moreover, MBE is a dynamic process of growing one-by-one atoms or molecules and not a thermodynamic and mass transfer process, thus it allows to grow films that are difficult to grow according to ordinary thermal equilibrium growth methods [150].

On the other hand, MOCVD includes thermodynamics, hydrodynamics, mass transport, and kinetics. It is a chemical vapor deposition technology widely used in compound optoelectronic devices and microelectronics devices. It involves the gas-phase transport of (1) organometallic precursors (trimethylaluminum (TMAl), trimethylgallium (TMG), cyclopentadienyl magnesium (Cp2Mg)) and associated carrier gases for the successful transport of the vapors of these liquid and solid sources into the reactor chamber, (2) hydrides containing nitrogen, and (3) diluent gases including H_2 and N_2 that prevent pyrolysis of the precursors in the gas phase prior to reaching a heated substrate on which occurs decomposition of the reactants, reaction of the products of the decomposition, and growth of the desired film [152]. The schematic of III-Nitride epitaxial growth is illustrated in Figure 94 [153].

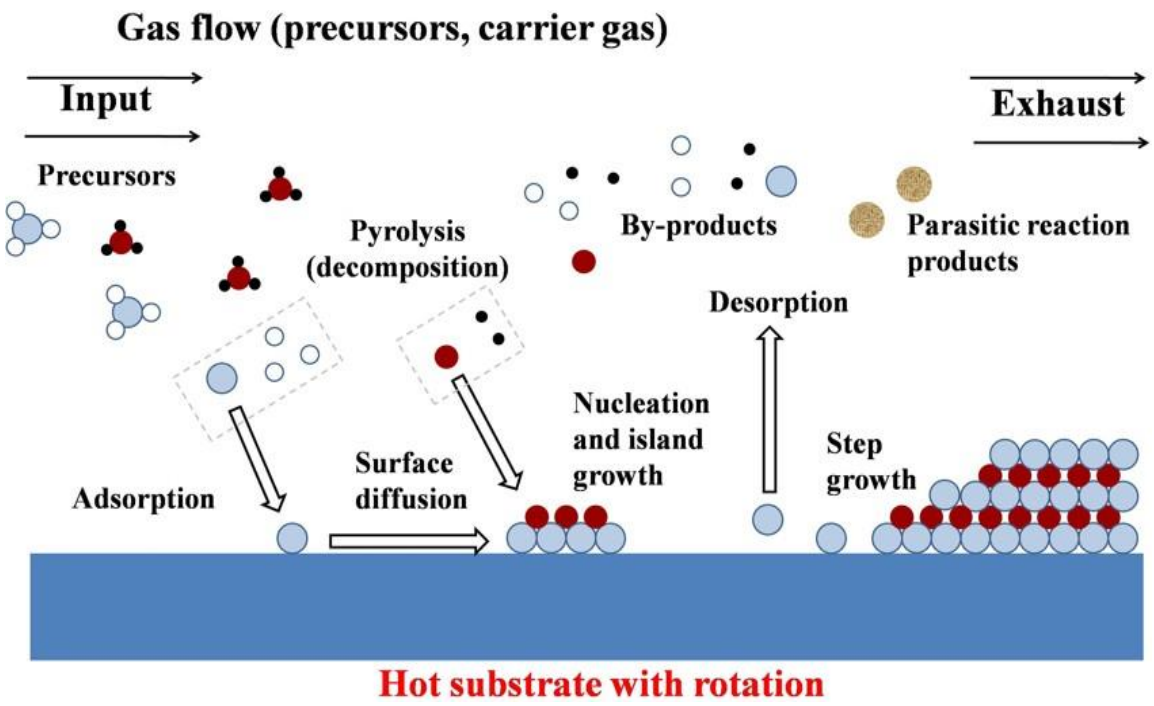

Figure 94 - Schematic illustration of III-Nitrides MOCVD growth [153].

The MOCVD process can be summarized by the following steps [150]:

- Metal-organics such as TMGa and TMIn are transported into the reaction chamber through carrier gases such as N_2 or H_2;
- The mixed source gas is transported on the surface of the heated substrate and thermally decomposed;
- Atoms from the chemical reaction are adsorbed on the surface of the substrate;
- The reacting atomic cluster migrates to the nucleation site to form a stable physical adsorption;
- The by-product of the surface reaction leaves the surface of the substrate and is pumped to the exhaust gas treatment system;

The growth rate and the quality of the epilayers depend on temperature, pressure, V/III ratio (the ratio of NH_3 flow rate to the total flow rate of III and V precursors) and choice of the carrier gases. Compare to MBE, MOCVD technique (i) doesn't need a high vacuum, (ii) it allows a high growth rate, (iii) scalable for large-scale production.

It has been commercialized on a large scale for industry and research by AIXTRON and VEECO. These two companies monopolize the world 90% market [150]. All the h-BN-based and GaN-based MQWs LED structures presented in this thesis were grown on an AIXTRON Close-Coupled Showerhead (CCS) MOCVD reactor at IRL 2958 Georgia Tech-CNRS Laboratory whereas nanopyramid-based InGaN structures were grown on a custom-made T-shape MOCVD available in the same laboratory.

REFERENCES

[1] H. Kum *et al.*, “Epitaxial growth and layer-transfer techniques for heterogeneous integration of materials for electronic and photonic devices,” *Nat. Electron.*, vol. 2, no. 10, pp. 439–450, 2019.

[2] S. W. Bedell, K. Fogel, P. Lauro, D. Shahrjerdi, J. A. Ott, and D. Sadana, “Layer transfer by controlled spalling,” *J. Phys. D. Appl. Phys.*, vol. 46, no. 15, p. 152002, 2013.

[3] M. Chen, B. P. Zhang, L. E. Cai, J. Y. Zhang, L. Y. Ying, and X. Q. Lv, “Auto-Split Laser Lift-Off Technique for Vertical-Injection GaN-Based Green Light-Emitting Diodes,” *IEEE Photonics J.*, vol. 5, no. 4, p. 8400407, 2013.

[4] A. Rajan *et al.*, “Wafer-scale epitaxial lift-off of optoelectronic grade GaN from a GaN substrate using a sacrificial ZnO interlayer,” *J. Phys. D. Appl. Phys.*, vol. 49, no. 31, p. 315105, 2016.

[5] J. Kim *et al.*, “Principle of direct van der Waals epitaxy of single-crystalline films on epitaxial graphene,” *Nat. Commun.*, vol. 5, pp. 1–7, 2014.

[6] Y. Kobayashi, K. Kumakura, T. Akasaka, and T. Makimoto, “Layered boron nitride as a release layer for mechanical transfer of GaN-based devices,” *Nature*, vol. 484, no. 7393, pp. 223–227, Apr. 2012.

[7] R. Dahal *et al.*, “Epitaxially grown semiconducting hexagonal boron nitride as a deep ultraviolet photonic material,” *Appl. Phys. Lett.*, vol. 98, no. 21, p. 211110,

May 2011.

[8] T. Ayari *et al.*, “Wafer-scale controlled exfoliation of metal organic vapor phase epitaxy grown InGaN/GaN multi quantum well structures using low-tack two-dimensional layered h-BN,” *Appl. Phys. Lett.*, vol. 108, no. 17, p. 171106, Apr. 2016.

[9] T. Ayari *et al.*, “Gas sensors boosted by two-dimensional h-BN enabled transfer on thin substrate foils: towards wearable and portable applications,” *Sci. Rep.*, vol. 7, no. 1, p. 15212, 2017.

[10] T. Makimoto, K. Kumakura, Y. Kobayashi, T. Akasaka, and H. Yamamoto, “A Vertical InGaN/GaN Light-Emitting Diode Fabricated on a Flexible Substrate by a Mechanical Transfer Method Using BN,” *Appl. Phys. Express*, vol. 5, no. 7, p. 72102, 2012.

[11] T. Ayari *et al.*, “Heterogeneous Integration of Thin-Film InGaN-Based Solar Cells on Foreign Substrates with Enhanced Performance,” *ACS Photonics*, vol. 5, no. 8, pp. 3003–3008, 2018.

[12] W. S. Wong, T. Sands, and N. W. Cheung, “Damage-free separation of GaN thin films from sapphire substrates,” *Appl. Phys. Lett.*, vol. 72, no. 5, pp. 599–601, 1998.

[13] K. Qiao *et al.*, “Graphene Buffer Layer on SiC as a Release Layer for High-Quality Freestanding Semiconductor Membranes,” *Nano Lett.*, vol. 21, no. 9, pp. 4013–4020, May 2021.

[14] X. L. Hu, Z. Y. Qi, H. Wang, and X. C. Zhang, “Performance of InGaN-based thin-film LEDs with flip-chip configuration and concavely patterned surface fabricated on electroplating metallic substrate,” *IEEE Photonics J.*, vol. 8, no. 1, pp. 1–8, 2016.

[15] E. Alarcón-Lladó *et al.*, “Temperature rise in InGaN/GaN vertical light emitting diode on copper transferred from silicon probed by Raman scattering,” *J. Appl. Phys.*, vol. 108, no. 11, 2010.

[16] H.-H. Hsueh, S.-L. Ou, D.-S. Wuu, and R.-H. Horng, “InGaN LED fabricated on Eco-GaN template with a Ga2O3 sacrificial layer for chemical lift-off application,” *Vacuum*, vol. 118, pp. 8–12, 2015.

[17] J. S. Ha *et al.*, “The fabrication of vertical light-emitting diodes using chemical lift-off process,” *IEEE Photonics Technol. Lett.*, vol. 20, no. 3, pp. 175–177, 2008.

[18] F.-L. Wu *et al.*, “Thin-film vertical-type AlGaInP LEDs fabricated by epitaxial lift-off process via the patterned design of Cu substrate,” *Opt. Express*, vol. 23, no. 14, p. 18156, 2015.

[19] J. J. Schermer *et al.*, “Epitaxial Lift-Off for large area thin film III/V devices,” *Phys. Status Solidi Appl. Mater. Sci.*, vol. 202, no. 4, pp. 501–508, 2005.

[20] K.-T. Shiu, J. Zimmerman, H. Wang, and S. R. Forrest, “Ultrathin film, high specific power InP solar cells on flexible plastic substrates,” *Appl. Phys. Lett.*, vol. 95, no. 22, p. 223503, Nov. 2009.

[21] C.-W. Cheng, K.-T. Shiu, N. Li, S.-J. Han, L. Shi, and D. K. Sadana, “Epitaxial lift-

off process for gallium arsenide substrate reuse and flexible electronics," *Nat. Commun.*, vol. 4, no. 1, p. 1577, 2013.

[22] C. Y. Cho *et al.*, "Growth and separation of high quality GaN epilayer from sapphire substrate by lateral epitaxial overgrowth and wet chemical etching," *Appl. Phys. Express*, vol. 4, no. 1, pp. 11–14, 2011.

[23] C. Youtsey *et al.*, "Wafer-scale epitaxial lift-off of GaN using bandgap-selective photoenhanced wet etching," *Phys. status solidi*, vol. 254, no. 8, p. 1600774, Aug. 2017.

[24] J. Park, K. M. Song, S.-R. Jeon, J. H. Baek, and S.-W. Ryu, "Doping selective lateral electrochemical etching of GaN for chemical lift-off," *Appl. Phys. Lett.*, vol. 94, no. 22, p. 221907, Jun. 2009.

[25] R. Delmdahl, C. L. Gmbh, and C. Kg, "Laser lift-off : reducing device heights in micro - electronics by means of substrate transfer," *Photonik Int.*, pp. 2–4, 2013.

[26] K. Xu, J.-F. Wang, and G.-Q. Ren, "Progress in bulk GaN growth," *Chinese Phys. B*, vol. 24, no. 6, p. 66105, 2015.

[27] Q. Wang, Y. Liu, Y. Sun, Y. Tong, and G. Zhang, "Fabrication of extremely thermal-stable GaN template on Mo substrate using double bonding and step annealing process," *J. Semicond.*, vol. 37, no. 8, p. 83001, 2016.

[28] S. Bornemann *et al.*, "Femtosecond Laser Lift-Off with Sub-Bandgap Excitation for Production of Free-Standing GaN Light-Emitting Diode Chips," *Adv. Eng. Mater.*,

vol. 22, no. 2, p. 1901192, Feb. 2020.

[29] N. Yulianto *et al.*, "Ultrashort Pulse Laser Lift-Off Processing of InGaN/GaN Light-Emitting Diode Chips," *ACS Appl. Electron. Mater.*, vol. 3, no. 2, pp. 778–788, Feb. 2021.

[30] C. Gerhard and M. Stappenbeck, "Impact of the Polishing Suspension Concentration on Laser Damage of Classically Manufactured and Plasma Post-Processed Zinc Crown Glass Surfaces," *Applied Sciences* , vol. 8, no. 9. 2018.

[31] Z. Gong, "Layer-scale and chip-scale transfer techniques for functional devices and systems: A review," *Nanomaterials*, vol. 11, no. 4, pp. 1–41, 2021.

[32] F. Dross *et al.*, "Stress-induced large-area lift-off of crystalline Si films," *Appl. Phys. A*, vol. 89, no. 1, pp. 149–152, 2007.

[33] D. Shahrjerdi *et al.*, "Ultralight High-Efficiency Flexible InGaP/(In)GaAs Tandem Solar Cells on Plastic," *Adv. Energy Mater.*, vol. 3, no. 5, pp. 566–571, May 2013.

[34] S. W. Bedell *et al.*, "Vertical Light-Emitting Diode Fabrication by Controlled Spalling," *Appl. Phys. Express*, vol. 6, no. 11, p. 112301, 2013.

[35] P. Zhu and N. Tansu, "Resonant cavity effect optimization of III-nitride thin-film flip-chip light-emitting diodes with microsphere arrays," *Appl. Opt.*, vol. 54, no. 20, pp. 6305–6312, 2015.

[36] S. W. Bedell *et al.*, "Kerf-Less Removal of Si, Ge, and III–V Layers by Controlled Spalling to Enable Low-Cost PV Technologies," *IEEE J. Photovoltaics*, vol. 2, no.

2, pp. 141–147, 2012.

[37] Z. Suo and J. W. Hutchinson, “Steady-state cracking in brittle substrates beneath adherent films,” *Int. J. Solids Struct.*, vol. 25, no. 11, pp. 1337–1353, 1989.

[38] S. W. Bedell, P. Lauro, J. A. Ott, K. Fogel, and D. K. Sadana, “Layer transfer of bulk gallium nitride by controlled spalling,” *J. Appl. Phys.*, vol. 122, no. 2, p. 25103, Jul. 2017.

[39] T. Ayari *et al.*, “Wafer-scale controlled exfoliation of metal organic vapor phase epitaxy grown InGaN/GaN multi quantum well structures using low-tack two-dimensional layered h-BN,” *Appl. Phys. Lett.*, vol. 108, no. 17, 2016.

[40] N. R. Glavin *et al.*, “Flexible Gallium Nitride for High-Performance, Strainable Radio-Frequency Devices,” *Adv. Mater.*, vol. 29, no. 47, 2017.

[41] M. J. Motala *et al.*, “Transferrable AlGaN/GaN High-Electron Mobility Transistors to Arbitrary Substrates via a Two-Dimensional Boron Nitride Release Layer,” *ACS Appl. Mater. Interfaces*, vol. 12, no. 19, pp. 21837–21844, 2020.

[42] A. E. Del Rio Castillo, A. Ansaldo, V. Pellegrini, and F. Bonaccorso, “Exfoliation of layered materials by wet-jet milling techniques,” Patent, WO2017089987A1, 2016.

[43] D. Chugh, J. Wong-Leung, L. Li, M. Lysevych, H. H. Tan, and C. Jagadish, “Flow modulation epitaxy of hexagonal boron nitride,” *2D Mater.*, vol. 5, no. 4, 2018.

[44] J. Narayan, “Recent progress in thin film epitaxy across the misfit scale (2011 Acta

Gold Medal Paper)," *Acta Mater.*, vol. 61, no. 8, pp. 2703–2724, 2013.

[45] R. Y. Tay, Chemical Vapor Deposition Growth and Characterization of Two-Dimensional Hexagonal Boron Nitride. Springer, ISBN 978-981-10-8809-4, 2018.

[46] A. K. Geim and I. V Grigorieva, "Van der Waals heterostructures.," *Nature*, vol. 499, no. 7459, pp. 419–425, Jul. 2013.

[47] C. R. Dean *et al.*, "Boron nitride substrates for high-quality graphene electronics.," *Nat. Nanotechnol.*, vol. 5, no. 10, pp. 722–726, Oct. 2010.

[48] L. Wang *et al.*, "Growth and Etching of Monolayer Hexagonal Boron Nitride," *Adv. Mater.*, vol. 27, no. 33, pp. 4858–4864, Sep. 2015.

[49] Z. Zuo, Z. Xu, R. Zheng, A. Khanaki, J.-G. Zheng, and J. Liu, "In-situ epitaxial growth of graphene/h-BN van der Waals heterostructures by molecular beam epitaxy," *Sci. Rep.*, vol. 5, no. 1, p. 14760, 2015.

[50] H. Sediri et al., "Atomically Sharp Interface in an h-BN-epitaxial graphene van der Waals Heterostructure," Scientific reports, vol. 5., p. 16465, 2015.

[51] S. Majety *et al.*, "Hexagonal boron nitride and 6H-SiC heterostructures," *Appl. Phys. Lett.*, vol. 102, no. 21, p. 213505, May 2013.

[52] X. Z. Du, J. Li, J. Y. Lin, and H. X. Jiang, "The origin of deep-level impurity transitions in hexagonal boron nitride," *Appl. Phys. Lett.*, vol. 106, no. 2, p. 21110, Jan. 2015.

[53] X. Li *et al.*, "Large-Area Two-Dimensional Layered Hexagonal Boron Nitride

Grown on Sapphire by Metalorganic Vapor Phase Epitaxy," *Cryst. Growth Des.*, vol. 16, no. 6, pp. 3409–3415, 2016.

[54] Y. Kobayashi and T. Akasaka, "Hexagonal BN epitaxial growth on (0001) sapphire substrate by MOVPE," *J. Cryst. Growth*, vol. 310, no. 23, pp. 5044–5047, Nov. 2008.

[55] A. Koma, K. Sunouchi, and T. Miyajima, "Summary Abstract: Fabrication of ultrathin heterostructures with van der Waals epitaxy," *J. Vac. Sci. Technol. B Microelectron. Process. Phenom.*, vol. 3, no. 2, p. 724, Mar. 1985.

[56] A. Koma and K. Yoshimura, "Ultrasharp interfaces grown with Van der Waals epitaxy," *Surf. Sci.*, vol. 174, no. 1, pp. 556–560, 1986.

[57] A. Koma, "Van der Waals epitaxy—a new epitaxial growth method for a highly lattice-mismatched system," *Thin Solid Films*, vol. 216, no. 1, pp. 72–76, 1992.

[58] A. Koma, "Van der Waals epitaxy for highly lattice-mismatched systems," *J. Cryst. Growth*, vol. 201–202, pp. 236–241, 1999.

[59] A. K. Geim and K. S. Novoselov, "The rise of graphene," *Nat. Mater.*, vol. 6, no. 3, pp. 183–191, 2007.

[60] K. Chung, C.-H. Lee, and G.-C. Yi, "Transferable GaN layers grown on ZnO-coated graphene layers for optoelectronic devices.," *Science*, vol. 330, no. 6004, pp. 655–657, Oct. 2010.

[61] G. Sandí, "Handbook of Layered Materials, S.M. Auerbach, K.A. Carrado, P.K.

Dutta (Eds.). Marcel Dekker, New York, NY (2004), 650 pp, price US\$199.95, ISBN: 0-8247-5349-6," *Microporous Mesoporous Mater.*, vol. 81, 2005.

[62] T. Ayari *et al.*, "Novel Scalable Transfer Approach for Discrete III-Nitride Devices Using Wafer-Scale Patterned h-BN/Sapphire Substrate for Pick-and-Place Applications," *Adv. Mater. Technol.*, vol. 4, no. 10, p. 1900164, Oct. 2019.

[63] S. Karrakchou *et al.*, "Effectiveness of selective area growth using van der Waals h - BN layer for crack - free transfer of large - size III - N devices onto arbitrary substrates," *Sci. Rep.*, pp. 1–9, 2020.

[64] C. Xiong *et al.*, "Integrated GaN photonic circuits on silicon (100) for second harmonic generation," *Opt. Express*, vol. 19, no. 11, pp. 10462–10470, 2011.

[65] D. Feezell and S. Nakamura, "Invention, development, and status of the blue light-emitting diode, the enabler of solid-state lighting," *Comptes Rendus Phys.*, vol. 19, no. 3, pp. 113–133, 2018.

[66] X. Guo and E. F. Schubert, "Current crowding in GaN/InGaN light emitting diodes on insulating substrates," *J. Appl. Phys.*, vol. 90, no. 8, pp. 4191–4195, 2001.

[67] S. J. Chang *et al.*, "Nitride-based LEDs with an insulating SiO2 layer underneath p-pad electrodes," *Electrochem. Solid-State Lett.*, vol. 10, no. 6, pp. 175–177, 2007.

[68] R. H. Horng, C. C. Chiang, D. S. Wuu, H. Y. Hsiao, and H. I. Lin, "Enhanced thermal dissipation and light output of GaN/sapphire light-emitting diode by direct Cu electroplating," *Electrochem. Solid-State Lett.*, vol. 11, no. 11, pp. 300–303,

2008.

[69] R. Delmdahl, M. Kunzer, and U. Schwarz, “Thin film LEDs gaining ground: Excimer laser lift-off enables high brightness LED production,” *Laser Tech. J.*, vol. 8, no. 3, pp. 48–52, 2011.

[70] C. Weisbuch, “Review—On The Search for Efficient Solid State Light Emitters: Past, Present, Future,” *ECS J. Solid State Sci. Technol.*, vol. 9, no. 1, p. 016022, 2020.

[71] C. A. Tran *et al.*, “High brightness GaN vertical light emitting diodes on metal alloyed substrate for general lighting application,” *J. Cryst. Growth*, vol. 298, no. SPEC. ISS, pp. 722–724, 2007.

[72] S. J. Wang *et al.*, “Use of patterned laser liftoff process and electroplating nickel layer for the fabrication of vertical-structured GaN-based light-emitting diodes,” *Appl. Phys. Lett.*, vol. 87, no. 1, 2005.

[73] D. S. Wuu, S. C. Hsu, S. H. Huang, and R. H. Horng, “Vertical-conducting p-side-up GaN/mirror/Si light-emitting diodes by laser lift-off and wafer-transfer techniques,” *Phys. Status Solidi Appl. Res.*, vol. 201, no. 12, pp. 2699–2703, 2004.

[74] M. Asad, Q. Li, M. Sachdev, and W. S. Wong, “Enhanced Surface-Emitting Vertical InGaN Light-Emitting Diodes by Self-Aligned Sidewall Electrodes and Optical Cavity Length Modulation,” *ACS Appl. Electron. Mater.*, vol. 3, no. 2, pp. 882–889, Feb. 2021.

[75] S. Karrakchou *et al.*, “Monolithic Free-Standing Large-Area Vertical III-N Light Emitting Diode Arrays by One-Step h-BN-based Thermo-Mechanical Self-Lift-Off and Transfer,” *ACS Appl. Electron. Mater.*, pp. 1–17, 2021.

[76] W. H. Teh, L. T. Koh, S. M. Chen, J. Xie, C. Y. Li, and P. D. Foo, “Study of microstructure and resistivity evolution for electroplated copper films at near-room temperature,” *Microelectronics J.*, vol. 32, no. 7, pp. 579–585, 2001.

[77] Y. Koide *et al.*, “Effects of annealing in an oxygen ambient on electrical properties of ohmic contacts to p-type GaN,” *J. Electron. Mater.*, vol. 28, no. 3, pp. 341–346, 1999.

[78] G. Greco, P. Prystawko, M. Leszczyski, R. Lo Nigro, V. Raineri, and F. Roccaforte, “Electro-structural evolution and Schottky barrier height in annealed Au/Ni contacts onto p-GaN,” *J. Appl. Phys.*, vol. 110, no. 12, 2011.

[79] A. J. Trindade *et al.*, “Heterogeneous integration of gallium nitride light-emitting diodes on diamond and silica by transfer printing,” *Opt. Express*, vol. 23, no. 7, p. 9329, 2015.

[80] F. Liu *et al.*, “Hexagonal BN-Assisted Epitaxy of Strain Released GaN Films for True Green Light-Emitting Diodes,” *Adv. Sci.*, vol. 7, no. 21, pp. 1–8, 2020.

[81] O. B. Shchekin *et al.*, “High performance thin-film flip-chip InGaN-GaN light-emitting diodes,” *Appl. Phys. Lett.*, vol. 89, no. 7, pp. 2004–2007, 2006.

[82] E. Suhir, “Interfacial Stresses in Bimetal Thermostats,” *J. Appl. Mech.*, vol. 56, no.

3, pp. 595–600, Sep. 1989.

[83] F. Kraemer, M. Roellig, R. Metasch, J. Ahmar, K. Meier, and S. Wiese, “Experimental determination of the Young’s modulus of copper and solder materials for electronic packaging,” *Microelectron. Reliab.*, vol. 91, pp. 251–256, 2018.

[84] T. A. Hahn, “Thermal Expansion of Copper from 20 to 800 K—Standard Reference Material 736,” *J. Appl. Phys.*, vol. 41, no. 13, pp. 5096–5101, Dec. 1970.

[85] J. B. WACHTMAN JR. and D. G. LAM JR., “Young’s Modulus of Various Refractory Materials as a Function of Temperature,” *J. Am. Ceram. Soc.*, vol. 42, no. 5, pp. 254–260, May 1959.

[86] W. M. Yim and R. J. Paff, “Thermal expansion of AlN, sapphire, and silicon,” *J. Appl. Phys.*, vol. 45, no. 3, pp. 1456–1457, Mar. 1974.

[87] H. Rokni and W. Lu, “Direct measurements of interfacial adhesion in 2D materials and van der Waals heterostructures in ambient air,” *Nat. Commun.*, vol. 11, no. 1, p. 5607, 2020.

[88] X. Li, P. Li, Z. Wu, D. Luo, H.-Y. Yu, and Z.-H. Lu, “Review and perspective of materials for flexible solar cells,” *Mater. Reports Energy*, vol. 1, no. 1, p. 100001, 2021.

[89] J. Ramanujam *et al.*, “Flexible CIGS, CdTe and a-Si:H based thin film solar cells: A review,” *Prog. Mater. Sci.*, vol. 110, p. 100619, 2020.

[90] S. A. Hashemi, S. Ramakrishna, and A. G. Aberle, “Recent progress in flexible-

wearable solar cells for self-powered electronic devices," *Energy Environ. Sci.*, vol. 13, no. 3, pp. 685–743, 2020.

[91] C. H. Lee, D. R. Kim, and X. Zheng, "Transfer Printing Methods for Flexible Thin Film Solar Cells: Basic Concepts and Working Principles," *ACS Nano*, vol. 8, no. 9, pp. 8746–8756, Sep. 2014.

[92] J. Yoon *et al.*, "GaAs photovoltaics and optoelectronics using releasable multilayer epitaxial assemblies," *Nature*, vol. 465, no. 7296, pp. 329–333, 2010.

[93] S. Sundaram *et al.*, "Nanoselective area growth and characterization of dislocation-free InGaN nanopyramids on AlN buffered Si(111) templates," *Appl. Phys. Lett.*, vol. 107, no. 11, 2015.

[94] H. Katagiri *et al.*, "Development of CZTS-based thin film solar cells," *Thin Solid Films*, vol. 517, no. 7, pp. 2455–2460, 2009.

[95] K. Wang *et al.*, "Thermally evaporated Cu2ZnSnS4 solar cells," *Appl. Phys. Lett.*, vol. 97, no. 14, p. 143508, Oct. 2010.

[96] G. C. Righini and F. Enrichi, *Solar cells' evolution and perspectives: A short review*. Elsevier Ltd, 2019.

[97] J. Wu *et al.*, "Small band gap bowing in In1−xGaxN alloys," *Appl. Phys. Lett.*, vol. 80, no. 25, pp. 4741–4743, Jun. 2002.

[98] K. Pantzas *et al.*, "Semibulk InGaN: A novel approach for thick, single phase, epitaxial InGaN layers grown by MOVPE," *J. Cryst. Growth*, vol. 370, pp. 57–62,

2013.

[99] W. Zhao, L. Wang, J. Wang, Z. Hao, and Y. Luo, “Theoretical study on critical thicknesses of InGaN grown on (0001) GaN,” *J. Cryst. Growth*, vol. 327, no. 1, pp. 202–204, 2011.

[100] A. E. Romanov, T. J. Baker, S. Nakamura, and J. S. Speck, “Strain-induced polarization in wurtzite III-nitride semipolar layers,” *J. Appl. Phys.*, vol. 100, no. 2, p. 23522, Jul. 2006.

[101] J. J. Wierer, A. J. Fischer, and D. D. Koleske, “The impact of piezoelectric polarization and nonradiative recombination on the performance of (0001) face GaN/InGaN photovoltaic devices,” *Appl. Phys. Lett.*, vol. 96, no. 5, p. 51107, Feb. 2010.

[102] L. Li *et al.*, “The Effects of a Low-Temperature GaN Interlayer on the Performance of InGaN/GaN Solar Cells,” *Chinese Phys. Lett.*, vol. 30, no. 2, p. 28801, 2013.

[103] O. Jani *et al.*, “Effect of phase separation on performance of III-V nitride solar cells,” *22nd Eur. Photovolt. Sol. Energy Conf.*, no. September, pp. 64–67, 2007.

[104] O. Jani, I. Ferguson, C. Honsberg, and S. Kurtz, “Design and characterization of GaN/InGaN solar cells,” *Appl. Phys. Lett.*, vol. 91, no. 13, p. 132117, Sep. 2007.

[105] M. Arif *et al.*, “Improving InGaN heterojunction solar cells efficiency using a semibulk absorber,” *Sol. Energy Mater. Sol. Cells*, vol. 159, no. October 2016, pp. 405–411, 2017.

[106] N. G. Young *et al.*, "High performance thin quantum barrier InGaN/GaN solar cells on sapphire and bulk (0001) GaN substrates," *Appl. Phys. Lett.*, vol. 103, no. 17, p. 173903, Oct. 2013.

[107] C. J. Neufeld, N. G. Toledo, S. C. Cruz, M. Iza, S. P. DenBaars, and U. K. Mishra, "High quantum efficiency InGaN/GaN solar cells with 2.95 eV band gap," *Appl. Phys. Lett.*, vol. 93, no. 14, p. 143502, Oct. 2008.

[108] L. Redaelli *et al.*, "Effect of the quantum well thickness on the performance of InGaN photovoltaic cells," *Appl. Phys. Lett.*, vol. 105, no. 13, p. 131105, Sep. 2014.

[109] B. W. Liou, "Design and fabrication of InxGa1−xN/GaN solar cells with a multiple-quantum-well structure on SiCN/Si(111) substrates," *Thin Solid Films*, vol. 520, no. 3, pp. 1084–1090.

[110] S. Sundaram *et al.*, "Nanoscale selective area growth of thick, dense, uniform, In-rich, InGaN nanostructure arrays on GaN/sapphire template," *J. Appl. Phys.*, vol. 116, no. 16, p. 163105, Oct. 2014.

[111] G. F. Brown, J. W. A. Iii, W. Walukiewicz, and J. Wu, "Solar Energy Materials & Solar Cells Finite element simulations of compositionally graded InGaN solar cells," *Sol. Energy Mater. Sol. Cells*, vol. 94, no. 3, pp. 478–483, 2010.

[112] S. Adachi, *Physical properties of III-V semiconductor compounds : InP, InAs, GaAs, GaP, InGaAs, and InGaAsP*. New York: Wiley, 1992.

[113] R. Magnusson and S. S. Wang, "New principle for optical filters," *Appl. Phys. Lett.*,

vol. 61, no. 9, pp. 1022–1024, Aug. 1992.

[114] R. Dahal, J. Li, K. Aryal, J. Y. Lin, and H. X. Jiang, "InGaN/GaN multiple quantum well concentrator solar cells," *Appl. Phys. Lett.*, vol. 97, no. 7, p. 73115, Aug. 2010.

[115] N. G. Young *et al.*, "High-performance broadband optical coatings on InGaN/GaN solar cells for multijunction device integration," *Appl. Phys. Lett.*, vol. 104, no. 16, p. 163902, Apr. 2014.

[116] W. El-Huni, A. Migan, D. Alamarguy, and Z. Djebbour, "Modeling of InGaN/Si tandem cells: comparison between 2-contacts/4-contacts," *EPJ Photovolt.*, vol. 8, 2017.

[117] M. D. Kelzenberg, M. C. Putnam, D. B. Turner-Evans, N. S. Lewis, and H. A. Atwater, "Predicted efficiency of Si wire array solar cells," in *2009 34th IEEE Photovoltaic Specialists Conference (PVSC)*, 2009, pp. 1948–1953.

[118] K. Yang, J. R. East, and G. I. Haddad, "Numerical modeling of abrupt heterojunctions using a thermionic-field emission boundary condition," *Solid. State. Electron.*, vol. 36, no. 3, pp. 321–330, 1993.

[119] W. El-huni, A. Migan, Z. Djebbour, J. Salvestrini, and A. Ougazzaden, "High-efficiency indium gallium nitride / Si tandem photovoltaic solar cells modeling using indium gallium nitride semibulk material : monolithic integration versus 4-terminal tandem cells," Progress in Photovoltaics Research and Applications 24(11), pp. 1436–1447, 2016.

[120] M. R. Islam, M. R. Kaysir, M. J. Islam, A. Hashimoto, and A. Yamamoto, "MOVPE Growth of InxGa1−xN (x ∼ 0.4) and Fabrication of Homo-junction Solar Cells," *J. Mater. Sci. Technol.*, vol. 29, no. 2, pp. 128–136, 2013.

[121] P. G. Moses and C. G. Van de Walle, "Band bowing and band alignment in InGaN alloys," *Appl. Phys. Lett.*, vol. 96, no. 2, p. 21908, Jan. 2010.

[122] W. El Huni *et al.*, "Nanopyramid-based absorber to boost the efficiency of InGaN solar cells," *Sol. Energy*, vol. 190, 2019.

[123] C. A. M. Fabien *et al.*, "Simulations, Practical Limitations, and Novel Growth Technology for InGaN-Based Solar Cells," *IEEE J. Photovoltaics*, vol. 4, no. 2, pp. 601–606, 2014.

[124] Z. Q. Li, M. Lestradet, Y. G. Xiao, and S. Li, "Effects of polarization charge on the photovoltaic properties of InGaN solar cells," *Phys. status solidi*, vol. 208, no. 4, pp. 928–931, Apr. 2011.

[125] D. Elwell and M. M. Elwell, "Crystal growth of gallium nitride," *Prog. Cryst. Growth Charact.*, vol. 17, no. 1, pp. 53–78, 1988.

[126] C. G. Van De Walle, C. Stampfl, and J. Neugebauer, "Theory of doping and defects in III-V nitrides," *J. Cryst. Growth*, vol. 189–190, pp. 505–510, 1998.

[127] B. N. Pantha, H. Wang, N. Khan, J. Y. Lin, and H. X. Jiang, "Origin of background electron concentration in InxGa1-xN alloys," Phys. Rev. B, vol. 84, no. 7, p. 75327, Aug. 2011.

[128] W. Zhou and Z. Lin, "Scanning Microscopy for Nanotechnology : Techniques and Applications" Springer, ISBN 978-0-387-39620-0. 2007.

[129] R. Puybaret, “Epitaxial Graphene and Nitrides : New Processes for Improved Electronics and Optoelectronics Epitaxial Graphene and Nitrides : New Processes for Improved Electronics,” PhD Thesis, 2015.

[130] A. Raghunathan and J. G. Hartley, “Influence of secondary electrons in high-energy electron beam lithography,” *J. Vac. Sci. Technol. B*, vol. 31, no. 1, p. 11605, Jan. 2013.

[131] Falco C. M. J. M. van Delft, “Delay-time and aging effects on contrast and sensitivity of hydrogen silsesquioxane,” *J. Vac. Sci. Technol. B Microelectron. Nanom. Struct.*, vol. 20, no. 6, pp. 2932–2936, 2002.

[132] L. O’Faolain, M. V Kotlyar, N. Tripathi, R. Wilson, and T. F. Krauss, “Fabrication of photonic crystals using a spin-coated hydrogen silsesquioxane hard mask,” *J. Vac. Sci. Technol. B Microelectron. Nanom. Struct. Process. Meas. Phenom.*, vol. 24, no. 1, pp. 336–339, Jan. 2006.

[133] G. Orsal *et al.*, “Bandgap energy bowing parameter of strained and relaxed InGaN layers,” *Opt. Mater. Express*, vol. 4, no. 5, pp. 1030–1041, 2014.

[134] R. Singh, D. Doppalapudi, T. D. Moustakas, and L. T. Romano, “Phase separation in InGaN thick films and formation of InGaN/GaN double heterostructures in the entire alloy composition,” *Appl. Phys. Lett.*, vol. 70, no. 9, pp. 1089–1091, Mar. 1997.

[135] R. A. Oliver *et al.*, "Microstructural origins of localization in InGaN quantum wells," *J. Phys. D. Appl. Phys.*, vol. 43, no. 35, p. 354003, 2010.

[136] P. Hirsch, M. Kässens, M. Püttmann, and L. Reimer, "Contamination in a scanning electron microscope and the influence of specimen cooling," *Scanning*, vol. 16, no. 2, pp. 101–110, Mar. 1994.

[137] R. Tiron, L. Mollard, O. Louveau, and E. Lajoinie, "Ultrahigh-resolution pattern using electron-beam lithography HF wet etching," *J. Vac. Sci. Technol. B Microelectron. Nanom. Struct. Process. Meas. Phenom.*, vol. 25, no. 4, pp. 1147–1151, Jun. 2007.

[138] G. Greco, F. Iucolano, and F. Roccaforte, "Ohmic contacts to Gallium Nitride materials," *Appl. Surf. Sci.*, vol. 383, pp. 324–345, 2016.

[139] F. Olivier, S. Tirano, L. Dupré, B. Aventurier, C. Largeron, and F. Templier, "Influence of size-reduction on the performances of GaN-based micro-LEDs for display application," *J. Lumin.*, vol. 191, no. PB, pp. 112–116, 2017.

[140] S. Valdueza-Felip *et al.*, "P-i-n InGaN homojunctions (10–40% In) synthesized by plasma-assisted molecular beam epitaxy with extended photoresponse to 600nm," *Sol. Energy Mater. Sol. Cells*, vol. 160, pp. 355–360, 2017.

[141] E. Monroy *et al.*, "Modification of GaN(0001) growth kinetics by Mg doping," *Appl. Phys. Lett.*, vol. 84, no. 14, pp. 2554–2556, Apr. 2004.

[142] L. Lahourcade *et al.*, "Mg doping and its effect on the semipolar GaN(11$\bar{2}$2)

growth kinetics," *Appl. Phys. Lett.*, vol. 95, no. 17, p. 171908, Oct. 2009.

[143] E. C. Young *et al.*, "Hybrid tunnel junction contacts to III–nitride light-emitting diodes," *Appl. Phys. Express*, vol. 9, no. 2, p. 22102, 2016.

[144] C. Zhou *et al.*, "Review—The Current and Emerging Applications of the III-Nitrides," *ECS J. Solid State Sci. Technol.*, vol. 6, no. 12, pp. Q149–Q156, 2017.

[145] S. A. Dyer, "Wiley Survey of Instrumentation and Measurement," p. 1112, 2004.

[146] H. Morkoç, "Handbook of Nitride Semiconductors and Devices," *Handb. Nitride Semicond. Devices*, vol. 1, pp. 1–1255, 2009.

[147] W. Paszkowicz, J. B. Pelka, M. Knapp, T. Szyszko, and S. Podsiadlo, "Lattice parameters and anisotropic thermal expansion of hexagonal boron nitride in the 10-297.5 K temperature range," *Appl. Phys. A Mater. Sci. Process.*, vol. 75, no. 3, pp. 431–435, 2002.

[148] A. R. Denton and N. W. Ashcroft, "Vegard's law," *Phys. Rev. A*, vol. 43, no. 6, pp. 3161–3164, Mar. 1991.

[149] O. Ambacher *et al.*, "Two-dimensional electron gases induced by spontaneous and piezoelectric polarization charges in N- and Ga-face AlGaN/GaN heterostructures," *J. Appl. Phys.*, vol. 85, no. 6, pp. 3222–3233, Mar. 1999.

[150] J. Li et al., "III-Nitrides Light Emitting Diodes : Technology and Applications", Springer, ISBN 978-981-15-7949-3, 2020.

[151] L. C. Lew Yan Voon, M. Willatzen, M. Cardona, and N. E. Christensen, "Terms

linear in k in the band structure of wurtzite-type semiconductors," *Phys. Rev. B*, vol. 53, no. 16, pp. 10703–10714, Apr. 1996.

[152] R. F. Davis et al., "Organometallic Vapor Phase Epitaxial Growth of Group III Nitrides", Reference Module in Materials Science and Materials Engineering, Elsevier, 2017.

[153] X. Li, "BAlGaN-based vertical cavity surface-emitting lasers operating in deep UV region", PhD Thesis, 2016.