ULTRA-WIDEBAND AND HIGHLY LINEAR 43-97 GHZ RECEIVER FRONT-END

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ULTRA-WIDEBAND AND HIGHLY LINEAR 43-97 GHZ RECEIVER FRONT-END

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SUMMARY

This research presents a wideband mmWave receiver front-end that covers the frequency range from 43 to 97 GHz, supporting the operation in the major parts of the V-, E- and W-bands. The front-end incorporates a passive mixer-first topology to achieve high linearity and wideband performance along with an optimum operational instantaneous bandwidth. The front-end adopts I/Q generation at the RF port, using a coupled-line-coupler (CLC), rather than at the LO port in order to mitigates the cross-talk of the overlapping I/Q LO signals specially present at high frequencies. The CLC at the RF input facilitates ultrawide band input matching. The front-end implements the multi-gate gm3 cancellation technique at the IF amplifiers to preserve the linearity and provide gain at the IF section. Image rejection capabilities using a current mode transformer based IF 90^{o} coupler is implemented on chip and demonstrated with measurements. The front-end is fabricated on the GlobalFoundries 22nm FD-SOI CMOS process and demonstrates an ultra-wideband performance across the frequency range 43-97 GHz (2.25:1 bandwidth) with image rejection of up to 32 dB, IIP3 of 1.6-5.2 dBm and gain of 15 dB. Furthermore, the measurement results show that the front-end supports high speed modulated signals of up to 6 Gbps 64QAM modulation data.

CHAPTER 1. INTRODUCTION

Next generation high frequency mmWave communication links mandates extreme data rates (multi-Gb/s) to enable existing and emerging applications such as radar systems, 5G new radio (NR) and high speed/capacity backhaul communications. These links can be supported on a variety of available frequency bands that offer wide available bandwidths and can be exploited for faster and higher data capacity. Such high frequency bands include the V-band (40-75 GHz), E-band (71-76 GHz, 81-86 GHz, and 92-95 GHz) and W-band (75-110 GHz) that can be utilized with massive MIMO and phased array systems. With such a wide available frequency spectrum, high-performance wireless hardware implementations are required to best utilize these resources. Wireless receivers' frontends are one of the key components in such links; they have stringent performance requirements to maintain the overall quality. For example, receiver frontends should be able to support and successfully receive high speed modulated signals with good quality. In addition, they need to provide high linearity performance, especially in a congested and contested environment where large blockers can degrade or even completely shut down the desired communication link. Furthermore, frontends need to reject and attenuate the undesired image signal present in the surrounding EM environment. Existing state of the art high frequency and wideband receiver front-end designs include either mixer-first [1-3] or LNA-first [4-11] topologies. However, although achieving good performances, most of the existing designs only support limited carrier frequency bandwidth and, hence, cannot simultaneously cover most of the high frequency mmWave bands with only one chip footprint. LNA-first topology provides lower noise figure, however, presents limited

linearity and blocker rejection in the RF domain. This limited first-stage blocker rejection is critical for wideband implementations where usually SAW filters are not used. Thus, in a congested EM environment and in presence of strong co-side interferences, the LNA, and hence the receiver, might saturate, causing the desired wireless link to be lost. On the contrary, mixer-first implementations can support ultra-wideband frequency coverage while at the same time provide an optimal instantaneous bandwidth since the bandwidth is limited by the bandpass filtering behavior at the very first stage; the mixer. Therefore, it is less susceptible to out of band blockers. In addition, the mixer-first topology can achieve better linearity in terms of intermodulation performance. This is very critical in multi-stream and multi-beam MIMO links that are vulnerable to intermodulation and cross modulation products of the upcoming streams/interferers [12]. Although, the mixer-first topology provides inferior noise figure performance compared to the LNA-first topology, the overall SNR of the received signal is enhanced by the array gain when implemented in a beamforming/MIMO system [13]. As a comparison between mixer-first and LNA-first topologies, Fig. 1 presents a summary of performances of the state-of-the-art wideband CMOS implementations. It is clearly shown that both topologies can achieve large carrier frequency bandwidth, however, only mixer-first topology presents an optimal instantaneous bandwidth at an early stage in the front-end along with similar in-band compression points.

Given the challenges and requirements for wireless links at high frequency mmWave bands, we propose an ultra-wideband receiver frontend that can better fit with these requirements. This thesis is organized as follows. Chapter 2 presents the overall proposed architecture and chosen topology of the front-end. Then, it presents circuit implementation

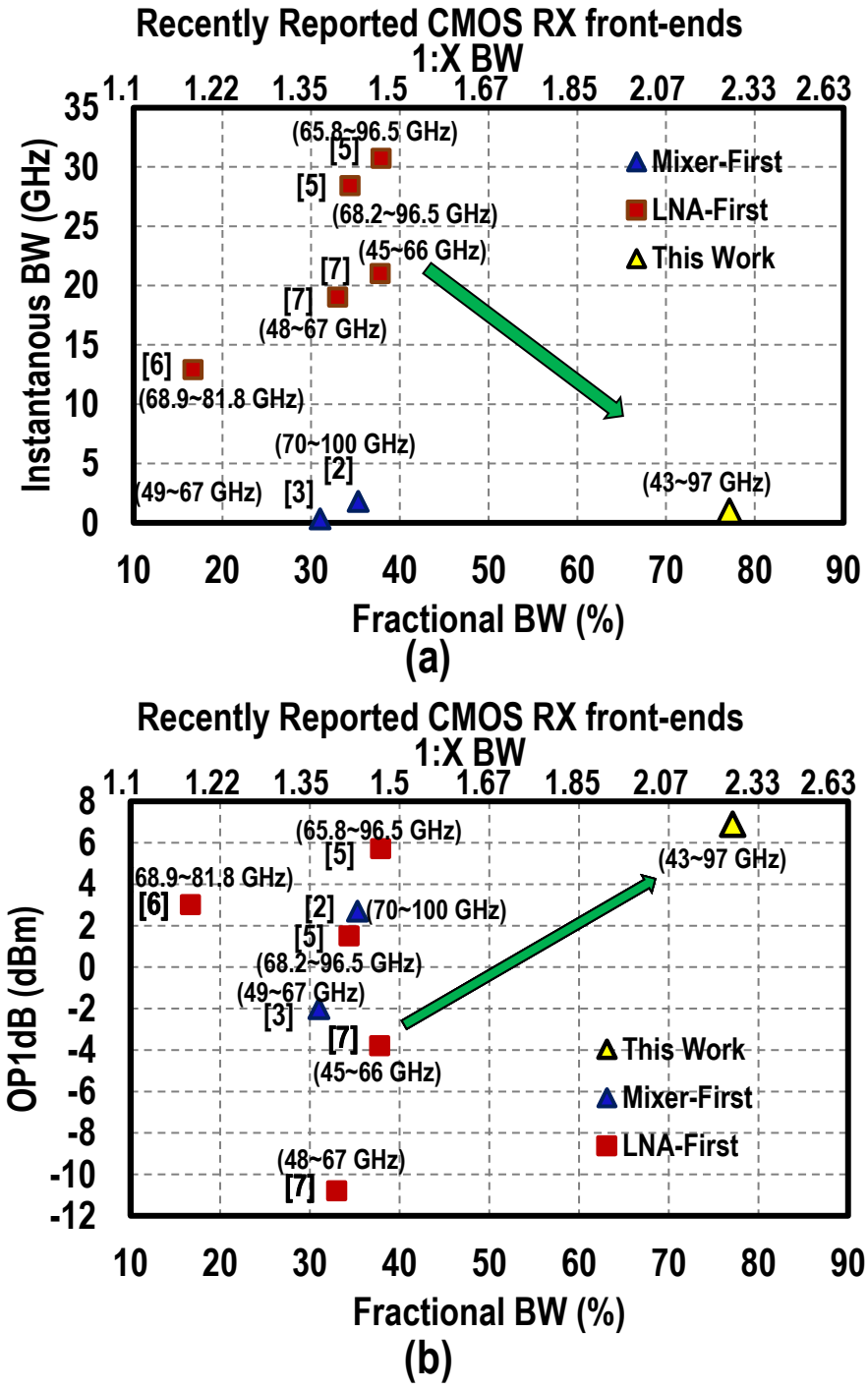

Figure 1 Gain and Image

details and simulation results. Chapter 3 summarizes the experimental test setups and

measurement results and compares this work with the state of the art. Finally, chapter 4 concludes the work.

CHAPTER 2. PROPOSED WIDEBAND FRONT-END

In order to achieve a wideband receiver front-end while providing only the desired instantaneous bandwidth at the early stage of operation and maintaining high intermodulation performance, this work presents a mixer-first front end achieving an ultra-wideband frequency of operation from 43 to 97 GHz (77% fractional bandwidth) covering most of the high frequency mmWave bands while maintaining a 1 GHz instantaneous bandwidth of operation [14]. The bandwidth of operation (1 GHz) is chosen to be able to provide Gbps data rates suitable for future mmWave communications as indicated in the exemplary link budget table in [13].

The proposed chip (Fig. 2) incorporates RF 90^{o} coupled-line-coupler (CLC) to generate quadrature signals at the RF domain rather than the LO domain. This configuration is used because the characteristics of the CLC can be exploited to achieve wideband input matching without the need for additional high order matching networks that will induce losses. In addition, and more importantly, at such high frequencies it is not possible to generate non overlapping I/Q LO phases, hence, the choice of quadrature LO generation will cause cross talk between mixer switches to occur, thus, degrading the down conversion performance [15-16]. Finally, this design decouples the input matching design from the mixer size choice. The generated quadrature signal is then down converted to IF frequency using passive mixers; designed with high linearity in order reduce the effect of interferes' intermodulation products and to provide bandpass filtering for out of band blockers. The choice of the mixer switch size is determined by the NF and linearity

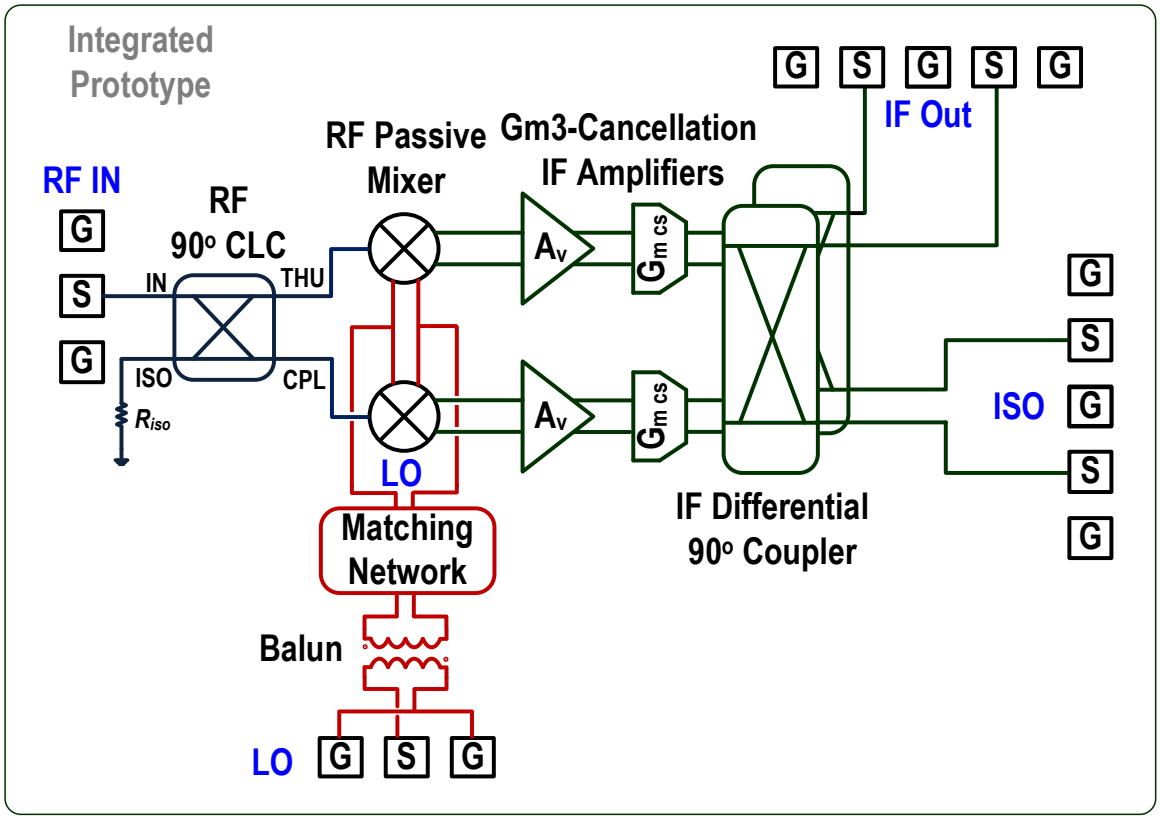

Figure 2 Proposed front-end implementation.

requirements without worrying about the input matching performance. The mixer switches are driven by a differential LO signal generated with on-chip Marchand balun.

The IF section of the front-end consists of two-stage high linearity amplifiers incorporating multi-gated transistors (MGTRs) [17-23] in order to maintain high intermodulation performance (IP3), necessary when implementing beamformer or MIMO systems [12]. The second stage is loaded with a transformer-based coupler [24-29] to provide current mode on-chip image rejection.

2.1 Circuit Implementation and Simulation Results

2.1.1 RF Coupled-Line-Coupler

The structure of the multi-section CLC is shown in Figure 3. Figure 3a and 3c show the parameters and EM structure used, and Fig. 3b shows the flowgraph of an ideal coupled line coupler. The s-parameters of an ideal coupled-line-coupler is shown in (1) where C is the coupling coefficient [29-31].

$$\begin{aligned} S_{11} = S_{22} = S_{33} = S_{44} = 0 \\ S_{12} = S_{21} = S_{34} = S_{42} = -j\sqrt{1-C^2} \\ S_{13} = S_{31} = S_{42} = S_{24} = C \\ S_{14} = S_{41} = S_{23} = S_{32} = 0 \end{aligned} \tag{1}$$

From Figure 3b, if port 4 is matched ($\Gamma_4 = 0$), then the input reflection coefficient (Γ_{IN}) is calculated to be:

$$\begin{aligned} \Gamma_{IN} &= S_{21}S_{12}\Gamma_L + S_{31}S_{13}\Gamma_L \\ &= C^2\Gamma_L - (1-C^2)\Gamma_L = (2C^2-1)\Gamma_L \\ &= 0 \quad when\ C = {}^1/_{\sqrt{2}} \end{aligned} \tag{2}$$

This indicates that regardless of the load impedance presented at the coupled and through port (arbitrary Γ_L), the input matching is maintained as long as the input power is equally split between the coupled and through ports. This is demonstrated with simulating S11 of the CLC structure loaded with different impedances (Figure 4a) and showing good matching performance. Figure 4b shows the overall gain and phase matching of the CLC when loaded with the actual mixer load.

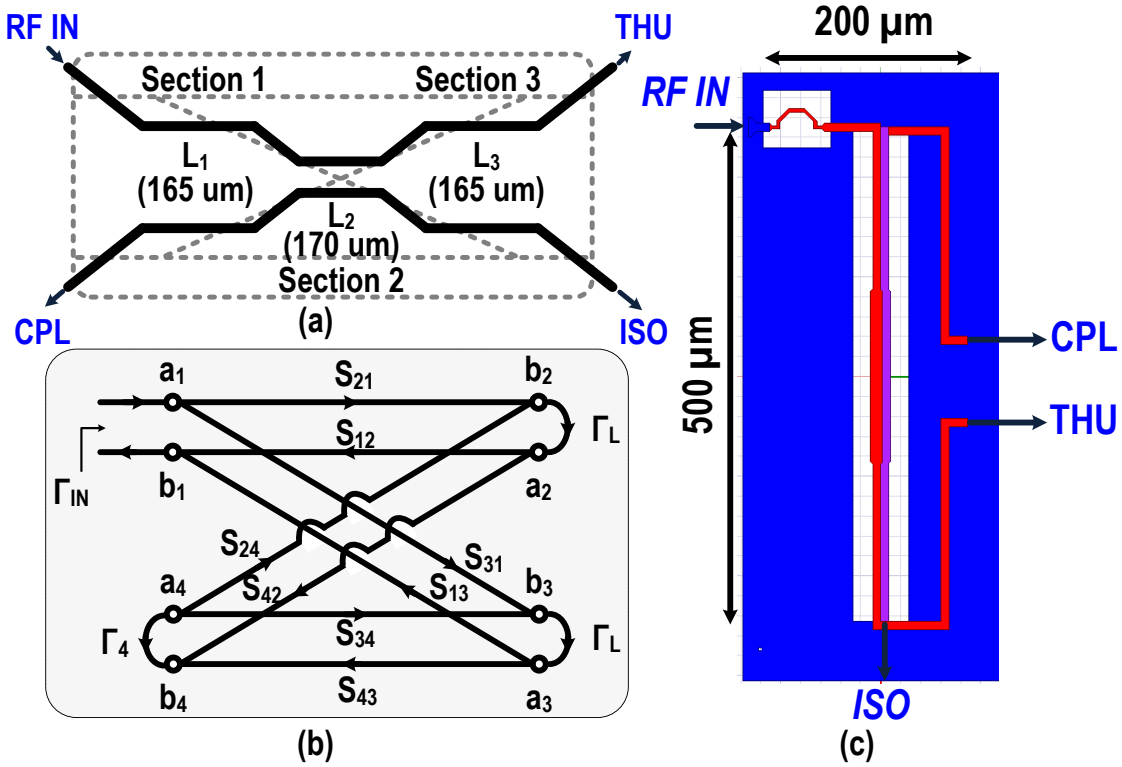

Figure 3 RF Coupled-Line-Coupler (CLC) (a) Multi-section parameters, (b) Ideal signal flowgraph (c) EM structure.

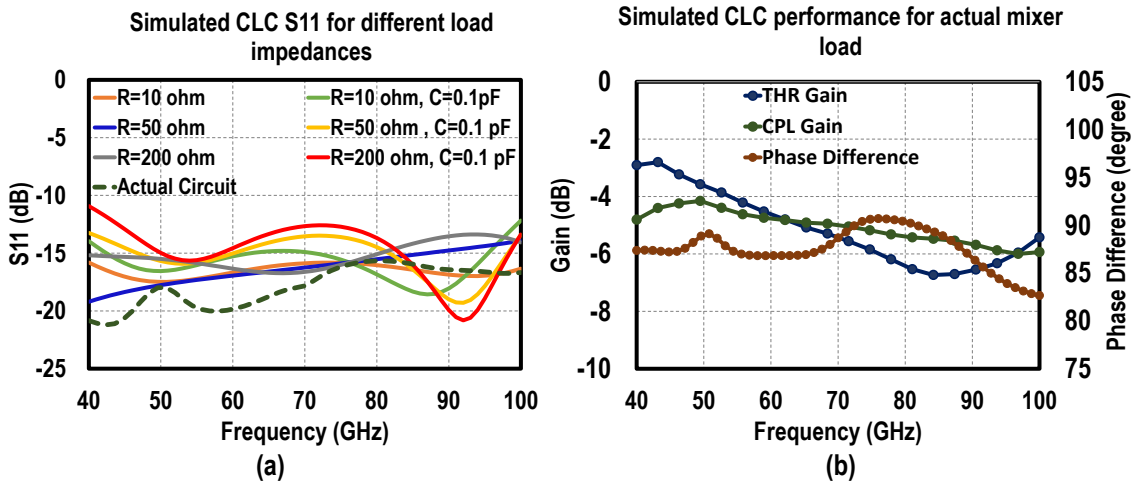

Figure 4 Simulated CLC (a) S11 for different load impedances, (b) phase difference and gain of the coupled and through ports.

The choice of a multi-section CLC helps in extending the performance range of the

I/Q balance of the structure [29]. Figure 5 shows the simulated I/Q balance of the coupler when loaded with 50 Ω. The figure compares a plot for the multi-section coupler versus a family of plots for the single section coupler, where the length and width are swept, showing a wider performance bandwidth for the multi-section implementation. The equation used is (which is the inverse of IRR shown in [28] and assuming small mismatch):

$$I/Q\ Balance = \frac{(1+\varepsilon)^2 - 2(1+\varepsilon)cos\,\Delta\theta + 1}{(1+\varepsilon)^2 + 2(1+\varepsilon)cos\,\Delta\theta + 1} \approx \frac{\varepsilon^2 + \Delta\theta^2}{4} \tag{3}$$

Where ε represents the amplitude mismatch and Δθ represents the phase mismatch.

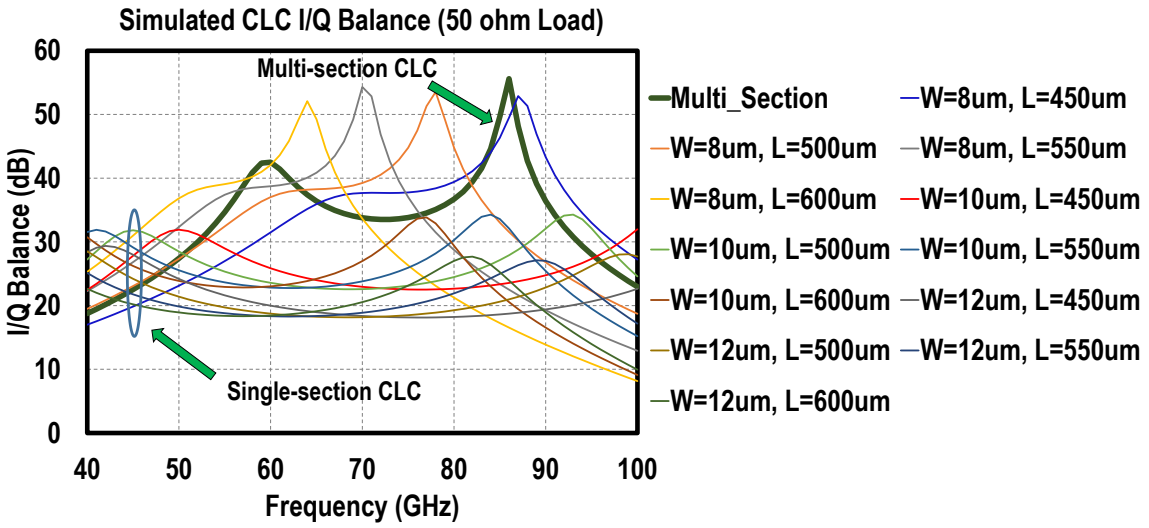

Figure 5 Simulated I/Q balance of the CLC

2.1.2 Passive Mixer and LO Balun

The passive mixer implementation is shown in Figure 6a, it consists of a single-balanced implementation for each of the I/Q cells with a differential sin wave LO signal. The simulated conversion gain around the LO harmonics is shown in Figure 6b. The fact that the LO signal is sin wave, ideally only the fundamental component of the LO should

be present. However, because of the non-linearities and on-off-like operation of the transistors, RF signals around the third harmonic of the LO signal will be down-converted to the desired IF band (similar to N-path filters [32-34]). Several techniques are proposed in the literature to further reduce or cancel the third harmonic folding [35-38]. However, some of these techniques requires the use of driving frequencies at harmonics of the LO or generation of more than 4 LO phases. These techniques are either complex and cause degraded performance or not practical at such high frequencies. In this implementation, third order harmonic will always be outside the bandwidth of operation (43~97 GHz) and

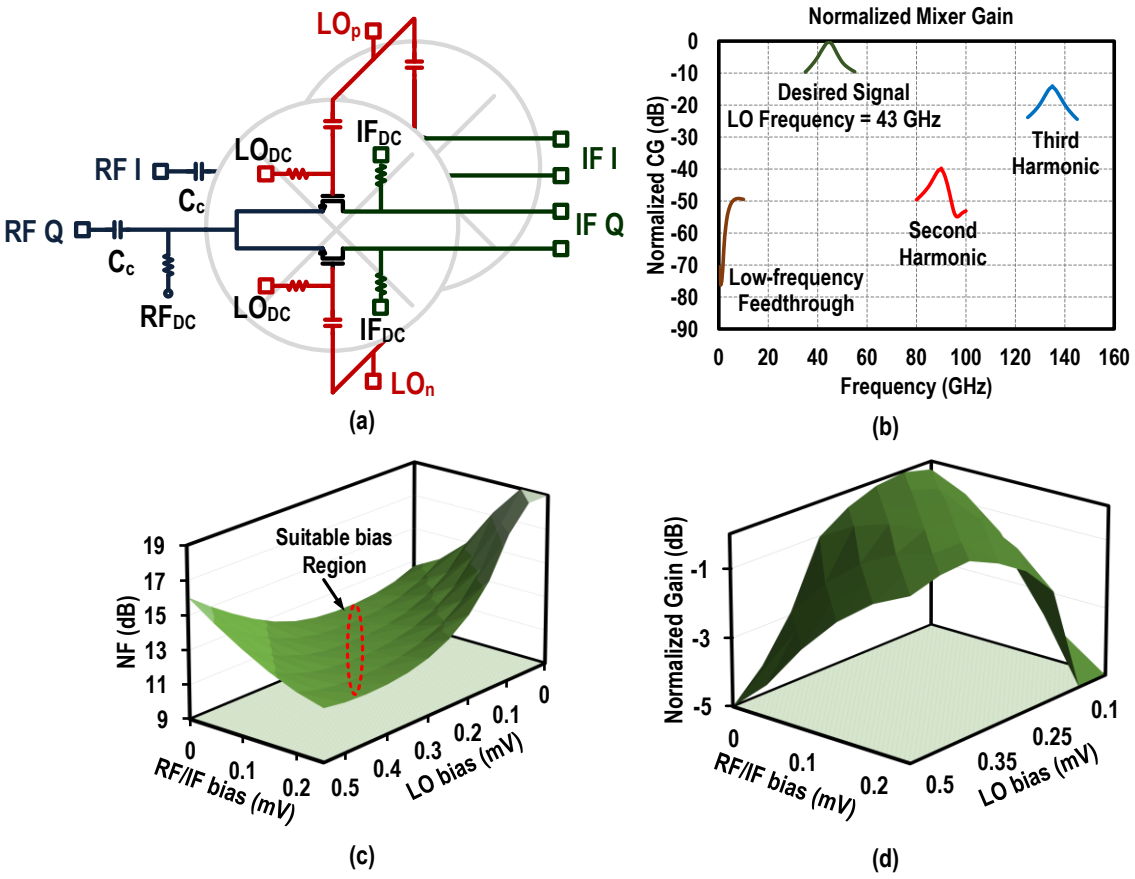

Figure 6 (a) Passive I/Q mixer implementation, (b) Normalized gain at different harmonics, (c) noise figure versus bias voltages, (d) normalized gain versus bias voltages.

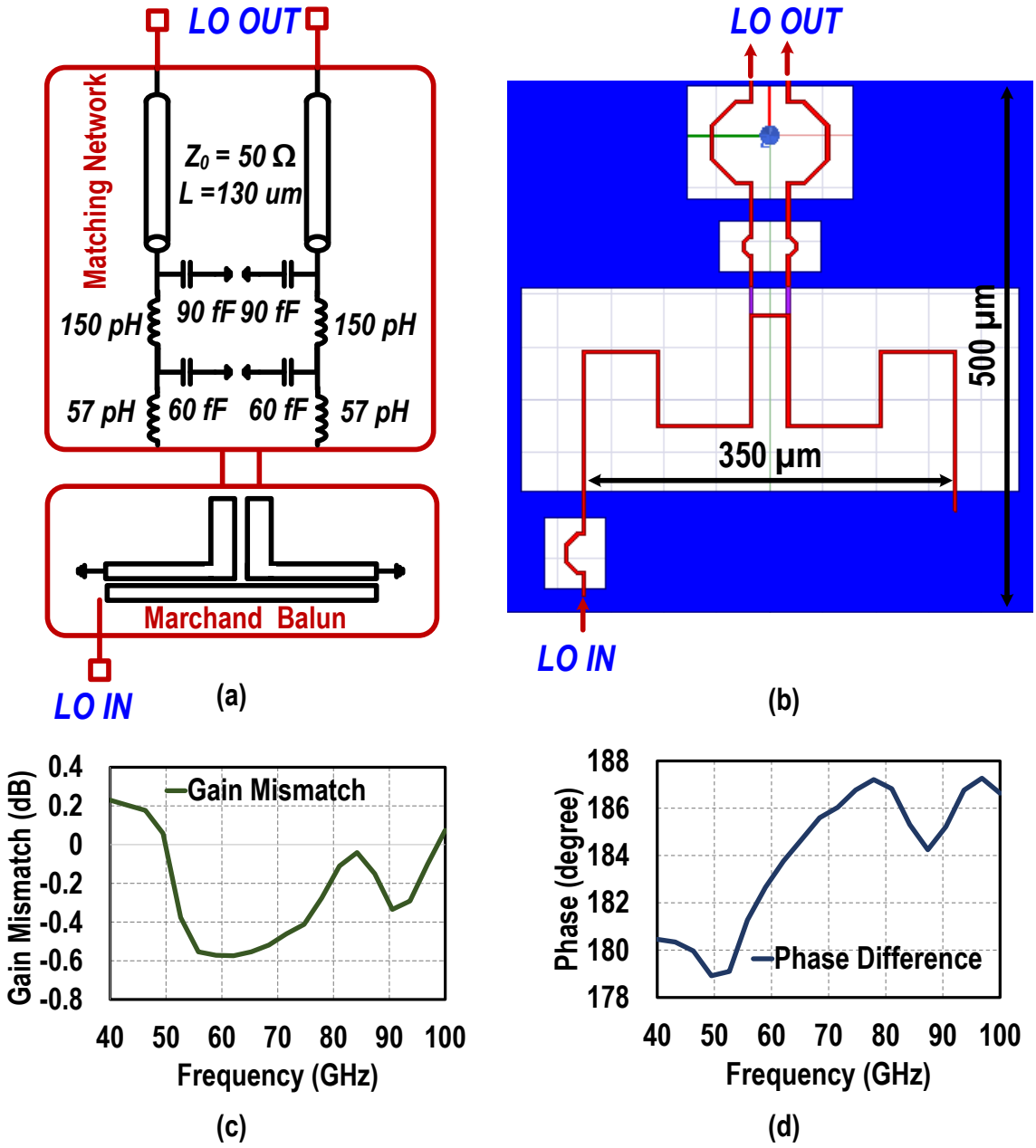

Figure 7 (a) LO Marchand balun and matching network, (b) EM structure, (c) gain mismatch of the differential outputs, (d) phase difference of the outputs.

will not be suppressed when the front-end is integrated with the corresponding antenna. Therefore, these techniques are not implemented to avoid performance degradation. Figure 6c and d shows the simulated noise figure and normalized gain versus the LO (gate) bias and RF/IF bias voltages. The optimum difference between the LO and RF/IF voltages is

around 0.2 V. The differential LO phases are generated with an on-chip Marchand balun [29][39-40] and a high order matching network (Figure 7). The simulated gain mismatch between the signal is between -0.6 to 0.2 dB (Figure 7c) and the phase difference is shown in Figure 7d.

2.1.3 IF Section

The IF gain section is composed of two stage amplifiers employing multi-gated transistors to achieve gm3 cancellation of the main transistor [17-23]. The first stage (Figure 8a) is implemented as tuned cascode structure with one main transistor and three auxiliary transistors with different sizes and bias voltages. Figure 9a shows the gm3 of each of the four transistors as well as the overall gm3. Here, the auxiliary transistors (M2-M4) have a reduced bias voltage (compared to M1) allowing them to switch later on and shift their gm3 plots to the left, hence, collaboratively equalizing the highly negative gm3 of the main transistor and achieving a flat overall gm3 performance. Since the auxiliary transistors need to be biased in class B or C (or AB), they are implemented as high threshold voltage transistors (hvt) as opposed to low threshold voltage transistor (lvt) used for M1.

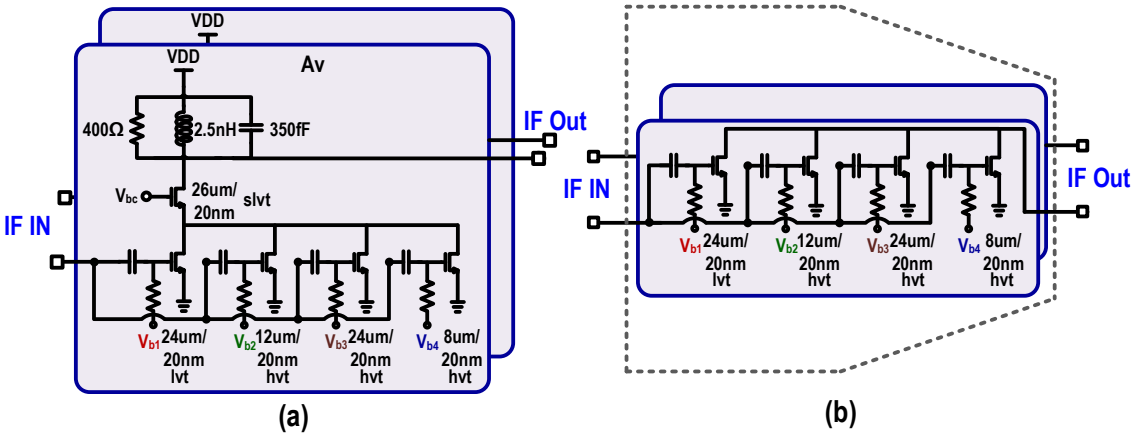

Figure 8 (a) IF first gain stage, (b) IF second gain stage.

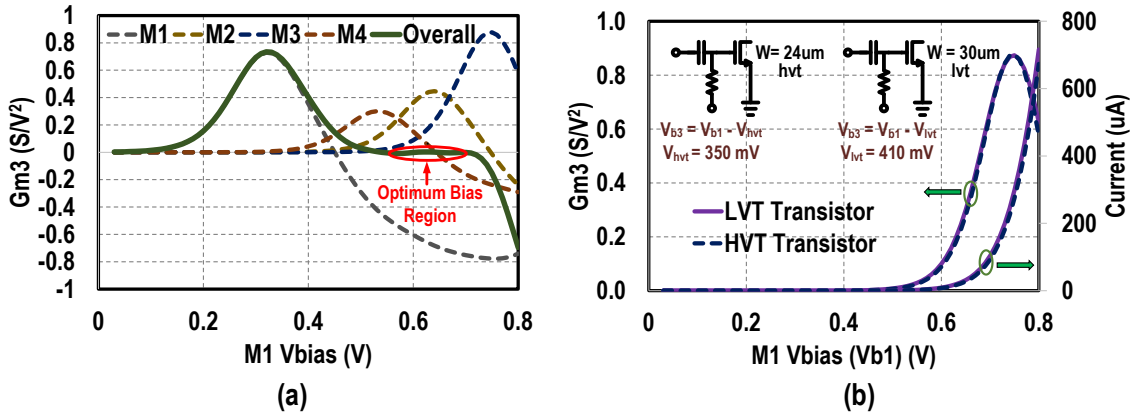

Figure 9 (a) Gm3 (second derivative of the transconductance), (b) gm3 performance with different transistor flavors.

Choosing between hvt and lvt transistors to implement M2-M4 is arbitrary and both options can achieve similar performance. In Figure 9b, simulations for the transistor M3 with lvt and hvt flavors show indeed the gm3 value and current consumption is almost the same for both options with the correct bias values and sizes (W= 30µm for lvt and 24µm for hvt). However, the lvt transistor requires 60mV lower bias voltage than the hvt transistors and hence impose more limitation on the usable bias voltage range of the main transistor when

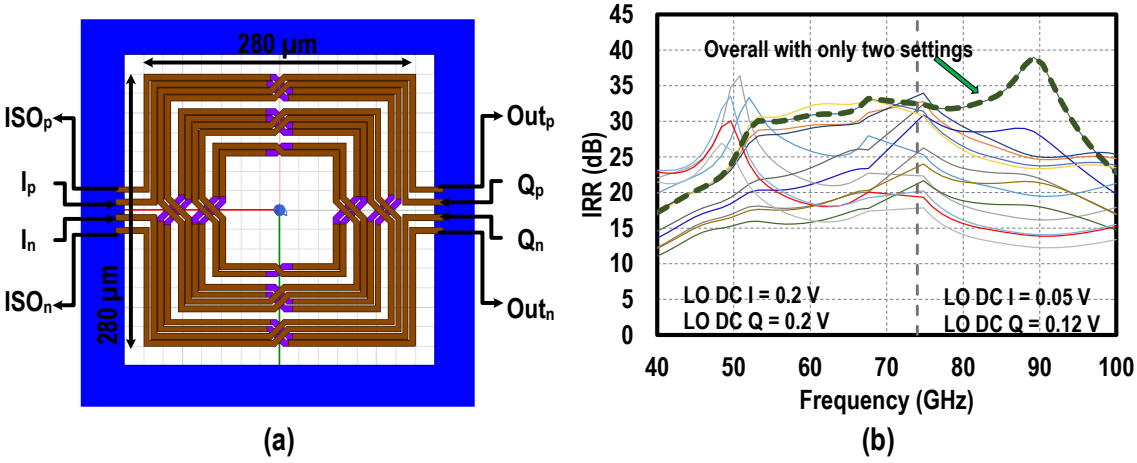

Figure 10 (a) EM structure of the IF 90 coupler, (b) simulated image rejection performance of the frontend while sweeping the I/Q mixers' gate biases.

all the bias voltages should be positive (i.e. the M1 bias cannot be lower than 350mV when using hvt transistor and 410mV for lvt transistor). The second stage (Figure 8b) is a gm stage implementing the same multi-gate transistors without the cascode transistor. The output current of the gm stages from the I and Q paths are used to feed an IF transformer-based coupler [24-29] (Figure 10a) acting as a polyphase filter in order to reject the image signal.

The simulated image rejection performance of the overall frontend is shown in Figure 10b. Here, the gate biases of the I/Q passive mixer transistors are independently swept from 50mV to 250mV and the image rejection ratio (IRR) is calculated as the difference between the desired and image signals' gain. In this design, only two settings (shown in Figure 10b for the LO DC bias values) are chosen to cover the overall bandwidth (although using more than two setting regions can achieve higher performance in some frequency ranges).

CHAPTER 3. MEASURMENT RESULTS

The designed ultra-wideband mixer-first front-end is fabricated in GlobalFoundries 22 nm CMOS FDSOI process and fully characterized using high frequency probes. All DC and biasing pads are wire-boned to the PCB. The chip micrograph is shown in Figure 11. All corresponding building blocks are highlighted in the figure and the overall chip occupies a total area (including pads) of 1.4mm*1.2mm. Single-ended probes up to 110 GHz (T110A-GSG100) are used for both the RF and LO input signals, and differential probes up to 50 GHz (SP-I50-AD-GSGSG-02) are used to measure the output port and terminate the ISO port of the chip.

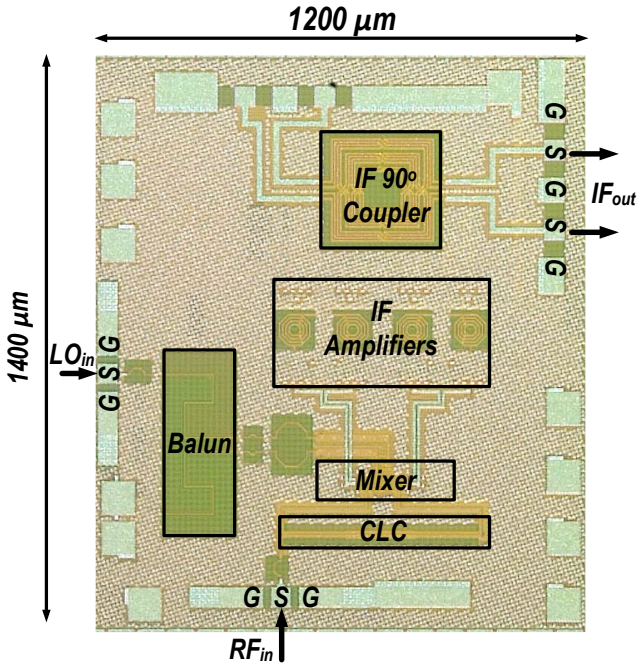

Figure 11 Chip micrograph

Signal generators are used to generate a continuous wave (CW) RF signals for the RF and LO ports. Since the signal generator cannot generate signals up to 100 GHz,

different source modules (frequency extenders) are used across different frequency bands. For example, VDI WR15SGX module is used for the frequency range 50-75 GHz, VDI WR12SGX module is use for the frequency range 60-90GHz, and OML S10MS and Agilent 83558A modules are used for the frequency range 75-110 GHz.

Next, different measurement setups and characterization results of the chip are presented. This includes gain, S11, NF, P1dB, IIP3 and modulation results.

3.1 Gain, Image rejection and Matching

The measurement setup used for gain and image rejection is shown in Figure 12. A signal generator (E8257D-567) is used (along with the corresponding source module) to generate a continuous wave (CW) signal as an RF input to the chip for measuring the gain. The LO port is driven by another source module followed by a power amplifier to generate sufficient LO signal power. The chip frequency down-converts and amplifies the signal,

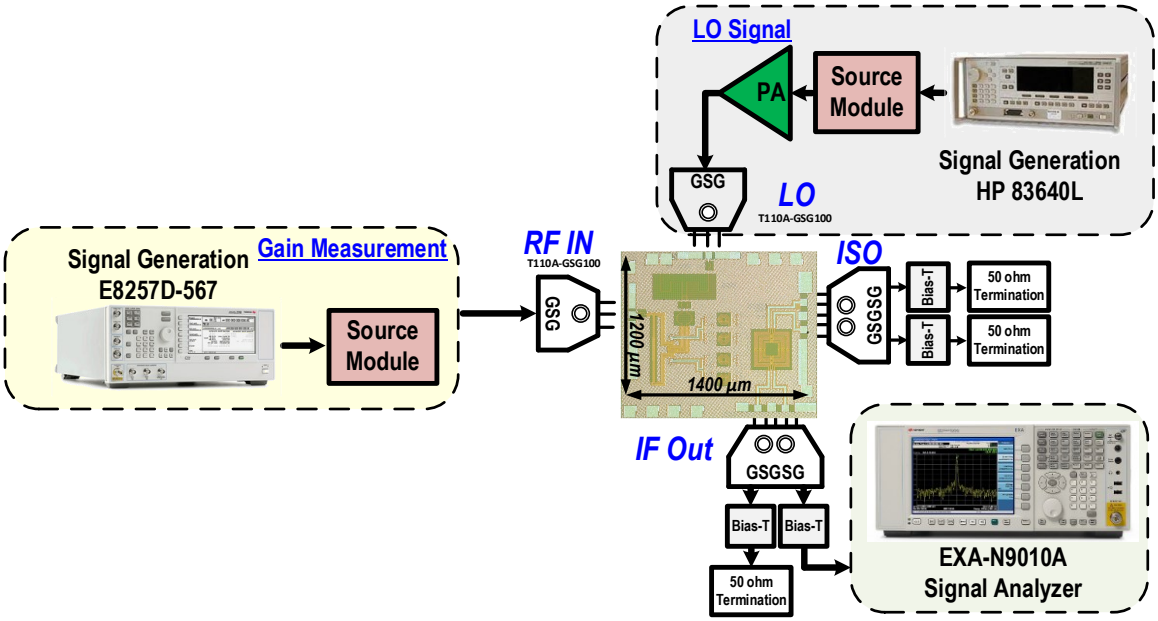

Figure 12 Gain and image rejection measurement setup

then, the output signal frequency and power are measured using a signal analyzer (EXA-N9010A). The overall performance (Figure 13a) shows a state-of-the-art 3-dB gain bandwidth from 43 to 97 GHz (77.14% fractional bandwidth) with a peak gain of 15 dB. The same setup is used to measure the image rejection capabilities of the chip. The desired signal followed by the image signals are used as the input to the chip and the output power difference is captured (Figure 13b). As mentioned in Section I, only two settings are used to cover the while bandwidth with image rejection ratio (IIR) of up to 32 dB.

The matching performance is carried out using Anristu 37397D VNA along with Anristu transmission-reflection module at the RF port of the chip. The S11 is measured with the LO port of the chip both switched on and off and the results are shown in Fig. 11b. The results indicate that the input matching using the coupled-line-coupler at the RF port is indeed resilient to the impedance presented to the coupled and through ports as can be observed by the good matching for both LO cases. The reason that the S11 (LO ON) is not

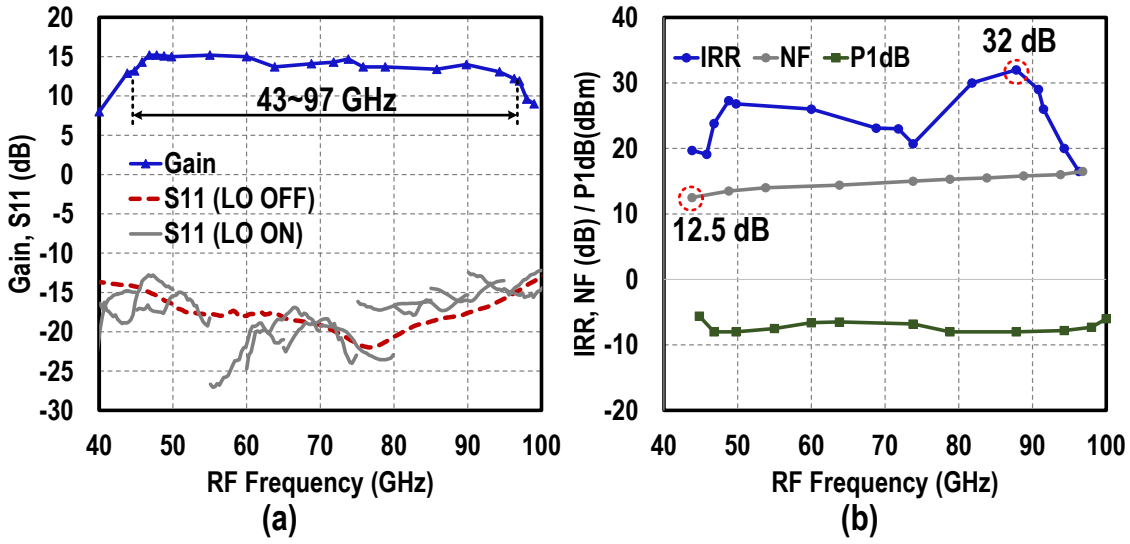

Figure 13 Measurement results (a) gain and S11, (b) IRR, NF and P1dB

very smooth is because three different modules (and power amplifiers) are used to drive the LO signal at different frequency ranges causing some slight LO driving power differences (in addition to having to re-land the input probes each time the LO driving equipment is changed, which will cause small variations to the measurements).

3.2 Linearity

The intermodulation performance of the receiver front-end is characterized by measuring the input referred third order intercept point (IIP3). One way to generate the two RF tones required for testing the chip is to generate two IF tones and combine them in the IF domain then up convert the combined signal to the RF domain using up-conversion mixers. This method might impose some inaccuracy in the measurements due the low linearity of the available up conversion mixers specially at such high frequencies (~ -19 dBm OP1dB) which might dominate the non-linearity performance especially when measuring high linearity chips. Although this effect can be relaxed by using an RF amplifier following the mixer, the measurement setup used to characterize the chip adopts combing the two tones in the RF domain rather than the IF domain. The block diagram of the measurement setup used for IIP3 measurement is shown in Figure 14 and the actual setups is presented in Figure 15. For example, in order to measure IIP3 at RF frequency at 75 GHz (with 3.8 GHz IF frequency), two signal generators followed by two source modules (VDI E-band module [60-90 GHz], and OML W-band module [75-110 GHz]) are used to generate two high frequency tones around 75 GHz frequency range, then power combiner (SWP-60390302-12-S1 [60-90 GHz]) is used for RF power combining. The output spectrum is observed using signal analyzer and the IIP3 value is calculated. Figure 16a shows the measured IIP3 versus two tone input separation with an in-band IIP3 of up

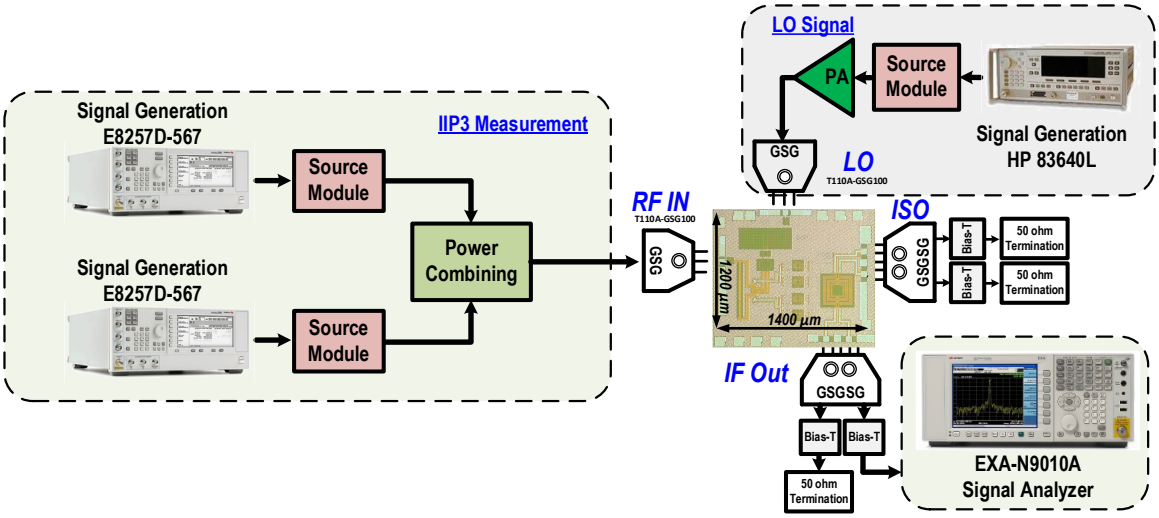

Figure 14 IIP3 measurement setup

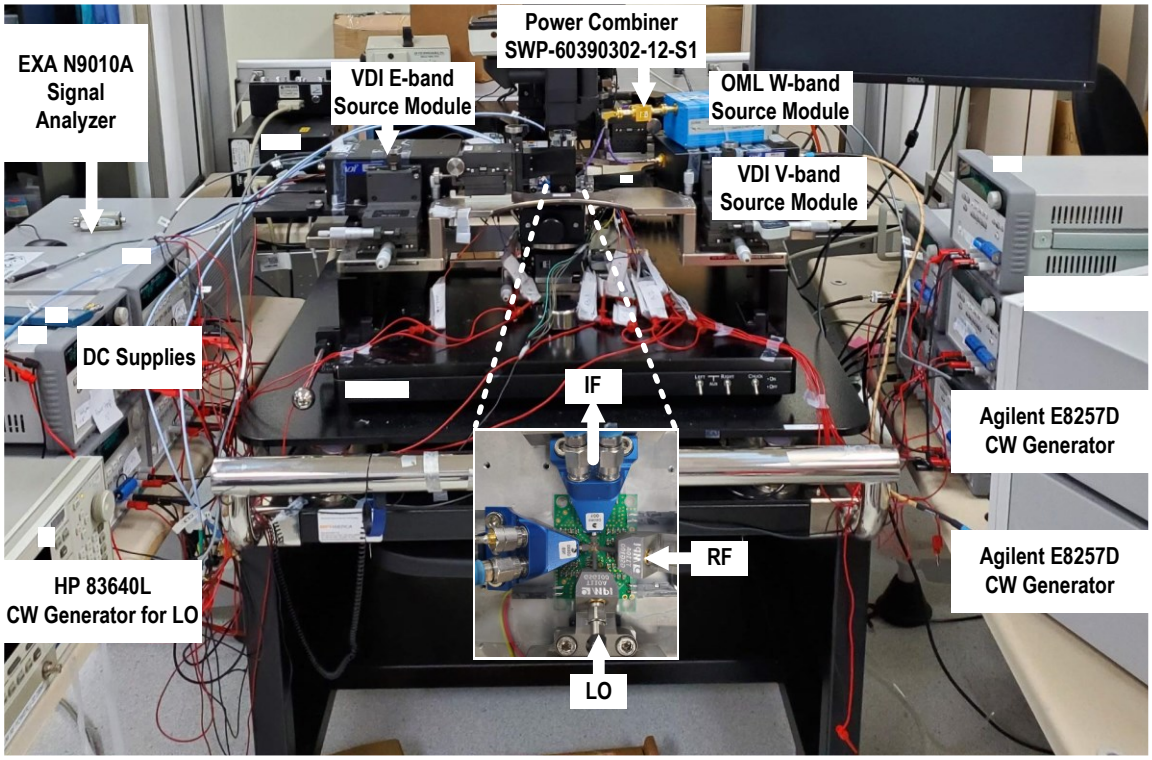

Figure 15 Actual IIP3 measurement setup

to 5.2 dBm (in this measurement one tone is fixed at the center of the IF band and the other tone is frequency swept and the IM3 component closer to the first tone is used to calculate

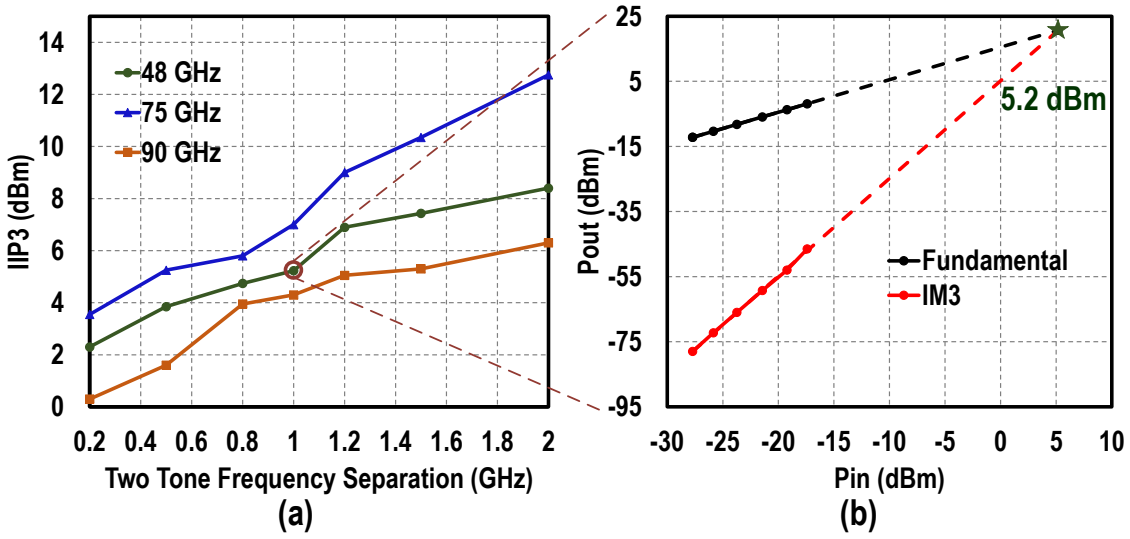

Figure 16 IIP3 results (a) versus two tone frequency separation, (b) versus input power.

the IIP3). Figure 16b shows the output fundamental and IM3 components versus the input power. Finally, the input compression point (Pin1dB) of the font-end is also characterized, the setup used is similar to the gain measurement setup (Figure 12) and the results are shown in Figure 13b.

3.3 Noise

Noise figure measurements is carried out using PXA signal analyzer (N9030A) with noise figure measurement capabilities and several noise sources for different frequency ranges. The noise sources used are Agilent (up to 50GHz), Quinstar QNS-FB15TV (50-75 GHz) and Quinstar QNS-FB12LW (75-110 GHz). The measurements show a noise figure performance between 12.5 to 16.5 dB across the frequency range (Figure 13b). Simulations are carried out to investigate the noise figure after every stage of the frontend, this is shown in Figure 17. After the CLC, the noise figure is equal to the loss of the coupler (Figure 4)

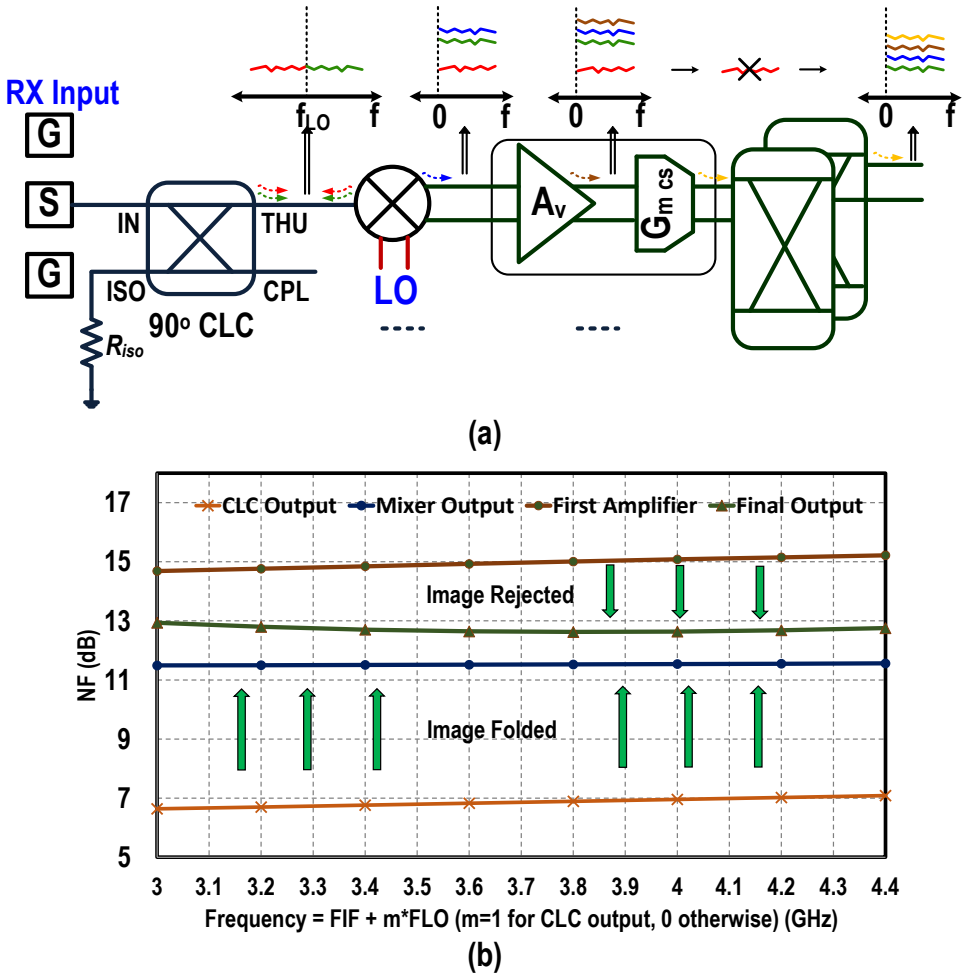

Figure 17 Simulated noise figure at different nodes.

in addition to the noise contribution from the loading components. After down conversion noise is added by the mixer switches in addition to folding of the image noise (and harmonics) to the desired frequency band. Next, the amplification stages add more noise, however, after the image rejection operation, the folded image signal is rejected.

3.4 Modulation

The implemented frontend supports high speed modulated signals (multi-Gbps data rate) required for future communication links. This is demonstrated by testing the chip with

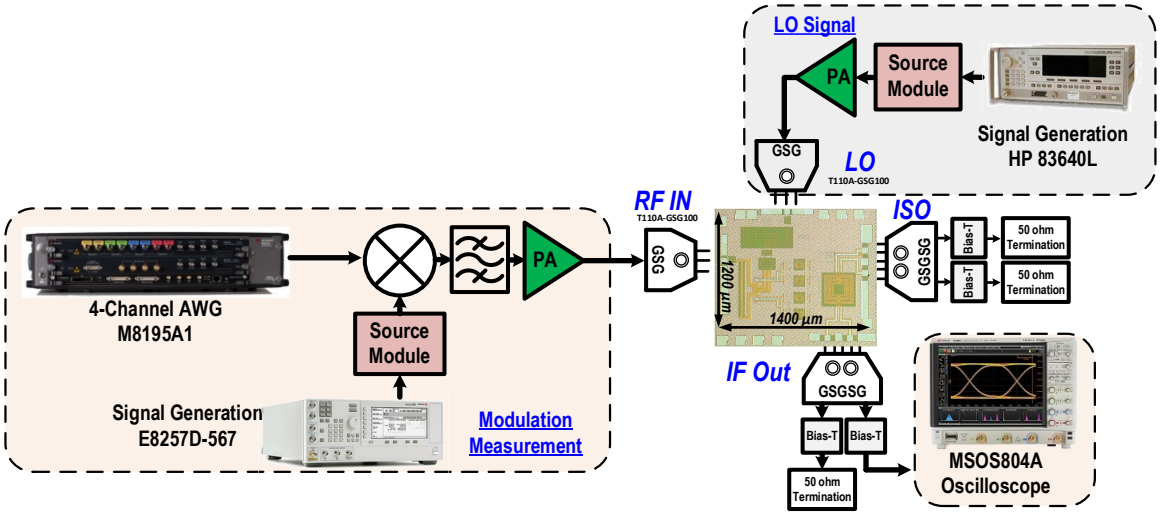

Figure 19 Modulation measurement setup.

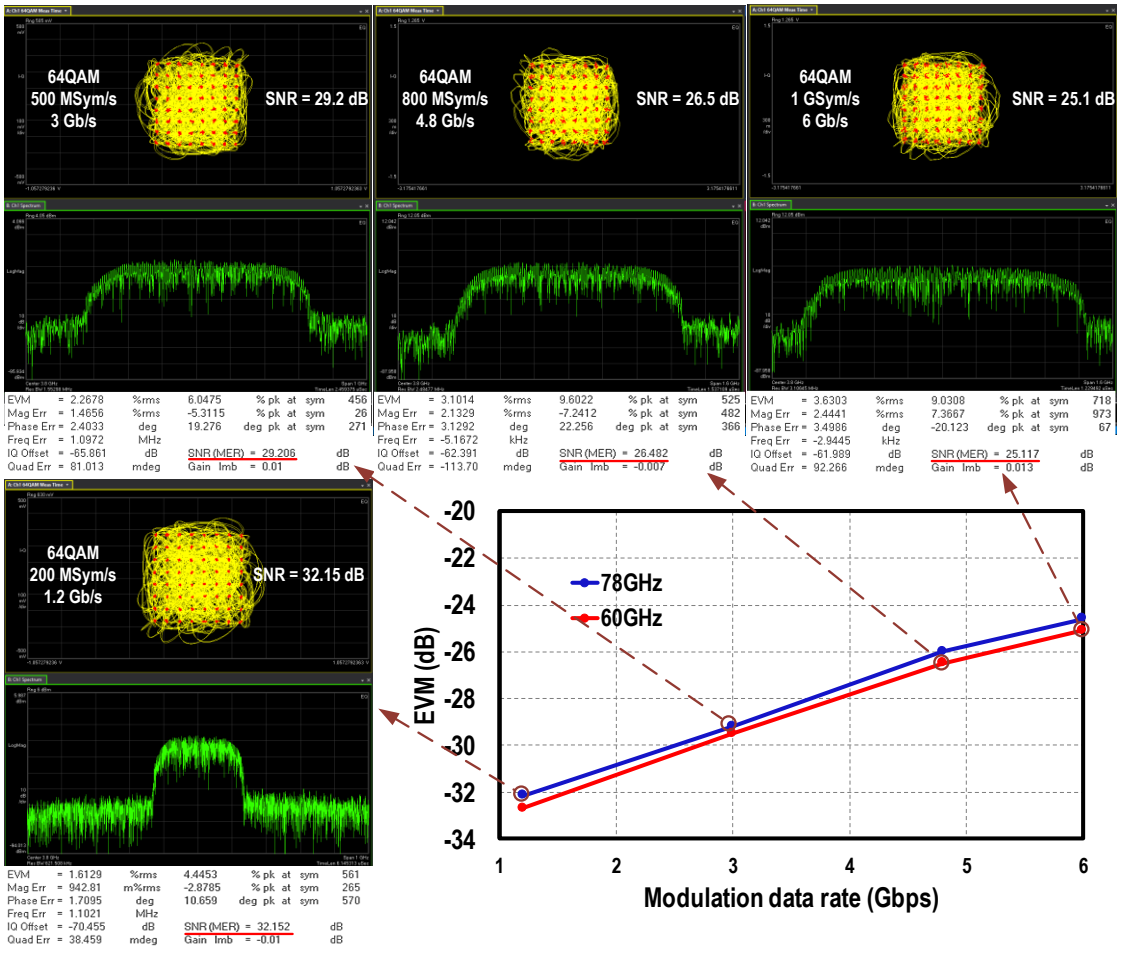

Figure 18 Modulation performance for different data rates

the modulation test setup shown in Figure 19. The modulated signal is generated using an

Arbitrary Waveform Generator (AWG) M8195A1 at low frequency (with an optional attenuator following the AWG), which is then upconverted to the desired RF frequency, bandpass filtered (to suppress the LO leakage and the up converted image signal) and finally amplified. This signal is applied as the input of the proposed frontend chip and the final output is demodulated using an oscilloscope (MSOS804A). Figure 18 shows the demodulated signal's constellation and EVM performance for different bit error rates. The front-end is able to successfully frequency down convert and amplify 64QAM signals with data rates up to 6 Gbps with an EVM of better than -24.6 dB.

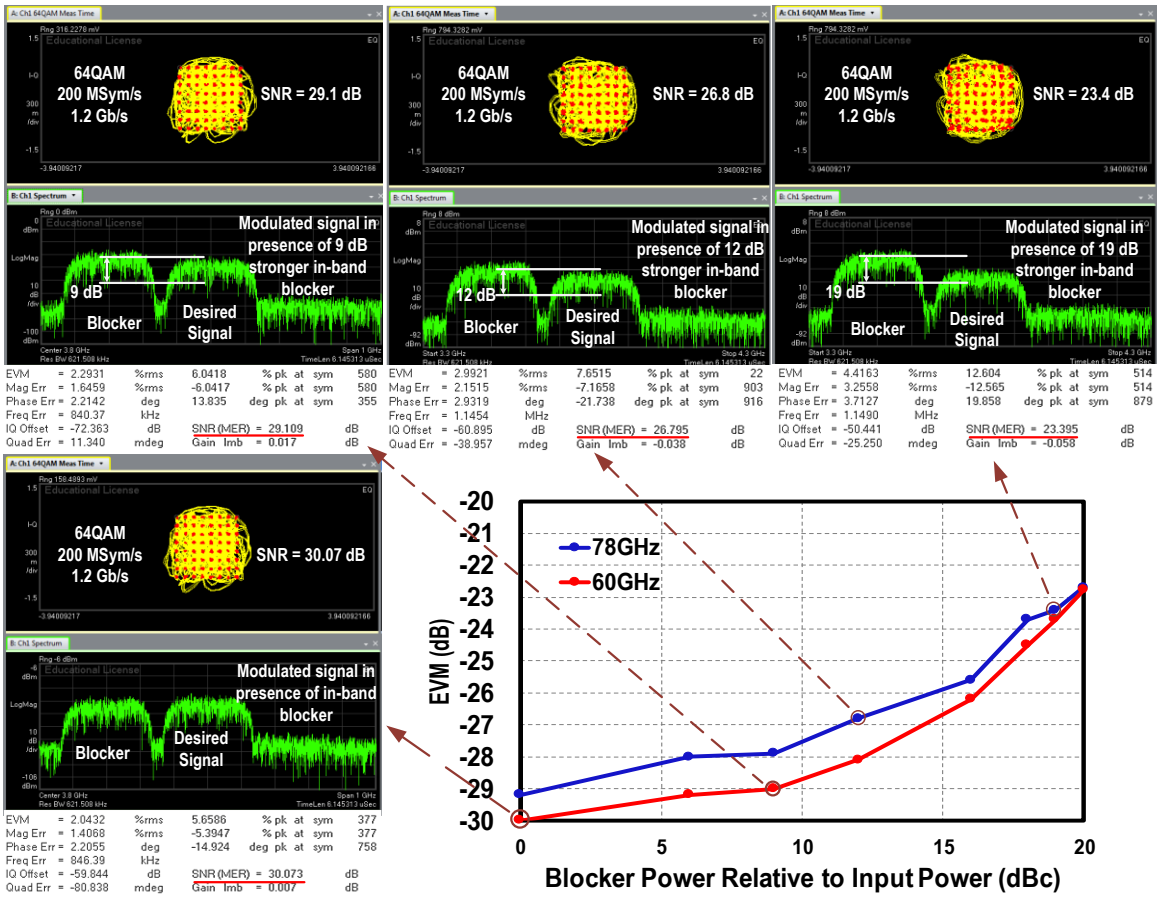

Figure 20 Modulation performance in presence of blocker signal

In addition to requiring high speed communication links, future EM environment will be congested and contested imposing a challenge on the frontend receivers to be able

to successfully demodulate the desired signal in presence of blocker signals, especially in-band blockers with no out of band frequency rejection applied. The case of large in-band blocker is demonstrated by applying the desired signal accompanied by an in-band blocker signal to the chip and demodulating the desired output signal. Figure 20 shows the EVM of the successfully demodulated desired signal versus the relative input power level. The results show a successful demodulation even in a presence of blocker signal of up to 20 dBc.

CHAPTER 4. CONCLUSION

This thesis presented an ultra-wideband mixer-first receiver frontend that covers a 77% fractional bandwidth from 43 to 97 GHz and supports a multi-Gbps wireless links mandated by the future high frequency communication systems. The frontend presents high IIP3 performance required for future MIMO and phased array systems, this is enabled using passive mixers and multi-gated transistors to implement the IF amplifiers. The proposed chip demonstrates an on-chip image rejection capability. The receiver front end in implemented and fabricated on GF 22nm CMOS FD-SOI process.

The overall result of the proposed ultra-wideband chip is compared with state-of-the-art high frequency CMOS designs and the comparison is shown in Table I. The proposed frontend achieves the highest carrier bandwidth (77.14% fractional bandwidth) amongst all CMOS ultrawide band designs. Additionally, the proposed design presents a state-of-the-art linearity performance achieving an IIP3 of 1.6dBm to 5.2dBm. Furthermore, on-chip image rejection capability is demonstrated by the proposed receiver frontend while not presented by any other design. Besides, compared to state-of-the-art designs shown in Table I, this work is the only to demonstrate demodulation performance of the desired signal with and without the presence of large blocker signal.

Table 1 – Comparison with the state-of-the-art

		CMOS Node	Operation Freq. (GHz) (Fractional BW %)	IIP3 (dBm)	Pin1dB (dBm)	Gain (dB)	NF_{DSB} (dB)	Power (mW)	On chip image rejection (dB)	Modulation	Architecture
Mixer First Topology	**This Work**	**22nm FDX**	**43 ~ 97 (77.14%)**	**1.6 ~ 5.2[4]**	**-5.6 ~ -8**	**12~15**	**12.5 ~ 16.5**	**36**	**17~32**	**64QAM 1.2 to 6 Gbps (-32.7 to -24.6 dB)[5]**	**Mixer-first low-IF down conversion**
	L. Lotti [1-2] ISSCC '18 JSSC '20	28nm	74~94 (26.5%)	N/R	-26.5 ~ -18	21~26	8.2 ~ 10.8	8	N/A	N/R	Mixer-first direct conversion
			70 ~ 100 (35.3%)	N/R	-24 ~ -16.8	19.5~25.3	8 ~ 12.7	12	N/A	N/R	
	Moroni [3] RFIC '10	65nm	49 ~ 67 (31.0%)	N/R	-12	10-13	11 - 14	14	N/A	N/R	Mixer-first direct conversion
LNA First Topology	Vigilante [5] JSSC '17	28nm	68.2~96.5 (34.4%)	-24 ~ -18[1]	-28.1	29.6	6.4-8.2[3]	31.3	N/A	N/R	Sliding IF heterodyne
			65.8~ 96.5 (37.9%)	-18 ~ -12[1]	-12.3	18	7.8-9.8[3]	11.7	N/A	N/R	
	Vigilant [7] ISSCC' 18	28nm	68.85~81.75 (16.7%)	N/R	-25	28	8.3 ~ 10	77.3[2]	N/A	N/R	Coupled-RTWO-based subharmonic receiver
	Kundu [8] JSSC '15	45nm SOI	45~66 (37.8%)	N/R	-27	23.2-26.2	5.5 ~ 10[1]	30	N/A	N/R	Active mixing direct conversion
			48~67 (33.0%)	N/R	-28	17.2-20.2	7.7 ~ 12[1]	14	N/A	N/R	
	Khanpour [10] JSSC '08	65nm	75~91 (19%)	N/R	-16	13	5.5~7.5	89	N/A	N/R	Direct Conversion
	Guermandi [11] ISSCC '15	28nm	75~83 (10%)	N/R	-32.5	35	<7	59	N/A	PMCW	Direct Conversion

NR: Not Reported, [1] Estimated from figures, [2] Receiver power, [3] Up to 90 GHz, [4] At 0.5GHz two tone offset, [5] With equalization

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