WIDEBAND CIRCUITS AND ANTENNA DESIGNS FOR MM-WAVE/5G PHASED ARRAYS

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WIDEBAND CIRCUITS AND ANTENNA DESIGNS FOR MM-WAVE/5G PHASED ARRAYS

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To my parents and Jiho, for always believing in me.

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SUMMARY

The objective of this work is to present the performance and feasibility of wideband circuits and antennas for future mm-Wave phased array systems.

Chapter 1 introduces the motivation of this research, first explaining the desire to operate at higher frequency regimes. Then focus is directed on the rich application spaces at mm-Wave frequencies and the corresponding need for wideband, compact, and fully integrated system-on-chip (SoC) solutions. A brief study of advanced node commercial silicon processes is also examined to demonstrate the increasing feasibility of implementing the aforementioned SoC solutions on silicon.

Chapter 2 presents a design methodology of a novel ultra-compact, low-loss, and wideband mm-Wave Wilkinson Power Divider (WPD). Careful study and analysis reveal optimal and necessary design parameters and equations in terms of the coupling and mutual inductances within the structure, yielding a device that is competitive with existing literature. This work was presented in *2019 IEEE MTT-S International Microwave Symposium* [1].

Chapter 3 first introduces the operation principle of spiral antennas (SA). The unique properties of SAs that make them great candidates for use in future mm-Wave phased arrays are explored. The rest of this chapter discusses the design, analysis, and results of an octagonal 4-arm Archimedean SA. This work was presented in *2019 IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting* [2].

Lastly, Chapter 4 provides closing remarks and discusses potential future work.

CHAPTER 1

INTRODUCTION

1.1 Motivation

The current frequency spectrum is both incredibly diverse and crowded, facilitating mobile communications to providing detailed imaging for radio astronomy. In particular, the RF spectrum, defined from 225 MHz to 7.125 GHz by the National Telecommunications and Information Administration (NTIA), is unquestionably crowded, providing no leniency for spectral leakage and strict windowing requirements as set by the Federal Communications Commission (FCC) [3]. A peek at the NTIA/FCC spectrum allocation chart from 2016 shows the plethora of applications, as shown in Figure 1.1.

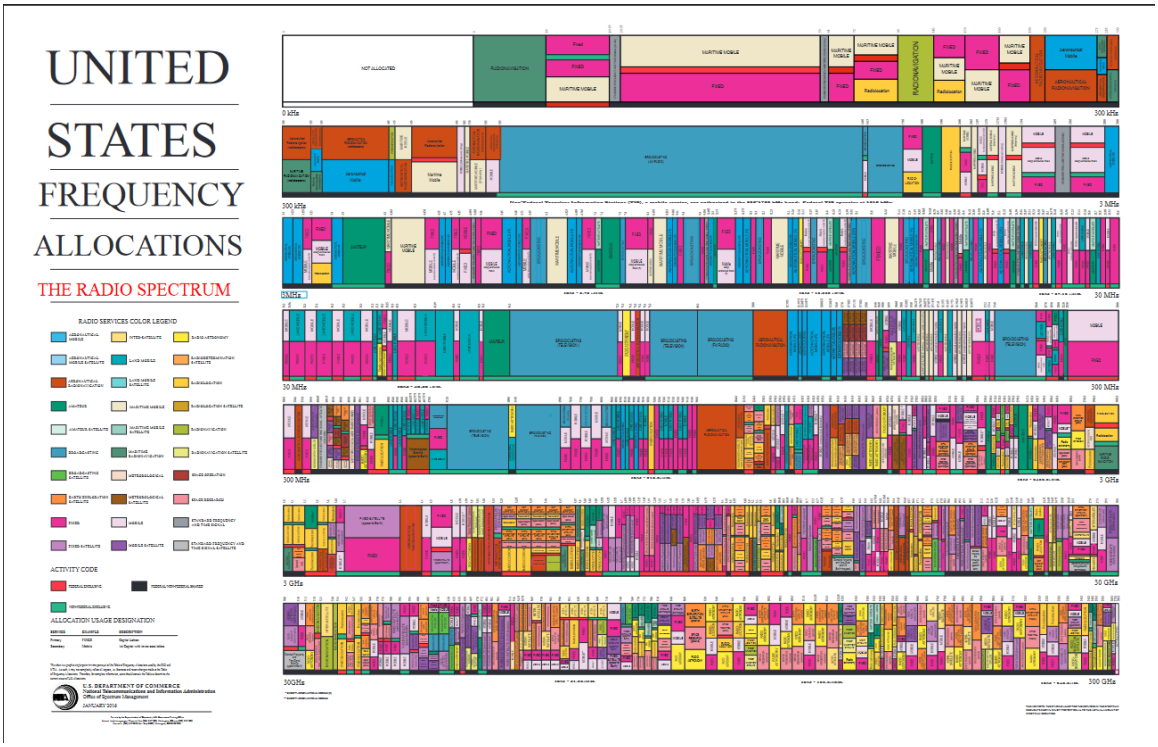

Figure 1.1: The frequency allocation spectrum chart determined by the FCC, 2016 [4].

However, technology plays a ubiquitous role in our everyday lives, resulting in a larger

number of devices and thus more users in a given frequency band. Consequently, this causes the crowding that is forcing industries to look at less populated frequency spectra. Figure 1.2 shows an example of the different types of everyday devices that can be subscribed to a base station phased array; frequency congestion could be caused should there be an extreme amount of devices within close proximity, say at a live music venue concert or an extremely crowded urban environment.

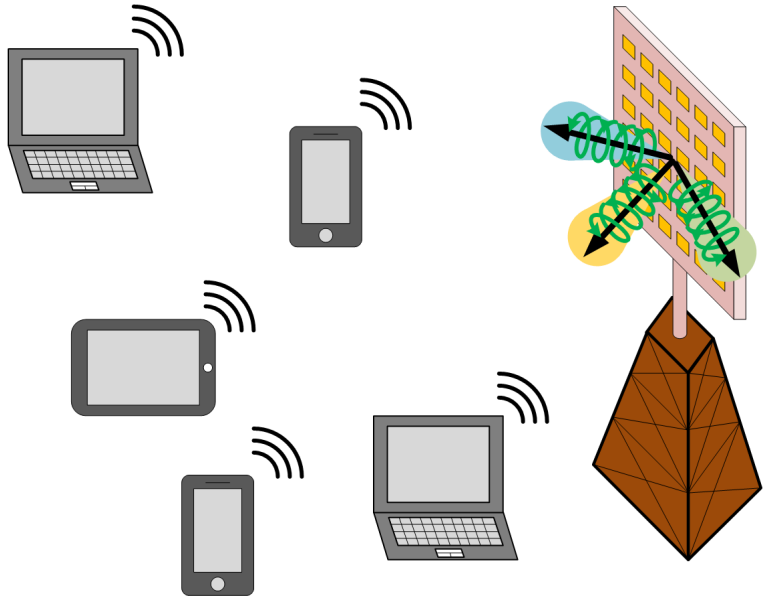

Figure 1.2: A typical phased array base station system with a variety of subscribed devices.

As a result, the FCC has unlocked access towards the higher frequency regime, namely the mm-Wave frequency bands loosely defined above 30 GHz. Recently, in 2020 the FCC has auctioned off the spectrum allocation in the higher frequency regimes, such as the 37 GHz, 39 GHz, and 47 GHz bands. Cellular companies like Verizon, AT&T, and T-Mobile have spent collectively over $7,558,703,201 to bid for the coveted spectrum licenses, underscoring the demand for more available spectra [5].

However, as shown in Figure 1.3, the proposed 5G/mm-Wave network contains many bands that are not universalized across the world. Moreover, countries differ on which bands to use, potentially causing issues on international compatibility. This could have profound impacts on downstream manufacturing as certain chipsets would not function

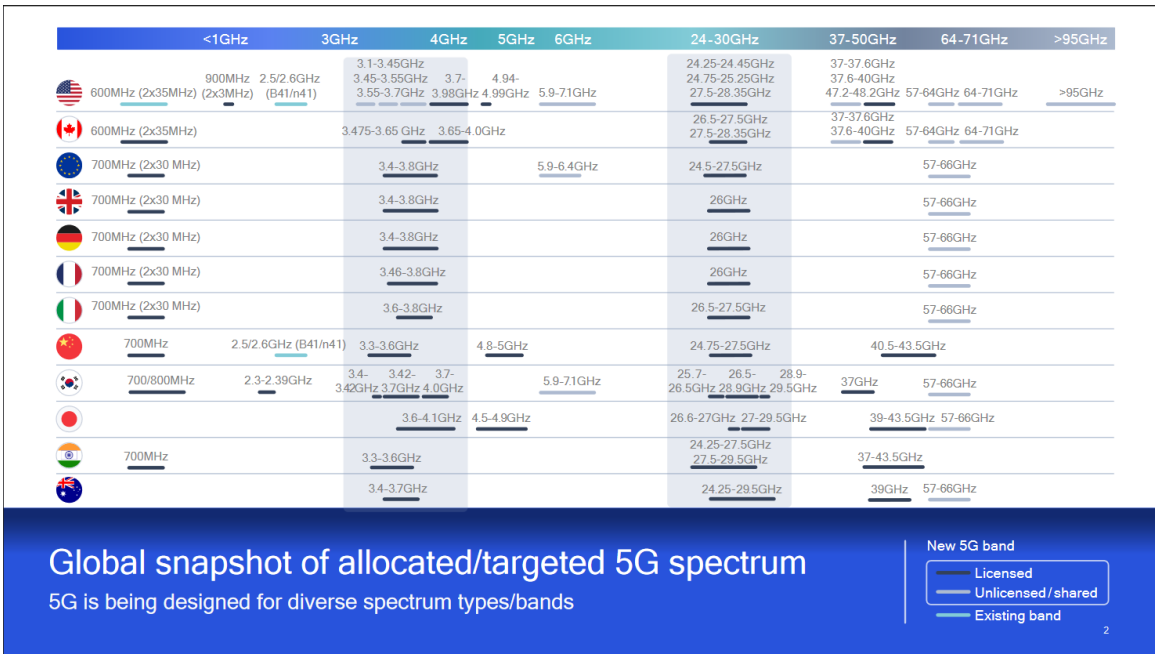

Figure 1.3: Proposed 5G/mm-Wave frequency bands per country [6].

as desired depending on the user's physical location. One solution to this issue would be to standardize the frequency bands internationally, but this option has proved to be difficult as countries worldwide are keen on pioneering the standards as quickly as possible or have been struggling to successfully implement new mm-Wave/5G networks. One way to resolve this issue would be to design multi-band or wideband electronics as they can cover multiple target frequency bands [7, 8, 9], obviating the need for different chipsets per country.

Coupled with more flexibility and freedom within these newly allocated frequency bands, the advent of mm-Wave/5G technology has spurred vast development and clearance for high-speed wireless communications, international roaming, radar, imaging, and remote sensing applications [10, 11, 12, 13, 14, 15], as shown in Figure 1.4. However, the larger path loss at these higher frequency regimes due to increased atmospheric absorption necessitates the use of some power combining to improve the EIRP of the overall system. Such common ways include utilizing improved low-loss power combining backend electronics architectures or propagation-mode power combining beyond the antenna, namely

phased array or multiple-input-multiple-output (MIMO) beamforming systems.

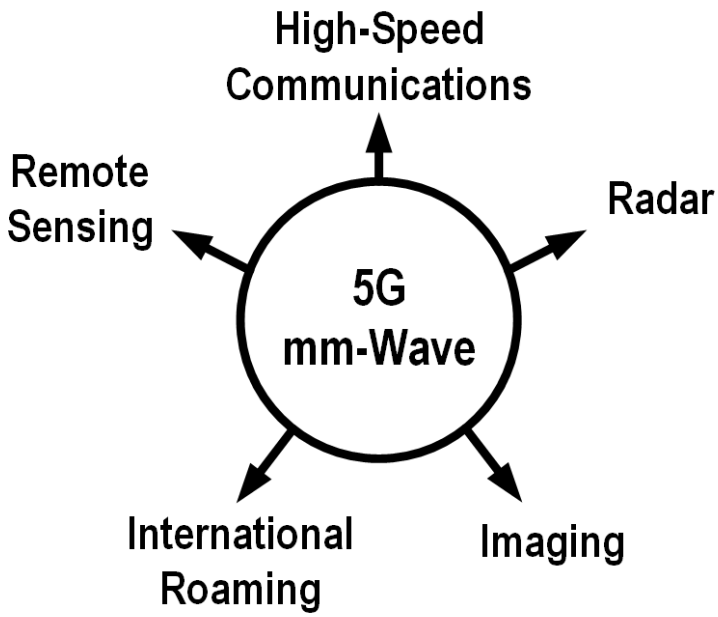

Figure 1.4: Diverse application spaces for upcoming mm-Wave spectrum.

As a result, in order to efficiently and successfully implement these new mm-Wave/5G technologies, the goal is to develop low-loss and wideband components that can be used within phased array or MIMO beamforming systems. Due to the large scope of MIMO beamformers, this thesis will limit the discussion to mm-Wave/5G phased array systems, which is discussed in the following section.

1.2 Phased Arrays

While the phased array concept has seen historic success at the lower frequency regimes, it has played a crucial role in facilitating mm-Wave systems thanks to the enhanced EIRP seen by utilizing multiple antennas. One example of a traditional system architecture of a phased array utilizing a corporate feed network is shown in Figure 1.5.

Behind each antenna is its own series of backend electronics that include (but not limited to) amplifiers, phase shifters, mixers, filters, and power dividers/combiners. The area consumed by these backend components can quickly add up, forcing the electronics foot-

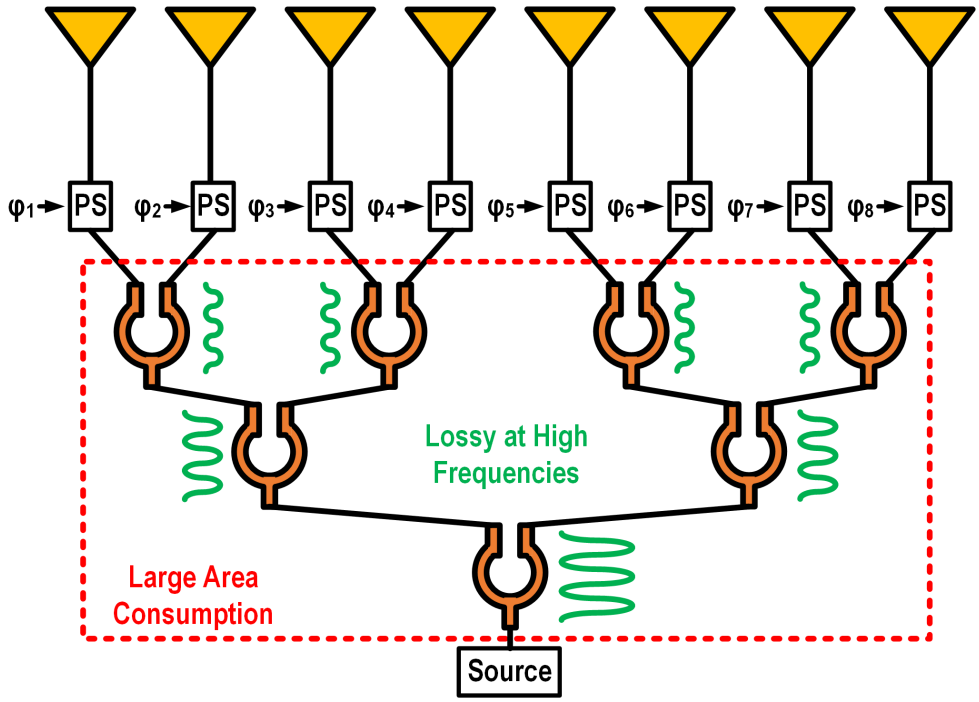

Figure 1.5: Traditional phased array system implementation using corporate feed networks.

print behind each antenna element to increase, potentially requiring greater than $\lambda/2$ or λ spacing between antenna elements and causing increased grating lobe levels. While at RF frequencies antennas are typically the limiting factor in physical size as they are much bigger than their backend electronics, one must still take careful consideration in the layout of the phased array system.

It should come as no surprise that these phased array systems are easily scalable. However, there are several factors one must consider with increasing number of elements within an array. The financial cost of building these phased arrays can grow exponentially with increasing number of elements, as maintenance of large-scaled phased arrays also proportionally become progressively cumbersome. While the Cobra Judy phased array system in Figure 1.6 operates at low RF frequencies, it reminds us that the cost to build and upkeep these large scale arrays can be extremely expensive, as a single broken element within a large phased array can have profound impacts on the overall system performance.

The design complexity in terms of signal distribution also becomes increasingly dif-

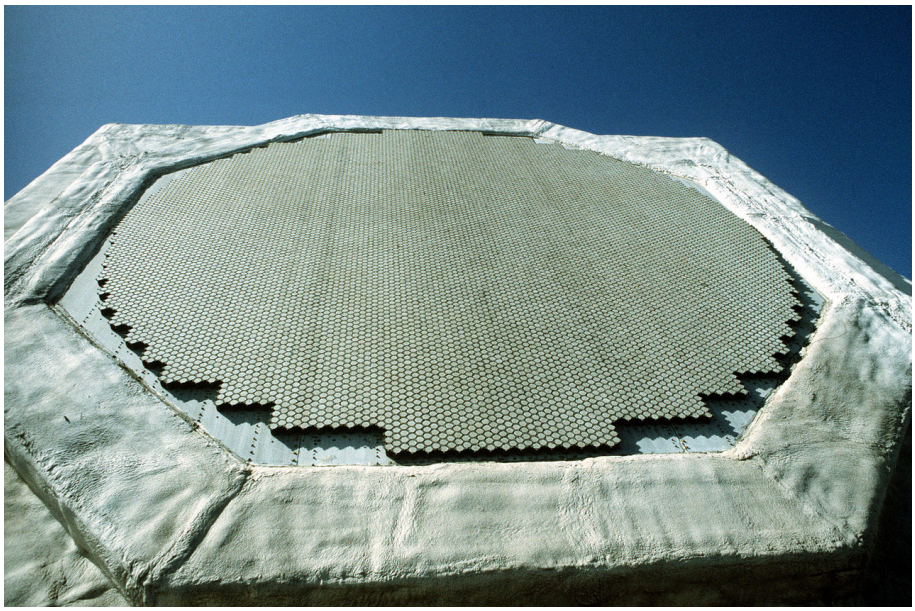

Figure 1.6: The AN/SPQ-11 Cobra Judy phased array system on the USNS Observation Island missile range instrumentation ship [16].

ficult with larger number of elements, potentially requiring more stages of amplification or loss-compensation within each unit cell, which in turn uses more area and power, increasing costs. The schematic and die photo of a 77 - 81 GHz SiGe receiver in Figure 1.7 demonstrates the multi-stage amplification to compensate for the loss at higher mm-Wave frequencies [17]. Not only will the incoming signals face atmospheric attenuation until reaching the receiving antenna port, but they will also incur insertion losses from at least four different power combiners, all adding design complexity to compensate for these losses.

As a result, there is a tradeoff in the mm-Wave phased array design space between the antenna and its driving electronics. While on one hand the phased array implementation is highly desired to improve the overall system EIRP, having a larger number of elements can quickly add system complexity and limit the benefits gained from utilizing a phased array architecture. Despite this, we are starting to see a compromise between these two opposing factors with improved silicon technologies, as discussed in the next section.

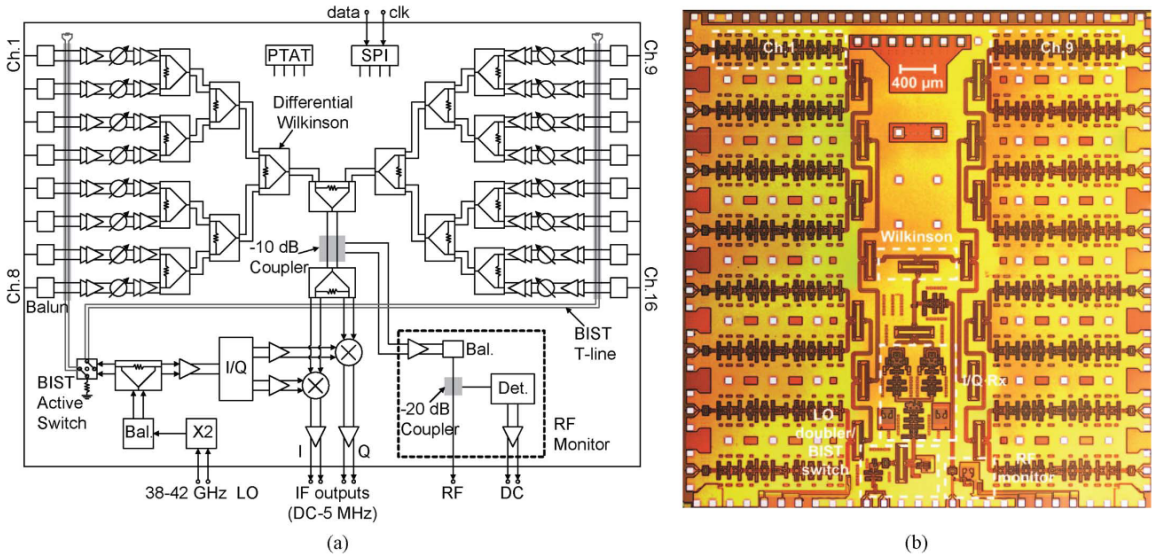

Figure 1.7: A 77 - 81 GHz 16-element phased array receiver implemented in 130nm SiGe [17].

1.3 PCB and Commercial Silicon Technologies

Printed circuit board (PCB) technology has dominated the early development of RF electronics and hardware, due to their relative ease of fabrication and accessibility. State of the art PCB manufacturers can achieve trace width/spacing tolerance levels within a couple of thousandths of an inch and board thicknesses that can be as thin as several hundredths of an inch. This alone has enabled a plethora of both passive and active RF circuit designs. However, the drawback with PCB technology is that these small features are becoming extremely difficult to fabricate reliably and consistently. Moreover, surface mount components for resistors, capacitors, and inductors are extremely large and lossy at higher frequencies. Furthermore, the latter two devices may have self-resonance frequencies (SRFs) that are close to the operation frequency, which is not recommended nor desired for overall performance.

On the other hand, silicon (Si)/silicon-germanium (SiGe) technologies have continued to scale down in size while improving the performance of the device. The transistor cut-off/transit frequency, f_t, and maximum oscillation frequency, f_{max}, increased throughout

the last several decades, enabling remarkable advances in a wide variety of amplifiers, oscillators, and much more. Si/SiGe technologies also offer on-chip resistors, capacitors, and inductors, which are directly integrated within the active area. Unlike their PCB counterparts, the latter two components are more amenable to higher frequencies of operation as they have more forgiving SRFs and the designer has the freedom to determine the size and value of these components, rather than buying COTS components with limited options.

As Si/SiGe technology continues to advance, mm-Wave phased arrays become increasingly realizable on these platforms. Thus, this thesis aims to show the coming together of these two topics to provide a compact SoC that can address the issues and motivations brought up earlier from Chapter 1.

CHAPTER 2

LOW-LOSS ULTRA-COMPACT WIDEBAND WILKINSON POWER DIVIDER

As discussed in Chapter 1, a strong emphasis is placed on low-loss and highly integrated mm-Wave passive power combiners/dividers for signal distribution in large phased arrays. However, these devices typically exhibit lossy performance and consume large area that degrade and limit system level performance like bandwidth, gain, and efficiency. To address these challenges, an ultra-compact and wideband Wilkinson power divider (WPD) utilizing artificial multi-section transmission lines realized within one inductor footprint is proposed in this chapter to achieve substantial size reduction, low-loss performance, and wideband operation.

2.1 Introduction

Looking back at Figure 1.5, an eight antenna element phased array will require seven power dividers/combiners within a corporate feeding network. Thus, the series path losses incurred from the single port to any antenna element will be at least 9 dB, either requiring an extremely high power (and expensive) source or compensation in downstream backend electronics to boost and recover the desired power/EIRP. At the same time, having seven power dividers/combiners can take up a lot of area, especially if the component is not compact. Thus, a proof-of-concept design for the proposed circuit is implemented in 22nm FD-SOI CMOS process. The total area of the ultra-compact design is 0.0361 mm^2 (0.00064 λ^2 at 40 GHz), achieving greater than 1.5× size reduction compared to the state-of-the-art. It also attains low additional insertion loss of 1.17 dB at 34 GHz with minimal phase mismatch (less than 3°) and amplitude imbalance (less than 0.2 dB) between 15 – 55 GHz, enabling future multi-band and multi-standard 5G applications (24, 28, 37, 39, and 43 GHz).

2.2 Transmission Line-based WPDs

A traditional implementation of the WPD employs lossless λ/4 transmission lines [18], as shown in Figure 2.1. While this is its most straightforward implementation, λ/4 transmission lines pose a significant challenge as they are inherently large and narrowband.

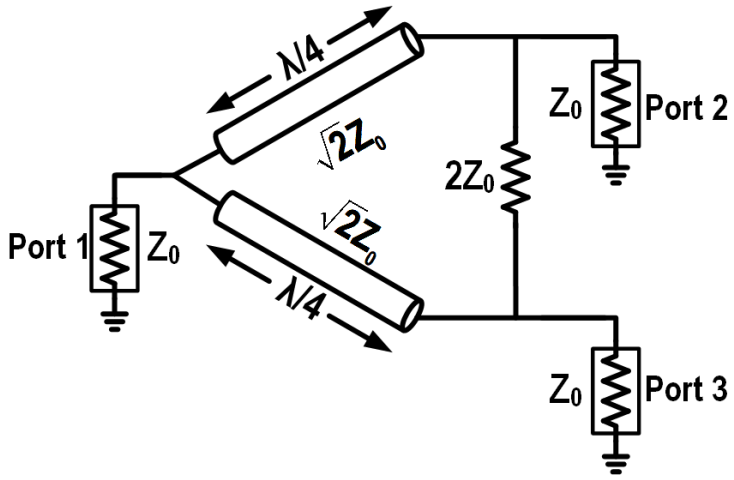

Figure 2.1: Lossless transmission line model of WPD.

To mitigate these performance constraints, artificial transmission lines are normally used to extend the passband and can be synthesized using lumped element inductors and capacitors (LC) [19]. Nevertheless, it requires a large area to cascade multi-section LC elements and causes extreme loss at mm-Wave in practice. A general artificial transmission line model of the WPD can be extended to a multi-section lumped-element model using n-cascaded π-model lumped-element unit cells, as shown in Figure 2.2.

Port 1 is defined to be the input port, while Port 2 & Port 3 are the output dividing ports. Assuming a lossless transmission line, the unit cell inductance and capacitances can be written as:

$$\begin{aligned} \mathrm{L}_{\pi(\mathrm{n})} &= \frac{\sqrt{2}\mathrm{Z}_0}{\omega} \\ \mathrm{C}_{\mathrm{n}} &= \frac{1}{2\sqrt{2}\mathrm{Z}_0\omega} \end{aligned} \tag{2.1}$$

where ω is the operating frequency and Z_0 is the characteristic impedance of the loss-

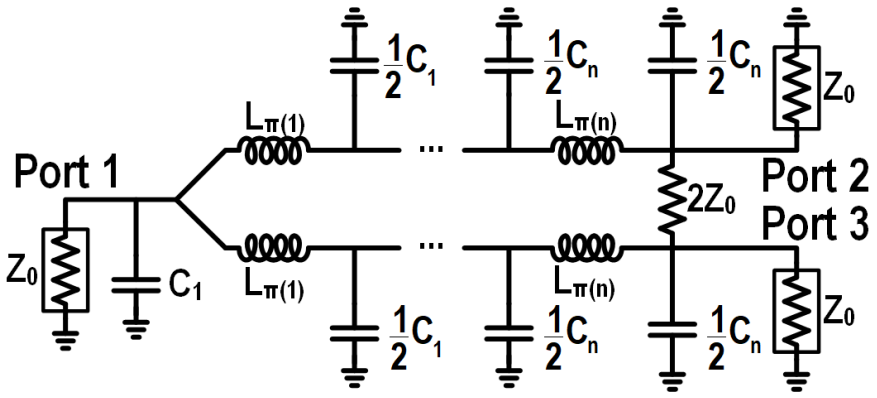

Figure 2.2: Equivalent lumped-element circuit model of WPD using n-cascaded multi-section transmission lines.

less transmission line. So long as the desired $\lambda/4$ phase response is achieved through n-cascaded π-model lumped-element unit cells, the artificial transmission line can replace the distributed transmission line elements in the traditional WPD.

2.3 Folded Inductor-based WPD

Utilizing artificial transmission lines is again a straightforward approach to designing WPDs, with the added benefit of extending the passband region due to the cascading of unit cell sections. At the same time however, this multi-section lumped-element model utilizes up to n inductors, which can take substantial area. To provide significant area reduction without sacrificing the benefits of artificial transmission lines, cascaded inductors and shunt capacitors are embedded within one inductor footprint for the proposed WPD. A similar approach has been utilized in [20, 21, 22], for other passive structures such as the rat-race coupler. The circuit model of the two section WPD is shown in Figure 2.3, where the values of the capacitor C_n and port definitions are the same as those in Figure 2.2.

The 3D EM model of the equivalent circuit model for the proposed WPD are shown in Figure 2.4. Note that nodes 1 to 6 are respectively labeled in both the EM model and the equivalent circuit model. The self-inductance and magnetic coupling of the adjacent inductor traces are modeled through mutual inductance coefficients M_1, M_2, and M_3. However,

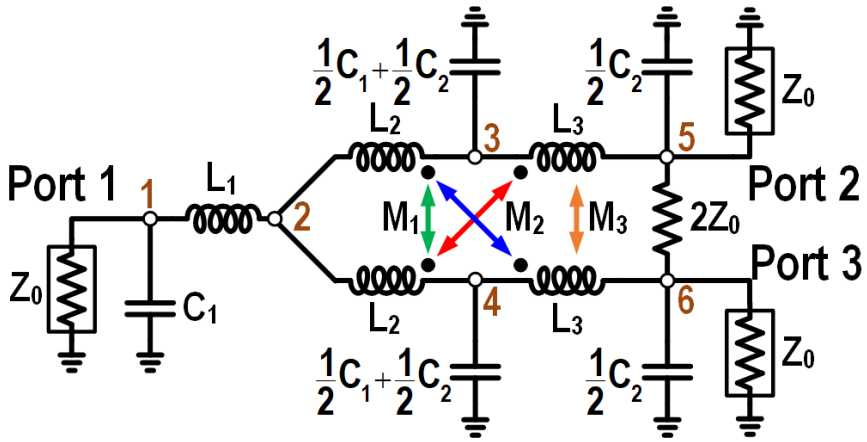

Figure 2.3: Proposed equivalent circuit schematic of folded inductor-based WPD.

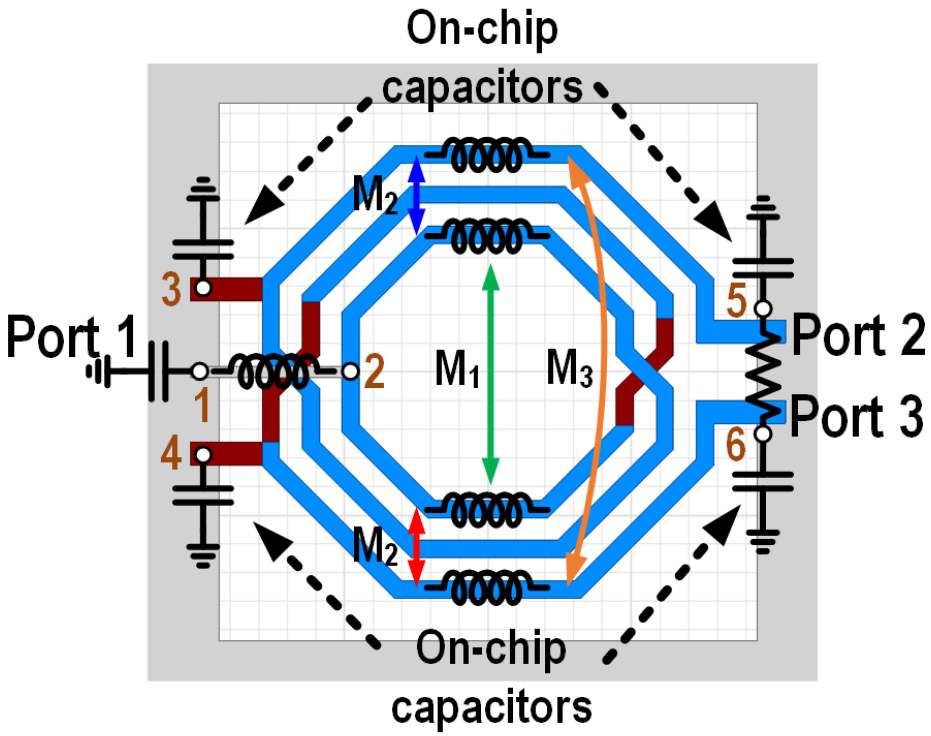

Figure 2.4: 3D EM model of the proposed folded inductor-based WPD.

the M_3 mutual inductance contribution is negligible as the two inductors L_3 are located far from each other with negligible inductive coupling.

The following sub-sections explain the design equations used to implement the proposed WPD in Figure 2.3. Even-mode and odd-mode analyses are then applied for the derivation.

2.3.1 Even-Mode Analysis

The desired operation mode of the WPD is its even-mode. The even-mode excitation signals (V_e, I_e) are applied to Port 2 & Port 3, while Port 1 is terminated with Z_0 (50 Ω), as shown in Figure 2.5. Since the circuit is symmetric about the centerline, the single-ended impedance of Port 1 can be rewritten as two parallel resistors of $2Z_0$ and the shunt resistor of $2Z_0$ can be split into two series resistors of Z_0 impedance each with an open circuit in between.

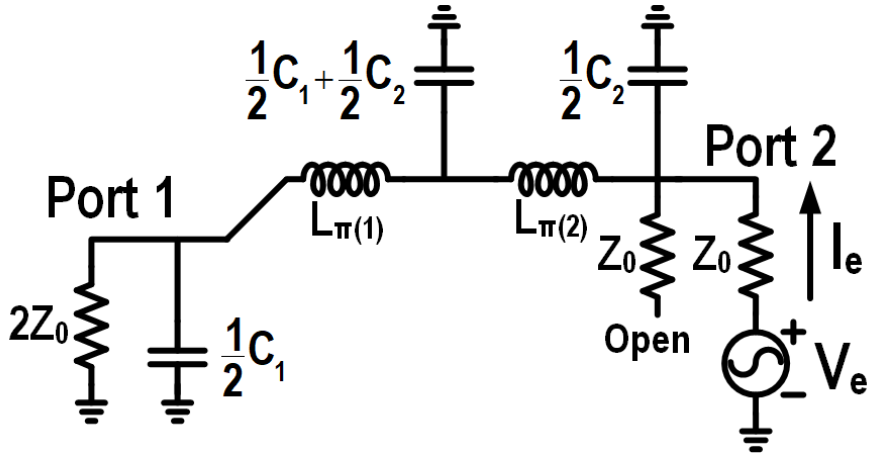

Figure 2.5: Half-circuit representation of the nominal 2-section equivalent schematic for even-mode operation analysis.

Furthermore, the π-model inductors in Figure 2.5 can be replaced with their respective artificial TL inductances as denoted in Figure 2.3, resulting in Figure 2.6 for the half-circuit even-mode representation of the proposed folded inductor-based WPD.

Since no even-mode currents flow through L_2& L_3 due to the open circuit condition, there are no mutual inductances M_1 and M_2 or coupling to consider in this even-mode analysis. As a result, the input impedance looking from Port 2 in both the nominal and proposed half-circuits is the following:

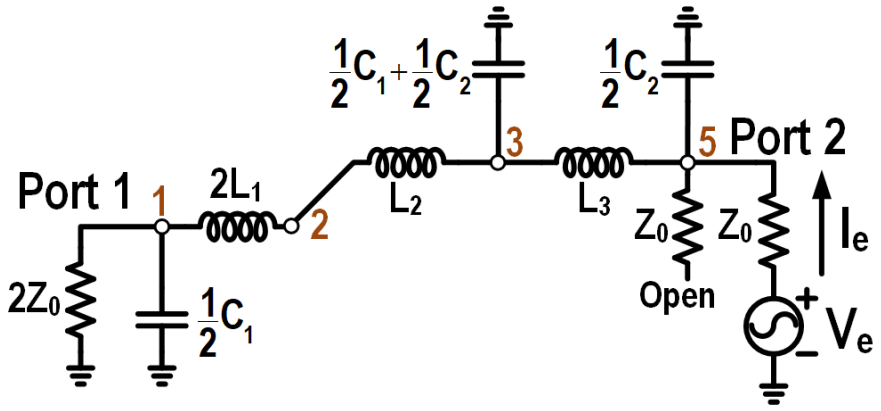

Figure 2.6: Half-circuit representation of the proposed folded inductor equivalent schematic for even-mode operation analysis.

$$\left(2Z_0||\frac{1}{\frac{1}{2}sC_1}+sL_{\pi(1)}\right)||\frac{1}{s\left(\frac{1}{2}C_1+\frac{1}{2}C_2\right)}+sL_{\pi(2)}$$
$$=\left(2Z_0||\frac{1}{\frac{1}{2}sC_1}+s2L_1+sL_2\right)||\frac{1}{s\left(\frac{1}{2}C_1+\frac{1}{2}C_2\right)}+sL_3 \quad (2.2)$$

2.3.2 Odd-Mode Analysis

The odd-mode excitation signals (V_o, I_o) are then applied to Port 2 & Port 3, while Port 1 is terminated with Z_0 (50 Ω). A virtual ground is formed along the symmetric centerline of the circuit, allowing us to split the shunt resistor of $2Z_0$ into two series resistors of Z_0 each while tying a virtual ground in between them. In addition, a virtual ground can be tied to the power dividing node, shorting Port 1 and the π-model capacitor to ground, effectively tying the inductor $L_{\pi(1)}$ and $2L_1$ in the nominal and proposed circuit to ground, respectively, as shown in Figure 2.7.

However, mutual inductances must be considered in the proposed design as the odd-mode excitation current, I_o, along the half-circuit symmetry will induce magnetic coupling among the inductor traces. Its respective equivalent circuit is shown in Figure 2.8.

The odd-mode currents at node 3 can be divided into two currents, I_1 & I_2. Their relationship with $\beta = I_2/I_1$ can be defined by inspecting the impedances of the inductors:

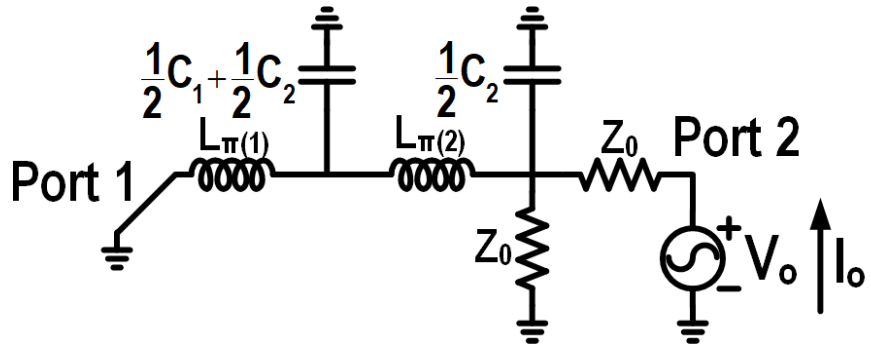

Figure 2.7: Half-circuit representation of the nominal 2-section equivalent schematic for odd-mode operation analysis.

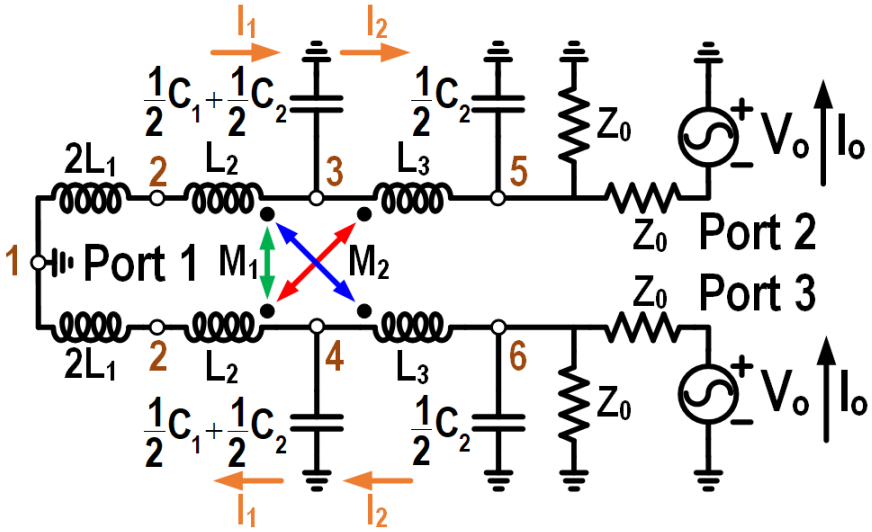

Figure 2.8: Half-circuit representation of the proposed folded inductor equivalent schematic for odd-mode operation analysis.

$$-\mathrm{I_1L_2} + \mathrm{M_1I_1} + \mathrm{M_2I_2} - \mathrm{I_12L_1} = -\mathrm{I_2L_3} + \mathrm{I}I_1\mathrm{M_2} \tag{2.3}$$

$$\beta = \frac{\mathrm{I_2}}{\mathrm{I_1}} = \frac{2\mathrm{L_1} + \mathrm{L_2} - \mathrm{M_1} + \mathrm{M_2}}{\mathrm{L_3} + \mathrm{M_2}} \tag{2.4}$$

The input impedances seen by Port 2 between the nominal and proposed half-circuit should be the same, yielding:

$$sL_{\pi(1)} || \frac{1}{s\left(\frac{1}{2}C_1 + \frac{1}{2}C_2\right)} + sL_{\pi(2)}$$
$$= \left(s2L_1 + sL_2 - s\frac{1}{\beta}M_1 - s\beta M_2\right) || \frac{1}{s\left(\frac{1}{2}C_1 + \frac{1}{2}C_2\right)} + sL_3 - \frac{1}{\beta}M_2 \quad (2.5)$$

2.4 Simulation and Measurement Results and Discussions

A proof-of-concept design was fabricated using the GlobalFoundries 22 nm FD-SOI CMOS process. In this design, a characteristic impedance Z_0 of 50 Ω is chosen. Two two-port test structures (Port 1 – Port 2, Port 1 – Port 3) are designed with on-chip 50 Ω termination at the unused port to characterize the WPD using single-ended probes and Keysight 67 GHz 4-port vector network analyzer (N5247B). The chip micrograph of one of the test structures is shown in Figure 2.9. The core chip area is 190 μm × 190 μm.

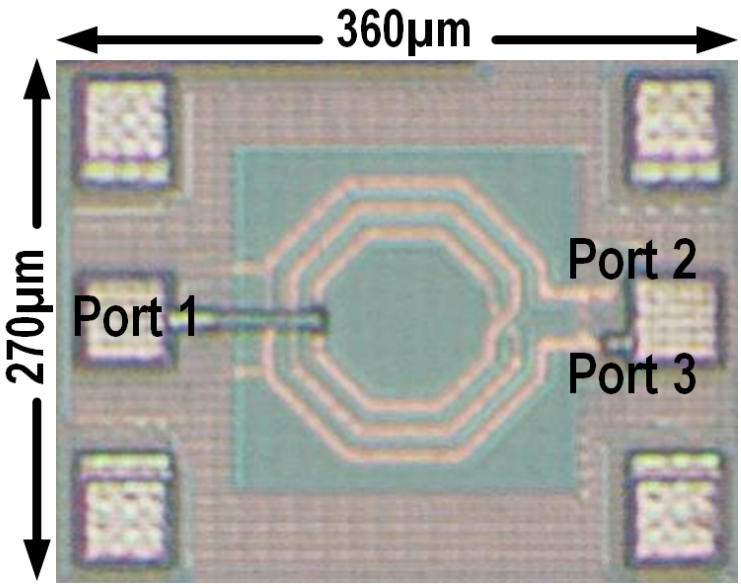

Figure 2.9: Chip micrograph of the proposed folded inductor-based WPD implemented in the GlobalFoundries 22 nm FD-SOI CMOS process.

Due to measurement equipment limitations, the results are measured from 15 – 67 GHz. In Figure 2.10, measured return loss for all three ports are greater than 10 dB.

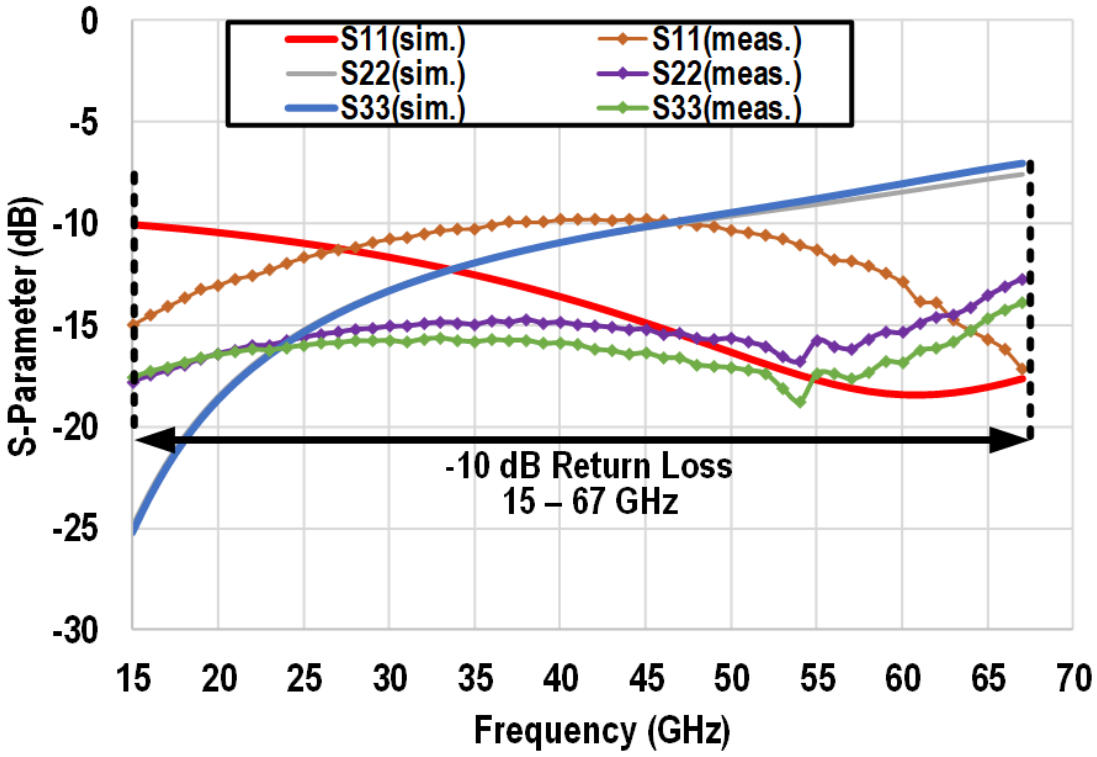

Figure 2.10: Measured and 3D EM simulated return loss of the folded inductor-based WPD. Port definitions are denoted in Figure 2.3.

Since the fundamental equal power division loss is 3 dB, additional insertion loss shown in Figure 2.11 is between 0.5 & 1.17 dB, outperforming the state-of-the-art designs. The simulated isolation between Port 2 & Port 3 is also shown in Figure 2.11 to be better than 10 dB, demonstrating the operation bandwidth from 15 – 55 GHz of this wideband ultra-compact WPD.

The magnitude and phase responses are presented in Figure 2.12 between the input (Port 1) and output ports (Port 2 & Port 3), exhibiting less than 3° phase mismatch and less than 0.2 dB amplitude imbalance from 15 – 67 GHz, making this design well balanced.

The difference between the 3D EM simulated and measured results can be attributed to the additional probe and pad parasitics that shift the resonance frequencies of the S-parameter responses. Table 2.1 summarizes the performance comparison with existing published on-chip mm-Wave WPD.

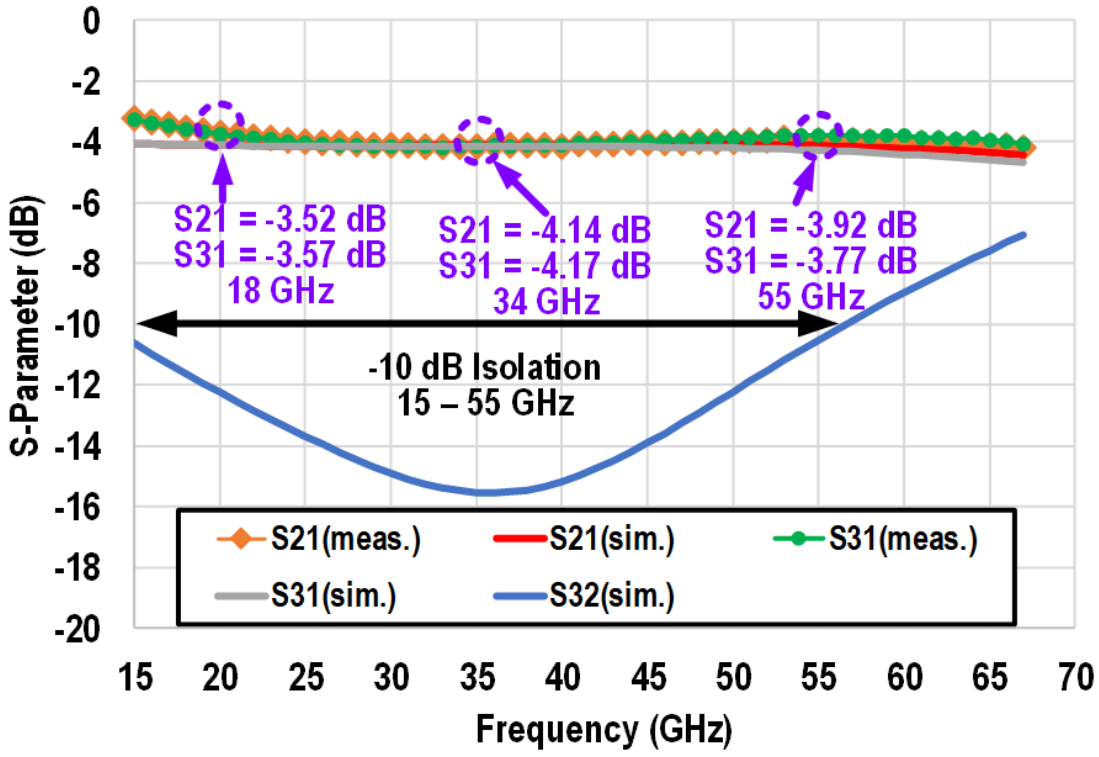

Figure 2.11: Measured and 3D EM simulated insertion loss and isolation of the folded inductor-based WPD. Port definitions are denoted in Figure 2.3.

2.5 Summary

In this paper, the analysis and design equations of a wideband ultra-compact folded inductor-based mm-Wave WPD is presented. A proof-of-concept demonstration operating from 15 – 55GHz occupying only 0.0361 mm^2 within one folded inductor footprint is demonstrated, achieving greater than 1.5× size reduction compared to state-of-the-art CMOS mm-Wave WPDs while achieving low insertion loss from 0.5 – 1.17 dB and well-balanced outputs, with less than 3° phase mismatch and less than 0.2 dB amplitude imbalance throughout the entire frequency band, enabling future 5G multi-band applications.

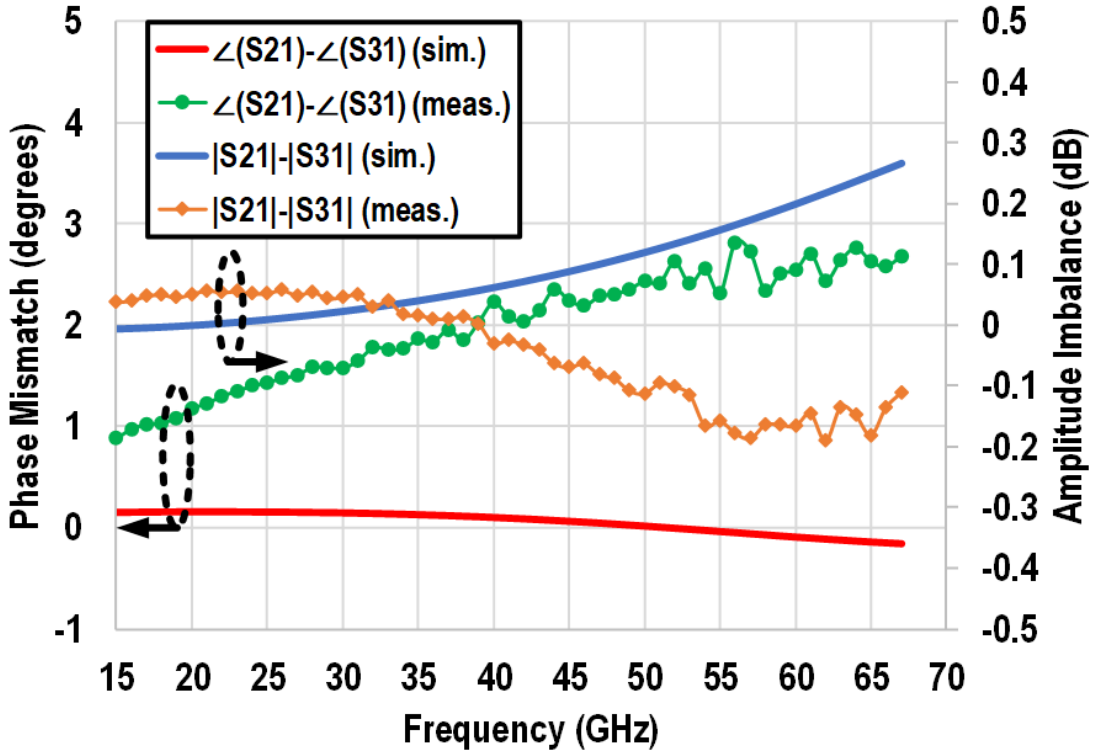

Figure 2.12: Measured and 3D EM simulated amplitude imbalance and phase mismatch of the folded inductor-based WPD. Port definitions are denoted in Figure 2.3.

Table 2.1: Comparison of CMOS mm-Wave WPDs

Ref.	Tech.	Freq. (GHz)	Top.	IL (dB)	RL (dB)	Iso. (dB)	ΔAmp. (dB)	ΔPhase (deg)	Size (mm^2)	Normalized Size (λ^2) @ 40 GHz
[19]	65 nm CMOS	20-40	$\lambda/6$ TL	0.91	>10.5	>12*	N/A	N/A	0.125	0.0022
[23]	90 nm CMOS	54-67	Stub-loaded Elevated-CPW	2.3	>10	>10	<0.16	<0.45	0.051	0.0009
[24]	0.18 μm BiC-MOS	24-61	Cap. loading Slow-wave CPW	1	>10	>15	<0.5	<2	0.078	0.00139
[25]	90 nm CMOS	40-50	Asym. Shunt-Stub	4.2	>12	>19	<0.5	N/A	0.06	0.001
This Work	**22 nm CMOS**	**15-55**	**Folded Inductor**	**0.5-1.17**	**>10**	**>10***	**<0.2**	**<3**	**0.0361**	**0.00064**

* Simulated Isolation.

CHAPTER 3

WIDEBAND PLANAR ARCHIMEDEAN SPIRAL ANTENNA

The spiral antenna (SA) and its variants (e.g. logarithmic, sinuous) have been explored extensively for wideband operation since their input impedance is independent across frequency due to their self-similar nature. In this chapter, we discuss the advantages of the SA geometry and its physical construction for high-speed wireless communications, radar, imaging, and direction of arrival applications within mm-Wave phased array systems [26, 27, 28].

3.1 Introduction

Mm-Wave phased arrays demand a compact unit element antenna that can achieve broadband performance to minimize the overall array size, while adding more functionality such as polarization reconfigurability to allow for versatile applications. As frequency scaling continues to climb, the antenna footprint can proportionally decrease, allowing for convenient integration on a CMOS platform to realize an on-chip implemented antenna [29]. At the same time, the antenna element should fit within either a $\lambda/2$ or λ spacing from center to center, to minimize the grating lobe levels that are detrimental for phased array performance.

Due to the self-complementary nature of the SA geometry, the primary principle of radiation is through an illuminated ring" which scales proportionally with operating frequency. More specifically, the circumference of the active "ring" determines the frequency of radiation; Figure 3.1 illustrates the SA geometry.

Thus, the lower and upper frequency bounds of the SA are determined by the circumferences of the outermost and innermost rings (denoted by dashed blue circles), respectively. The "ring" is formed by a constructive interference of the surface currents (denoted by

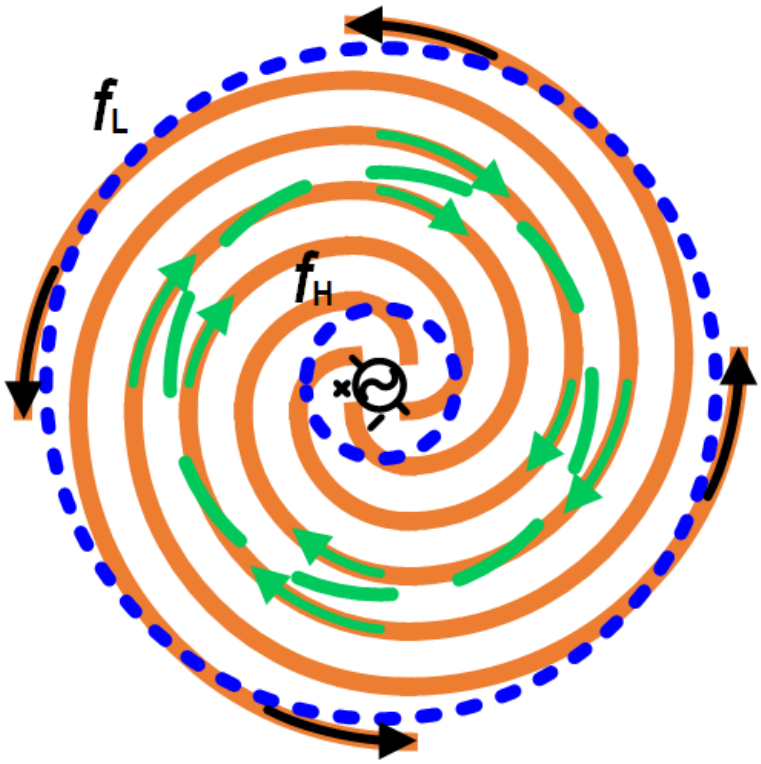

Figure 3.1: Geometry of the SA with lower and upper frequencies of operation determined by the circumferences of the outer and inner dashed blue circles, respectively. When the surface currents along the arms add constructively as denoted by the green arrows, radiation occurs.

green arrows) traveling around the arms of the SA. As a result, the diameter of the spiral antenna from the outermost circle would be approximately $d = \frac{\lambda_{low}}{\pi}$, which fits within the $\lambda/2$ or λ spacing constraint within phased arrays.

The SA example in Figure 3.1 is excited through a center feed (nominally a vertical coaxial feed), which is feasible for materials and processes that allow for vertical feeding ports (e.g. most PCB technologies). In practice however, such 3D feeding mechanism becomes cumbersome to integrate on planar platforms (e.g. advanced silicon processes), where access to the back may not be easily accessible, unless through-silicon vias (TSVs) are offered. However, TSVs add overhead and complexity for both the designers and foundries, so their feasibility becomes obviated in this discussion. Thus, edge-feeding is introduced as a viable replacement that complies with the design rules for planar structures, while minimizing transition losses and allowing for easy integration with other electronics.

As a result, the SA can be fed from the edge, provided that the phase progression of the feeding points are carefully maintained [30]. Different combinations of phase progressions along the different arms can yield different radiating modes and patterns, which have been extensively used for direction-of-arrival applications, [31, 32].

As a result, the combination of edge feeding and maintaining phase progression along the different arms of the SA allows one to provide on-antenna power combining through a concept called multi-feed driven antennas. These antennas have been studied to eliminate the need for bulky and lossy passive combining/dividing networks because they can provide power combining within a single element footprint while preserving single element radiation pattern [13, 33, 34]. Yet, the multi-feed antennas that have been explored so far have been standing-wave structures, which have limited bandwidth due to the fundamental nature of their geometry.

3.2 Octagonal Four-Arm Archimedeam Spiral Antenna

To address the challenges while combining the desired qualities of the spiral antenna, a four-arm edge-fed octagonal Archimedean SA is proposed. The four-arm implementation is capable of providing four single-ended signals to combine on the antenna and propagate. Contrary to its standing-wave counterpart, the SA is a traveling-wave structure, allowing for extremely wide impedance bandwidths.

The nominal spiral begins with an initial radius, r_i, which determines the spiral antenna's highest frequency of operation. The arm radius, ρ_0, expands as a function of the growth rate, α, and independent variable angle, θ, which increases in the counterclockwise direction until $2\pi n$, where n is the number of turns,

$$\rho_0(\theta) = r_i e^{\alpha\theta}, \theta \in [0, 2\pi n] \tag{3.1}$$

The Archimedean type is chosen as it is most amenable to standard PCB/silicon tech-

nology design rules, which typically only allow 45°/90° bends. While curved edges can be approximated with enough resolution, the design complexity is far from desirable especially with the goal of making scalable phased array in mind. As a compromise, the octagonal shape was chosen as it best maintains the traveling waves along the spiral arms as there are less sharper corner discontinuities than that of a square spiral, preserving the broadband impedance behavior.

The antenna arms are excited in a phase progression with respect to each adjacent neighbor, forming modes that provide different radiation characteristics. In Mode 1 formation, the arms have 0°, 90°, 180°, and 270° counterclockwise phase progression, resulting in a main beam in the boresight direction (θ = 0°). On the other hand, Mode 2 with phase progression 0°, 180°, 360°, and 540° results in a null in the boresight direction. While there are up to n-1 modes, typically the most pertinent ones for a four-arm spiral are Modes 1 & 2. As a result, the 4-arm SA obviates the need for a separate component by providing power combining on the antenna by in-phase summation of two pairs of differentially driven arms, providing improvement in gain performance over frequency. Although the proof-of-concept design includes a linear tapered impedance transformer to match the antenna input impedance to 50 Ω, in practice a carefully integrated system would account for the impedance levels across different stages. Nonetheless, as the impedance transformer is employed in this design, its design principle and performance are also discussed in the next section.

3.3 Linear Tapered Impedance Transformer

The impedance transformer consists of a linearly tapered coplanar waveguide (CPW) to provide wideband matching across 10 – 70 GHz from antenna driving impedance of 130 Ω to 50 Ω termination. Each arm is attached to an impedance transformer, adjusting the width of the signal line until the desired impedance is achieved. Vias are placed along the taper to ensure the fields remain within the substrate and signal line. The designed impedance

transformer is shown in Figure 3.2.

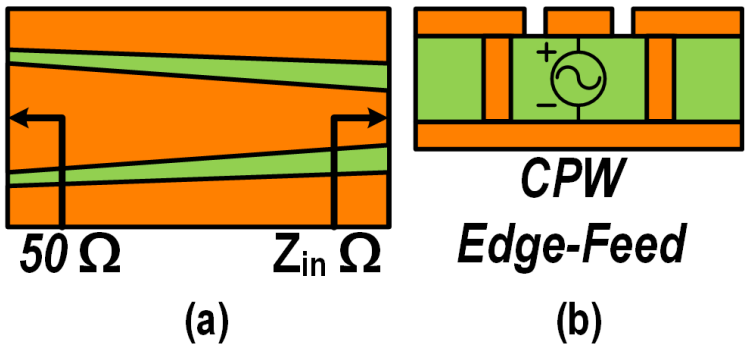

Figure 3.2: Linear tapered CPW impedance transformer from the (a) top-view and (b) cross-sectional view.

3.4 Fully Integrated Spiral Antenna

The EM structure models a spiral antenna realized on a two-layer printed circuit board (PCB), as shown in Figure 3.3. Each arm has one turn with a width of 0. 6mm and a spacing of 0.45 mm between adjacent arms. The substrate material is Rogers© RT/Duroid 5880 which is 0.254 mm thick, placed in between two 1oz copper layers. In Figure 3.3(b) there is a 11.8 mm × 11.8 mm hole space in the bottom copper layer of the antenna underneath the spiral antenna to provide backside radiation through the substrate. The PCB is 27.6 mm × 27.6 mm including the matching networks. The blue dots in Figure 3.3(a) near the edge of the impedance transformers represent the edge-feeding point.

3.5 Simulation Results

The antenna's differential return loss was characterized by placing differential ports at opposite arms. The simulated return loss, or S_{11}, and isolation, S_{21}, seen in Figure 3.4 are greater than 10 dB and greater than 60 dB, respectively, between 15 – 75 GHz. The respective port numbering in the S-parameter response is the same as that seen in Figure 3.3(a).

Gain variation less than 3 dB is observed from 5 – 65 GHz, while axial ratio (AR) of the spiral antenna in the Mode 1 excitation is shown to be less than 3 dB across the entire

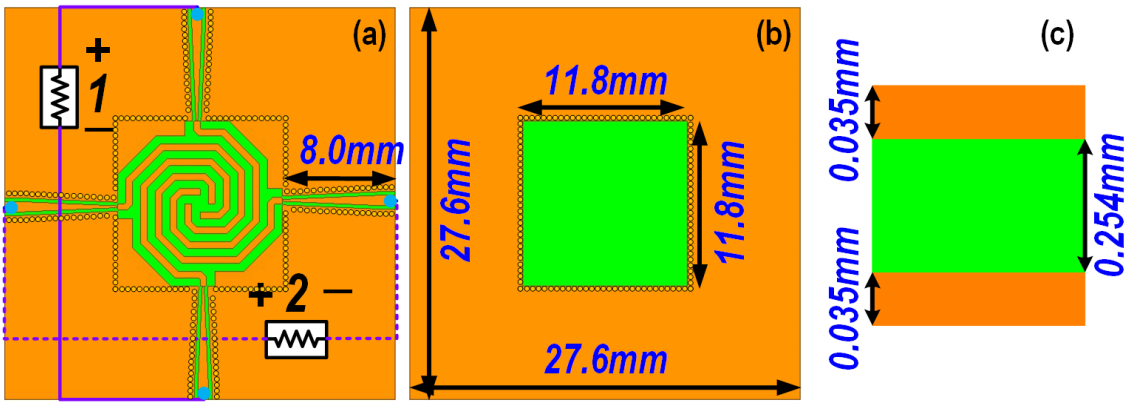

Figure 3.3: EM model of antenna showing differential ports 1 & 2: (a) top side; (b) bottom side; (c) cross-sectional view.

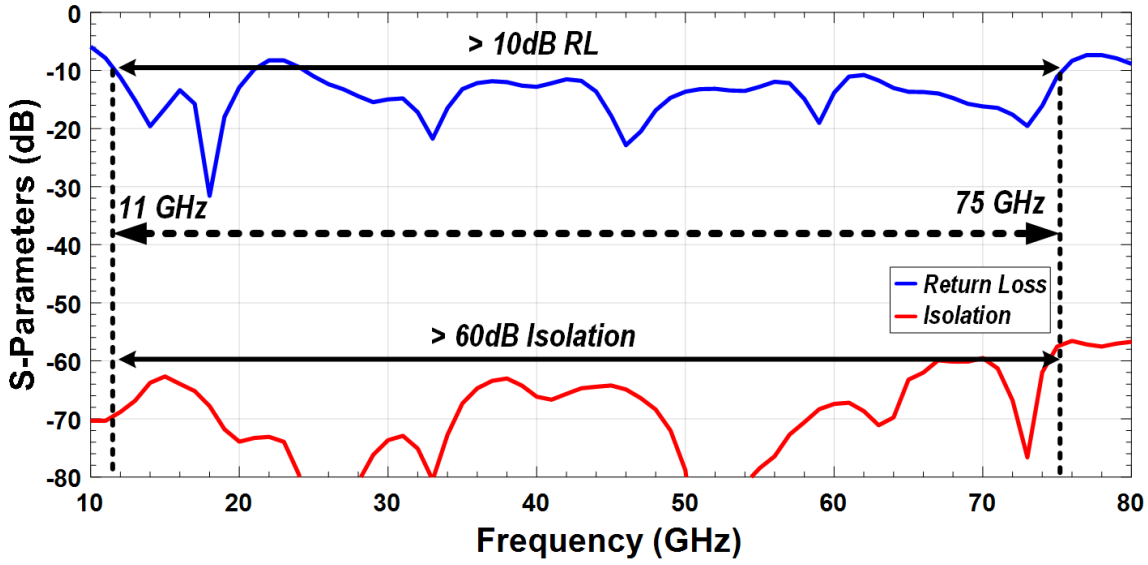

Figure 3.4: Simulated return loss (blue) and simulated isolation (red).

range except for 75 – 78 GHz, as shown in Figure 3.5. This sudden spike is attributed to the resonance at 75 GHz that hinders the pattern and causes the energy to be directed opposite of the substrate. At high frequencies the main lobe leaks energy to its adjacent sidelobes.

Normalized radiation patterns were simulated in increments of 20 GHz from 15 – 75 GHz with Mode 1 excitation, as shown in Figure 3.6. There is degradation to the main beam which leaks to the sidelobes at higher frequencies. This is best shown in Figure 3.7, where the surface currents show different regions of the spiral antenna adding their surface currents constructively and radiating. More specifically, multiples of the radiating ”rings”

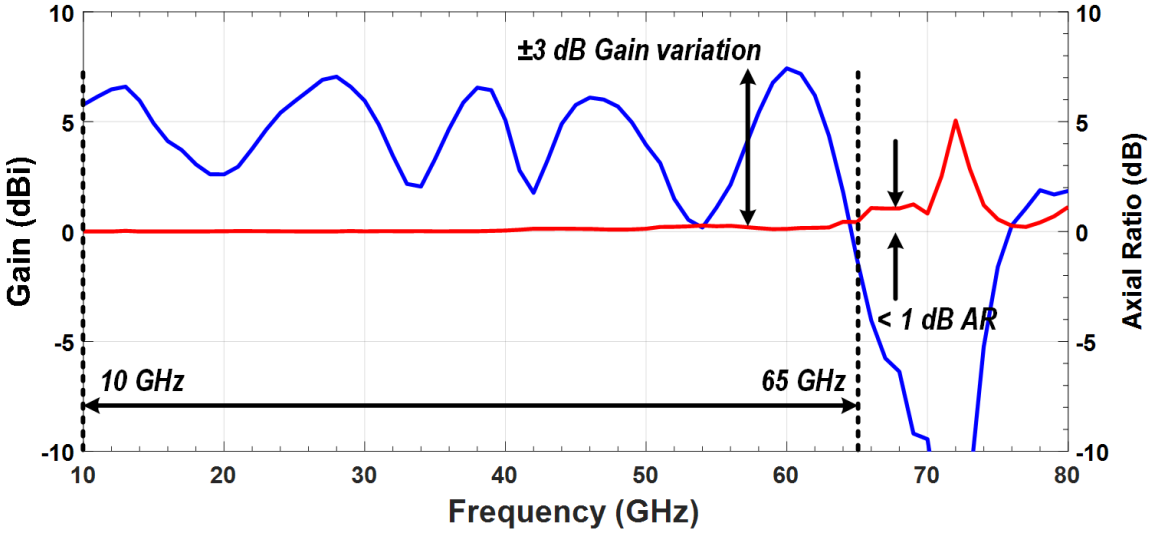

Figure 3.5: Simulated return boresight gain (blue) and simulated AR (red).

can exist within the same SA, consequently causing the higher order modes to interfere and distort the main beam pattern as shown in Figure 3.6. However, the HPBW greater than 45° due to the circularly polarized nature of the antenna.

The simulated performance of the linear tapered impedance transformer is also shown in Figure 3.8. In practice, this would be fabricated as a separate test structure to isolate and accurately evaluate the SA's characteristics by de-embedding the incurred transformer insertion losses. Nonetheless, greater than 10 dB return loss is achieved across the desired impedance matching bandwidth, providing a broadband impedance transformation.

3.6 Summary

This paper presents an octagonal dual polarized four-arm Archimedean SA integrated with edge-fed impedance transformers covering mm-Wave frequencies. Compared to a conventional center-fed antenna with vertical coaxial feed, this compact planar proof-of-concept design mimics an on-chip implementation and demonstrates edge-feeding and a geometry that is amenable to multi-feed on-antenna power combining, while maintaining desired spiral antenna characteristics such as broad bandwidth and dual polarization. The form factor of the SA also is compact enough to fit within standard $\lambda/2$ or λ phased array

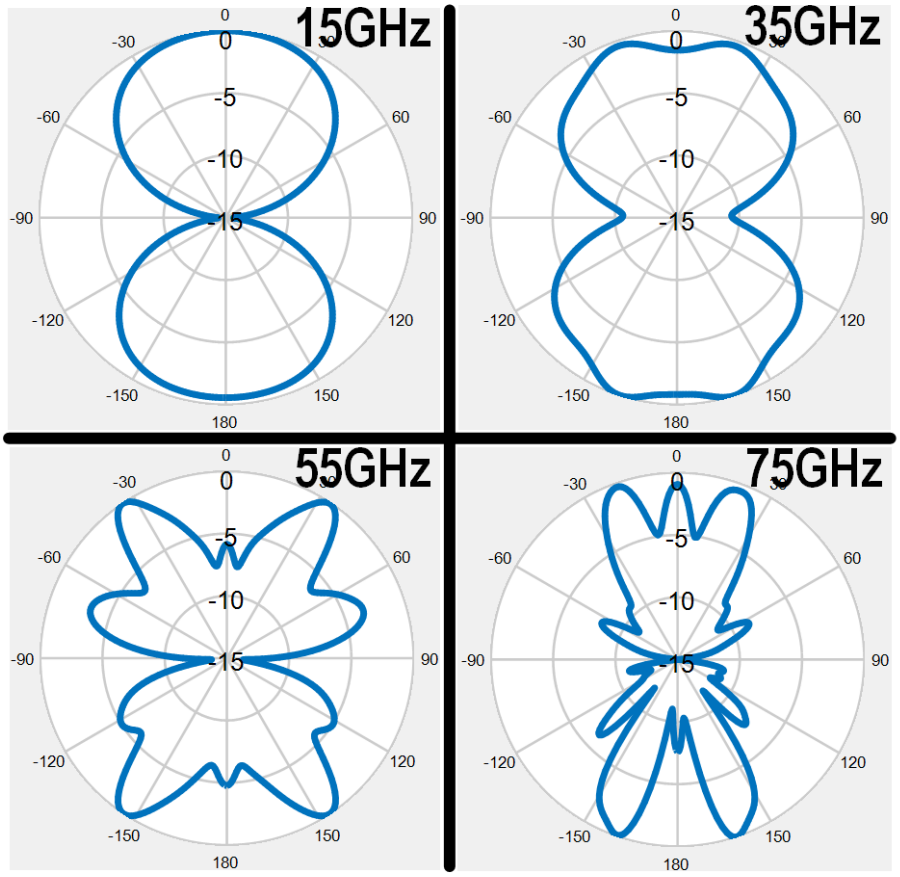

Figure 3.6: Normalized radiation patterns across different frequencies.

configurations, proving it to be a potential candidate for next generation wideband mm-Wave phased array antennas. The simulated results of the proposed antenna show return loss greater than 10 dB, isolation greater than 60 dB, and HPBW greater than 45°, covering nearly 7:1 bandwidth ratio from 11 – 75 GHz.

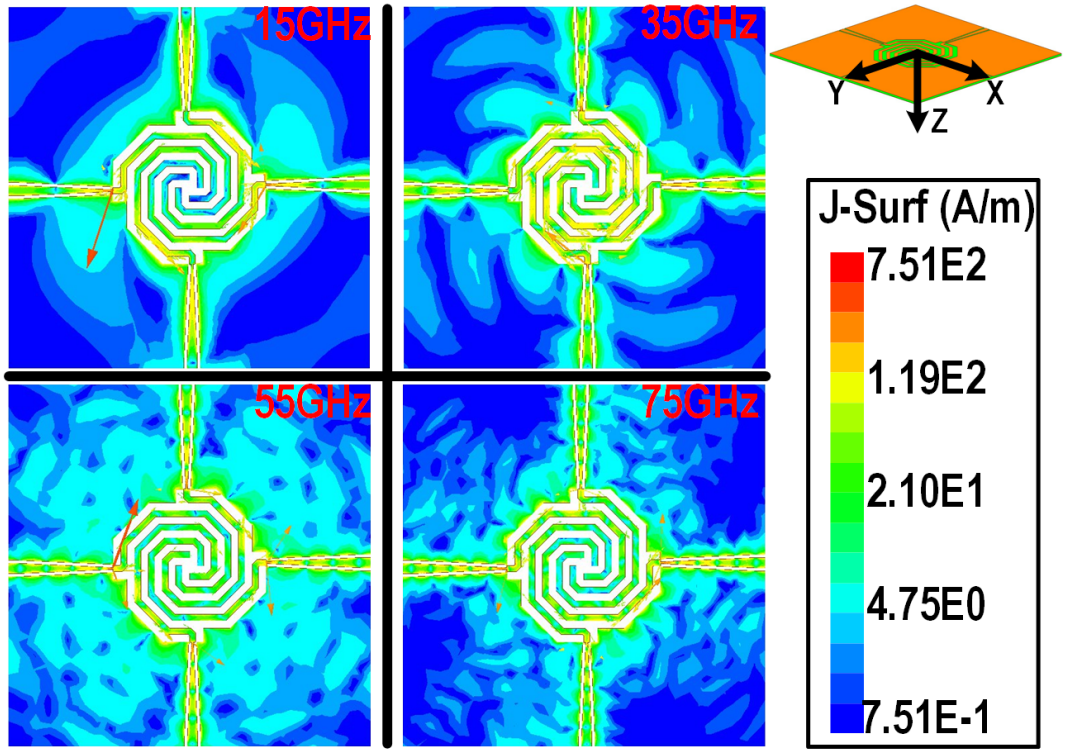

Figure 3.7: Surface current distribution across different frequencies.

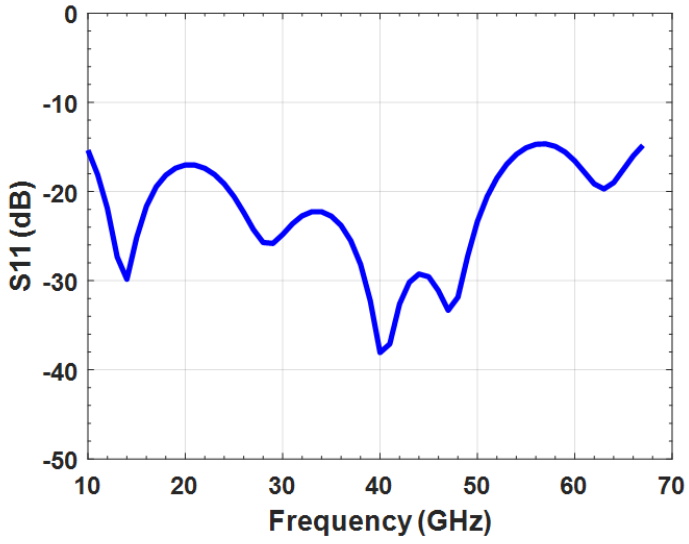

Figure 3.8: Simulated return loss performance of the linear tapered impedance transformer.

CHAPTER 4
CONCLUSION

This work presented designs in two critical areas of mm-Wave phased array systems. First, an ultra-compact, low-loss, wideband mm-Wave WPD within a folded inductor footprint on advanced 22nm Si FD-SOI CMOS shows promise to simplify the phased array system complexity within the signal distribution. Second, a wideband, edge-fed, planar PCB SA demonstrates the feasibility of being used as a phased array antenna element thanks to its simple construction and feeding mechanism, while also providing on-antenna power combining to improve the overall system EIRP. Improving the performances in these two design spaces can greatly aid the eventual realization of these mm-Wave phased array systems on advanced Si/SiGe platforms.

An immediate extension to the SA would be to fabricate and characterize its performance. Once this is verified, an arrayed version of the SA would provide an interesting study in phased array layout management and comparison for improved system EIRP due to the inherent on-antenna power combining nature of the 4-arm SA with respect to a single-feed antenna.

More importantly, the next steps would be to design and fully integrate these components within the same platform. On-chip antennas serve as promising candidates to make the SoC dream come to fruition, so long as they adhere to standard design rules set by the manufacturers/foundries. Fully integrated wideband mm-Wave SoCs can promise the unification of mm-Wave/5G standards across the world, potentially bringing together the plethora of applications mentioned earlier worldwide. Until then, continued and careful study of the feasibility of the integration must be carried out in future works beyond this thesis.

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