Design and Analysis of Capacitive Parametric Ultrasound Transducers for Wireless Power Transfer

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By

Charles Wei

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Design and Analysis of Capacitive Parametric Ultrasound Transducers for Wireless Power Transfer

Approved by:

Dr. F. Levent Degertekin, Advisor
School of Mechanical Engineering
Georgia Institute of Technology

Dr. Karim Sabra
School of Mechanical Engineering
Georgia Institute of Technology

Dr. Peter J. Hesketh
School of Mechanical Engineering
Georgia Institute of Technology

Date Approved: July 21, 2021

To my parents, sister, and René Descartes

Just kidding about the last part

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LIST OF SYMBOLS AND ABBREVIATIONS

WPT	Wireless Power Transfer
CMUT	Capacitive Micromachined Ultrasound Transducer
CPUT	Capacitive Parametric Ultrasound Transducer
BEM	Boundary Element Method
FEA	Finite Element Analysis
SOI	Silicon on Insulator
PECVD	Plasma Enhanced Chemical Vapor Deposition
RIE	Reactive-ion Etching
IPA	Isopropyl Alcohol
SPDT	Single Pole Double Throw

SUMMARY

For wireless ultrasonic power delivery to implantable medical devices, a capacitive parametric ultrasound transducer system is analyzed and improved upon. While 1D modeling had sufficed for proof of concept and power transfer with low efficiency has been demonstrated, a more detailed model gives insight to behavior that were previously overlooked. Simulations of large capacitive membrane arrays show higher power transfer efficiencies in some cases when the array is operating at a higher order mode. Analysis also shows that in tissue, fluid damping dominates the mechanics of the membrane array, allowing the array frequency to be tuned by adjusting the membrane thickness through analytical or finite element methods. To complete the power delivery chain, a modified power rectification circuit is simulated, demonstrated experimentally, and compared to a traditional rectification circuit highlighting improvements in power transfer efficiency. Finally, a capacitive membrane design optimized for 1MHz operation in fluid is fabricated in a cleanroom environment and used to demonstrate viable passive ultrasonic wireless power transfer, from hydrophone to load application.

CHAPTER 1. INTRODUCTION

1.1 Wireless Power Transfer

The concept of wireless power transfer is not new. Nowadays, near field wireless power transfer is most commonly achieved through inductively coupled coils, perhaps most ubiquitously found as a convenient way to recharge smartphones. While wireless charging may seem like a luxury in the world of smartphones, they are more essential for applications such as medical implant devices where reducing the number of invasive surgery operations is desirable. In particular, wireless power transfer through ultrasonic means have certain advantages over inductive coupling including better penetration depths, more total power due to higher safety limits in tissue, and smaller form factors than induction coils [1].

This thesis investigates an ultrasonic wireless power transfer device called capacitive parametric ultrasound transducer, or CPUT. Here, capacitive refers to the array of micromachined capacitive membranes used to receive acoustic waves, parametric refers to the way in which energy is pumped into the circuit by varying a parameter (capacitance), and ultrasound transducer refers to the means by which energy is transferred. While analysis and experimental demonstration of power transfer with CPUTs have been shown, a more thorough investigation of each stage of the power recovery chain is necessary to improve the overall power transfer efficiency; these investigations form the content of this work. On the mechanical side, membrane array geometries are optimized through finite element analysis and numerical simulations that account for acoustic radiation forces. The optimized membranes are fabricated with the sacrificial release process, while common

pitfalls and possible solutions are documented. Finally, on the electrical side, a modified power rectification circuit is implemented for parametric circuits to minimize losses while still sustaining parametric resonance. The result of our analysis is a self-contained CPUT system with demonstratable power transfer that can deliver sufficient power to implanted medical devices.

1.2 Capacitive Parametric Ultrasonic Transducer

A CPUT consists of a capacitive micromachined ultrasound transducer (CMUT) membrane array that acts as a variable capacitor in a series resonant circuit, converting acoustical energy from the surrounding medium into electrical energy across a load impedance [2] [3]. When an ultrasonic signal above a required threshold drives the membranes at twice the circuit's resonance frequency, energy is passively introduced into the circuit and can be harnessed across an electrical load. Figure 1.1 shows a simplified diagram of the CPUT; it can be most easily thought of as a coupled CMUT and parametric circuit.

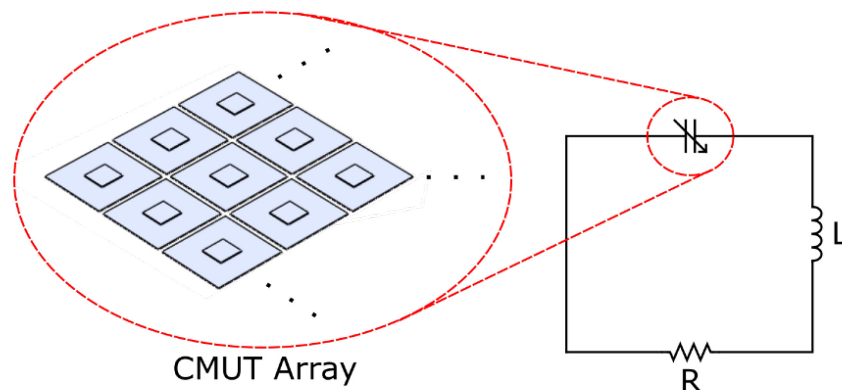


Figure 1.1 – Diagram of CPUT acoustical to electrical power transfer circuit with multidimensional CMUT array as variable capacitor.

1.2.1 Capacitive Micromachined Ultrasound Transducer

Although a newer technology than the piezoelectric transducer, CMUT operation has been studied extensively since its inception. A simplified diagram of a single CMUT membrane is shown in Figure 1.2. It consists of two parallel electrodes situated on a dielectric membrane and separated by a vacuum gap, forming a variable parallel plate capacitor.

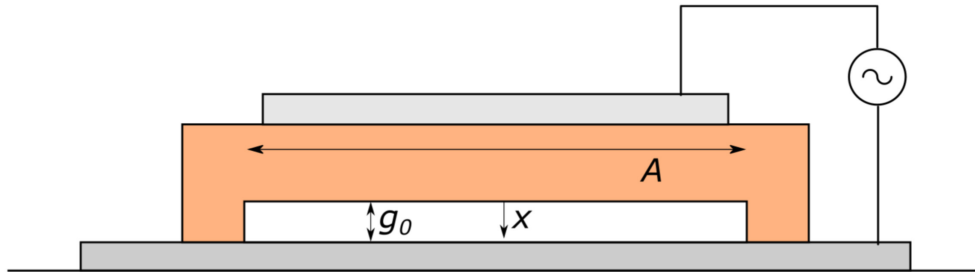


Figure 1.2 – Diagram of single CMUT membrane with one fixed electrode and one electrode positioned on a flexible, suspended membrane

Application of a voltage differential across the plates pulls the plates together due to coulombs law, allowing for transmission of acoustic waves. In receive mode, the changing membrane deflection can be measured as a change in capacitance. However, because the electrostatic force between the capacitor plates is dependent on the square of the applied voltage as in11 Equation 1, a significantly larger dc bias, $V = V_{dc} + V_{ac}$, is needed for linear operation in transmit and receive applications so that in Equation 13, the $2V_{dc}V_{ac}$ term dominates. In Equations 1 and 13 , ε_0 is the vacuum permittivity, g_0 is the nominal capacitor gap, A is the parallel plate area, and x is the parallel plate

displacement. A dc bias is not required for power transfer applications, allowing CPUTs to be a completely passive device.

$$F_e = \frac{\varepsilon_0 A V^2}{2(g_0 - x)^2} \tag{1}$$

$$F_e = \frac{\varepsilon_0 A}{2(g_0 - x)^2}(V_{dc}^2 + 2V_{dc}V_{ac} + V_{ac}^2) \tag{2}$$

The electrostatic force directly relates to another important parameter of CMUT; its collapse voltage. The collapse voltage is the voltage at which the electrostatic force pulling the plates together overcomes the mechanical spring force of the membrane, thus collapsing the membrane. It is found by equating the mechanical restoring force $F_m = kx$ to the electrostatic force and solving for voltage, giving the collapse voltage (Equation 3) and maximum displacement before collapse (Equation 4).

$$V_{coll} = \sqrt{\frac{8kg_0^3}{27\varepsilon_0 A}} \tag{3}$$

$$x_{coll} = \frac{g_0}{3} \tag{4}$$

A more thorough derivation of the collapse voltage as well as detailed analysis of additional principles of operation such as equivalent circuit modeling, electromechanical coupling coefficients and frequency bandwidths can be found in [4]. For even more accuracy, analytical displacements of circular membrane cells as discussed in [5] can be used to calculate effective membrane stiffnesses.

1.2.2 Parametric Circuit

The method in which energy is pumped into a circuit is by performing mechanical work on a time varying capacitor in a specific manner. It is established that the electrostatic force between two capacitor plates is always attractive and dependent on the charge across the plates.

$$F_e = \frac{q^2}{2\varepsilon_0 A} \tag{5}$$

In Equation 5, which is a reformatting of Equation 1 written in terms of capacitor charge instead of voltage, q is the charge on one plate of the capacitor. If mechanical work is applied on the capacitor against the electrostatic force instantaneously, i.e. pulling the plates apart, then the charge stays constant and it can be shown that the mechanical work (Equation 6) exactly equals the increase in energy stored in the capacitor (Equation 7) [6].

$$W_{mech} = \int_{x_0}^{x_1} F_e \, dx = \int_{x_0}^{x_1} \frac{q^2}{2\varepsilon_0 A} \, dx = \frac{q^2}{2\varepsilon_0 A}(x_1 - x_0) \tag{6}$$

$$\Delta E_{cap} = \frac{q^2}{2C_1} - \frac{q^2}{2C_0} = \frac{q^2}{2\varepsilon_0 A}(x_1 - x_0) \tag{7}$$

Since the charge across the capacitor in a LC circuit is sinusoidal with frequency $\omega = 1/\sqrt{LC}$, then the charge will be zero two times every cycle. Hence, the capacitor plates can be brought together during that time and no energy will be pumped out of the system.

In a CPUT, the capacitive membrane obviously cannot move instantaneously. Nevertheless, even under sinusoidal motion, the energy pumped into the circuit when the

charge is at a maximum is greater than the energy pumped out when the charge is zero. This revelation makes it clear why power transfer is sensitive to frequency changes and why the ultrasonic signal must be twice the circuit frequency. Since there are two points in each resonant cycle in which the charge crosses zero, the capacitor plates must be brought together two times per cycle. Deviations from the center frequency also means that capacitor plates are brought together while there is still charge across it, leading to losses in energy.

1.3 Literature Review

Passive energy harvesting from mechanical vibrations were shown in 2017 by modulating the inductance in a parametric circuit [7]. In their work, mechanical vibrations cause a spring-loaded mass to oscillate within the air gap of an inductor core, varying the inductance; they demonstrated 18 mW of power per 1 g of acceleration. Power transfer with CPUTs were also first analyzed and demonstrated in the same year [2]. In this case, acoustic excitation of a CMUT array causes a change in the capacitance in an RLC circuit. Regardless of the parameter varied, maximum power transfer was found in both cases to occur with an optimal load and when the forcing frequency is exactly twice the circuit frequency. CPUTs were analyzed in more detail in [3] by modeling the CMUT as a 1D mass-spring-damper system in which the mass is defined by the membrane mass plus fluid loading, the spring by the effective stiffness of the membranes, and the damper by the radiation impedance of a circular baffled piston. Consideration of the acoustical radiation forces in this work revealed that in addition to optimal electrical parameters for maximum power transfer efficiency, CMUT membrane design also played a major role in

performance, as impedance matching had to be considered. Under matched conditions, power transfers over 90% were achieved in simulation.

1.4 Contents of Thesis

The work in this thesis aims to improve CPUT operation by designing more optimal CMUT membrane geometries. In Chapter 2, methods of approximating multi-membrane CMUT arrays frequencies and more comprehensive modeling are explained. Chapter 3 details the fabrication process for optimal CMUTs with larger vacuum gaps than are typically used for imaging applications. Chapter 4 covers validation of CPUT simulation results with experimental power transfer using the fabricated devices. Finally, Chapter 5 concludes with a summary the contributions made towards CPUT design and possible areas for future work.

CHAPTER 2. METHODS

2.1 CPUT Models

Although a CPUT can be modeled with a 1D lumped element approach, it is most practically designed using an array of capacitive membranes. Arrays have smaller gaps to achieve larger capacitances and are easier to design for frequencies in the MHz range. However, this also makes it more complicated and expensive to simulate, as each individual membrane is mechanically and acoustically coupled. The 1D lumped model previously mentioned was developed to simplify computation time by lumping an array of membranes into an equivalent mass-spring-damper system. In that model, the effective stiffness k of the array is calculated using finite element analysis in COMSOL Multiphysics (COMSOL Inc., Burlington, MA, USA) by applying a force over a single membrane, dividing it by the mean membrane displacement, and multiplying by the total number of membranes. The effective mass m is calculated using k and the natural frequency of the membrane ω_0 according to the natural frequency relationship for a mass-spring system. Finally, the effective damping b is approximated as the real part of the radiation impedance for a circular baffled piston of equivalent area to the array.

The 1D model, however, is not ideal for accurate simulation of large membrane arrays because it has been shown that these acoustic metasurfaces can exhibit multiple mode shapes not only in individual membranes, but across the array surface as well [8]. To capture these higher order array mode shapes, a more detailed model should be used. A large signal model [9] utilizes the boundary element method (BEM) to calculate the forces and displacements between each individual membrane in an array. Each membrane can

furthermore be subdivided into two or more lumped patches depending on the membrane mode shapes. This model considers the nonlinear electrostatic forcing of each membrane as well as acoustical crosstalk between membranes in the array. Although this BEM model is more computationally intensive than the 1D model, it is still comparably faster than a transient 3-D finite element analysis of the array in a fluid domain. Transmitted pressure from a 16x16 array using the BEM model has been experimentally verified to within 2 dB up to 40 MHz operation as conducted in [9].

Simulink is used to replace the existing 1D spring mass model of the CMUT with the more appropriate large signal model. Figure 2.1 and Figure 2.2 show a block diagram representation of the 1D piston CMUT model and a high-level overview of the multi-dimensional BEM CMUT model.

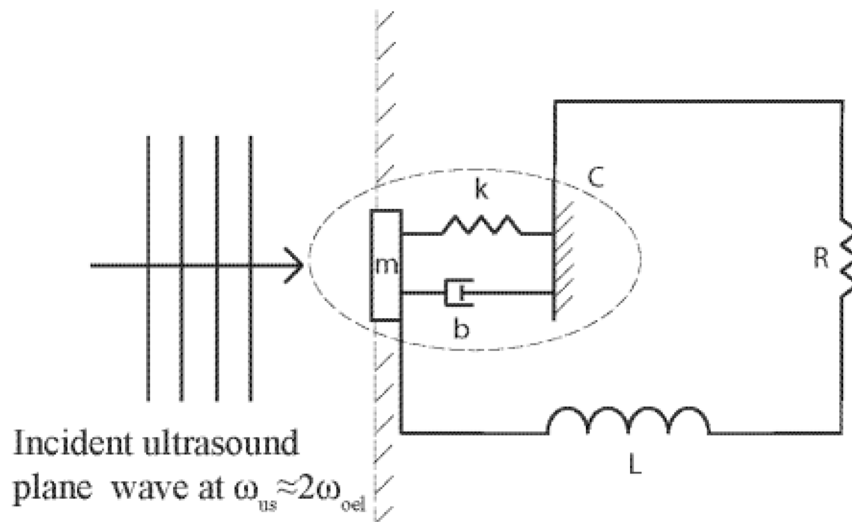


Figure 2.1 – CPUT model with 1D lumped mass spring damper CMUT model [3]

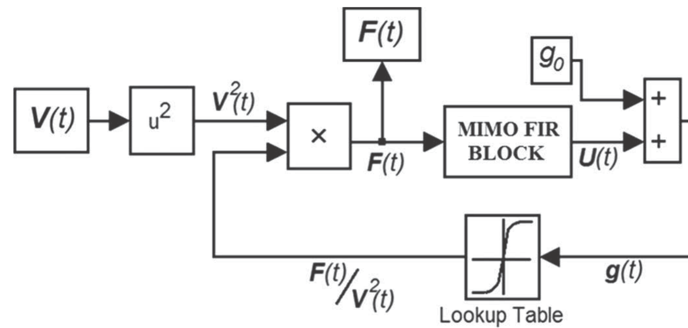


Figure 2.2 – Block diagram of multi-dimensional CMUT model relating membrane voltages to membrane displacements [9].

The combined large scale CPUT model shown in Figure 2.3 is used throughout the rest of thesis for CPUT simulations. An equivalent simscape model of the CPUT is also shown in Figure 2.4 in which the BEM CMUT model is incorporated into the circuit through a variable capacitor block. This model becomes more convenient for modeling more complex electrical systems with non-linear diodes, such as with a power rectification circuit.

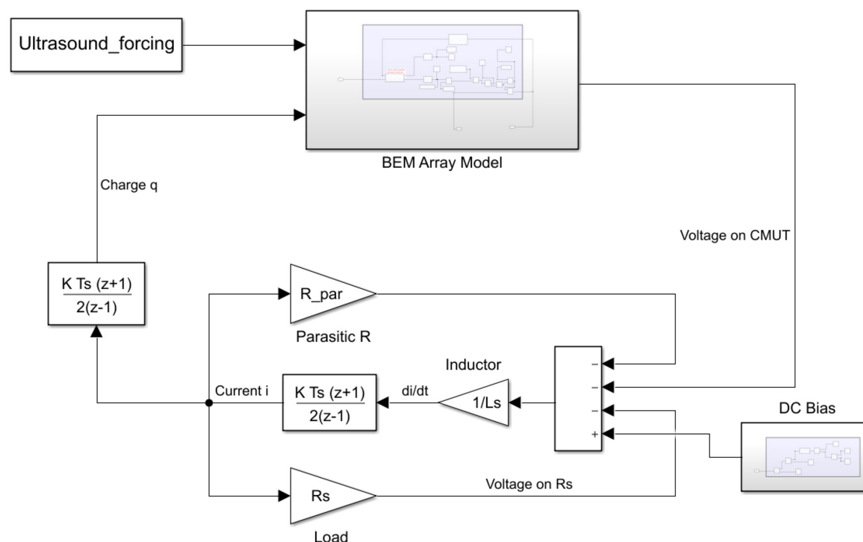


Figure 2.3 – Simulink implementation of RLC circuit with BEM CMUT model.

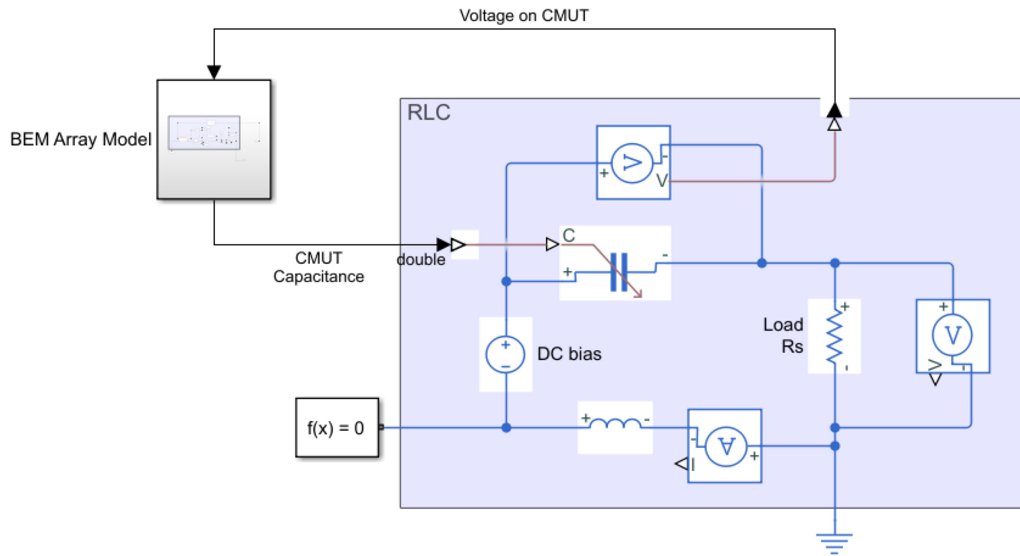


Figure 2.4 – Simscape implementation of RLC circuit with BEM CMUT model.

2.2 Model Validation

The CPUT models presented are validated through a power transfer experiment conducted using a 36 x 10 array of 70 x 70 µm membranes to obtain efficiency vs. load resistance data at a forcing frequency of 2.4 MHz (corresponding to an electrical frequency of 1.2 MHz). This CMUT was originally designed for imaging applications in past work. The experimental setup consisted of a piezoelectric ultrasound transmitter in a water tank, powered by an amplified signal from a function tor (Figure 2.5).

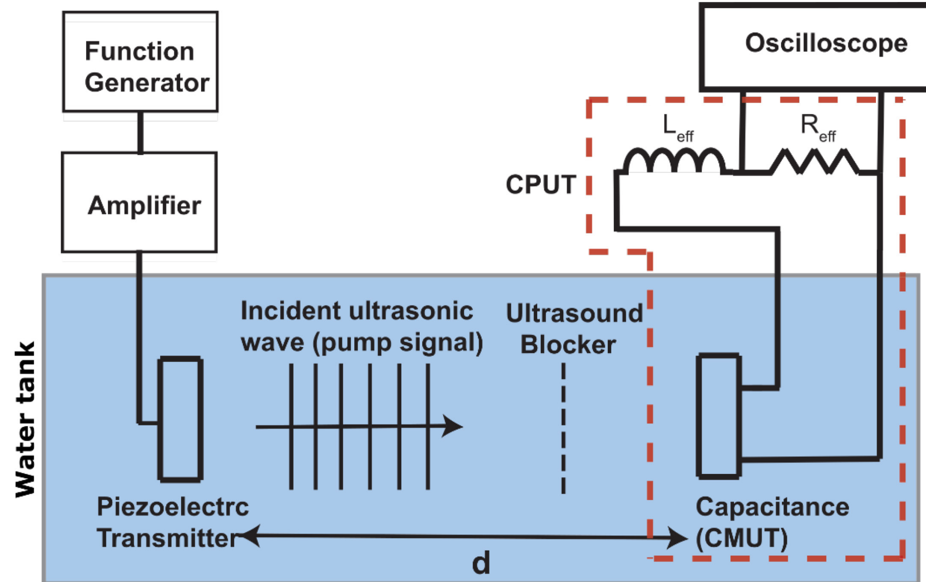


Figure 2.5 – Experimental schematic of CPUT power transfer [2].

The CMUT array is located at an arbitrary distance d away from the transmitter in series with an inductor and potentiometer, and immersed in Flourinert FC-70, shown in Figure 2.6. FC-70 is an electrically inert fluid with an acoustic impedance (1.36 MRayl) similar to that of water (1.46 MRayl), fat (1.34 MRayl) or blood (1.65 MRayl) [10]. Power across the potentiometer was measured using an oscilloscope for various loads. A hydrophone was used to determine the forcing intensity at same distance d to be roughly 300 kPa. This value was used to calculate experimental efficiencies and applied as the forcing term in the BEM simulation. Figure 2.7 reveals that despite low power transfer efficiencies due to sub optimal array design and forcing conditions, the experimental data shows good agreement with BEM simulations in terms of absolute value of efficiency and the cut-off value of the load resistance for parametric resonance.

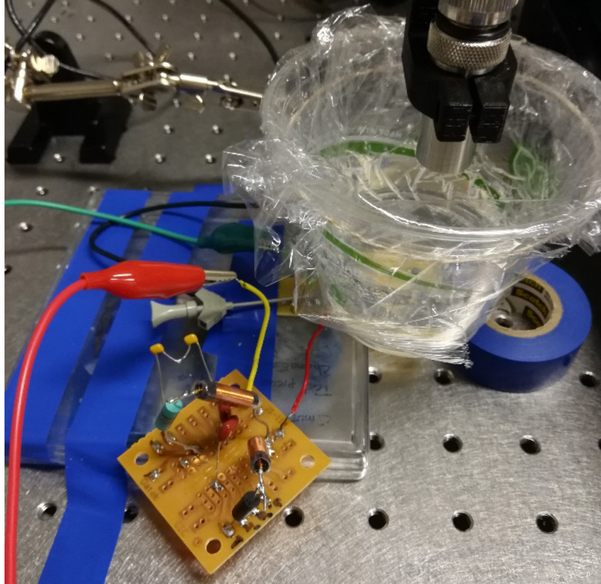


Figure 2.6 – Experimental setup with CMUT in FC70.

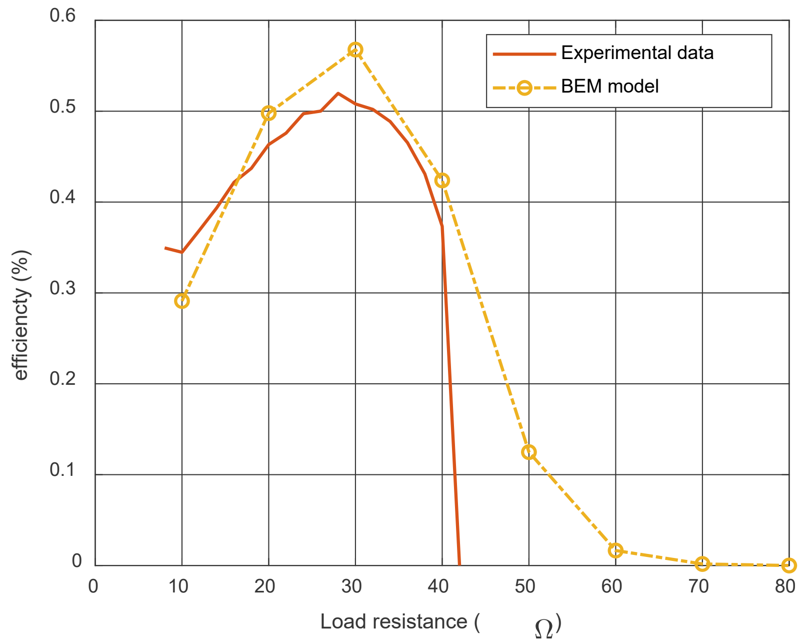


Figure 2.7 – Experimental vs BEM model simulation of CPUT power transfer efficiencies with a 36 x 10 CMUT array.

2.3 CMUT Design

Design of optimized CMUT typically involve a highly iterative process. Due to the time and computational resources required for large simulations, approximations can be used to determine a starting point for select parameters. For high frequency imaging CMUT arrays, frequency limits can be determined to be between the single membrane frequency and the Bragg's resonance frequency [11]. These values can be chosen to be far apart to obtain a good fractional bandwidth. For power transfer in medical applications, a lower frequency of operation is desired due to lower attenuation losses and US Food and Drug Administration limits on diagnostic ultrasound intensities.

2.3.1 Radiation Impedance

Since tissue contributes a significant damping effect on a CMUT array, the array frequency is heavily dependent on total array size. To avoid long computations for large arrays through BEM impulse simulations, the array can be approximated as a circular baffled piston and viscous damping approximated as the radiation impedance of a baffled piston.

$$Z_r = \rho_0 c_0 \left[1 - \frac{2J_1(2ka)}{2ka} + j\frac{2K_1(2ka)}{2ka}\right] \tag{8}$$

In Equation 8, J_1 and K_1 are first order Bessel and Struve functions and a is the radius of the piston [12]. The imaginary component of Z_r represents the equivalent mass loading of the fluid on the CMUT, and is shown for a 10x10 CMUT array of with total area 0.4 mm^2 in Figure 2.8.

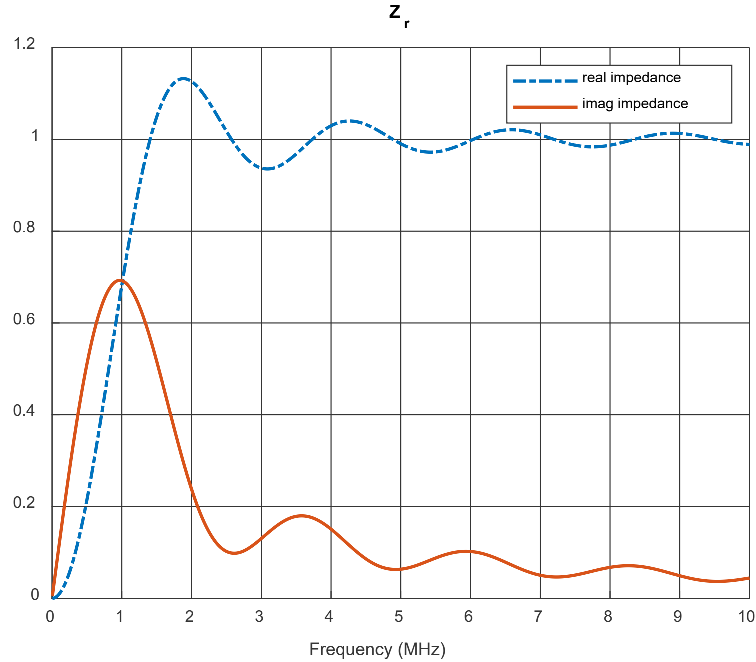


Figure 2.8 – Radiation impedance on the surface of a circular baffled piston radiating in half space.

2.3.2 Array Frequency in Fluid

Approximation of the array impedance allows for a straightforward estimation of the natural frequency in fluid starting with the single membrane characteristics. For a certain membrane geometry consisting of a rectangular silicon nitride plate and rectangular aluminum electrode, the effective mass m_{eff} is equivalent to the physical mass of the system. Finite element analysis (FEA) with COMSOL Multiphysics is used to determine the fundamental mode frequency of the membrane F_0, with an example depicted in Figure 2.9.

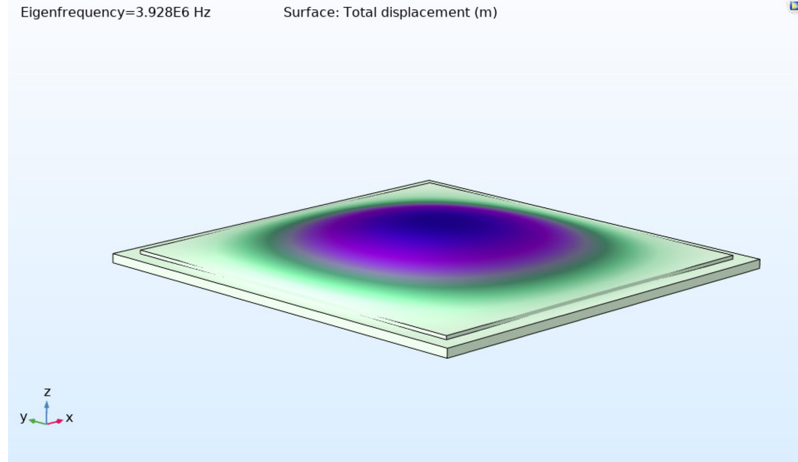


Figure 2.9 – FEA determination of first eigenfrequency of a single silicon nitride membrane with aluminum electrode in air.

The effective stiffness is calculated then as

$$k_{eff} = m_{eff}(F_0 * 2\pi)^2 \tag{9}$$

Assuming there is no mechanical coupling between membranes in an array, k_{eff} and m_{eff} can be directly scaled to n number of membranes by multiplying by n. Since the imaginary component of radiation impedance manifests as an additional mass, it can be lumped together with the m_{eff}, and the frequency of CMUT array with n membranes can be expressed as

$$F_{array} = \sqrt{\frac{n * k_{eff}}{n * m_{eff} + imag(Z_r(ka))}} \tag{10}$$

Equation 10 is an implicit expression of the array frequency because the radiation impedance is itself a function of the wavenumber k (frequency) and area a (number of membranes). For resonant behavior, the array frequency should match the acoustic

frequency for which the radiation impedance is calculated at. Solving Equation 10 can be achieved iteratively for increasing n. At each array size, the radiation impedance is calculated as a function of acoustic frequency for a baffled piston with fixed radius equal to the half the side length. This results in F_{array} as a function of acoustic frequency, as shown in Figure 2.10 for a single membrane array and a 20x20 array with the same single membrane geometries.

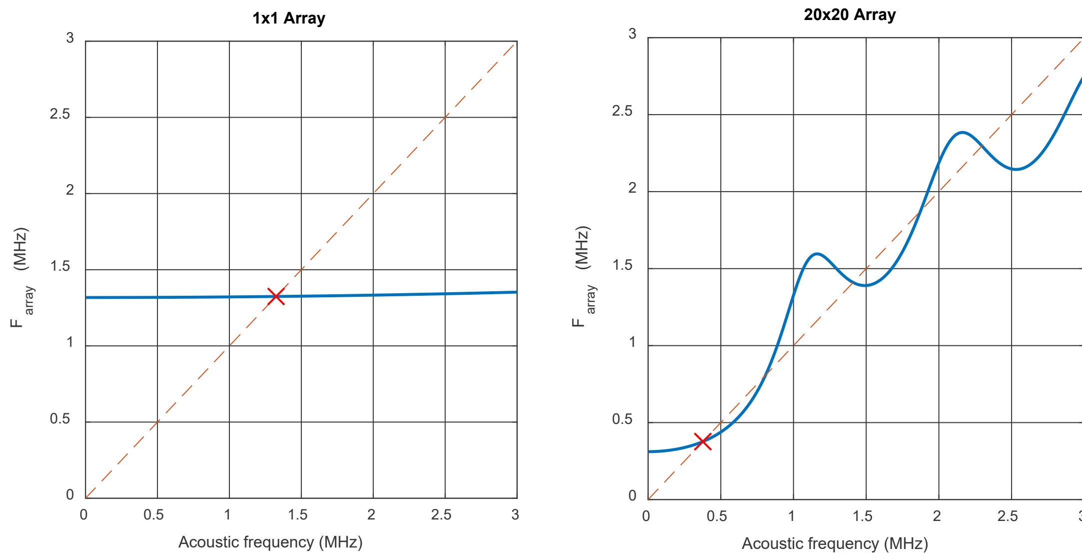


Figure 2.10 – Calculated array frequencies vs. acoustic wave frequencies for single cell membrane (left) and 20 x 20 array (right) in fluid.

In larger arrays, the calculated array frequency matches the acoustic conditions at various frequencies, and the lowest fundamental frequency is taken as the frequency of operation. The natural frequency analysis using this approach starts to deviate for larger arrays, as the individual membranes may no longer move in uniform motion and the baffled piston radiation impedance condition no longer applies. A plot of the predicted array frequencies vs. array size is shown in Figure 2.11. Array frequencies for arrays of size 1x1, 4x4, 10x10, and 20x20 were determined by calculating the full BEM model and taking the Fourier

transform of an impulse simulation. A comparison between the two methods suggests that for design of large CMUT arrays in immersion, the frequency for optimal operation can be tuned without computationally expensive iteration of full-scale models.

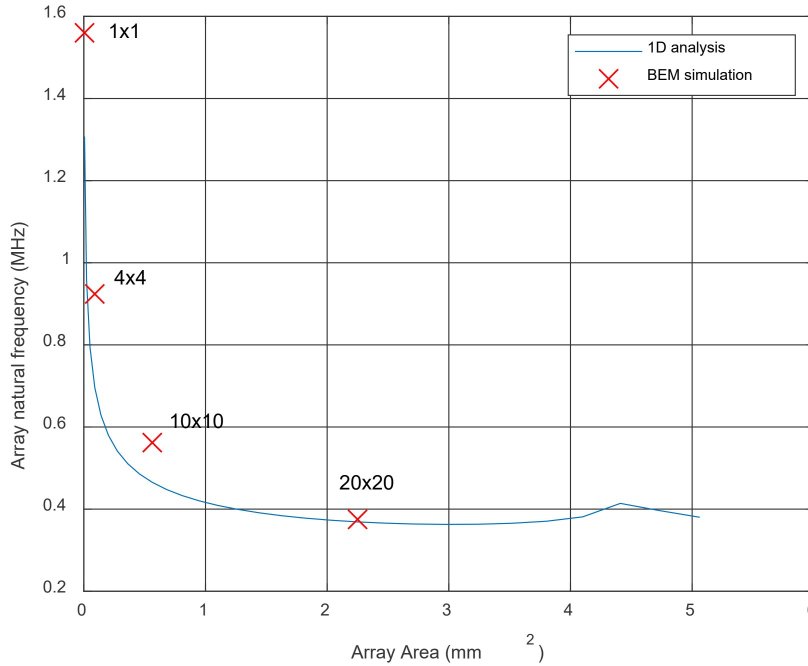


Figure 2.11 – Estimation of array frequencies in fluid vs total array size and validation with large signal BEM simulation frequencies.

Also of note, the contribution of added fluid mass at the natural frequency significantly dominates the mass of the membrane as the array size increases; for arrays with area larger than $1mm^2$, the fluid mass contributes to less than 2% of the total effective mass term. Therefore, it is possible to tune the desired frequency by adjusting the membrane thickness since the effective stiffness, based on thin plate theory, is proportional to the thickness cubed [13]. Then, from Equation 10, increasing the thickness by a factor of x should approximately increase the resonant frequency by a factor of $x^{3/2}$, since the total effective mass does not change appreciably in the denominator.

2.4 Efficiency Definition

For characterizing power transfer efficiency, care is taken in computing the total available acoustic power on the surface of the CMUT. An ultrasound forcing signal is applied to each patch in the BEM array model as a pressure level input. In the model, the pressure input is converted to a force, summed with the electrostatic force, and applied on each array patch. The available acoustic power input defined by Equation 11.

$$P_{avail} = \frac{P_{amp}^2}{2Z_r} * A \tag{11}$$

Here, P_{amp} is the pressure amplitude, A is the area of the CMUT, and Z_r is the radiation impedance of a baffled piston of equal half length, as discussed in Chapter 2.3.1. Because the pressure force is applied directly on the face of the CMUT array, Z_r is not simply the acoustic impedance for a plane wave through a medium $Z_r = \rho c$. If the input forcing signal is instead given as an intensity level some distance away from the array rather than a pressure on the face of the CMUT, then the available power can be defined as $P_{avail} = \frac{P_{amp}^2}{2\rho c} * A$. However, in this case, the physical force imparted on the membranes by the acoustic wave needs to be corrected by the circular baffle radiation impedance. If care is not taken in calculating the available input power, then the calculated efficiencies can show erroneous power transfer above 100%. A similar phenomenon is described in [14] in which receiver efficiency on a piezoelectric transducer exceeded 100% for dimensions smaller than the acoustic wavelength due to the receiver having an effective aperture larger than the physical aperture.

The output power is determined as the average power across the resistive load after transient simulations have reached steady state. In simulations, the average power is determined numerically. Since the voltage and current across the load is nearly sinusoidal, the output power can be formally defined as

$$P_{out} = P_{avg} = \frac{P_{max}}{2} \tag{12}$$

where P_{max} is the peak power across the load. The power transfer efficiency is a straightforward calculation, $\eta = \frac{P_{out}}{P_{avail}}$.

2.5 Power Rectification

To complete the power recovery chain, it is desirable to convert the ac voltage into dc to power circuits and electronic devices. However, rectification of parametric energy harvesting circuits cannot be easily achieved with a general diode bridge for a few reasons. First, the voltage across the load is typically on the scale of a few hundred mV, rarely exceeding 1 V peak to peak. This is seen both in simulation and in experimental validation of the BEM model. These values are generally not enough to overcome the 0.7V_f forward voltage of silicon diodes. Schottky diodes with lower forward voltages in the 0.2V_f range are therefore used, but even so, a minimum voltage of 0.4V_f is necessary for full bridge rectification, placing an additional restriction on CPUT operating conditions. Secondly, because CPUTs require the load impedance to be within a specific range (above a minimum load but lower than the critical load), power transfer into a bridge rectifier will not initiate from an idle state, since the impedance of the diodes when under the forward bias is typically larger than the critical load.

To remedy this, a single pole double throw (SPDT) switch is implemented to route the load across a resistive load when the voltage is below the diode forward voltage as in Figure 2.12. In this state, the CPUT operates in its normal behavior. After steady state is reach, there is sufficient energy in the system and the peak voltage is above the diode forward voltage; the output switches to the full bridge rectifier. During this stage of operation, the full bridge rectifier alone may provide a suitable impedance to sustain parametric resonance without needing to switch to load R_0, even when the voltage transitions between the positive and negative cycle. In the case that parametric resonance cannot be sustained, then it is possible to use a comparator to switch to load R_0 every cycle when the absolute voltage drops below the diode threshold. Additionally, if the load voltage is above a single Schottky diode V_f but below $2V_f$, then a half bridge rectifier can function. Because the CPUT sees a large impedance for the entire negative voltage cycle, switching between R_0 and the rectified R_L for half wave rectification must be implemented. A Simulink model show in Figure 2.13 is used for simulations in determining optimal R_0 and R_L values for power transfer.

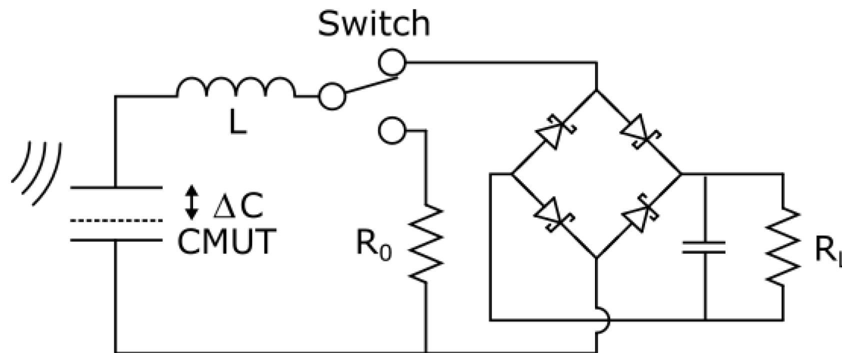


Figure 2.12 – CPUT circuit with load termination switching between resistor and full bridge rectifier.

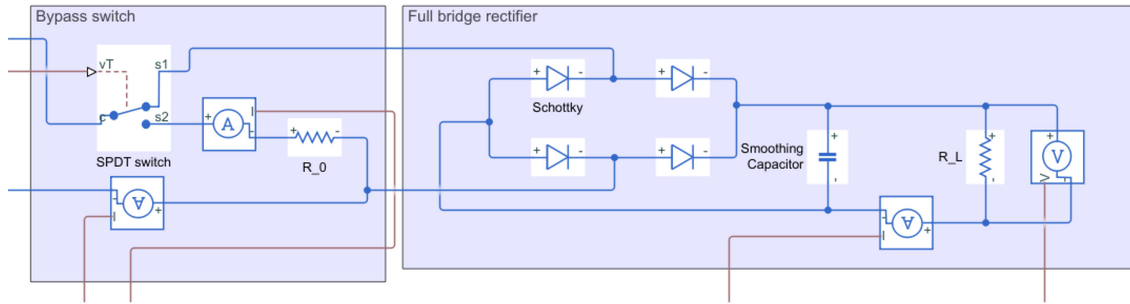


Figure 2.13 – Simulink/Simscape model of switch and rectifier circuit.

CHAPTER 3. CMUT FABRICATION

Microfabrication of CMUT arrays in a cleanroom generally falls under two main processes; the sacrificial release process and the wafer bonding process [15]. In the sacrificial release process, the vacuum cavity is formed through wet etching of a sacrificial material. The vias used to reach the sacrificial layer are subsequently sealed through a deposition step in vacuum, sealing the cavity. In the wafer bonding process, the vacuum cavity is instead formed through bonding of two wafers in vacuum. On one wafer, the cavity and all the features below it are first processed. A second silicon on insulator (SOI) wafer, a wafer with a thin oxide layer buried within the silicon, is fusion bonded onto the membrane cavity wafer in vacuum. Wet etch removal of the thin oxide layer then removes the bulk of the silicon wafer, leaving only the thin silicon membrane bonded to the CMUT cavity wafer. A comparison of the sacrificial release and wafer bonding process for the vacuum cavity formation step is shown in Figure 3.1.

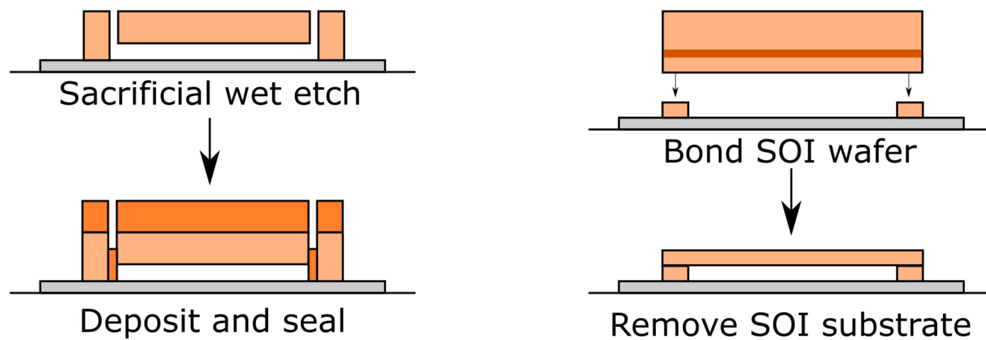


Figure 3.1 – Sacrificial release process (left) and wafer bonding process (right) for creating the CMUT vacuum cavity.

Although the wafer bonding process requires fewer masks than the sacrificial release process, fabrication of CMUT arrays for the purposes of this thesis were done using the sacrificial release process for a few reasons. First, a maskless aligner is used for all photolithography steps, allowing for quick redesign and negating the expensive and time-consuming process of ordering physical masks. Secondly, the sacrificial process avoids the need for expensive SOI wafers. Removal of the base silicon after the bonding step through wet etching without damaging the silicon on the cavity device can also be challenging. The rest of this chapter details each step in the CMUT fabrication process including the tools used, issues that arise, and potential solutions to those issues.

3.1 Sacrificial Layer Pattern

Device fabrication begins with a doped silicon wafer with a thin layer of thermally grown oxide, typically 3 um. Plasma-enhanced chemical vapor deposition (PECVD) can also be used for depositing oxide, and is required for direct fabrication of CMUT on CMOS chips due to the lower process temperature below 250 °C. CMUTs have been successfully fabricated using low all temperature processes on silicon and quartz wafers [16], as well as on CMOS circuits for intravascular imaging applications [17]; these CMUT on CMOS devices reduces parasitic capacitances in the interconnections significantly compared to wire bonding methods.

The bottom electrode is produced through wet etching of thin film chromium. Chromium is chosen for the bottom electrode due to its anti-corrosive nature and because it will not be etched by copper etchant during removal of the sacrificial layer later. Deposition of chromium is achieved through sputtering in an argon enriched low vacuum

environment. Sputtering is preferred over evaporation for its better deposition uniformity and lower impurity levels. After application of photoresist, UV photolithography is achieved with a mask or maskless aligner. The Heidelberg MLA150 maskless aligner is used for each of the five photolithography steps in these devices. The chromium bottom electrode is patterned through wet etching in chromium etchant 1020AC. This process takes roughly 20 minutes to completely etch 350 Å, although visual inspection is a much better indication of complete etching. The slow etch rate combined with low aspect ratio feature sizes means over etching is not an issue in this step. Images of the bottom electrode after wet etching is show in Figure 3.2. A few devices were also fabricated with small regions of the bottom electrode between membranes removed in order to further reduce parasitic capacitances. A close up of the dimensions post etch is show in Figure 3.3. Since the aspect ratio of these features are much higher, the photoresist geometry must account for the undercut distance during over etching. If the bottom electrode dimensions are smaller than the vacuum cavity dimensions, problems will arise during the subsequent sacrificial layer step.

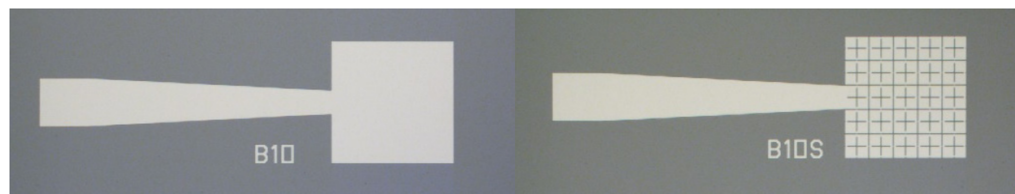


Figure 3.2 – Metal bottom electrode pattern for 10x10 array with full bottom electrode (left) and reduced bottom electrode (right)

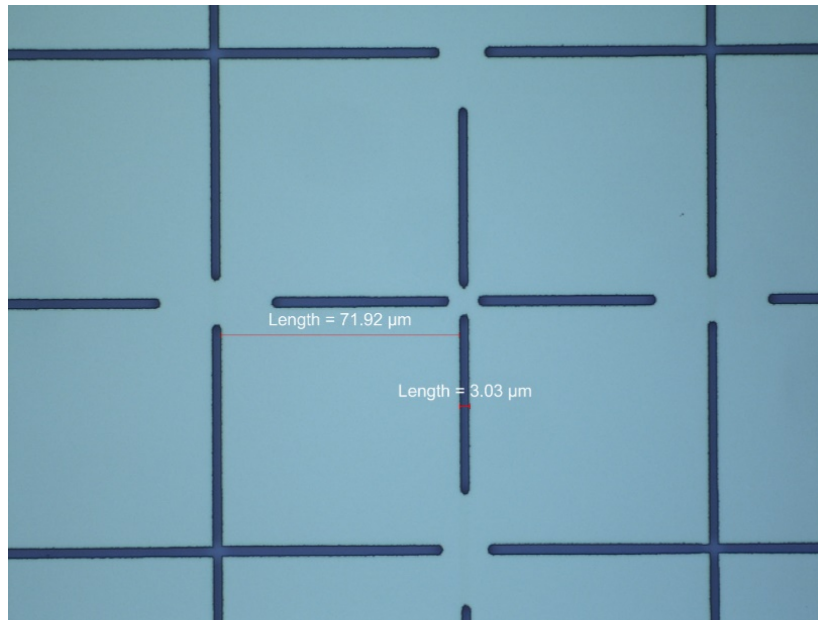


Figure 3.3 – Close up of feature sizes of reduced bottom electrode area.

For more electrical passivation between the top and bottom electrodes, a conformal layer of PECVD oxide is deposited next, equaling the thickness of the sacrificial layer. Depending on the recipe used, the deposition rate of PECVD oxide can be fairly uniform; in this recipe, a deposition rate of 60 nm/min was achieved. The exact oxide film thickness can be measured using spectroscopic reflectometry of oxide on silicon, a process that determines thin film thickness by shining an incident light on the wafer surface and measuring the intensity of the reflected light which varies based on film thickness due to constructive and destructive interference.

The next step involves patterning the sacrificial layer for deposition of the sacrificial material through lift off. Negative resist is used for this step to facilitate the lift off process. Before deposition of the sacrificial material, the oxide is first removed through reactive-ion etching (RIE); the chromium bottom electrode acts as an etch stop during this dry etch step. Sacrificial copper is then deposited through electron beam evaporation,

defining the vacuum gap thickness. Since the same photoresist pattern is used to etch the oxide and deposit the Cu in its place, there is no misalignment between the oxide passivation layer and the sacrificial layer. Cu is used for the sacrificial layer due to its ease in removal by wet etch; however, a variety of sacrificial material can be used such as polysilicon [15] as long as the etching liquid does not damage other components of the CMUT. Evaporation is also used to deposit the sacrificial layer because the directional deposition assists with the lift off process. Although a negative resist profile assists with lift off, the dry etching of the oxide passivation layer may reduce the angle of the negative profile. Therefore, evaporation is still desirable to maintain good device yield. Figure 3.4 shows a group of four sacrificial membrane layers including the interconnects between membranes where holes will be etched to reach the sacrificial layer. Subdivision of the sacrificial layer into groups of four is done to isolates each section from the rest and improve overall yield. Cracks or improper sealing in subsequent membrane deposition limits failure to just four membranes, rather than failure of the whole CMUT array. In the early fabrication stages, an attempt was made to isolate each membrane with their own etch holes, thus improving yield even more. However, this was not achieved due to the limited 5 um space between membranes and feature size limitations on the maskless aligner.

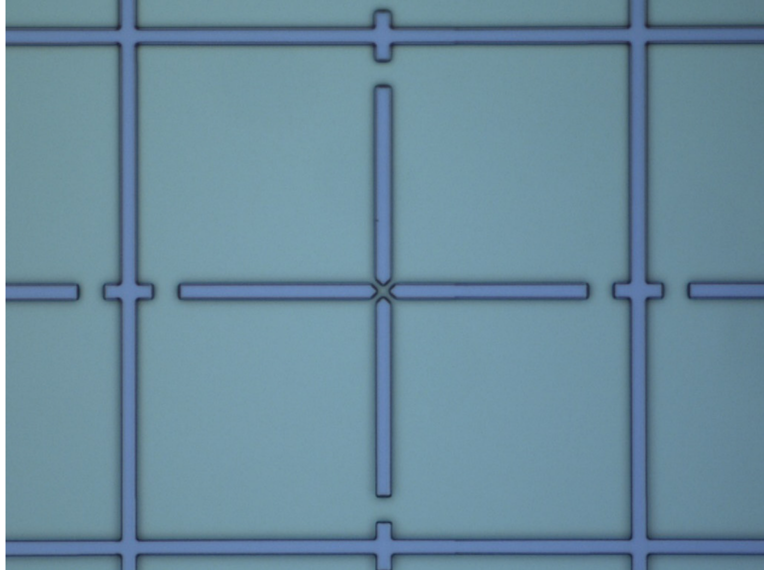


Figure 3.4 – Subsection of four membrane sacrificial pattern, defining the vacuum gap geometry.

3.1.1 Liftoff Ear Formation

A challenge faced during the fabrication of CMUTs with large 400 nm gaps was the formation of copper ears during the sacrificial layer deposition stage. These ears form as a result of metal depositing on the sidewalls of the photoresist during the evaporation process due to slight variations om the orthogonal angle. A profile of the height across the Cu sacrificial layer (conducted on a Tencor P15 Profilometer) is shown in Figure 3.5, showing the formation of ears on a test section in the boundary between the copper and oxide passivation layer. Although the height of these ears varies based on the location and amount of wafer misalignment in the evaporator chamber, they were measured up to 400 nm across multiple devices and can cause significant problems in CMUT yield. Due to their high aspect ratios, they can cause stress concentrations in the membrane after the sacrificial release, leading to cracks and loss of vacuum. Large ears also require a thicker deposition to seal the etch holes after the sacrificial release, needing to deposit a minimum

of the gap height + ear height to successfully seal the etch holes. This can be an issue if the desired membrane thickness is lower than gap + ear height, since an extra processing step would be needed to thin down the membrane without re-opening the etch holes.

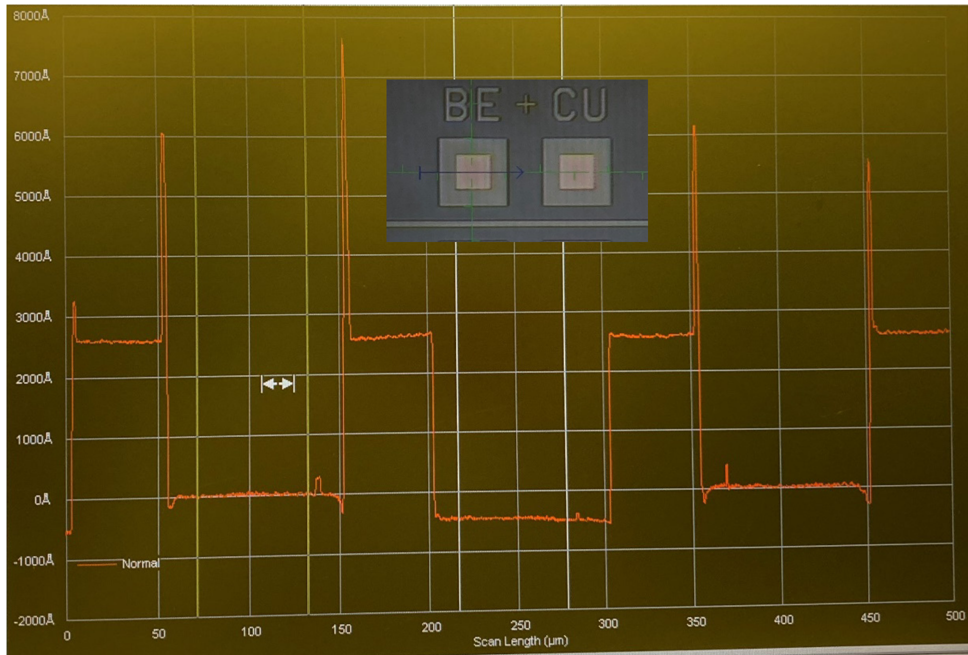
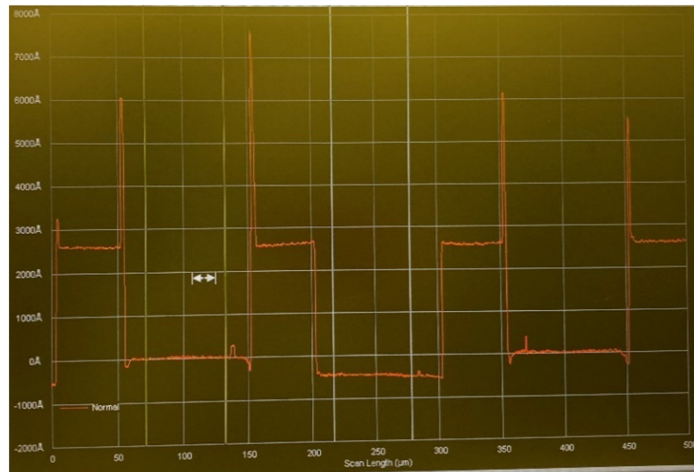
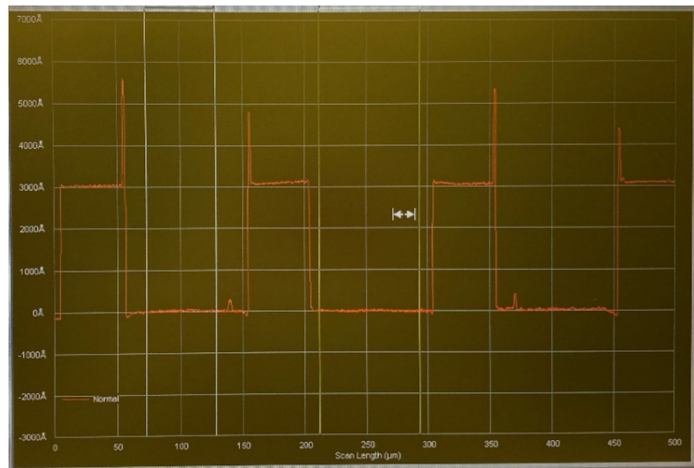


Figure 3.5 – Profile of high aspect ratio ears between sacrificial and passivation layer after lift-off.

A solution to reduce the effect of ears is to dip the wafer in a dilute etchant solution for the sacrificial layer. Since the aspect ratio and exposed surface area of the ears is much higher compared to the flat membrane region, the ears should etch at a much faster rate. The wafer with the devices shown in Figure 3.5 was dipped in a dilute solution of 20:1 APS100 copper etchant in 10s intervals. Figure 3.6 shows a timeline of the ear profile before and after 20s of ear removal etch. After 10s of etching, the ear height was reduced significantly with the highest aspect ratio ears reduced the most, while the sacrificial layer was reduced about 45 nm. After 20s of etching, most of the ears were reduced to below 100nm in height while the sacrificial layer was reduced a total of 65 nm.





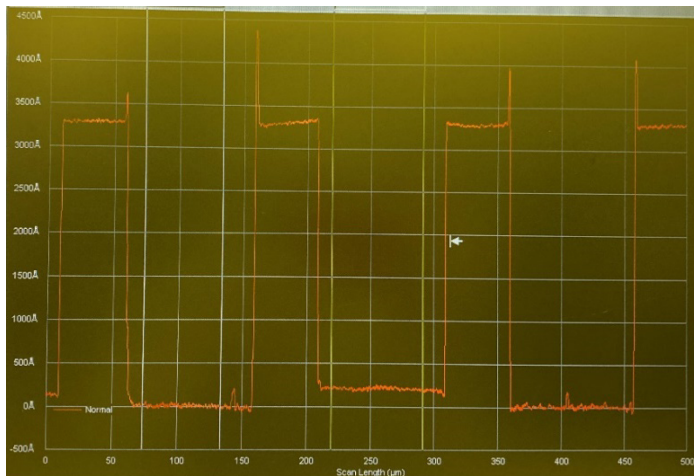


Figure 3.6 – Profile of ear geometries after a short etchant dip. Initial measurement (top), after 10 seconds (middle), and after 20 seconds (bottom).

Therefore, a diluted etchant bath proved to be a suitable method for reducing the formation of ears if its formation is unavoidable due to limitations in evaporator tooling. The reduction in sacrificial layer thickness can be accounted for in the initial evaporation thickness, allowing the ear removal etch to bring the thickness down to the desired value. A similar approach to minimize lift off ears was demonstrated by Dimaki et al. [18] to prevent metal ears after lift off from oxide. Instead of using an etchant to remove ears after their formation, they introduced an isotropic HF dip before the metal deposition to create a groove in the underlying oxide, showing reduction in ear height from 900 nm to below 50nm. This could be adapted for CMUT fabrication, as HF or buffered oxide etch (BOE) does not etch the underlying chromium. However, undercutting the oxide passivation layer undermines its purpose to some degree, especially when the passivation region is small to begin with. In this case, it may be more straightforward to skip the passivation layer entirely.

An alternative process to avoid ear formation is to deposit the sacrificial layer thin film first, pattern the vacuum gap through wet or dry etching, and deposit the oxide passivation through lift off if desired. However, it is difficult to control tight feature sizes with isotropic wet etching compared to the relatively anisotropic dry etch. Figure 3.7 shows the result of a sacrificial pattern with severe undercutting due to over-etching, with membrane geometries measuring 63 um compared to the 70 um photoresist pattern. As the copper on the 4” wafer completed etching at different rates, the amount of undercut varied on devices across the wafer. Etch rate uniformity can possibly be improved by choosing a different sacrificial material or modifying the etchant concentration for faster or slower

etch rates. Wet etching of sacrificial layers with lower thicknesses may have better uniformity, highlighting another challenge in fabrication of CMUTs with larger gaps.

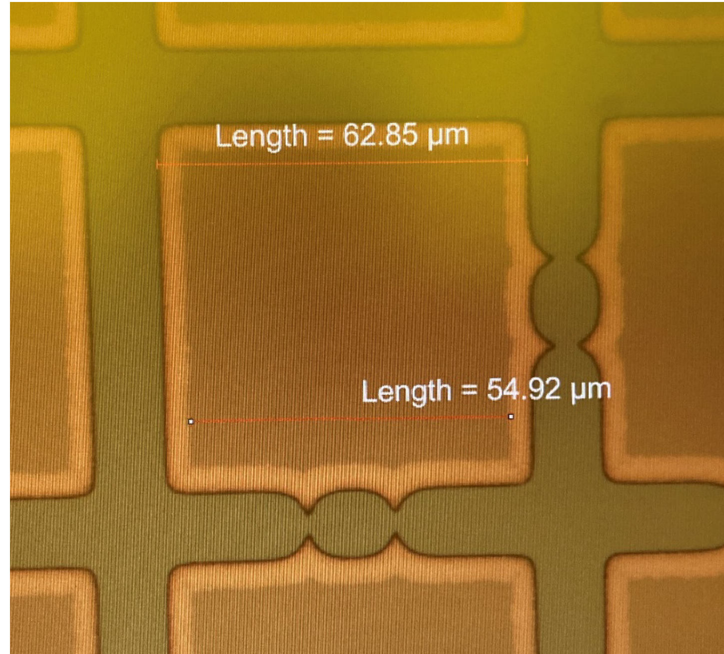


Figure 3.7 – Over etching of copper sacrificial layer by wet etch.

3.2 Sacrificial Release and Sealing

After lift-off of the sacrificial layer and removal of ears present, PECVD silicon nitride is deposited to form the membrane structure. Silicon nitride is used for its high dielectric constant (κ = 6-8) compared to silicon oxide (κ = 4) or silicon oxynitride [19]. High-κ dielectric materials such as hafnium oxide (κ = 16) through atomic layer deposition can also be used in designs with low vacuum gaps to increase the breakdown voltage [20], although these are design considerations more for CMUT applications in imaging rather than power transfer. Because a later nitride deposition will be required to seal the etch holes, the initial nitride is deposited to a thickness below the final membrane thickness, in this case 500 nm of the total 1500 nm. A low stress PECVD nitride recipe is used with a

deposition rate of 8.5 nm/min at 250 °C. A drawback of the sacrificial release process is the presence of thermal stress in the membranes which can become significant in large membrane designs. Thus, the wafer bonding fabrication method is more suitable for designs with either large membrane widths or small gaps in which membrane stress can cause contact with the bottom electrode. Figure 3.8 shows a profile across the nitride membranes after the first deposition stage; on the left, a profile of membranes with 200 nm ears, and on the right, a profile of membranes with minimal ears.

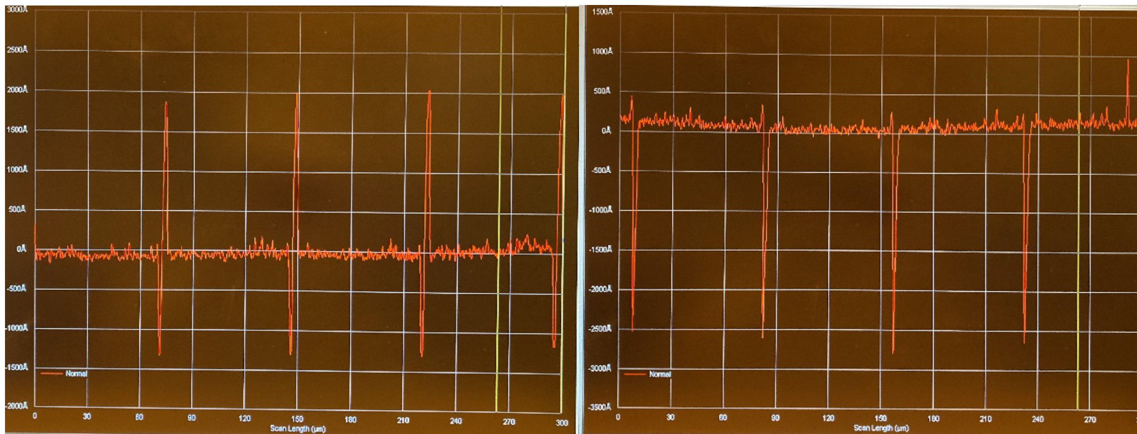


Figure 3.8 – Profile of membrane after first deposition with (left) and without (right) ears.

Nitride deposition thickness can be measured using reflectometry of nitride on oxide on silicon. However, for accurate measurement, the oxide thickness must be known and set in the reflectometer settings. Alternatively, measurement can be made on a dummy Si wafer placed next to the actual device in the PECVD chamber, as measurement of nitride on silicon results in less errors than nitride on oxide on silicon.

To begin the sacrificial release process, 3 um diameter etch holes are drilled down to the sacrificial layer using RIE, the third mask in the process. In this step, the copper acts

as the etch stop. Figure 3.9shows the location and pattern of the etch holes. The wet etching of the sacrificial layer is conducted in 10:1 APS100 copper etchant solution. As the etchant does not attack the chromium bottom electrode, the wafer can safely be left in etchant overnight. After 5 minutes of initial etching, the region around the etch holes should show a visible etch pattern as in Figure 3.10 (left). The completely etched vacuum gap is shown in Figure 3.10 (right).

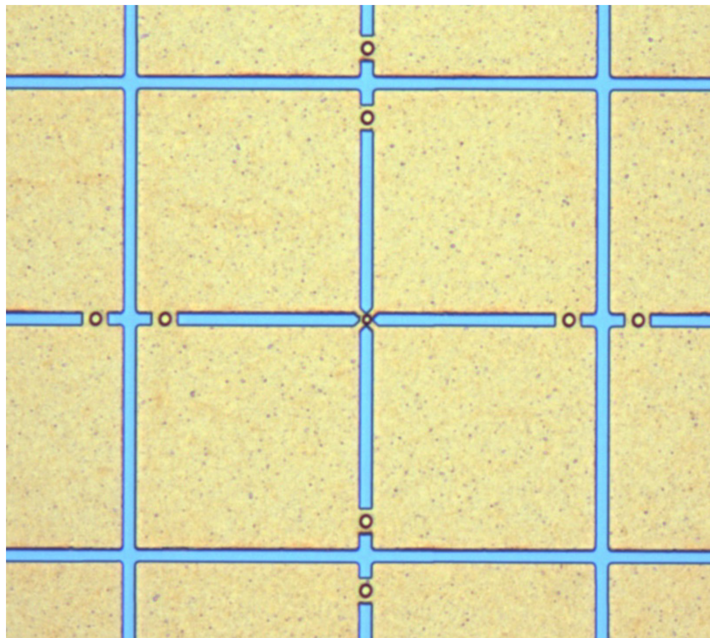


Figure 3.9 – Etch hole locations and pattern.

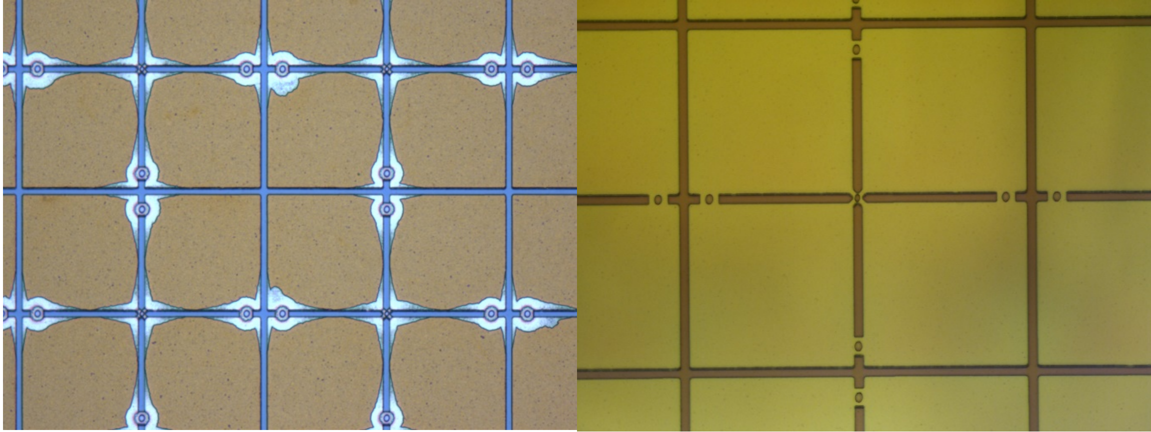


Figure 3.10 – Pattern after 5 minutes etching (left) and fully etched membranes (right).

To remove the etchant from the vacuum gap, the wafer is moved from the etchant into deionized water, and finally into isopropyl alcohol (IPA) and left overnight. The lower surface tension of IPA facilitates the complete removal of IPA in a 90 °C oven afterwards. For devices with relatively small gaps (<50nm), high stiction forces impede the ability for IPA to evaporate out of the vacuum gaps. In that case, supercritical drying can be used to insure proper fluid removal.

Sealing of the vacuum gap is achieved with a second low stress PECVD nitride deposition, bringing the membrane to the final thickness at the same time. Similarly, a dummy wafer should be used to measure the exact thickness of the additional nitride thickness. Successful sealing can be verified through immersion of the wafer in DI water/solvent and checking for leaks as well as profiling across the membrane. A deflection should be measured due to atmospheric pressure on the membrane as shown in Figure 3.11; for a 70 x 70 x 1.5 um nitride membrane, the expected atmospheric deflection calculated through FEA is roughly 80 nm.

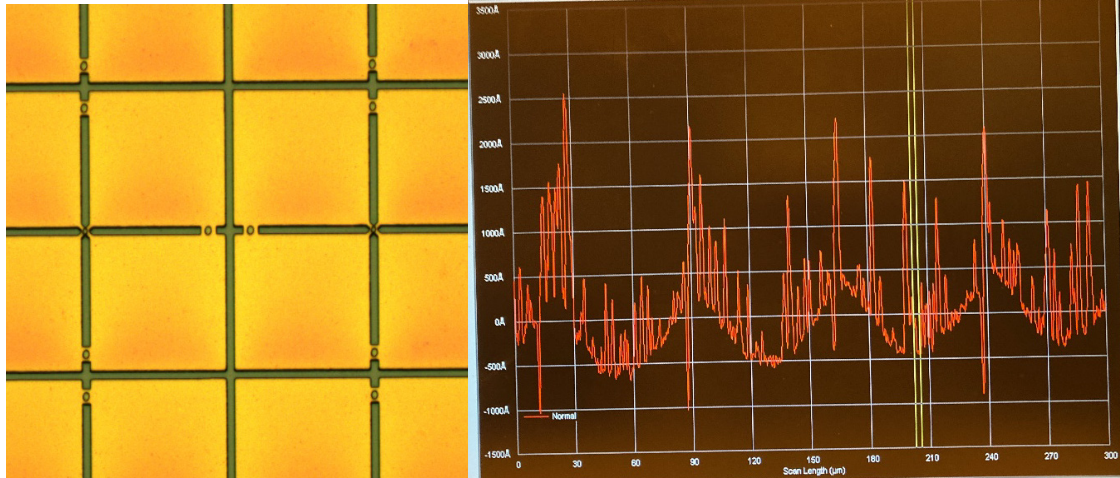


Figure 3.11 – Microscope image and profile of fully sealed membranes showing deflection due to atmospheric pressure.

3.3 Top Electrode and Device Packaging

The final top electrode patterning consists of sputtering a layer of metal, in this case 500 nm aluminum, and wet etching the excess aluminum in aluminum etchant type A solution. The top electrode can also be sandwiched between the membrane as in [21] in which case the capacitance of the CMUT is increased, leading to improved performance and sensitivity. An image of the top electrode pattern is shown in Figure 3.12 with ~84% electrode coverage over the membrane area.

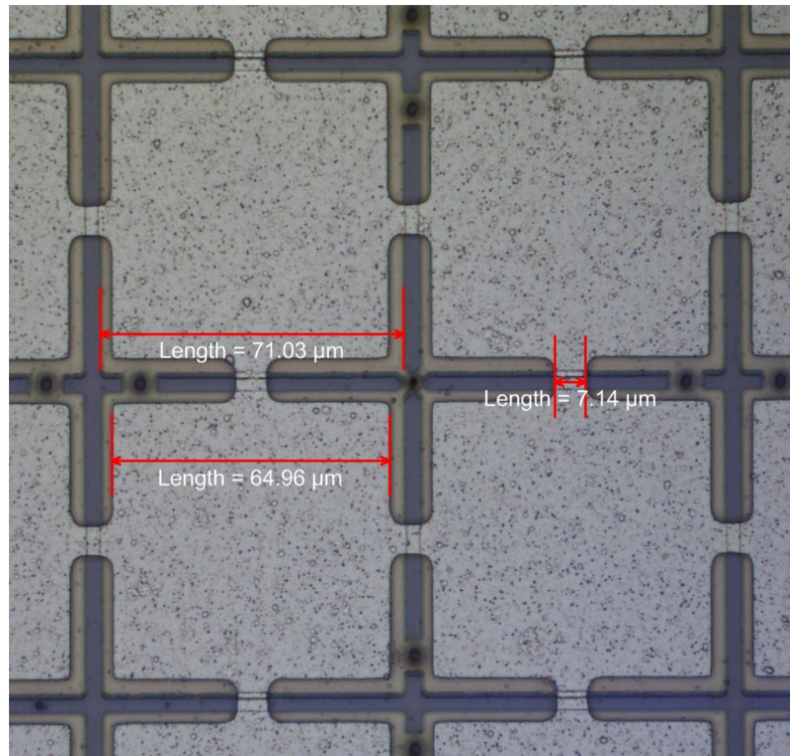


Figure 3.12 – Pattern and dimensions of aluminum top electrode on completed CMUT devices.

The final processing step is to dry etch bond pad channels to the bottom electrode for electrical connections. Thicker photoresist on the order of 7 um is used for this step since nearly 2 um of silicon nitride and oxide need to be dry etched. As the top electrode is the final layer in this design, wire bonds can be made anywhere aluminum is exposed. Images of the final diced CMUT arrays are show in Figure 3.13 along with measured device geometries in comparison to intended values in Table 3.1.

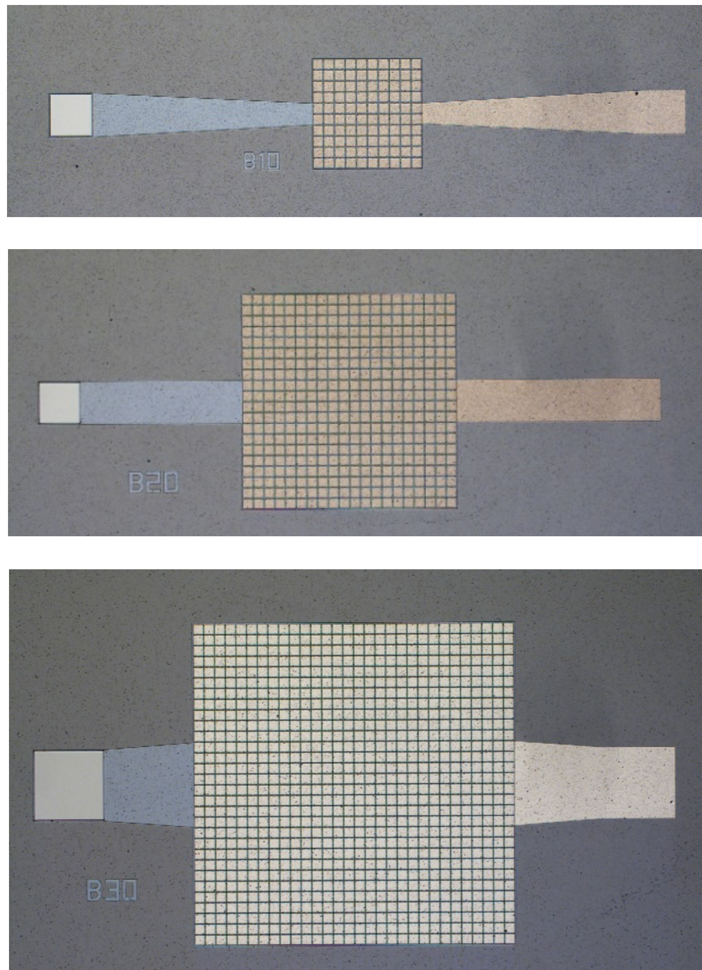


Figure 3.13 – Fabricated 10x10 (top), 20x20 (middle), and 30x30 (bottom) CMUT arrays with wire bond pads for bottom and top electrodes.

Table 3.1 – Measured Membrane Geometries vs Design

	Designed Values	Fabricated Values
Gap Thickness	400 nm	430 nm
Membrane Size	70 x 70 um	71 x 71 um
Membrane Thickness	1.5 um	1.478 um
Top Electrode Size	65 x 65 um	65 x 65 um
Top Electrode Thickness	500 nm	600 nm

CHAPTER 4. RESULTS AND EXPERIMENTAL VALIDATION

Simulations of various CMUT membrane designs using the large signal BEM model revealed insights that are overlooked in the lumped element 1D model. Most importantly, the BEM CPUT model reveals the effects of non-uniform motion and higher order mode shapes across the array, accounting for phase differences between individual membranes. This is a major limitation in the 1D lumped model, as acoustic crosstalk interaction between membranes are not accounted for. Differences in the operating frequency of CMUTs for imaging and power transfer applications are also explored by comparing frequencies of maximum pressure output vs. frequencies of maximum membrane displacement.

The 1D model also suggests that the quality factor plays an important role in the maximum power transfer efficiency, with higher quality factors leading to higher maximum efficiencies due to less energy loss. In terms of membrane design, increasing quality factor can be achieved by loading the membranes with a material of high density to stiffness ratio such as gold or tungsten. Doing so increases the mass of the membranes without increasing stiffness, leading to an increase in the quality factor $Q = \frac{\omega_0 m}{b}$.

Lastly, a power rectification circuit is designed with modifications needed to function in a parametric circuit. To prevent large losses in power during rectification, it was determined that a switching circuit should be implemented. With fabricated CMUT arrays of various sizes, the analysis performed through simulations are validated. After characterizing the devices to determine their impedances and operational frequencies, the BEM CPUT model is updated with the physical parameters of the devices. Simulations of

power transfer with the updated model are compared to experimental data. Separately, the power rectification circuit is built and demonstrated, both validating modeling and showing the effects of the switching circuit on power rectification efficiency. Analysis and discussion of each of the investigated topics are detailed in the following subchapters.

4.1 Frequency of Operation

The frequency response of a CMUT array is obtained by taking the Fourier transform of the far field pressure as a response to an impulse force. The far field pressure is calculated using Rayleigh's integral by summing the pressure contribution of each node in the array as if it were a baffled point source radiating into half space. However, unlike for imaging applications which prefer wide frequency bandwidths, the power transfer mechanism in CPUTs depends mostly on the change in capacitance and therefore, change in the mean displacements. Therefore, the Fourier transform of the mean membrane displacement can also be taken to find the frequency response of the CMUT. Figure 4.1 shows the mean displacement and pressure signal at a distance 10 cm away for a 10x10 membrane array in response to a impulse force at t = 2e-5s. The Fourier transform of the pressure signal shows membrane crosstalk peaks in the 1MHz range, but shows a broadband response at higher frequencies above 10 MHz. The Fourier transform of the mean displacement, however, shows maximum response in the crosstalk region.

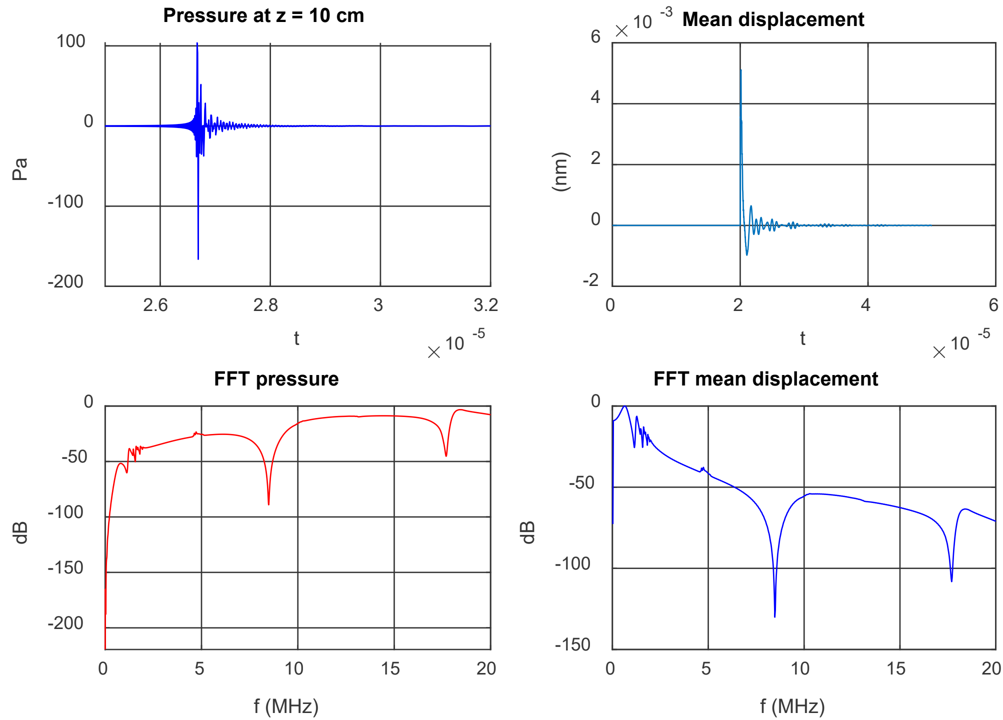


Figure 4.1 – Frequency response of far field pressure (left) and mean displacement (right).

A transient frequency sweep simulation in the crosstalk region from 0 to 2 MHz is conducted with a fixed forcing pressure of 100 kPa and resistive load of 100 Ω. The mean array displacement and the maximum membrane displacement in the array is plotted against frequency in Figure 4.2. The multiple peaks that appear within this frequency range correspond to the multiple array vibration modes; Figure 4.3 depicts the mode shapes for the first four major array modes and their frequencies for this specific membrane geometry. An interesting phenomenon occurs in which the higher order modes have larger maximum displacements but lower average displacements due to phase cancellation between patches of membranes. In the first mode, the array moves in phase, but the maximum displacement is only on the order of 60 nm. This is the frequency predicted by the baffled piston analysis as the uniform array motion most resembles a single baffled plate. In the second through

fourth mode, the maximum displacements reach values on the order of 200 nm. Despite high maximum displacements, the mean displacement, and therefore average change in capacitance, suffers. Additionally, the maximum displacement plot vs. frequency more closely resembles the pressure frequency response of the CMUT. This can be attributed to fact that the pressure is closely related to the individual membrane velocities (the piston velocity appears in Rayleigh's integral for pressure calculation).

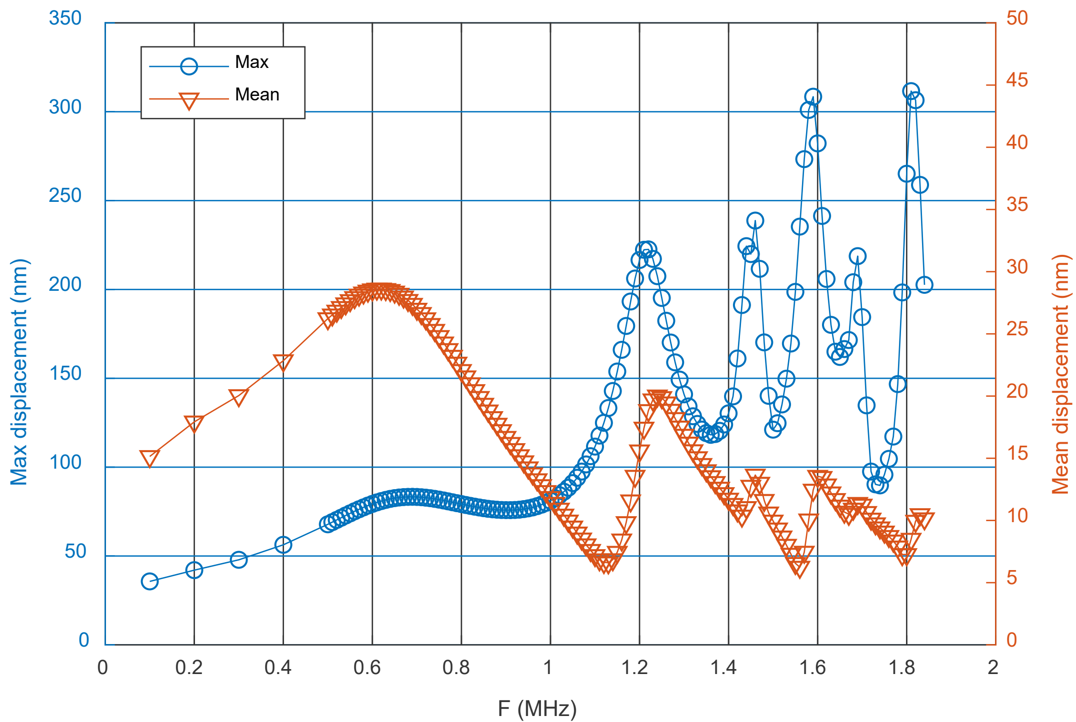


Figure 4.2 – Maximum and average array displacement from transient RLC simulation

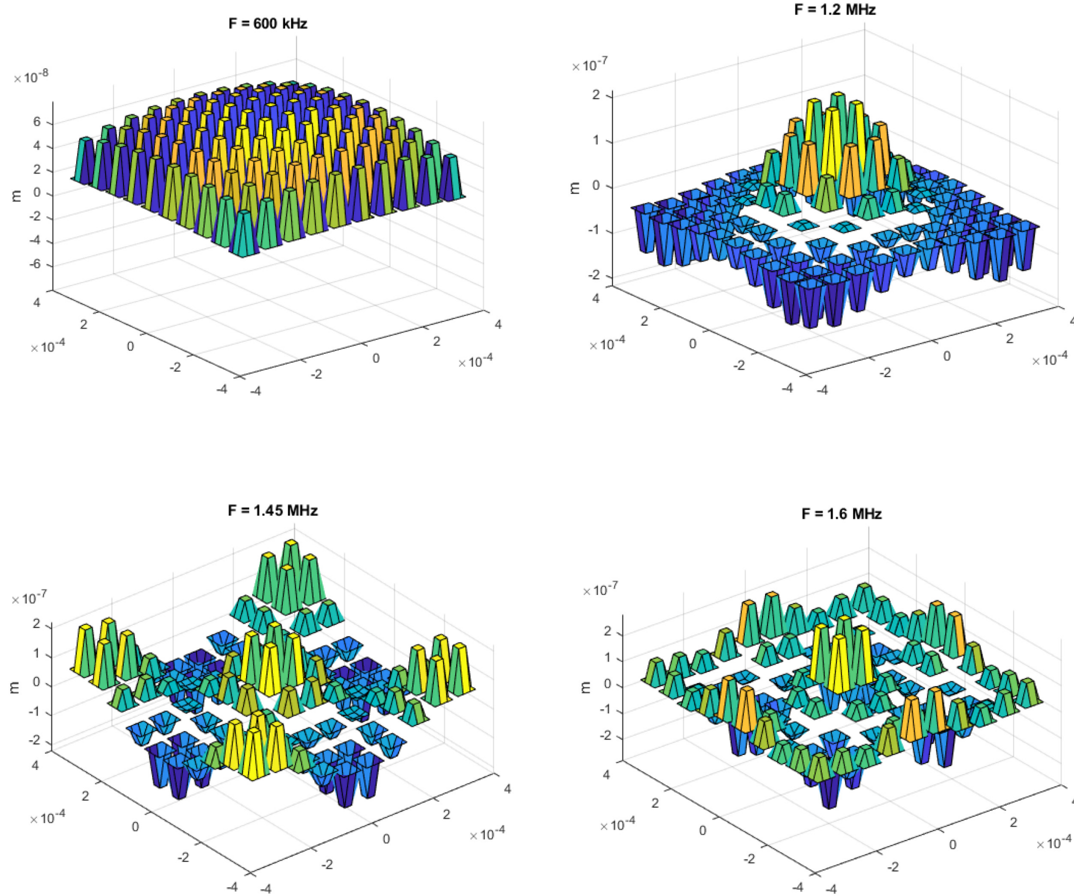


Figure 4.3 – Array mode shapes at the first four frequency response peaks

4.2 Power Transfer Simulations

Two CPUT arrays were designed to achieve operational frequencies in the 300 kHz-1.5 MHz range. The dimensions of both CMUT arrays are summarized in Figure 4.1. The first design is a 10 x 10 array of 70 x 70 μm membranes with a single membrane frequency of 1.01 MHz. Each membrane consists of a 500 nm silicon nitride membrane and 400 nm silver electrode, along with a gold mass load to increase the mechanical quality factor and force the membranes to operate in its first mode.

Table 4.1 – Two Mass Loaded CMUT Membrane Designs

	CPUT Array Design	
	Low Frequency 10 x 10	High Frequency 16 x 16
Si_3N_4 membrane	70 x 70 x 0.5 um	40 x 40 x 0.5 um
Ag electrode	70 x 70 x 0.4 um	40 x 40 x 0.4 um
Au mass load	23 x 23 x 1 um	13 x 13 x 1 um
Total array size	750 x 750 um	720 x 720 um

The first design is a 10 x 10 array of 70 x 70 µm membranes with a single membrane frequency of 1.01 MHz. Each membrane consists of a 500 nm silicon nitride membrane and 400 nm silver electrode, along with a 23 x 23 x 1 µm gold mass load to increase the mechanical quality factor and force the membranes to operate in its first mode. Silver was chosen as the electrode material due to its lower elastic modulus compared to aluminum, a secondary mean to increase quality factor. Membrane and electrode geometries were chosen to achieve a 1 MHz membrane frequency. The second design is a 16 x 16 array of 40 x 40 µm membranes with an array (as opposed to single membrane) mode frequency around 1 MHz. To do so, it was determined that the single membrane frequency needed to be near 3 MHz; hence the membrane dimension was decreased to 40 µm. The array size was increased such that the overall area remained approximately equal to the 10 x 10 array; this keeps the overall radiation impedance roughly the same between the two designs. The smaller membranes are mass loaded with a 13 x 13 µm gold block, while all thicknesses remained the same. Since the smaller 10 x 10 design has an array frequency near 300 kHz, we refer to the two designs as a low frequency device (10 x 10) and high frequency device (16 x 16).

Using the large signal BEM model, CPUT power transfer efficiencies for mass loaded membrane arrays can be determined. Figure 4.4 displays efficiency maps over a range of frequencies and forcing intensities at a fixed load. At low frequencies and high driving intensities, CPUT operation is limited by the capacitive membrane gap; there is a diminishing return to the relative capacitance change as forcing is increased. At higher frequencies and low forcing intensities, efficiencies also drop to zero as the forcing is below the threshold required for parametric resonance. For the low frequency device, power transfer efficiency does not vary between the first few array modes, averaging around 4%. For the high frequency device, power transfer efficiency reached up to 24% in the arrays second mode, with larger variations between array modes. However, the contour maps show efficiencies at fixed load values, while optimal power transfer efficiency is known to depend on forcing intensity and frequency.

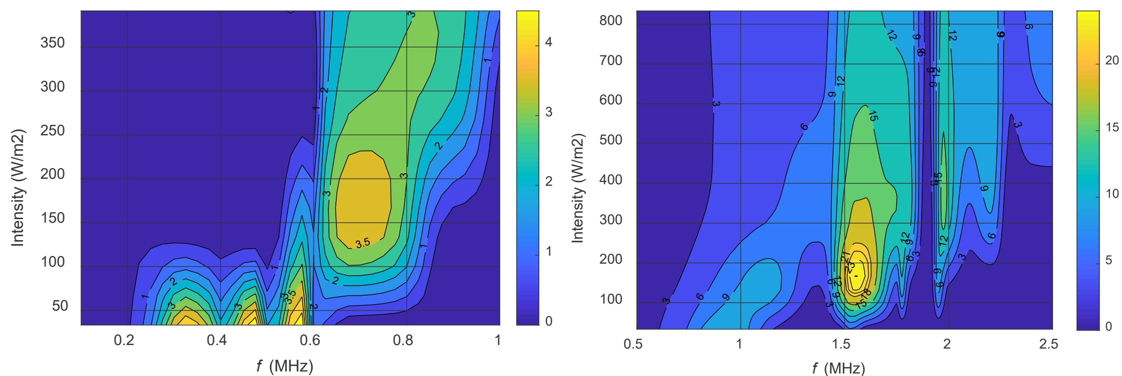


Figure 4.4 – Efficiency contour maps over frequency and forcing intensity for 10x10 (left) and 16x16 (right) CMUT arrays

Efficiency maps are therefore plotted at each of the array eigenfrequencies over a range of load values, thereby showing the optimal load impedances for each case. These maps, along with the corresponding array mode shapes are shown in Figure 4.5. Between

the low and high frequency design, power transfer efficiency is shown to reach up to 25%, although the highest efficiency does not occur at a common mode shape. The low frequency device for example, shows better efficiencies in the first array mode, while the higher frequency design shows better efficiencies in the second array mode. Observing the low frequency CPUT, with a 75 W/m^2 input intensity, 66.6 µW and 0.45 V DC is harnessed across a 3000 Ω load with 21.3% efficiency at 300 kHz. Under the same input conditions, operation at 475 kHz only provides 8.2 µW (0.07 V DC) across a 600 Ω load with 6.1% efficiency. Additionally, the input intensity can be increased beyond 160 W/m2 in the 300 kHz mode without significant decrease in efficiency, whereas in the 475 kHz mode, efficiency begins to drop once the input intensity increases beyond 70 W/m^2.

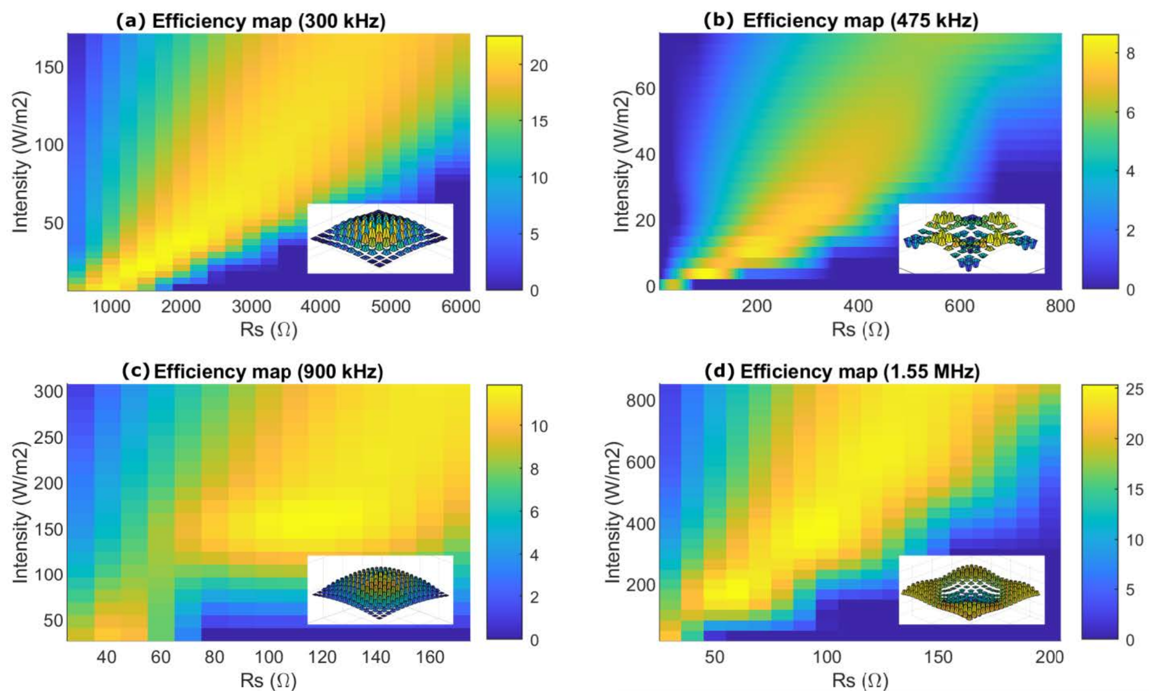


Figure 4.5 – Efficiency maps for first and second mode of low frequency CPUT at (a) 300 kHz, (b) 475 kHz and high frequency CPUT at (c) 900 kHz, (d) 1.55 MHz.

In contrast, the second array mode of the high frequency CPUT array provides better power transfer operation. At 1.55 MHz, 92.5 μW can be harnessed across a 140 Ω load (0.11 V DC) with 22.4% efficiency, while the first array mode only provides 22.0 μW across a 160 Ω load (0.06 V DC) with 11.3% efficiency. Also, unlike the low frequency CPUT, the second array mode of the high frequency device can be driven at higher input intensities without significant changes in efficiency.

These simulations show that complex modeling or experimentation is needed to determine the best array operating mode and condition, and using proper array modes, CPUTs can provide reasonable efficiencies over a large range of load conditions and ultrasound intensity variations. Note that, the simulations so far have been conducted with uniform ultrasound forcing on the array. This assumption is validated based on the fact that both arrays are sub wavelength in size; thus, an incoming ultrasound signal can be approximated as a plane wave, even with small variations in incidence angle. Larger forcing intensities can also be applied, although design changes such as a larger gap will need to be implemented to accommodate for such. The US Food and Drug Administration limits diagnostic ultrasound in tissue to 7,200 W/m^2 [22], while our high frequency device starts to reach its geometric limit around 800 W/m^2, meaning devices could be optimized to output power levels nearly 10x of that shown.

The presence of higher order array modes even with mass loaded membranes suggests that while mass loading can suppress higher order modes in individual membranes, fluid mass loading effects dominate on the array scale. As discussed previously, for array areas larger than 1 mm^2, fluid mass generally constitutes over 90% of the total effective mass. As a study, a theoretical CMUT array with a quality factor 50x the

low frequency devices is simulated. This is done by arbitrarily multiplying the stiffness and mass matrix [K] and [M] by 50 when solving the BEM CMUT model. The membrane resonant frequency doesn't change, but the quality factor is increased fifty-fold. The frequency response of the 10x10 array in fluid is maximum at 1 MHz, matching the single membrane frequency in air, rather than 300 kHz for the lower quality factor design (Figure 4.6). However, despite the large increase in membrane mass, the fluid mass still remains significant. The mode shape of the dominating frequency (Figure 4.7) contains regions that are out of phase with each other, meaning acoustical crosstalk forces are still in effect. Regardless, mechanical design of such a membrane with 50x quality factor is infeasible, meaning CPUTs need to be designed with these higher order array modes in mind.

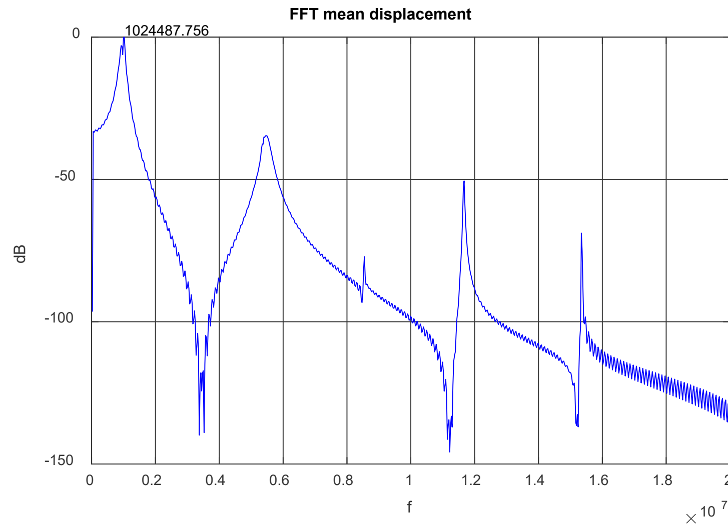


Figure 4.6 – Frequency response of high quality factor CMUT array

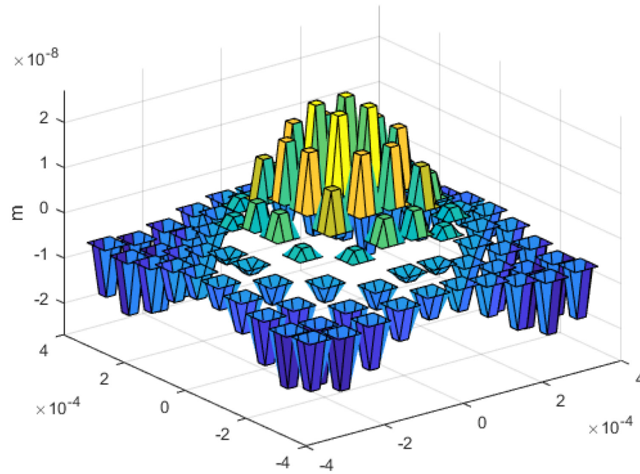


Figure 4.7 – Mode shape of high quality factor CMUT at 1 MHz

4.3 Power Transfer Validation with Fabricated CMUTs

The fabricated CMUTs of size 10x10, 20x20, and 30x30 are characterized on a network analyzer while applying a range of DC bias to determine center frequencies and device impedances. Figure 4.8 and Figure 4.9 are the real and imaginary components of the fabricated 10x10 device, from which the center frequency, resistance and parasitic capacitances can be deduced. The measure values for all the devices are tabulated in Table 4.2. The measured center frequency of the membranes is about 4 MHz, a 2% deviation from the 3.92 MHz calculated with FEA. Spring softening with application of DC biases up to 100 V is also clearly visible in the impedance measurements, a phenomenon in which increasing electrostatic forces decreases the stiffness matrix and in turn the resonant frequency [23].

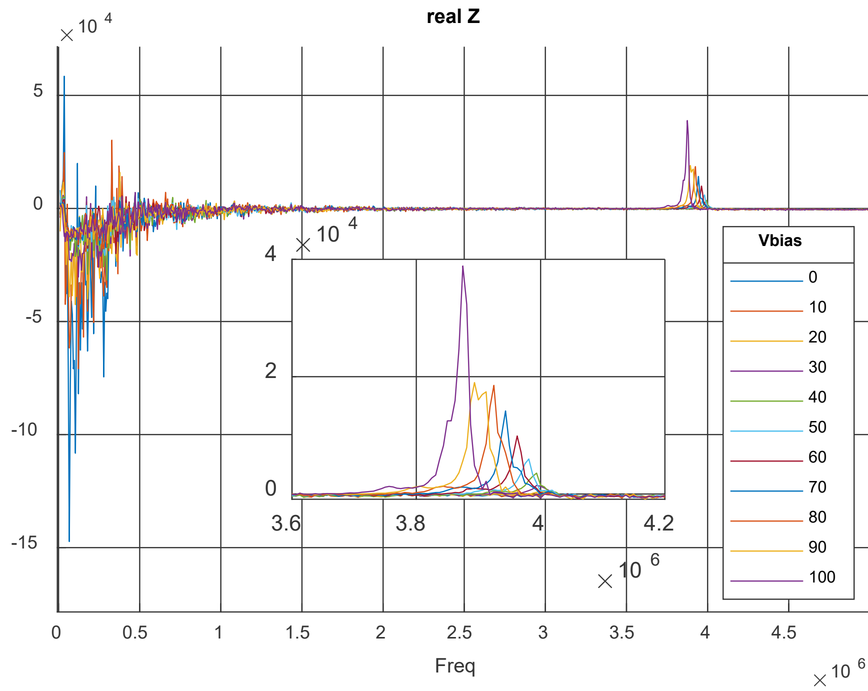


Figure 4.8 – Real component of 10x10 CMUT impedance

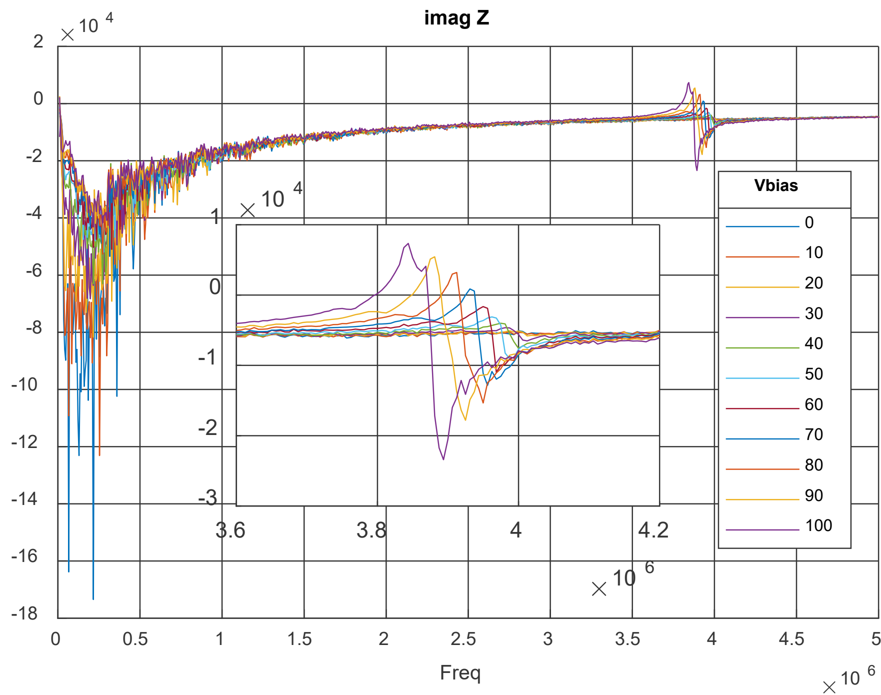


Figure 4.9 – Imaginary component of 10x10 CMUT impedance

Table 4.2 – Measured Device Capacitances and Parasitics

Device	Theoretical C_0 (pF)	Measured C_0 (pF)	Parasitic C (pF)
10x10	5.7	12.9	7.2
20x20	22.9	33	10.1
30x30	51.4	76	24.6

To determine the pressure frequency response of the CMUT in immersion, a hydrophone is used to measure the far field pressure of the CMUT in FC-70. A voltage impulse and DC bias is applied across the terminals of the CMUT, and the pressure response at a distance approximately 5 cm away is measured with a hydrophone. The frequency response for various DC bias values are plotted in Figure 4.10, showing a peak response in the 1.5-2 MHz range.

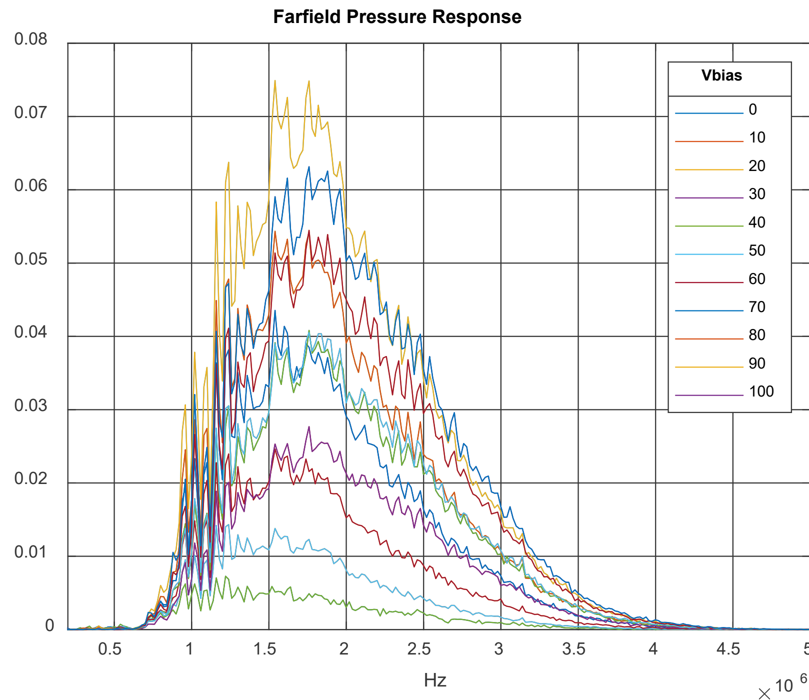


Figure 4.10 – Acoustical Frequency response of 20x20 CMUT array

Since the far field pressure according to Rayleigh's integral is a function of individual membrane velocities, obtaining the displacement response can be estimated by dividing the frequency response by ω in the frequency domain. The displacement response is show in Figure 4.11. In contrast to the pressure response, the maximum displacement response occurs closer to 1.25 MHz compared to 1.5 MHz. The cross talk region between 0.75 and 1.25 MHz shows multiple peaks and dips corresponding to various higher order array modes.

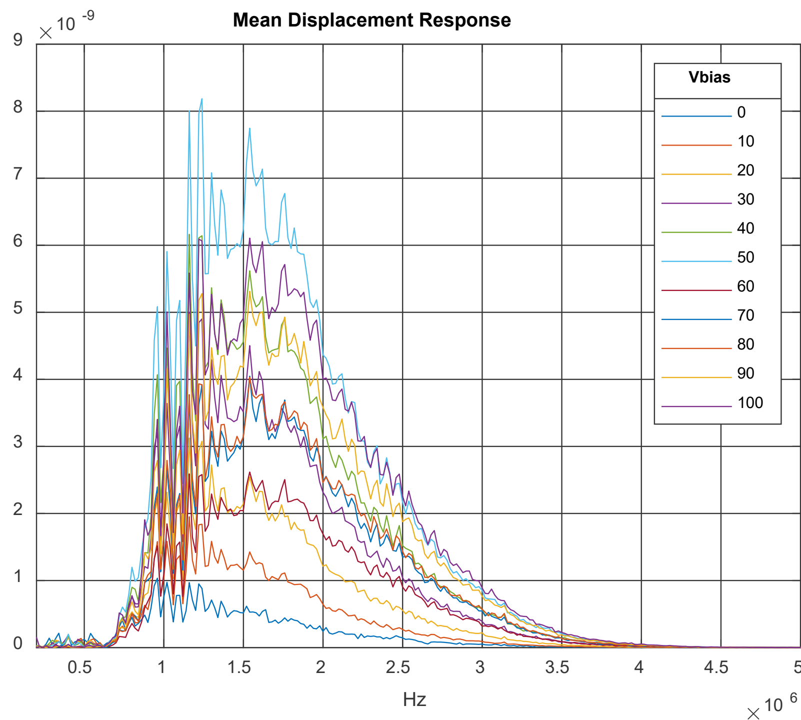


Figure 4.11 – Approximate mean displacement response of 20x20 CMUT array

A comparison of the relative magnitudes between simulation and experiment is shown in Figure 4.12. According to impulse simulations, the mean displacement magnitude is largest for the first array mode, decreasing for higher order modes. However, the displacement response as calculated from the pressure hydrophone measurements show a

peak response at modes in the 1 MHz range. This can be due to the fact that the pressure response is not derived from the mean velocity. The pressure at far field from Rayleigh's integral depends not only on membrane velocity but phase as well; thus, the pressure response does not directly correlate to mean velocity. Subsequently, derivation of mean displacement from the pressure response does not correlate well in terms of absolute magnitudes.

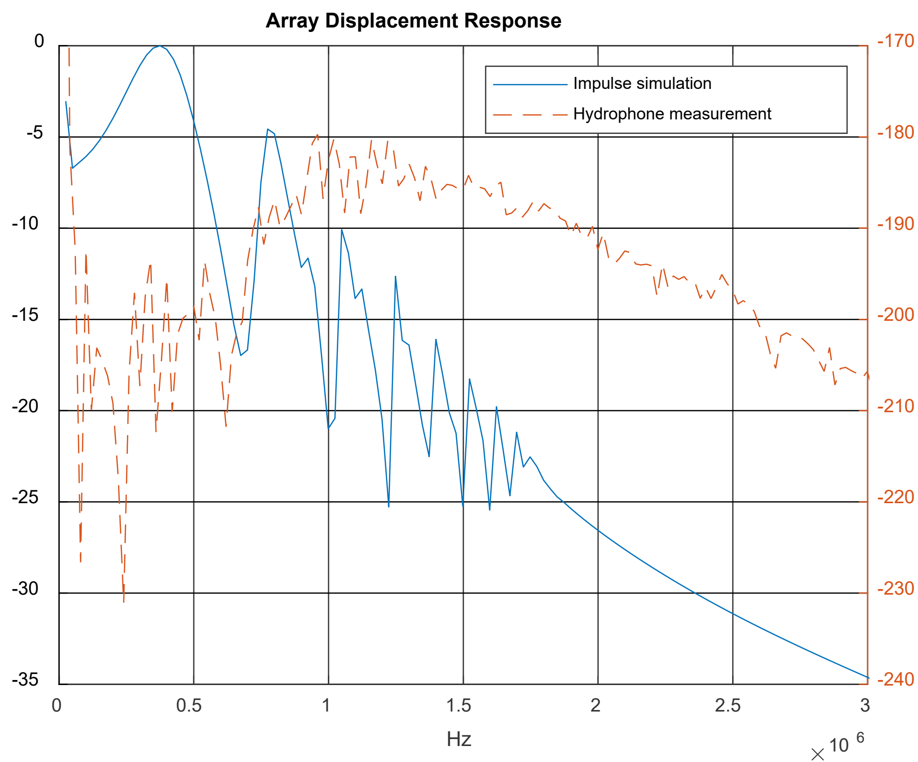


Figure 4.12 – Simulated displacement response vs. hydrophone measurement

More frequency peaks and valleys are also detected from experimental measurements as compared to simulations. This is not only due to noise, but also to the fact that the simulation of array modes utilizes symmetric boundary conditions, meaning asymmetric modes are not accounted for. In theory, asymmetric modes should also not

radiate any pressure along the center axis; however, radiation can occur at locations off center due to phase differences and measured, as is the case when the hydrophone is not exactly centered away from the CMUT. To investigate the parameters that impact power transfer the most, experiments are conducted at various frequencies at which the pressure or mean displacement magnitudes are maximum.

For experimental testing of power transfer, the CMUT devices are attached and wire bonded to a circuit board. A container is epoxied around the CMUT for immersion testing in FC-70. In Figure 4.13, a 20x20 CPUT is shown in the testing setup with a 1.4 mH inductance and variable resistor, corresponding to an electrical resonance of 737 kHz.

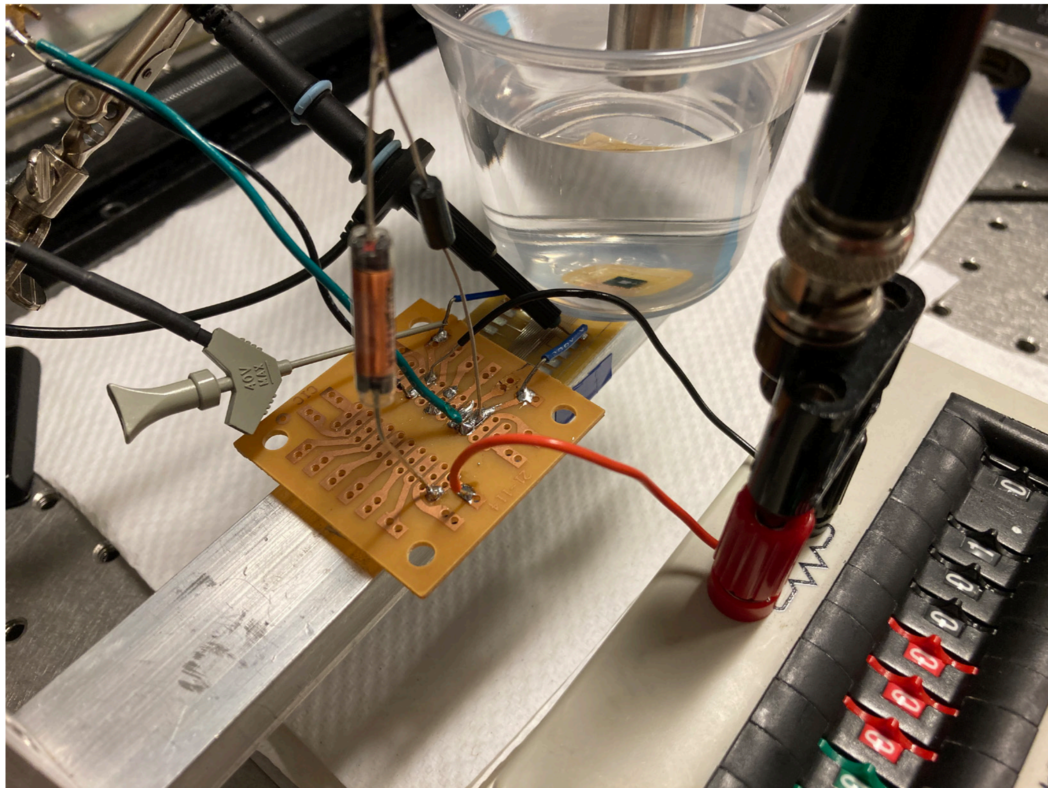


Figure 4.13 – Experimental setup of RLC CPUT in FC-70

The exact circuit resonance including additional parasitic capacitances from the measurement probes is measured by applying a voltage impulse across the resistor and measuring the response of the voltage across the capacitor array (Figure 4.14). The measured circuit resonance is in reality closer to 620 kHz, a significant deviation from the theoretical 737 kHz. Thus, the additional parasitic capacitance and inductances introduces a correction factor of approximately 1.4 to the product LC as in equation 13.

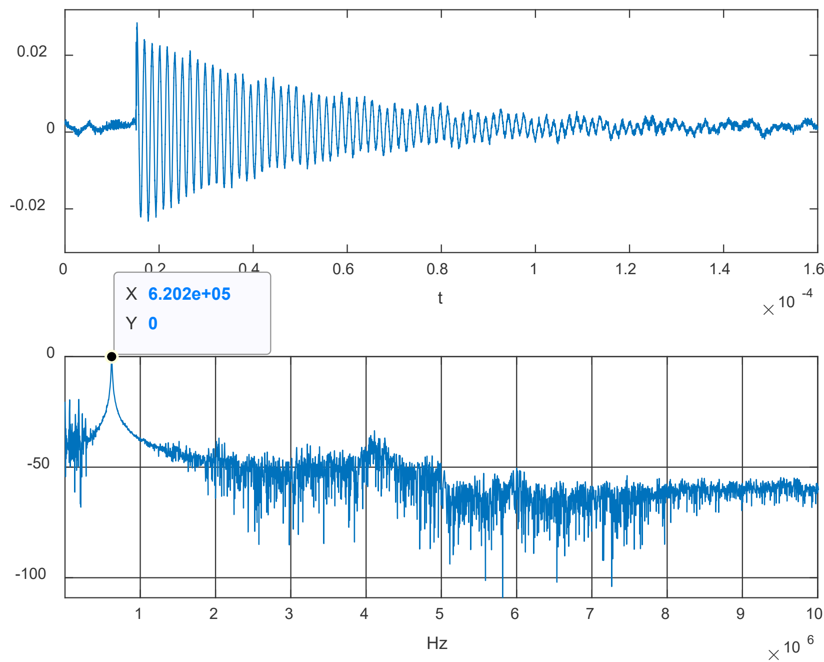


Figure 4.14 – Circuit response to impulse voltage and corresponding circuit resonance

$$\omega_e = \frac{1}{2\pi\sqrt{1.4 * LC}} \tag{13}$$

Ultrasonic forcing is applied using a 1 MHz immersion piezoelectric transducer (Olympus A303S) at a distance of approximately 5 cm, placing the CPUT in the far-field region of the transducer; thus, the signal is approximately a plane wave. The voltage across the

variable resistor is measured to determine the electrical power output while the resistance is swept from 0 to the critical load. The output power for three frequency peaks in the pressure response (Figure 4.11) is plotted in Figure 4.15. The peak to peak voltage applied to the ultrasound transducer is also noted, as this value and the distance from the CPUT is required to measure the pressure at the same distance for later efficiency calculations.

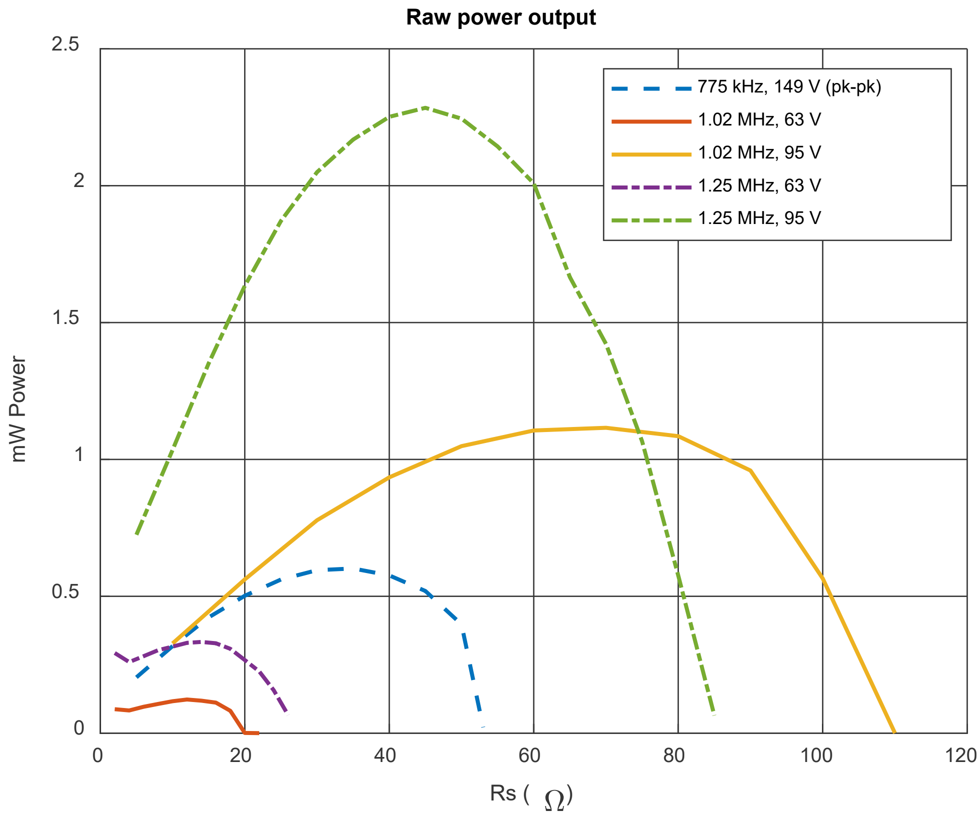


Figure 4.15 – Electrical power output vs. load resistance for various frequencies and forcing pressures.

A few conclusions are made from the output power data. The output power is zero under no load, increasing to a maximum at an optimal load when the circuit impedance matches the acoustic impedance, then drops to zero at the critical load. Increasing the applied forcing level (applied voltage to transducer) increases the critical load. According to

simulations, the critical load has a direct linear correlation with input forcing pressure as long as the membranes are not collapsing, i.e. all displacements are less than the gap. Increasing the applied pressure force by a factor of *n* also increases the critical load by the same factor *n.* However, the added resistances from the capacitive array, inductor, and other components essentially creates a voltage divider between the load resistance and the added parasitic resistances. Since the parasitic resistance does not change, it is desirable to operate with larger forcing pressures such that the optimal load resistances are larger with respect to the parasitic resistance. In the experimental results at 1.25 MHz operation, two forcing levels are recorded with transducer driving voltages of 63 and 95 V peak to peak, corresponding to a pressure increase of 1.5x. The critical load, however, increases from roughly 36 Ω to 95 Ω, an increase of 2.6x. In order to bring the critical load ratio to 1.5, an additional resistance of 82 Ω should be included such that (95 + 82) Ω / (36 + 82) Ω = 1.5. This 82 Ω is consistent with the measured 20x20 CPUT resistance of 88 Ω using a network analyzer as shown previously in Figure 4.8. It is therefore beneficial to reduce CPUT parasitic resistances as much as possible through judicious design and fabrication, for example by designing shorter interconnects, thicker electrodes, and choosing materials with lower resistivity. However, care must also be taken to keep parasitic capacitances at a minimum as well, highlighting some of the intricacies that go into CPUT design.

4.4 Power Rectification Simulation and Experiments

To determine the effectiveness of the switching circuit and power rectification efficiencies introduced in Chapter 2.5, simulations are run with a smaller 4x4 CMUT model to save computational resources and time. Both cases in which the rectification circuit is in parallel with the load R_0 (no switching logic involved) and cases in which the output is

actively switched between R_0 and R_L are run. Concurrently, the power rectification circuit with switching logic is built and shown in Figure 4.16, comprised of 1N5817 Schottky diodes and a Texas Instruments SN74LVC1G3157 SPDT analog switch. The two yellow wires correspond to the input and output of the rectifier, and the two orange lines depict the switch between the unrectified load R_0 and a half bridge rectified load R_L with a single Schottky diode. The blue line is the signal that controls the switching when the voltage exceeds the diode forward voltage.

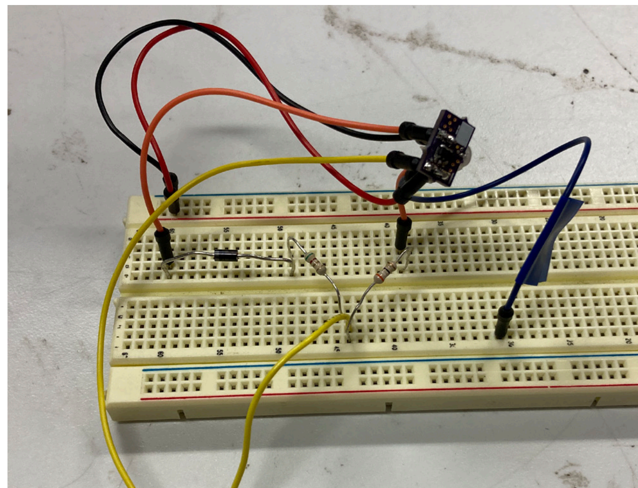


Figure 4.16 – Power rectifier and switching logic circuit

The CPUT is formed using three elements of a commercially available Philips CM12 CMUT. The device area totals 1.8 mm^2 with a capacitance of 60 pF and a mechanical center frequency of ~1 MHz in FC-70 fluid. The particular CPUT only produced sufficient voltages for a half bridge rectifier, so simulations were modified for half wave rectification as well. Across a range of R_L values, voltage levels were measured across R_0 and R_L and used to calculated power across the loads, with rectifier efficiency being calculated as

$$\eta_{rect} = \frac{P_L}{P_L + P_0} \tag{14}$$

Figure 4.17 compares rectifier efficiencies between simulation and experiment, with and without active switching with a half bridge configuration. Additionally, full bridge power rectification efficiencies from simulations with and without switching logic is shown in Figure 4.18. Since simulations and experiment were done with CPUTs with different array geometries, the load resistance is normalized to the critical load for valid comparison.

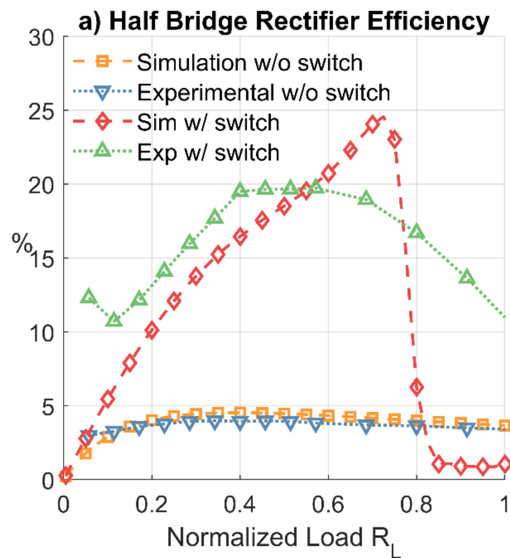


Figure 4.17 – Simulation vs. Experimental half bridge rectifier efficiencies

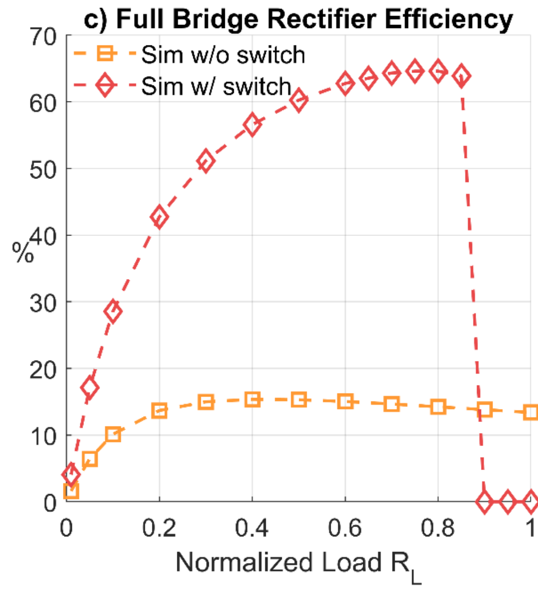


Figure 4.18 – Simulation of CPUT with full bridge rectification

Rectification efficiencies without the switching logic implemented show a maximum of 4% with excellent agreement between simulation and experiment. The low efficiency is due to R_L and R_0 essentially functioning as resistors in parallel. A significant amount of power is lost across R_0 without the switching circuit. As previously mentioned, the necessity of R_0 is a limitation on energy harvesting in parametric circuits. When the switching circuit is implemented, rectification efficiencies improve to 20-24%, a five-fold improvement from previously. However, this value is still only half of the theoretical 40% maximum efficiency for half bridge rectifiers because the diode voltage drop constitutes a significant loss compared to the relatively low input voltages. With a full wave rectifier, the switching circuit improves rectifier efficiency from 15% to 65% when R_L is optimized. Nonetheless, inclusion of a switching circuit is proven to be an essential component of power rectification in CPUTs by preventing energy losses while maintaining optimal conditions for maximum power transfer.

CHAPTER 5. CONCLUSION

Through the efforts of this research, a more comprehensive analysis on CPUTs as a means of wireless power transfer is shown. Using a multiple degree of freedom model, validated through experimental power transfer with a CMUT designed for imaging, an improved CMUT was designed for the purposed of maximum power transfer. It is shown that the operating conditions for optimal power transfer occur under different conditions than for optimal imaging applications. For imaging, large bandwidths, large pressures, and smaller vacuum gaps are preferred, while for power transfer, the array mode shape and frequencies impact total power transfer efficiency the most. Larger gaps are also necessary due to the larger displacements encountered, and therefore, typical microfabrication processes should be adapted for the fabrication of large gap CMUTs, especially with the formation of metal ears during the lift off process. Under ideal operating conditions, CPUTs are shown to be able to transfer power in the mW range over a 2.25 mm^2 device, making it a comparable alternative to piezoelectric counterparts. Finally, due to the limitations of parametric circuits, passive power rectification is achieved by implementing a switching circuit to control a diode bridge. The switching circuit is shown in simulation and through experimental demonstration to improve rectification efficiencies significantly, showing the practicality of a full end to end ultrasound based power delivery system.

5.1 Further Work

The flexibility of CMUT array design allows for optimization at multiple stages of design. This work has shown methods to design individual membrane widths and

thicknesses for a desired frequency, but has explored only arrays with uniform membrane geometry. A list of possible design considerations for future exploration include:

1. *Non uniform array geometries*: It is shown that power transfer efficiency can be higher in array modes with out of phase regions. Since theses regions contribute negatively to performance, membrane geometries in these areas can be modified to suppress their effects. The electrodes can also be removed from those regions, in which case the acoustic response is not impacted significantly, but power transfer can be improved.
2. *Self-contained powering of rectification circuit components*: The power rectification components such as the SPDT integrated circuit and comparator op-amps are powered with laboratory power supplies in experiments. However, due to their low power draw, they can potentially be powered by the CPUT itself for a truly passive system. A portion of the CMUT array with a separate top electrode can be dedicated for powering theses devices, and a voltage multiplier circuit can be used to increase the low AC voltage output into a steady DC value to power the ICs.
3. *Effects of varying incidence angle*: The effect of varying the ultrasound forcing intensity was studied in simulation by changing the forcing level on each membrane uniformly. However, this does not account for phase variation across the array, which can be inaccurate for larger array sizes or higher frequencies. A more detailed study on incidence angle should be conducted by applying accurate forces with phase delays across the array.

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