DENSE 3D HETEROGENEOUS INTEGRATION USING SELECTIVE COBALT ALD DEPOSITION AND RECONSTITUTED TIERS

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DENSE 3D HETEROGENEOUS INTEGRATION USING SELECTIVE COBALT ALD DEPOSITION AND RECONSTITUTED TIERS

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SUMMARY

In this thesis, a new fine-pitch low-temperature bonding technology using selective Cobalt (Co) ALD deposition is presented. The benefits of selective Co ALD bonding are nanometer-scale controllability, low planarity requirement, low bonding temperature (200 ^{o}C) and potential for ultra-high-density bonds. To demonstrate selective Co ALD bonding, a Cu/Gap/Cu three-layered structure, which emulates 3D ICs stacking, is fabricated and carefully characterized. The testbed shows seamless Co interconnection between the Cu pads after Co ALD deposition for 1000 cycles. The electrical measurements demonstrate over 90% yield, which prove the Co connectivity between the Cu pads.

Moreover, in this thesis, a new type of SiO_2-reconstituted-tier stacking technology is proposed. The SiO_2-reconstituted-tier stacking technology utilizes low-temperature ICP-PECVD SiO_2 to encapsulate multi-sized chiplets. After ICP-PECVD SiO_2 encapsulation, the through-oxide-vias and the pads are formed on the SiO_2 to complete the reconstituted tier before stacking. Compared with conventional epoxy-molding-compound-based stacking, the SiO_2 approach can have smaller loss tangent (10x), lower CTE mismatch (3x) and the higher via density (>400x). The thickness of the proposed technology can be over 10 times smaller than conventional epoxy molding. The two technologies, with further analysis and studies, open up exciting new opportunities for future 3D IC heterogeneous integration.

CHAPTER 1: INTRODUCTION

1.1 Slow Down of Moore's Law:

The semiconductor industry has thrived in the past five decades by following Moore's law for transistor scaling. Moore's law was originally an observation from Gordon Moore in 1965 in the journal of Electronics: "The complexity for minimum component costs has increased at a rate of roughly a factor of two per year [1]." During the 1975 IEDM conference, Gordon Moore revised the projection of transistor doubling rate from every year to every two years [2]. Transistor scaling every two years corresponds to the doubling of computational performance for every 18 months if the energy consumption remains constant [2]. After five decades of improvement, the transistor line width has scaled from approximately 25 μm in 1961 to about 10-20 nm in 2021 [2] [3]. The semiconductor industry is now implementing EUV lithography systems to produce 3 nm node gate-all-around MOSFET and beyond [3] [4].

However, lateral transistor scaling can not continue forever. Figure 1 illustrates that performance scaling has slowed down over the past decade [5]. With exponentially increasing investment costs and process difficulties, shrinking down the transistors laterally may no longer be a sustainable business model [6] [7]. Besides the difficulty of scaling the transistors, back-end-of-line (BEOL) interconnects also face challenges as the dimensions scale e.g. increased interconnect RC delay, which is shown in Figure 3 [8] [9]. Therefore, we need new materials and technologies to overcome these challenges.

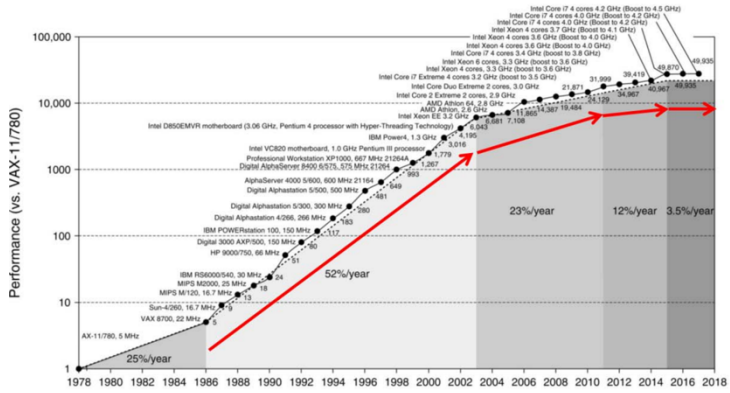


Figure 1 Computational performance vs. time [4]

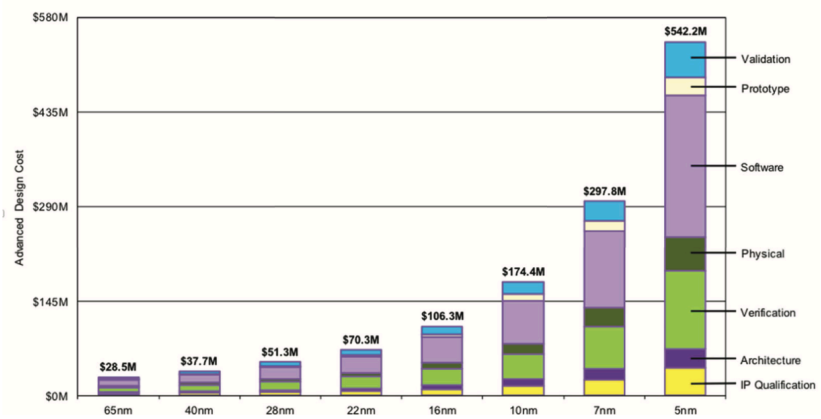


Figure 2 Exponential increase for design cost at advanced nodes [6]

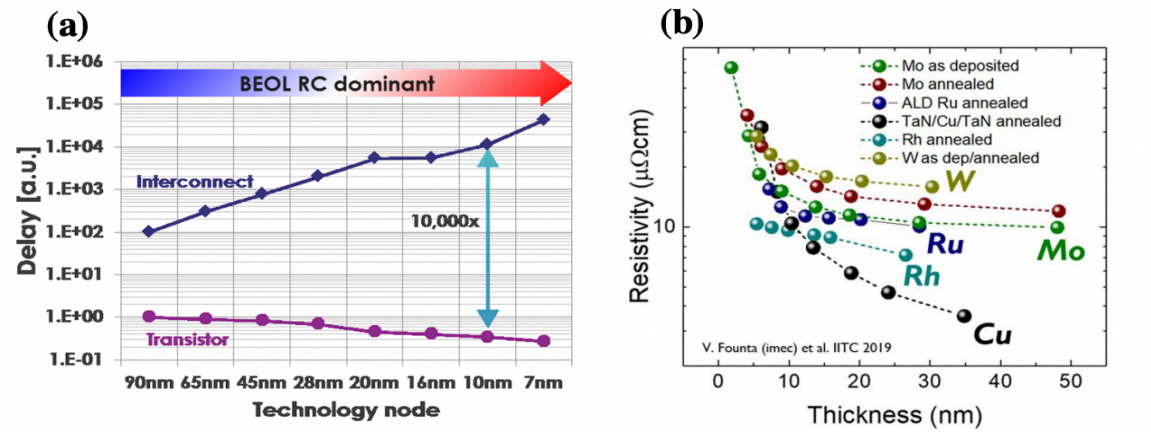


Figure 3 (a) Relationship between interconnect RC delay and the technology node, (b) Cu resistivity increases with scaling [8] [9]

1.2 Heterogeneous Integration

One method to improve the system's performance is heterogeneous integration. According to the definition from the Heterogeneous Integration Roadmap (HIR) 2019: "Heterogeneous integration refers to the integration of separately manufactured components into a higher-level assembly (System in Package – SiP) that, in the aggregate, provides enhanced functionality and improved operating characteristics [10]."

Heterogeneous integration has multiple advantages over a traditional 2D monolithic chip. Some of the advantages include larger data transmission bandwidth, better thermal solutions, smaller form factor, faster time to market, and flexibility in combining different nodes or functions of chips [11]. The cost reduction is another main reason due to the capability of reusing legacy designs, higher yield for smaller die size, and the option to select the most suitable process node for different functional blocks [12].

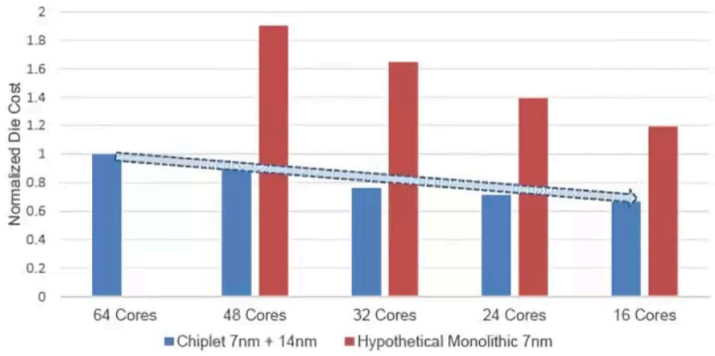


Figure 4 Comparison of normalized cost reduction for homogeneous and heterogeneous integration [13]

The cost saving from heterogeneous integration is one main driver for industry. AMD, GlobalFoundries, Intel, TSMC and some other major companies have studied the cost comparison with monolithic and heterogeneous approaches [13] [14]. Figure 4 shows the comparison of disintegrating a monolithic chip into multiple chiplets, and the studies

show that the normalized die cost can reduce by approximately 50% when each chiplet is selected from the most cost-effective process node [13].

The bandwidth density and energy efficiency can greatly improve by using heterogeneous integration. The bandwidth between memory and CPU is a key bottleneck for high performance computation. Figure 5 shows high bandwidth memory (HBM), which was developed by SK Hynix, AMD and Samsung, stacks multiple memory dice with through-silicon vias (TSVs) and solder microbumps to decrease the distance between the memory and the processor [15]. Due to the fine I/O pitch, multilayer stacking, and the close distance between chips, the HBM can reduce PCB footprint by three times and reduce the energy-per-bit by four times compared to a GDDR5 memory [16]. HBM2 can achieve 2 Gb/s pin speed, 256 Gb/s bandwidth per chip, and operates at 1.2 V supply volage [17].

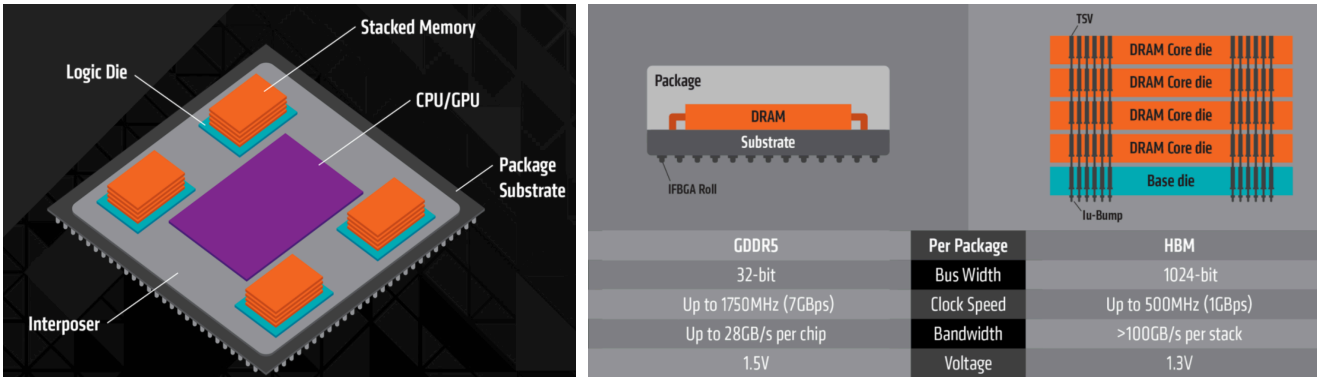


Figure 5 AMD HBM schematic and performance comparison [17]

1.3 Definition for 2D/3D Heterogeneous Integration

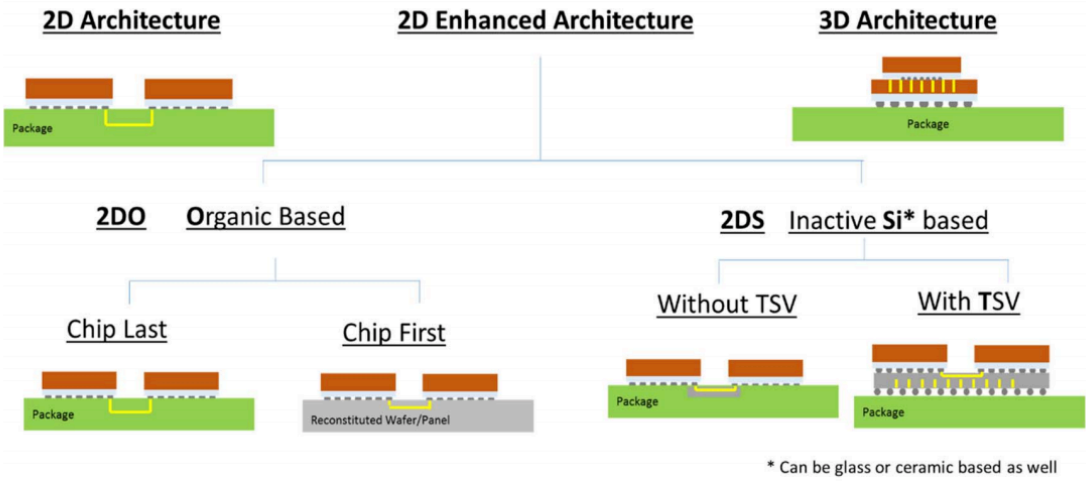


Figure 6 Classification from 2020 Heterogeneous Integration Roadmap [18]

The Heterogeneous Integration Roadmap 2020 (HIR 2020) has defined the different heterogeneous integration architectures into three groups: 2D, 2D Enhanced and 3D. From the HIR 2020:

- 2D: "A 2D architecture is defined as an architecture where two or more active silicon devices are placed side-by-side on a package and are interconnected on the package [18]."
- 2D Enhanced: "If the interconnect is 'enhanced', i.e., has higher interconnect density than mainstream organic packages, and is accomplished using an organic medium, the architecture is further sub-categorized as a 2DO (2D Organic) architecture and similarly, if the enhanced architecture uses an inorganic medium (e.g. a silicon/glass/ceramic interposer or bridge) the architecture is further sub-categorized as a 2DS architecture [18]."

- 3D: “A 3D architecture is defined as an architecture where two or more active silicon devices are stacked and interconnected without the agency of the package [18].”

1.4 3D Heterogeneous Integration

In the past three years, there have been lots of new 3D architectures and processes proposed by major semiconductor fabrication companies. For example, TSMC’s System on Integrated Chips (SoIC) [19], Samsung’s X-Cube [20], Intel’s Foveros [24], and GlobalFoundries’ hybrid wafer bonding (HWB) [22].The schematics of these architectures are shown in Figure 7. X-Cube and Foveros utilize solder microbumps at approximately 10-30 μm pitch for die bonding. SoIC and HWB use hybrid bonding that can shrink the pitch to below 10 μm.

TSMC’s SoIC is shown in Figure 7 (a). The SoIC is a multi-tier and multi-chip 3D integration method. This architecture can flexibly integrate both frontend 3D and backend 3D technologies. The backend 3D technologies are the well-developed TSMC InFO or CoWoS platform that can integrate the chip with the package. The frontend 3D technologiy is face-to-face bonding between two dice with bonding pitch as small as 9-0.9 μm [19]. Although the bonding method has not been disclosed yet, the method is bump-less and potentially a type of hybrid bonding based on Figure 7 (a). Compared with microbumps, which are 36 μm in pitch, SoIC increases the bump density to about 1-3 orders, and the bandwidth density increases by more than 191 times [19]. The bonding quality between dice is very critical and is affected by Cu cleanliness, Cu recess size, and misalignment [19]. Besides the bandwidth improvement, the SoIC bump-less bonding decreases the total

die thickness to 36% of a conventional 3D die stack that uses microbumps [21]. The smaller stack thickness can improve the power consumption by 20% [21].

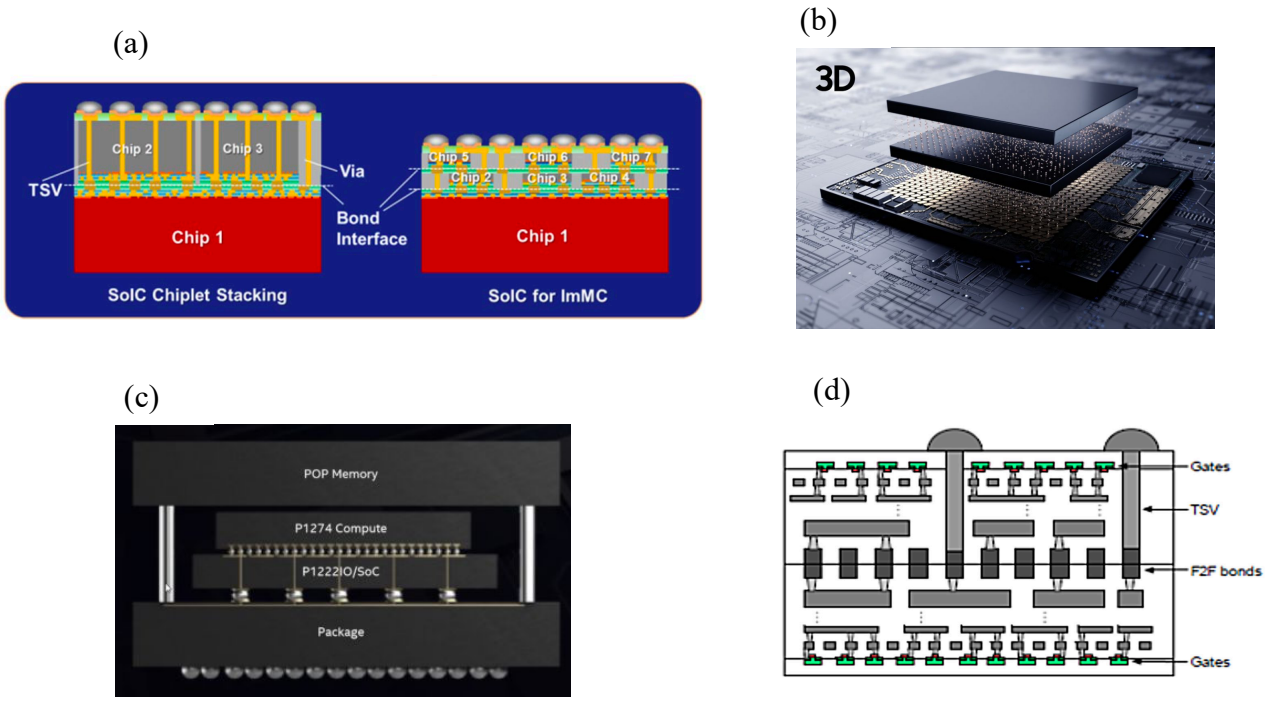


Figure 7 (a) TSMC SoIC [19], (b) Samsung X-Cube [20], (c) Intel Foveros [24], (d) GlobalFoundries HWB [22]

Globalfoundries developed a hybrid bonding process, which is called hybrid wafer bonding (HWB) for 3D integration (Figure 7 (d)). The HWB connects two dice face-to-face with through-silicon vias (TSVs) on one of the die [22]. The TSVs can be revealed after the dice are bonded and thinned down. The dice can be measured before and after bonding by the revealed TSVs. The smallest pitch is 5.76 µm and their next goal is to shrink below 2 µm. Due to the scaling of the pitch, hybrid-bonding 3D architecture demonstrated 10 times better bandwidth density and energy-per-bit by comparison to a 3D architecture that uses solder microbumps [23]. In a recent study in 2020, hybrid-bonded 3D integration

demonstrated 1.6-2.4 Gb/s pin speed, 204.8-307.2 Gb/s aggregated bandwidth and 0.013-0.021 pJ energy-per-bit [23].

Intel demonstrated Foveros as a TSV-based 3D logic-on-logic architecture in 2019. Foveros enables face-to-face stacking of two different logic dice together by microbumps at approximately 55-36 μm pitch. Each microbump consists of a Cu pillar, diffusion barrier and SnAg solder. The precise control of the bump height and the intermetallic compound are major factors to create a void-free joint. The bottom die has mid-processed TSVs that can connect the top die and the package. The TSV is formed by Bosch Si etch with oxide passivation layers and Ta barrier before the Cu electroplating [24]. The extra Cu, Ta barrier and oxide passivation layers are removed by CMP to expose the TSVs at the front side for the BEOL RDL. The exposure of backside TSVs can be processed by grinding a wafer to approximately 75 μm thick [25]. In terms of performance, Foveros 3D integration shows 0.5 Gb/s pin speeds, 12.5 Gb/s aggregated bandwidth and 0.2 pJ for energy-per-bit [26].

1.5 2D Enhanced Heterogeneous Integration (2.5 D)

Beside 3D heterogeneous integration, 2D enhanced architectures, more commonly called 2.5D, are also very important. Examples of 2D (inactive-silicon-based enhancement) are TSMC's chip-on-wafer-on-substrate (CoWoS), Intel's embedded multi-die interconnect Bridge (EMIB), and Georgia Tech's heterogeneous interconnect stitching technology (HIST). Examples for 2D (organ-based enhancement) are TSMC's wafer level integrated fan-out (InFo).

Intel's EMIB is one example of 2.5D architecture, as seen in Figure 8 (a). EMIB is constructed by embedding a thin silicon bridge die in an organic package to create a localized connection between the edges of two active dice. The organic substrate is etched to form the cavity for the bridge chip [27]. After placing the bridge chip in the cavity, the bridge chip is encapsulated by laminating a dielectric build-up film followed by via-formation. The active die is bonded onto the organic substrate with the bridge chip through vias and microbumps. The bridge chip thickness is <75 μm and has multi-layered RDL interconnections to allow high-density signal transmission [28]. The bump pitch of EMIB is 55 μm for AIB Gen1 protocol with 2-2.8 Gb/s bandwidth-per-pin, 1.5 Tbit/s/mm^2 bandwidth density, and 0.85-1.2 pJ energy-per-bit [29] [30].

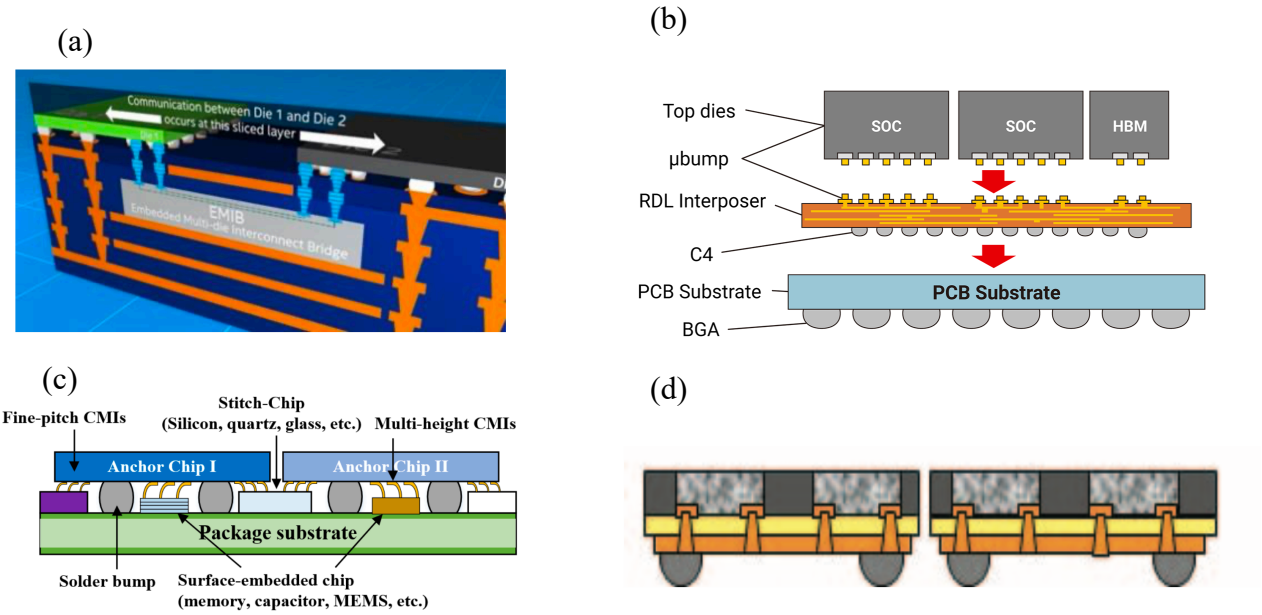


Figure 8 (a) Intel EMIB [27], (b) TSMC CoWoS [31], (c) Georgia Tech HIST [36],

(d) TSMC InFO [33]

TSMC's chip-on-wafer-on-substrate (CoWoS) is shown in Figure 8 (b). The CoWoS architecture uses a passive silicon interposer that has TSVs and high-density RDL.

The interposer acts as an intermediate layer to connect between active die and the package substrate. The interposer first bonds with the active die by microbumps; then the interposer is flip-chip bonded with the organic package substrate using C4 bumps. In this way, multiple dice can be connected through the interposer to generate high-density lateral communication. The interposer size can be as large as 2500 mm^2 by quadruple mask stitching to reach three full reticles [31]. The microbump pitch is approximately 40 μm for the LIPINCON interface with 0.56 pJ energy-per-bit, 8 Gb/s bandwidth-per-pin and 1.6 $Tbit/s/mm^2$ bandwidth density [32].

Another example of 2.5D architecture is Georgia Institute of Technology's heterogeneous interconnect stitching technology (HIST) for flexible polylithic 2.5 D platform. As shown in Figure 8 (c), stitch-chips with fine-pitch compressible microInterconnects (CMIs) provide flexible interconnections between multiple "anchor chips." The solder bumps form reworkable mechanical bonding between the anchor chips and package substrate [33]. CMIs can have multiple heights and pitches to accommodate different sizes of chiplets [34]. The CMIs have 20 μm in-line pitch size with 40 μm height and compressibility of up to 20 μm. From electromagnetic simulations, 90 μm tall CMIs with 500 μm long channels can have less than -0.4 dB insertion loss using quartz stitch-chips [34].

For organic based 2.5 D architecture, TSMC's integrated fan-out (InFO) wafer level package is a key technology. In Figure 8 (d), InFo uses epoxy molding compound (EMC) to encapsulate the die so that the bump location can be extend out from the silicon die area to increase the I/O count [35]. To fabricate an InFo package, the bare silicon die is first picked and placed onto a carrier substrate. The die, which is facing up, is then molded using

EMC. After grinding down the EMC to expose the pad, RDL layers and the bumps are formed onto the surface. The smallest RDL line width is 0.8 μm for ultra-high-density lateral connection, and the RDL can have up to 5 layers [36]. From the simulation results, InFo can have 0.424 pJ energy-per-bit, 0.3 Tbit/s/mm^2 bandwidth density, 36 μm die-to-die I/O pitch and 130 μm C4 bump pitch [37] [32].

To sum up, we have discussed the motivation, benefits, and few proposed definitions of heterogeneous integration technologies. Also, different examples of 2D and 3D heterogeneous integration technologies have been listed with discussion of their design, fabrication, and key metrics.

1.6 The Scope of This Thesis

In this thesis, a new fine-pitch low-temperature bonding technology using Cobalt (Co) ALD deposition is presented. The demonstrated Co ALD bonding, which can be deposited at 200 ^{o}C, has the potential to decrease the interconnect pitch down to the nanometer scale without requiring compression force or extreme surface conditions.

Moreover, in this thesis, a new 3D stacking method using SiO_2 low-temperature deposition to encapsulate multiple chiplets is proposed to form a SiO_2-reconstituted-tier for further batch-bonding processes. The SiO_2-reconstituted-tier stacking has the benefits of ultra-high density vias, low CTE mismatch between chiplets and SiO_2, low latency, and higher thermal dissipation capability relative to some integration platforms today.

CHAPTER 2: LITERATURE SURVEY OF HIGH-DENSITY INTERCONNECTS

2.1 High-density I/O

One major challenge facing the industry is how to enable high-bandwidth and low-loss communication between chips. Although increasing the data rate can increase the bandwidth, the trade-off will be higher power consumption and larger circuit area for equalization [38]. Another approach is to increase the density of Input/Output (I/O) interconnects, which increases the bandwidth between chips while maintaining circuit area and power trade-offs. Figure 9 shows the growth of 3D interconnect density across technologies versus years [39].

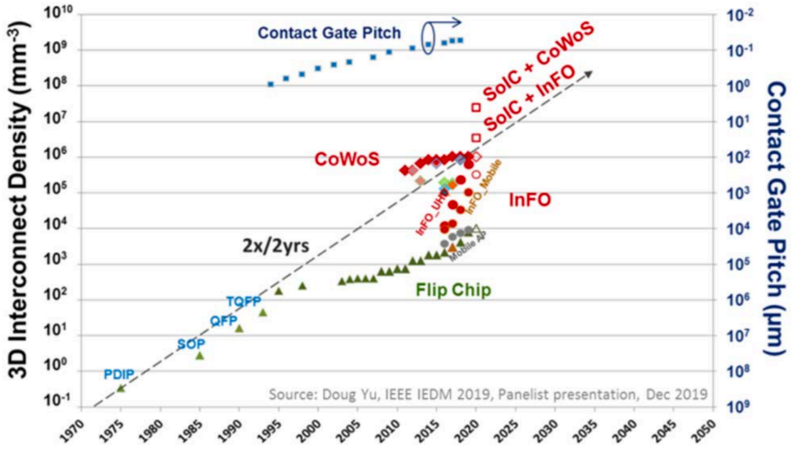


Figure 9 3D interconnect density over time [39].

Figure 10 shows the historical and projected I/O technologies to meet future demand [40]. In the past, the conventional method of bonding was solder bump technology, which is based on tin-based alloy with the pitch being 300-50 µm. As solder bumps continue to scale down to their projected limit of around 20 µm, they will face a number of

problems, including bridging between bumps, brittle intermetallic compound, and poor thermal stability [41]. The intermetallic compound can quickly consume the solder to form voids in between the joints under elevated temperature environment [42].

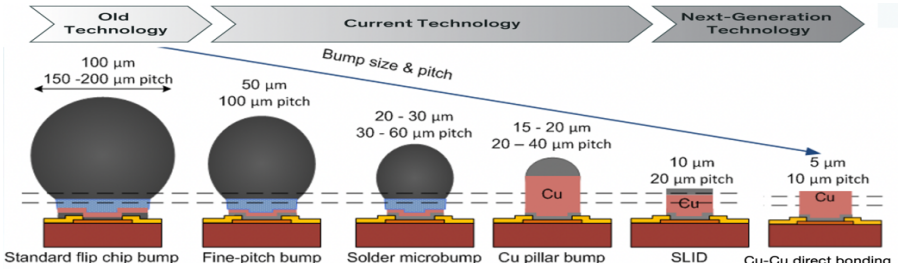
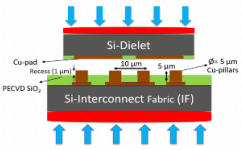
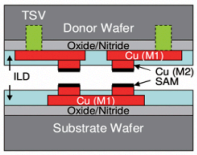
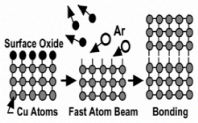
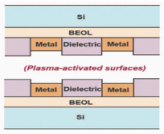
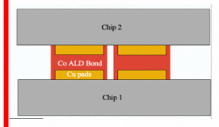


Figure 10 Trend of I/O bonding (Adapted from [11])

2.2 Prior Work on Cu-Cu Bonding Related Methods

Table 1 Comparison of different Cu-Cu bonding technologies

	Direct Thermal Compression [42]	Self Assemble Monolayer [82]	Solid-Liquid Interdiffusion (SLID) [55]	Surface Activation [50]	Hybrid Bonding [59]	Co ALD Bonding
Diagram						
Temperature (ºC)	350	250	200	25	150-300	200 ºC
Bonding Pressure (Pa)	$2.5x10^{-2}$	Atmospheric	10^{-3}	$2x10^{-5}$	Atmospheric	$8x10^{2}$
Bonding Force (MPa)	64	6.6	0.4	64	Unknown	No Force
Pitch (µm)	10	15	20	6	1.6	30
Surface Roughness	CMP 2.6 nm	CMP	CMP 1.2 nm	CMP 1.9 nm	CMP	No CMP 25 nm

Starting in the early 2000s, Cu-Cu bonding emerged as a technology to enable I/O pitch scaling. Cu-Cu bonding uses Cu pillars or Cu pads to bond and is suitable for high-density bonding. Cu-Cu bonding can prevent bump bridging and has outstanding electrical

conductivity, electromigration resistance, and thermal conductivity performance [43]. Moreover, Cu is already a well-understood material system for back-end-of-line (BEOL) redistribution layers (RDL) and through-silicon vias (TSV)s [43] for industry to implement. Table 1 lists six different Cu-Cu bonding approaches for high density I/O, and the following paragraphs will describe each bonding method. Selective Cobalt (Co) Atomic Layer Deposition (ALD) bonding is the method proposed in this thesis and will be discussed in detail in Chapter 3. Lastly, technology mapping of different Cu-Cu bonding methods is shown in Figure 11; all values are extracted from Table 1. The X-axis is bonding temperature, the Y-axis is bonding pitch size, and the size of the circle is the tolerable surface roughness. From Figure 11, selective Co ALD bonding has relatively low bonding temperature and much larger surface roughness tolerance range, which is approximately 25 nm from current experiments.

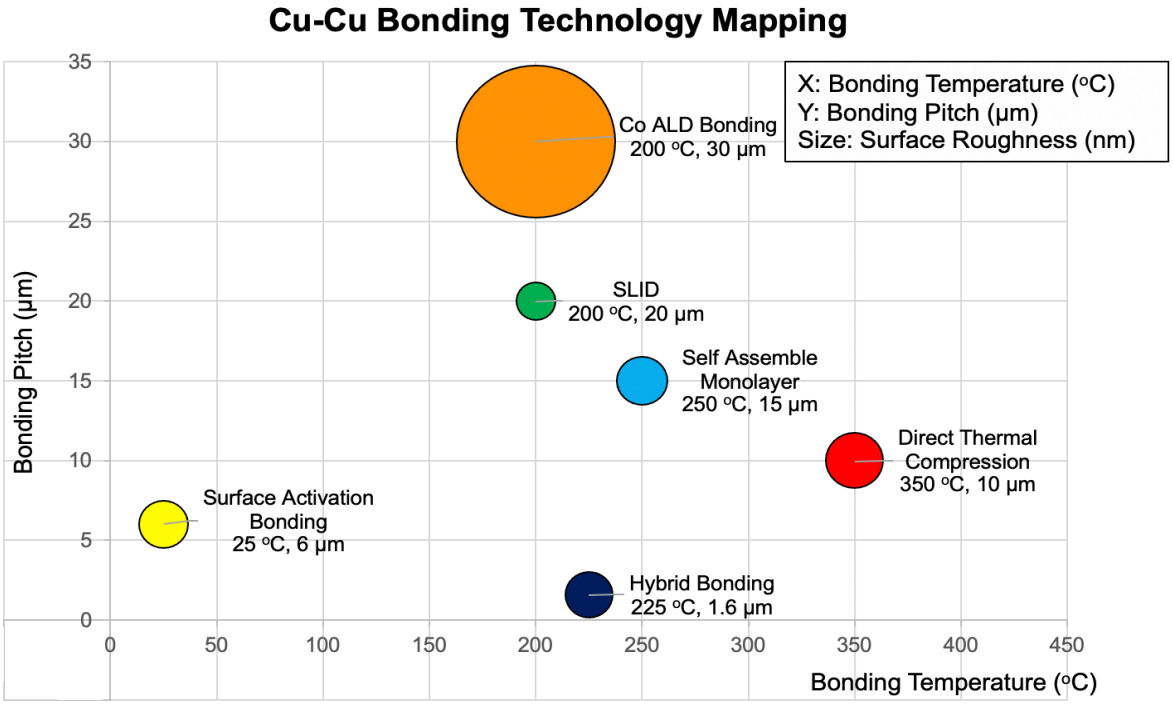


Figure 11 Technology mapping of Cu-Cu bonding [42][82][55][50][59]

2.2.1 Direct Thermal Compression Bonding

The first method is direct thermal compression bonding. Direct thermal compression bonding applies compression force and heat to induce the Cu diffusion between two Cu I/O surfaces [44]. In general, the bonding temperature is above 300 ^{o}C with 300-400 ^{o}C post-bonding anneal to increase the bonding strength. Compression force is mainly related to the surface planarity and cleanliness, which vary from 100-150 MPa for non-planarized surface to 2.5 MPa for chemical-mechanical polished Cu surfaces [45]. However, the main problem is thermal compression bonding requires a bonding/anneal temperature above 350 ^{o}C to achieve enough bonds strength. Various surface cleaning methods (e.g. formic acid, H_2) [46] [47], special microstructures (e.g. nanorod, nanoparticle, porous) [48] [49], and crystal orientations (e.g. 111-oriented nanotwin) [50] have been proposed to lower the bonding temperature.

2.2.2 Self-assembled Monolayer (SAM) Method

The self-assembled monolayer (SAM) method creates a protective chemical layer on top of the Cu I/O pads to prevent any contamination or oxidation. The protective layer can be alkane-thiol group, for example, 1-Hexanethiol [CH3 – (CH2]4 – CH2 – SH] [51] [52]. By immersing the chip in the 1-Hexanethiol right after metallization, the thiol (-SH) group will absorb onto Cu, and the methyl (-CH3) chain on the other side will form a densely packed monolayer of hydrophobic protective film [53] [54]. To desorb the SAM, Cu is annealed under N_2 gas at 250 ^{o}C for 10 min before thermal compression bonding to expose a clean Cu surface [54] [55]. C. Tan demonstrated SAM-protected Cu surface can

induce a much higher shear strength (~60 MPa) than methods without SAM (~10 MPa) [56]. However, the main challenge is that the protective chemical films take hours or days to fully absorb onto the metal surface.

2.2.3 Solid-Liquid Interdiffusion (SLID) Bonding

Solid-Liquid Interdiffusion (SLID) bonding deposits a thin layer of low-melting-point metal or alloy, such as Sn or Ti, on top of the Cu pads to decrease bonding temperature and create a high-melting-temperature intermetallic compound [57]. The benefits are the bonding time can be as fast as few seconds [58], and the bonding temperature can be lower than Cu thermal compression bonding. But as we scale down the size of the Cu pads, the portion of the undesired intermetallic compounds (IMC) will increase and cause yield issues after thermal cycling. Also, the SLID method must accurately control the ratio between the low-melting-temperature metal and Cu. If the amount of low-melting-temperature metal is too low, the Cu surface might not be able to wet fully and thus creating voids. But if the volume of the low-melting-temperature metal is too high, then it might diffuse through the under bump metallization (UBM) layer and cause shorting of the RDLs [59].

2.2.4 Surface Activation Bonding (SAB)

Surface activation bonding uses argon plasma under ultra-high vacuum (UHV) to clean the Cu surface before bonding. Argon plasma can remove the copper oxide or any contamination on the Cu surface so that the two Cu pads can directly bond due to surface cohesive and adhesive energy without applying heat [60]. By this method, T. Suga

demonstrated SAB Cu-Cu bonding under room temperature for 6-μm pitch I/Os with 20 MPa shear strength [53]. However, the challenges for SAB Cu-Cu bonding are the requirements of large contact area, highly planar and smooth Cu and chip surfaces, and ultra-high vacuum [61] [62].

2.2.5 Hybrid Bonding

Hybrid bonding is a method for achieving multiple material bonding at the same interface. While it is not the same as Cu-Cu bonding, there are few fundamental mechanisms that are similar to other Cu-Cu bonding methods. For Cu/dielectric hybrid bonding, a layer of SiO_2 is made mostly co-planer with Cu pillars. After CMP and plasma activation of both the oxide and Cu surfaces, the oxide layers will first bond under room temperature with the help of surface terminating chemistry to prevent the byproducts from forming voids in the pads. One example of the chemistry is hydrogen byproducts replacing water vapor: $Si\text{-}NH_2 + Si\text{-}NH_2 = Si\text{-}N\text{-}N\text{-}Si + 2H_2$ [63]. The plasma activation helps to remove any residual H_2O on the surface by Ar or N_2 plasma [64]. After one hour of 300 ^oC anneal, the Cu pads expand and merge to create Cu-Cu bonds. Although the pitch of hybrid bonding can reach 0.8 μm, it requires a sophisticated CMP process to create a few nanometers uniform dishing on all the Cu pads across the whole wafer [65].

2.3 3D Stacking of Reconstituted-Tier

2.3.1 IMEC 3D Stacking of Thinned Embedded Dice in BCB

IMEC proposed using Benzocyclobutene (BCB) as a dielectric layer to embed pre-thinned dice and perform multi-tier wafer-level-stacking [66] [67] [68]. Figure 12 shows the concept in which multiple layers of BCB-embedded thin chips are stacked and connected with RDL and TSVs. The method they use to thin down and transfer the dice is shown in Figure 12. The prefabricated-silicon-dice are DRIE etched to create shallow trenches and then temporary bonded to a Si carrier substrate. After thinning the device wafer down to 15 μm, the chips are cut and transferred to another wafer which has RDL and high aspect ratio vias on top. The thin chips are bonded to the wafer with BCB followed by the release of carrier substrate. Finally, the BCB is spin-coated to embed the thin chips and RDL is built on top.

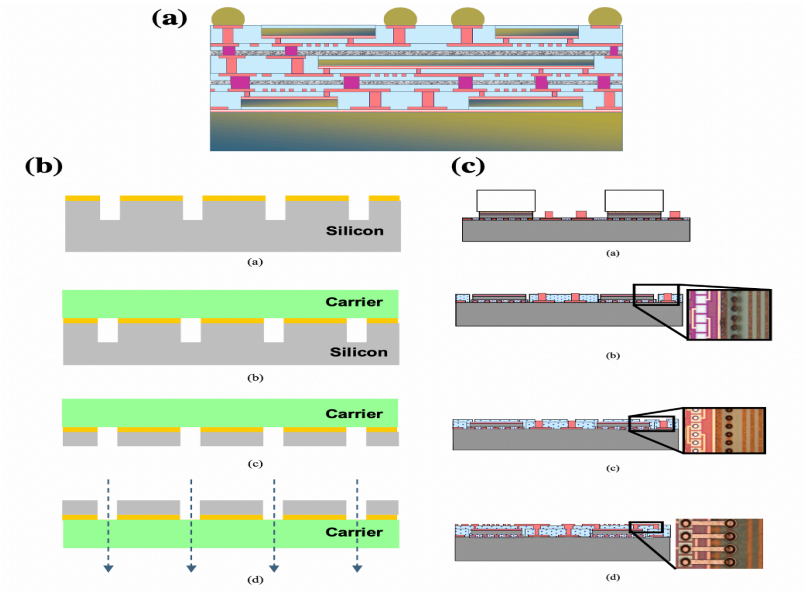


Figure 12 Schematic of IMEC 3D stacking thinned embedded dice:

(a) The concept [41], (b) Process flow of transferring thin chips [42], (c) Process flow of using BCB to embed thin chips [43]

2.3.2 MIT Lincoln Lab 3D Circuit Integration Technology

MIT Lincoln Laboratory developed 3D integration technology based on silicon-on-insulator (SOI) wafers that can be stacked [69]. The process flow is shown in Figure 13 (c); all the transistors are built on the SOI wafer's Si device layer with Cu RDL layers on top. After the devices and RDL are completed, two SOI wafers are bonded by low-temperature oxide-oxide wafer bonding at around 275 ºC for 10 hr anneal. The surface planarity is a critical factor for low-temperature oxide-oxide wafer bonding and the surface roughness has to be within 50 nm. After wafer bonding, the top wafer's silicon handle layer is removed by mechanical grinding and TMAH etch. TMAH has high selectivity between Si and SiO_2 (100:1) such that the BOX layer can protect the device layer and Si layer underneath. The via, which is shown in Figure 13 (b), is made after two SOI wafers are bonded and the via pitch is around 6 µm.

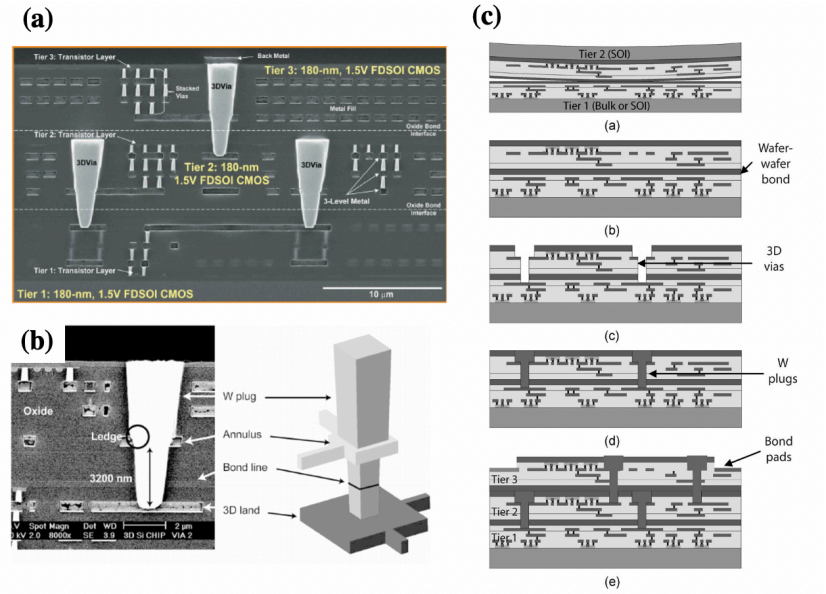


Figure 13 Lincoln Lab 3D Circuit Integration Technology [44] (a) Three tiers of SOI oxide layer, (b) Close-up view of the via, (c) Process schematics

2.3.3 TSMC 3D Stacking of Fan-Out Package

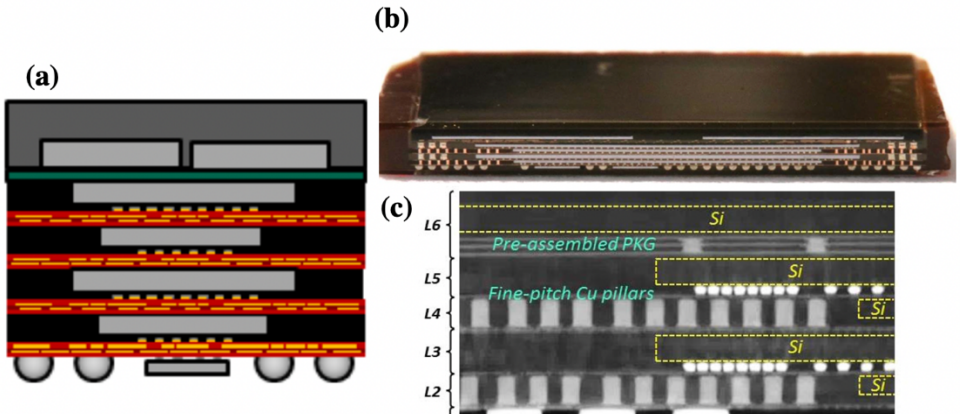


Figure 14 TSMC 3D Fan-Out Wafer Level Package (a) The concept, (b) Optical microscope cross-section image, (c) SEM cross-section image [65]

TSMC proposed a new 3D heterogeneous integration method by stacking multiple layers of fan-out wafer-level reconstituted chips. Figure 14 (a) is the schematic of the concept; multiple layers of epoxy-molding-compound-encapsulated chiplets are stacked with RDL and microbumps inbetween. Each chiplet can have a different size and location. Figure 14 (b)(c) are the cross-section of a six-layer stacked 3D fan-out wafer-level package with a total thickness of 1.15 mm. The minimum RDL is 1.5 μm in width, which can achieve 210 wires/mm and through-mold vias with 150 μm in pitch [70]. The benefits of 3D fan-out stacking compared with TSV-based 3D stacking are lower cost, no TSV keep-out-zone, and potentially better thermal dissipation [71].

2.4 PECVD and ALD Deposition

In this thesis, cobalt thermal selective ALD deposition and PECVD SiO_2 deposition are important enabling materials and processes for the demonstrated experiments. Both ALD and PECVD are a subset of chemical vapor deposition (CVD). Thus, the following paragraphs will discuss the fundamental mechanism of chemical vapor deposition.

2.4.1 Basic Mechanism of CVD Deposition

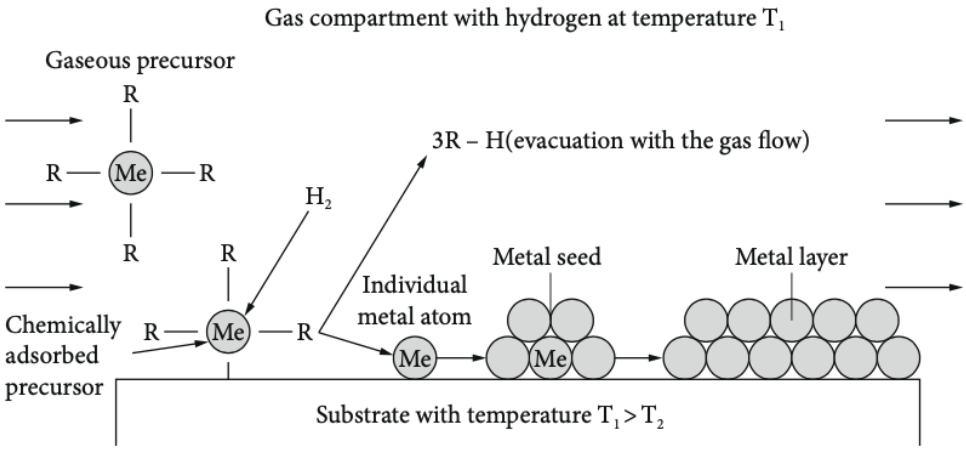


Figure 15 CVD mechanism [68]

CVD uses gas phase precursors to react with the substrate surface leaving behind the byproduct on the surface during film build up. There are generally three main steps for CVD deposition, which include the generation of reaction precursor gas, precursor transportation and film formation [72]. Figure 15 shows the step-by-step CVD mechanism. First, the gaseous precursor is transferred to the surface by laminar convection flow. The laminar flow is preferred rather than turbulent flow as the viscus regime improves the uniformity and the deposition rate. At the surface, the gas velocity is zero and a stagnant boundary layer is created [73]. Next, the precursor has to diffuse through the stagnant layer

to make contact with the substrate in order to be absorbed by the surface for further chemical reaction. After the precursor is absorbed onto the surface, different types of chemical reaction can occur, for example: pyrolysis, reduction, oxidation, nitridation, carbonization [72]. The solid byproduct from the chemical reaction remains on the substrate to start the nucleation process for film growth [72]. Lastly, the byproduct must be desorbed from the surface and transfered to the out-let gas stream by diffusion and to quickly exit the chamber.

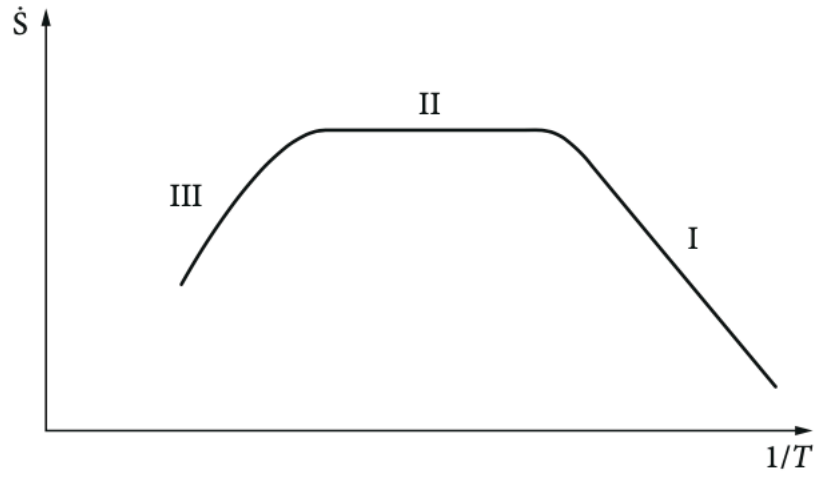


Figure 16 Three different temperature regimes for CVD

CVD deposition can greatly be affected by the temperature and there are three characteristic regimes, which are shown in Figure 16. Regime I occurs at relatively low temperatures in which the deposition rate is limited by the chemical reaction speed on the surface. In Regime I, temperature increase makes the deposition rate to increase [72]. Regime I is generally referred to as “temperature control regime” or “kinetic control regime.” Regime II is where the increase in temperature doesn’t increase the deposition rate significantly anymore. During Regime II, the chemical reaction is fast enough that all the precursors that diffuse onto the surface are reacted. Therefore, the reaction rate and film

quality are controlled by the mass transport of the precursors to supply enough chemical reactants [72]. Regime III is when the temperature is too high and the precursor can decompose during the gas phase, which will form powder or low-quality film [72].

The two main parameters affecting the CVD film structure are substrate temperature and vapor supersaturation. The temperature determines the growth rate, and the supersaturation determines the nucleation rate. These two parameters will create different structures including amorphous, whiskers, platelets, and polycrystals. The high substrate temperature and low supersaturation can induce a better crystalized film [73].

2.4.2 Basic Mechanism of ALD Deposition

Atomic Layer Deposition (ALD) alternates two self-limiting precursors to achieve highly conformal deposition and accurate thickness control [74]. The two precursors alternate sequentially and react with the substrate one at a time. Between the precursor pulses, the chamber is purged by inert gas or evacuation to prevent gas-phase reaction between the two precursors. In each cycle, the precursor can ideally grow one monolayer thick, which gives great deposition thickness control. As an example, HfO ALD growth is showing in Figure 17. The process starts with $HfCl_4$ pulse to react with the OH group on the surface followed by a purge step to remove the byproduct. Next, H_2O removes the -Cl bond and produces a new layer of -OH bonds for the next cycle to continue [74].

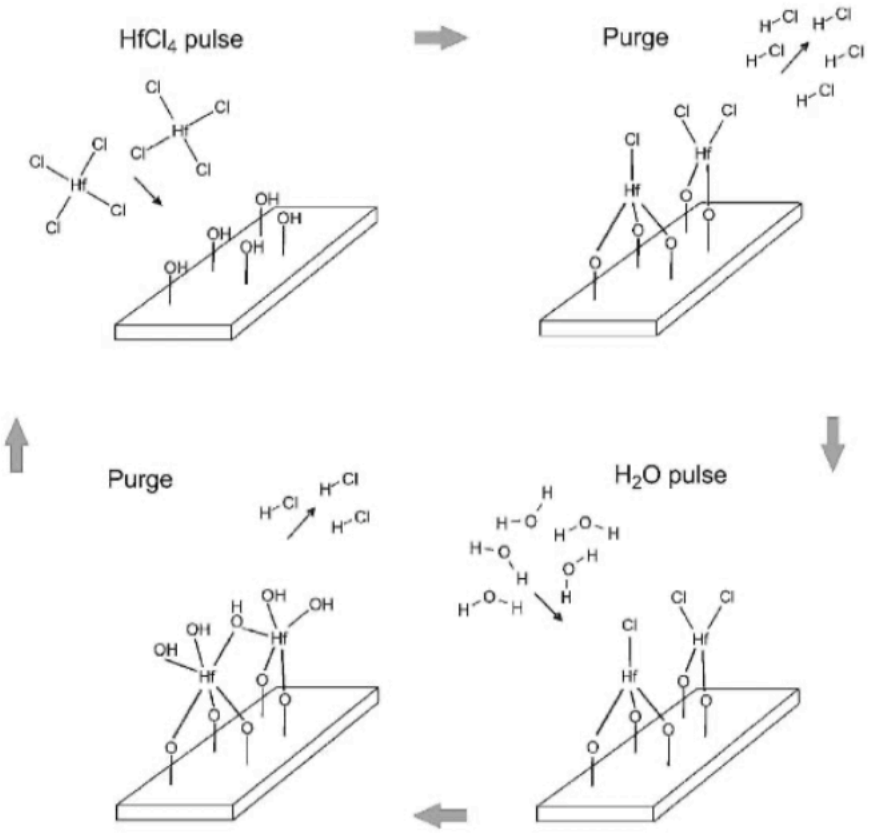


Figure 17 ALD mechanism [70]

Figure 18 (a) is the relationship between ALD growth rate and pulse time or temperature. If it is a self-limiting growth pattern, the growth rate is saturated after passing a certain pulse time. When the temperature increases, there is a higher chance of self-decomposition of the precursor causing the process to become CVD continuous growth. Although the CVD type self-decomposition can increase the ALD growth rate, too much of the CVD type growth can decrease the film quality [74].

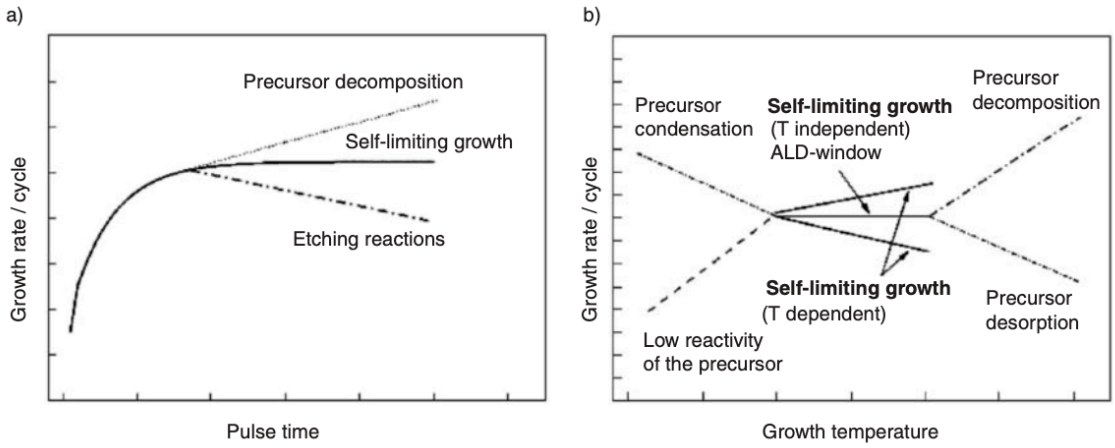


Figure 18(a) ALD growth rate and pulse time relation, (b) ALD growth rate and growth temperature relation [70]

2.4.3 Basic Mechanism of PECVD Deposition

The plasma-enhanced CVD (PECVD) uses plasma to supply more activation energy for chemical reactions so that the substrate temperature can decrease. The plasma contains high energy radicals, ions, and free electrons [72]. To sustain the plasma generation, the chamber pressure needs to be around 50 mtorr - 5 torr in order to have a mean-free path of around 3-300 μm for the electron to be energetic enough to disassociate other atoms or molecules. Also, at 50 mtorr - 5 torr, the ions are less energetic to sputter the substrate, which can decrease the deposition rate. If the chamber pressure decreases to 0.007-0.07 torr, this is the regime for ion-supported etching [75]. Figure 19 shows two

types of PECVDs, which are inductively coupled PECVD and capacitively coupled PECVD.

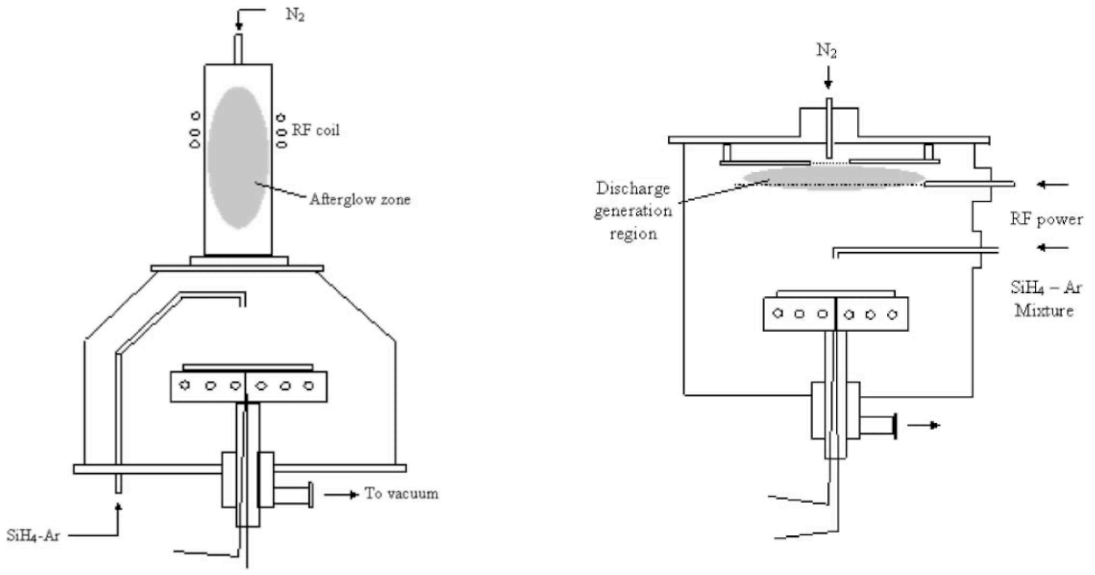


Figure 19 Inductive coupled PECVD and capacitive coupled PECVD [70]

2.5 Conclusion

In conclusion, this literature survey has covered different Cu-Cu bonding methods, 3D stacking of reconstituted-tiers, and fundamental CVD processes. The high-density Cu-Cu bonding methods have been explained and compared in detail using technology mapping to understand the value proposition. Next, three different types of reconstituted-tier stacking methods have been introduced. Lastly, the growth mechanism of ALD/PECVD processes and the effect of different temperature regime have been discussed.

CHAPTER 3: SELECTIVE COBALT ALD BONDING

3.1 ALD Bonding

Atomic layer deposition (ALD) is a process that can grow a film at the atomic layer due to the self-limit nature of the precursors. In 2017, Winter and Kummel developed the $Co(DAD)_2$ precursor, bis(1,4-di-tert-butyl-1,3-diazadienyl)cobalt, that can react with tert-butylamine (TBA) to grow Cobalt (Co) metal selectively only on Cu at around 200 °C [76]. The TBA lowers the thermal decomposition temperature of $Co(DAD)_2$ by coordinating the amine nitrogen atom lone pairs to the Co ions [77]. The full chemical reaction is shown in Figure 20.

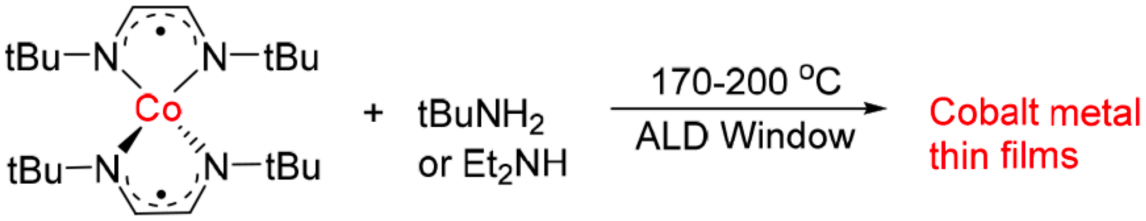


Figure 20 The Co ALD reaction by $Co(DAD)_2$ and TBA [76]

We collaborated with this team to propose a new Cu-Cu bonding technology by using selective ALD Cobalt deposition. As shown in Figure 21, the proposed selective thermal ALD process deposits Co only between the Cu pads to form interconnections when two (or multiple) chips are stacked with small gaps. Once the ALD deposit grows to the thickness of the gap between the two dice, the Cu pads (or copper pillars) become interconnected.

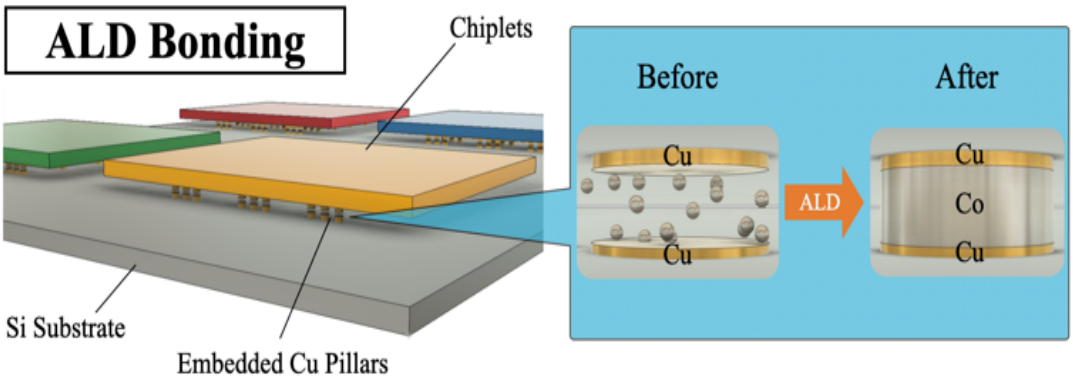


Figure 21. ALD bonding schematic [92]

ALD offers several advantages for ultra-dense bonding. First, ALD can control film thicknesses to the angstrom level, which theoretically can allow the bonding of I/Os at a nanometer scale. Second, ALD bonding does not require extreme Cu surface planarity or cleanliness, whereas most thermal compression related methods and hybrid bonding require. Third, ALD bonding does not involve external mechanical forces, which can prevent die or wafer cracking. Fourth, ALD deposition is not affected by the size of the Cu pads. This means the technology can bond multi-diameter and multi-pitch die pads simultaneously.

3.2 Test-Bed Design and Experiment

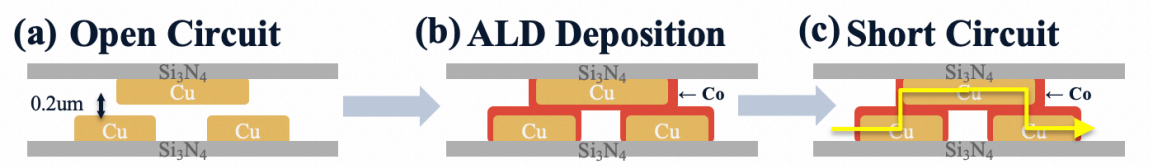


Figure 22: Schematic of the ALD Co test-bed design concept [92]

The concept of ALD bonding testbed is shown in Figure 22. In Figure 22 (a), before deposition, two parallel copper surfaces separated by a small gap form an open circuit

between the Cu pads. In Figure 22 (b), after undergoing a selective thermal ALD process, the ALD deposit, which is Co in this case, grows only onto the Cu pads and gradually builds up from both surfaces until the Co deposits merge to form the interconnections. By measuring the resistance before and after deposition, the result demonstrates the process functionality.

The schematic of the testbed which emulates the design concept of Figure 22 is shown in Figure 23, and the process flow is shown in Figure 24. In Figure 23 (a), the first layer of Cu, M1, with 150 nm thickness, has two square shaped bonding-pads in the middle and four probing-pads at the periphery. The M1 layer is fabricated by a PVD lift-off process with 150 nm thick of Cu and 15 nm thick of Cr adhesion layer, which is shown in Figure 24 (a). At the M1 layer, each bonding-pad is connected with two larger probing-pads. The size of the probing-pads is 200 µm x 200 µm and the bonding-pads are 20 µm x 20 µm. By connecting the voltmeter and ammeter to the probing-pads on each side, as shown in Figure 23 (a), the four probing-pads form a four-point-measurement structure to characterize the resistance of the bonding-pads (and the short traces leading to them).

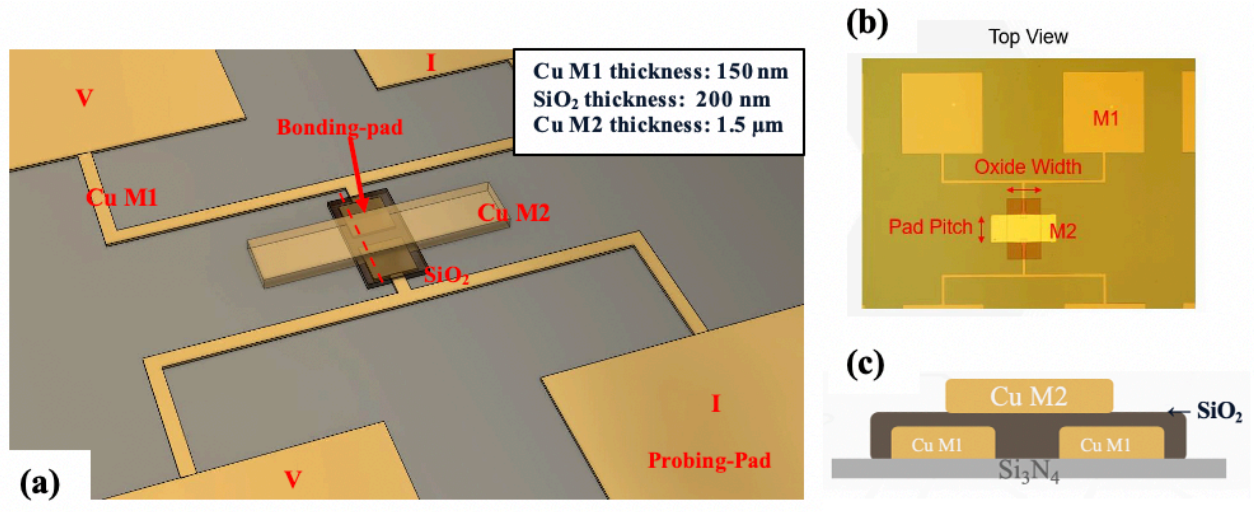


Figure 23 Co ALD Test-Bed Final Design (a) 3D CAD model, (b) Top view, (c) Side view [92]

In Figure 23 (c), the M1 bonding-pads are covered with SiO_2 and the second layer of Cu, M2. The SiO_2 layer is 200 nm thick and is fabricated by PECVD, which is shown in Figure 24 (b). As shown in Figure 24 (c), the M2 layer consists of 1.5 µm thick Cu and 15 nm thick Ti adhesion layer, which are fabricated by a PVD lift-off process. In Figure 24 (d), SiO_2 is a sacrificial layer that will ultimately be etched away by buffered oxide etch (BOE) to create the gap between M1 and M2 layers before ALD deposition. In Figure 25 (b), a uniform 200 nm gap (in red dashed line) is shown after etching the sample in BOE for 10 min. The BOE etch removes the SiO_2 and the copper native oxide. M1 and M2 are characterized to make sure both sides of the copper surfaces are clean before ALD deposition.

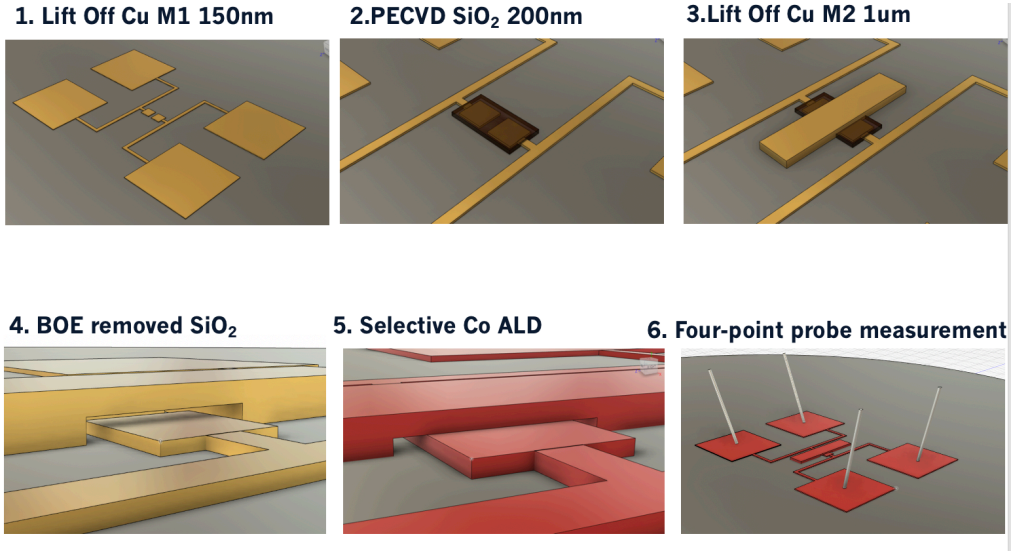


Figure 24 Fabrication and Experiment Steps [92]

Finally, a single chip, with multiple interconnect designs is placed in a thermal ALD system for Co deposition. Before the ALD deposition, samples are annealed at 350 ºC under UHV to remove residue. The subsequent ALD process steps are $Co(DAD)_2$ (5.0 s)/ turbomolecular pump down (10.0 s)/ tert-butylamine (0.2 s)/ turbomolecular pump down (10.0 s) at 200 ◦C; these steps are repeated for 1,000 cycles to fill the 200 nm gap in the

testbed. Each cycle grows approximately 1 Å of Co in a period of approximately 50 s. However, in a commercial ALD tool, the process would be much faster. The detailed mechanism of Co ALD deposition and precursor is well established [77]. And please note that beside pre-cleaning by 350 ºC anneal, various methods of Co ALD deposition (e.g., formic acid, acetone ultrasonication) have been demonstrated at temperatures below 200 ºC with great selectivity in previous studies [77] [78].

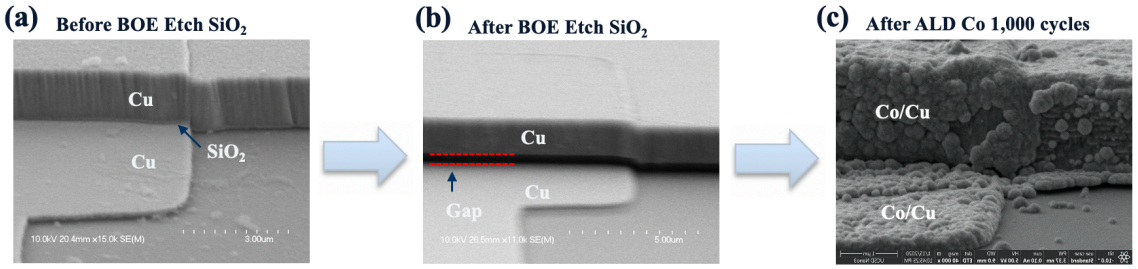


Figure 25 SEM side-view of testbed (a) Before BOE etch SiO_2 sacrificial layer, (b) After BOE etch SiO_2 to create the gap, (c) After 1000 cycles of Co ALD deposition [92]

3.3 Result and Discussion

Table 2 Resistance measurement before and after Co ALD bonding for 1,000 cycles (" - ": the fabricated testbed did not yield) [92]

Oxide Width (μm)	20	20	20	30	30	30	50	50	50	80	80	80	130	130	130	Ave
Pad Pitch (μm)	30	50	100	30	50	100	30	50	100	30	50	100	30	50	100	
Before ALD (Ω)	open	open	open	open	open	open	open	open	open	open	open	open	open	open	open	open
After ALD (Ω)	2.7	2.6	2.9	2.9	3.2	3.3	5.5	4.9	3.8	2.9	3.3	3.5	5.6	-	2.7	3.55

In Table 2, the resistance of each different interconnect design is measured before and after 1,000 cycles of Co ALD deposition. The average resistance after Co ALD deposition is 3.55 ohm with a standard deviation of 1.07 ohm and the calculated ideal resistance is

1.85 ohm. From the resistance measurement, ALD Co bonding creates electrical pathways (i.e., interconnections) between M1 and M2 layers, and thus, eliminating the open circuit.

To gain visual access within the gap, Kapton tape is employed to peel off the Cu M2 layer. Using an optical microscope, Figure 26 (a) shows the top side of Cu M1 layer, and Figure 26 (b) shows the bottom side of the Cu M2 layer. These two sides face each other inside the gap. As shown in Figure 26 (a), the bonding-pads of Cu M1 layer are covered with Co deposit over half of each pad. To confirm, the sample in Figure 26 (a) is characterized by SEM & EDS, as shown in Figure 27.

The geometrical form of the Co deposit is marked with the red dash boundary lines on Figure 26 (a) and Figure 26 (b). The boundary of Co in Figure 26 (a) matches the boundary of Co in Figure 26 (b). Comparison of the shapes of Co between Figure 26 (a) and Figure 26 (b) appears to be consistent with a full layer of Co being filled inside the gap before M2

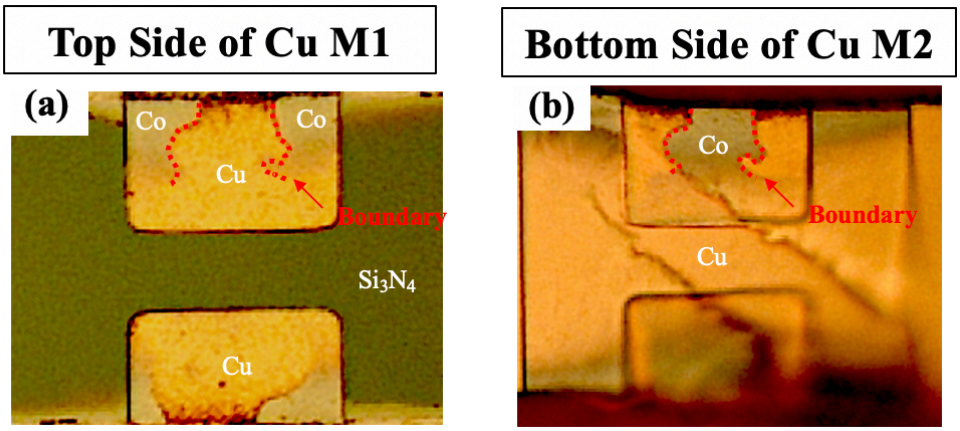


Figure 26 Optical Microscope Image of Bonding-Pads After Peel Off Cu M2 layer (a) Top Side of Cu M1, (b)Bottom Side of Cu M2 [92]

was peeled off. EDS characterization was also used to characterize surface chemistry and confirm the deposition of Co on the peeled pads, as shown in Figure 27 (b).

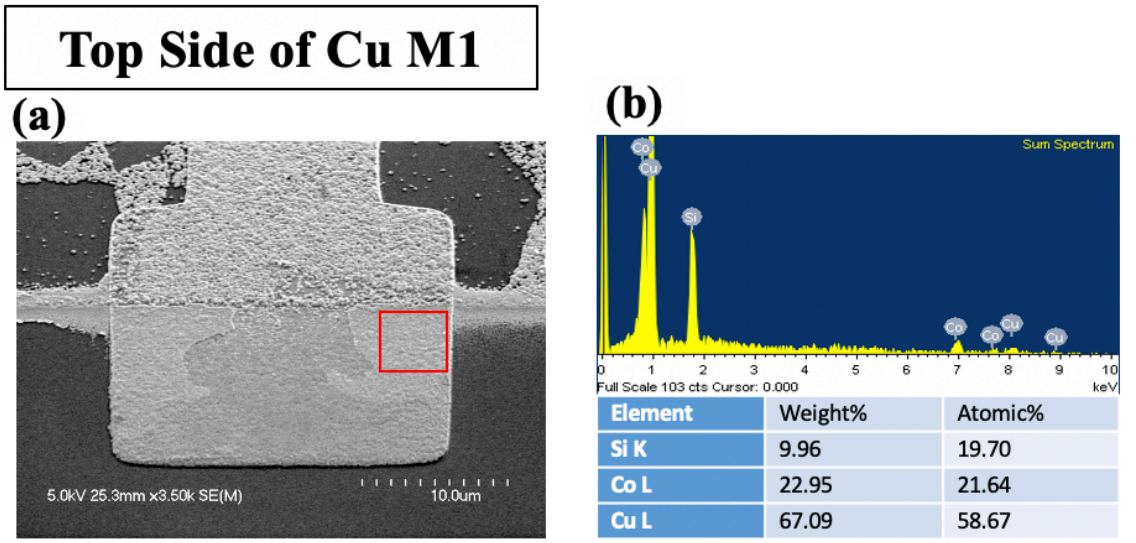


Figure 27 (a) SEM characterize of the silver deposit on the bonding-pad after ALD Co deposition for 1,000 cycles, (b) EDS reading of the red square area [92]

To investigate further, focus ion beam (FIB) sputtering is employed to create a cross-section of the ALD-bonded-pads and is observed under an SEM. Figure 28 (a) shows an approximately 200 nm gap prior to selective Co ALD deposition between the pads. Figure 28 (b) shows the gap between the copper pads filled with Co ALD (after 1,000 cycles) to create a seamless interconnection between Cu M1 and Cu M2.

The above data and measurements provide critical evidence of the feasibility of Co ALD for chip bonding. This new bonding method is not just limited to Co but is potentially compatible with other thermal ALD deposition with high growth selectivity on conductors (for example Mo, Ru, W).

The main difference between the proposed ALD bonding technology and all other thermocompression related Cu-Cu direct bonding or hybrid bonding methods is that ALD bonding does not require metal diffusion to create the bond. ALD bonding deposits an intermediate layer between the Cu pads. In this way, ALD bonding does not need high temperature annealing, large mechanical force, extreme surface planarity or cleanness. Prior efforts in the literature also focused on creating an intermediate layer between copper pads/pillars using electroless plating. For example, Yang et al. demonstrated that electroless Ni plating can bond Cu pillars at low temperature [79]. However, electroless plating is likely unable to support fine pitch bonding due to the possible need for an external pump to circulate the solution into small gaps (i.e., between chips). Using an external pump is difficult to implement in a bonding process, especially in a batch-scale wafer process due to large pumping pressures. Conversely, selective thermal ALD is based on gas diffusion and gas-surface reactions enabling bonding at finer gaps and pitches than liquid phase precursor.

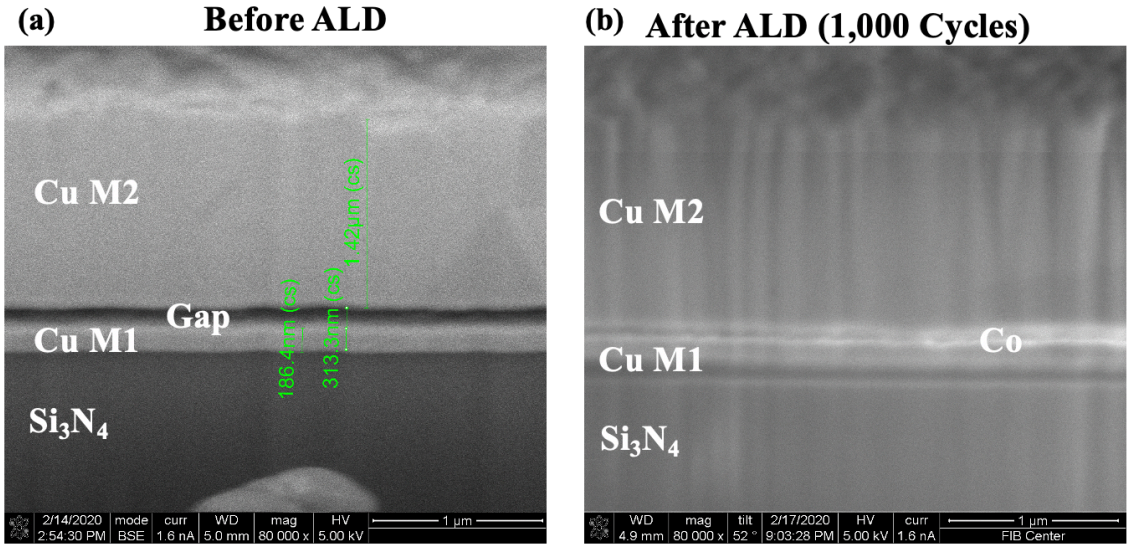


Figure 28 FIB Cross-Section across the bonding-pads (a) Before ALD, (b) After ALD Co Deposition 1,000 cycles [92]

3.4 Co ALD Substrate Selectivity Study

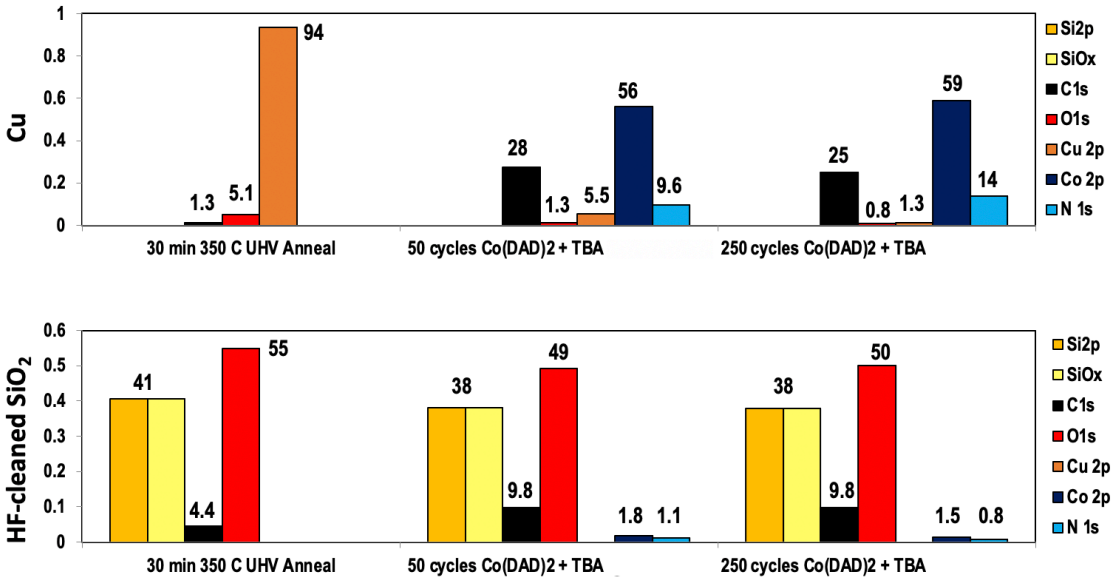


Figure 29 XPS of Cu and SiO2 during different cycles

To understand selectivity for 350 °C pre-cleaning process, Cu and SiO_2 films are measured by XPS and AFM under different cycles of $Co(DaD)_2$ + TBA deposition. The Cu is prepared by PVD and the SiO_2 is fabricated by LPCVD with 0.5% HF-cleaning. The XPS study of Cu and SiO_2 is shown in Figure 29. Before Co ALD deposition, the pristine Cu surface has 94% of Cu signal after the 350 °C anneal for 30 min at UHV pressure. The Cu signal decreases to 5.5% and the Co signal increases to 56% just after 50 cycles, meaning the Cu surface is almost buried by Co deposition. As for 250 cycles of Co deposition, the Cu surface's Cu signal further decreases to 1.3% and the Co signal increases to 59%. The 0.5% HF-cleaned SiO_2, on the other hand, shows almost no Co signal throughout the pre-cleaning up to 250 cycles. The AFM study of Cu and SiO_2 is shown in Figure 30. The surface roughness of Cu and SiO_2 after 250 cycles of Co ALD indicates a large selectivity difference. The Cu, after deposition, has a root-mean-square roughness of 1.4 nm with some 3-4 nm height Co nuclei. As for the SiO_2 surface, the surface root-mean-

square roughness is only 0.32 nm without noticeable Co nuclei in most areas. These results demonstrate selectivity of Co between a metal and a dielectric material, which is consistent with the previous studies.

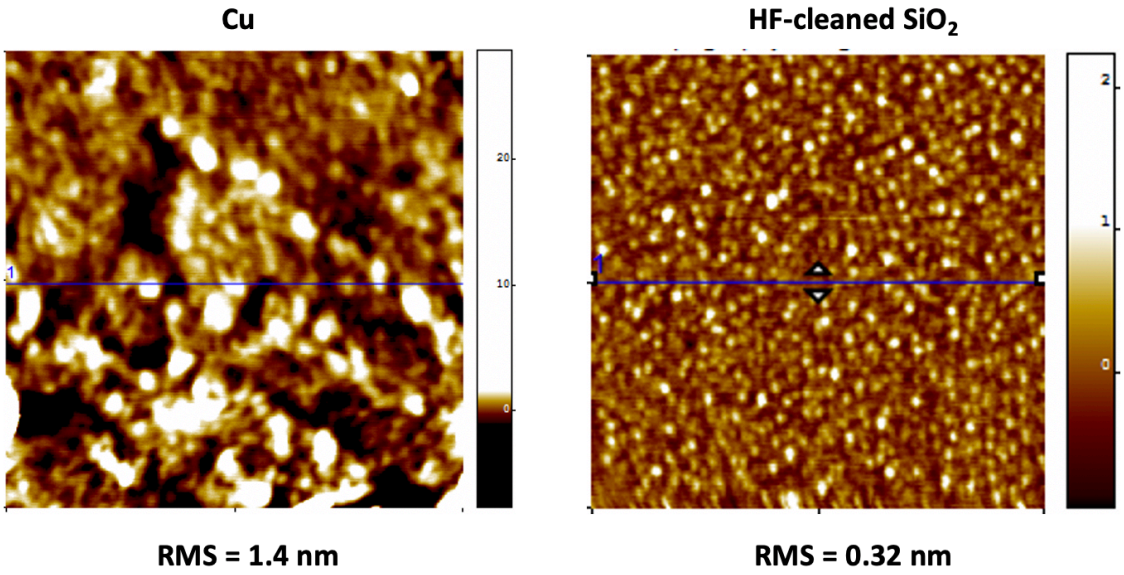


Figure 30 AFM measurement of the Cu and SiO2 surfaces after 250 cycles of Co ALD deposition

3.5 Conclusion

In conclusion, a new type of Cu-Cu bonding is proposed and preliminarily demonstrated. The process is based on selective Co thermal ALD at low temperature (200 ^{o}C), requires low surface cleanliness from native copper-oxide, and requires no mechanical forces. A Cu/200nm gap/Cu testbed is employed to emulate two chips stacked close together during bonding. By comparing the electrical resistance and FIB cross-sections before and after Co ALD deposition, Co ALD demonstrated over 90% yield and created a seamless interconnection within 200 nm gaps Cu gaps at 30 µm pitch. Lastly, the selectivity of Co ALD deposition on different types of substrates is shown by XPS and AFM measurements.

CHAPTER 4: SIO_2-RECONSTITUTED-TIER FOR 3D HETEROGENEOUS INTEGRATION

4.1 SiO_2-Reconstituted-Tier Stacking

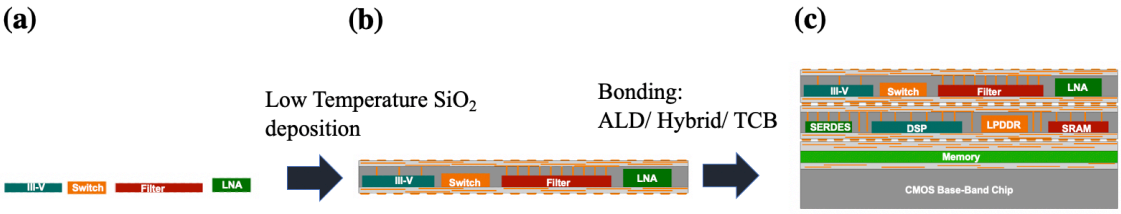


Figure 31 Design Concept of SiO2 Reconstituted Tier

We have discussed various 3D heterogenous integration methods in Chapter 2. In this chapter, we focus on the 3D fan-out wafer-level package (FOWLP) technology space. In particular, the vertical interconnect density in all demonstrated 3D FOWLP technologies is low due to through-mold via fabrication and CTE mismatch of the epoxy molding compounds (EMC) to silicon substrate. Therefore, here we propose an alternate approach for dense 3D heterogeneous integration by SiO_2-reconstituted-tier stacking.

	PECVD SiO_2 Reconstituted Tier Stacking	3D TSVs Stacking	Epoxy Molding Compound Stacking
RDL & Via Density	Higher	High	Medium
Chip Size & Location Flexibility	Flexible	Restrictive With KOZ	Flexible
Layer Thickness	Smaller	Small	High
Trace Length	Shorter	Short	Medium
Mechanical Robustness	Medium	High	Higher
CTE Mismatch	Small	Smaller	Medium
Power Consumption	Small	Smaller	Medium
Signal Latency	Smaller	Small	Medium
Testing	KGD Test	No KGD Test	KGD Test

Figure 32 Comparison between different stacking methods

Figure 31 illustrate the SiO_2-reconstituted-tier stacking. In Figure 31 (a)(b), multiple chiplets (e.g., switch, filter, LNA) can be encapsulated by SiO_2 using low-temperature ICP-PECVD deposition to turn multiple chiplets into a reconstituted tier. The reconstituted tier is then ready for redistribution layer (RDL) or through-oxide-vias (TOVs) fabrication to create lateral and vertical interconnections. Lastly, in Figure 31 (c), multiple layers of reconstituted tiers are stacked and bonded by either thermal compression bonding, hybrid bonding or ALD bonding on top of a monolithic IC. The final result can form a wafer-level, BEOL-integrated, multi-tier stacked 3D heterogeneous integrated chip. Please note that between each layer, a thermal dissipation solution can also be integrated.

Figure 32 shows the comparison between different methods of chiplet stacking; there are multiple benefits to the SiO_2-reconstituted-tier stacking. The first benefit of our method is that the TSV and RDL density can be higher than traditional FOWLP that uses epoxy molding compound to encapsulate chiplets. Second, the chiplets' location, quantity and size can be flexible in each layer without restriction. Third, the electrical latency and power efficiency can improve because of SiO_2's low dielectric constant. Fourth, the coefficient of thermal expansion (CTE) mismatch can be mitigated between chiplets and SiO_2, which increases the thermal mechanical reliability.

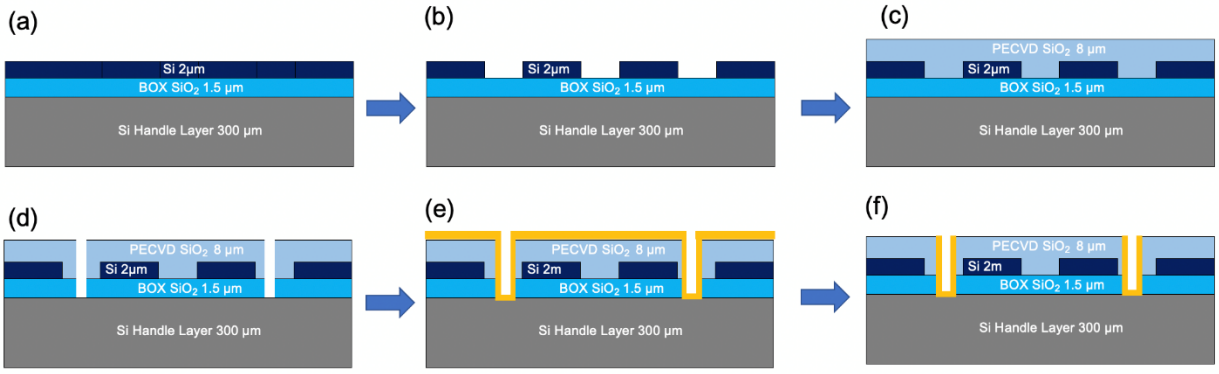


Figure 33 Fabrication steps for SiO_2-reconstituted-tier

4.2 Fabrication Steps

To demonstrate the SiO_2-reconstituted-tier, the fabrication steps are depicted in Figure 33. To emulate the chips, we first begin with a silicon-on-insulator (SOI) wafer with a 2 μm thick silicon device layer, a 1.5 μm thick buried oxide layer (BOX), and a 300 μm thick silicon handle layer. In Figure 33 (b) and Figure 34 (a), the SOI wafer's 2 μm thick silicon device layer is etched by DRIE to emulate diced chiplets on a carrier; Figure 34 (b) shows that the formed chiplets have multiple dimensions ranging from 10 x 10 μm to 1 mm x 1mm area.

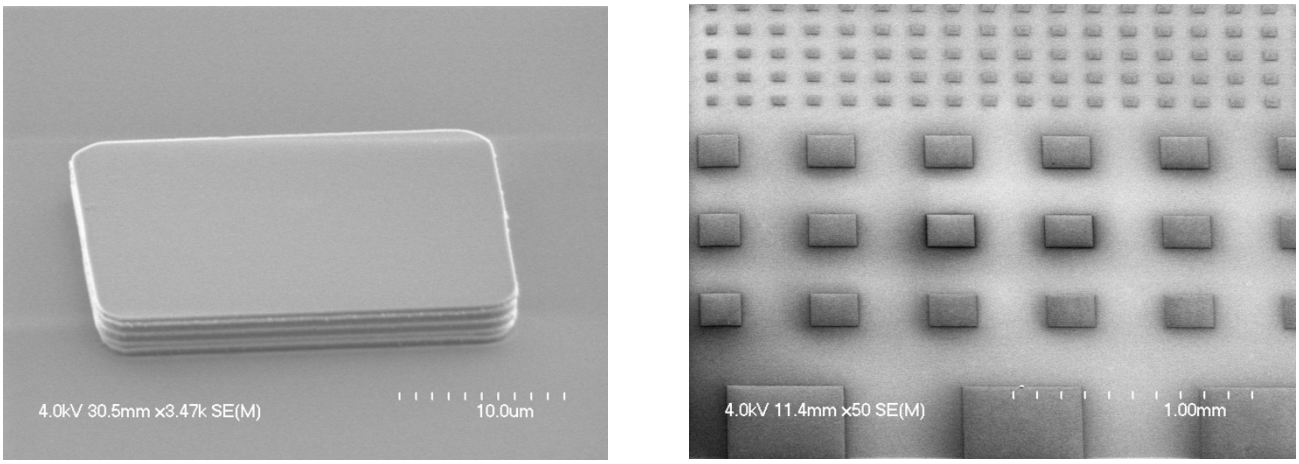


Figure 34 (a) Emulated chiplets from SOI device layer, (b) Multiple sizes of emulated chiplets

Next, the chiplets are encapsulated with a 8 μm thick SiO_2 film at 100 °C. The SiO_2 film is deposited by inductively-coupled plasma-enhanced chemical vapor deposition (ICP-PECVD) at 100 °C for 8 μm thick to encapsulate the chiplets. The deposition rate is 4 μm/hr and the precursors are 15 sccm SiH_4, 40 sccm N_2O, and 80 sccm Ar under 50 mTorr. The ICP power is 750 W and the substrate bias power is 20 W. In Figure 35 (a), a 50 μm x 50 μm silicon chiplet is fully covered by the SiO_2. The boundary lines on the SiO_2

surface reflect the shape of the chiplet's edges. Figure 35 (b) is the cross-sectional SEM image of a 10 µm x 10 µm SiO_2-encapsulated silicon chiplet. The cross-sectional image shows that the SiO_2 can be deposited evenly on the substrate and on top of the chiplet. Interestingly, the SiO_2 on the edges of the chiplets grows in a tilted orientation and eventually merges with the SiO_2 from the substrate to form a tightly sealed boundary line. This mechanism is independent of the lateral size of the chiplet and therefore SiO_2 encapsulation can be used for multiple sizes of chiplets simultaneously. The maximum deposition thickness of SiO_2 is 36 µm for the current recipe before the SiO_2 begins to peel off, thus, the maximum thickness of chiplets that can be encapsulated can be increased from the current demonstration.

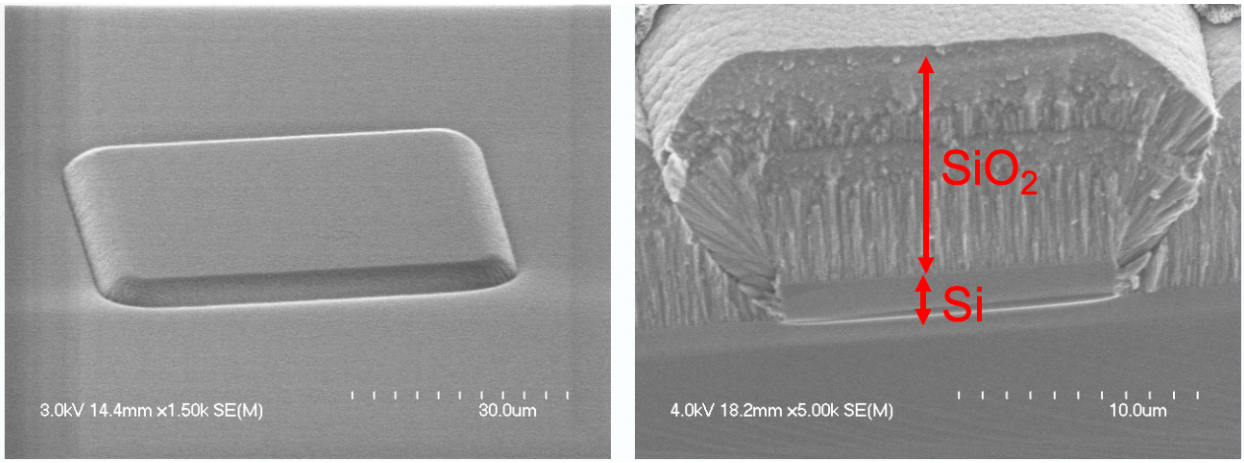


Figure 35 (a) top view of chiplet encapsulate by 8 µm SiO_2, (b) cross-section of chiplet encapsulate by 8 µm SiO_2

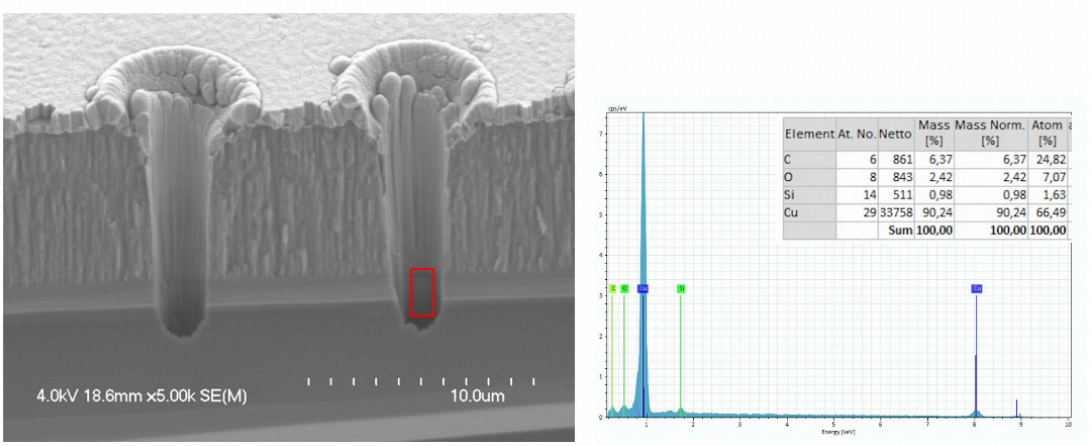


Figure 36 Through-oxide-via with Cu

After the chiplets are encapsulated by SiO_2, the through-oxide-vias (TOVs) are constructed for inter-tier connection. Figure 33 (d) illustrates that the SiO_2 encapsulated layer and the BOX layer are etched through with inductively-coupled plasma reactive-ion etch (ICP-RIE) to create the vias. The via size varies from 2 μm to 20 μm in diameter, and the pitch varies from 10 μm to 30 μm. Figure 33 (e) represents the filling of the via by sputtering copper (Cu) to make an annular-coated via. The reason for using the annular-coated via is to simplify the design flow at the early concept-development stage. The annular-coated vias can be infilled with electroplated Cu as shown previously [80]. Figure 36 is the cross-sectional image of the annular-coated through-oxide-vias (TOVs). The annular-coated TOVs are approximately 2 μm in diameter, 10 μm in pitch and 10 μm in depth. The sputtered-Cu is approximately 1 μm thick with 10 nm of Titanium (Ti) adhesion layer and the Cu on the via wall is around 200 nm. From the EDS material characterization, the bottom of the via is confirmed as Cu. The pitch of the TOV is 10x smaller than the size of conventional through-mold-via in 3D FOWLP, which is generally 100 μm in pitch.

4.3 *SiO_2-reconstituted-tier Transferring*

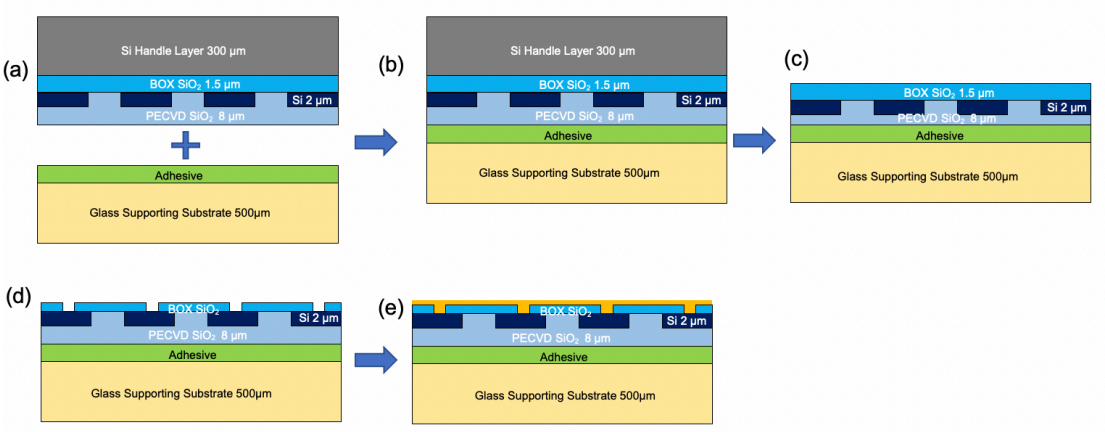


Figure 37 SiO_2-reconstituted-tier transfer by handle layer removal

The SiO_2-reconstituted-tier can be transferred onto another substrate by removing the silicon handle layer. The transfer of a SiO_2-reconstituted-tier is showing in Figure 37. For demonstration purpose, the SiO_2-reconstituted-tier is 2 cm x 2 cm and without TOVs. In Figure 37 (a)(b), the SiO_2-reconstituted-tier is first mounted onto a 500 µm thick glass supporting substrate. The glass supporting substrate has SU8 photoresist as adhesive on top so that the SiO_2-reconstituted-tier can be bonded. The bonding between the two substrates is executed in a vacuum oven at 150 °C for 15 min at <1 Torr. Next, as shown in Figure 37 (c), the silicon handle layer is removed by 30% KOH solution at 80 °C. KOH has much slower etch rate for SiO_2 than the silicon, and thus, the handle layer removal will intrinsically stop at the BOX layer. When the silicon handle layer is removed, the SiO_2-reconstituted-tier is transferred onto the glass supporting substrate with a total thickness of approximately 10 µm. Figure 38 (b) shows the top side of transferred-SiO_2-reconstituted-tier that is only 10 µm thick. Since both the SiO_2 layers and the glass substrate are transparent, the embedded chiplets with multiple sizes can be seen. In Figure 38 (b), 90%

of the SiO_2-reconstituted-tier area is successfully mounted and transferred to the glass substrate with only a small portion residual silicon on the left corner. Also, more than 90% of the chiplets are secured without damage. This suggests a very uniform and smooth KOH wet-etch and that the SiO_2-reconstituted-tier can protect the embedded-chiplets.

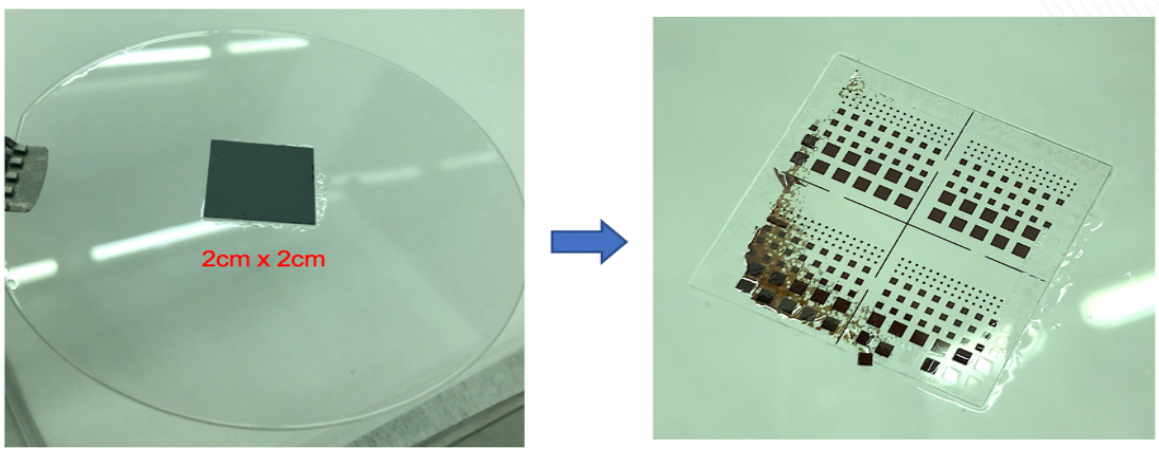


Figure 38 (a) The SiO_2-reconstituted-tier mounted onto the glass supporting substrate, (b) The transferred SiO_2-reconstituted-tier after removing the silicon handle layer

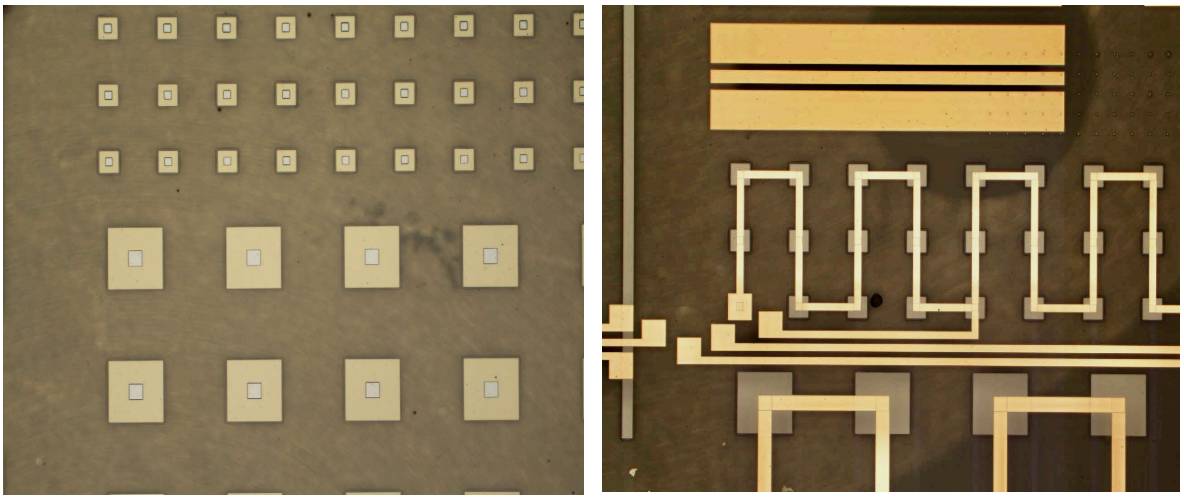


Figure 39 (a) Post-process of SiO_2-reconstituted-tier with via opening on top of chiplets (b) Post-process of SiO_2-reconstituted-tier with Cu redistribution layer to connect the chiplets

The transferred-SiO_2-reconstituted-tier can be post-processed at this point with vias or redistribution layers to increase the connectivity. Figure 37 (d) and Figure 39 (a) demonstrate the vias, which are etched by RIE, to create the openings on top of the chiplets. The etch depth is 1.5 μm to expose the silicon chiplet. To connect the exposed chiplets, an RDL is formed by PVD lift-off of 150 nm thick Cu. As shown in Figure 39 (b), the chiplets are directly connected with the 150 nm of Cu RDL through the vias.

4.4 TOV Resistance Measurement

To characterize the resistance of TOVs, a separate solid-filled TOV testbed was developed, as shown in the Figure 40 (a). Each measurement in the testbed consists of three solid-filled TOVs that are connected at the bottom of the vias through a layer of 500 nm thick Cu. The TOVs are 7.5 μm tall and etched by ICP-RIE to expose the underlaying 500 nm thick Cu. After exposing the underlaying Cu, the vias are filled by bottom-up Cu electroplating. Each via has a probing pad. The probing pads are fabricated by 300 nm Cu lift-off to connect the vias. The via diameters are 50 μm, 20 μm, 10 μm, 5 μm and 2 μm with 60 μm in pitch for every testbed. Figure 40 (b) is the optical microscope top-view image of a pair of 20 μm diameter vias. The *V* and *I* notation on the pads represent the setup of four-point Kelvin resistance measurement for the center via. The resistance measurement results for different diameters of solid-filled TOVs are presented in Figure 41. The average resistance is collected across 10 samples and the standard deviation are listed in Figure 41. From Figure 41, the average resistance increases from 0.036 ohm to 1.144 ohm when the via size shrinks from 50 μm to 2 μm. The trend of a larger via diameter with a smaller resistance corresponds to the larger cross-sectional area of Cu.

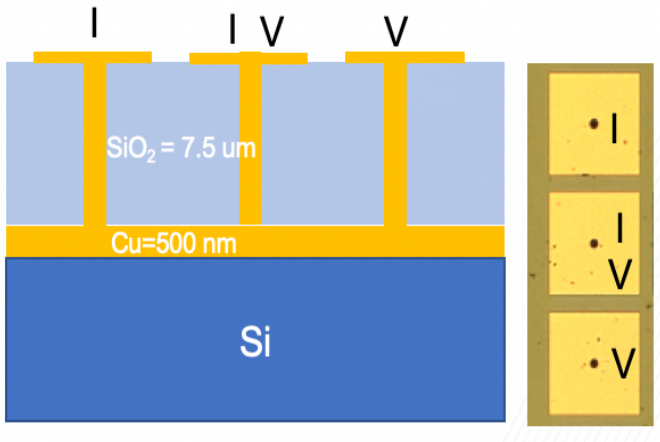
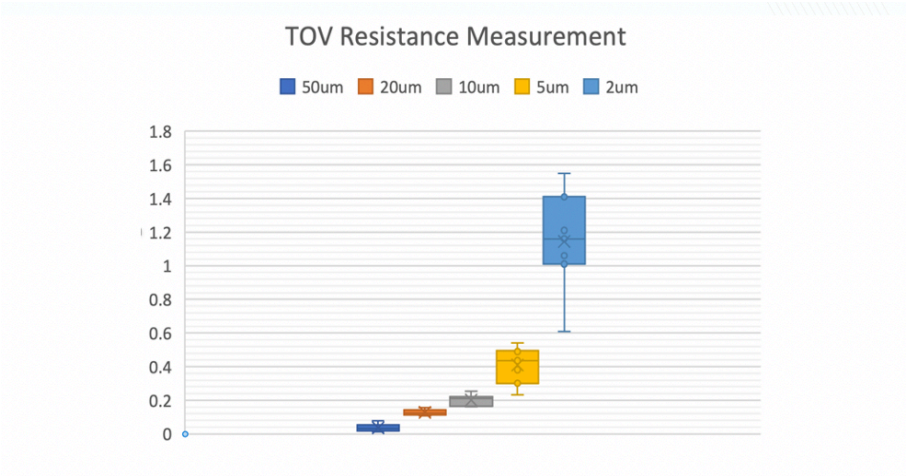


Figure 40 TOV resistance measurement design (a) Schematic side view, (b) Top view



(ohm)	50 um	20 um	10um	5um	2um
AVE	0.036	0.127	0.201	0.410	1.144
STD	0.022	0.016	0.032	0.112	0.302

Figure 41 TOV resistance measurement with different diameters

4.5 Conclusion

In conclusion, a new type of 3D heterogeneous integration by using SiO_2-reconstituted-tier has been proposed and demonstrated. The SiO_2-reconstituted-tier is

demonstrated on an etched SOI wafer to emulate multi-sized chiplets. The chiplets are encapsulated by low-temperature ICP-PECVD SiO_2 deposition, and high-density through-oxide-vias (TOVs) are fabricated around the chiplets. The 10 μm thick SiO_2-reconstituted-tier is transferred by bonding with a glass supporting substrate and the Si handle layer is removed by BOE wet etch to stop at the SiO_2 layer. After tier transfer, the RDL is deposited to connect with multiple embedded chiplets through the opening on the BOX layer. Lastly, the resistance of different diameter solid-filled TOVs are measured.

CHAPTER 5: FUTURE WORK AND CONCLUSION

5.1 Selective Co ALD Bonding

The current results demonstrate the feasibility of Co ALD bonding with 30 μm pitch I/O testbed. Next, the I/O pitch can be decreased from 30 μm, to 5 μm, and then to sub-micron scale. At the same time, the bonding area can be increased from the current small area to chip-scale, and then to wafer-scale. The ultimate objective of the proposed ALD Co bonding is to achieve a wafer-level batch-bonding process that has sub-micron I/O pitch, low bonding temperature, low surface-treatment requirement, and the capability for multi-pitch/multi-diameter bonding. Preliminary testbed with 5 μm pad size is shown in Figure 43 (a).

To achieve a chip-scale or wafer-scale bonding, the filling capability of ALD deposition is very important. Understanding the relations between gap size, chip size, deposition rate, and chamber pressure can determine the achievable maximum sample size. The preliminary testbed for filling capability is shown in Figure 42 (a). By changing the

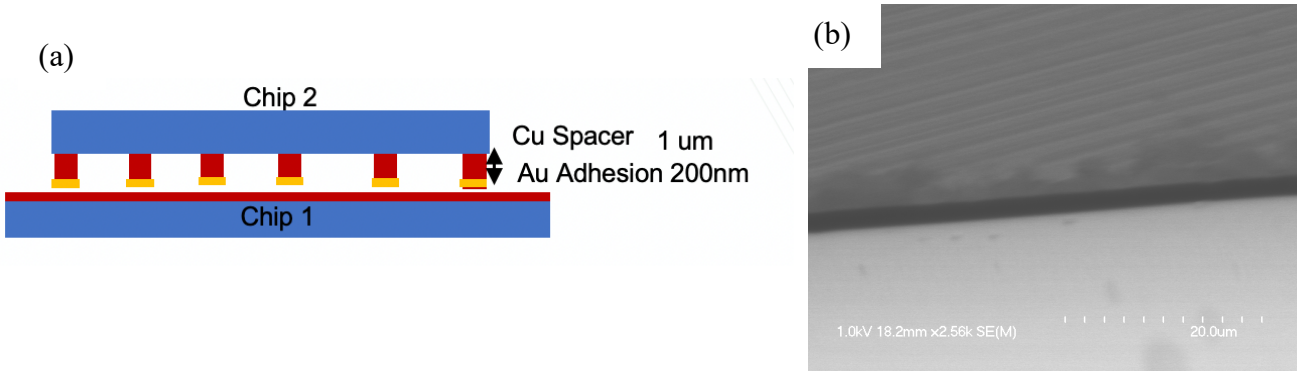


Figure 42 (a) Design schematic for ALD gap-filling testbed, (b) Preliminary fabrication result on the side view

thickness of the Cu spacer, the gap size can be controlled from a few hundred nm to a few microns. The gold adhesion layer is around 200 nm in order to perform thermal compression bonding between the top and bottom dice. After the Co ALD deposition, the chip on top can be removed by a blade and the thickness of Co at different regions inside the gap can be measured.

(a) (b)

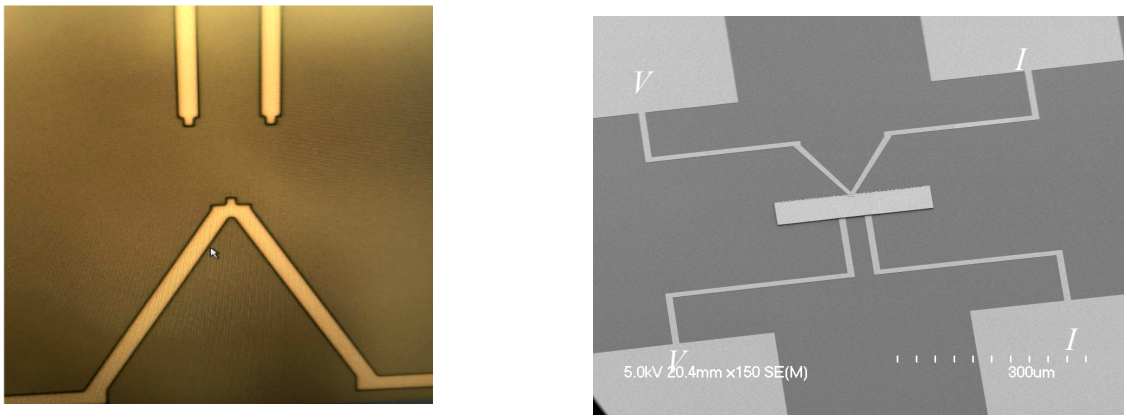


Figure 43(a) Smaller pad size testbed, (b) Contact resistance measurement testbed

If we want to measure only the contact resistance of a single Co bond, the current testbed needs to be redesigned. The testbed in Chapter 3 measures the total resistance of the Co bond, the Cu pads, and the Cu traces. The Cu traces can have much higher resistance than the Co bond. To solve this problem, a new testbed with a modified Kelvin structure that can measure the contact resistance of a single Co bond is needed (Figure 43 (b)).

5.2 SiO_2-Reconstituted-Tier Stacking

The future work for SiO_2-reconstituted-tier project can focus on three aspects. First, decreasing the diameter of through-oxide-vias by e-beam lithography. Second, increasing

the SiO_2 thickness to encapsulate thicker chiplets. Third, measuring the dielectric constant and loss tangent at high frequency for SiO_2.

The SiO_2 deposition thickness can increase to encapsulate thicker chiplets. So far, the SiO_2-reconstituted-tier is only 10 μm thick. The PECVD-deposited SiO_2 may peel off after exceeding a certain thickness. The maximum thickness can be improved by adjusting the adhesion material, increasing the deposition temperature, adjusting the plasma frequency, and changing the ratio between reaction gas to reduce the film stress.

Lastly, measuring the dielectric constant and loss tangent for SiO_2 is important to benchmark with other technologies. Co-planar waveguides can be fabricated to measure the losses and dielectric constant of the SiO_2 at different frequencies. The different thickness of SiO_2 layer and the quality of SiO_2 layer can both significantly affect the loss of high-frequency signal. The deposition condition, for example, the temperature, power, gas ratio may all be important factors to achieving a low loss dielectric film.

5.3 Final Conclusion

To conclude the thesis, a new type of Cu-Cu bonding by selective Cobalt (Co) ALD deposition is proposed and demonstrated. The benefits of Co ALD bonding are nanometer-scale controllability, low planarity requirement, low bonding temperature (200 ^{o}C) and potential for ultra-high-density bonds. A Cu/200nm gap/Cu testbed is employed to emulate two chips stacked close together during bonding. The testbed shows seamless Co interconnection between the Cu pads after Co ALD deposition for 1000 cycles by FIB cross-sections. The electrical measurements demonstrate over 90% yield, which prove the Co connectivity between the Cu pads. Lastly, the selectivity of Co ALD deposition on

different types of substrates is shown by XPS and AFM measurements. Future work includes scaling the I/O pitch to demonstrate sub-micron bonding capability.

Lastly, a new type of 3D heterogeneous integration by SiO_2-reconstituted-tier stacking is proposed and demonstrated. The SiO_2-reconstituted-tier is demonstrated on an etched SOI wafer to emulate multi-sized chiplets. The chiplets are encapsulated by low-temperature ICP-PECVD SiO_2 deposition and high-density through-oxide-vias (TOVs) are fabricated around the chiplets to complete the reconstituted tier. The 10 μm thick SiO_2-reconstituted-tier is later transferred by bonding with a glass supporting substrate and the Si handle layer is removed by BOE wet etch to stop at the SiO_2 layer. After tier transfer, the RDL is deposited to connect with multiple embedded chiplets through the opening on the BOX layer. The resistance of different diameters of solid-filled TOVs are measured. Compared with conventional epoxy-molding-compound-based stacking, the SiO_2 approach can have smaller loss tangent (10x), lower CTE mismatch (3x) and the higher via density (>400x). Future work may include the increase of SiO_2 film thickness to accommodate thicker chiplets, decrease the through-oxide-via size, and study the relation between deposition process and dielectric constant/ loss tangent. We also believe thinner layers of SiO_2 for ultra-thin dice will be key area of study.

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