DESIGN AND RELIABILITY OF MM-WAVE CIRCUITS IN SILICON-GERMANIUM

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DESIGN AND RELIABILITY OF MM-WAVE CIRCUITS IN SILICON-GERMANIUM

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To the current and former students of the Georgia Institute of Technology

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SUMMARY

The first goal of this research is to develop a methodology for the design of RF and mm-Wave circuits in Silicon-Germanium utilizing CMOS, PIN diodes, and passive circuits. Such circuits consist of a 2-20 GHz CMOS-based TR (Transmit/Receive) SPDT switch and an 18-47 GHz Wilkinson Power Divider-Combiner (WPDC). Optimal design techniques are utilized in these circuit designs to overcome the limitations of both Front End of the Line (FEOL: active devices) and Back End of the Line (BEOL: metal stack-up) in a commercial SiGe BiCMOS processes. The resulting performances utilize novel design techniques that allow them to be competitive with existing state-of-the-art designs across multiple IC technologies.

The second goal of this research is to understand the impact of DC reliability mechanisms on AC performance for analog SiGe HBT circuits and to locate an optimal DC biasing regime that balances the tradeoff between circuit reliability and performance. The circuit of interest is a DC-100 GHz wireline driver, which is widely used as a critical block in optical communications. The aim is to extend the concept of Safe Operating Area (SOA), which is the region of the DC I-V plane that does not damage a device over time, to the circuit level. This is done with the introduction of a performance-informed Circuit-Safe Operating Area (C-SOA), which is defined as the region of the DC I-V plane that does not result in a degradation to AC performance over time while maintaining the best possible AC performance. The wireline driver's highlighted AC performance is the OP_{1dB} or output-referred 1-dB compression point.

The work examined in this research is summarized as follows:

1. The design of the 2-20 GHz CMOS TR SPDT switch is presented. The design was not done in an SOI platform, which offers lower parasitic capacitance, so the devices used were triple-well NMOS transistors. The “triple well” NMOS device sits on an ordinary p-type region surrounded by an n-well, which rests on a p-type substrate. When the pn-junction of the NMOS body and the n-well are highly reverse biased, the decreased capacitance of the depletion region in series with the NMOS drain/source-bulk parasitic capacitance results in greater substrate isolation and in turn better insertion loss performance. This technique was used in conjunction with transistor stacking to achieve a high linearity, high isolation, and low insertion-loss TR switch.
2. The design of an 18-47 GHz WPDC is presented. The topology uses lumped elements to conserve chip area and implements each $\lambda/4$ line as 4 $\lambda/16$ π-networks to extend the cutoff frequency of the artificial transmission lines. This technique extends the bandwidth of the circuit. In addition, the 4 π-networks are implemented with only 2 symmetric inductors by utilizing center tap MOM capacitors at each inductor’s electrical center. The MOM capacitors resulted in far better Q-factor and insertion loss compared to standard MIM capacitors and had not yet been used in the literature for WPDC design. The work was submitted to IEEE Transactions on Circuits and Systems II in 2020 for publication and is awaiting approval.
3. The reliability study of the SiGe HBT based wireline driver consisted of performing 10,000 second DC stresses at multiple J_C (collector current density) and V_{CB} (collector-base voltage) for a differential cascode consisting entirely

of 0.1x6 μm^2 devices. The pre- and post- stress OP_{1dB} performance of the wireline driver was measured at 5 GHz. The optimal bias point that saw no performance degradation for enhanced OP_{1dB} performance was determined, and a performance-informed C-SOA was determined using this DC operating point as a reference. The physical mechanism for OP_{1dB} performance degradation beyond the optimal point was also investigated. It was increases in device base and emitter resistance due to high J_C and V_{CB} exciting Auger hot carriers to de-passivate the H-bonds on the STI interface of the polysilicon base and emitter. The de-passivation of H-bonds in the polysilicon base and emitter results in the creation of R&G traps, which drive up the effective base/emitter resistances. The resistance degradation was verified by measuring a single SiGe HBT's base and emitter resistances before and after stressing for 10,000 seconds at high J_C and V_{CB} conditions. The impact on performance degradation was verified by placing additional series resistors that corresponded with the value of measured increase at each of the device terminals in the circuit simulator. The resulting simulated OP_{1dB} degradation matched well with the measured OP_{1dB} performance degradation at high J_C and V_{CB}. The work was accepted and presented to IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium in 2020.

CHAPTER 1. INTRODUCTION

1.1 Background

The explosion in the depth and breadth of the application space of wireless communications in the last few decades has largely been driven by the improvements in semiconductor processes such as Silicon-Germanium (SiGe); the application space of SiGe technology includes but is not limited to radar, remote-sensing, Wi-Fi, cellular networks, wireline communications, space communications, and instrumentation [1]. SiGe maintains itself as a strong contender for the Radio Frequency Integrated Circuit (RFIC) market due to its competitive cost-performance with III-V and the ability to seamlessly integrate with CMOS backend [2]. As a result of 'Front End of the Line' (FEOL) SiGe device f_T improvements up to the 300 GHz range and 'Back End of the Line' (BEOL) SiGe processes offering metal stack-ups with thick, conductive top metal layers favorable to high-frequency operation [3], higher system-level data rates and robust performance can be reliably achieved in novel and integrated wireless communications systems [4].

In the context of SiGe FEOL devices, the question of 'device reliability' or the ability of a device to maintain normal operation under aggressive or normal conditions for extended periods of time, is a key question in setting the limitations of circuit performance [5]. For SiGe Heterojunction Bipolar Transistors (HBTs), the PDK recommended "Safe-Operating Area" (SOA) is defined as a region of bias in the DC I-V plane where the device is not expected to incur a degradation in its characteristics such as forward Gummel, base resistance, emitter resistance, etc. over an extended period. However, for circuit and system level designers, it is not individual device reliability that will determine the

reliability of the functionality of the circuit. For this reason, a Circuit Safe-Operating Area or C-SOA is introduced, where the circuit performance is not degraded over time for a given bias condition.

1.2 SiGe Based Transistor Technology for mm-Wave Design

SiGe HBT technology has evolved very rapidly in recent years pushing parameters like f_T and f_{max} to the 500 GHz range [6]. The importance of f_T and f_{max} lies in the fact that they are the highest frequencies at which the transistor has small signal gain and oscillates, respectively. These parameters are directly tied to the capacitive parasitics of a SiGe HBT, most notably C_{bc} and C_{be}, and as device technologies continue to be scaled down, these parameters continue to shrink resulting in a steady rise in performance [2]. The rapid evolution of this performance can be observed in Figure 1.

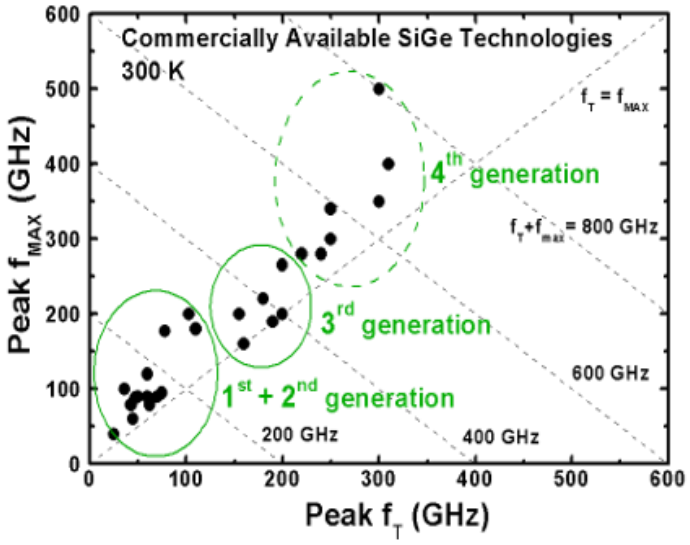

Figure 1. Evolution of SiGe technology peak f_T and f_{max} up to the 4th generation of modern devices.

The down-scaling and improved performance of SiGe technologies has opened the door for the design of high performance circuits in the mm-Wave frequencies of 100 GHz and beyond [6].

1.3 Passive Design at mm-Wave Frequencies

The design of on-chip passive structures at mm-Wave frequencies requires knowledge of microwave theory and design techniques to overcome problems due to lossy materials, limited area, and metal spacing DRC rules.

Lumped elements are typically utilized in on-chip designs under V-Band frequencies (50-75 GHz) in order to conserve area, routing, and minimize loss that a larger distributed element design would field [7]. For example, in the synthesis of lumped element t-networks, it is common practice to use center tapped inductors to conserve die area and minimize losses. This is demonstrated in Figure 2.

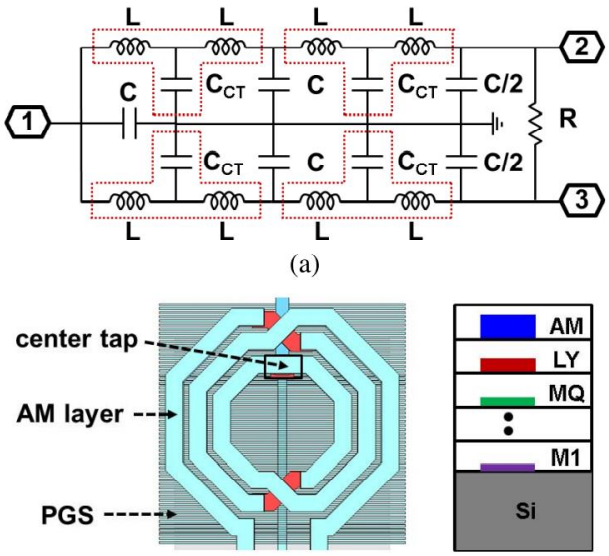

Figure 2. Illustration of center-tapped inductor WPDC topology.

Distributed elements are typically utilized above V-Band due to the more extreme size requirements placed on lumped elements at these frequencies and the self-resonance frequencies of inductors rendering most values above 200 pH impractical. At higher frequencies, electrical lengths become small enough such that conventional transmission line structures can be implemented without taking up too much die area. An example of a classic structure, a Marchand balun, being implemented at 95 GHz can be found in [8]. An illustration of the Marchand balun in [8] is shown in Figure 3.

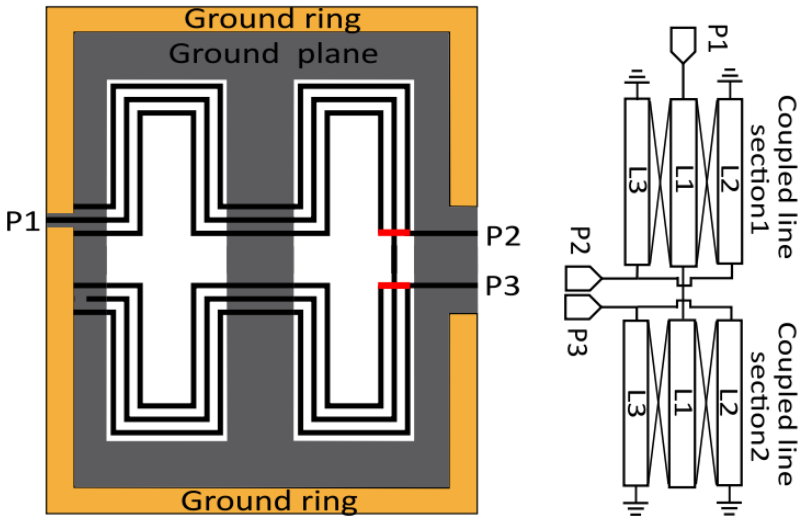

Figure 3. Illustration of a 94 GHz Marchand Balun implemented on chip.

Hybrid passive structures are typically employed most frequently when designs are based around the Ka-Band (26.5 – 40 GHz) or V-Band frequency ranges. This is due to the limitations in die area not allowing for purely distributed design and the relatively low self-resonance frequencies of inductors that can decimate in-band performance. An example of such a structure is a transformer-style, inductive coupling between transmission lines that is utilized to realize a Marchand balun in [9]. The sub-harmonic mixer in [9] operates from

32 to 70 GHz and as such, required a hybrid structure to achieve optimal functionality. An illustration of the hybrid Marchand balun is shown in Figure 4.

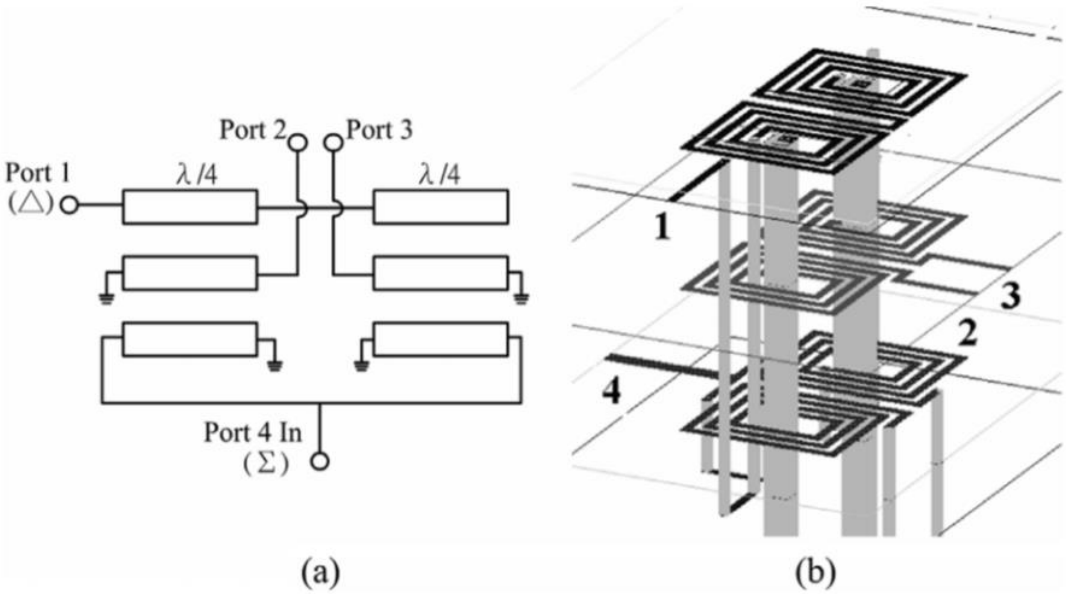

Figure 4. Hybrid Passive implementation of a Marchand Balun using broadside coupling.

1.4 CMOS Switch Design Methodology

In CMOS T/R based switch design, CMOS transistors are used in either series or shunt configurations to achieve switching functionality at mm-Wave frequencies. In the sub 20 GHz range, CMOS provides an advantage compared to SiGe HBTs in that it provides less on resistance and therefore less insertion loss [10]. This is while the increased capacitive parasitics of CMOS play a more minor role at lower frequencies, which makes CMOS a more ideal candidate for switch design in the sub 20 GHz regime compared to SiGe HBTs.

Common techniques for achieving good performance in CMOS T/R switches involve considering three key parameters: linearity, insertion loss, and isolation. For linearity and isolation, the primary problem in T/R switch design is that high voltage swing coming from the Tx can leak across the CMOS transistor's parasitic capacitances and appear at the transistor gate. If the voltage swing is large enough, it can cause for the transistor to being to turn on, which will be detrimental to linearity performance. It is for this reason that stacking the CMOS transistors to share the high voltage swing is a common design technique in switch design [11]. Stacking assists isolation for series switching because it increases the effective Z_{OFF} presented to the Tx, but it will degrade isolation in a shunt implementation because the effective Z_{ON} will be increased, which is unfavorable because when a shunt switch is on it must provide as close to an ideal path to ground. Stacking degrades insertion loss in series switches because it increases the effective Z_{ON}, but it will assist insertion loss in a shunt switch because the Z_{OFF} will be increased. It is for this reason that in CMOS SPDT switch design, careful consideration and optimization of the stacking design must be performed to ensure acceptable performance metrics for isolation, linearity, and insertion loss.

For isolation and insertion loss, strong signals from the Tx can leak across the substrate into the Rx, and the C_{db} and C_{sb} capacitances create a lossy signal path to ground. To solve this problem, a triple n-well technique is used to isolate the transistor body from the substrate and reduce the effective C_{db} and C_{sb} capacitances [12]. An illustration from [12] is shown in Figure 5, which demonstrates the triple-well NMOS structure.

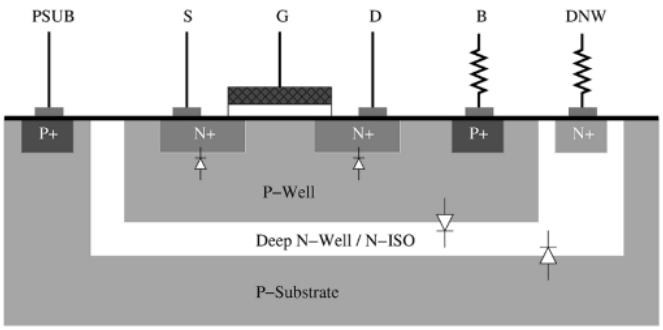

Figure 5. Illustration of Triple well NMOS device for use in CMOS-based T/R switch.

1.5 SiGe HBT Circuit-Level Reliability

Most modern SiGe process PDKs (Process Design Kits) delineate vague and general guidelines for SiGe HBT biasing in terms of a Safe Operating Area (SOA). This SOA is defined as the region in the DC IV plane where the device parameters do not degrade over time. This IV plane is shown in Figure 6. The two axes of this plane are the collector current density (J_C) and the collector emitter voltage (V_{CE}). The lines that encompass the SOA are typically the J_C at peak f_T and open base breakdown voltage (BV_{CEO}).

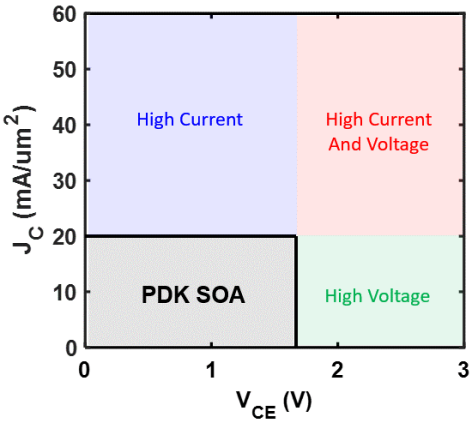

Figure 6. DC IV plane showing the PDK SOA in the bottom left region.

BV_{CEO} or 'open-base breakdown voltage' occurs where carrier avalanching due to high V_{CB} will cause base-current reversal [2]. The upper current boundary for the SOA is typically J_C at peak f_T, where it is demonstrated that current densities greater than this quantity will result in the high injection Kirk effect, which entails a buildup of majority carriers from the base in the collector. This buildup results in pushing the base-collector depletion region into the collector in a phenomenon known as 'base pushout'. This dramatically increases the base-collector transit time and degrades the transistor's most useful RF parameters of f_T and β [2].

When the boundaries of safe biasing are exceeded for prolonged amounts of time, the potential for circuit aging becomes a reality due to hot carriers, which are electrons that have been excited by the high electric fields and current densities in biasing regimes above the SOA. At high current densities, these excited carriers than then collide with the lattice in the extrinsic base and emitter- creating R&G trap centers that will degrade the transistor characteristics. These carriers can also cause damage to the extrinsic base and emitter shallow trench interface (STI) by de-passivating H-Bonds. This also results in the formation of R&G centers that diminish transistor parameters such as base resistance, emitter resistance, β, and I_B [13]. Figure 7 demonstrates this phenomenon in a SiGe HBT by highlighting the regions of interest of the extrinsic bases and emitters and the STI interface boundaries. The movement of the de-passivated H-bonds as can be seen is concentrated towards the extrinsic base and emitter regions of the device. Figure 8 demonstrates degradation in a device Gummel characteristic and DC current gain, β, due to mixed-mode (high voltage and current) stress over time [14].

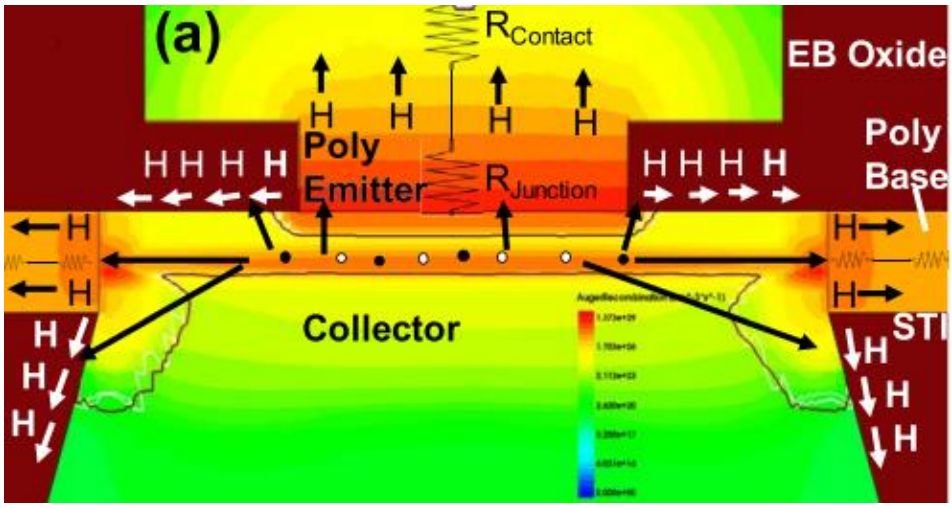

Figure 7. Model of SiGe HBT under stress demonstrating the physical effects of hot carriers under high injection.

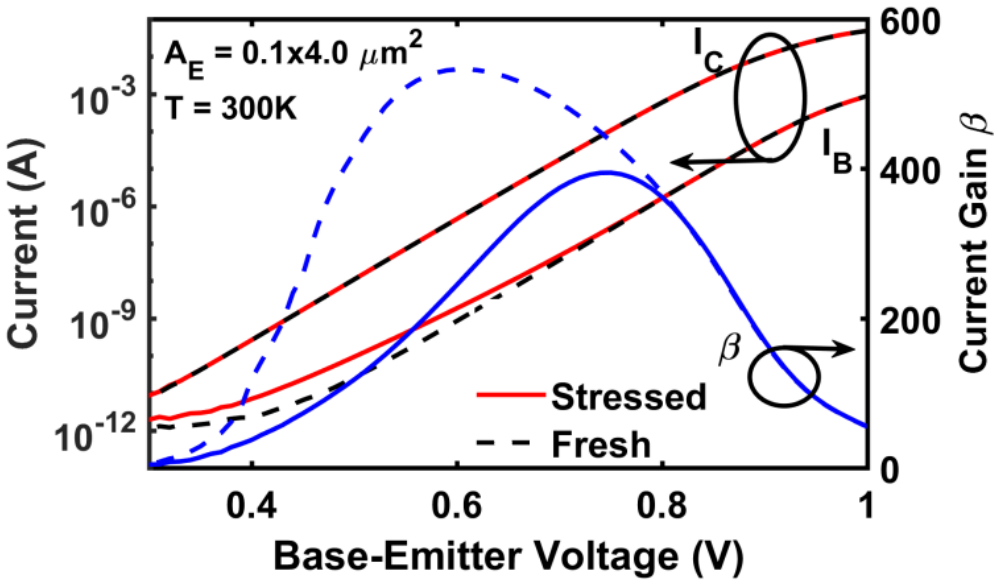

Figure 8. Degradation in Beta and I_B of a SiGe HBT under mixed-mode stress for 10,000 s.

It would also be expected that the reliability of SiGe HBTs directly impacts the performance of mm-Wave circuit blocks such as Power Amplifiers (PA) and Drivers. Works [5], [15], and [16] have explored the circuit-level considerations that are made

when designing reliable circuits in SiGe. [5] discusses the possibility of having AC voltage swings at 10 GHz greater than BV_{CEO} on SiGe HBT driver circuits due to the AC current being capacitive and not contributing to the formation of hot carriers. Figure 9 demonstrates this enhanced range of operation with the dynamic load line of the driver exceeding the DC failure contour of the driver. [15] discusses empirical methods in being able to accurately model and predict the degradation in output power of a Power Amplifier at >28 GHz frequencies at a given DC stress point over time using Cadence Virtuoso and validating such methods with measured results. [16] discusses utilizing the known benefits of current clamping a SiGe HBT in common base biasing scheme to the designer's advantage in an 80 GHz 2-Stage Differential Power-Amplifier. The enhanced linearity provided by the mode of operation results in the designer achieving a P_{SAT} of greater than 16 dBm at the center frequency. Figure 10 demonstrates the extended range of operation in the load line due to a forced emitter current approach to SiGe HBT biasing.

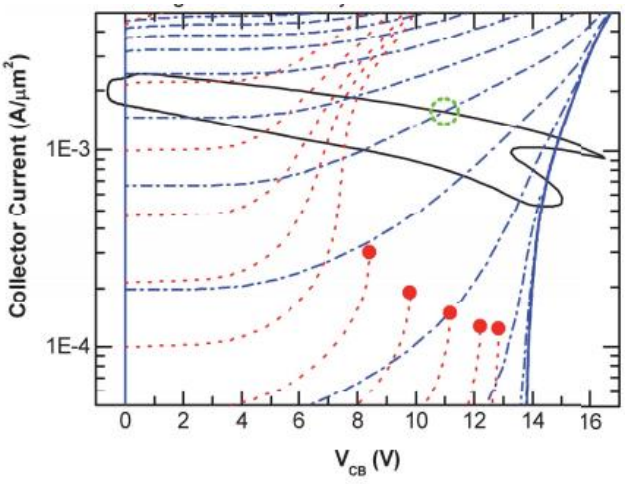

Figure 9. Dynamic load line of SiGe HBT shown in black. Red dots indicate V_{CB} biasing points of failure for a single device. Blue dashed lines indicate cascode points of failure. Note the black dynamic load line exceeds the dashed blue failure contour.

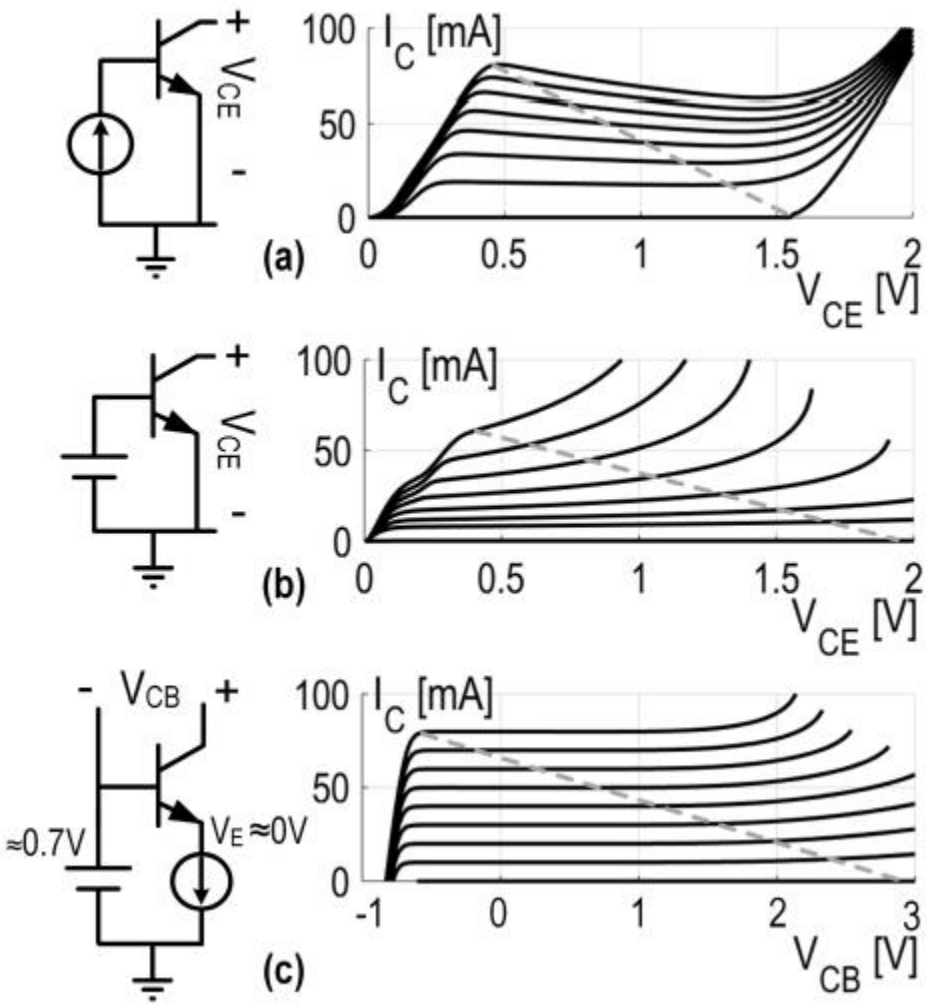

Figure 10. Comparison of Load Lines overlayed with I_C vs V_{CB} plots for a SiGe HBT.

CHAPTER 2. DESIGN OF 2-20 GHZ CMOS SPDT TR SWITCH

In this chapter, the design of a 2-20 GHz CMOS based SPDT switch is examined. The MOSFET triple-well device structure is presented as a viable candidate for TR switch design with parasitic capacitances and resistances of interest highlighted. Stacking and optimization challenges are presented with the final measured and simulated performance.

2.1 Introduction

The emergence of high-performance SiGe platforms that can compete with the performance of III-V technologies has spurred the development of highly integrated, Time Division Duplex (TDD) transceivers in SiGe [17]. These transceivers require a Single Throw Double Pole (SPDT) TR switch to achieve their functionality. The relevant performance metrics that an SPDT TR switch must demonstrate to achieve high system level performance are high isolation from Tx to Rx, low insertion loss for both paths, and good Tx linearity to support the high PA voltage swing at the output.

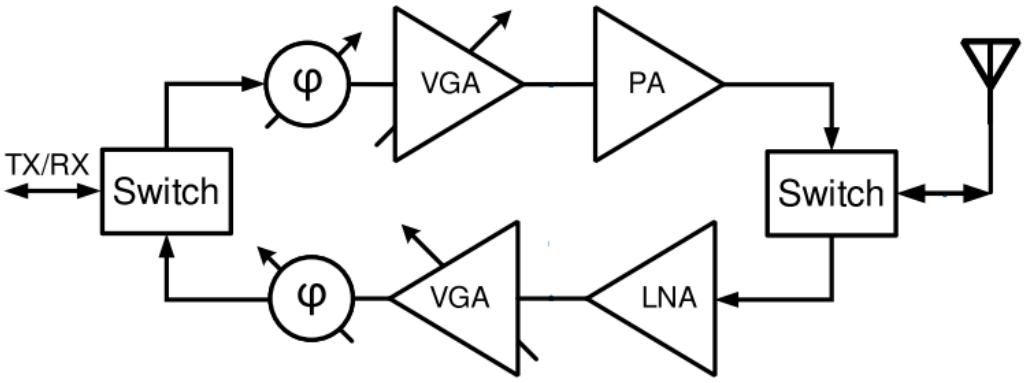

Figure 11. System-Level Schematic of an example TDD Transceiver system implemented in a 45 nm CMOS SOI process

2.2 Design

The design methodology of a CMOS-based SPDT switch from 2-20 GHz involves device-level parasitics to be taken into consideration. In this design, NMOS is selected over SiGe HBTs due to NFET transistors having better R_{on} vs R_{off} characteristics than SiGe HBTs at mm-Wave frequencies [10]. Other important design considerations involve mitigating the increased parasitic capacitance the FETs provide compared to SiGe HBTs.

In [12], it is demonstrated that by utilizing triple well NFETs, the parasitic capacitances of the NFET transistors can be reduced to achieve more robust performance.

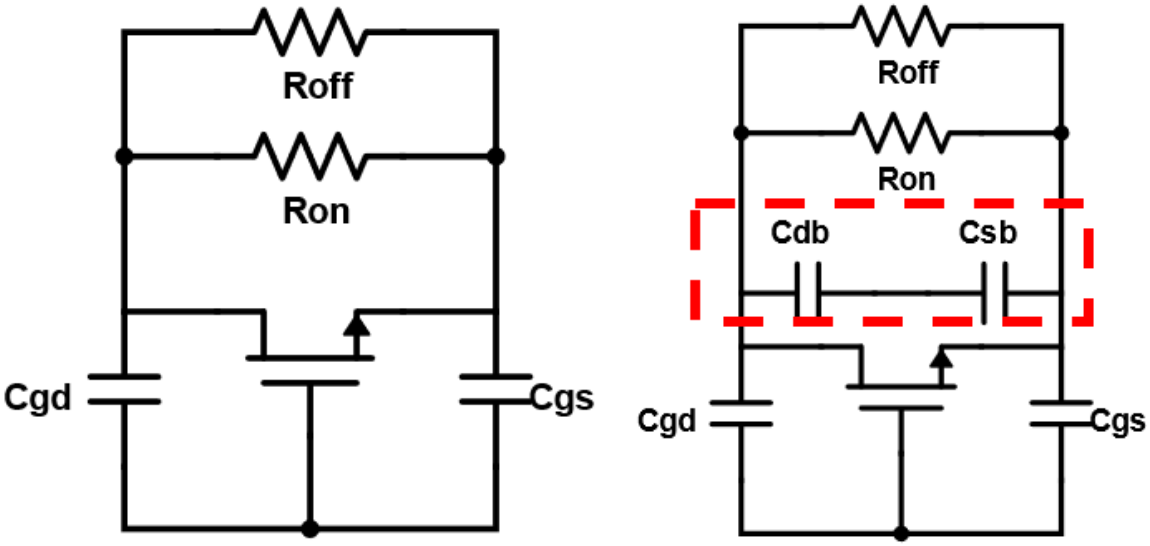

Figure 12. Comparison between simplified model of parasitics in an NFET transistors (left) vs more accurate depiction including source-bulk and drain-bulk capacitances (right)

Figure 5 shows the triple well structure and Figure 12 details the associated capacitive parasitics. The effect of reverse biasing the n-well that surrounds the local NFET p-type body shown in Figure 5 significantly reduces the C_{db} and C_{sb} capacitances respectively due

to the addition of a small series capacitance. As the bias voltage increases, it is expected that the depletion region capacitance would also reduce resulting in further mitigation of the FET parasitic capacitance.

This result is very important because the parasitic capacitance severely limits both achievable bandwidth, linearity, and isolation that the FET can provide across a broad range of frequencies. The device level benefit that using triple-wells provided informed the design decision to use triple-well NFET transistors in the SPDT switch.

Another important design technique in NFET TR switches is the utilization of transistor stacking [11]. Stacking allows the designer to achieve high linearity and isolation by taking advantage of the R_{on}, R_{off}, and parasitic capacitances of the NFET devices shown in Figure 12. Uneven stacking of transistors can be used in TR switch design to achieve optimal performance for Tx to Rx isolation and Rx insertion loss. Stacking on the Tx side is ideal for achieving high linearity because the shunt transistors can share the voltage swing and good isolation because the series transistors combined R_{off} can block the Tx signal from leaking into the Rx- saturating the receiver.

Upon careful optimization and tuning of components, the design of the unbalanced NFET TR switch is shown in Figure 13 with all component values listed. The transistor core was extracted using Assura QRC software, and the inductors were simulated using Sonnet Suites EM software. The circuit was designed in GlobalFoundries 130 nm SiGe BiCMOS 8HP technology platform.

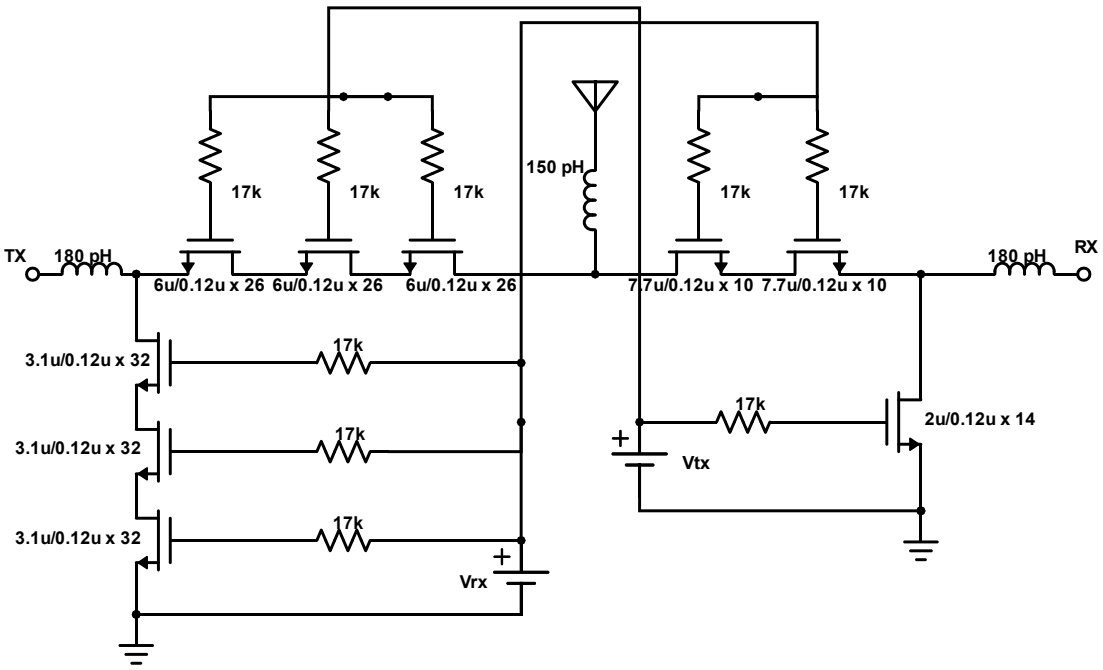

Figure 13. Schematic of NFET TR SPDT switch utilizing triple-well NFET transistors (inverter not shown).

2.3 Results

The resulting unbalanced SPDT was fabricated using multiple breakout structures to characterize Tx and Rx insertion loss and Tx to Rx isolation. 3 breakouts were fabricated in total with a 50 Ω termination placed on either the Tx, Rx, or ANT port of each breakout.

Due to a design flaw in the inverter biasing used to switch between Rx and Tx states, only the Tx performance could be characterized. The resulting measured versus simulated Tx S-parameters of the TR SPDT are shown in Figure 14. The resulting measured versus simulated linearity performance at 11 GHz center frequency is shown in Figure 15. The die photo is shown in Figure 16 with the final layout being 0.45 mm^2. A simulation vs. measurement performance table is detailed in Table 1.

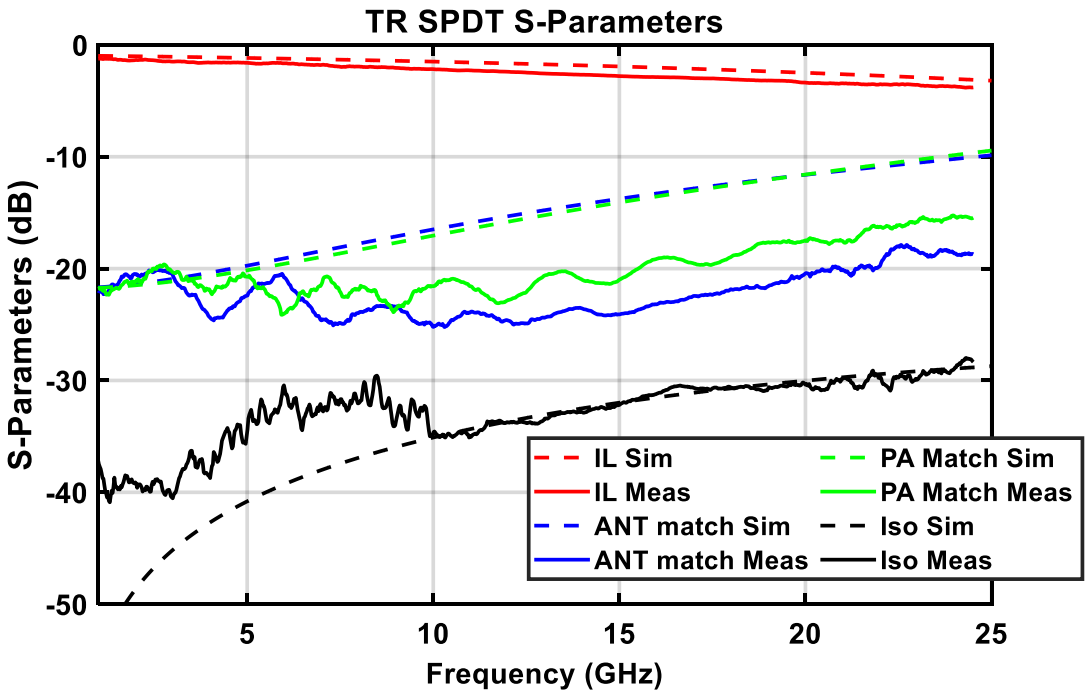

Figure 14. Measured vs Simulated Tx S-Parameters of TR SPDT

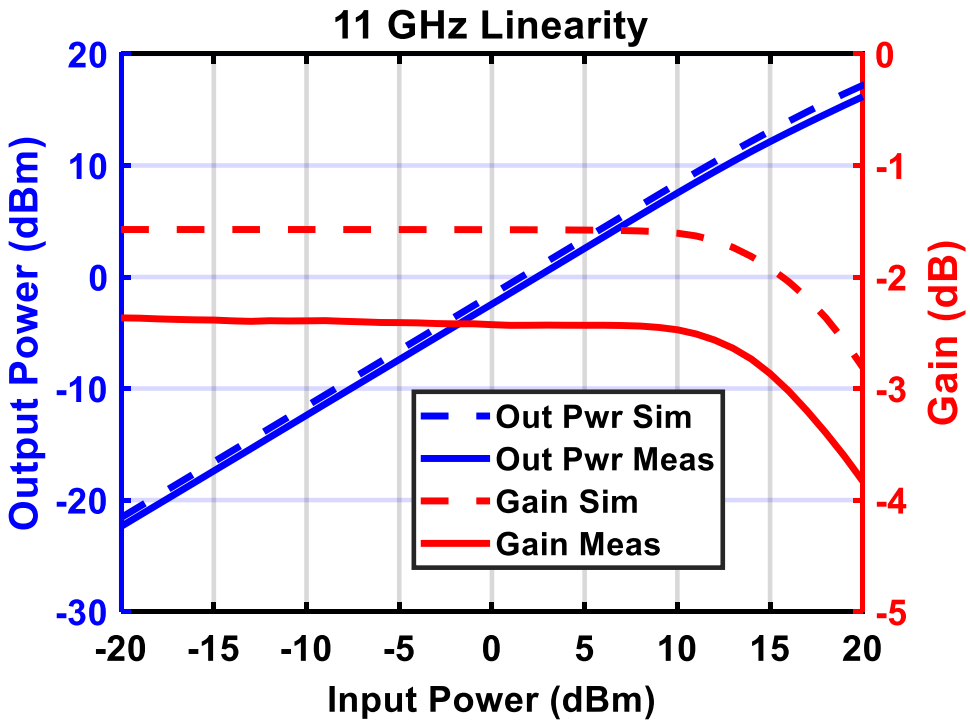

Figure 15. Measured vs Simulated Tx Linearity Performance of TR SPDT

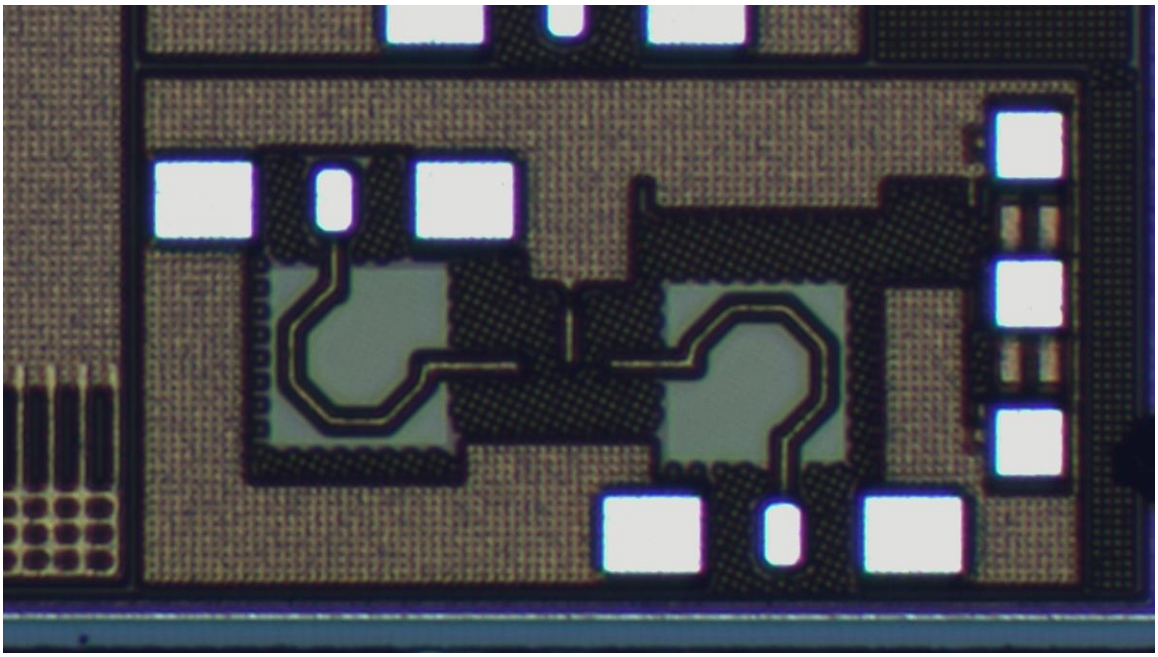

Figure 16. Die Photo of the Tx to Rx isolation breakout measurement structure

Table 1 - Simulation vs Measurement Performance of TR SPDT Switch

Performance Specification	Simulation	Measurement
Insertion Loss	<2.5 dB	<3 dB
Tx IP1dB @ 2 GHz	>19.8 dBm	>17.5 dBm
Tx IP1dB @ 11 GHz	>19 dBm	>17.9 dBm
Tx IP1dB @ 20 GHz	>19.4 dBm	>18.6 dBm
RL	>12 dB	>17 dB
Tx to Rx isolation	>30 dB	>30 dB

CHAPTER 3. DESIGN OF 18-47 GHZ WILKINSON POWER DIVIDER

In this chapter, the design of an 18-47 GHz Wilkinson Power Divider-Combiner is presented. First, the circuit theory behind artificial transmission lines is covered. Next, the advantage of using multi-section networks and compact layout techniques are discussed. Finally, a comparison between MOM and MIM capacitors is carried out, and it is established that using higher Q MOM capacitors is better for insertion loss performance across a broad range of frequencies. The simulated vs measured performance and a performance table are shown in conclusion.

3.1 Introduction

Wideband systems at mm-Wave frequencies have become increasingly relevant to achieve the high data rates and spectral efficiency that are desired for applications like 5G, 6G (emerging), and remote sensing [18]-[19]. However, although mm-Wave frequencies offer huge benefits in terms of data rates, the primary disadvantage of these broadband mm-Wave systems is the increased path loss due to antenna down scaling and increased atmospheric attenuation. To overcome this challenge, wideband, phased array antennas have been used in conjunction with wideband power distribution networks to feed these phased arrays. To achieve good performance for such systems, power divider/combiner circuit blocks with high isolation and return loss, low insertion loss, and wide bandwidth are required.

3.2 Design

Traditionally, power dividers are realized with two $\sqrt{2}Z_0$ Ω, λ/4 lines and a $2Z_0$ Ω resistor, but physical transmission lines take up too much space at <100 GHz mm-Wave frequencies making them poor candidates for design due to their large area [7]. As a result, artificial transmission lines implemented with lumped elements are considered instead.

Artificial transmission lines are limited by their cutoff frequency which is defined in Equation 1.

$$f_c = \frac{1}{\pi\sqrt{LC}} \tag{1}$$

L and C are the inductor and capacitor values utilized in the λ/4 equivalent π-network [20]. However, as shown in [20], this problem can be approached by dividing an artificial transmission line into "n" sections each with electrical lengths of λ/4n. To optimize between operating bandwidth and area, four λ/16 sections are selected,

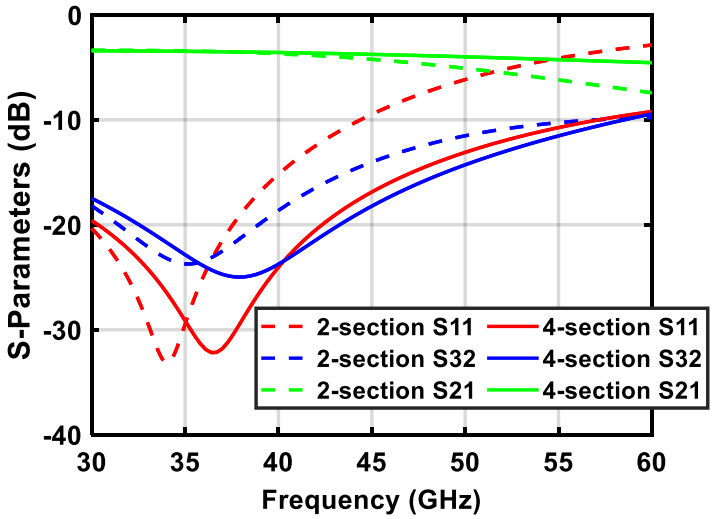

Figure 17. Simulation results showing the extended operating bandwidth achieved by using 4 λ/16 sections vs. 2 λ/8 sections for a WPDC

Figure 17 clearly shows the simulated benefit of both insertion loss and operating bandwidth achieved with 4 sections as opposed to a 2 section WPDC.

To further save area and enhance insertion loss performance, center tapped inductors with MOM capacitors are utilized over MiM capacitors. This layout technique is shown in Figure 18. This is because center-tapped inductors save area and reduce the number of inductors needed to realize 4 sections, which saves insertion loss in practicality. MOM capacitors demonstrate higher Q-factor than MiM capacitors as shown in Figure 19, and as a result they are used at the inductor center-taps to preserve insertion loss performance.

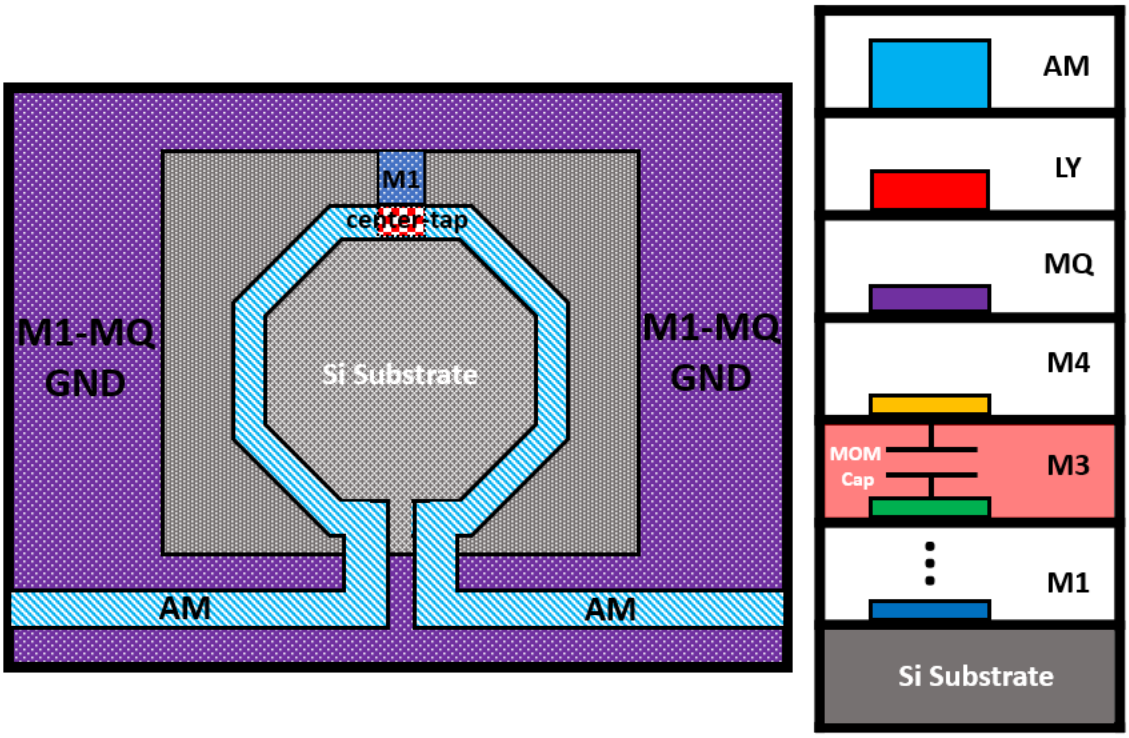

Figure 18. Layout Illustration of center-tapped inductor with MOM capacitors used at the center-taps

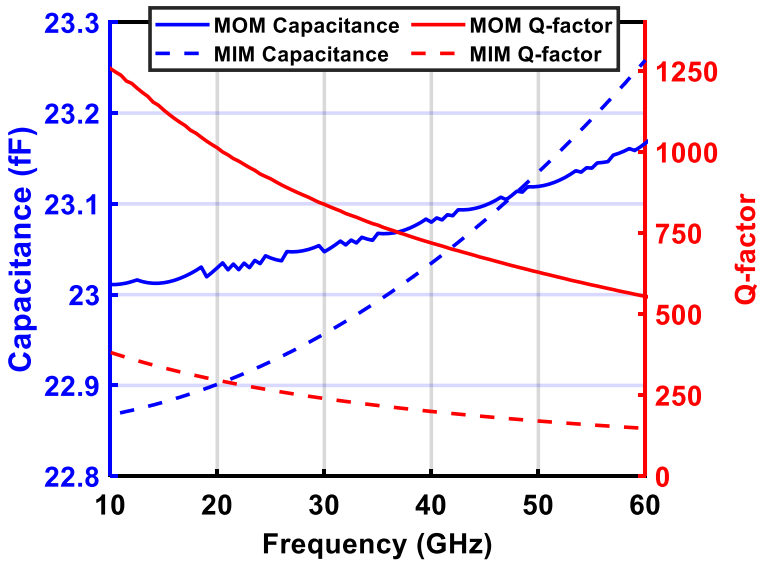

Figure 19. EM-simulated Q-factor and capacitance of 23 fF MOM and MiM capacitors. Note the significantly higher Q-factor achieved by the MOM capacitor at mm-Wave frequencies.

The higher Q-factor that MoM capacitors possess arises from their layout structure pictured in Figure 20 as being a more literal realization of a capacitor without the close dielectric spacing utilized in MiM capacitors, and as a result, they are ideal for achieving small capacitances with high Q.

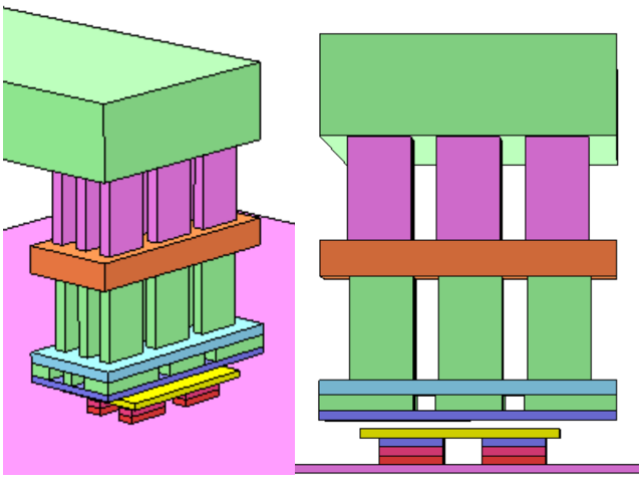

Figure 20. 3-D layout of the 23 fF capacitor rendered in Sonnet Suites 3-D visualizer

The enhanced insertion loss performance achieved in a WPDC utilizing an MOM capacitor over a MiM capacitor is shown in Figure 21.

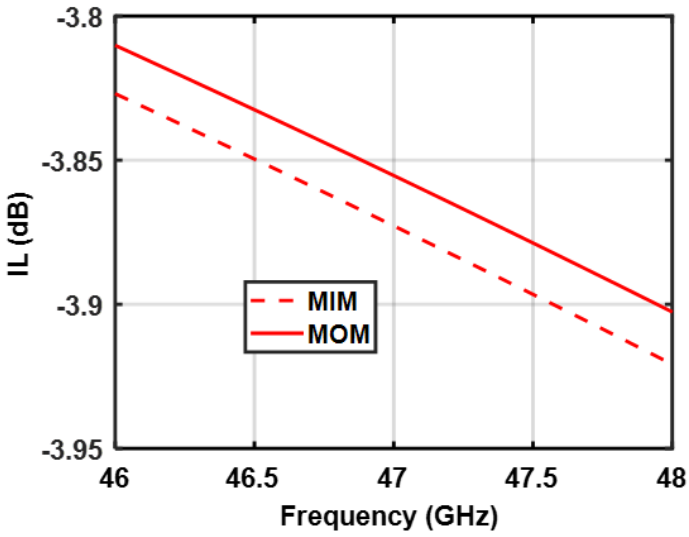

Figure 21. Enhanced insertion loss performance obtained by using an MOM capacitor vs MiM capacitor

The final EM-simulated design obtained with Sonnet Suites EM software is shown in Figure 22 with center-tap capacitors highlighted in red. The circuit was designed in GlobalFoundries 130 nm SiGe BiCMOS 8XP process.

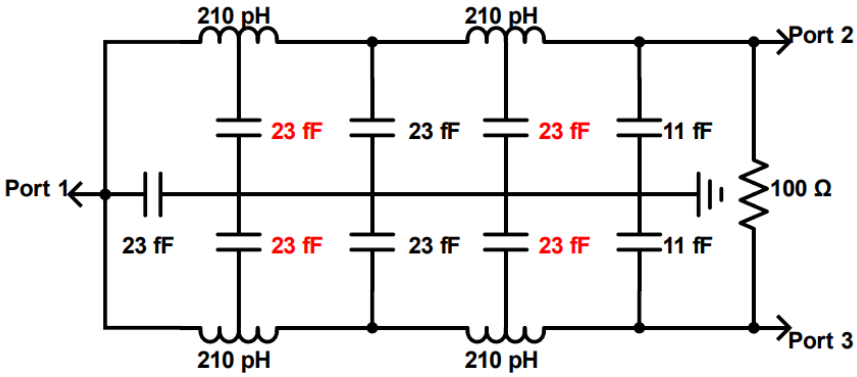

Figure 22. Final schematic of the WPDC with EM-simulated design values for inductors and capacitors. Center-tap capacitors are shown in red.

3.3 Results

The measured S-Parameter performance of the WPDC is shown in Figure 23-Figure 25. The die photo is shown in Figure 26; the resulting layout took up 0.21 mm^2 of die area. The performance comparison table is shown in Table 2.

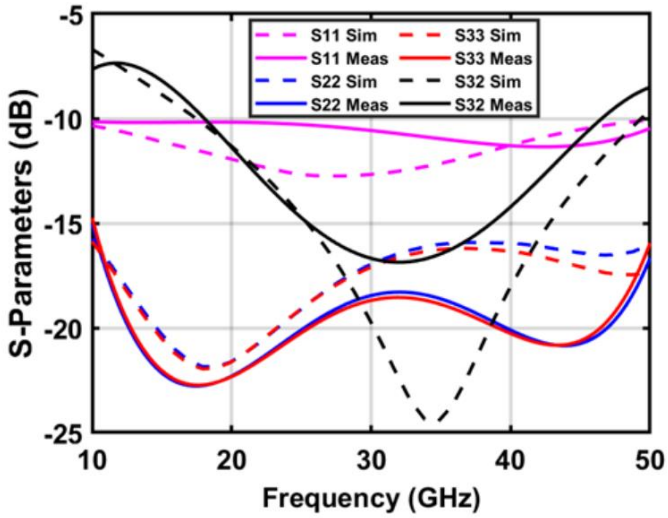

Figure 23. Measured vs. Simulated S-Parameter Isolation and RL Performance of the WPDC

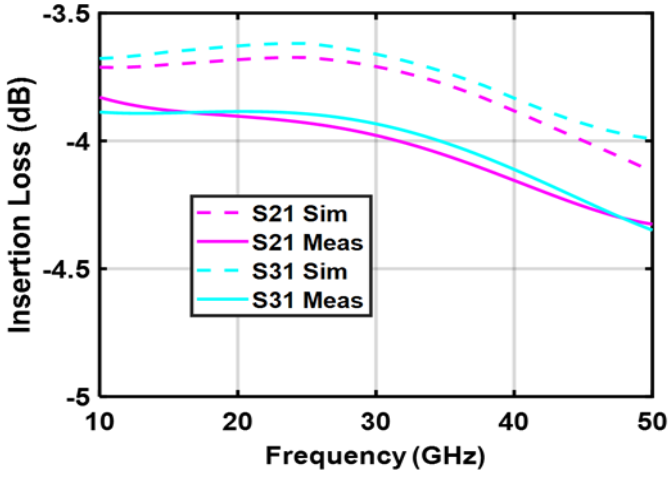

Figure 24. Measured vs. Simulated S-Parameter Insertion Loss Performance of the WPDC

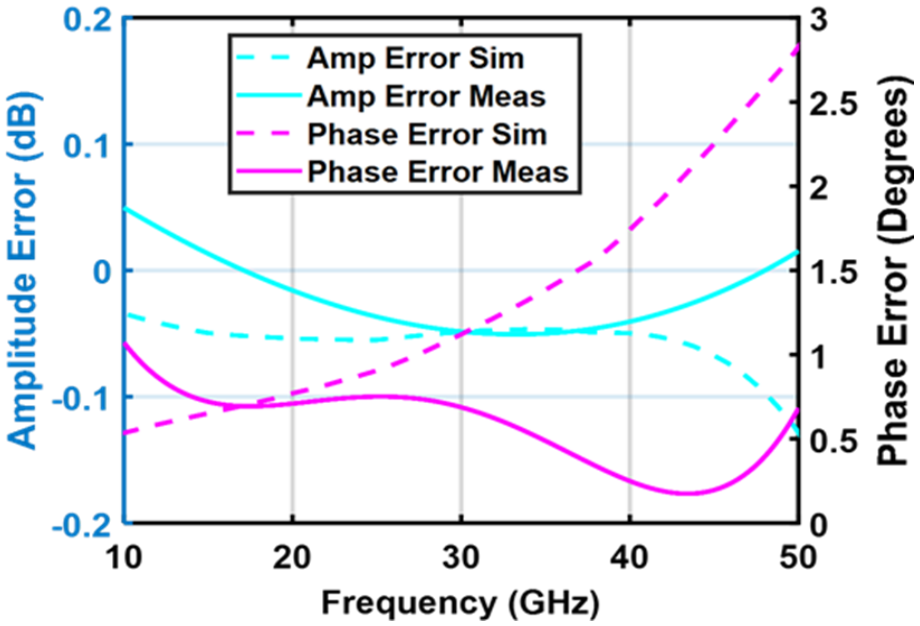

Figure 25. Measured vs. Simulated S-Parameter Amplitude and Phase Error Performance of the WPDC

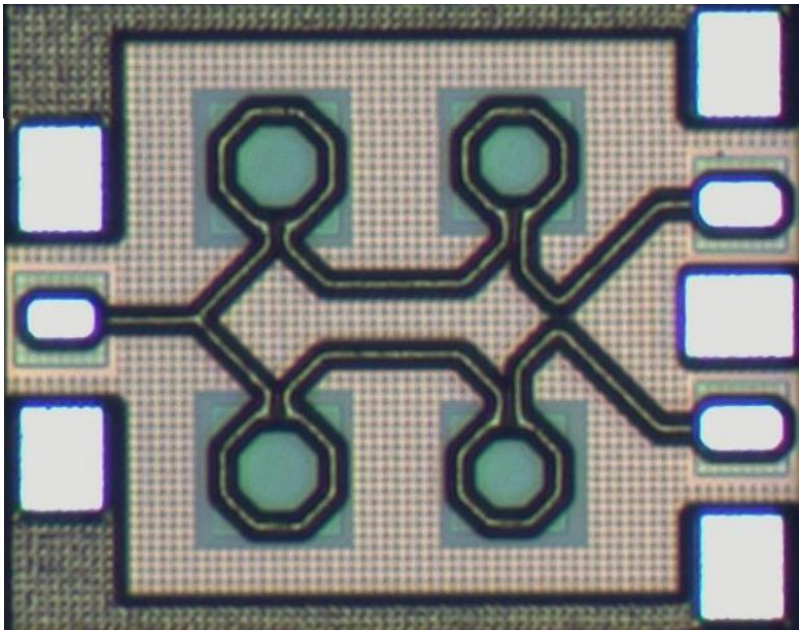

Figure 26. Die Photograph of the Fabricated WPDC

Table 2 - Performance Comparison with State-of-The-Art WPDC

Reference	[21]	[22]	[23]	[20]	**This Work**
Technology	Integrated Passive Device	65 nm CMOS	22 nm FD-SOI CMOS	130 nm SiGe BiCMOS	**130 nm SiGe BiCMOS**
Frequency (GHz)	14.2-37.8	20-40	15-55	5.2-19.5	**18-47**
IL (dB)	<1.2	<0.9	0.5-1.2	0.45-1	**0.83-1.3**
RL (dB)	>12	>10.5	>10	>10	**>10**
Isolation (dB)	>12	>12.7*	>10*	>10	**>10**
Amplitude Error (%)	N/A	N/A	<0.2	<0.06	**<0.05**
Phase Error (°)	<2	N/A	<3	<1	**<1**
Chip Area (mm^2)	0.274	0.125	0.036	0.11	**0.21**

*Simulated

CHAPTER 4. CIRCUIT-LEVEL SAFE-OPERATING-AREA OF A SIGE WIRELINE DRIVER

In this chapter, the Circuit-Level Safe-Operating-Area (C-SOA) of a DC-100 GHz SiGe BiCMOS wireline driver is determined at 5 GHz. First, the circuit of interest and its relevant performance metrics are presented. A measurement methodology of 10,000s DC stress across J_C and V_{CB} bias points is delineated and carried out. The pre- and post- 5 GHz OP1dB performance before and after the stressing is shown, and from the pre- vs post data, a C-SOA is established based on whether a performance degradation was shown for the best circuit performance. In conclusion, a C-SOA on a DC IV plane is shown with a degradation and performance table.

4.1 Introduction

Optical communications has become crucial to support modern applications such as 4G/5G backbones, internet, and emerging satellite communications [24]-[25]. In optical communications, an optical modulator is necessary for going from the electrical to the optical domain, which requires a large voltage swing in the electrical domain. Optical modulators change their refractive index as a function of the voltage applied across their terminals which results in the modulation of light or optical signals [26]. SiGe HBT technologies demonstrate highly competitive cost-performance with III-V technologies in the realm of driver circuits. SiGe HBTs can simultaneously achieve the good output power, high bandwidth, and gain necessary for driver circuits; at the same time, it also boasts

integrability with the CMOS backend data converters needed for modern digital communications [27]-[28].

Wireline drivers necessitate robust circuitry that can sustain large voltage output swings and good gain simultaneously [29]-[30]. The DC safe operating area and physical non-linearities defined at the device level dictate the reliable, practical performance that driver circuits can obtain. In general, higher device-level bias points allow for greater performance, but higher bias also poses a risk to the device or circuit reliability over time. However, using device reliability guidelines for practical circuit design may potentially throwaway reliable, improved performance, which is greatly undesired.

Most PDKs detail SOA in terms of a single device, but when devices are configured in a circuit, the boundaries of the SOA can shift beyond what was thought to be acceptable for a single device, which has been proven in [2]. Prior research has already investigated the limits of DC-SOA for single devices- developing aging models for base current increase [14]. Work has also been done in the area of reliable RF-operation of driver circuits, reliability-informed design techniques for Power Amplifiers, and empirical aging models of Power Amplifiers [5],[15]-[16]. However, these prior works never delineated a practical, performance-informed circuit safe-operating-area (C-SOA). In this work, a C-SOA is presented that is defined as a region where the circuit performance does not degrade over time [31]. This C-SOA also maintains that it is performance informed meaning the best possible performance is being achieved without degrading the circuit performance over time. The mechanisms for circuit performance degradation are also investigated to develop a physical understanding of the C-SOA.

4.2 Circuit

4.2.1 SiGe HBT DC Reliability Mechanisms

With greater I_C and V_{CB}, SiGe HBT non-linearity is known to be reduced [2]. However, a potential pitfall of biasing at more aggressive regimes to achieve improvements in large-signal performance is damaging the SiGe HBT device over time. In [13], it has been shown that under high injection and mixed-mode stress, Auger hot-carriers can damage the polysilicon regions of the base and emitter of SiGe HBTs. This is due to the collision of carriers excited by strong electric fields with the oxide interface; this results in a de-passivation of H-bonds and reduction of carrier mobility in the base and emitter polysilicon regions. In turn, this phenomenon can increase base and emitter resistance over time, which can degrade both linearity and gain performance of a circuit [13].

4.2.2 Circuit Design and Biasing Scheme

The circuit of interest is a SiGe HBT differential cascode wireline driver, and its schematic is pictured in Figure 27. The collector and base voltages are being forced, and the tail current is being forced through the Q_5:Q_6 current mirror. The J_C of each individual device is calculated via Equation 2.

$$J_C = \frac{I_C}{2A_E} \tag{2}$$

I_C is the measured collector current and A_E is the emitter area of Q_1-Q_4, which are all identical. I_C is divided by 2 to yield I_C for each branch- owing the nature of the differential circuit. V_{CB} for the upper device is set through Equation 3.

$$V_{CB,upper} = V_{CC} - \frac{R_L * I_C}{2} - V_{CAS} \quad (3)$$

V_{CC} is the collector voltage, V_{CAS} is the cascode voltage, I_C is the measured collector current, and R_L is the load resistor of 70 Ω. V_{CB} for the lower device was set by Equation (4).

$$V_{CB,lower} = V_{CAS} - V_{BE34} - V_{BB} \quad (4)$$

V_{BE34} is the base-emitter voltage of the cascode devices assumed to be ~1 V at high injection, and V_{BB} is the base bias voltage that is forced through a bias-tee.

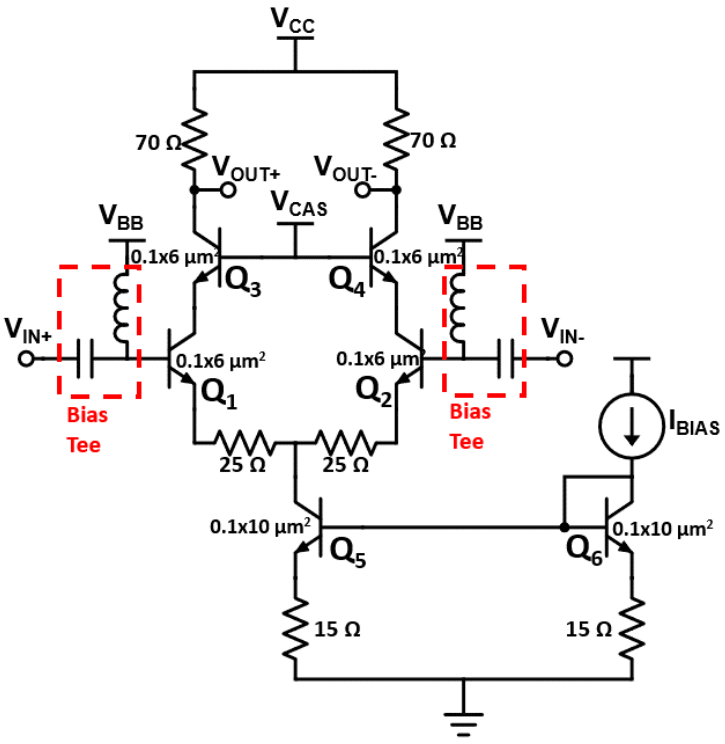

Figure 27. Schematic of differential SiGe cascode driver circuit

4.3 Experiment and Results

To determine the best bias points for delineating the C-SOA, Gain and OP1dB at 5 GHz was measured at bias points across J_C and V_{CB} of each individual device in the circuit as computed in Equations 2-4 and shown in Figure 28. The optimal biasing point was found to be J_C=42 mA/μm^2. So, the tradeoff between gain and OP1dB had to be determined at this current density as a function of V_{CB} in Figure 29, which would be the parameter of interest for mixed-mode stress. Upon performing these measurements, 10,000 second DC stress measurements for increasing V_{CB} at J_c=42 mA/μm^2 were done to gauge a performance vs. reliability tradeoff of the driver.

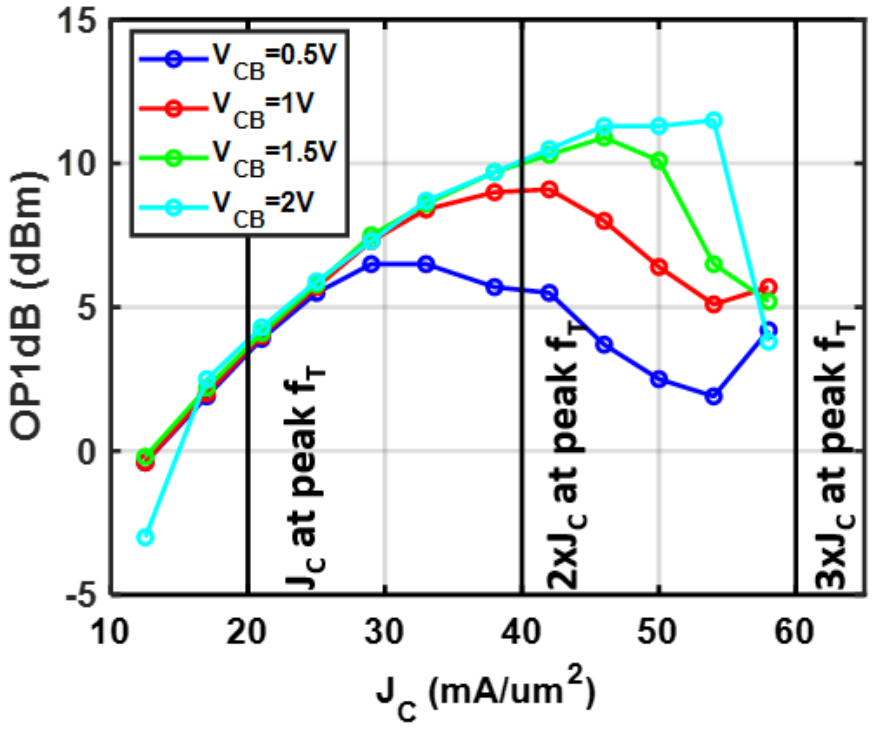

Figure 28. Driver cricuit OP1dB vs. J_C for various V_{CB} operating points

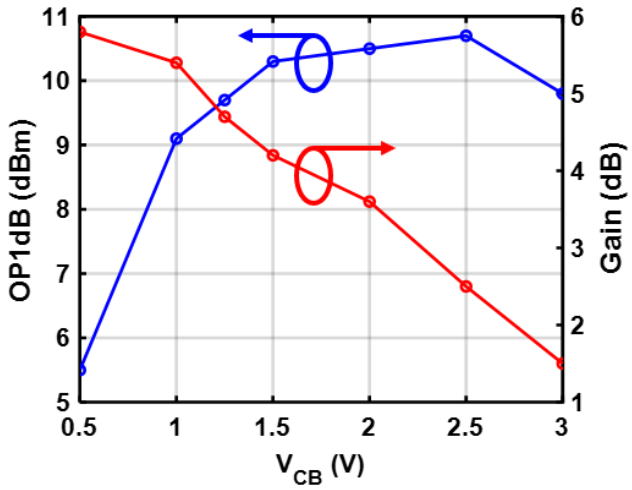

Figure 29. Gain and OP1dB vs. V_{CB} for fixed JC=42 mA/μm^2

In Figure 30, the results showed that no degradation in performance was seen beyond V_{CB} = 1 V. Thus, the optimal point for performance and reliability was found to be J_c=42 mA/μm^2 and V_{CB}=1V. Even at bias points beyond this optimal point, degradation was found to be minimal.

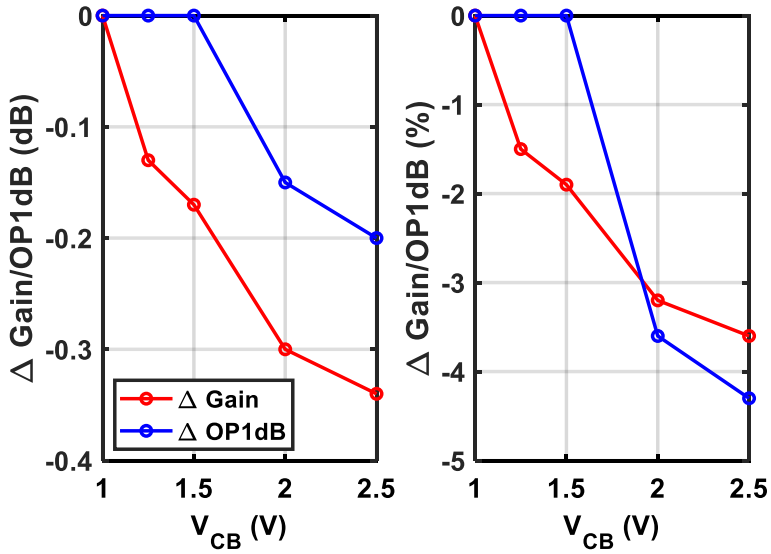

Figure 30. OP1dB and gain degradation vs. VCB. Note that percent degradation was computed by converting dB to linear

To determine the physical cause of the gain and OP1dB degradation at increasing V_{CB}, a single SiGe HBT under mixed mode stress for 10,000 seconds had to be characterized for pre- and post- stress characteristics. The 0.1x4 μm^2 device was biased at J_C=42 mA/μm^2 and V_{CB}=1.3 V for 10,000 seconds with pre- and post- base and emitter resistances extracted via the Z-parameter method shown in Figure 31. Although this method does not accurately capture the exact value, it shows the relative change well.

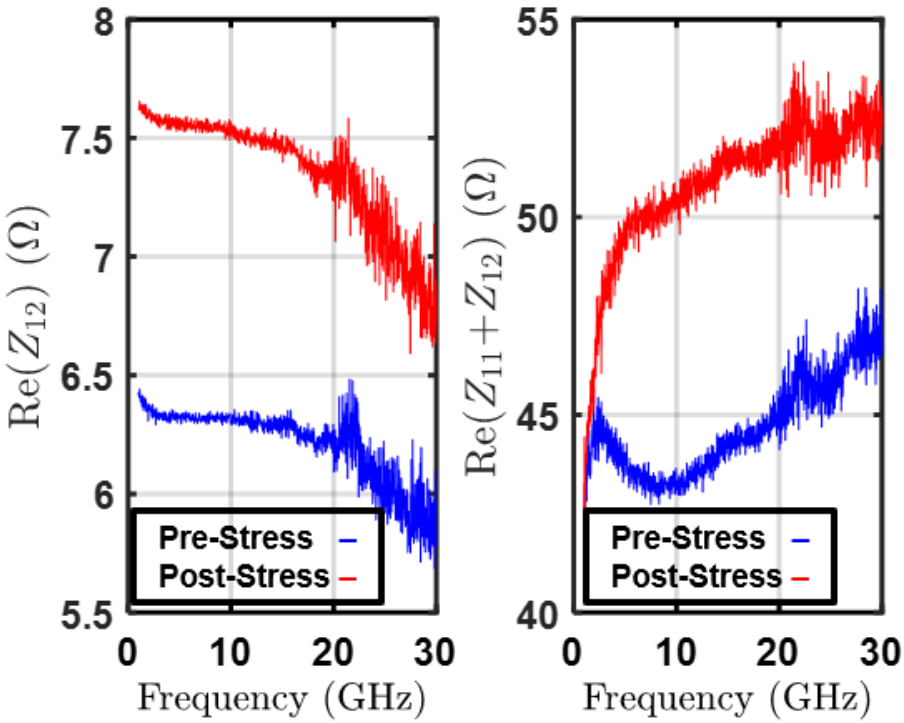

Figure 31. On the left, emitter resistance is shown to increase by 1 Ω after 10,000 seconds of stress time, whereas base resistance increased by 5 Ω after the same period. The device measured was a 0.1x4 μm^2 common-emitter device biased at V_{CB}=1.3 V and J_C=40 mA/μm^2 .

Based on the relative degradation in base and emitter resistances, the circuit was re-simulated in Cadence Virtuoso and compared with the measured performance degradation shown in Figure 32. The resistances were added as ideal series resistors with

the transistor terminals. The simulations closely match the measured performance degradation at V_{CB}=1.5 V.

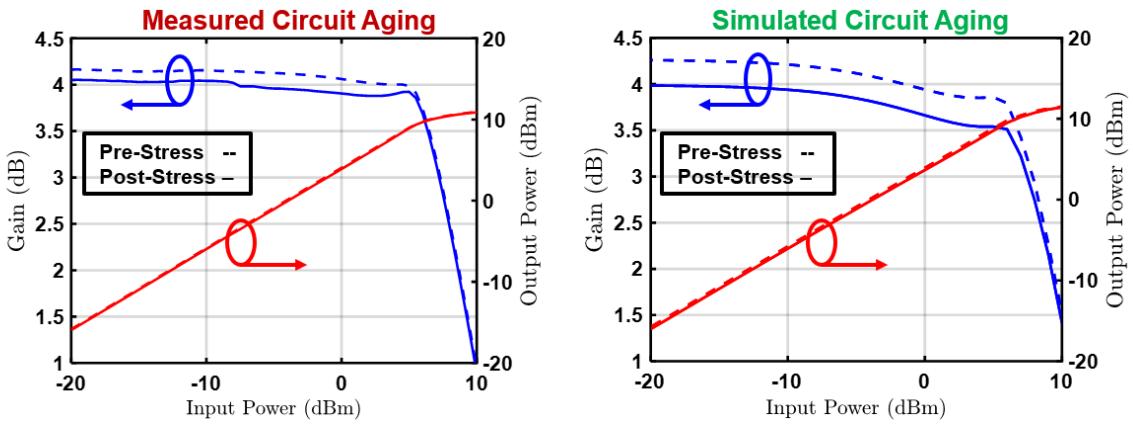

Figure 32. Simulated vs Measured driver performance degradation under mixed-mode stress

4.4 Conclusion

The optimal C-SOA point was found to be J_C=42 mA/μm^2 and V_{CB}=1 V or V_{CE}=2 V, which resulted in the best possible performance without any circuit performance degradation after 10,000 seconds of DC stress. Although degradation was seen at V_{CB} in excess of 1V, it was minimal while still maintaining OP1dB performance merit. J_C above 42 mA/μm^2 was not investigation due to not possessing optimal performance compared to the optimal point found at J_C = 42 mA/μm^2. The measured, performance-informed C-SOA on a DC IV plane is pictured in Figure 33. A pre- and post- stress OP1dB and Gain performance table is shown in Table 3.

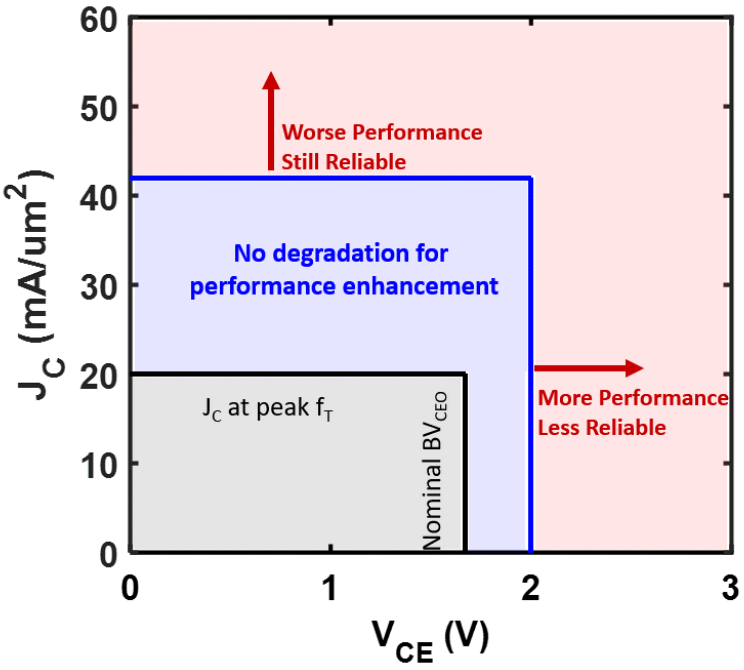

Figure 33. Circuit-SOA overlaid with PDK-defined single transistor SOA

Table 3 - Pre Vs. Post Stress Circuit Performance At Fixed J_C and Increasing V_{CB}

V_{CB} (V)	RF Performance		
	Pre-Stress Gain (dB)/OP1dB (dBm)	Post-Stress Gain (dB)/OP1dB (dBm)	ΔGain/ΔOP1dB (dB)
1	5.4/9.1	5.4/9.1	0/0
1.25	4.2/10.3	4.0610.3	-0.14/0
1.5	3.6/10.5	3.42/10.5	-0.18/0
2	2.5/10.7	2.2/10.55	-0.3/-0.15
2.5	1.5/9/8	1.15/9.6	-0.35/-0.2

*J_C=42 mA/μm^2 for all VCB bias voltages

CHAPTER 5. CONCLUSION

5.1 Summary of Works

This study has demonstrated design techniques for CMOS-based TR switches and WPDC through knowledge of passive design on-chip and device level parasitics direction translation to circuit level performance. Triple n-well design and stacking was utilized to mitigate the effects of device parasitics for the CMOS TR switch, and embedded high-Q MOM capacitors were used to save area, maximize bandwidth, and minimize insertion loss for the WPDC. The performances achieved in both circuits demonstrate SiGe BiCMOS technologies to be a strong contender for applications in the mm-Wave and RF sphere of circuit design.

The study has also demonstrated the C-SOA of a SiGe HBT based wireline driver by defining the best possible performance bias point where the circuit endured no performance degradation. Such robust performance under 2x J_C peak f_T bias pushes the limit of what was thought possible based on individual device PDK SOA. The circuit performance achieved showcase SiGe HBTs to be a viable candidate for use in driver circuits that require high output power and reliable output stages.

The specific contributions of this work are listed below:

1. The design of the 2-20 GHz CMOS TR SPDT switch was presented. The switch achieved low insertion loss, good linearity, and large bandwidth across the frequency range of 2-20 GHz. This was achieved due to the utilization of the triple well device and optimized transistor stacking. The

linearity performance of >18 dBm at 11 GHz and <3 dB insertion loss is competitive with existing state-of-the-art TR switches.

2. The design of an 18-47 GHz WPDC was presented. The circuit achieved low insertion loss, low amplitude and phase error, wide bandwidth, and small die area across the frequency range of 18-47 GHz. This was achieved due to the utilization of 4 $\lambda/16$ π-networks to push out the artificial transmission line cut-off frequency and center-tapped inductors with MOM capacitors at the center-taps to improve insertion loss. This design is very competitive with existing state-of-the-art WPDCs in terms of measured performance of <1.3 dB insertion loss and 30 GHz of bandwidth for negligible amplitude and phase error.
3. The reliability study of the C-SOA of a SiGe HBT based wireline driver was presented. It demonstrated that due to the configuration of individual SiGe HBT devices in a differential cascode structure with forced tail current, device defined PDK SOA limits could be breached to achieve a large OP1dB performance gain of 5 dB compared to the baseline SOA performance. This was previously not thought to be possible at an operating point of J_C=42 mA/μm^2 and V_{CB}=1 V, but the study showed that this mixed-mode stress operating point of BV_{CEO} and 2x J_C at peak f_T saw no degradation in circuit performance over time while achieving the best performance. For higher V_{CB}, the device-level mechanism that caused degradation was verified to be increases in the base and emitter resistances due to mixed-mode stress. However, even at bias voltages where the

performance degraded, the degradation was minimal. This study proved SiGe HBTs to be a highly robust and reliable candidate for wireline driver design.

REFERENCES

[1] F. Ellinger, C. Tzschoppe, D. Fritsche, P. Stärke, K. Ishida, and T. Meister, "Review of Fast, Efficient and Bendable Radio-Frequency Integrated Receivers for the Wireless Communication Systems ofthe Future," in *2018 IEEE-APS Topical Conference on Antennas and Propagation in Wireless Communications (APWC)*, 2018, pp. 766-768.

[2] J. D. Cressler and G. Niu, *Silicon-germanium heterojunction bipolar transistors*, Boston, MA: Artech House, 2003

[3] J. J. Pekarik *et al.*, "A 90nm SiGe BiCMOS technology for mm-wave and high-performance analog applications," in *2014 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*, 2014, pp. 92-95.

[4] H. Zirath, S. Carpenter, Z. He, V. Vassilev, and M. Bao, "Multifunction MMICs for high datarate wireless and optical communication based on state-of-the-art InP DHBT and SiGe BiCMOS processes," in *2018 22nd International Microwave and Radar Conference (MIKON)*, 2018, pp. 230-233.

[5] M. A. Oakley, U. S. Raghunathan, B. R. Wier, P. S. Chakraborty, and J. D. Cressler, "Large-Signal Reliability Analysis of SiGe HBT Cascode Driver Amplifiers," *IEEE Transactions on Electron Devices*, vol. 62, no. 5, pp. 1383-1389, 2015.

[6] G. G. Fischer, B. Heinemann, M. Kaynak, and H. Rücker, "High-speed SiGe BiCMOS technologies for applications beyond 100 GHz," in *2013 European Microwave Integrated Circuit Conference*, 2013, pp. 172-175.

[7] D. M. Pozar, *Microwave engineering*, 3rd ed. Hoboken, NJ: J. Wiley, 2005

[8] S. Chakraborty, L. E. Milner, X. Zhu, O. Sevimli, A. E. Parker, and M. C. Heimlich, "An Edge-Coupled Marchand Balun With Partial Ground for Excellent Balance in 0.13 μm SiGe Technology," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 68, no. 1, pp. 226-230, 2021.

[9] C. Kuo, C. Kuo, C. Lien, J. Tsai, and H. Wang, "A Novel Reduced-Size Rat-Race Broadside Coupler and Its Application for CMOS Distributed Sub-Harmonic Mixer," *IEEE Microwave and Wireless Components Letters*, vol. 18, no. 3, pp. 194-196, 2008.

[10] R. L. Schmid, A. Ç. Ulusoy, P. Song, and J. D. Cressler, "A 94 GHz, 1.4 dB Insertion Loss Single-Pole Double-Throw Switch Using Reverse-Saturated SiGe HBTs," *IEEE Microwave and Wireless Components Letters*, vol. 24, no. 1, pp. 56-58, 2014.

[11] M. Ahn, C. Lee, B. Kim, and J. Laskar, "A Novel Multi-Stack Device Structure and its Analysis for High Power CMOS Switch Design," in *2007 IEEE/MTT-S International Microwave Symposium*, 2007, pp. 1393-1396.

[12] Q. Li and Y. P. Zhang, "CMOS T/R Switch Design: Towards Ultra-Wideband and Higher Frequency," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 3, pp. 563-570, 2007.

[13] U. S. Raghunathan *et al.*, "Hot-Carrier-Damage-Induced Current Gain Enhancement (CGE) Effects in SiGe HBTs," *IEEE Transactions on Electron Devices*, vol. 65, no. 6, pp. 2430-2438, 2018.

[14] B. R. Wier, R. P. Martinez, U. S. Raghunathan, H. Ying, S. Zeinolabedinzadeh, and J. D. Cressler, "Revisiting Safe Operating Area: SiGe HBT Aging Models for Reliability-Aware Circuit Design," in *2018 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)*, 2018, pp. 215-218.

[15] P. Srinivasan, P. Colestock, T. Samuels, S. Moss, F. Guarin, and B. Min, "A novel methodology to evaluate RF reliability for SOI CMOS-based Power Amplifier mmWave applications," in *2020 IEEE International Reliability Physics Symposium (IRPS)*, 2020, pp. 1-4.

[16] E. Rahimi, J. Zhao, F. Svelto, and A. Mazzanti, "High-Efficiency SiGe-BiCMOS E-Band Power Amplifiers Exploiting Current Clamping in the Common-Base Stage," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 8, pp. 2175-2185, 2019.

[17] N. Rostomyan, M. Özen, and P. M. Asbeck, "Synthesis Technique for Low-Loss mm-Wave T/R Combiners for TDD Front-Ends," *IEEE Transactions on Microwave Theory and Techniques*, vol. 67, no. 3, pp. 1030-1038, 2019.

[18] H. J. Ng, R. Feger, and D. Kissinger, "Scalable mm-Wave 4-Channel Radar SoC with Vector Modulators and Demodulators for MIMO and Phased Array Applications," in *2018 IEEE/MTT-S International Microwave Symposium - IMS*, 2018, pp. 1472-1475.

[19] T. Fujibayashi *et al.*, "A 76- to 81-GHz Multi-Channel Radar Transceiver," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 9, pp. 2226-2241, 2017.

[20] I. Ju, M. Cho, I. Song, and J. D. Cressler, "A Compact, Wideband Lumped-Element Wilkinson Power Divider/Combiner Using Symmetric Inductors with Embedded Capacitors," *IEEE Microwave and Wireless Components Letters*, vol. 26, no. 8, pp. 595-597, 2016.

[21] Z. Li, L. Lv, R. Zeng, and J. Lv, "A Compact Wideband Wilkinson Power Divider using Periodic Synthesized Transmission Line in Silicon IPD Process," in *2019 49th European Microwave Conference (EuMC)*, 2019, pp. 133-136.

[22] H. Oh *et al.*, "28 GHz Wilkinson power divider with λ/6 transmission lines in 65nm CMOS technology," in *2016 46th European Microwave Conference (EuMC)*, 2016, pp. 206-209.

[23] S. Lee, M. Huang, Y. Youn, and H. Wang, "A 15 – 55 GHz Low-Loss Ultra-Compact Folded Inductor-Based Multi-Section Wilkinson Power Divider for Multi-Band 5G Applications," in *2019 IEEE MTT-S International Microwave Symposium (IMS)*, 2019, pp. 432-435.

[24] A. O. Mufutau, F. P. Guiomar, M. A. Fernandes, A. Lorences-Riesgo, A. Oliveira, and P. P. Monteiro, "Demonstration of a hybrid optical fiber–wireless 5G fronthaul coexisting with end-to-end 4G networks," *IEEE/OSA Journal of Optical Communications and Networking*, vol. 12, no. 3, pp. 72-78, 2020.

[25] X. Zhang *et al.*, "Free-space broad-spectrum optical communication based on supercontinuum," in *2017 16th International Conference on Optical Communications and Networks (ICOCN)*, 2017, pp. 1-3.

[26] T. L. Nguyen, L. Li, G. Salamanca, and O. Mizuhara, "90mW, 4.4Vp-p, 11.35Gb/s MZM driver enabling low-power tunable transmitter for SFP+ module application," in *2017 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, 2017, pp. 1-3.

[27] I. G. López, P. Rito, L. Zimmermann, D. Kissinger, and A. C. Ulusoy, "A 40 Gbaud SiGe:C BiCMOS driver for InP segmented MZMs with integrated DAC functionality for PAM-16 generation," in *2016 IEEE MTT-S International Microwave Symposium (IMS)*, 2016, pp. 1-4.

[28] P. Rito *et al.*, "A monolithically integrated segmented driver and modulator in 0.25 µm SiGe:C BiCMOS with 13 dB extinction ratio at 28 Gb/s," in *2016 IEEE MTT-S International Microwave Symposium (IMS)*, 2016, pp. 1-4.

[29] S. Mandegaran and A. Hajimiri, "A Breakdown Voltage Multiplier for High Voltage Swing Drivers," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 2, pp. 302-312, 2007.

[30] A. H. Ahmed *et al.*, "30.6 A 6V Swing 3.6% THD >40GHz Driver with 4.5× Bandwidth Extension for a 272Gb/s Dual-Polarization 16-QAM Silicon Photonic Transmitter," in *2019 IEEE International Solid- State Circuits Conference - (ISSCC)*, 2019, pp. 484-486.

[31] A. Moradinia, R. P. Martinez, J. W. Teng, N. Sepúlveda-Ramos, H. Lee, and J. D. Cressler, "Circuit-Level Safe-Operating-Area of a High-Speed SiGe BiCMOS Wireline Driver," in *2020 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)*, 2020, pp. 1-5.