CHARGE TRAPPING IN POLYMER DIELECTRICS AND

POTENTIALS AT ORGANIC DONOR-ACCEPTOR JUNCTIONS—THE

ROLE OF INTERFACE AND BULK CONTRIBUTIONS

by

Olivia Alley

A dissertation submitted to Johns Hopkins University in conformity with the

requirements for the degree of Doctor of Philosophy

Baltimore, Maryland

May, 2016

ABSTRACT

Organic electronics have attracted increasing interest during the past decade due to their potential applications in transparent, large-area, printable, and stretchable devices. Solution based material deposition considerably reduces processing costs, and allows the use of non-standard substrates in device design. Many organic electronic device parameters are controlled by interfacial as well as bulk properties.

Organic donor-acceptor junctions are relevant to organic photovoltaics (OPVs) as well as organic light emitting diodes (OLEDs). In an OPV, interfacial potentials between the hole transporting (donor) organic semiconductor (OSC) and electron transporting OSC (acceptor) lead to separation and recombination of electrons and holes. The mechanisms behind interfacial potential formation in organic donor-acceptor junctions are not fully understood and are an active area of study. In this thesis, the interfacial potential was measured, and interface and bulk contributions were separated by fabricating lateral organic donor-acceptor junctions both with and without a gap between the donor and acceptor materials. Contact between the donor and acceptor materials increases the interfacial potential beyond that calculated from bulk values.[1] This can be explained through differences in electron affinity of the donor and acceptor, and also by differences in the delocalization of molecular orbitals (MOs) of the two OSC films. Greater delocalization of MOs allows for electron donation to adjacent molecules,[2] a surprising result in organic electronics. In addition, the effect of the substrate on the potential was examined. The field is persistently negative on the acceptor side when the junction is made on a SiO_2 substrate.

When Al_2O_3, a substrate with higher dielectric constant, is used, the field decreases in one case, and reverses in the other.

For organic field effect transistors (OFETs), the instability of switching voltages is an interface-dominated issue which causes the device left on to turn off over time, referred to as bias stress. Bias stress, caused by charges trapped at the dielectric/OSC interface, can be quantified by a shift in the threshold voltage (V_{th}) of the device. This thesis discusses localizing trapped charges in an OFET dielectric to control bias stress and operating voltages. By changing numbers and positions of trapped charges in the dielectric, the voltage at which the OFET turns on can be defined, and by pre-populating interfacial traps before running the device, bias stress may be reduced. In this thesis, charging of bilayer and trilayer dielectrics made from in-house synthesized 'chargeable' substituted polymers was studied.[3] There was greater stabilization of trapped charges at the dielectric/OSC interface in chargeable polymers adjacent to the OSC, indicating charging occurs through an interface-driven mechanism. However, when they were encapsulated such that the chargeable polymer was situated between two layers of unsubstituted polymer, there was less response to charging than in the fully unsubstituted control. This reduction in bias stress susceptibility could stem from the bulk dielectric polarization of the chargeable layer, which counteracts the charge trapping mechanism at the dielectric/OSC interface.

Advisor: Professor Howard E. Katz

CONTENTS

LIST OF TABLES

LIST OF FIGURES

x

CHAPTER I: Introduction to Organic Electronics

1   The current state of organic electronics

Organic electronics are highly versatile in form, with the potential for electronic devices with mechanical flexibility and stretchability, optical transparency or translucency, and self-healing characteristics. Many organic electronics materials can be processed at low temperatures and from solution, which could vastly reduce production costs and allow for printed, spray-coated, or painted electronics, as well as deposition on novel substrates. Organic materials can form the conducting, semiconducting, and/or insulating layers of electronic devices such as photovoltaics, LEDs, and transistors. The highly developed field of synthetic organic chemistry allows for precise control of physical, electronic, and optical properties of materials to obtain these characteristics.

Organic electronics devices include organic photovoltaics (OPVs), organic light emitting diodes (OLEDs), and organic field effect transistors (OFETs). OPVs produce current under illumination when light absorption leads to excitation of an electron to a high-energy state, creating a bound electron/hole pair. Separation of the electron and hole occurs at the interface between a hole transporting and an electron transporting organic semiconductor (OSC). The performance of OPVs has increased significantly in recent years, with the current world record for power conversion efficiency (PCE) as of February 2016 reaching 13.2%, measured in a proprietary multi-junction OPV by the solar energy company Heliatek.[4] In a 2013 Advanced Materials review article, Gan, et al. discussed modification of single junction OPVs to gain 10% efficiencies by incorporating metallic nanoparticles to

increase light absorption.[5] In a 2012 study published in Nature Photonics, a tandem (two junction) polymer solar cell performed with 8.5% efficiency.[6] Dou, et al. were able to observe this efficiency in a majority (300 out of 500) of the cells they fabricated. They also tested device stability, and observed a drop in PCE of 0.4% or less in the first 30 days. Current research is focused on increasing the PCE, scalability, reproducibility, and lifetime of organic solar cells. While the efficiencies in OPVs are lower than they are in silicon solar cells, their appeal lies in the potential for low temperature, large-scale production, and the use of non-standard substrates. The infrastructure to produce OPVs on a larger-than-lab scale exists currently as shown in the 2015 World Expo, where solar energy company Belectric provided roof-scale arrays of translucent roll-to-roll printed OPV cells with 5% PCE to generate energy for a structure.

OLEDs are, similar to OPVs, composed of two OSCs, one that transports holes, the conductive layer, and one that transports electrons and has light emitting properties, the emissive layer. The OSCs are sandwiched between electrodes. A voltage is applied across the electrodes, which injects electrons into the emissive layer and holes into the conductive layer. The electrons and holes meet and recombine within the emissive layer, from which light is emitted. OLED research now is focused on increasing the device operational lifetime of OLEDs, specifically those that emit in the blue region. As Kim et al., describes in a review of blue OLED materials, difficulties arise in matching the energy levels of the blue light emissive material with those of the electrodes. The large band gap in blue emitters doesn't overlap well with electrode work functions, and the mismatch reduces efficiency as well as the device lifetime.[7] Nonetheless, OLEDs are currently highly commercialized, used in large-area lighting and flexible, translucent, or curved displays.

OFETs are thin film transistors utilizing organic semiconductors, typically operating in accumulation mode due to their low intrinsic conductivity. In accumulation mode, free carriers must be generated in the channel of the OFET for current to flow, as illustrated in Figure 1. Thin film transistors, including OFETs, are three terminal devices, with two electrodes (the source and drain) held at a constant bias across a region of OSC (the channel), and the third 'gate' electrode separated from the OSC by a dielectric layer. Carriers injected from the electrodes are transported across the channel when there is a sufficiently high gate voltage.
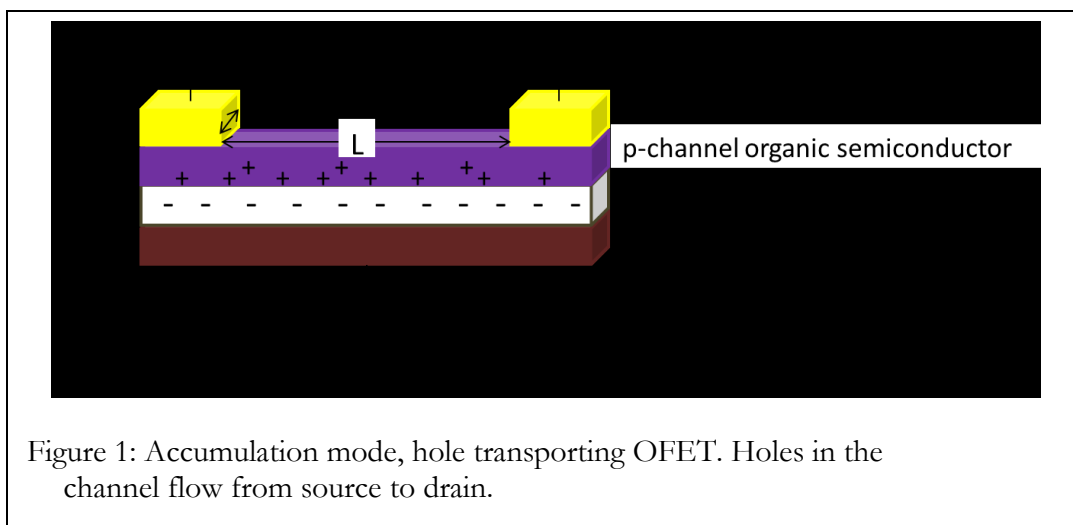
Figure 1: Accumulation mode, hole transporting OFET. Holes in the channel flow from source to drain.

Output current measured at the drain electrode depends on the source/drain voltage, source/drain electrode dimensions, gate voltage, and the mobility of the free carriers in the semiconductor/dielectric combination used. OFETs are modified for use in sensing platforms, and also are of interest for cheap, flexible memory. Another major application is characterization of new organic semiconductors and insulators, since analysis of an OFET allows extraction of key material parameters.

Besides organic electronics devices, a common application of organic electronic materials is in xerography, as the dopant in molecularly doped polymers (MDPs), used in

nearly all photocopiers today. MDPs are made up of 70% non-conductive base, such as polycarbonate, and 30% triphenyl amine, an organic molecule that exhibits photoconductivity.[8] The final MDP blend has high conductivity when illuminated, but low conductivity in the dark. This breakthrough in xerography occurred in the 1970s.

2   Organic semiconductors: materials, processing, and charge transport mechanism

2.1   Small molecule semiconductors

The first OSCs developed were single crystals of the small molecules naphthalene and anthracene (Figure 2). Both of these molecules have delocalized π orbitals from conjugated (alternating single and double) carbon-carbon bonds. However, the brittle nature of these molecular crystals required the use of relatively thick crystals to prevent breaks. Combined with the already high barrier to conduction in OSCs, this meant that the operating voltages for single crystal OSC devices were hundreds of volts, which was deemed too high for practical applications.[8] The field of OSCs shifted away from single crystals to amorphous and polycrystalline films which could be deposited from solution or vapor onto a substrate.[8] Because amorphous and polycrystalline films are less brittle, thinner layers are used, which decreases the required operating voltages. Other polyacenes such as tetracene, pentacene, pyrene, and perylene were developed, and it was determined that polyacenes with an increasing number of rings have a higher free carrier mobility. This pattern continues for larger materials such as hexacene, but polyacenes with six or more rings are not stable to air and light. Hexacene, for example, was found to degrade by photo-oxidation to an

endoperoxide structure, with significant depletion of hexacene absorptions after less than 30 minutes. [9]
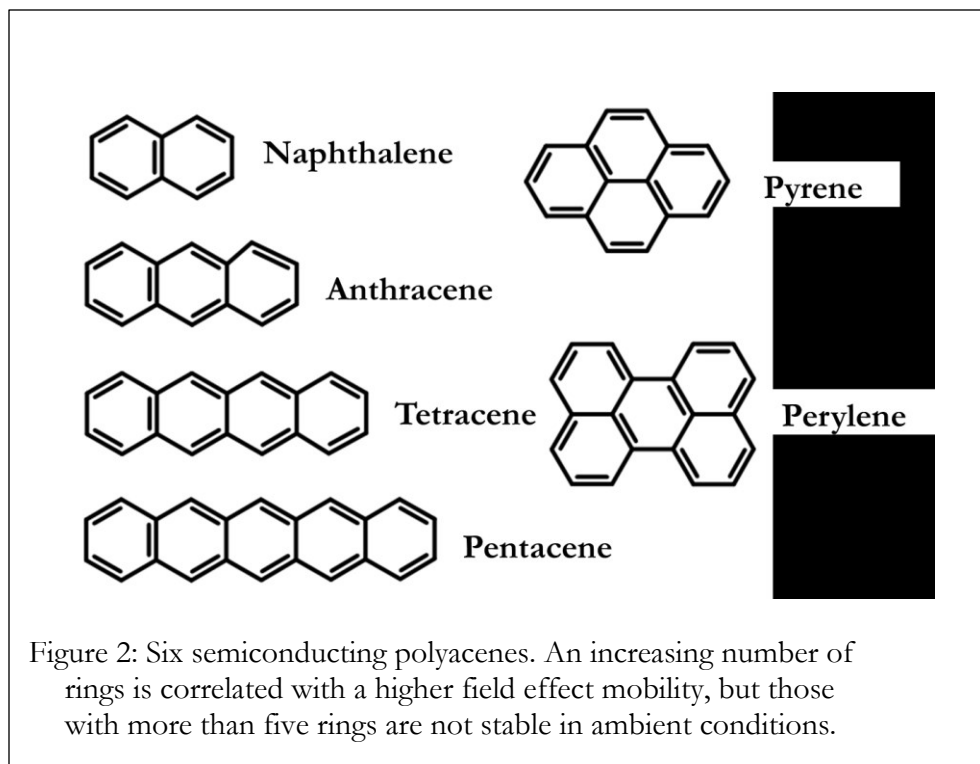
Figure 2: Six semiconducting polyacenes. An increasing number of rings is correlated with a higher field effect mobility, but those with more than five rings are not stable in ambient conditions.

Today, pentacene is a commonly used hole transporting small molecule semiconductor. It is vapor deposited to give a good quality polycrystalline film, but has low solubility so cannot be solution processed. Since one of the benefits of organic electronics is their potential to be deposited from solution on flexible, large area, or non-standard substrates, OSCs which can be dissolved in common organic solvents are also needed. For example, by adding a pair of particular solubilizing side chains to pentacene, another OSC is obtained, 6,13-bis(triisopropylsilylethynyl) pentacene (TIPS-pentacene). This substitution increases solubility, and also slightly shifts the energy levels of the material, as shown in Figure 3. As will be discussed in the next section, the highest occupied molecular orbital (HOMO) and lowest unoccupied molecular orbital (LUMO) are the main energy levels

where carrier transport occurs. The values of HOMO and LUMO here were calculated using density functional theory (DFT).[10] A third effect of the addition of side chains to a semiconducting core can be to improve packing by maintaining a set distance between semiconducting cores.[8]

Figure 3: The structures and frontier orbitals of pentacene and 6,13-bis(triisopropylsilylethynyl) pentacene (TIPS-pentacene).
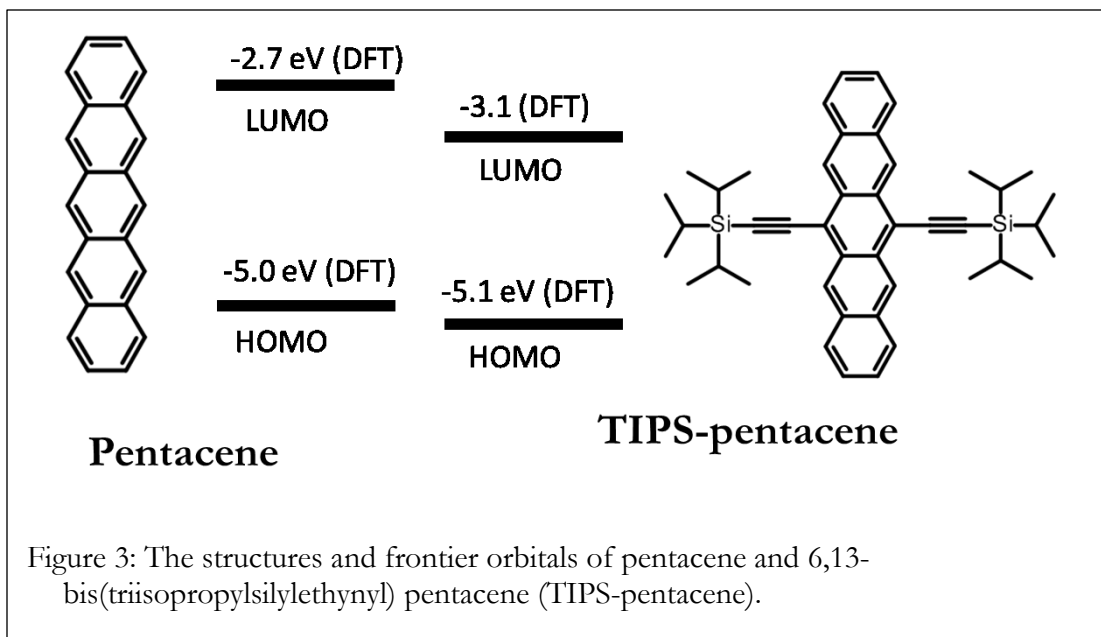
Besides polyacenes, there are numerous other types of molecular OSCs, including the graphene-esque fullerenes and carbon nanotubes. Fullerenes, aka buckyballs, are commonly used as electron transporting materials in OPVs. The smallest fullerene, C_{60}, is composed of 60 carbon atoms arranged in 20 six-membered rings and 12 five-membered rings. Each five membered ring is surrounded by five six membered rings, as shown in Figure 4. C_{60} has low solubility, so is frequently vapor deposited. A substituted fullerene, phenyl-C_{61}-butyric acid methyl ester (PCBM), can be deposited from either vapor or solution. The orbital energies in Figure 4 were determined by DFT.[11,12]

Besides having increased solubility, PCBM is slightly more air-stable than C_{60}. The LUMO of PCBM is farther from vacuum, -3.7 eV compared to -3.2 eV. The reduction

6

potential of water and oxygen is equivalent to approximately -4 eV from vacuum, implying

materials with oxidation potentials smaller than that can be oxidized.[12] When C_{60} has been

reduced by electron transfer to C_{60}^-, the occupied LUMO has a 0.8 eV driving force to be

oxidized by ambient water and oxygen, while for PCBM, oxidation is still favorable, but the

driving force is reduced. Fullerenes have been synthesized with LUMOs greater than 4 eV,

and shown to be fairly air stable, but they are not in mainstream use currently.[13] However,

besides this rule of thumb concerning the position of the LUMO, stability in air depends on

morphology of the film as well as possible film contaminants.[12]

Figure 4: The structure and frontier orbitals of C_{60} and PCBM, calculated by
density functional theory (DFT). The LUMO of PCBM is 0.5 eV greater
than that of C_{60}, giving it somewhat higher air stability in addition to higher
solubility.
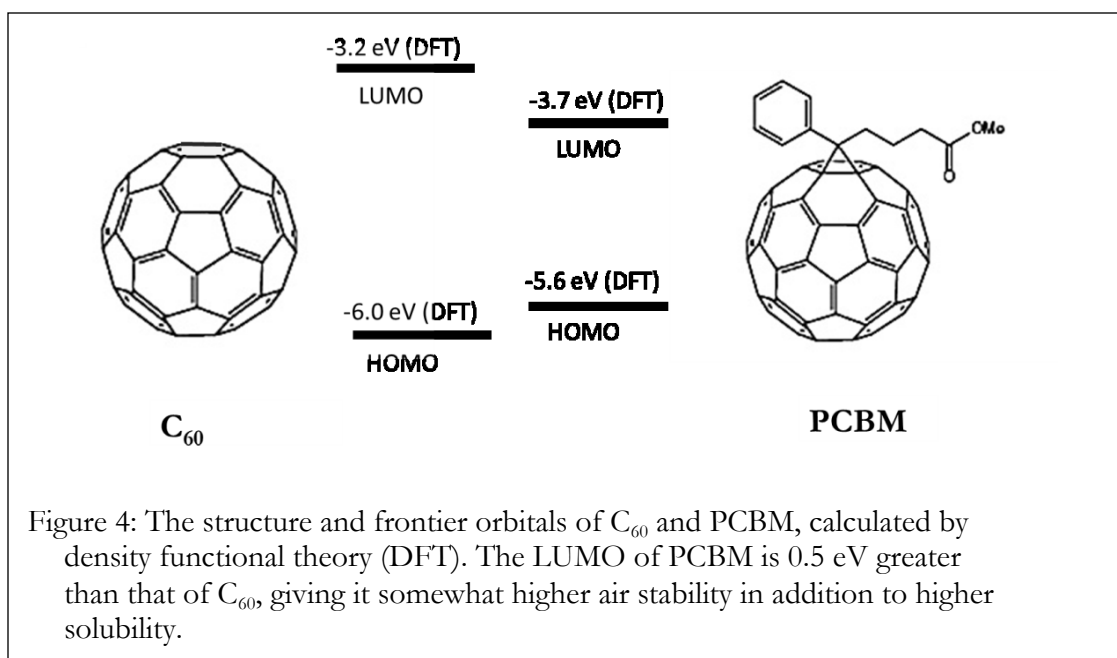
Semiconducting single-walled carbon nanotubes (s-SWCNTs) are hole-transporting

semiconductors used in OPVs, which absorb light in the infrared portion (IR) of the

spectrum. The IR tends to be an underutilized portion of the solar spectrum in OPVs, since

most polymer donors have band gaps that absorb visible light. The exact absorbance of a

specific s-SWCNT is defined by its diameter or 'chirality', which is determined by the

alignment of the hypothetical graphene layer rolled up to make the tube. Chirality determines

if the carbon nanotube is conductive (metallic) or semiconducting. Among semiconducting

carbon nanotubes, smaller diameter s-SWCNTs absorb at higher energy, shorter

wavelengths, and in a film containing several chiralities, energy can be lost as free carriers

hop between different chiralities. Therefore, it is desirable to have films composed of only a

few chiralities.[14]

2.2   Semiconducting polymers

Conjugated polymers are another type of OSC, which, similar to small molecule

OSCs, use aliphatic side chains to increase solubility in organic solvents and organize the

polymer chains by providing steric hindrance.[8] The conjugated regions where charge

transport occurs typically lie in the polymer backbone.

Three examples of semiconducting polymer are shown in Figure 5. Regioregular

poly(3-hexylthiophene) (rr-P3HT or P3HT) is a hole transporting polymer and light

absorbing layer used in OPV and OFET research. Poly(2-methoxy-5-(2-ethylhexyloxy)-1,4-

phenylenevinylene), or MEH-PPV, is used as the emissive layer in OLEDs. MEH-PPV is

based on the first electroluminescent polymer studied, poly(p-phenylenevinylene) (PPV).

The methoxy and ethylhexyloxy side chains significantly increase the solubility of the

backbone PPV. Poly(9,9'-dioctylfluorene), or PFO, is also an OLED emissive layer, which

additionally finds use in processing carbon nanotubes. The length and orientation of its side

chains, along with the rigidity of its backbone, allows its use in sorting semiconducting

chiralities of carbon nanotubes from metallic chiralities, while maintaining the electronic

properties of the carbon nanotubes.[15,16] The side chains of PFO and its derivatives wrap

around specific chiralities, rendering them soluble, as non-wrapped nanotubes precipitate.
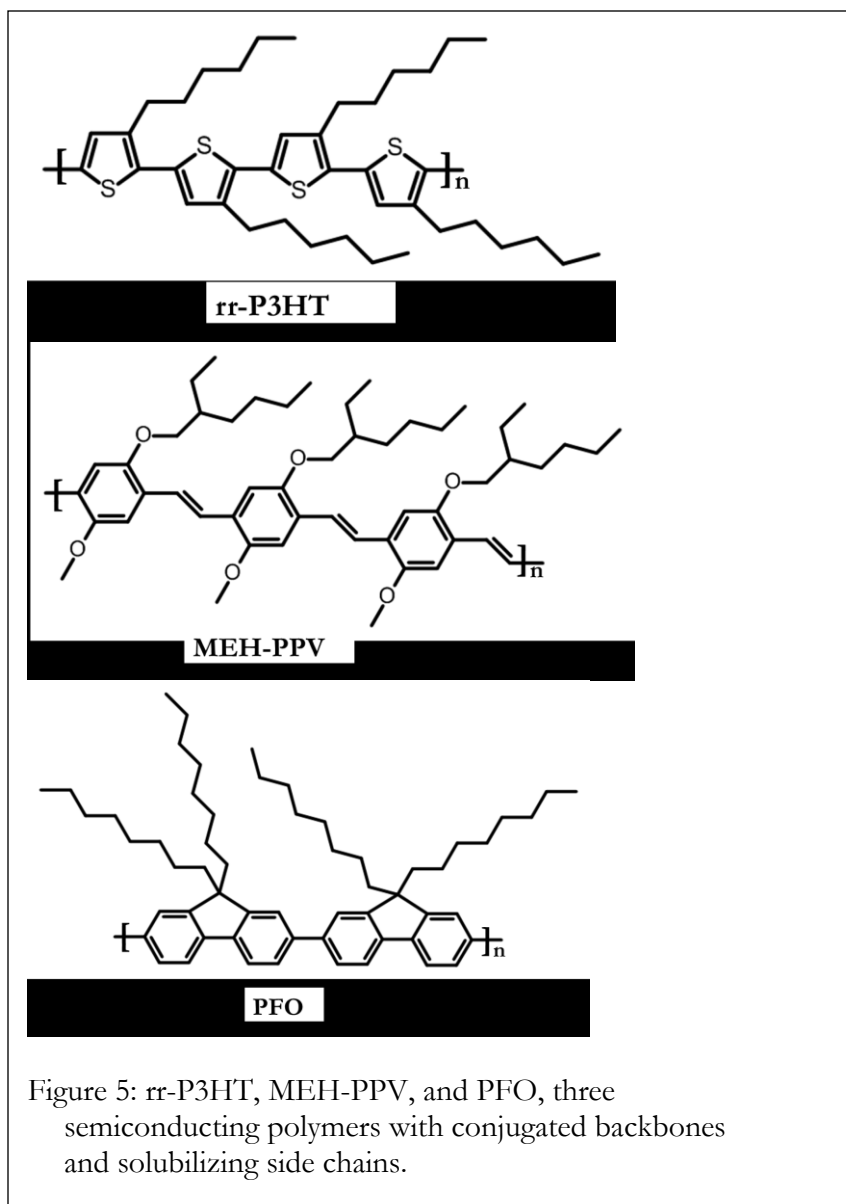
Figure 5: rr-P3HT, MEH-PPV, and PFO, three semiconducting polymers with conjugated backbones and solubilizing side chains.

2.3   Charge transport mechanism

Unlike inorganic semiconductors, charge transport in OSCs does not occur in continuous bands, but between discrete molecular orbitals. The efficacy of charge transport depends on the degree of delocalization of the orbitals, which affect both inter- and intra-molecular charge transport. Bonding in conjugated molecules results in delocalization of π and π^* orbitals over the length of the conjugation, which stabilizes induced free carriers

(electrons or holes). Conjugated orbitals have increased degeneracy, which stabilizes the free carrier within the molecule by sharing it between many equivalent states. This makes oxidation or reduction of the molecule more favored than it would be in an unconjugated molecule.

To illustrate, in the molecular orbital energy diagram of the small conjugated molecule butadiene there are four molecular orbitals derived from linear combinations of the four carbon p_z atomic orbitals (Figure 6). One electron is provided by each p_z orbital, so in the lowest energy configuration, two of the four orbitals are filled and two are empty. While butadiene is not a semiconductor, it serves to illustrate the principle of delocalization. If an electron were added to a butadiene molecule's LUMO, it would be stabilized by delocalization over two atoms. If an electron were removed from the HOMO, a hole would be delocalized over two atoms. Increased delocalization length leads to increased stability.
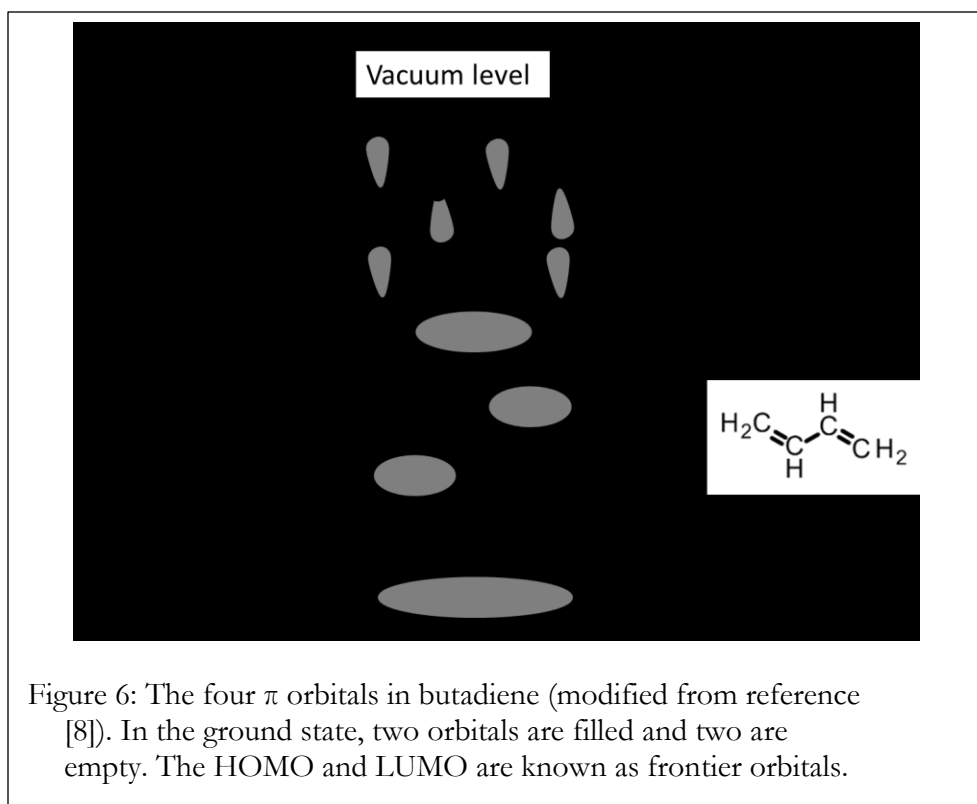
Figure 6: The four π orbitals in butadiene (modified from reference
[8]). In the ground state, two orbitals are filled and two are
empty. The HOMO and LUMO are known as frontier orbitals.

The degree of delocalization also affects intermolecular transport. There is reduced intermolecular delocalization of free carriers compared to crystalline semiconductors, so band transport does not occur. Transport between molecules is limited to statistically driven hopping which is favored by stronger intermolecular interactions.[8] Interactions between molecules are limited to van der Waals forces, meaning the energy levels of adjacent molecules overlap only to the degree that the orbitals are diffuse and polarizable.

In OSCs, a hole can be injected into the HOMO or an electron can be injected into the LUMO. The energy levels of the OSC determine whether oxidation or reduction is more favored, and so dictate if the material is electron- or hole-transporting. Electron transporting OSCs are also referred to as n-channel or acceptor OSCs, while hole-transporting OSCs are also referred to as p-channel or donor OSCs. OSCs that transport both electrons and holes are called ambipolar. Together, the HOMO and LUMO are referred to as the frontier orbitals, where most charge transport takes place. The energy to add an electron to the OSC is defined as the electron affinity (EA), and is frequently approximated as the LUMO. The energy to remove an electron is defined as the ionization energy (IE), and is approximated as the HOMO.

One caveat to this convenient visual of the HOMO and LUMO is that atomic and molecular orbital characteristics can only be calculated for occupancy by one electron, meaning the orbital energies determined for the molecular orbitals by calculation are not describing the same electron energy levels as the experimentally determined IE and EA. The energies represented by the HOMO and LUMO do not take into account electron-electron effects like Coulombic interactions or spin exchange energies, which are highly relevant in

OSCs due to their low ε_R.[8] Despite this, the molecular orbital picture remains a useful tool to conceptualize carrier transport in OSCs.

2.4   OSC/electrode potential matching

OSC performance is affected by the work function of the electrode used in conjunction with it. By carefully selecting the electrode metal, it is possible to decrease the barrier to charge injection. Generally, lower work function metals like aluminum work best with n-channel OSCs, while higher work function metals like gold are more compatible with p-channel OSCs. Figure 7 shows a schematic of hole injection from a gold electrode into the pentacene HOMO, or equivalently, the injection of an electron from the pentacene HOMO into the electrode. By comparing this to hole injection from aluminum, a metal with a smaller work function than gold, it is clear that the former case is more favorable.

Figure 7: Hole injection barriers from Au and Al into the HOMO of pentacene. The higher work function of Au more closely matches the HOMO of pentacene, reducing the barrier to hole injection into pentacene.
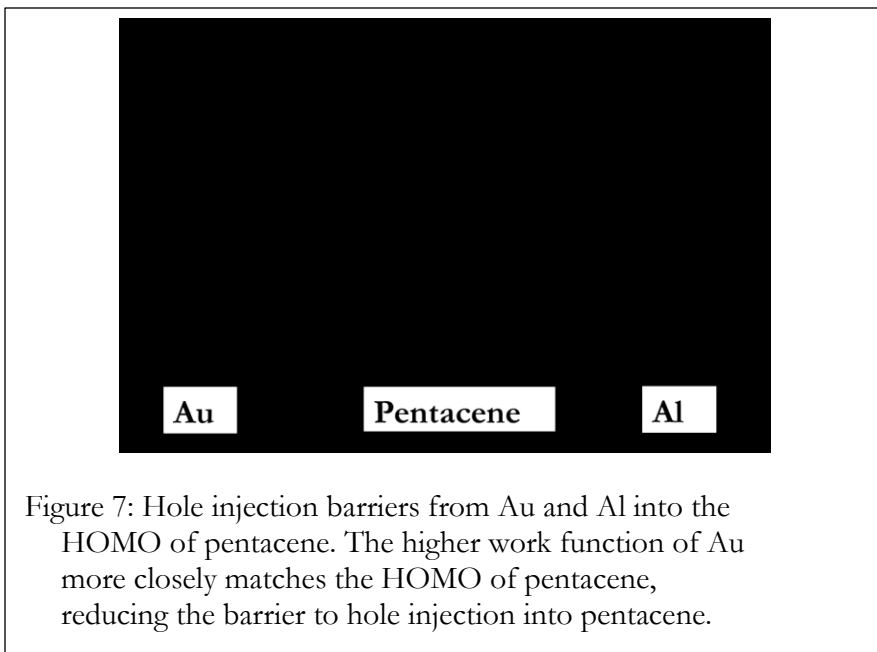
In electron transporting materials such as PCBM, electrons must be injected into the LUMO, so low work function metals have a smaller barrier, as seen in Figure 8. Notice that

because charges are also being extracted from the OSC into the metal, there will always be a barrier to charge transfer in one of the two directions, so it is important to select electrode materials that have a work function as close to the HOMO or LUMO as possible, in order to prevent unnecessary losses in performance.

Figure 8: Electron injection barriers from Au and Al into the LUMO of PCBM. The low work function of Al makes it favorable for use in conjunction with PCBM.
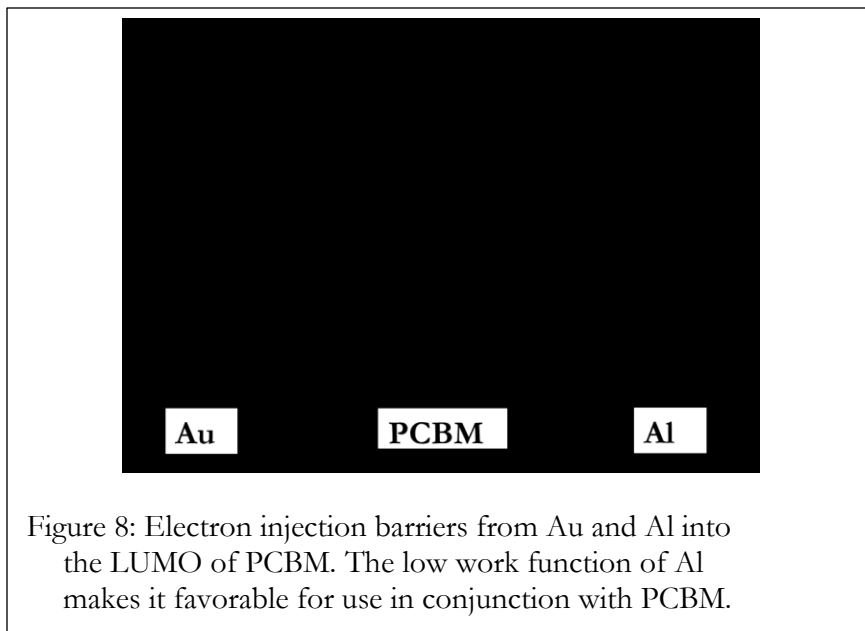
2.5   Thin film processing for organic electronics

OSCs and other materials used in organic electronics are deposited either by solution processing or physical vapor deposition (PVD). PVD is used with molecular OSCs such as pentacene, as well as electrode materials such as gold, chromium, silver, and aluminum. In PVD of pentacene, the chamber containing the substrate on which pentacene is to be deposited, as well as the source crucible with ~20 mg of pentacene, is evacuated to a level of 4E-6 Torr. Current is run through the tungsten coil surrounding the alumina source, resistively heating the crucible until the van der Waals forces holding the pentacene molecules together break, and the pentacene begins to sublime. The deposition rate is determined from a quartz crystal microbalance (QCM) thickness monitor, which measures

13

the rate of mass increase. This is combined with the density of the material deposited and the exposed area of the microbalance to get the rate of deposition in nm or Å/second. As shown in Figure 9, the QCM is in a different part of the vapor cone compared to the substrate. A 'tooling factor' must be set to account for the different vapor densities in the different regions of the cone, in order to get a reliable thickness measurement.

Figure 9: A thermal physical vapor deposition chamber. After the chamber is at a sufficiently low pressure, current is passed through the crucible holder which leads to evaporation or sublimation of the material in the crucible.
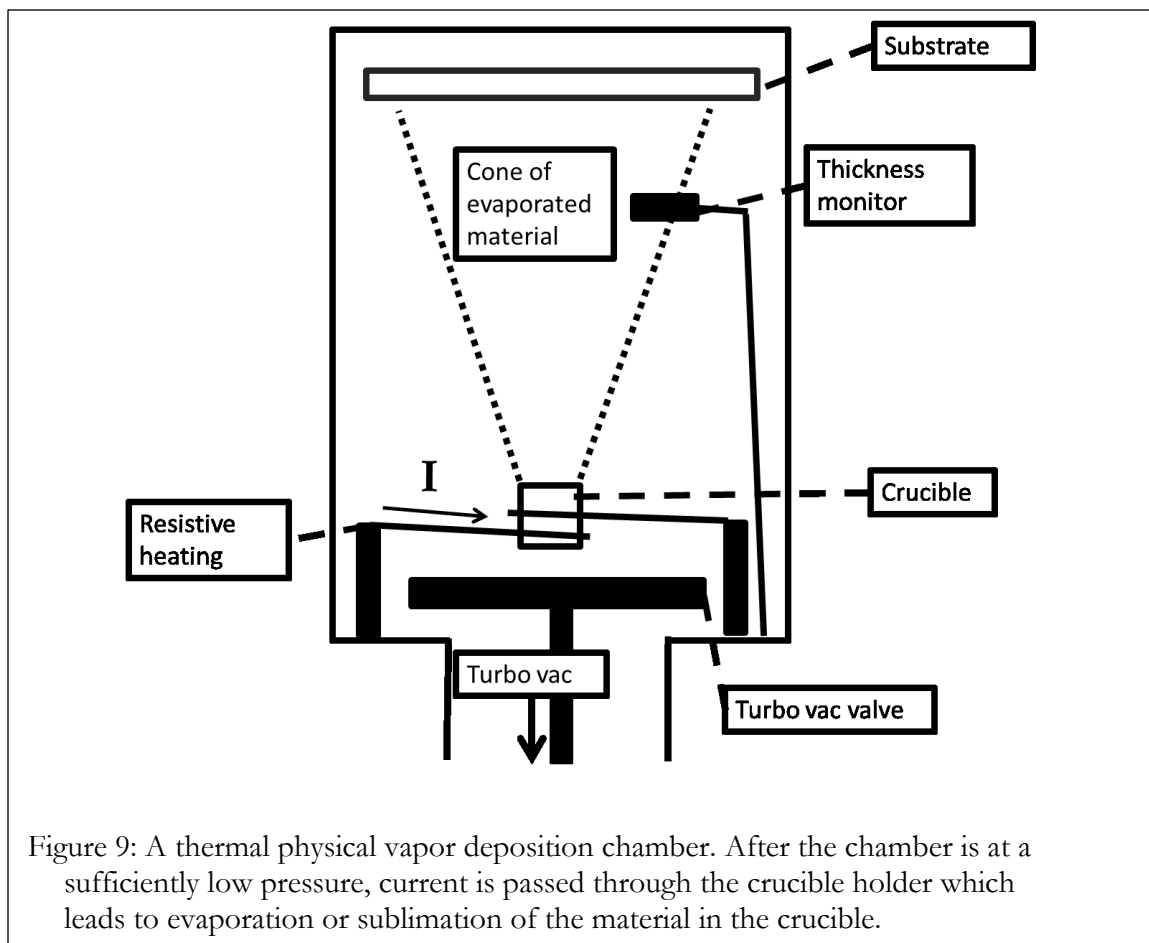
Once the rate of pentacene evaporation is steady (rates around 0.3Å/second work well for organic materials), the shutter covering the substrate is opened. As the vapor hits the substrate, the molecules in the vapor cool and form a polycrystalline film on the substrate. In an OFET the bulk of carrier transmission occurs in the first few layers of the OSC film, and good electronic results are obtained from OFETs with pentacene films 15-50 nm thick.

14

To determine what ideal film would look like, the potential energy of van der Waals interactions, PE_{VdW}, between two molecules can be modeled in terms of the polarizability α and inter-molecular distance r as: $PE_{VdW} \propto \frac{\alpha^2}{r^6}$. The interaction between adjacent molecules is proportional to the square of the polarizability of the orbitals, and inversely proportional to the sixth power of the distance between the molecules, meaning the interaction drops off quickly as distance increases. Hence, tightly packed crystals will have improved charge transport compared to amorphous materials with significant free volume, because the former has a lower barrier to intermolecular hopping.[8]

Various methods are used to improve the packing of small molecules deposited from vapor. The simplest one is to use a slow deposition rate, which allows molecules time to rearrange on the substrate before being locked in place by overlying molecules. The substrate may also be heated during deposition. This provides additional thermal energy to the pentacene molecules as they hit the substrate, allowing rearrangement and improved crystallinity of the film.

Two solution deposition techniques among the many used to deposit organic thin films are spin coating and doctor blading. In spin coating, a soluble material, such P3HT, is dissolved in chlorobenzene or another appropriate solvent with a typical concentration of 4-10 mg/mL. The solution is filtered through a 0.2 or 0.45 μm pore size Teflon (PTFE) syringe filter into a second vial, to remove large aggregates or particles. The cleaned substrate to be spin coated on is blown with nitrogen to remove dust, and placed on the spin coater chuck. The vacuum line is turned on, holding the substrate on the chuck. The filtered P3HT solution is quickly pipetted onto the substrate to cover the surface, then rotation of the substrate is initiated. For highly viscous solutions, like CYTOP, PMMA e-beam lithography

resist or S-1813 photoresist, less solution is needed, so solution should be added to the center of the substrate so that 15-20% of the surface area is covered. In spin coating, the thickness of the film is controlled by changing the solution concentration and the rotation velocity. For more viscous solutions, longer spin times must be used as the solution will be more resistant to flattening, but for most solutions from chloroform, toluene, or chlorobenzene, 30-60 seconds is sufficient. Similar to heating the substrate during vapor deposition, the packing and/or crystallinity of spin cast solutions may be improved by thermal annealing following deposition. To anneal a spin cast P3HT film, the substrate is heated on a hot plate at 95-100°C for 10 minutes. This removes solvent and allows the polymer chains to densify so the molecules are in closer proximity to each other. In polycrystalline materials, annealing will also increase the size of the crystals.

Doctor blading is accomplished by dropping a solution or suspension onto a heated substrate, then pulling the substrate under a blade of fixed height to spread the solution to a uniform thickness, and remove excess, as in Figure 10. Like in the case of spin coating, the sample may then be annealed to drive off remaining solvent and improve packing. Unlike spin coating, doctor blading is a scalable deposition technique that can be used for fabrication of large area samples along with processing techniques such as roll-to-roll printing.

Figure 10: A film being deposited by doctor blade.
Solution is added to the substrate, and the blade is
pulled across the surface at a constant vertical
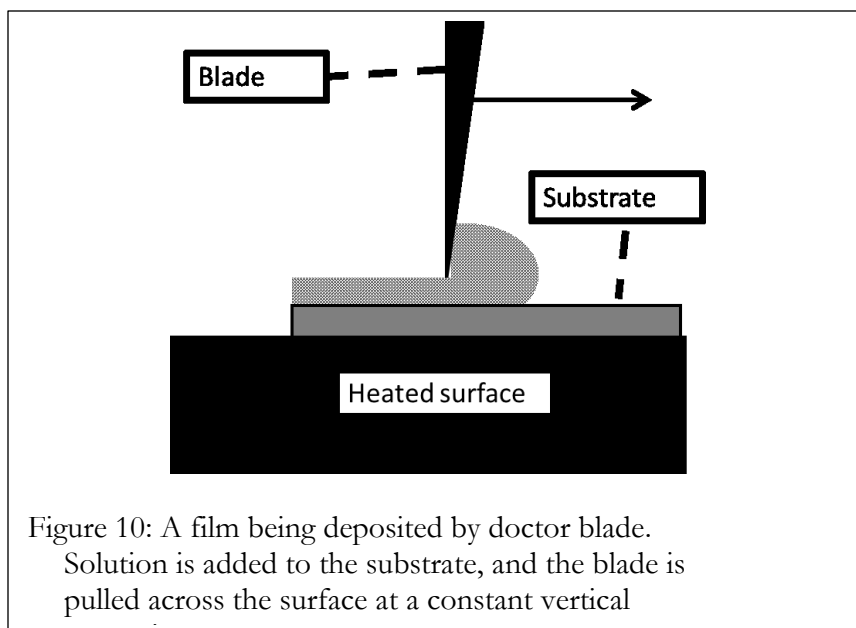
While the benefit of soluble polymer or small molecule OSCs is that they can be

solution processed, which allows for large scale deposition by methods such as roll-to-roll

printing, stamp printing, ink-jet printing, and dip coating, depositing one material over

another using solution processing presents challenges. Solvents used in the upper layers can

act to damage or swell underlying layers, affecting the final device performance. This is

addressed from two directions—using orthogonal solvents so the solvent of the top layer is

not a solvent for the bottom layer as in references [17,18], or rendering the bottom layer

insoluble, e.g. by crosslinking it, before deposition of the top layer.

3   Organic electronic devices: application of OSCs

3.1   Organic photovoltaics (OPVs)

A single junction OPV is composed of two semiconducting materials—a hole

transporting donor and an electron transporting acceptor. Light absorption can occur in

either material, but predominantly is seen to occur in the donor. The photon can have the

17

precise energy of the donor band gap, or can have a higher energy, in which case the electron will be excited to states above the LUMO, with extra energy mainly dissipated thermally. P3HT, a highly studied OPV donor polymer, absorbs significantly between about 500 and 600 nm, and has a maximum absorbance at around 550 nm. After a photon is absorbed by the donor molecule, an electron/hole pair is formed by excitation of an electron from the HOMO to the LUMO. The electron/hole pair, linked by a 0.2-1.5 V Coulombic attraction, must separate into free carriers at a donor-acceptor junction. The diffusion length of the exciton is approximately 10 nm, so to assure that excitons can be easily separated, the interface cannot be more than 10 nm away. This theory has made bulk heterojunctions, where the donor and acceptor are blended and deposited as one phase-separated film, a popular structure. On the other hand Ayzner et al., show that the exciton diffusion length is not the limiting factor in OPV efficiency.[18] Efficiencies comparable to BHJ efficiencies were found in devices with donor layers over 100 nm thick, when the time the hole and electron travel through the donor and acceptor were equal, rather than the thickness of the donor being minimized. It was hypothesized that limiting the efficiency of these devices was electron transport through the acceptor, not exciton transport through the donor.

After diffusion to a junction, the exciton is separated into a free electron and hole. Separation of the electron/hole pair is thought to occur by Brownian motion of the carriers while they remain inside the Coulombic radius (Onsager-type carrier generation[19]), which would be statistically driven towards splitting by the larger electron affinity of the acceptor compared to the donor. (Figure 11) It is hypothesized that the difference between the ionization potential of the excited donor molecule and the acceptor LUMO must be greater than the Coulombic binding energy for the exciton to separate into free carriers.[20] After an

18

exciton is split, Langevin recombination can occur, where free carriers near the interface move via Brownian motion until they enter the Coulombic radius and recombine. Recombination can also occur at the charge transfer state at the interface, which is at lower energy than either donor or acceptor LUMO.[19] If these recombination paths are avoided, the high mobility of the electron in the acceptor material and the hole in the donor material, as well as distinct work functions of the two electrodes, facilitate transport of the free charge carriers to electrodes for collection. Multi-junction OPVs combine multiple OSCs to absorb a broader range of wavelengths and give greater efficiencies for the same illumination.
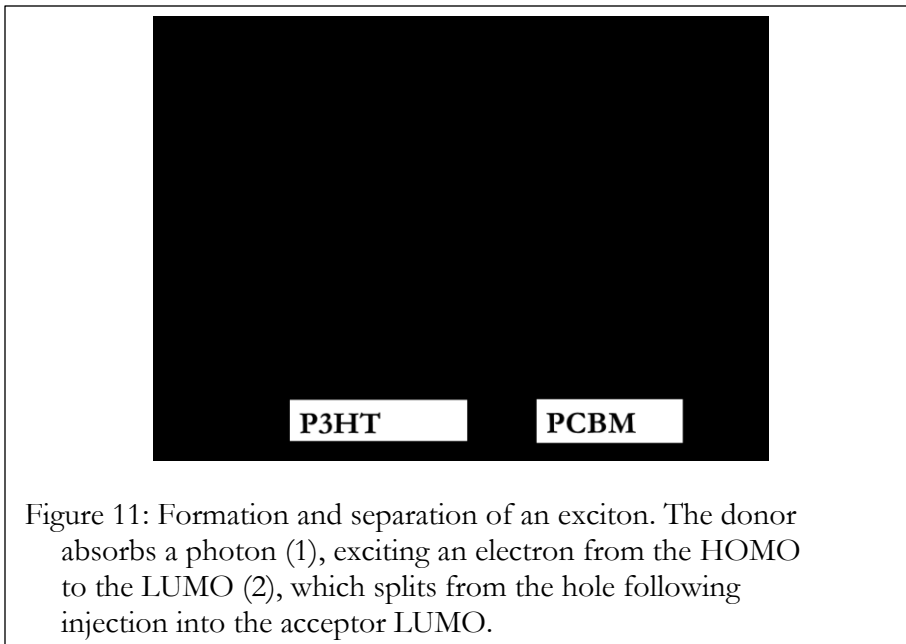
Figure 11: Formation and separation of an exciton. The donor absorbs a photon (1), exciting an electron from the HOMO to the LUMO (2), which splits from the hole following injection into the acceptor LUMO.

To measure the quality and efficiency of a solar cell, it is analyzed as a diode while under illumination. A voltage is applied across the electrodes while it is under illumination, and the photocurrent output is measured. See Figure 12 for a characteristic image of this, taken from reference [6].

Figure 12: a) I/V characteristics of showing V_{oc} and I_{sc} points at the x and y intercepts and b) EQE as a function of illumination wavelength of a tandem polymer OPV from reference [6]. Its efficiency remains the same across a range of wavelengths.
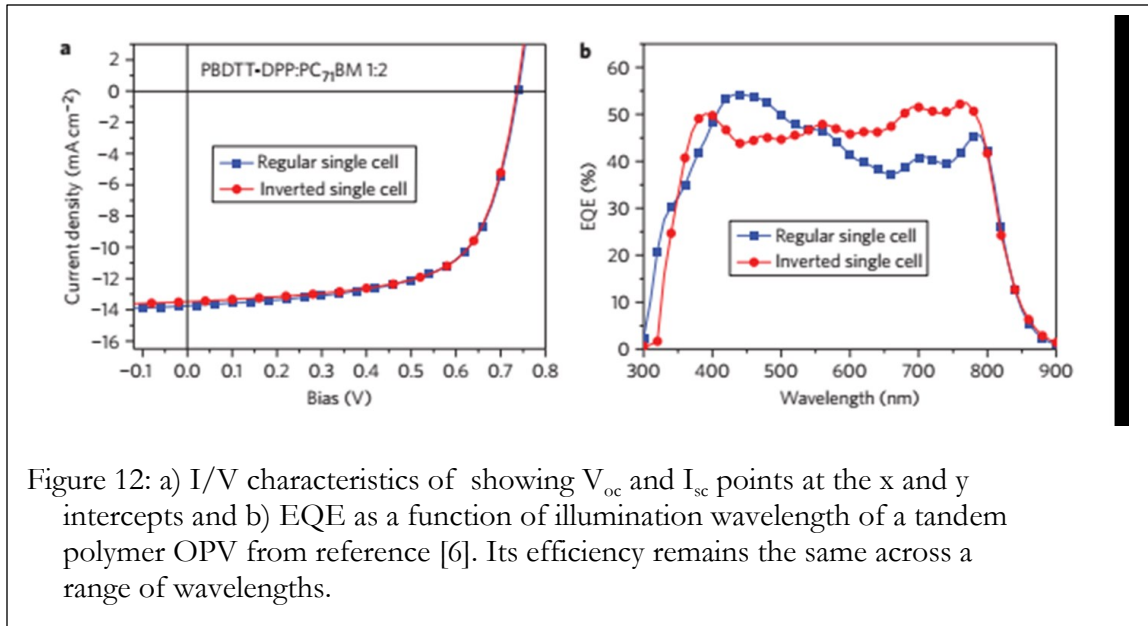
There are three important values in this plot: At zero current, the voltage is the open circuit voltage, or V_{oc}, which represents the voltage that is built up when no current is flowing. V_{oc} for inorganic p-n junction photovoltaics is determined by the work function offset between the two electrodes (typically ITO and aluminum),[21] but the open circuit voltage of OPVs is determined by the exciton binding energy, the exciton separation efficiency, and the HOMO/LUMO offset of the donor and acceptor.[22] A donor with a lower HOMO or an acceptor with a higher LUMO can increase the V_{oc}, but this must be balanced against the energy of absorbed light and the favorability of electron injection into the acceptor.

The second important point on the curve is the short circuit current, or I_{sc}, which is the current measured at zero voltage. The power P generated in the cell is P = I * V, so no power is generated at either I_{sc} or V_{oc}. However, they are useful values for calculating the quality of the OPV. The third point on the curve is the maximum power point, P_{max}, where the product of the current and the voltage is at a maximum. By comparing the maximum

20

power point to I_{sc} and V_{oc}, the ideality, or fill factor (FF) can be determined. The FF

determines what fraction of the theoretical maximum power is produced by the cell at P_{max},

and is calculated in Equation 1:

Equation 1

$$FF = \frac{I_{max}V_{max}}{I_{sc}V_{oc}}$$

Besides the FF, a commonly reported value to compare solar cells to each other is

the power conversion efficiency, (PCE). PCE relates P_{max} to the incident power from

illumination:

Equation 2

$$PCE = \frac{I_{max}V_{max}}{P_{incident}}$$

Internal quantum efficiency (IQE) and external quantum efficiency (EQE) are

sometimes also reported, and are measures of the proportion of charge carriers collected at

the electrodes given the number of incident photons (EQE) or given the number of

absorbed photons (IQE). IQE and EQE can vary with the wavelength of the absorbed light,

and it is ideal if they are relatively constant over a broad band of wavelengths. For instance,

in Figure 12b, the EQE of the two junction cell is around 45% between 400 and 800 nm

wavelengths.

3.2   Organic field effect transistors (OFETs)

OFETs are thin film transistors that operate in accumulation mode. When an OFET

is turned on by biasing the gate dielectric and the source/drain electrode pair, free carriers

flow across the OSC channel from the source to the drain. Figure 13 shows the structure

and operation of a p-channel OFET. The following discussion may be applied to n-channel

OFETs by substituting positive gate and drain voltages for negative, and electrons for holes.

The channel, through which carriers are transported, is a region at the

OSC/dielectric interface with length and width established by the electrode dimensions. To

turn on a p-channel OFET, the source electrode is grounded, and a negative voltage is

applied to the drain and gate electrodes. Holes from the source electrode are pulled into the

channel and flow from source to drain, where the output current I_d is measured.

The dielectric charge induced in the gate dielectric by the gate voltage controls the

number of carriers in the channel. As the gate voltage is increased from zero, the first

induced carriers in the channel are trapped by the OSC or the OSC/dielectric interface. To

create *mobile* carriers in the channel, a gate voltage (V_g) above the threshold voltage (V_{th})

must be applied.

Figure 13: Structure and operation of a p-channel OFET. I_d is turned on
by a negative source/drain voltage and a negative gate voltage.
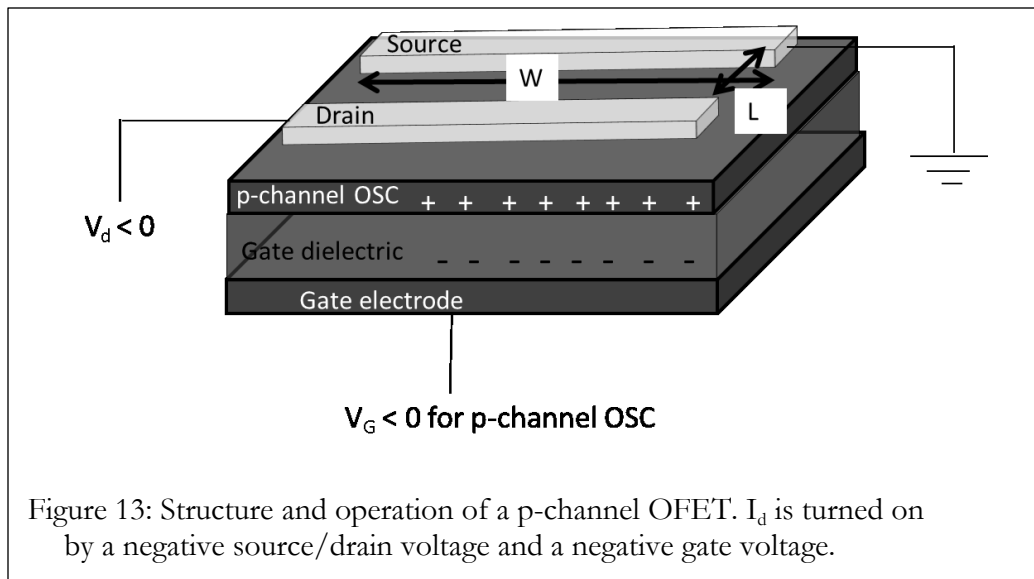
The measured I_d depends on the number of mobile carriers, Q_{mob}, in the channel,

calculated as for a parallel plate capacitor using the dielectric capacitance Ci, the gate voltage

V_g, the threshold voltage V_{th} and the drain voltage V_d. For small values of V_d (the linear

22

regime), Q_{mob} decreases linearly along the length of the channel from a maximum value of

$Q_{mob} = Ci(V_g - V_{th})$ at the source to $Q_{mob} = Ci(V_g - V_{th} - V_d)$ at the drain. For larger values

of drain voltage, the free carriers induced at the drain voltage decrease, until when

$V_d = V_g$ - V_{th}, $Q_{mob} = 0$ at the drain electrode (the 'pinch off point'). For $V_d > V_g - V_{th}$, the

saturation regime, the pinch off point moves through the channel towards the source.

Though there are no free carriers induced in the channel near the drain at this point, current

still flows because the electric field between source and drain sweeps carriers through.

The drain voltage depends on the number of mobile carriers, Q_{mob}, the field effect

mobility μ_{FE}, the width of the channel W, and Faraday's constant: $I_d = W \cdot Q_{mob} \cdot \mu_{FE} \cdot F$. In the

saturation regime, using the above expression for Q_{mob}, this is evaluated to get Equation 3.[8]

W and L are the channel dimensions, Ci is the capacitance of the dielectric in nF/cm^2, μ_{sat} is

the saturation field effect mobility in cm^2/V·s , and V_{th} is the threshold voltage in V.

$$I_{D,\,sat} = \frac{W}{2L} C_i * \mu_{sat} * \left(V_g - V_{th}\right)^2$$

Equation 3

There are two types of data that are collected from electrical measurements on an

OFET. First the output curve results when, for a series of gate voltages, drain voltage is

scanned and drain current is measured. By plotting drain current vs. drain voltage for each

gate voltage, (Figure 14) the linear regime and the saturation regime are clear. In the linear

regime, the drain current increases linearly with increasing drain voltage. In the saturation

regime, the drain current does not depend on the drain voltage, so the curve flattens out.

Figure 14: Output characteristics of a p-channel OFET.
For each gate voltage, with increasing drain voltage the
drain current increases, then saturates.
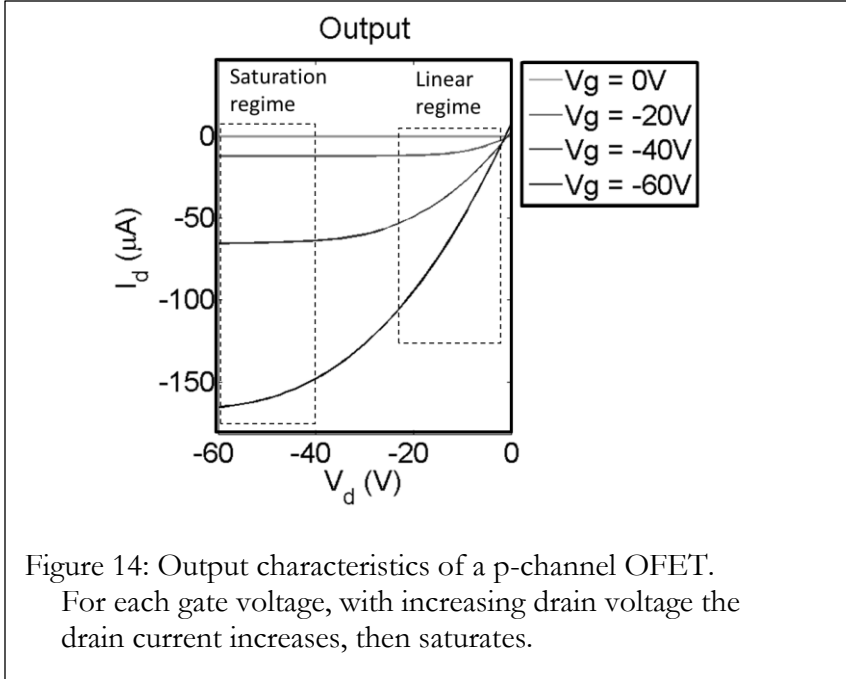
The second type of data collected from an OFET is the transfer curve, where I_d is

measured as V_g is swept while V_d is held at a value in the saturation regime. To get the

transfer curve for the device with the output curve shown in Figure 14, V_d was held at -60V,

and V_g was swept from 0V to -60V. The transfer curve is shown in Figure 15.

Figure 15: Transfer curve of a p-channel
OFET. V_d is held at -60V, and V_g is
swept from 0V to -60V.
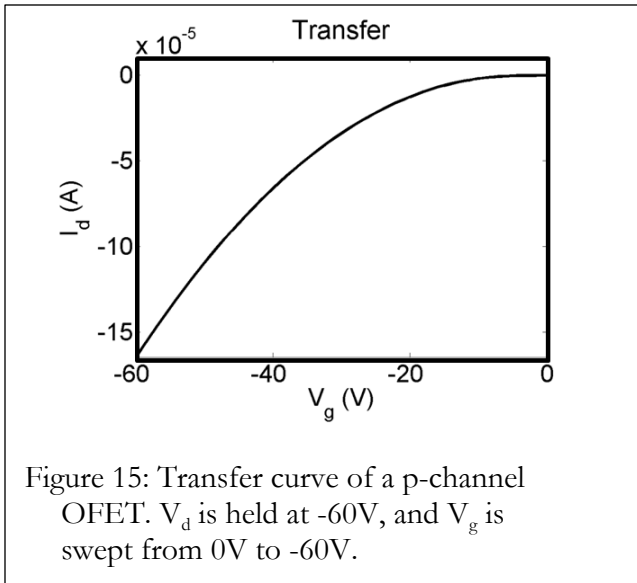
When analyzing transfer data of an OFET, two modifications of the transfer curve are commonly used. The square root or logarithm of I_d may be plotted against Vg, shown in Figure 16a and Figure 16b for the transfer curve in Figure 15.
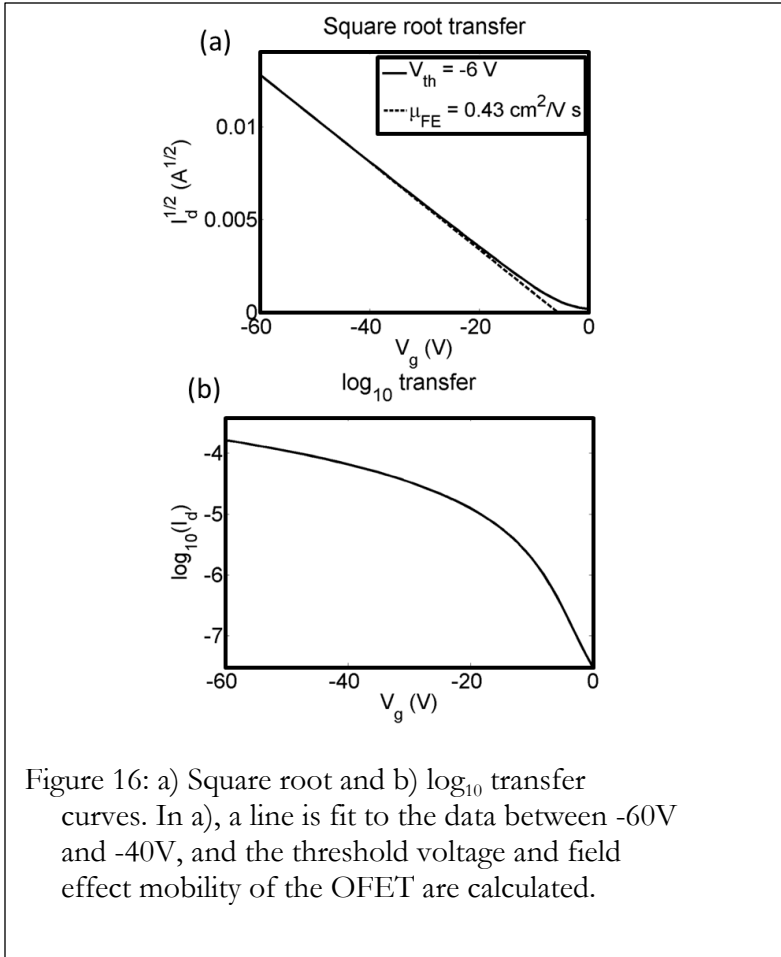
Figure 16: a) Square root and b) $\log_{10}$ transfer curves. In a), a line is fit to the data between -60V and -40V, and the threshold voltage and field effect mobility of the OFET are calculated.

3.2.1 Threshold voltage and field effect mobility

Threshold voltage is a measure of the gate voltage is required to turn the OFET on, while field effect mobility is a measure of how facile carrier transport is in the channel while the OFET is on. There are several literature methods of extracting V_{th}, with one of the main ones being to find the x-intercept of a straight line fit to the linear portion of the square root

transfer curve (see Figure 16a).[23] To see this, the square root of the saturation drain current equation is taken to get:

$$\sqrt{I_{D,\,sat}} = \sqrt{\frac{W}{2L} C_i * \mu_{sat}} * (V_g - V_{th})$$

Equation 4

This can be simplified to find V_{th} by solving for $V_g - V_{th}$ and setting $I_{d,sat} = 0$:

$$\frac{\sqrt{I_{D,\,sat}}}{\sqrt{\frac{W}{2L} C_i * \mu_{sat}}} = V_g - V_{th}$$

Equation 5

To calculate the field effect mobility, Equation 4 is solved for μ_{sat} in terms of the slope of the fitted line, the channel dimensions W and L, and the capacitance of the dielectric:

$$slope = \sqrt{\frac{W}{2L} C_i * \mu_{sat}}$$

Equation 6

$$\mu_{sat} = \frac{(slope)^2 * 2L}{W * C_i}$$

Equation 7

26

In fully crystalline materials, field effect hole mobilities have been found up to 50 cm^2/V s.[8] However, common hole mobilities for polycrystalline or amorphous OSCs are typically below 1 cm^2/V s, and electron mobilities for n-channel OSCs are typically still lower. Improved OSC packing and synthesis of OSCs with increased delocalization gives improved mobility by allowing greater overlap between neighboring orbitals. Another method of increasing mobility is to treat the substrate with a self-assembled monolayer (SAM). A SAM eliminates traps at the substrate/OSC interface, which would otherwise trap free carriers as they are transported through the OSC. In addition to this, the SAM has been seen to improve packing of the small molecule as it is deposited.[24]

Another factor that can be modified to affect the mobility is the dielectric constant of the substrate. The permittivity of the insulating substrate (frequently the gate dielectric of an OFET) has been seen to decrease the free carrier mobilities of adjacent OSCs. Hulea, et al., show that the decreased field effect mobility can originate from the increased formation of polarons that act to screen free carriers at interfaces with higher dielectric constant insulators.[25] Richards, et al., agree that the dielectric constant of an insulator next to an OSC decreases the field effect mobility of the OSC, but argue that the cause can be differing amounts of static dipolar disorder.[26,27] An insulator with a larger dielectric constant has more randomly oriented static dipoles, or static dipolar disorder, than an insulator with a smaller dielectric constant. The density of states (DOS) of the first 0.5-1.0 nm of OSC at the dielectric interface is broadened by the presence of randomly oriented strong dipoles in the high-k dielectric. The broadened DOS decreases the favorability of charge carrier hopping and thereby reduces the mobility.[26,27]

3.2.2　Bias stress

Stability is an important consideration in OFETs. Many are susceptible to bias stress, which is seen both as a decreasing output current during prolonged operation and an increasing threshold voltage when the OFET is turned off and on again. Bias stress can be reliably quantified by the observed shift in V_{th}, as it has minimal effects that will not be captured by that shift.[28] Bias stress results from formation or filling of trap states at the dielectric/OSC interface, as the dielectric undergoes prolonged polarization. Trapped charges were observed with a surface potential measurement of a SiO_2 dielectric after a prolonged bias was applied, then the OSC was removed.[28] One approach for reducing bias stress is to use a fluorinated dielectric, which decreases the trap density at the interface.[29] However, the hydrophobicity of perfluorinated materials can alter the morphology of the OSC deposited on top, potentially unfavorably.

In addition to the unwanted instability caused by bias stress, memory devices are being researched that will store charges in a static fashion, altering the output current from one stable state to another. A charged memory device is reversibly written by application of a DC voltage to the gate for a specified time. Charge trapping or bulk polarization occurs in the gate dielectric, and following writing, the current output for a given voltage input to the device is increased, compared to the current prior to charging. Erasing is done by application of a voltage with the polarity reversed from that of the writing voltage.[30]

Charging the dielectric is also an approach that can be used to make devices that have low power requirements, or so they can operate without a continuously applied gate. A static field trapped in the dielectric increases the carrier density in the adjacent OSC so in an

unperturbed state the OSC is conductive, either decreasing the threshold voltage to a smaller value, or forming an 'always on' OFET.

CHAPTER II: Interfacial Fields at Organic Donor-Acceptor Junctions

1 Introduction

In this chapter, the interfacial potential at two organic donor-acceptor junctions is measured using Scanning Kelvin Probe Microscopy. The bulk and interface contributions to the potential at one junction are isolated, and the effect of the insulating substrate used on the measured interfacial potential is determined.

1.1 Interfacial fields in organic electronics

The electrical potential profile of the interface between two organic semiconductors (OSCs)—a donor or hole-transporting material, and an acceptor or electron-transporting material—governs the workings of organic light emitting diodes (OLEDs) and organic photovoltaics (OPVs). In a donor-acceptor bilayer or bulk heterojunction (BHJ) OPV system, excitons—Coulombically bound electron-hole pairs—are generated in either the donor or acceptor by incident light. The excitons diffuse through the material to a donor-acceptor interface, where charge separation takes place. At the interface, electron injection from the excited molecule into the acceptor's LUMO is energetically favored if the electron affinity and the oxidation potential of the acceptor are larger. Following separation, the electron and hole must escape the existing Coulombic potential across the interface. This is thought to be accomplished via Brownian motion.[19,31,32] Brownian motion can also bring separated charges back within the Coulombic radius and cause Langevin recombination, reducing the efficiency of the OPV.[19] If the electron and hole escape from the interface successfully, they make their ways to electrodes for collection.

Throughout this process, the interfacial potential difference at the donor-acceptor junction contributes to the forces acting upon the electron and hole. For instance, a donor-acceptor pair with an interfacial potential difference favoring recombination will have higher rates of Langevin recombination, and lower quantum efficiency. Besides the effects of the field on free carriers, the interfacial potential difference also affects the energy levels of the HOMO and LUMO of the donor and acceptor. Unlike at inorganic p-n junctions, vacuum level alignment by carrier drift does not occur in organic donor-acceptor junctions.[33] Instead, the vacuum level of each component determines how the two band gaps align with each other. Vacuum level can be shifted by the interfacial potential difference.

The theoretical interfacial potential difference at inorganic p-n junctions is calculated using established methods.[34] Thermally generated free carriers flow from higher to lower electrochemical potential until the Fermi levels are aligned. Following this equilibration, a depletion region exists at the interface, which gives rise to current rectification, photocurrent, and contact resistance behavior.

OSCs should not be analyzed with this model primarily because they generally do not have large densities of free charge carriers at room temperature. Charge carriers in OSCs exist in high energy bonding and antibonding orbitals. These orbitals are stabilized through intramolecular orbital delocalization, but they are still typically completely filled or unoccupied, respectively, at room temperature and without external perturbation. Furthermore, OSC molecules generally interact with each other only via van der Waals forces, reducing the intermolecular delocalization of free charges. Taken together, these effects decrease the tendency of electrons and holes to transfer across interfaces. However, it

is known that OSCs do have regions of interfacial polarity akin to depletion regions at OSC/OSC interfaces. Present theories do not always allow for accurate prediction of the magnitude and direction of built-in potentials at donor-acceptor junctions, which is why more study of interfacial potential difference in OSCs is needed.

The unperturbed HOMO and LUMO and the density of states surrounding donor-acceptor junctions have been measured by cyclic voltammetry (CV),[35] ultraviolet photoelectron spectroscopy (UPS), and inverse photoelectron spectroscopy (IPES). [33,36–38] When studying the interfacial potential difference, the relative positions of OPV donor P3HT and OPV acceptor PCBM molecular orbitals—measured by UPS and IPES of bilayers—have been seen to depend on whether or not P3HT and PCBM are in contact. To explain this, vacuum level alignment at the donor-acceptor interface is dismissed in favor of an interfacial dipole.[33] Scanning Kelvin Probe Microscopy (SKPM) of a BHJ active layer[39–41] provides further direct evidence for a dipole at donor-acceptor interfaces.

There are multiple contributions to the interfacial potential difference at OSC-OSC junctions—molecular dipoles, trapped charges, and charge carrier transfer from OSC or impurity orbitals. It is difficult to separate out which contribution is most important in any given case, but significant progress has been made. It is known that the macroscopic dipole created by summing of molecular dipoles alters the favorability of charge transfer across an organic donor-acceptor interface at equilibrium.[38] Molecular dipoles contribute electrostatically to the interfacial potential difference without necessarily implying equilibrium charge carrier transfer.

That said, in the case of the donor polymer P3HT, Aarnio et al. have suggested a mechanism for charge transfer following thermal annealing.[19] Polymer chains move to

higher energy conformations during thermal annealing, and do not all return fully to their lowest energy conformation once cooled again. This introduces disorder into the chains, which reduces the effective distance over which the ground state wave function can extend, and increases its energy. The ionized state is then more energetically favorable relative to the ground state than it was before thermal annealing.[19] This can make equilibrium charge transfer more likely from an annealed donor polymer such as P3HT to an acceptor like PCBM.

1.2 Measuring surface potential with Scanning Kelvin Probe Microscopy

Scanning Kelvin Probe Microscopy (SKPM) is a scanning probe technique that provides a map of the electrostatic potential of the surface (surface potential) using a variant on the vibrating capacitor method of determining work functions.[2,39–43] It is not only applicable for work functions, however, and does not require a fully conductive sample to give reliable results.[2] In an OSC, SKPM measures the density of trapped and free charges in the film, superimposed upon the difference in bulk vacuum levels. A region of negative surface potential corresponds to a region with a positive vacuum level shift in a standard HOMO/LUMO energy diagram.

SKPM has been used to measure the surface potential of bulk heterojunctions (BHJ). In Figure 17, the surface potential of a MDMO-PPV/PCBM BHJ shows that the fullerene has a more negative potential than the polymer, which translates to a positive vacuum level shift.[41]
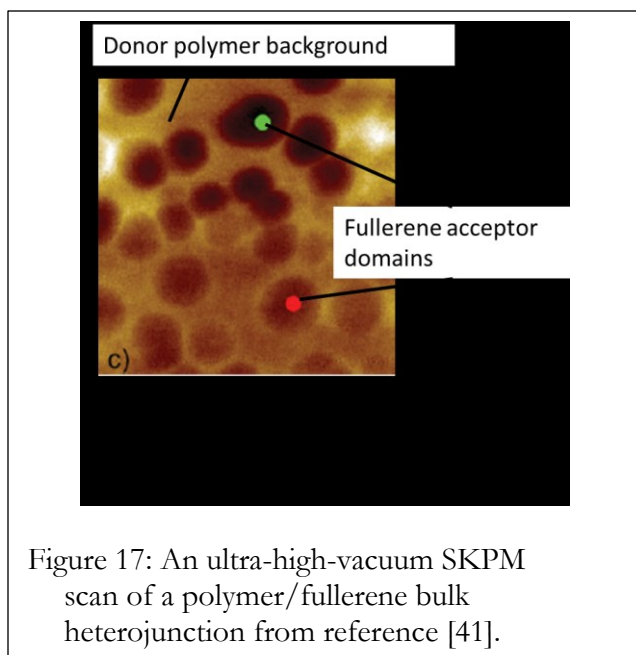
Figure 17: An ultra-high-vacuum SKPM
scan of a polymer/fullerene bulk
heterojunction from reference [41].

SKPM allows the potential at the interface to be observed without the risk of influencing the result by charging the sample, which can occur during photoelectron spectroscopy on OSCs. Measuring the surface potential occurs in two passes by the scanning probe tip. First, a standard tapping mode AFM scan is taken to measure the height of the surface. Then, the tip is raised by a set amount above the measured height, frequently around 100 nm, and it is rescanned across the surface it just covered. During the second scan, an AC voltage is applied to the tip as it is scanned across the electrostatic potential of the surface. Interactions with the potential induce vibrations in the cantilever, which are measured by a laser/photodiode combination and minimized by a compensating applied DC voltage. What is produced is a 2D map of the potentials at the surface, which originate from differences in work functions, trapped and free charge carriers, and externally applied voltages. In this chapter, SKPM is used to measure the potentials present at organic donor-acceptor junctions.

1.3   Materials

We used regioregular poly-(3-hexylthiophene) (P3HT) and semiconducting single walled carbon nanotubes (s-SWCNTs) for the donor. P3HT has good air stability and hole mobility, and is commonly studied as the donor material in organic photovoltaics. [20,44,45] s-SWCNTs are air stable and absorb in the IR, which tends to be an underutilized portion of the solar spectrum in OPVs.[*] S-SWCNTs also have excellent charge transport properties, and are relevant for all-carbon solar cells.[14,46–48] Michael Arnold and Meng-Yin Wu at University of Wisconsin, Madison isolated four s-SWCNT chiralities by exploiting the fact that 9,9-octyl polyfluorene (PFO), complexes with the (7,5), (7,6), (8,6), and (9,7) chiralities. By rinsing away the non-complexed metallic and semiconducting nanotubes, the desired chiralities, wrapped with PFO, are isolated.[49–51]

The acceptor material used in this work is the widely studied PCBM, which has characteristics that make it well suited for an electron acceptor, including favorable morphology, a high electron affinity, and two low-lying excited anionic states. [52,53] The low lying excited states increase the charge transfer rate from the donor, as the total rate is the sum of the charge transfer rate to the ground state and the excited states. In the present work, PCBM films were both solution- and vapor- deposited with similar interfacial potential observed from both methods. This shows that the results apply equally well to solution-deposited and vapor-deposited OPVs.

The two substrates used were 300 nm thick thermally grown SiO_2 on degenerately doped silicon, and 90 nm thick solution processed Al_2O_3 [54] on Corning glass.

---

[*] Most polymer donors absorb in the visible portions of the spectrum.

2   Methods

2.1   Lateral diode fabrication

Lateral devices have previously been used for observing the effect of an applied 'gate' voltage on the potentials and charge transport at the junction between P3HT and the n-channel small molecule naphthalene tetracarboxydiimide (NTCDI).[55] This work builds from that study, with more focus on the effects of contact between the donor and acceptor, and also on the effect of the substrate on the potential. Lateral devices have also been used to quantify charge trapping in lateral OFET materials following operation and intentional biasing.[56,57]

To fabricate lateral diodes, a fluoropolymer-based lithographic process was used.[55,56] Fluorinated and hydrogenated materials tend to be mutually insoluble, so by layering fluorinated and hydrogenated materials, each can be patterned independently. Two substrates—thermally grown SiO_2 on degenerately doped Si and solution processed Al_2O_3 on Corning glass—were used to distinguish the properties of the lateral junction from those of the substrate.

2.1.1   Substrate preparation

Silicon/silicon dioxide substrates were prepared by first dicing wafers into one inch squares, then cleaning them by submerging in a 3:1 solution of H_2SO_4:30%H_2O_2 for 30 minutes, followed by sonication for 15 minutes each in sequential baths of deionized (D.I.) water, acetone, and isopropanol. The diced wafers were then dried under a stream of nitrogen. Corning glass/aluminum oxide samples were prepared in the following way: Corning glass squares were cleaned by sonication in acetone and isopropanol then dried with a stream of nitrogen. Aluminum oxide was deposited using a sol-gel process that leads to a

polycrystalline film.[54] The precursor solution was made by dissolving 2.34 g. Al(NO$_3$)$_3$•9H$_2$O in 12.5 mL methoxyethanol, then adding 0.64 mL acetylacetone and stirring for six hours at room temperature. The solution was allowed to sit at room temperature for one day or more, and then filtered through a 0.45 μm PTFE syringe filter. It was deposited on the Corning glass by spin coating at 500 rpm for 6 seconds, then 3000 rpm for 30 seconds. The resulting film was annealed for 10 minutes on a 300°C hot plate, then a second layer was added in the same way. Lastly, the sample was placed in a 300°C furnace. The temperature was raised to 500°C, and the alumina was allowed to bake for 1 hour. Surfaces were passivated by OTS treatment at 25 cm Hg and 140°C for two hours.

On some SiO$_2$ samples, OTS treatment was done as above, or HMDS treatment was done under 25 cm Hg vacuum at 105°C for two hours. No difference was seen in the interface polarization of treated vs. non-treated samples.

2.1.2 Bottom contact electrode deposition

Bottom contact electrodes, which were used for the majority of the samples, were deposited by physical vapor deposition immediately following substrate preparation. For P3HT samples that were used in the statistical analysis, electrodes were deposited using photolithography and a lift-off method. First, S-1813 positive photoresist was deposited on the cleaned Si/SiO$_2$ wafers by spin coating at 2000 rpm for 60 seconds, then annealing at 95°C for 10 minutes. The photoresist was patterned with a mask with an electrode spacing of 40 μm, then 5 nm Cr and 45 nm Au were deposited at rates of 0.3 and 0.5 Å/second. The gold between the electrodes was removed by brief (~20 seconds) sonication in acetone. For the rest of the P3HT samples and all s-SWCNT samples, a shadow mask was used that gives an inter-electrode spacing of 250 μm. To deposit gold electrodes, a 5 nm Cr adhesion layer

was first deposited, followed by 45 nm Au. To deposit Al, 100 nm Al was deposited directly on the substrate at a high rate of 1 nm/second to prevent oxidation. Aluminum was found to give better electrical contact with the PCBM layer than gold because of closer energy alignment between the PCBM LUMO and the aluminum work function. No noticeable problems were encountered from the native aluminum oxide layer between the aluminum electrode and the overlying OSCs for these devices.

2.1.3 Donor film deposition

The donor material was deposited from solution by spin coating (P3HT) or doctor-blading (s-SWCNTs) on the cleaned substrates. P3HT films were deposited by spin coating one to three times at 2000 rpm for 60 seconds from 10 mg/mL P3HT solution in chlorobenzene, then annealing at 95°C for 10 minutes. Multiple spin coating steps were required to deposit a continuous film on top of the hydrophobic HMDS or OTS for treated substrates.

s-SWCNT films were deposited by Meng-Yin Wu in the laboratory of Michael Arnold at University of Wisconsin, Madison, using the procedure that Meng-Yin described as follows:[1]

"We adapt methods from Nish et al.[16] to prepare semiconducting single-walled carbon nanotubes. More details about preparation of semiconducting carbon nanotube solution can be found from our previous work.[47,58]

70mg of CNTs (SG65i, SouthWest NanoTechnologies) and 140mg of poly(9,9-dioctylfluorenyl-2,7-diyl) (PFO, American Dye Source) are added to 70ml of toluene. The mixed solution is ultrasonicated using a 0.5 inch horn tip ultrasonicator for 30 minutes at 40% max amplitude with a water bath. After sonication, the PFO-CNT slurry is

ultracentrifuged for 15 minutes at 300,000g. The unwanted CNT bundles, unselected CNT chiralities, and catalyst particles are all pelleted into bottom during the centrifugation. The top 90% of the resulting supernatant is carefully decanted and filtered through a 5.0 μm PVDF membrane filter. Toluene is selectively removed from the filtered PFO-CNT solution via vacuum distillation. The PFO-CNT mud is redissolved into hot tetrahydrofuran (THF). The resulting solution is centrifuged in a fixed-angle rotor (ThermoFisher Fiberlite) at 50,000g at 4 °C for 24 hours. CNTs are selectively sedimented from the PFO-rich THF solution after centrifugation. We discard the top PFO-rich THF solution and redisperse the CNT-rich pellet in THF again. The PFO-removal process is repeated for at least three times. The pellet is finally redispersed in chlorobenzene. We take the optical absorption from the final CNT solution to calculate the PFO:CNT weight ratio by using calibration standards for the optical cross section of PFO and optical cross sections of CNT first transition bandgap (S1) as reported by Hertel et al.[59] A CNT solution with PFO:CNT weight ratio less than 2:1 is used to cast a CNT film. The CNT solution is briefly dispersed using microtip ultrasonication for 10 seconds at 10% max amplitude before casting a film. We doctor-blade the CNT solution on top of the prepared Si/SiO_2 and $Glass/Al_2O_3$ substrates in glovebox on a hot plate at 100 °C and 110 °C, respectively. The cast CNT films are annealed at 150 °C in glovebox for 10 min to remove residual solvent."

2.1.4   Lithographic patterning of the donor film

A 1 μm thick film of the fluorinated polymer CYTOP (Bellex International) was deposited over the P3HT or s-SWCNT film by spin coating at 2000 rpm for 240 seconds, followed by annealing at 95°C for 10 minutes. The positive photoresist S-1813 was then spin coated over the CYTOP. Several methods were used to spin coat the photoresist despite the

hydrophobicity of the CYTOP. Initially, the CYTOP was briefly etched with oxygen plasma for 5 seconds or less to make the surface rougher. However, this method was challenging to control, as over-etching the CYTOP by a small amount resulted in failure of the lithography process. The second method was to leave the S-1813 on the surface of the CYTOP before beginning spin coating. The photoresist was added to cover the entire surface, then after 1-2 minutes, spin coating was begun. S-1813 was spin coated at 3000 rpm for 1 minute, followed by annealing for 10 minutes at 95°C.

The S-1813 was patterned using a UV mask aligner to place the interface. For P3HT devices used in the statistical analysis, half of them had interfaces placed one third and two thirds of the way between the electrodes. For the rest of the devices with bottom contact electrodes, the interface was half way between the electrodes, and for devices with top contact electrodes the interface was placed around the middle of the wafer. Samples were exposed to 100 J/cm^2 of UV light over several seconds (using the constant energy mode), developed in CD-26 for 40 seconds, then rinsed with deionized water and dried with nitrogen. The wafer was exposed to O_2/O_3 plasma at 200 W for 3 minutes. The power and time used were calibrated to work best for this purpose. Figure 18 shows the lithographic patterning steps described above.

Figure 18: Oxygen plasma was used to etch CYTOP and P3HT films away. PCBM deposition followed by CYTOP removal exposed the P3HT/PCBM interface.
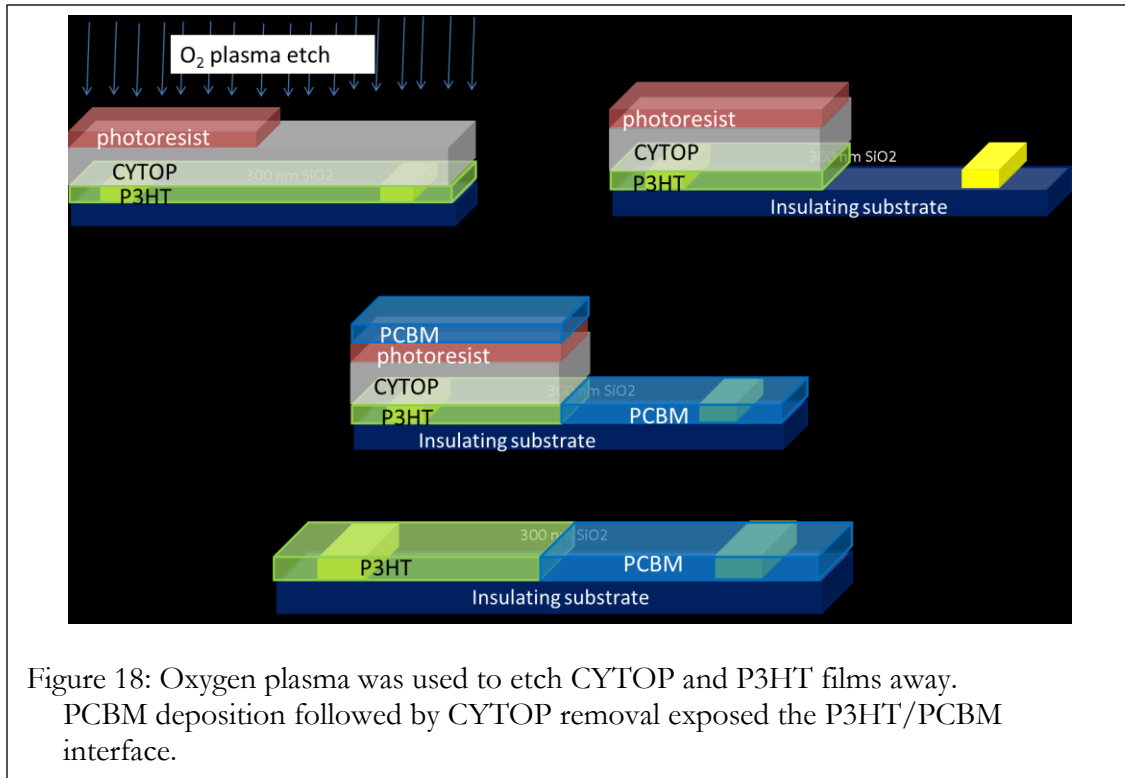
2.1.5 PCBM deposition

PCBM was deposited by spin coating or vapor deposition. No difference was seen in the interfacial potential of samples where PCBM was deposited from solution compared to vapor, as discussed further in Chapter II, Section 4.1. Solution processed PCBM films were made by spin coating from a 10 or 20 mg/mL solution in toluene, chlorobenzene, or 2-chlorotoluene. Spin coating was done at 2000 rpm for 1 minute, with no annealing. PCBM solutions were initially made in toluene. Later, chlorobenzene and 2-chlorotoluene were used, with 2-chlorotoluene giving the highest quality PCBM films. 2-chlorotoluene was selected for having high PCBM solubility and a low P3HT solubility.[60] PCBM was vapor deposited at a pressure of 0.5×10^{-6} Torr or less, and a rate of approximately 0.05-0.4 Å/second.

Prior to PCBM deposition, the OTS or HMDS treated samples were subjected to a second HMDS or OTS treatment to cover the portion of the substrate exposed via oxygen plasma. Again, no difference was noted between the surface potentials of treated and non-treated samples.

2.1.6 CYTOP removal

To expose the lateral junction, the wafers were submerged in perfluorodecalin in a tightly closed glass container. The container was heated at 50°C for 1 hour, and then allowed to sit until the CYTOP/S-1813 layer was removed, approximately 12 hours. This was followed by a rinsing step to remove residual material that would affect the SKPM scans.

For top contact samples, the majority of the CYTOP/S-1813 layer was peeled off first with scotch tape, followed by the perfluorodecalin treatment. Despite findings that scotch tape application and removal can cause charge trapping,[28] the same interface polarity and magnitude of voltage step at the lateral junction was seen whether or not tape was used. It is likely that the processing steps following the delamination with scotch tape, as well as sample grounding during surface potential measurement, served to dissipate trapped charges from the P3HT or s-SWCNT layer.

2.1.7 Top contact electrode deposition

The initial geometry of the lateral diodes was top contact, with the electrodes deposited on top of the complete diode. For the top contact samples, a metal mask was aligned so the electrodes would fall on either side of the formed interface. The electrodes for these samples were separated by 1 mm. Top contact electrodes were 100 nm aluminum or 50 nm gold.

2.2 SKPM of lateral donor-acceptor junctions

SKPM was used to measure the interfacial potential of the lateral donor-acceptor junctions. For most samples, single line scans were taken perpendicular to the interface. An example line scan of a P3HT/PCBM junction is shown in Figure 19. The interfacial potential was calculated from contact potential difference values measured by the SKPM, which were scaled and plotted using a MATLAB script written for this purpose.

Figure 19: A 70 μm SKPM line scan across a P3HT/PCBM junction showing a more negative potential over the PCBM.
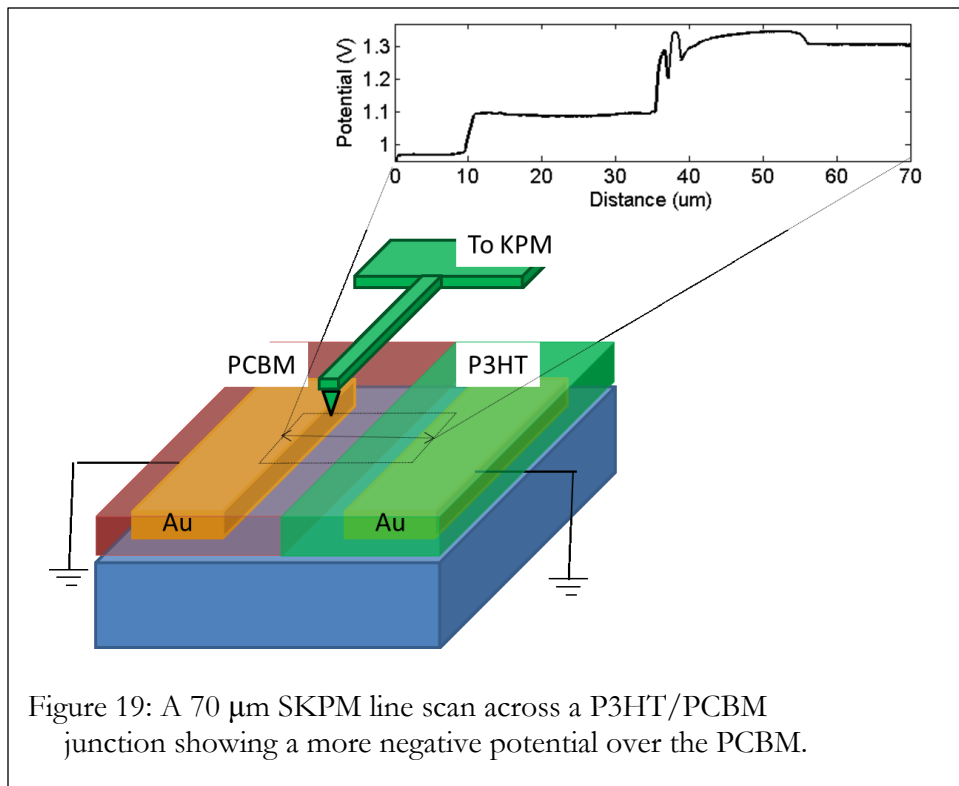
The potential difference between the materials was calculated by subtracting the potential of a flat region of PCBM from the potential of a flat region of the donor.

3 Spectroscopic and I/V characterization of lateral architecture devices

3.1 Spectroscopic characterization of the plasma etched surface

There was concern that the donor/CYTOP layers were not fully removed from the surface following oxygen plasma etching, so the PCBM layer deposition occurred over residual donor and/or CYTOP. Therefore, Raman and UPS measurements of the surface were taken following etching for several samples. Raman spectra were acquired on P3HT/CYTOP and s-SWCNT/CYTOP samples with and without oxygen plasma etching. The spectra were acquired by Natalia Drichko from the Johns Hopkins Department of Physics and Astronomy. Convenient Raman frequencies to look for in a regioregular P3HT film are sharp peaks at 1450 and 1380 cm^{-1}.[61] The G band absorbance around 1600 cm^{-1} [62] was used for the nanotube samples. Figure 20 shows the spectra obtained with and without etching—showing clearly that both OSCs are present initially, and removed by etching.

CYTOP does not have Raman active peaks due to its high transparency, so it was not possible to determine the presence of CYTOP on the surface from Raman. However, since in all cases CYTOP was deposited on top of the donor layer, it is logical that since the donor material has been removed completely, the CYTOP has also been removed.

Figure 20: Raman spectra of P3HT/CYTOP and s-SWCNTs/CYTOP, as well as these materials following etching with oxygen plasma. The OSC peaks are eliminated following etching.
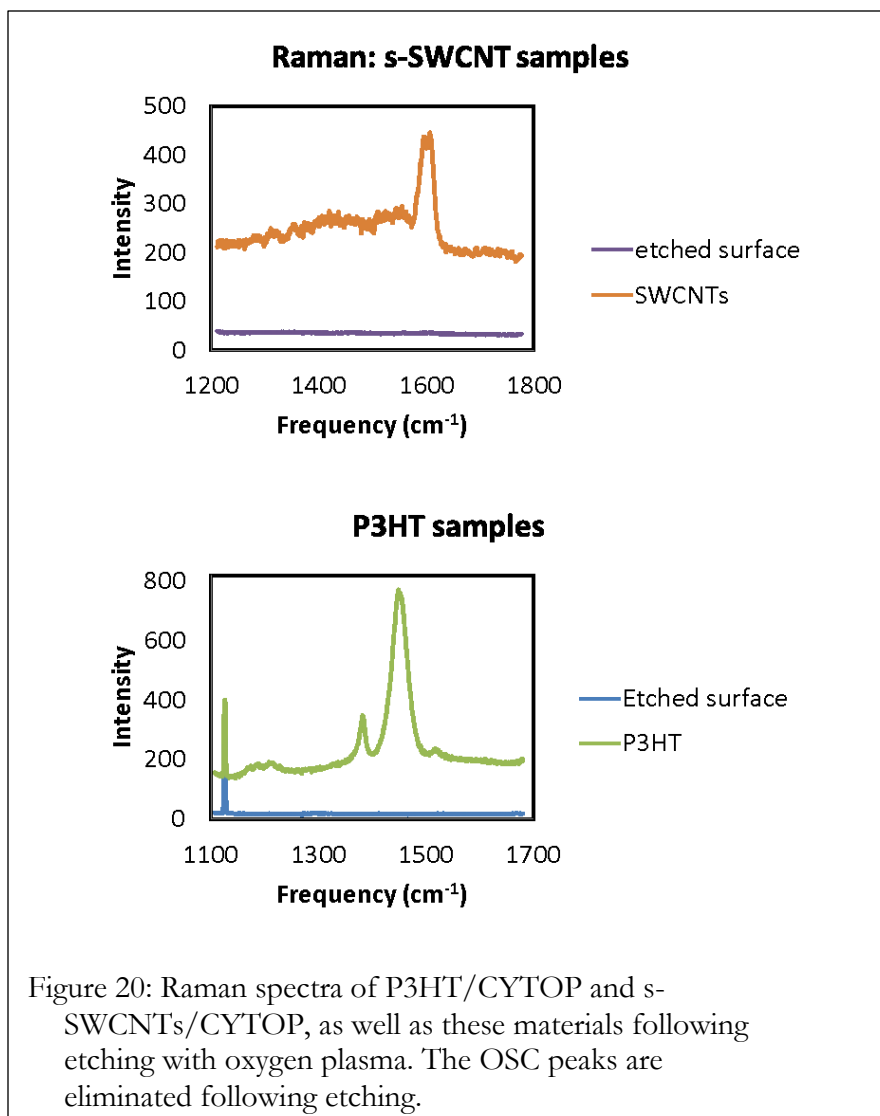
To further examine the surface following etching, XPS was used to measure the relative amounts of elements on the sample. The elements that would have shown the presence of remaining material were, for P3HT, carbon and sulfur; for s-SWCNTs and PFO, carbon, only; and for CYTOP, carbon, oxygen, and fluorine (see Figure 21 for the structure of CYTOP). Fluorine from CYTOP, and sulfur from P3HT were the best markers to look for, because carbon and oxygen are always found on samples taken from the air.

Figure 21: Chemical structure of CYTOP.
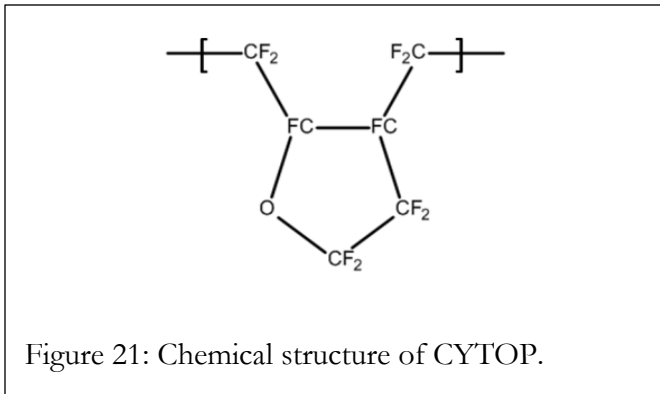
The XPS spectra were taken by on a model PHI 5400 instrument by Michael Barclay in Howard Fairbrother's group in JHU Materials Science. Survey scans were taken of each of three types of sample. First, a wafer on which CYTOP had been deposited and from which it was then etched; second, a wafer that had P3HT, then CYTOP deposited thereon, then etched therefrom; and finally a wafer with s-SWCNTs and CYTOP deposited thereon and then etched therefrom. The CYTOP-only sample is shown in Figure 22, with peaks of interest labeled.

Figure 22: XPS survey scan of an etched CYTOP-only sample showing a large fluorine peak, a small carbon peak, and a clear peak from the silicon.

46
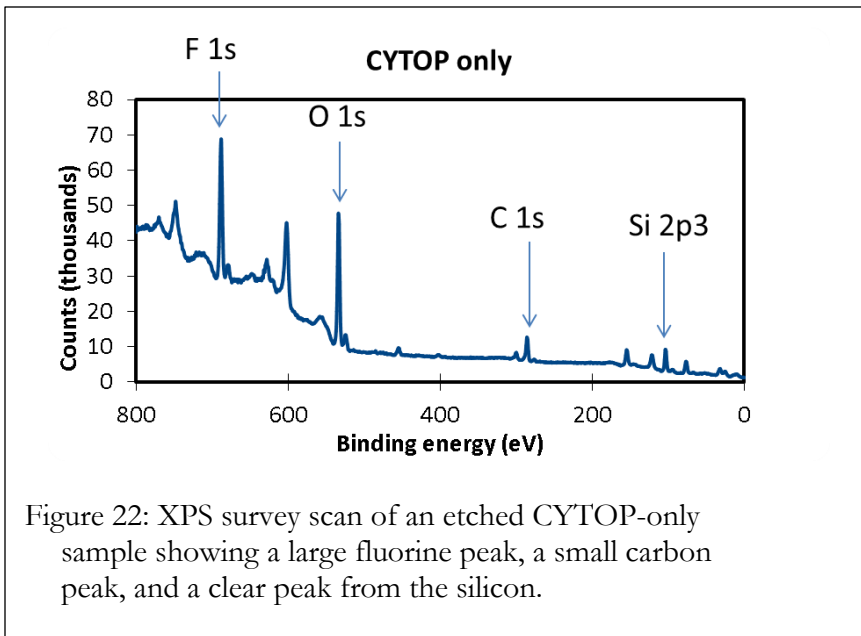
The data from all three is summarized in Table 1. All three samples showed a large

fluorine peak, which could be from residual CYTOP or from XPS chamber contamination,

the latter being a known issue for this XPS system. The P3HT sample did not have a peak

for sulfur, confirming the results from Raman that P3HT was fully etched off. On the other

hand, the s-SWCNT sample showed increased fluorine and carbon peaks, along with a

decreased silicon peak. The smaller size of the silicon peak indicates the SiO_2 surface has

increased coverage compared to the other two samples. For the s-SWCNT sample, this

indicates that the films may not have been etched off completely.

	F 1s	O 1s	C 1s	Si 2p3
CYTOP only	9k	8k	2k	8.6k
P3HT and CYTOP	5k	2k	4k	8.9k
s-SWCNTs and CYTOP	8k	1k	1k	3.2k

Table 1: XPS counts for fluorine, oxygen, carbon, and silicon on three etched
    surfaces: CYTOP, P3HT+CYTOP, and s-SWCNTs+CYTOP.

3.2   I/V characterization of lateral diodes

Given the XPS indication that CYTOP might be incompletely etched during

fabrication on some or all of the substrates, further confirmation of the quality of the lateral

diodes was required. Current/voltage tests of the lateral diode were used to determine if the

lateral diodes were electronically functional. The voltage across the electrodes spanning the

junction was scanned between +100V and -100V, and the current through the junction was

measured. The distance between the electrodes for these samples was 900 μm. Both

P3HT/PCBM and s-SWCNTs/PCBM show increased current under forward bias compared to reverse (Figure 23), indicating that they function as diodes. Forward current and rectification are both lower than typically seen in diodes with the standard vertical architecture, for two reasons. First, the distance between electrodes is much larger, so the electric field for a given voltage is smaller. Second, the area of interface between the donor and acceptor is smaller in the lateral architecture than in a standard vertical architecture.

Figure 23: Diode scans of lateral P3HT/PCBM and s-SWCNT/PCBM junctions showing current rectification.
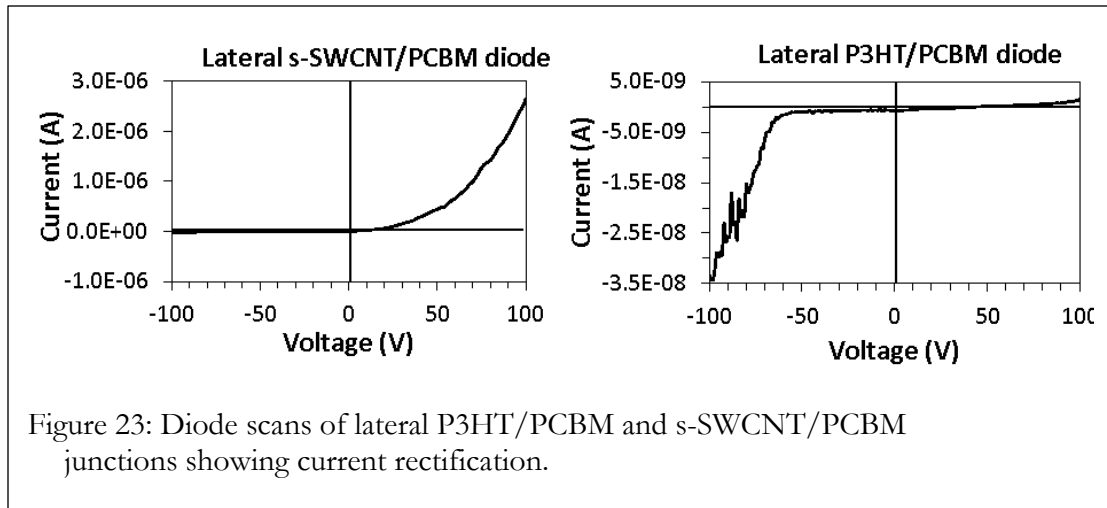
3.3   OFET output curves

To test film quality of the OSCs, P3HT, PCBM, and s-SWCNTs were each made into OFETs using a Si/300 nm SiO_2 gate. Output curves of the OFETs (Figure 24) confirmed the materials had reasonable field effects and current saturation behavior.
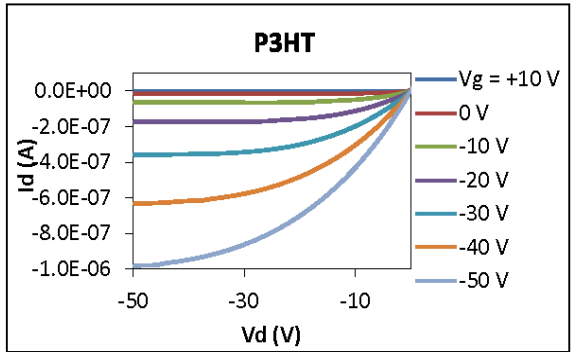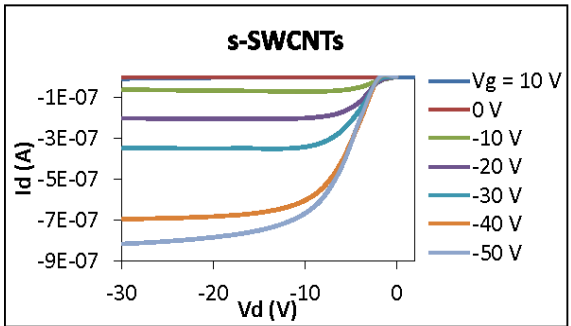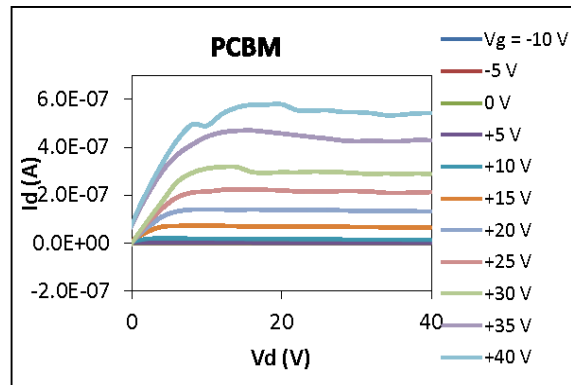
Figure 24: Output curves of PCBM, P3HT, and s-SWCNT films.

4   Measuring the surface potential of lateral donor-acceptor junctions

4.1   Negative polarity of PCBM adjacent to donor macromolecule domains

Here we report a direct study of interfacial potential difference in single donor-acceptor junctions. We formed side-by-side (lateral) donor-acceptor junctions on insulating substrates using a fluoropolymer-based photolithography process developed by our lab.[55–57] Scanning Kelvin Probe Microscopy (SKPM) was used to map the electrostatic potential profile of the exposed donor-acceptor interface.

Because of the flexible nature of the lateral junction technique, we were able to compare samples where the donor and acceptor were in contact, with those deposited with a narrow gap between the donor and acceptor. This allowed us to isolate the contribution to the interfacial potential difference from donor-acceptor contact from that of the bulk donor and acceptor.

Furthermore, this geometry allows us to observe the potential difference at the OSC/OSC interface without the risk of influencing the result by charging the sample, which can occur during photoelectron spectroscopy on OSCs. Fabrication itself can incorporate extraneous charges, though, so to eliminate these, we also ground both terminals of the junction during SKPM measurement.

Figure 25 shows an illustration of a lateral P3HT-PCBM junction and the region we scanned with SKPM. SKPM provides a map of the electrostatic potential of the surface (surface potential) using a variant on the vibrating capacitor method of determining work functions.[2,39–43] In an OSC, SKPM measures the density of trapped and free charges in the film, superimposed upon the difference in bulk vacuum levels.

50

We observe a consistent polarity at the interface between P3HT and PCBM (Figure 25b). The PCBM side is negative, as has been observed in the past with SKPM of bulk heterojunctions using a PCBM acceptor.[40,41] As mentioned before, PCBM was deposited both from solution and from vapor with identical results. This is shown for P3HT/PCBM junctions in Figure 26.

Figure 25: a) A diagram of the region observed. The surface potential of a) P3HT/PCBM and b) s-SWCNTs/PCBM both show the more negative potential on PCBM.
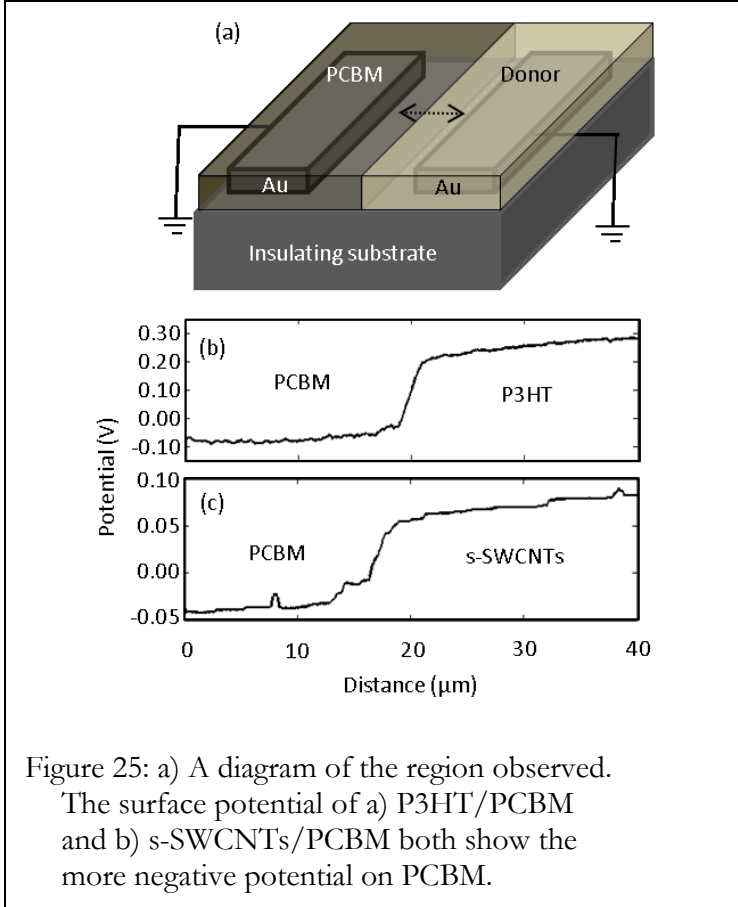
The value of the interfacial potential difference varies slightly from sample to sample. It is presented as mean ± standard deviation, with n indicating the number of samples. For P3HT/PCBM, it was 0.21 ± 0.04 V, n = 10. For SWCNTs/PCBM, the interfacial potential difference was 0.06 ± 0.04 V, n = 12 (Figure 25c). Though coverage of the substrate by the s-SWCNTs was less continuous than for the P3HT samples, a similar but smaller

51

polarization was observed; meaning this direction of polarization could be a more general phenomenon for PCBM. The smaller potential difference for the s-SWCNT samples can be explained by different bulk work functions of P3HT and s-SWCNTs, and also may have contributions from the effect noticed by Aarnio, et al. in which a donor polymer, once annealed, is more likely to reduce a neighboring PCBM molecule.[19] This is attributed to decreased conjugation length—and increased ground state energy—of P3HT molecules near the interface.
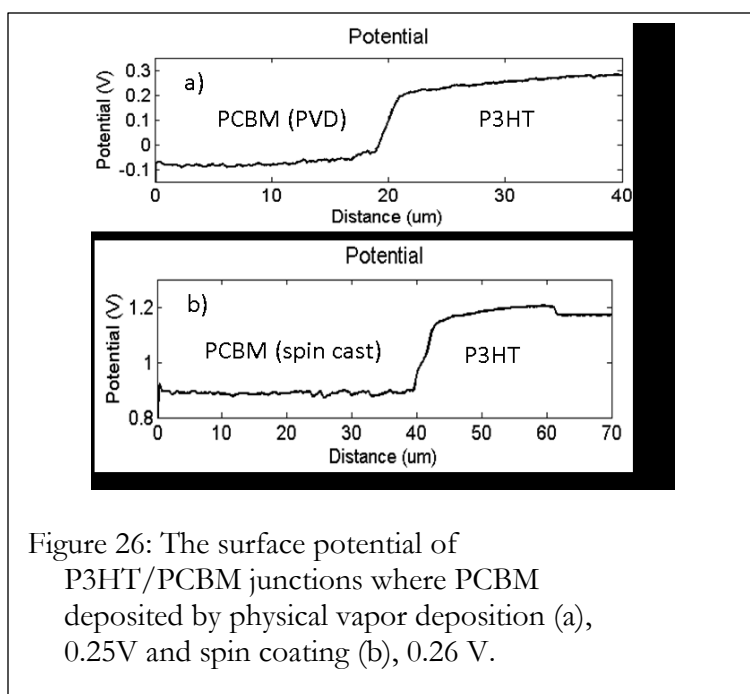
Figure 26: The surface potential of P3HT/PCBM junctions where PCBM deposited by physical vapor deposition (a), 0.25V and spin coating (b), 0.26 V.

Following storage under ambient conditions, the magnitude of the potential difference decreased, but the general observation that PCBM is more negative than the donor was consistently seen. This potential difference should be accounted for in analyzing organic solar cell performance, as it is a significant fraction of typical open circuit voltage.

To isolate the effect of contact between the donor and acceptor from their bulk properties, nine samples were made with a small, approximately 15 µm, gap inserted between

P3HT and PCBM (Figure 27). The total over which scanning could be done was 70 µm, due to instrument limitations, so P3HT, PCBM, and the space between them were patterned within this width.

Figure 27: A diagram of PCBM/SiO$_2$/P3HT showing that intermolecular interactions are not possible in this geometry.
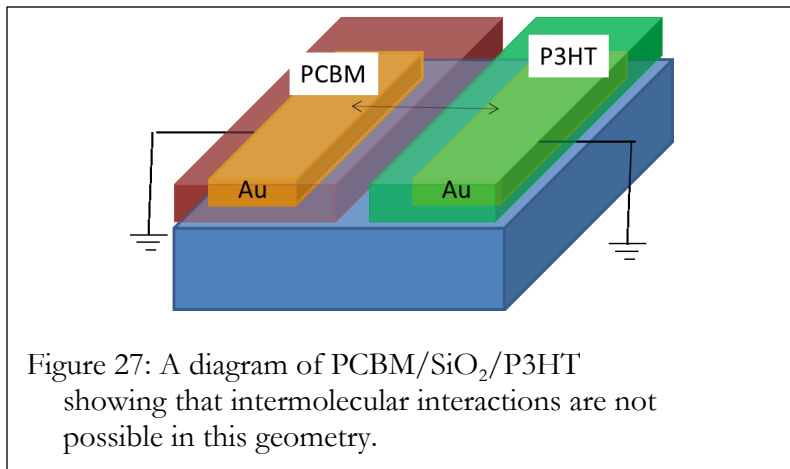
Surface potential scans across the P3HT-SiO$_2$-PCBM configuration resulted in measurements of the relative voltages of P3HT and PCBM when they are insulated from each other and not touching. For the nine samples made, the surface potential measured between P3HT and PCBM of 0.10 ± 0.03 V (Figure 28b, and summarized in Table 2).
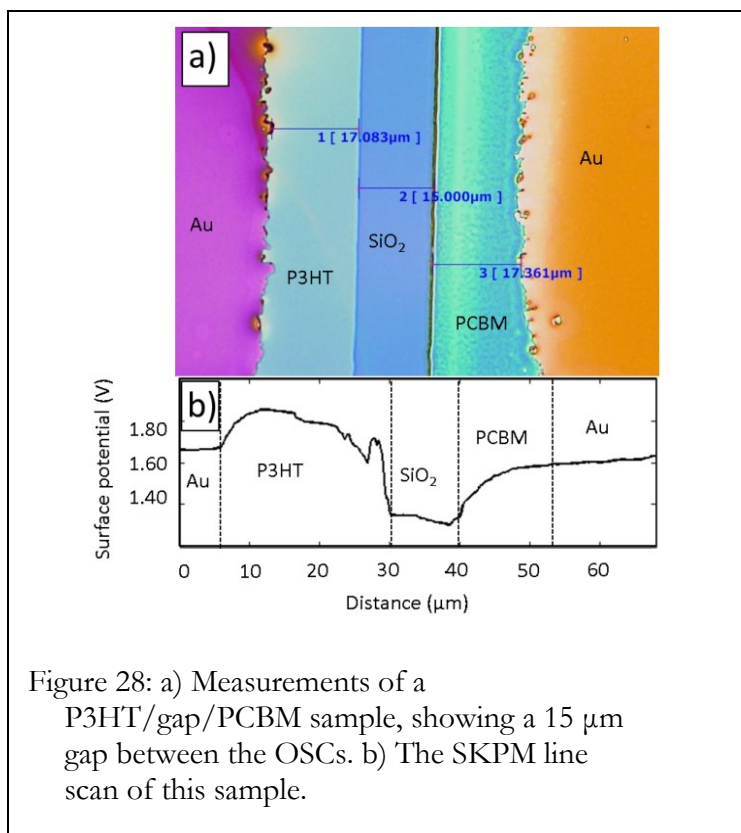
Figure 28: a) Measurements of a
P3HT/gap/PCBM sample, showing a 15 µm
gap between the OSCs. b) The SKPM line
scan of this sample.

The potential difference measured in the samples with a gap between the OSCs is not indicative of interfacial potential difference, as the two materials are not in contact. Instead, this potential difference originates only from the different electronic states of the individual materials and their possible occupancies by trapped charges.

	N	Mean	Std. Dev.
P3HT-PCBM	9	0.21	0.04
P3HT-SiO$_2$-PCBM	9	0.10	0.03

Table 2: Mean and standard deviation of potential difference with and without gap, demonstrating a higher potential difference when P3HT and PCBM are in contact.

A Student's "t" test was done to compare this data set with the previously obtained surface potential of P3HT/PCBM junctions. To give the same number of samples for both,

one data point was removed from the P3HT-PCBM data set at random. Then, normal

distribution of the nine surface voltage measurements in each data set was confirmed by

Q-Q plots (Figure 29). Chi-square testing is typically used to test normal distribution, but it

requires a larger data set. In the Q-Q plot, the points lie close to the y = x line, indicating the

data is normally distributed.

Figure 29: Q-Q plots to test data normality.
Points lie close to the y = x line, indicating
that the data is likely to have a normal
distribution.
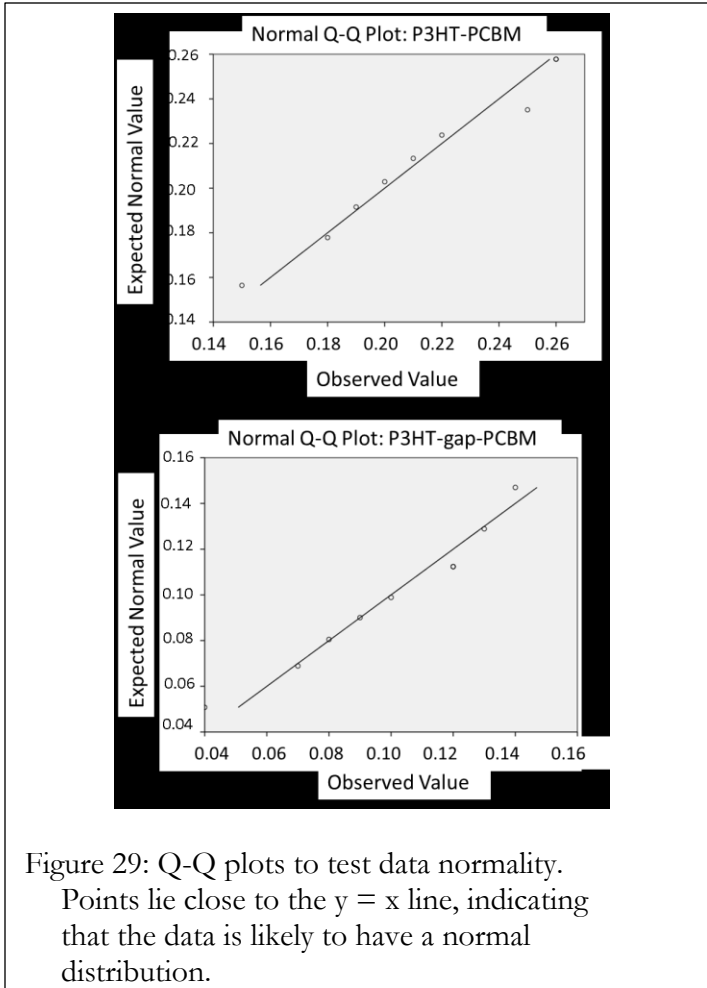
Using a two variable independent t-test of equal means, the variances of the two data

sets were determined to be equal, and the 99% confidence interval for the difference

between the means is -0.16 V to -0.07 V, summarized in Table 3.

Independent Samples Test									
	Levene's Test for Equality of Variances		t-test for Equality of Means						
								99% CI of the Difference	
	F	Sig.	t	df	Sig. (2-tailed)	Mean Difference	Std. Error Difference	Lower	Upper
Equal variances	0.280	0.604	-6.886	16	0.000	-0.11444	0.01662	-0.16299	-0.06590

Table 3: t-test results indicating that there is less than a 0.05% chance that both data sets are from the same distribution (rounded to 0.00% by software). The 99% confidence interval of the difference in means between the two samples is 0.16V and 0.07V.

With p < 0.0005, rounded to 0.000 by SPSS software, the 18 data points are from different distributions. This indicates there is less than 0.05% probability that the data is all from the same distribution. Therefore, there is a contribution to interfacial voltage brought about by contact between the materials.

4.2   Substrate effects on interface polarity of a carbon nanotube/fullerene junction

To investigate the possibility of embedded charges in the SiO_2 substrate being the cause of the consistent negative polarity of PCBM at junctions with P3HT and s-SWCNTs, a second substrate, Al_2O_3 on Corning glass, was used. Comparing lateral junctions made on SiO_2 with those made on Al_2O_3, we saw that while P3HT/PCBM gave the same direction of interfacial potential difference (Figure 30a), s-SWCNTs/PCBM did not (Figure 30b). Over four samples of P3HT/PCBM, we obtained a 0.14 ± 0.05 V interfacial potential difference, which was approximately 0.05 V less than the average potential measured on SiO_2. However, since the standard deviation of interfacial potential measurements ranges from 0.03 – 0.10 V, this is not statistically significant, and more work would be required to determine if it is meaningful. For s-SWCNTs/PCBM, over five samples, we obtained a 0.35 ± 0.10 V interfacial potential difference, with the negative side of the dipole now on the s-SWCNTs.
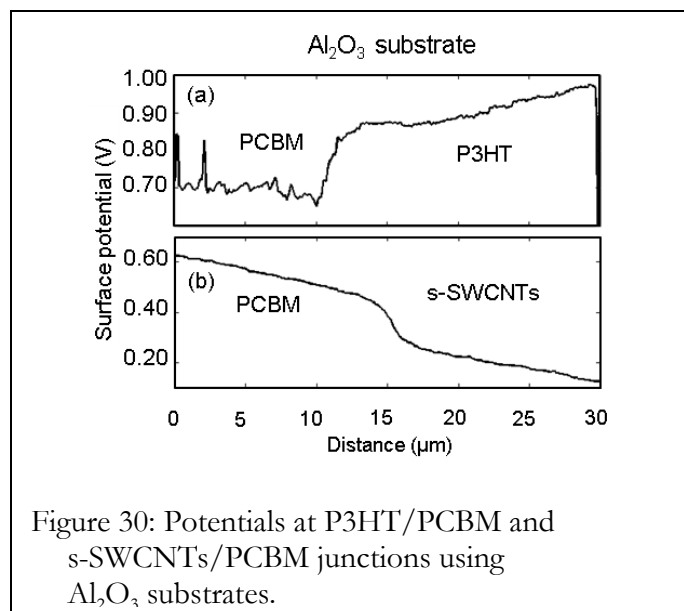
Figure 30: Potentials at P3HT/PCBM and
s-SWCNTs/PCBM junctions using
Al$_2$O$_3$ substrates.

Two points stand out—first, the interfacial potential difference of s-SWCNTs on an Al$_2$O$_3$

substrate is approximately 0.35 V more negative than PCBM, while on SiO$_2$ it is approximately

0.07 V more positive. Second, the interfacial potential difference of P3HT/PCBM is similar on both

SiO$_2$ and Al$_2$O$_3$ substrates, while it is not for s-SWCNTs/PCBM. There are likely contributions to

both from the substrate and the s-SWCNTs.

The s-SWCNT layer may allow surface effects on the surface potential that P3HT does not.

The s-SWCNT layer is both thinner (<5 nm compared to ~50 nm) and more conductive than the

spin-coated P3HT film, so it will screen the surface potential of the substrate less effectively.

Because Al$_2$O$_3$ is known to be more chemically reactive than SiO$_2$, its surface could be subject to

trapping oxygen or water from the air, which the s-SWCNTs would fail to screen completely. This

would alter the electrostatic potential at the surface.

To test if the layer of nanotubes was too thin to screen the Al$_2$O$_3$ substrate, PCBM/Al$_2$O$_3$

and PCBM/SiO$_2$ lateral samples were made by leaving off the initial P3HT or s-SWCNT deposition

step. Line scans of the surface potential are shown in Figure 31a and Figure 31b, respectively.

PCBM/SiO_2 and PCBM/Al_2O_3 both have a surface potential difference of 0.09 V with the PCBM

on the positive side.

Figure 31: Surface potential of PCBM adjacent toSiO$_2$ and Al$_2$O$_3$.
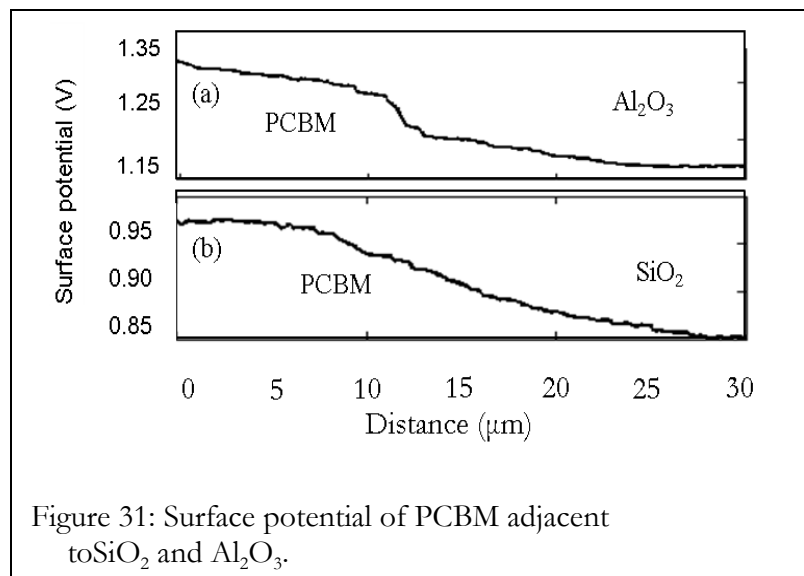
However, the potential difference in Figure 31a at the PCBM/Al_2O_3 interface is only 0.09 V,

compared to the 0.35 V difference seen in Figure 30b. The potential difference is increased when the

Al_2O_3 is coated with a thin layer of s-SWCNTs, but not when the SiO_2 is so coated. This leads us to

believe that the negative surface potential of PCBM in Figure 30a and in Chapter II, Section 4.1,

comes from occupancies of its own electronic states perturbed by contact with the donor, not from

trapped charges in the substrate.

To understand the possible mechanism behind this, we looked at the relative permittivities

of SiO_2 and Al_2O_3. The permittivity of Al_2O_3, at 9.4, is higher than that of SiO_2, at 3.9.[25] Dielectric

constant of an insulator has been seen to affect the states in an adjacent OSC causing a decrease in

carrier mobility. Hulea, et al., shows that the decreased field effect mobility can originate from the

increased formation of polarons that act to screen free carriers at interfaces with higher dielectric

constant insulators.[25] Richards, et al., agrees that the dielectric constant of an insulator next to an

OSC decreases the field effect mobility of the OSC, but shows that the cause can be differing

59

amounts of static dipolar disorder.[26,27] An insulator with a larger dielectric constant has more randomly oriented static dipoles, or static dipolar disorder, than an insulator with a smaller dielectric constant. The density of states (DOS) of the first 0.5-1.0 nm of OSC at the dielectric interface is broadened by the presence of randomly oriented strong dipoles in the high-k dielectric. The broadened DOS decreases the favorability of charge carrier hopping and reduces the mobility.[26,27]

In this SKPM study, we did not move charges through OSCs, but these findings are relevant. Greater charge carrier screening by polarons and a broader DOS near the interface can alter the surface potential of a thin OSC layer over a high dielectric constant insulator like Al_2O_3. Free charges are necessary to interact with these traps, but they can accumulate in the OSC during processing or from the grounded electrodes during the scan. Those under the more insulating P3HT and PCBM layers are largely screened from the scanning probe, but the thin layer of s-SWCNTs may not be capable of such screening. It is interesting that substrate effects may be seen by scanning probe microscopy, which is frequently assumed to be a surface-specific measurement. Further work is needed to determine under what conditions the dielectric constant of the substrate affects the surface potential of an organic thin film, as this has relevance for both scanning probe and OPV fields.

5   Conclusion

Here we measured the interfacial potential differences at donor-acceptor junctions using SKPM, and quantify for the first time how much of the potential difference originates from physical contact between the donor and acceptor. We see a statistically significant and pervasive negative polarity on the PCBM side of PCBM/donor junctions, which should also be present at the complex

interfaces in bulk heterojunctions. This potential difference may originate from molecular dipoles, interfacial interactions with donor materials, and/or equilibrium charge transfer due to the higher work function and electron affinity of PCBM. We show that the contact between PCBM and P3HT doubles the interfacial potential difference, a statistically significant difference. Control experiments comparing the surface potential on two substrates demonstrated that this potential difference between P3HT and PCBM was not due to charges trapped in the underlying substrate. The direction of the observed potential difference would lead to increased V_{oc}, but would also likely pose a barrier to electrons being injected into the PCBM and make recombination more favorable. Our method may allow unique information to be obtained in new donor-acceptor junctions.

There are four possible sources of the observed interfacial potential difference. First is electron transfer to PCBM from the donor. For the P3HT/PCBM system, this is made more likely because each P3HT film was annealed at 95°C for 10 minutes. The annealing process can shorten the delocalization length in the polymer film and make oxidation more favorable[19] , which would not happen across a gap between the materials.

The second potential source is from molecular dipoles forming across the interface due to van der Waals interactions or polar orientations of molecules. This is likely to be present to some degree in any heterojunction, and could only result from contact between the two materials.

A third possible source of interfacial potential difference is trapped static charges, which would be reduced by sample grounding if the trap states were above the Fermi level. If PCBM had more deep traps for electrons than P3HT or s-SWCNTS, one would observe the negative potential in PCBM. This does not require contact between the donor and acceptor.

The final possible contribution to the observed interfacial potential difference is from film impurities with oxidation or reduction potentials favorable for equilibrium charge transfer to occur,

i.e. with the capability to trap charges originating from the opposite side of the interface. However, the consistency of results in Figure 26, where PCBM was deposited from vapor (a) and solution (b), presumably leading to films with different impurity levels, indicates that impurities are not the determining factor for the direction of the interfacial potential difference.

In addition to the effect of contact on the potential difference, we have observed a reversed interfacial potential difference at a carbon nanotube/fullerene interface when it is formed on Al_2O_3 compared to when it is formed on SiO_2. We do not observe this reversal in the polymer/fullerene junction. We hypothesize the cause is a combination of poorer screening of a more reactive substrate (Al_2O_3) by the nanotubes (which are a thinner, more conductive film than the polymer film) and greater static dipolar disorder at the Al_2O_3 interface. The static dipolar disorder leads to stable trapping of otherwise mobile charges, which may originate from the carbon nanotubes, the externally applied potential, or low lying static charges from the insulating substrate.

Future work on this project would include correlation of OPV efficiency with the interfacial potential measured at the donor-acceptor junction. If a relationship was determined between the interfacial potential and PCE, it would help clarify what qualities a good OPV material has, and allow development of improved semiconductors for solar applications.

CHAPTER III: Localizing Static Fields in Organic Dielectric Layers

1   Introduction

OFETs continue development as substitutes and supplements for silicon-based electronics in large-area and flexible electronics. Their well-known advantages include: scalable, low-temperature fabrication techniques; control over electronic properties via organic chemistry; and device qualities like transparency, self-healing, flexibility, and stretchability for use in new applications. However, the issue of bias stress leading to the increase of V_{th} over time continues to detract from the applicability of OFET-based circuits.

Charge trapping and storage in polymer dielectrics can be harnessed for the control of semiconductor device behavior, including that of OFETs. The gate insulator chosen for an OFET affects bias stress and V_{th} of the OFET. Charging the dielectric can control the operating voltage and the bias stress susceptibility of the device by, respectively, incorporating additional electric fields, and pre-filling interface traps.

In this chapter, a layered gate dielectric made of substituted and non-substituted polystyrene (PS) forms the sole gate dielectric for pentacene OFETs. Thermal cross-linking of benzocyclobutene subunits ensures layer integrity so the layers of polymer can be deposited sequentially from solution. This method of crosslinking was used because it does not add heteroatoms or small molecule byproducts to the crosslinked film. Neutron reflectivity (NR), scanning electron microscopy, and atomic force microscopy (AFM) of the dielectric stacks showed that individual layer thicknesses varied systematically with polymer concentration in deposition solutions, and interfacial thicknesses ranged from 1.5-4 nm, independent of layer thickness, demonstrating formation of distinct layers with minimal intermixing.

OFETs were fabricated from the newly-synthesized PS derivatives. The V_{th} shift following poling of the gate dielectric for 10 minutes was used as a metric of charge-trapping capabilities and bias stress susceptibility in the device.

Bias stress can arise from subtle differences in dielectric polymers. For example, the number of chain ends or internal branching was found to increase the bias stress from a polystyrene dielectric, likely by a charge trapping mechanism.[63,64] The increasing free volume in the series isotactic, syndiotactic, and atactic PMMA correlated with increased bias stress in pentacene transistors.[65] Some solutions for bias stress instability utilizing polymer dielectrics have been proposed in the literature. One approach is to use a fluorinated gate dielectric,[29] which decreases the trap density at the OSC/dielectric interface. On the other hand, fluorinated gate dielectrics are also hydrophobic, which can affect the morphology and adhesion of subsequent layers.

1.1   Dielectric effects on V_{th} and bias stress in OFETs

Dielectric polymer films affect performance of electronic devices such as memory elements and piezoelectrics in ways beyond passive insulation.[66–69] In OFETs, the bulk and interface properties of the gate dielectric determine operating voltage ranges. The OSC/dielectric interface greatly influences the V_{th} and the number densities and mobilities of charge carriers in the OSC.[70] Electric fields applied to the OFET gate dielectric can cause charge trapping or polarization, so after the field is removed, V_{th} shifts of tens of volts are seen. These either are produced intentionally in the case of nonvolatile transistors for memory applications,[23,66,71,72] or incidentally as a result of bias stress. Greater control over the amount and direction of charge is desired in order to produce memory devices, and it is proposed that bias stress can be eliminated by charging as well. This would be accomplished by pre-populating charge trap states, preventing further charge trapping to a significant degree upon device operation.

65

Modifications to polymer dielectrics, in conjunction with charging, have been studied for both nonvolatile memory and bias stress reduction. Ferroelectric polymers contain polar groups that, following application of a bias, retain an electrostatic polarity. Ferroelectric polymers as well as polymers without these polar groups have been used as bulk electrostatically polarizable film materials. Examples of polymers used in these studies include poly(methylstyrenes),[73,74] poly(vinylidene fluoride),[75,76] polystyrene-poly(vinylidene fluoride-co-trifluoroethylene) bilayers,[77] and poly(vinyl alcohol) paired with polystyrene (PS) as a tunneling layer.[78] Multiple inorganic dielectrics have also been stacked to make trap-based memory devices, such as one case where an inorganic gate dielectric stack sandwiches HfO_2 between layers of Al_2O_3 to result in extremely high hole and electron trapping capacity.[79] An organic/inorganic hybrid trap-based memory device with an Al_2O_3 dielectric modified by self-assembled monolayer showed clear memory characteristics.[80] A substituted triphenylene trap layer was sandwiched between poly(methyl methacrylate) (PMMA) and oxide to form a memory element.[81] Doping a bulk polymer with a small amount of electron donor or acceptor has been used to increase charge trapping. Nakajima and Fukjii used fullerene-polystyrene blends in hysteretic gate dielectrics characterized as capacitors.[30,82] Fullerenes were embedded in polymer or self-assembled monolayer dielectrics for charge storage.[30,83,84] Fluorene polymer and polyaniline particles with poly(methyl methacrylate), and fluorene-methacrylate di-block copolymers with poly(vinyl alcohol), respectively, were blended to function as the gate dielectrics in pentacene memory transistors.[85–87] Fluorene, triarylamine, diphenyl ether, thiophene/selenophene oligomers, or polycyclic arenes were considered as the "donor" when embedded in polyimides where the imide was the "acceptor" in "donor-acceptor" electrets.[88–91] A fluorene oligomer was placed as a side group in a polystyrene, and ferrocene was mixed with polystyrene-co-poly(4-vinylpyridine) for the same

66

purpose.[92] Much of the published work relies on silicon oxide protective "blocking" layers to prevent leakage current, rather than designing this protective capability in polymer dielectric materials themselves. An upper protective "tunneling" layer is often employed as well. In the present study, a general procedure for introducing vertically localized functionality into an electret film composed of a single type of hydrophobic polymer is described.

1.2   Bulk and interface charging of polymer dielectrics

There are two major mechanisms by which charging can occur in nonvolatile, or hysteretic, gate dielectric systems.[93,94] The first is the conventional "bias stress" mechanism where trap occupancy energies become equilibrated to an applied gate voltage, shifting V_{th} toward the voltage being applied from the gate. In this mechanism, net static charge is stored at the semiconductor-dielectric interface, or immobile carrier states emerge at energies equivalent to the charging voltage, and the OFETs turn off over time as they are left in the on state.[28] The second is the "dielectric polarization" mechanism, in which the stored charge arises from the polarization response of the bulk of the dielectric, possibly in combination with the semiconductor or gate electrode, to the applied charging voltage. As illustrated in Figure 32, the effect of charging on the induced polarization felt in the bulk of the polymer is opposite for the two mechanisms. Which mechanism is active in any given system depends on the materials used, their structure, and the charging method used.

Figure 32: Poling a trilayer dielectric, leading to (left) interface charge trapping and (right) bulk polarization. The direction of the static field remaining depends on the charging mechanism.
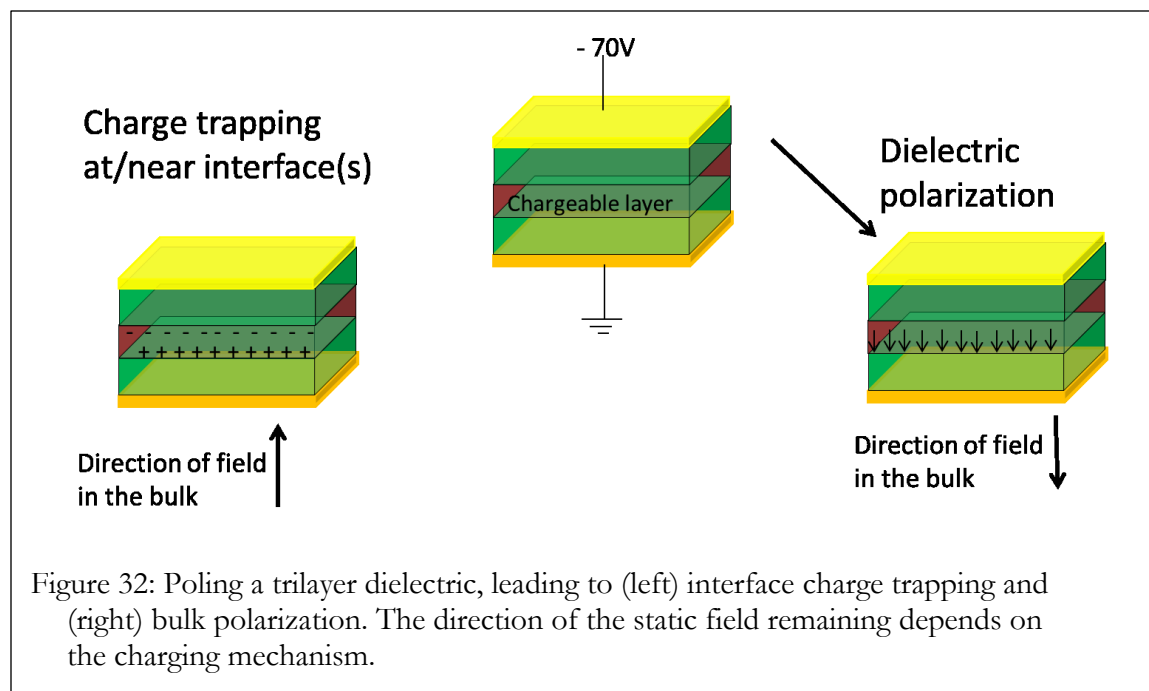
2   Methods

In this chapter, a polymer film system based on polystyrene (PS) is described, which allows the placement of electron donor or acceptor groups in different vertical positions of the dielectric stack. The integrity of the multilayer stacks was assured using neutron reflectivity (NR) and the film thicknesses were measured by NR and scanning electron microscopy (SEM). Layer roughness was characterized by NR for interlayer roughness and atomic force microscopy (AFM) for surface roughness.

2.1   Multilayer dielectric fabrication

Pentacene OFETs were fabricated using the synthesized polymers as in Figure 33, where PS* refers to a PS layer that may have functionality different from the PS layer on which it is deposited. Fabrication steps included spin coating dielectric polymers for each layer on a substrate

containing multiple thermally vapor-deposited gold gate pads, crosslinking any layer on which an additional layer would be deposited, and vapor deposition of pentacene semiconductor and gold source-drain electrodes, as detailed below. Gold rather than silicon was used as the gate, to prevent the complicating effect of the intervening native oxide layer in series with the dielectric polymer to be studied. The structure used here also has the benefit of decreasing short circuits during device testing by placing the source/drain electrode pads over an insulator, rather than over the gate electrode.
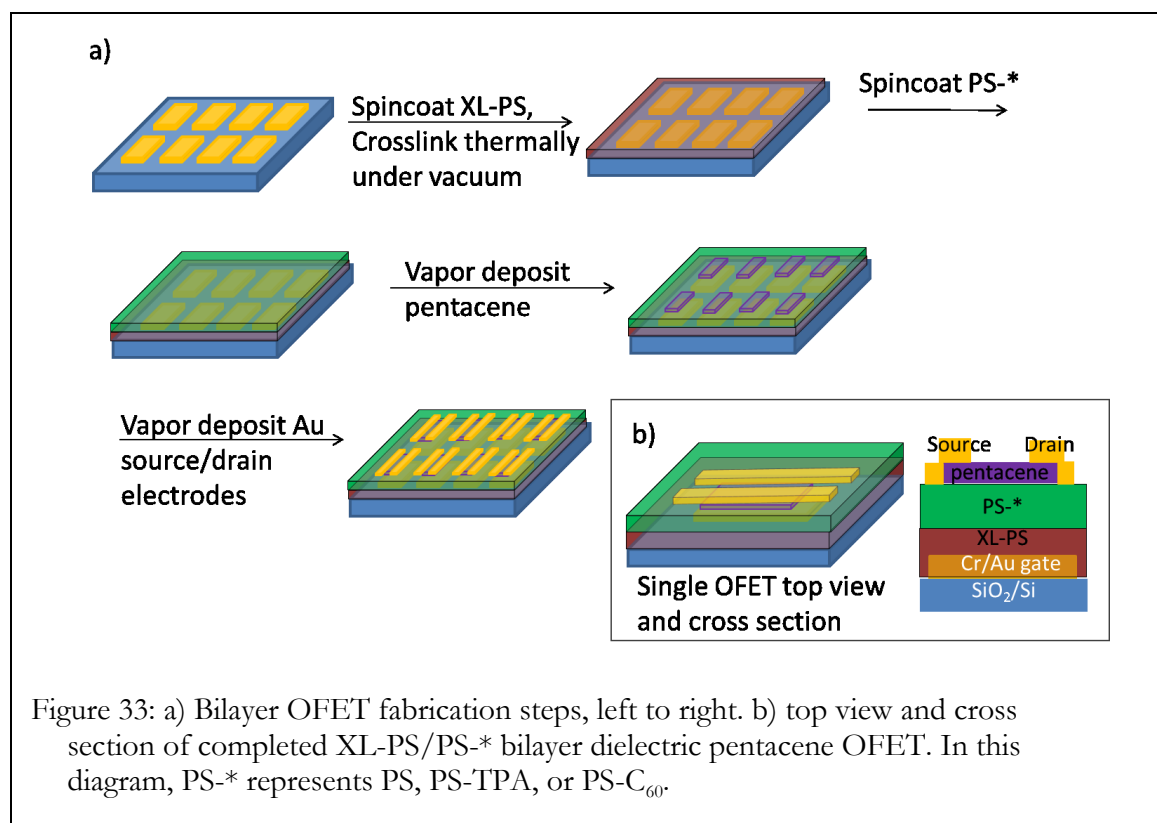
Figure 33: a) Bilayer OFET fabrication steps, left to right. b) top view and cross section of completed XL-PS/PS-* bilayer dielectric pentacene OFET. In this diagram, PS-* represents PS, PS-TPA, or PS-C_{60}.

2.1.1 OFET substrate preparation

Highly doped Si wafers on which a 300 nm thick SiO_2 layer was grown were diced into one inch squares and cleaned in 3:1 H_2SO_4:30% H_2O_2, followed by sonication in deionized (D.I.) water, acetone, and isopropanol. They were dried with a stream of nitrogen. Gate electrodes were patterned

by thermal evaporation of 5 nm Cr/30 nm Au through a shadow mask to give 8 gate pads per one-inch square wafer.

2.1.2 Gate dielectric

Multilayers of polystyrene and substituted polystyrenes were deposited by spin coating over the entire one-inch square wafer. Spin coating was done under a dry nitrogen atmosphere in a glove box to eliminate effects of moisture. All spin coating was done at 1500 rpm for 60 seconds, and the film thickness was controlled by varying the polymer concentration in the range 5 - 20 mg/mL. To deposit layers of crosslinked PS, solutions of crosslinkable PS in $CHCl_3$ were sonicated at 30°C for 60 minutes. Prior to spin coating, the solution was filtered into a second vial through a 0.2 μm or 0.45 μm pore size PTFE syringe filter. Crosslinking was done by heating the wafers in a vacuum oven at 180-200°C under -26" to -28" Hg vacuum for 1 hour. Subsequent PS layers were then spin coated and crosslinked if required.

2.1.3 Pentacene and source-drain electrode deposition

Following the deposition of the gate dielectric, 50 nm pentacene was evaporated through shadow masks so each gate electrode had a pentacene region over it. Source and drain electrodes were deposited through shadow masks over the pentacene films to make 8 devices, each with a source/drain pair, per one-inch square wafer.

2.1.4 Neutron reflectivity sample preparation

Native oxide silicon wafers were used for neutron reflectivity (NR) rather than 300 nm SiO_2 as a thinner layer of SiO_2 simplifies the spectrum obtained and the fitting process. Wafers were diced into 1.5 inch squares, then oxide was cleaned from highly doped Si wafers by 6:1 buffered oxide etch (HF) for 4 minutes, followed by rinsing in D.I. water and drying on a hot plate. Wafers were then cleaned with 3:1 H_2SO_4:30% H_2O_2, followed by sonication in D.I. water, acetone, and isopropanol.

They then were dried by a stream of dry N_2. For samples built on a Cr/Au substrate, 5 nm Cr, followed by 10 nm Au was deposited via physical vapor deposition. The gate dielectric stack was built as for OFET fabrication, with deuterated polymers alternated with nondeuterated polymers for contrast. For bilayers, XL- PS- d_8 was on the bottom with a hydrogenated polymer on top, or a crosslinked hydrogenated polymer was on the bottom and PS-d_8 was on the top. For trilayers, XL-PS-d_8 was on the bottom and PS-d_8 was on the top; a hydrogenated layer was in the middle. PS with chargeable side chains was always hydrogenated, and nonfunctionalized PS flanking layers were deuterated for NR experiments. For samples with a gold or pentacene top surface to facilitate charging, the edges of the sample were masked off with aluminum foil to insulate them from the underlying conductive silicon, followed by vapor deposition of 50 nm gold or pentacene.

2.1.5 Removable PDMS electrode fabrication

To create removable electrodes for charging PS multilayers for NR measurements, a 10:1 polydimethylsiloxane (PDMS, Sylgard 184) solution was prepared by stirring 10 parts by weight of base with 1 part by weight of curing agent in air for 20 minutes, followed by degassing for 20 minutes under vacuum. The uncured PDMS was poured into a petri dish and cured at 70°C for 1 hour. The cured PDMS was cut into 1- or 1.5-inch squares while face-down in the petri dish, then the squares were removed and taped by the corners face-up on the thermal evaporator sample holder. 10 nm Cr followed by 80 nm Au was deposited over the PDMS squares. The conductivity of the metal was verified with a multimeter. Carbon paint was applied to an edge and a small patch on the opposing surface of the PDMS, and electrical continuity between the gold face and the carbon paint on the reverse side was verified. The efficacy of the removable PDMS electrode for charging was ascertained by charging pentacene/SiO_2 OFETs with a PDMS electrode and comparing the V_{th} shift observed to that seen following charging with probes on the vapor deposited source/drain

electrodes. The results were similar using the two charging mechanisms, indicating that the PDMS electrode is a reliable way to charge materials without probing directly on the surface.

2.2   OFET V_{th} measurement and charging

To analyze charging of polymer multilayers, their effect on the V_{th} of an OFET was measured. First, transfer and output characteristics of the OFET were measured. Then, the device was charged by poling for 10 minutes with the gate electrode grounded and +/-70V on the source and drain electrodes (Figure 34). Following charging, the transfer and output characteristics were measured again. The sample was not moved from the probe station during this time. The probes were initially connected to the semiconductor analyzer, then the probes were lifted, connected to the voltage source, and lowered again during charging. The probes were lifted again when the analyzer was reconnected.

Figure 34: Top view and cross section of bilayer dielectric charging. +/-70V was applied to the source and drain electrodes while the gate was grounded for 10 minutes.
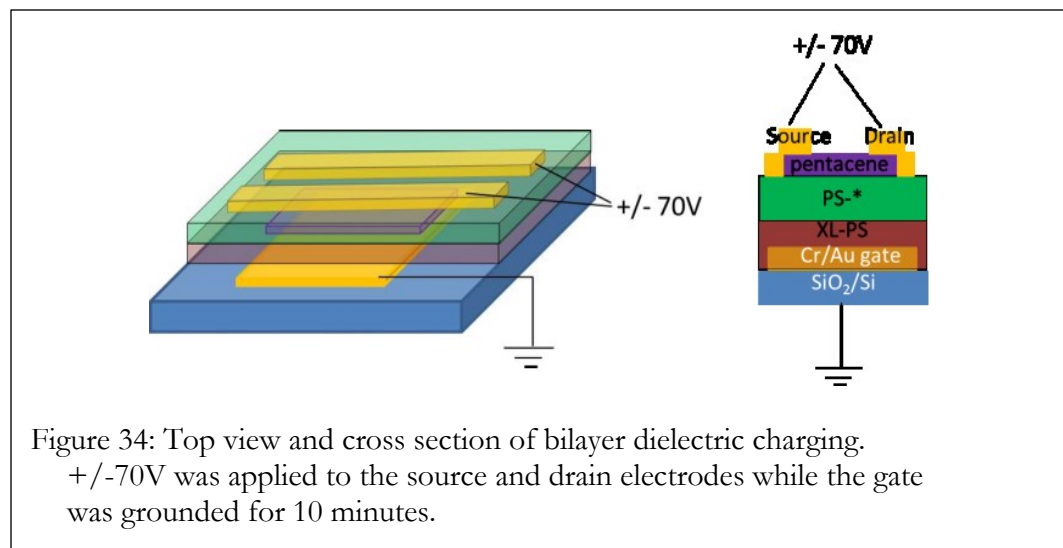
Gate leakage current was measured simultaneously with the drain current for each sample analyzed. The square root of the gate current vs. the applied gate voltage, for ease of comparison with square root transfer curves, is shown in Figure 35 for representative devices. The square root of the gate current is typically about an order of magnitude lower than the square root drain current,

meaning the absolute value of the gate current is two orders of magnitude lower. This means the OFET does not have significant current leaking through the gate dielectric. The noise observed in these plots could be attributed to charge traps in the dielectric or at the interface, but due to the small overall current are not significant.

Figure 35: Representative gate current plots for each dielectric showing the square root of the gate current vs. the gate voltage for ease of comparison with square root transfer curves. Gate current was two orders of magnitude lower than drain current, indicating minimal gate leakage.
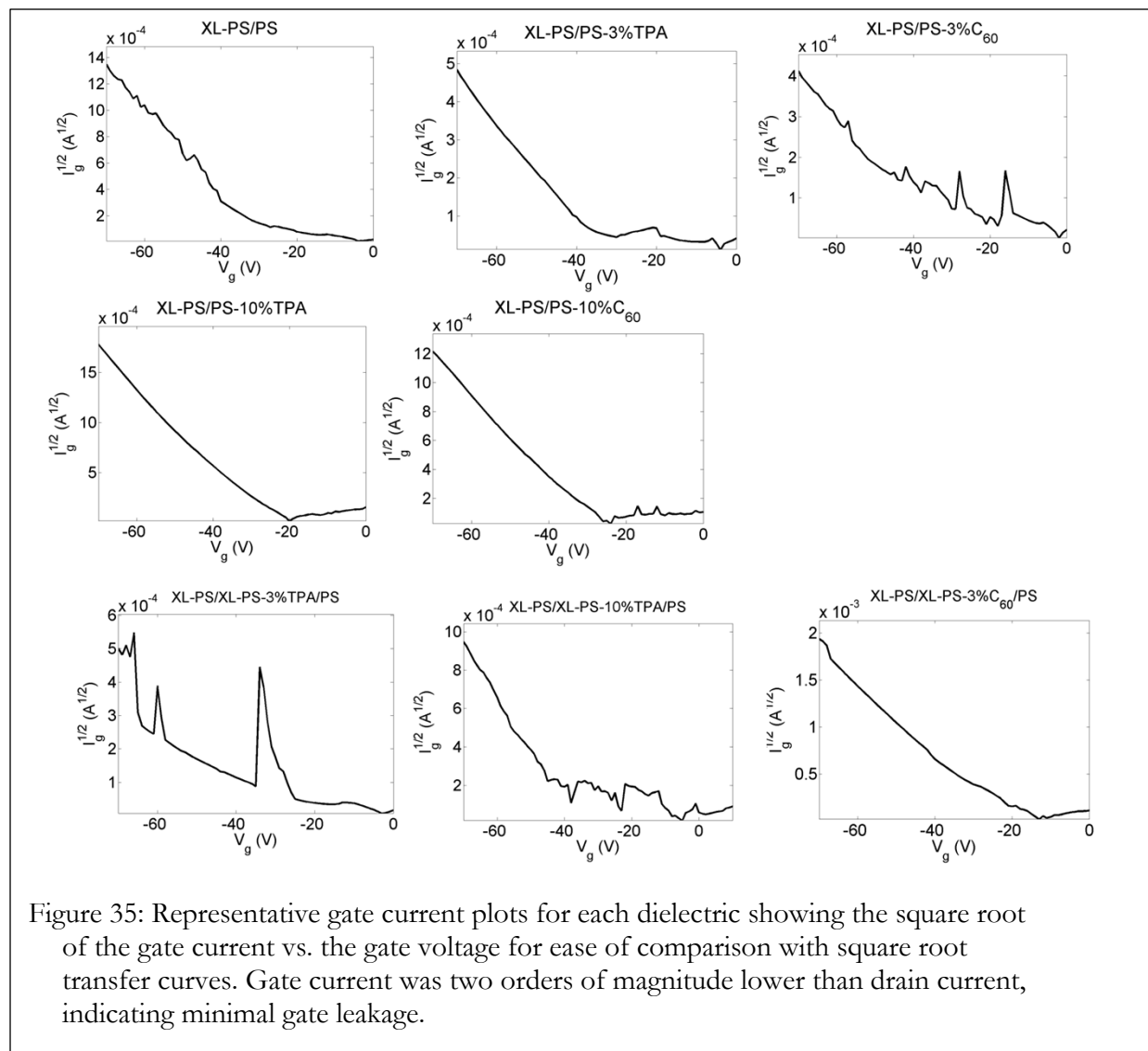
2.3 Multilayer dielectric analysis

NR techniques

NR was done at the National Institute of Standards and Technology Center for Neutron Research, or NCNR, on the Polarized Beam Reflectometer (PBR). Data reduction and model fitting were carried out using the Reflpak and Refl1d software packages, respectively.[95,96] Experiments were facilitated by PBR instrument scientist Brian Kirby and other NCNR staff. Reduction, fitting, and analysis of NR data were done by Evan Plunkett, a student in the Johns Hopkins department of Physics and Astronomy.

SEM and AFM instrument details

Scanning Electron Microscopy (SEM) was used to measure layer thicknesses. SEM images were obtained by Tejaswini Kale, in the JHU departments of Materials Science and Chemistry, using a FEI Quanta 200 Environmental SEM with a cross-sectional sample holder from Electron Microscopy Sciences. Atomic Force Microscopy (AFM) was used to ensure film continuity and measure surface roughness. AFM was obtained using a Veeco MultiMode AFM in tapping mode.

3 Localizing static fields in organic dielectric layers

3.1 Synthesis, fabrication, and characterization

3.1.1 Polymer design, synthesis, and film formation

Polymer synthesis of the substituted polystyrenes was done by Tejaswini Kale and Xin Guo, and polymer design was done by Howard Katz, Xin Guo, and Jasmine Sinha, all from Johns Hopkins Department of Materials Science and Engineering. One important characteristic of the styrene based polymers produced, shown in Figure 36 from reference [3], was their ability to be

crosslinked sufficiently to prevent dissolution of existing films when overlying films are deposited. A copolymer with 10% of the crosslinking functionality cyclobutenostyrene was found to be optimal, giving a smoother film than the copolymer made with 5% cyclobutenostyrene. Chargeable groups TPA and C_{60} were incorporated in 3% or 10% amounts, with or without cyclobutenostyrene crosslinkable units. For samples used in neutron reflectivity studies, the unsubstituted styrene groups were perdeuterated as needed to provide scattering contrast. Crosslinking via divinylbenzene subunits, either using benzoyl peroxide or ultraviolet initiation, was not as effective as the cyclobutenostyrene.

Figure 36: AIBN polymer synthesis schemes for crosslinkable and chargeable PS. The crosslinking functionality is present in 10% concentration, and chargeable functionalities C_{60} and TPA are present in 3% or 10% concentration.
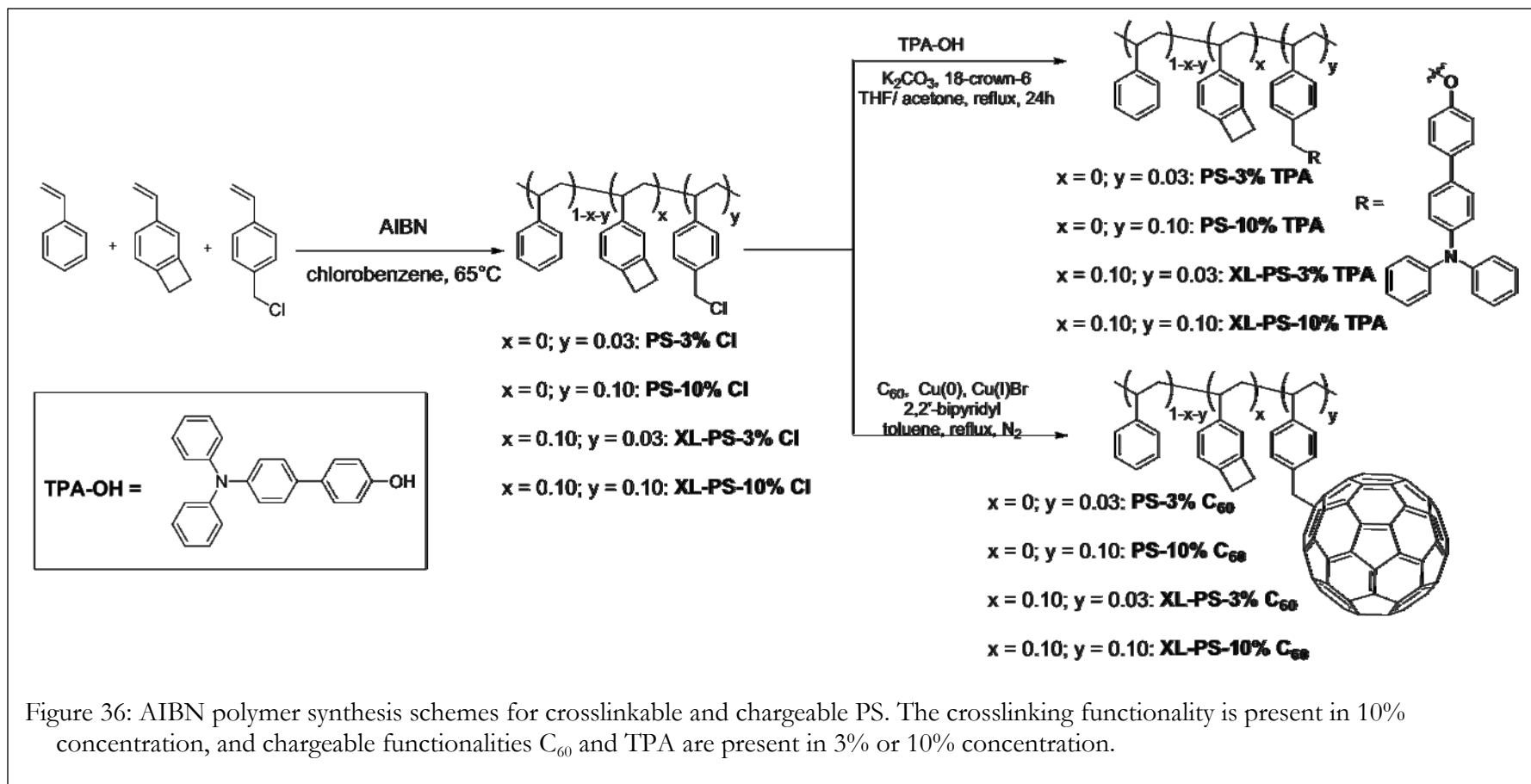
3.1.2   AFM morphology determination

The surface roughness of crosslinked PS (XL-PS) samples was measured by AFM, both to assure film quality of the XL-PS, and to compare with the roughness observed by NR. In general, the roughness seen by AFM was lower than that found by NR for buried interfaces involving these materials, indicating either that the spin coating of subsequent layers causes some modest alteration of the film interface, or that there is some variation in the topography results because of the smaller lateral scales probed by AFM compared to NR. In Figure 37a, the RMS roughness of XL-PS from a 20 mg/mL solution, spin coated on a gold surface was found to be 0.34 nm. In Figure 37b, d_8 XL-PS spin coated from a 10 mg/mL solution on native SiO_2 was found to have a RMS roughness of 0.28 nm. The similarity between the surface roughness of these two films showed that interface quality was not sensitive to the substrate for films in the thickness range used (50 - 200 nm).

Figure 37: Measurements of RMS roughness using AFM of XL-PS films.
  a) 20 mg/mL XL-PS on Au had a roughness of 0.34 nm. b) 10
  mg/mL XL-PS on native oxide had a roughness of 0.28 nm.
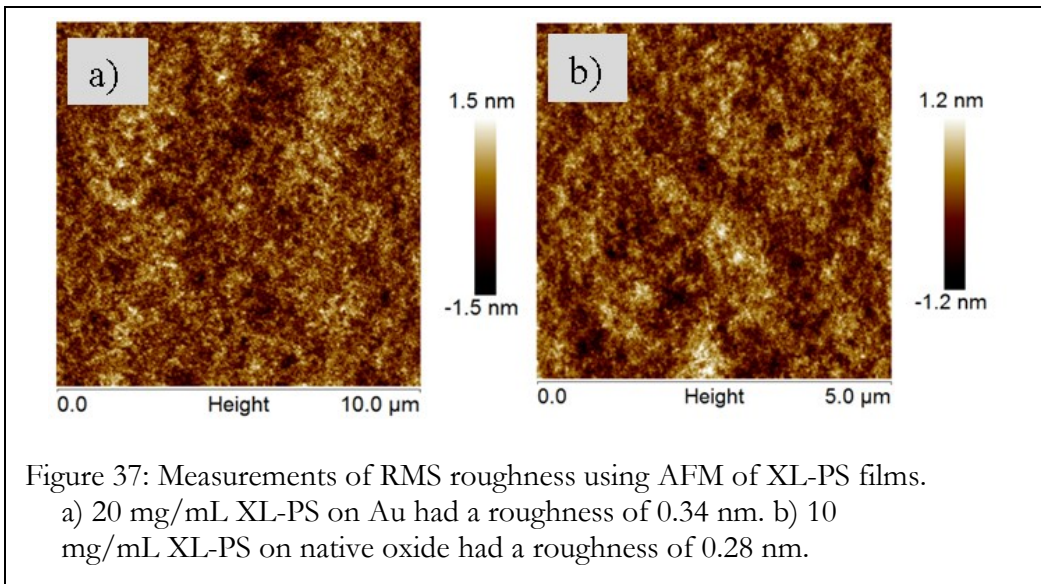
3.1.3   SEM thickness determination

The film thicknesses of the single XL-PS layer and a XL-PS/PS bilayer, both

deposited on Cr/Au substrates, were determined using cross sectional SEM. Figure 38

shows the images obtained for a single layer of XL-PS and a bilayer of XL-PS/PS. The

following was written by T. Kale to describe the SEM experiment: [3]

"… film thickness of a single layer of polystyrene (XL-PS) spin coated from a 20

mg/mL solution was found to be 240.4 ± 5.5 nm (15 measurements on a single sample).

Sharp focusing was difficult due to charging of the film from the electron beam. The Cr/Au

layer was clearly visible as a bright feature on the bulk silicon, and was found to be 36.6 ±

3.3 nm (10 measurements). When a second PS layer was deposited from a 20 mg/mL

solution after cross-linking the first layer, the overall film thickness was found to be 551.1 ±

8.1 nm (11 measurements, Figure 3b). While a sharp contrast between the two polymer films

was not obtained, a distinct region was visible at the bottom of the film which may be the

cross-linked polymer layer. This further corroborates the idea that the integrity of the initially

deposited polymer layer is maintained through the second deposition step. "

Figure 38: Cross sectional SEM of a) XL-PS giving a layer thickness
of 240 nm and b) XL-PS/PS giving a total thickness of 551 nm.
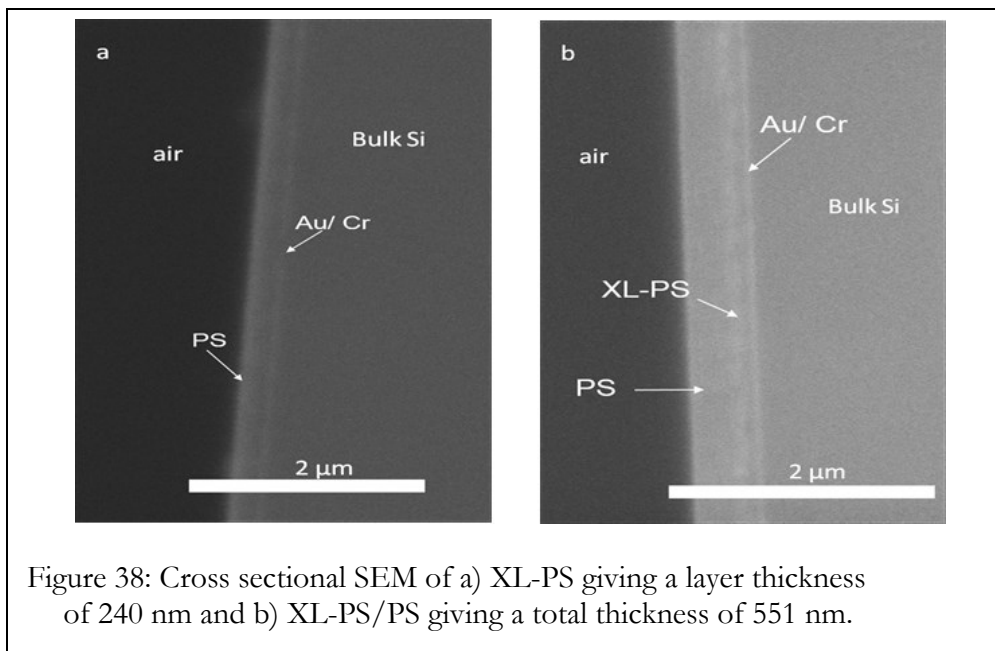
The measured thickness of the bilayer is not exactly twice that observed for the single layer. Though the concentrations of the two solutions and the spin coating conditions were the same, the substrate on which the second layer was deposited was different from the substrate the first layer was deposited. It is logical that the wetting properties and final thickness would also be somewhat different.

3.1.4 Neutron reflectivity

Using NR, layer thickness was measured, and correlated with the concentration of the solution it was spin coated from. This is shown in Figure 39. Interfacial roughness was also measured, and found to be between 1.5 nm and 4 nm, independent of layer thickness. Higher roughness was found for films of PS-C_{60}, compared to PS-TPA. The roughness of the buried interfaces in our work is somewhat larger than that observed for XL-PS / air interfaces observed by AFM, suggesting that some minimal intermixing may occur near the crosslinked layer boundaries. This is perhaps not surprising, as the low cross-linker density

(10%) may still allow for some local flexibility or deformability in the XL layers when exposed to solvents in subsequent spin-coating steps.

These analyses were useful in measuring the properties of the dielectrics used in OFETs (Section 3.2). In XL-PS/PS-* bilayer dielectrics, both layers were spin coated from 20 mg/mL CHCl$_3$ solutions. The crosslinked PS layer was measured at 240 nm thick by SEM and at 125-175 nm thick by neutron reflectivity, indicating the true thickness is likely around 200 nm. The second PS layer was determined by SEM to be approximately 310 nm, but the 20 mg/mL PS on 20 mg/mL XL-PS bilayer was too thick to be measured by neutron reflectivity. Both bilayer and trilayer OFET dielectrics were determined to have a total thickness of approximately 400 – 500 nm based on these measurements.
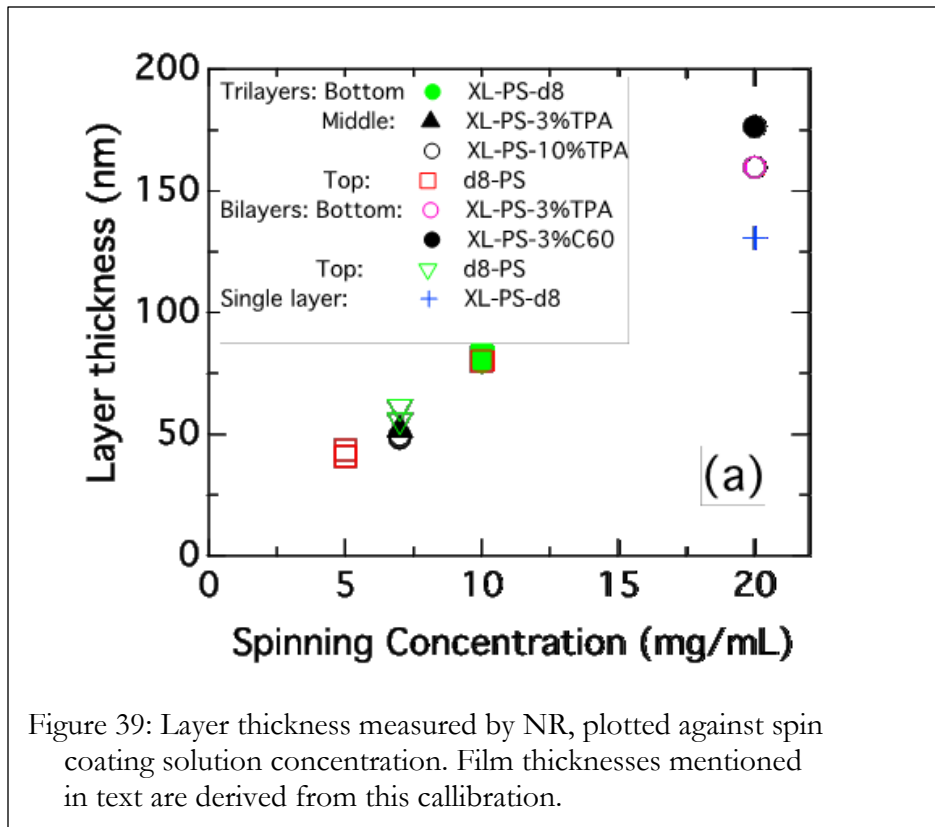
Figure 39: Layer thickness measured by NR, plotted against spin coating solution concentration. Film thicknesses mentioned in text are derived from this callibration.

To test for the possibility that structural changes arising from the charging process could influence the electronic properties of our OFET devices discussed below, reflectivity measurements were made on a set of PS-trilayer samples with either Au or pentacene top layers. NR measurements were made both before and after charging with a removable PDMS electrode. No samples measured exhibited statistically distinguishable changes in their reflectivity post-charging, for charging voltages of up to $\pm$ 70 V. across a total sample thickness of 200 nm or less. The dielectric in OFET structure was twice this thick, meaning it underwent only half the field withstood by the charged NR samples. This implies that charging done during OFET V_{th} shifting experiments does not have a significant impact on the morphology, and any observed effects of charging in devices is not significantly attributable to field-induced change in the dimensions or integrity of the layers.

3.2 Modulation and stability of V_{th} in multilayer dielectric OFETs

The PS-based materials were used as the sole gate dielectrics for pentacene OFETs, without any intervening oxide. The effects of the chargeable groups C_{60} and TPA on OFET charging were observed. The charge trapped in the gate dielectric was measured by comparing the V_{th} of the OFET before and after a charging step. V_{th} is a measure of the free carrier and trap densities in and near the semiconductor channel, which is modulated by local electric fields. Fields produced by bulk polarization or charge trapping in the gate dielectric layer increase or decrease the free carrier density in the OSC. Therefore, at a given gate voltage (V_g), the number of free carriers, and therefore the output current, changes depending on local static fields. In a p-channel pentacene OFET, an electrostatic field oriented with the negative charge layer near the pentacene acts to induce free holes into the channel and decrease the V_{th}, according to the "bias stress" charging mechanism. Here, a

decrease in the magnitude of V_{th}—indicating the device is easier to turn on—is defined as a negative V_{th} shift, and an increase in the magnitude of V_{th} is defined as a positive V_{th} shift.

V_{th} for each device, before and after charging, was calculated from the square root transfer curve. Using a MATLAB script written for this purpose, a straight line was fit from data taken between gate voltages V_g of -70V and -50V, shown in Figure 40a for an XL-PS/PS-C_{60} OFET and Figure 40b for a XL-PS/PS control, along with the structures of each. V_{th} was defined as the x intercept of this line. Extrapolation to the x-axis is one of the main methods of calculating threshold voltage seen in the literature.[23] The V_{th} shift following charging was determined by subtracting V_{th} of the original OFET from V_{th} after charging. ±70 V was used for charging, as this was the highest voltage at which breakdown rarely occurred, keeping in mind that the device architecture does not include any protective oxide barrier layer in series with the polymer dielectrics.

The threshold voltage shifts observed were consistent with the bias stress mechanism for charging in a dielectric, where charges with the sign of the charging voltage are injected into the dielectric/OSC interface. An increased V_{th} shift was found following charging devices with substituted PS, particularly PS-TPA, next to the pentacene. In Figure 40, an increase of 15V was seen following charging the XL-PS/PS-10%TPA device, but in the XL-PS/PS control device V_{th} increased only 3V.
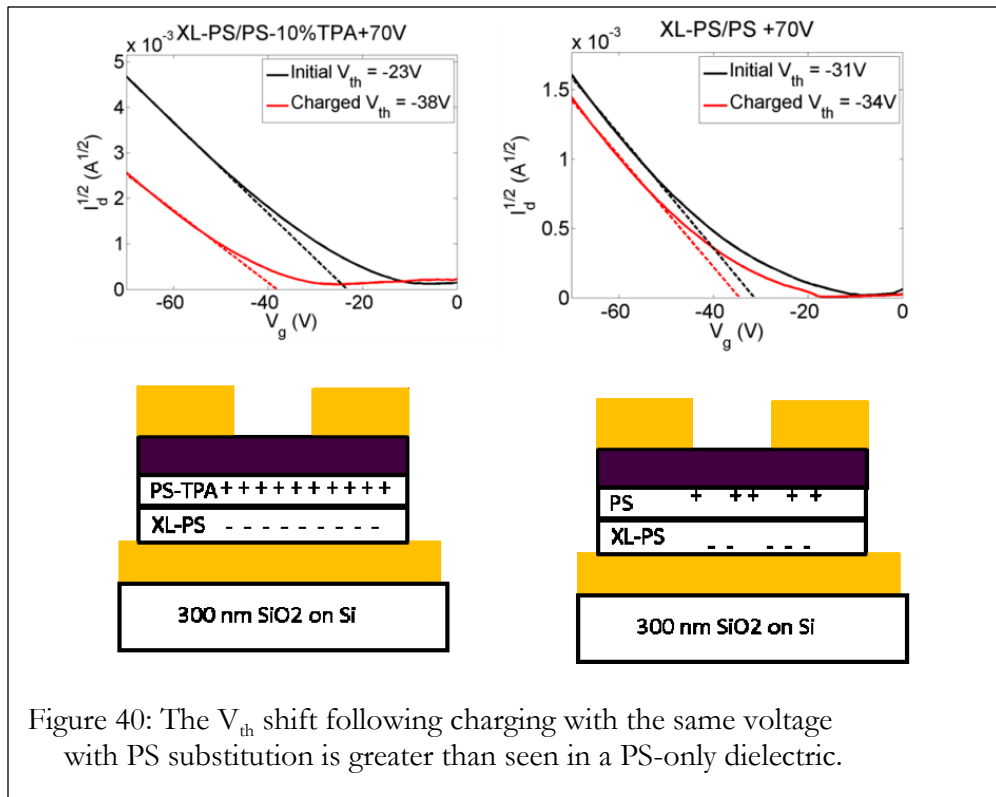
Figure 40: The V_{th} shift following charging with the same voltage with PS substitution is greater than seen in a PS-only dielectric.

Output curves for the multilayer dielectric OFETs generally showed extremely flat saturation regions and the excellent agreement between maximum currents obtained using the transfer and output voltage sweep modes, both of which indicate reliable OFETs. Figure 41a shows the square root transfer curves of a XL-PS/PS-10%TPA device before and after charging with -70V. Output data from the same device are shown before and after charging in Figure 41c and Figure 41d. The decrease of 15V in the Vth increases the maximum output current seen from 3 μA to nearly 7 μA, indicating a shift of the transfer curve towards zero following charging.

Figure 41b shows the square root transfer curve of a XL-PS/PS-10%C_{60} device before and after charging with +70V. The threshold voltage shift was an increase by 6V. Maximum V_{th} shifts for this structure were smaller than those seen in XL-PS/PS-TPA devices.

Figure 41: a) V_{th} of XL-PS/PS-TPA decreases by 15V following charging. b) XL-PS/PS-C_{60} shows smaller V_{th} shifts. c) and d) output of device in a) before and after charging, showing an increase in I_d consistent with the charge trapping mechanism.
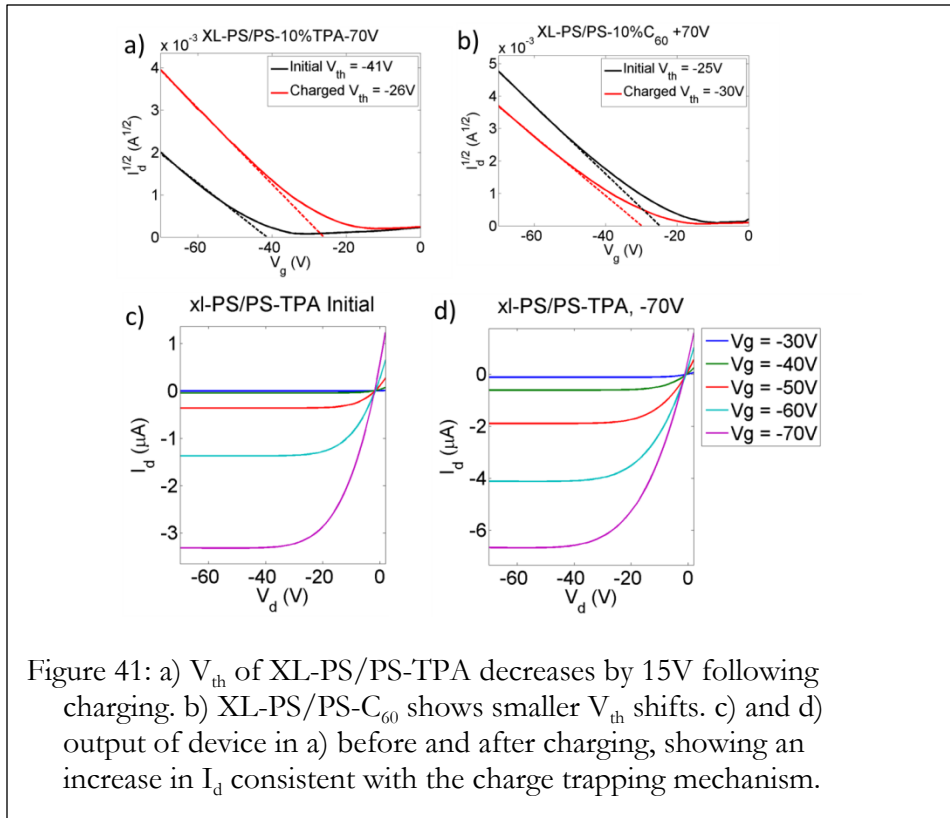
V_{th} shifts in two types of systems were investigated. The first had a bilayer gate dielectric composed of a crosslinked layer deposited on the gate electrode, covered by a non-crosslinked layer adjacent to the pentacene film. We obtained the baseline shifts from unsubstituted PS control devices, using a bilayer of unsubstituted PS deposited on crosslinked PS (referred to here as XL-PS/PS). V_{th} shifts seen here are a measure of the charge trapping of PS alone. Then, substituted PS was used as the top dielectric layer in OFETs to measure the effect of substituents on charge trapping capability. For these, substituted PS was deposited as the top layer over XL-PS. The substituents were present in the polymers at either 3% or 10% concentration. The V_{th} shifts upon charging these devices were larger and variable for both PS-TPA and PS-C_{60}, with differences seen between positive

and negative charging, as well as between the two materials. A histogram illustrating the threshold voltage shifts seen for each set of devices is shown in Figure 42.

Figure 42: Bilayer dielectric V_{th} histograms. XL-PS/PS-TPA has the largest shifts, and also the largest range of shifts between fabrication batches.
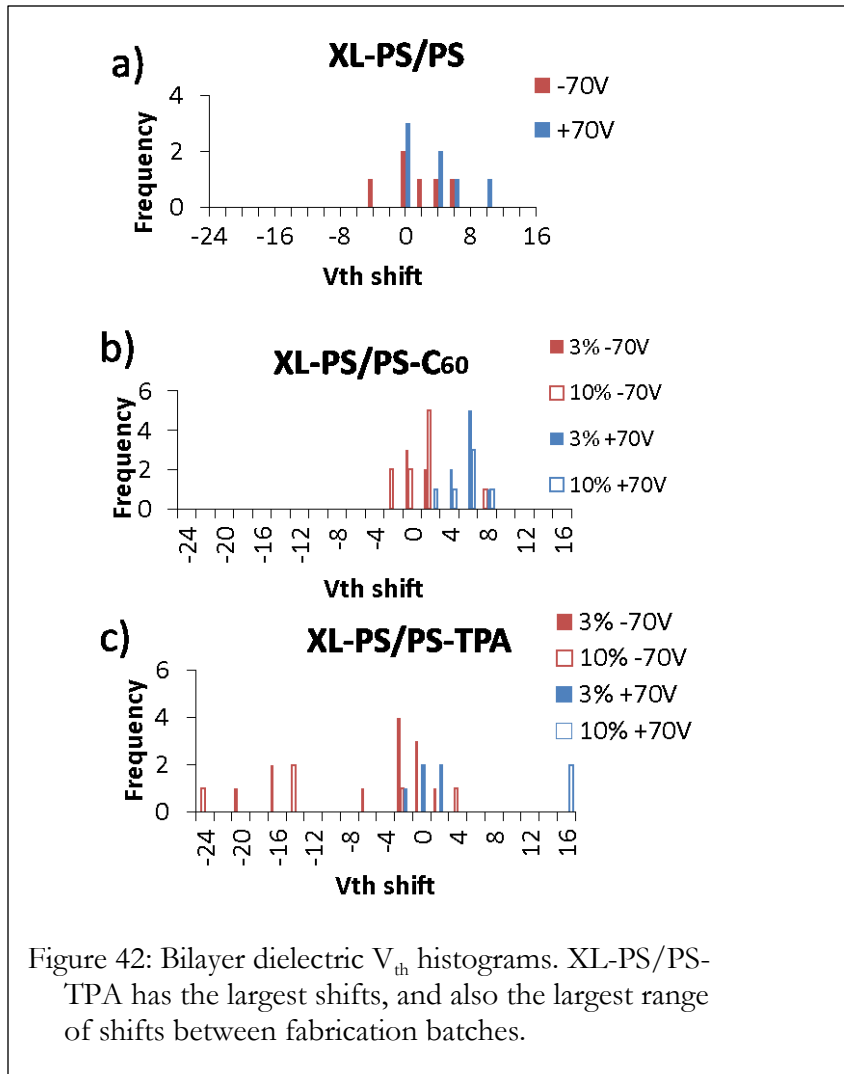
The bilayer dataset indicates that charging PS-only films gives small and inconsistent V_{th} shifts where the polarity of charging does not have a strong correlation with the sign of the V_{th} shift. The somewhat more systematic charging (most shifts are zero or positive) seen when charging with positive voltages could be from one of two causes. Because the voltage is applied to the top surface of the dielectric through a pentacene film, it could be that positive voltages are more easily transferred through the pentacene than negative voltages.

The other possible explanation is that traps in the bottom crosslinked PS layer accept negative charges more easily, or the top PS layer accepts positive charges more easily.

In general, with the C_{60} functionality, there was no difference in charge-capturing performance between those with 10% and with 3% functionalization, as seen in Figure 42b, but with the TPA functional group, 10% TPA resulted in more frequent large V_{th} shifts, as seen in Figure 42c. When comparing positively and negatively charged samples in Figure 42c, negative charging gave large shifts more frequently than positive charging. This could indicate that PS-TPA accepts negative charges more readily than it accepts positive charges, unlike what was observed for pure PS films in the control samples. The directions of these top-chargeable layer V_{th} shifts are overwhelmingly consistent with bias stress effects, except for C_{60} with negative charging, which showed little effect in either direction. The range of results seen for XL-PS/PS-TPA was thought to have resulted from occasional charge dissipation from the TPA into the pentacene, and/or some form of substituent clustering that is required for large V_{th} shifts. The latter would be consistent with the observation that large shifts occur more frequently for PS-10%TPA than for PS-3%TPA.

In addition to studying bilayers with substituted PS on top of unsubstituted, crosslinked PS, we studied bilayers made with unsubstituted PS on top of substituted, crosslinked PS. The difference here was whether the substituents C_{60} or TPA were next to the pentacene layer or next to the gate electrode. When the substituted PS was on the bottom layer, next to the gate electrode, all threshold voltage shifts following charging were under 3V, out of 14 devices. When comparing this to the V_{th} shifts seen in Figure 42b and Figure 42c, where the substituted PS was on top, it is clear that placing the substituted PS adjacent to the pentacene resulted in a larger V_{th} shift, particularly in the XL-PS/PS-TPA

devices. When comparing with Figure 42a, which did not have any substituents, it is possible that somewhat smaller V_{th} shifts are seen in the bilayer with substituted PS next to the gate. It is possible that putting substituted PS near the gate has decreased the bias stress susceptibility of the device, but more work is required to fully examine this possibility.

The second type of systems V_{th} shifts were investigated in was OFETs with trilayer dielectrics, with the middle PS layer substituted with either C_{60} or TPA, and the outer layers without these substituents. They were studied both in an attempt to prevent charge dissipation into the pentacene, which could have contributed to the large range of results seen in Figure 42c, and to accomplish the initial goal of positioning a layer of charges a fixed distance from the pentacene. The first layer was crosslinked PS spin coated from a 20 mg/mL $CHCl_3$ solution. The middle layer was spin coated from a 15 mg/mL $CHCl_3$ solution of crosslinked, substituted PS (e.g. XL-PS-C_{60}). From Figure 39, which plots spin coating concentration versus NR-determined thickness, the thickness of these films may be interpolated to be approximately 125 nm. Likewise, the top layers of PS spin coated from 5 mg/mL $CHCl_3$ solutions may be seen to be approximately 50 nm thick. The final structures, along with V_{th} shifts with charging, are shown in the schematic in Figure 43.

Figure 43: OFETs with trilayer dielectrics with substituted PS as the middle layer showed high stability of V_{th} to charging, indicating bias stress resistance.
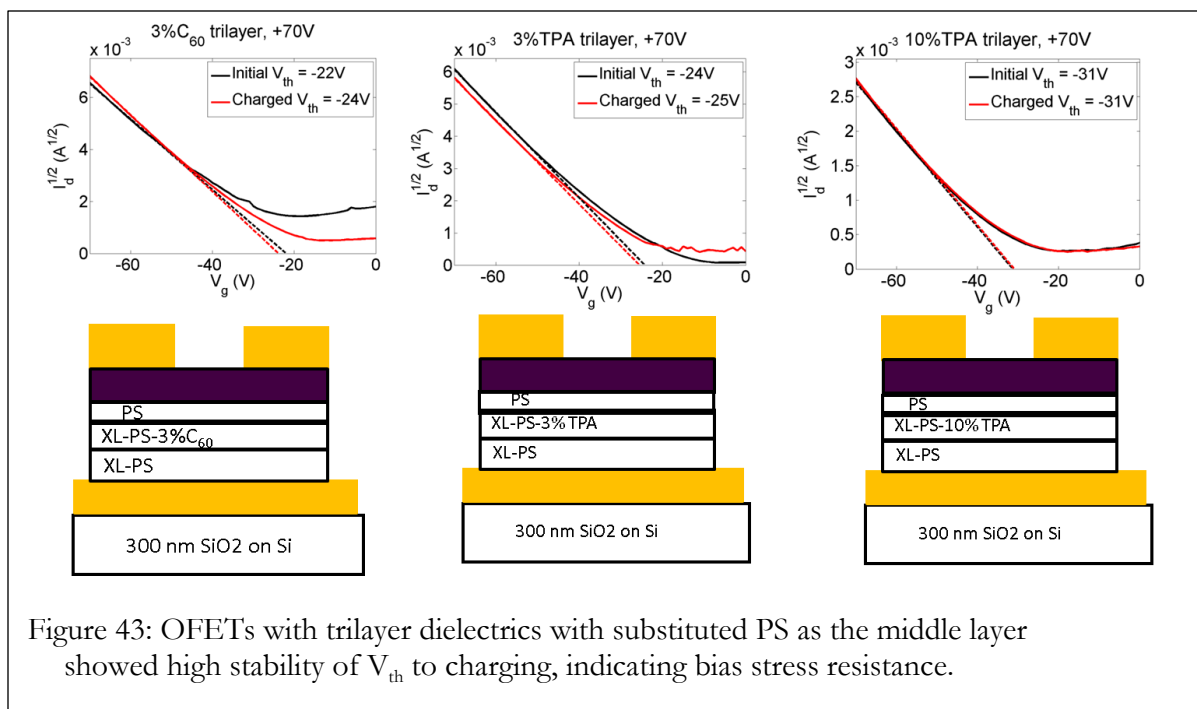
The threshold voltage shifts upon charging these devices were much smaller, smaller even than those seen in the XL-PS/PS bilayer devices. In addition to having smaller Vth shifts, the trilayer devices also had a small range of Vth shifts, compared to that seen in the bilayer dielectric with substituted PS on top. For XL-PS/XL-PS-TPA/PS, a moderate difference between the devices made with XL-PS-TPA with 10% TPA substitution, and those made with 3% substitution was noted: all V_{th} shifts of magnitude 1V or greater occurred in devices made with 3% XL-PS-TPA as the middle layer, as shown in Figure 44a. Also, devices with 10% TPA as the middle layer show essentially zero V_{th} shift when charging with + or -70V. XL-PS-C_{60} with 10% substituents was too insoluble to make devices.

An important goal of organic transistor bias stress investigations is to build a device that is not subject to V_{th} shifting, as stated in the introduction. A likely mechanism for the

88

present result, involving compensation of interface charge effects by charging of the middle layer, is discussed in more detail below.

Figure 44: Trilayer histograms of frequency of V_{th} shift ranges show less variability and significantly smaller shifts than bilayer dielectrics did.
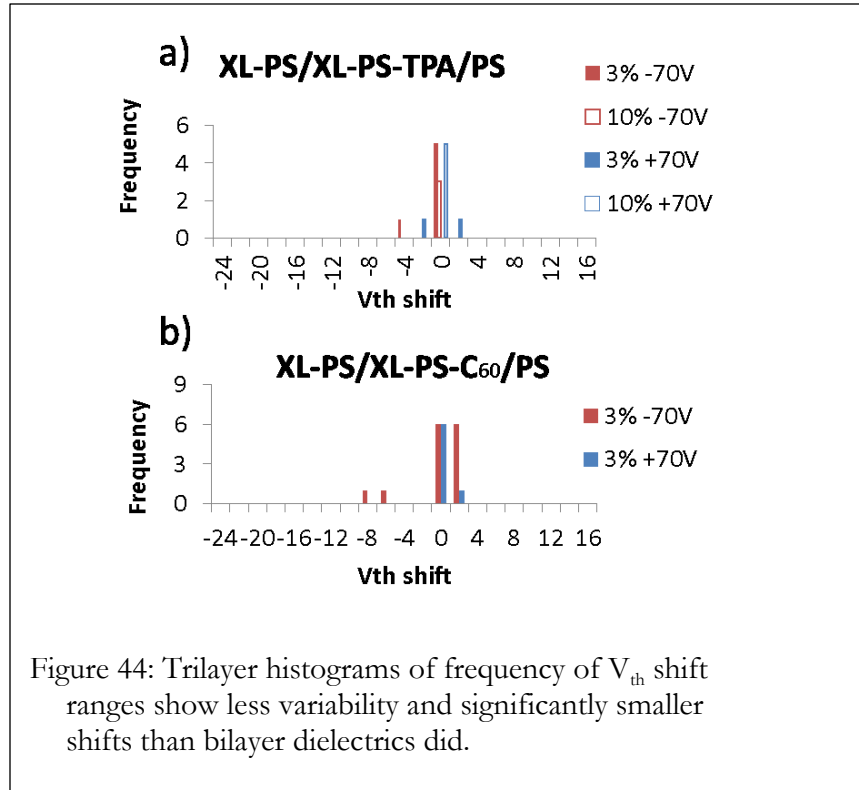
Because of the interdependence of field effect mobility and capacitance, there was the concern that differing capacitance of the dielectrics lead to significantly different charge transport behavior in the OFETs. To answer this question, the capacitance of several bilayer and trilayer dielectrics was measured at 1 kHz after charging and OFET testing, using a voltage of 500 mV. The relative permittivities ε_R were calculated, as enumerated in Table 4.

Multilayer (400 nm thickness)	C_i (nF/cm^2)	ε_R
PS (C_i calculated from typical ε_R)	5.3-6.6	2.4-3.0 typical
XL-PS/PS	5.4	2.4
XL-PS/PS-3%C60	5.7	2.6
XL-PS/PS-3%TPA	5.7	2.6
XL-PS/PS-10%TPA	9.8	4.4
XL-PS/XL-PS-10%TPA/PS	8.9	4.0
XL-PS/XL-PS-3%C60/PS	8.8	3.9

Table 4: Representative relative permittivities of bilayer and trilayer dielectric films.

For several of the samples, the capacitance is in good agreement with the reported values for PS. Capacitances 30-50% higher than that of PS were seen in both the XL-PS/PS-10%TPA and in the trilayer dielectrics. In the former case, it could be from an increase in percent of polarizable species (i.e. 10% TPA compared to 3%), which may increase the polarization response of the film to the applied voltage. In the case of the capacitance of a trilayer dielectric, the additional interface and the substituted middle layer may be locations of increased polarizability. Further work is needed to determine the contributions to the polarizability and chargeability properties of multilayer dielectrics.

To determine if the variation in ε_R between dielectrics was responsible for a change in mobility of the OFETs, which might lead to differing V_{th}, mobility was also calculated. No strong relationship was seen between the mobility for a specific dielectric and its measured capacitance. The devices all show a range of mobility dependent on the quality of the evaporated pentacene film, and vary from batch to batch somewhat. The highest mobilities

seen were in the 3% TPA bilayer, over many sets of sample fabrication, and the 3% C_{60}

trilayer, neither of which had exceptionally high or low ε_R.

4   Discussion and conclusions

We propose that different V_{th} shift mechanisms are active in bilayer devices

compared to trilayer devices. In bilayers, the dominant charging mechanism appears to be

charge trapping near the OSC/dielectric interface. The most probable direction of V_{th} shift,

to increase the V_{th} with positive charging and decrease it with negative charging, confirms

this. In the trilayer devices, however, we not only see a decreased magnitude of V_{th} shift

from dielectric insulation between the charged layer and the OSC, but also see a very tight

range of V_{th} shifts, surrounding zero, as opposed to the much larger range of probable V_{th}

shifts in devices with substituted PS as the top of the bilayer dielectrics. We believe the large

range seen in bilayers is caused by the statistically-driven probability of grouping multiple

substituents together at the surface near the pentacene. When substituents are buried or

over-diluted, they cannot lead to the consistent charge trapping required to shift the energy

levels at the pentacene interface. A cluster of substituents may be needed for the extra

trapping beyond that done in the PS-only control. The more frequent large shifts observed

in 10% TPA compared to 3% TPA top layer OFETs is consistent with this. This effect was

not observed in 3% vs 10% C_{60} substituted PS, which is logical since the C_{60} molecule is

much larger and may not be able to form clusters at the dielectric/OSC interface.

The greater effect of negative charging relative to positive charging at PS-TPA is

somewhat counterintuitive considering that TPA is nominally an electron donor. However,

there is the possibility that some fraction of the TPA becomes ionized in the course of

91

sample preparation, and its neutralization during the charging process results in a net negative charge. Another possibility is that TPA aggregates form traps that stabilize negative charges through local polarization. The use of more strongly electron-donating side chains at even higher concentrations in future work should clarify this issue. The frequent negative shifts seen with TPA also point to an eventual route to nonvolatile tuning of V_{th} for lower voltage OFET operation with the use of stronger electron-donor side groups.

On the other hand, if the mechanism for charging the middle of a trilayer is polarization rather than charge injection, it is not necessarily susceptible to this clustering effect. Alignment or formation of dipoles in the polymer matrix will likely not depend on substituent clustering in the way that the charge trapping mechanism does. Note that if trilayer charging effects were the result of a simply diluted effect analogous to what was seen with bilayers because of more difficult charge injection into the middle layer, the V_{th} shifts would still have been in a consistent direction. However, instead we observe V_{th} shifts in the trilayers that are non-directional in addition to being very small.

We propose that during charging the trilayer structure, both bias stress and dielectric polarization charging mechanisms occur, as is illustrated in Figure 45. Charges are injected into the semiconductor/dielectric interface, and a dipole involving the middle layer is also formed. These effects counter each other, resulting in little or no net change of the threshold voltage. The insulator/semiconductor interface is still charged by the addition of net static charge via filling of traps or creation of new traps—this happens, for example, for charging with negative voltage on the semiconductor, by injecting negative carriers into the semiconductor/dielectric interface. Since the semiconductor/dielectric interface of the

trilayers does not have substituents, the baseline level of charge trapping occurs, as was observed with the unsubstituted PS dielectrics.
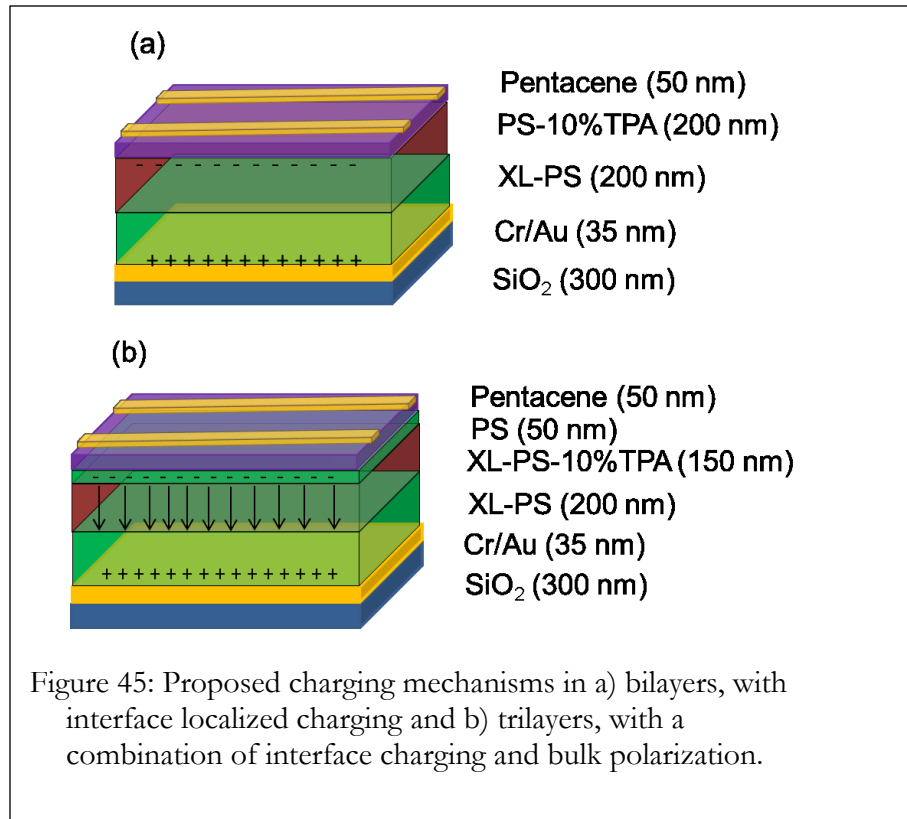
Figure 45: Proposed charging mechanisms in a) bilayers, with interface localized charging and b) trilayers, with a combination of interface charging and bulk polarization.

One remaining question is why bulk dipole formation does not seem to occur in bilayers, as we are hypothesizing for the trilayers. In a bilayer, there are three relevant interfaces. Two are directly in contact with electrodes, and one is between dielectric layers. In a trilayer, there are four relevant interfaces. Interfaces are likely locations for charge traps and defects, and the additional interface in the trilayer structure may create another layer of charges that can act on the middle substituted PS layer.

Acknowledgement and disclaimer

CHAPTER IV: Improved Polymer Dielectrics for Organic Electronics

1   Introduction

Using the OFET and lateral junction structures presented in the previous chapters, two dielectrics besides polystyrene have been analyzed in an effort to improve field effect mobility and decrease bias stress. First, poly(trifluoromethyl-styrene) (PTFMS) was synthesized, and examined for its use as a dielectric that will have lower bias stress than polystyrene. Fluorinated dielectrics are known to reduce bias stress by decreasing the trap density at the OSC/dielectric interface. [29] However, the hydrophobicity of purely fluorinated polymers can also change the morphology of layers deposited on top of them. A partially fluorinated polymer might be thought to combine the low trap density of perfluorinated materials with easy processing of less hydrophobic polymers. Both the 2- and 3- substituted PTFMS were synthesized, shown in Figure 46.

Figure 46: Structures of poly(2-trifluoromethyl styrene) and poly(3-trifluoromethyl styrene).
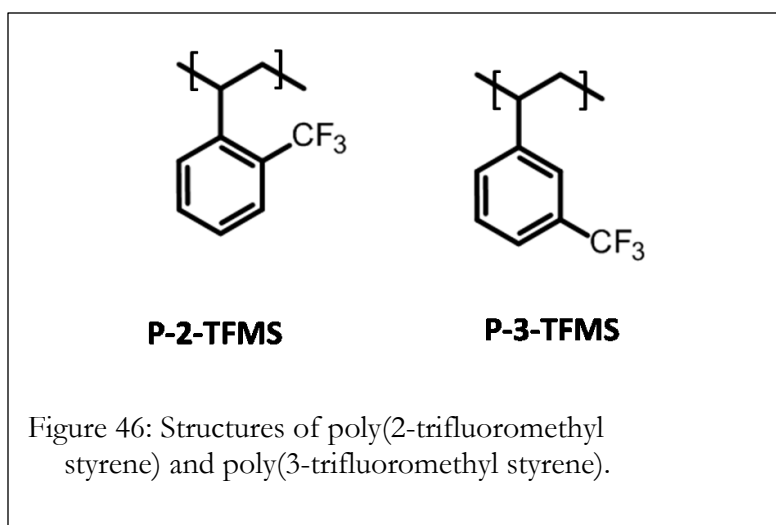
Poly(benzyl methacrylate) (PBMA, structure in Figure 47) was studied due to its potential for improved surface morphology compared to PS. Improved surface morphology of the dielectric can decrease trap densities at the interface to decrease bias stress and increase field effect mobility. The heteroatoms in PBMA increase the polarity and the hydrophilicity, which improves processing and final film quality.

Figure 47: Structure of poly(benzyl methacrylate)
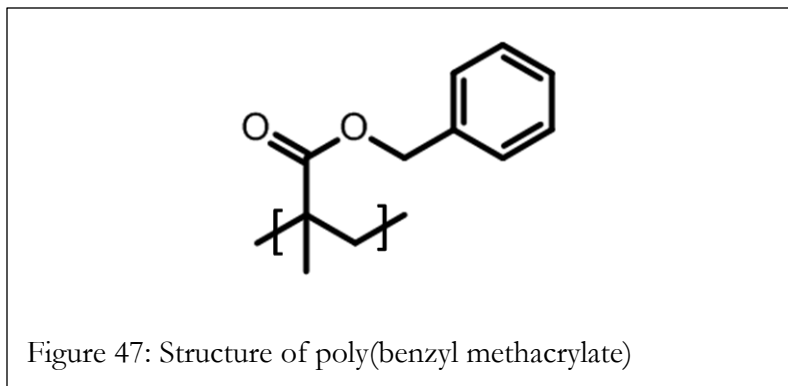
PBMA was compared to PS as a gate dielectric for pentacene OFETs. Additionally, OFETs were made on PBMA with other semiconductors. Adding more conjugated rings to pentacene is known to improve mobility. While hexacene, pentacene with an additional conjugated six membered ring, has been seen to have a mobility of nearly 1 cm^2/V s, it is unstable when exposed to light.[9] It has been determined that by adding heteroaromatic rings to polyacene bases, improved mobility can be obtained while air and light stability is maintained.[97] Two examples of these molecules are diphenyl [1]benzothieno[3,2-b][1]benzothienophene (DPh-BTBT) and dinaptho[2,3-b:2',3'-t]thieno[3,2-b]thiophene (DNTT), with their structures pictured in Figure 48 along with pentacene.

Figure 48: Pentacene compared with DNTT
and DPh-BTBT, two heteroaromatic
small molecule OSCs.
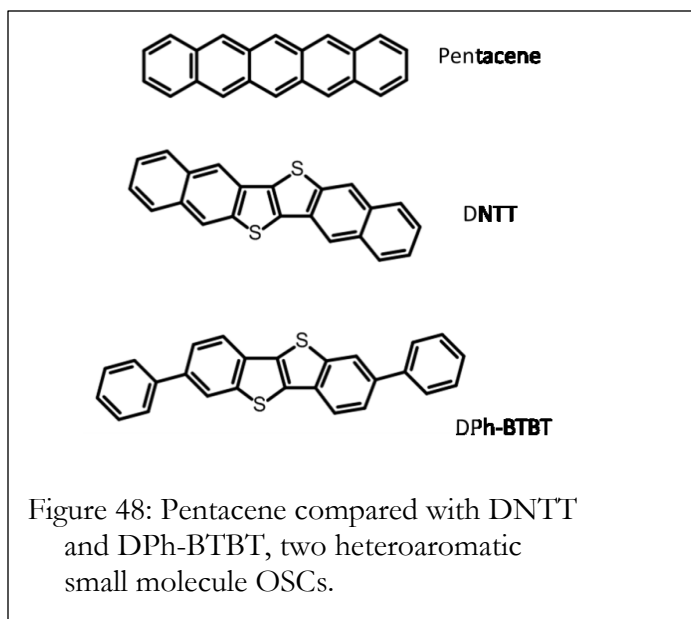
2 Methods

Many of the methods used for the device fabrication and analysis done in this chapter have been presented in previous chapters, so are not repeated here.

2.1 Thermally initiated polymerization of 2- and 3- trifluoromethyl styrene

The synthesis of P-2 and P-3-TFMS was developed starting with the protocol seen in reference [98]. The yield of polymerizing from a neat solution was found to be higher than the yield from methods involving solvent and initiators. To increase the yield further, the 3-TFMS monomer was filtered through basic alumina to remove the inhibitor. To assure the purity of the final product, $CHCl_3$ was used as a solvent instead of acetone. Also, while P-2-TFMS precipitated from methanol, P-3-TFMS was found to have high solubility in methanol, so instead was precipitated from a water/methanol mix. Purification was done by dissolving the product in chloroform and precipitating again from the water/methanol mix.

Figure 49: Scheme of the thermally initiated polymerization of 3-TFMS.
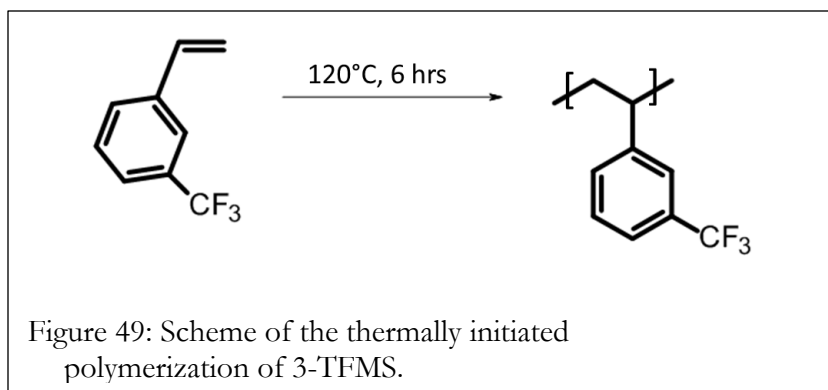
Both the 2- and 3- trifluoromethyl styrene monomers were polymerized here without solvent or initiator, using only thermal initiation. Basic alumina was used to remove the 4-*tert*-butylcatechol, added as an inhibitor, from the 3-trifluoromethylstyrene monomer (CAS# 402-24-4). To do this, the plunger was removed from a 6 mL syringe, and the syringe body was fitted with a 0.45 um pore size PTFE syringe filter. An approximately 3 mm thick layer of basic alumina (CAS# 1344-28-1) was poured into the syringe. 1 mL (1.16g) 3-trifluoromethylstyrene pipetted into the syringe body, and the syringe plunger was replaced and depressed. The filtered monomer was added along with a stir bar to an airtight glass tube fitted with a Teflon screw cap.

The monomer was degassed by either freezing the monomer with liquid nitrogen, followed by three cycles of nitrogen/vacuum purging, or sealing the tube with parafilm and positioning a long needle so nitrogen could be bubbled for 15 minutes without significant monomer evaporation. Following degassing, the tube was sealed with the Teflon cap and stirred at 120°C for 6 hours. The product was dissolved in a small amount of $CHCl_3$ and precipitated from a ~20:1 $MeOH:H_2O$ mixture. To purify, it was dissolved and re-precipitated once, and was found to be pure by NMR. P-3-TFMS yielded 0.8 g (69%) of

white solid. When the inhibitor is not removed before polymerization, in the case of P-2-

TFMS the yield was 30%, but whether that was a function of the presence of the inhibitor or

the different monomer is not clear.

The polymer was determined to be free of monomer by NMR. Gel permeation

chromatography (GPC) was used to determine the degree of polymerization of the final

polymer. Figure 50 shows the trace of the GPC obtained. The weight average molecular

weight (Mw) obtained was 191 kDa, and the polydispersity index (PDI) was 1.77. From the

former value, the degree of polymerization is obtained by dividing Mw by the mass of one

monomer, 172 Da. This gives the average degree of polymerization as approximately 1,110.

From the PDI, we can see the relative uniformity of the polymers. Perfectly uniform sample

of polymers with all the same length would have a PDI of 1.0, and radical polymerizations

frequently result in PDI between 1.5 and 2.0.

Figure 50: GPC of P-3-TFMS showing a broad
peak with retention times 10-15 minutes
corresponding to a Mw of ~191 kDa.
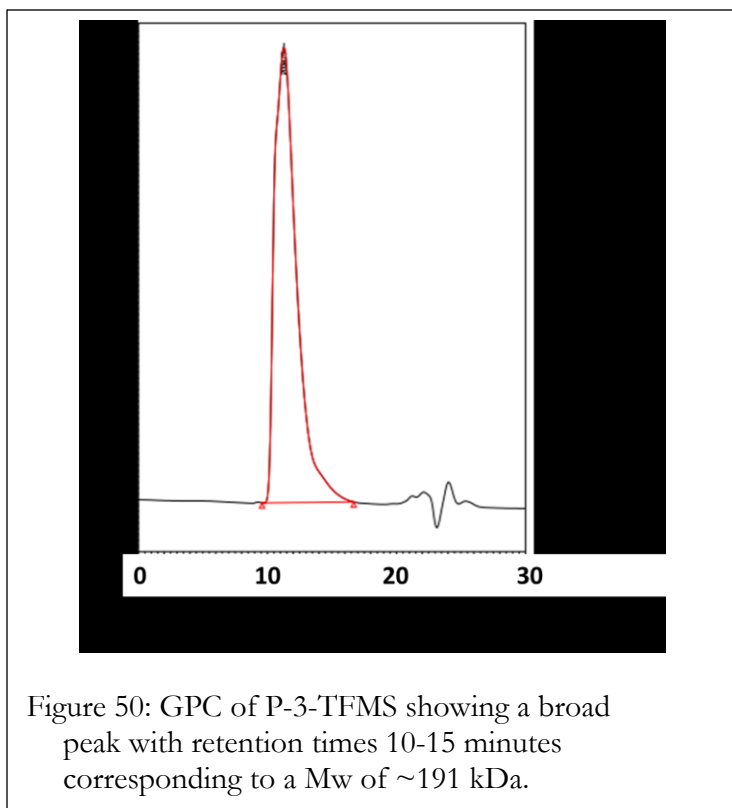
2.2   Fabrication of lateral two-dielectric OFETs

Fabrication of lateral OFETs was done using the same method used for analysis of lateral p-n junctions, with the difference that two interfaces were made rather than one. Bottom contact gate, source, and drain electrodes were deposited on 300 nm SiO_2 on Si. The initial dielectric, either PS or PTFMS, was spin coated, followed by CYTOP and S-1813. The first interface was positioned approximately 1/3 of the way from the gate electrode to the source/drain electrodes. Following the dry etch step, the second dielectric was spin coated, and the CYTOP was removed, exposing the first interface. CYTOP was then spin coated over the sample again, followed by S-1813 and a second round of patterning by lithography. This time, the interface is placed approximately halfway between the first interface and the source/drain electrodes. Finally, pentacene was deposited and CYTOP was removed. The structure is shown in Figure 51.

Figure 51: Lateral OFET electrode geometry. L = 40 μm
and W = 50 nm, which is the thickness of the
pentacene layer.
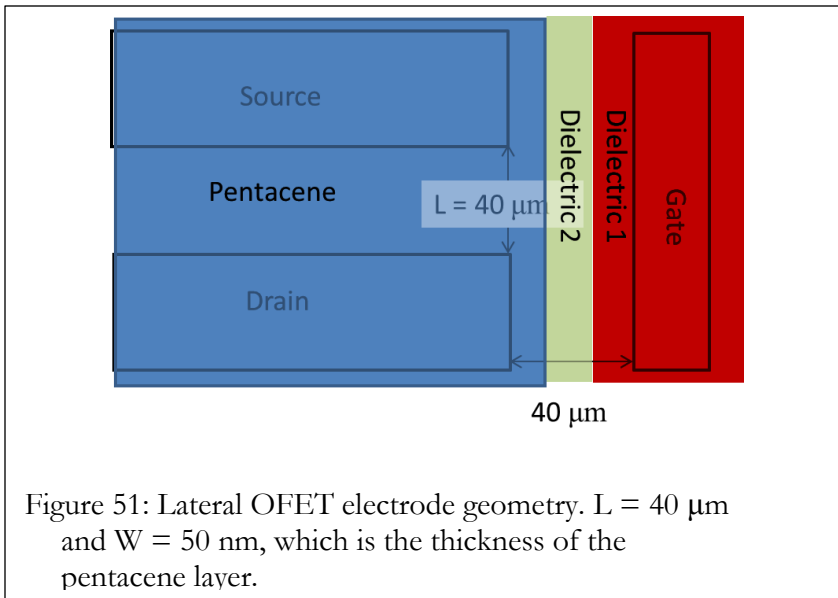
2.3   Fabrication of gold gate OFETs

To compare PS and PBMA as gate dielectrics, fabrication techniques presented in Chapter III were used, with the difference of depositing only one layer of gate dielectric rather than multiple layers. Following deposition of the Au gate electrodes, a 100 mg/mL solution of PS or PBMA was sonicated at 30°C for 60 minutes, then filtered through a 0.2 or 0.45 µm pore PTFE syringe filter into a second vial. PS was spin coated from CHCl$_3$ at 1500 rpm for 60 seconds, with no annealing. PBMA was spin coated from anisole for 5 seconds at 500 rpm, followed by 60 seconds at 2500 rpm. The PBMA was annealed at 80°C for 60 minutes. 15 or 50 nm Pentacene or DNTT was deposited at 0.1-0.3 Å/s. Gold source/drain electrodes were then deposited through a shadow mask. The device schematic for the individual gate, single layer dielectric OFETs is shown in Figure 52.

Figure 52: Diagram of an individual gate, single layer dielectric OFET.
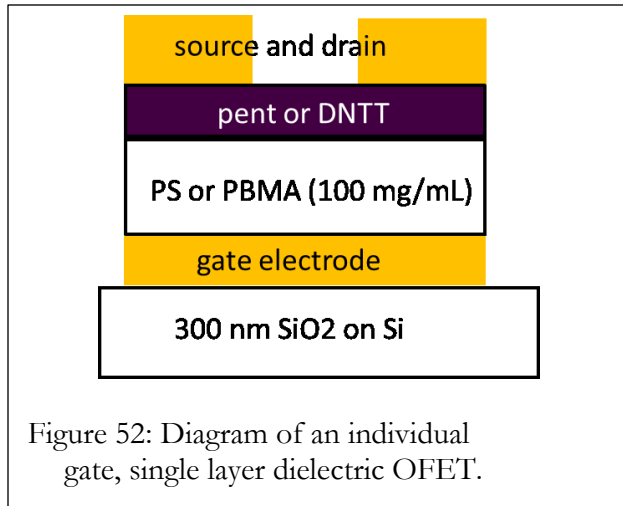
3   Improved polymer dielectrics for organic electronics

3.1   Bias stress and charging in PTFMS

P-2-TFMS has been shown to have decreased bias stress propensity in a lateral OFET architecture by Dawidczyk et al.[57] In that experiment, lateral OFETs were made,

using P-2-TFMS, synthesized as above, and PS as gate dielectrics. The lateral OFETs were initially scanned with SKPM to observe the initial distribution of potentials, and then run as an OFET. The SKPM scan was repeated to observe the static charge distribution in the gate dielectrics that built up as the OFET was run. Positive charge built up in the dielectric, corresponding to bias stress on the OFET that would lead to the device turning more off. The PS dielectric was seen to have a larger amount of static charge built up as the OFET operated, distributed throughout the PS. The P-2-TFMS dielectric had a much smaller accumulation of static charge, indicating lower bias stress susceptibility. However, it also had a lower capacity for charge trapping than PS when the device was purposefully biased to shift V_{th}. In order to have a dielectric that both can stably shift Vth by charge capture and also have decreased bias stress, it would be beneficial to combine the charge trapping property of PS (or similar dielectrics discussed in Chapter 3) with the bias stress resistance of partially fluorinated materials such as PTFMS.

To study this further, lateral pentacene OFETs with layered dielectrics were made, with PS and P-2-TFMS as the two dielectrics. A similar experiment as that described above was run, with the difference that no surface potential scan was taken before the OFETs were run. The initial SKPM scan was taken of the lateral OFET following measurement of output characteristics. Then, the OFET was charged by application of a voltage on the source and drain electrodes, while grounding the gate electrode, for 10 minutes. A second SKPM scan was done, followed by a second measurement of output characteristics.

Two types of sample were made, one with P-2-TFMS adjacent to pentacene, and one with PS adjacent to pentacene.

It was observed in the latter device, 'PTFMS-PS', shown in Figure 53, that after operating the device, a quantity of positive charges were trapped in the PS gate dielectric adjacent to the pentacene. This is an illustration of bias stress, as positive charges trapped in the dielectric will, over time, cause the OFET to turn more off. The lateral OFET was then charged by applying -20V to the source and drain electrodes, while grounding the gate electrode. PS readily traps negative charges, as had been seen previously.[56,57] The PTFMS layer retains a relatively more positive voltage.

Figure 53: Surface potential of lateral PTFMS-PS gate dielectric OFET, a) before and b) after charging.
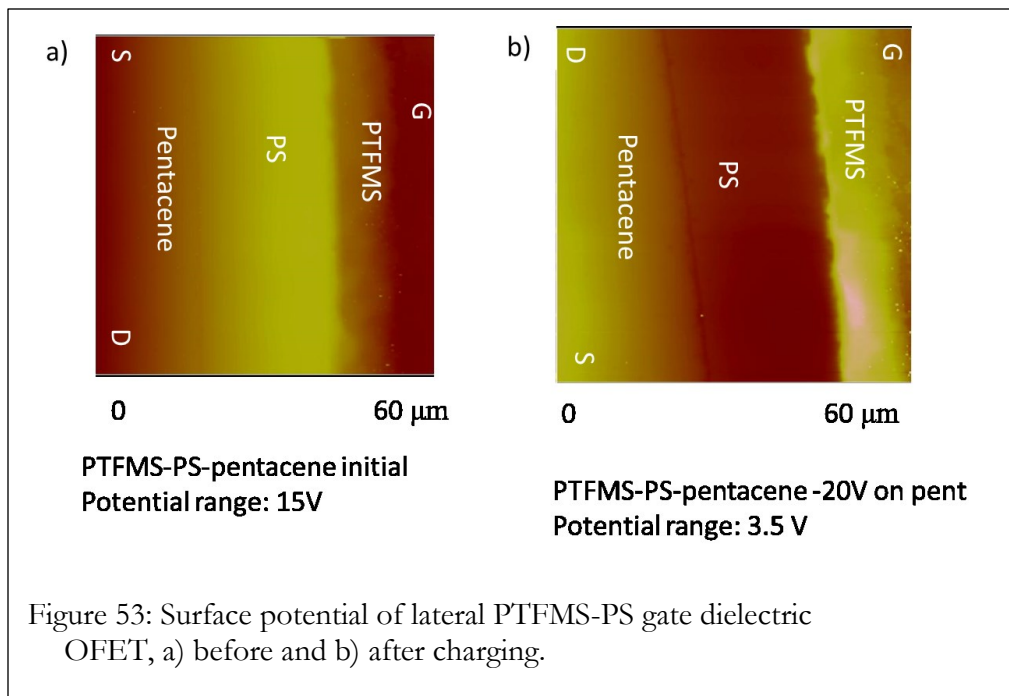
When charging the 'PTFMS-PS' device, the output current was slightly increased, as seen in Figure 54. This result is expected when negative charges are trapped in the dielectric adjacent to the pentacene.
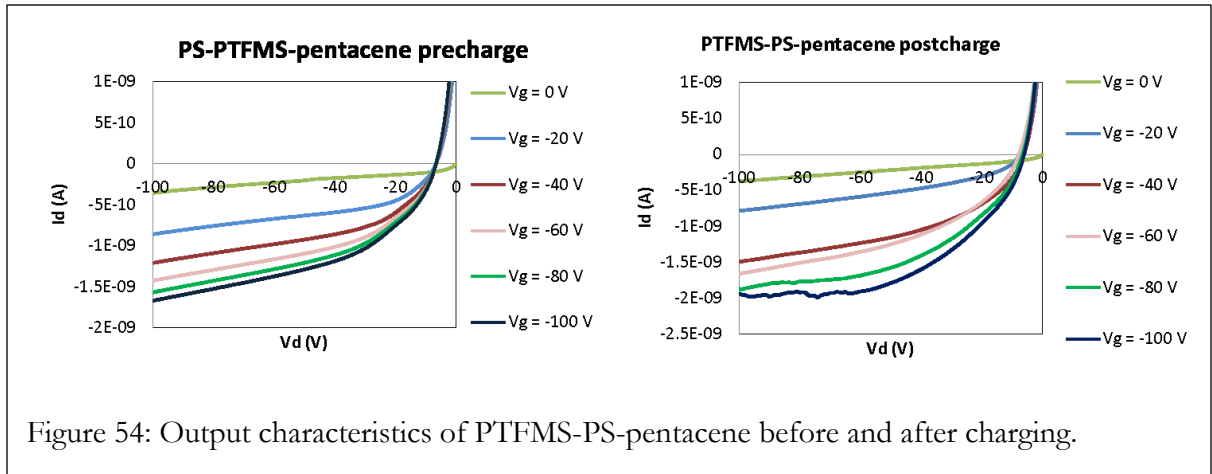
Figure 54: Output characteristics of PTFMS-PS-pentacene before and after charging.

It was observed in the second dielectric heterostructure, 'PS-PTFMS', shown in Figure 55, that after running the sample, negative charges rather than positive charges are trapped in the dielectric. Charging from the pentacene side with -20V somewhat increases the magnitude of the negative charge. This can be seen by the darker and more uniform color of the PS and PTFMS layers in Figure 55b, although the range of the voltage is not seen to change following charging, indicating that there is not a large amount of charges trapped.

Figure 55: Surface potential of lateral PS-PTFMS gate dielectric OFET, a) before and b) after charging.
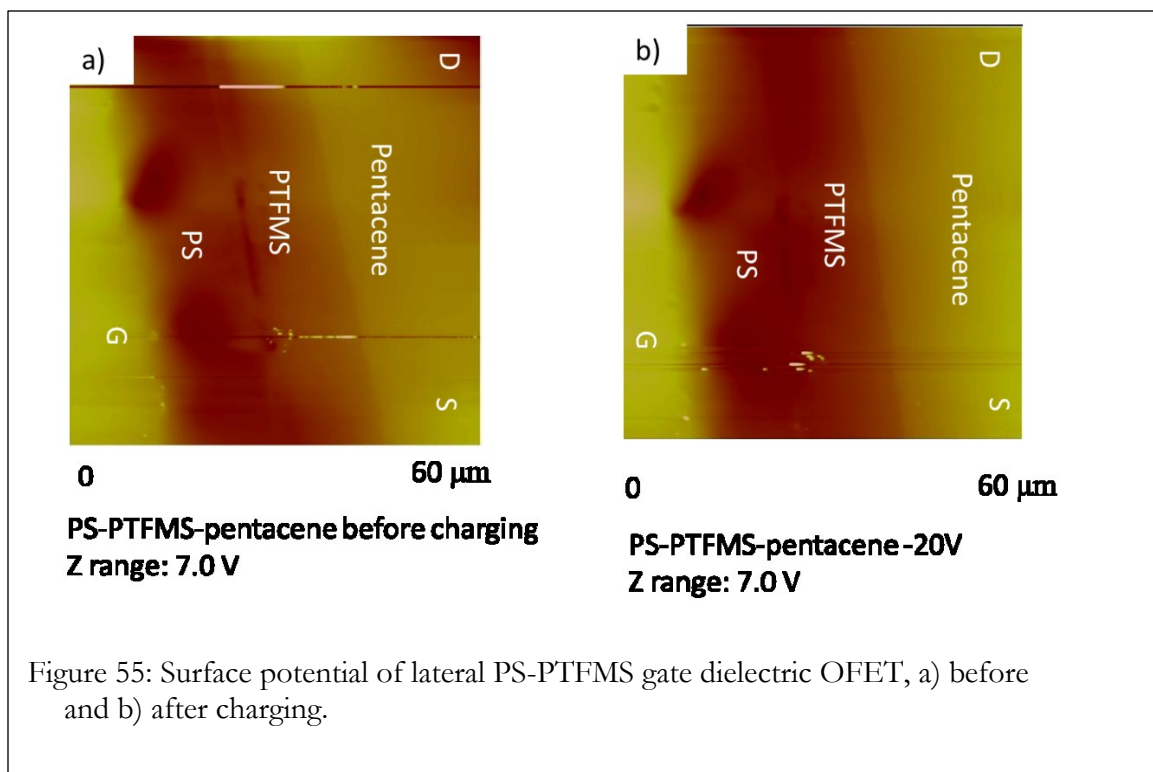
3.2   Comparison of PBMA and PS as OFET dielectrics

PBMA was analyzed as a dielectric in OFETs, compared to PS. Two OSCs were used in this comparison, pentacene and DNTT.

3.2.1 OSC comparison

To select which OSCs to use in further analysis, all three were deposited on 300 nm SiO_2 and their function was compared in SiO_2 OFETs. A diagram of the device used, and the square root transfer curves for each material are shown in Figure 56.

Figure 56: Comparison of transfer characteristics of OFETs made from three small molecule OSCs. a) OFET structure, b)-d) OSC transfer curves, V_{th}, and mobility.
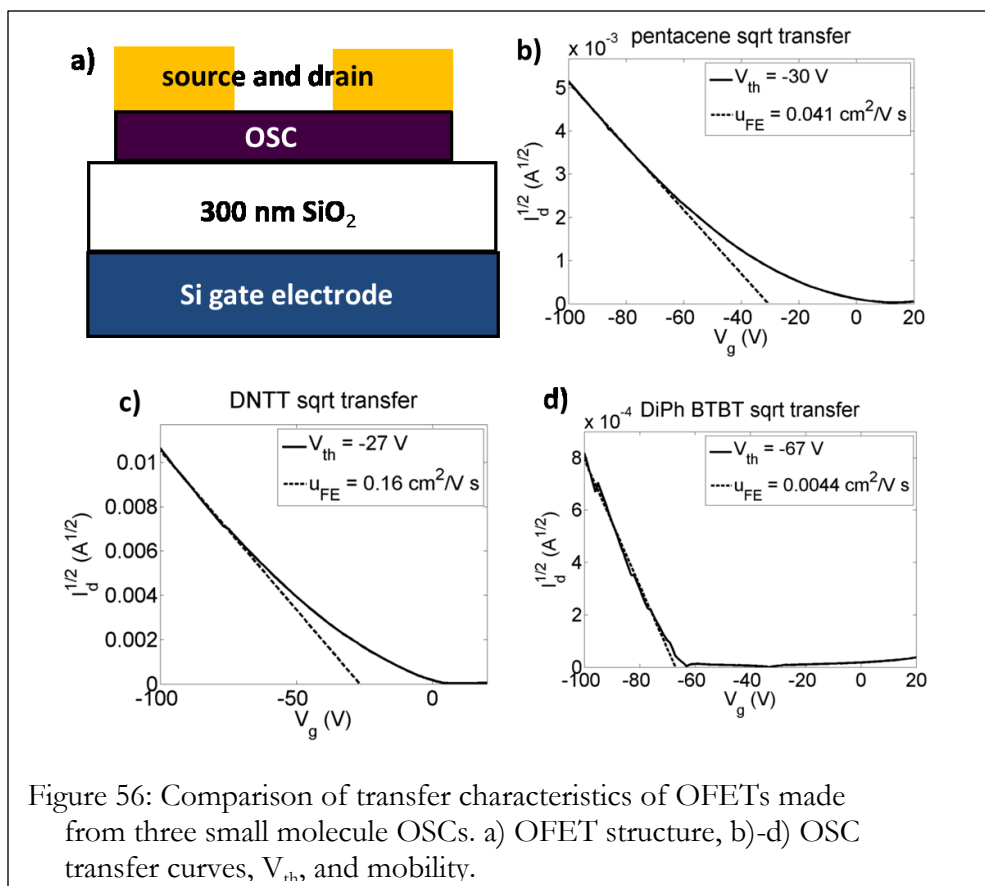
OSC	Mean μ_{FE} (cm^2/Vs)	Max μ_{FE} (cm^2/Vs)	Mean V_{th} (V)
pentacene	0.033	0.041	30
DNTT	0.13	0.16	30
DPh-BTBT	0.0022	0.0044	48

Table 5: Mobility and threshold voltage of pentacene, DNTT, and DPh-BTBT OFETs with a Si/SiO$_2$ gate.

A summary of mobility and V_{th} for each OSC are in Table 5. DPh-BTBT was found to have extremely sharp turn-on behavior, but had the lowest mobility and highest V_{th} of the

three, given the deposition conditions used. Because we were interested in making OFETs with very high mobility, DPh-BTBT was not examined further.

3.2.2 Comparison of mobility and Vth of OFETs made with PBMA and PS

Next, the mobility of pentacene was then compared on PS and PBMA dielectrics. Devices were fabricated as described in section 2.3, and the structure of the OFET is illustrated in Figure 52. Example square root transfer and output characteristics for pentacene OFETs on PS compared to PBMA are in Figure 57. Pentacene OFETs on PBMA were seen to have increased mobility and decreased threshold voltage, likely as a result of improved interface quality.

Figure 57: Pentacene OFETs with a PBMA dielectric were seen to give higher output currents and lower V_{th} than those with a PS dielectric.
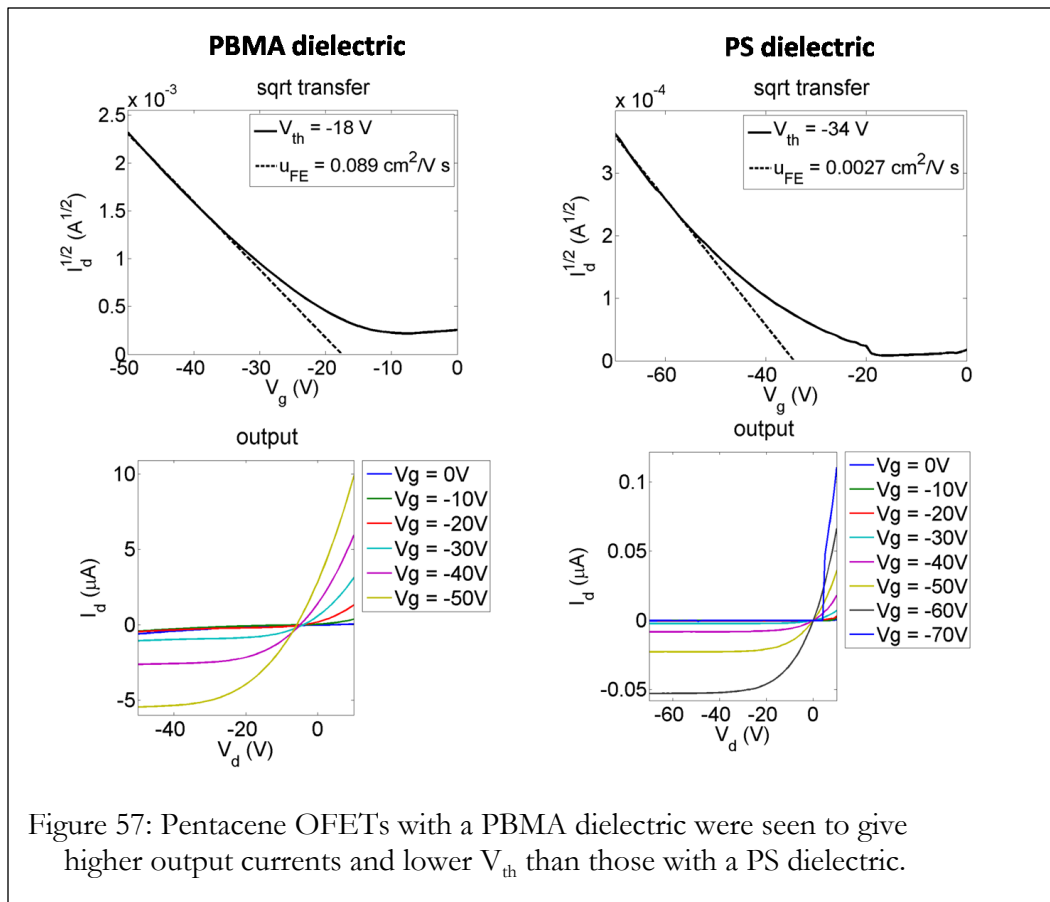
The average mobility of pentacene on PBMA was 0.27 cm^2/V s, and the average V_{th} was -16V, compared to an average mobility of pentacene on PS of 0.0028 cm^2/V s, and an average V_{th} of -38V. Reasonably good saturation was obtained for both systems, but the current is higher in the PBMA dielectric OFET. Finally, DNTT and pentacene were compared on a PBMA dielectric. Example square root transfer and output curves comparing pentacene and DNTT OFETs made with a PBMA dielectric is shown in Figure 58.

Figure 58: DNTT OFETs were seen to give higher mobility and lower V_{th} than and pentacene OFETs, both with a PBMA gate dielectric.
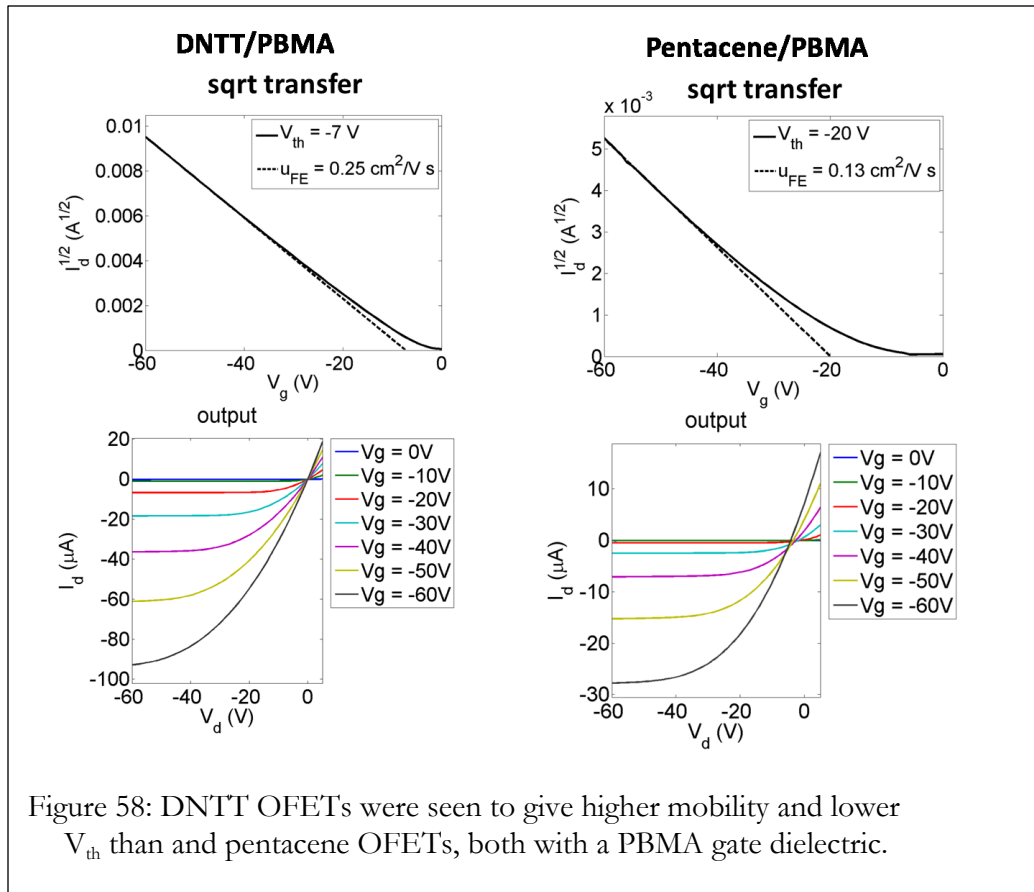
The average mobility for the DNTT devices was 0.36 cm^2/V s, and the average V_{th} was -7V, compared to an average mobility for the pentacene devices of 0.15 cm^2/V s, and an average V_{th} of -20V. This means that by the combined improvement in semiconductor and dielectric demonstrated here, the average mobility was increased by two orders of magnitude

compared to pentacene/PS OFETs. This demonstrates a method for comparing OSC and dielectric combinations, which is particularly applicable to solution processed devices.

4   Conclusions and future work

Here two dielectrics and two analytical methods have been presented. Both dielectrics exhibited improved properties compared to polystyrene. PTFMS was shown to decrease bias stress susceptibility in OFETs, and PBMA OFETs have increased field effect mobility, both compared to PS dielectrics. Future work will include synthesis of copolymers of trifluoromethylstyrene and styrene, to synthesize polymers that might combine charge trapping and bias stress resistance. Copolymers of trifluoromethylstyrene with cyclobutenostyrene would allow crosslinking of the film, which would allow solution processing of subsequent layers. Additionally, future work includes further analysis of semiconductor/dielectric pairs, including those that are solution processed, to find combinations that have high mobility and low V_{th}. This has applications in flexible and low voltage organic electronics devices.

BIBLIOGRAPHY

[1]   O.J. Alley, M. Wu, G.L. Johns, T.J. Dawidczyk, J.F.M. Hardigree, N. Markovic, et al.,

        Negative polarity of phenyl-C61 butyric acid methyl ester adjacent to donor

        macromolecule domains, Applied Physics Letters. 033301 (2015) 1–5.

        doi:10.1063/1.4905650.

[2]   B.V. Palermo, M. Palma, P. Samorì, Electronic Characterization of Organic Thin

        Films by Kelvin Probe Force Microscopy, Advanced Materials. 18 (2006) 145–164.

        doi:10.1002/adma.200501394.

[3]   O.J. Alley, E. Plunkett, T.S. Kale, X. Guo, G. McClintock, M. Bhupathiraju, et al.,

        Synthesis, Fabrication, and Heterostructure of Charged, Substituted Polystyrene

        Multilayer Dielectrics and Their Effects in Pentacene Transistors, Macromolecules. 49

        (2016) 3478–3489. doi:10.1021/acs.macromol.6b00253.

[4]   Heliatek sets new Organic Photovoltaic world record efficiency of 13.2%., Heliatek

        Sets New Organic Photovoltaic World Record Efficiency of 13.2%. [Press Release]

        Retrieved from Http://www.heliatek.com/en/press/press-Releases/details/heliatek-

        Sets-New-Organic-Photovoltaic-World-Record-Efficiency-of-13-2. (2016).

        http://www.heliatek.com/en/press/press-releases/details/heliatek-sets-new-organic-

        photovoltaic-world-record-efficiency-of-13-2.

[5]   Q. Gan, F.J. Bartoli, Z.H. Kafafi, Plasmonic-enhanced organic photovoltaics:

        Breaking the 10% efficiency barrier, Advanced Materials. 25 (2013) 2385–2396.

        doi:10.1002/adma.201203323.

[6]   L. Dou, J. You, J. Yang, C.-C. Chen, Y. He, S. Murase, et al., Tandem polymer solar

        cells featuring a spectrally matched low-bandgap polymer, Nature Photonics. 6 (2012)

180–185. doi:10.1038/nphoton.2011.356.

[7]   S. Kim, B. Kim, J. Lee, H. Shin, Y. Il Park, J. Park, Design of fluorescent blue light-emitting materials based on analyses of chemical structures and their effects, Materials Science and Engineering R: Reports. 99 (2016) 1–22. doi:10.1016/j.mser.2015.11.001.

[8]   A. Kohler, H. Bassler, Electronic Processes in Organic Semiconductors, Wiley-VCH, 2015.

[9]   M. Watanabe, Y.J. Chang, S.-W. Liu, T.-H. Chao, K. Goto, M.M. Islam, et al., The synthesis, crystal structure and charge-transport properties of hexacene, Nature Chemistry. 4 (2012) 574–578. doi:10.1038/nchem.1381.

[10]   I. Kaur, W. Jia, R.P. Kopreski, S. Selvarasah, M.R. Dokmeci, C. Pramanik, et al., Substituent effects in pentacenes: Gaining control over HOMO-LUMO gaps and photooxidative resistances, Journal of the American Chemical Society. 130 (2008) 16274–16286. doi:10.1021/ja804515y.

[11]   A.A. Peyghan, M. Noei, DFT study on [4+2] and [2+2] cycloadditions to [60] fullerene, Chemical Papers. 68 (2013) 409–416. doi:10.2478/s11696-013-0448-z.

[12]   T.D. Anthopoulos, G.C. Anyfantis, G.C. Papavassiliou, D.M. De Leeuw, Air-stable ambipolar organic transistors, Applied Physics Letters. 90 (2007) 8–11. doi:10.1063/1.2715028.

[13]   T.D. Anthopoulos, F.B. Kooistra, H.J. Wondergem, D. Kronholm, J.C. Hummelen, D.M. De Leeuw, Air-stable n-channel organic transistors based on a soluble C84 fullerene derivative, Advanced Materials. 18 (2006) 1679–1684. doi:10.1002/adma.200600068.

[14]   D.J. Bindl, M.S. Arnold, Efficient Exciton Relaxation and Charge Generation in

Nearly Monochiral (7,5) Carbon Nanatube/C60 Thin-Film Photovoltaics, The

Journal of Physical Chemistry C. 117 (2013) 2390–2395.

[15]   G.J. Brady, Y. Joo, S. Singha Roy, P. Gopalan, M.S. Arnold, High performance

transistors via aligned polyfluorene-sorted carbon nanotubes, Applied Physics Letters.

104 (2014). doi:10.1063/1.4866577.

[16]   A. Nish, J.-Y. Hwang, J. Doig, R.J. Nicholas, Highly selective dispersion of single-

walled carbon nanotubes using aromatic polymers., Nature Nanotechnology. 2 (2007)

640–6. doi:10.1038/nnano.2007.290.

[17]   K.-J. Baeg, Polymer Dielectrics and Orthogonal Solvent Effects for High-

Performance Inkjet-Printed Top-Gated P-Channel Polymer Field-Effect Transistors,

ETRI Journal. 33 (2011) 887–896. doi:10.4218/etrij.11.0111.0321.

[18]   A.L. Ayzner, C.J. Tassone, S.H. Tolbert, B.J. Schwartz, Reappraising the Need for

Bulk Heterojunctions in Polymer - Fullerene Photovoltaics : The Role of Carrier

Transport in All-Solution-Processed P3HT / PCBM Bilayer Solar Cells, Journal of

Physical Chemistry C. 113 (2009) 20050–20060.

[19]   H. Aarnio, P. Sehati, S. Braun, M. Nyman, M.P. de Jong, M. Fahlman, et al.,

Spontaneous Charge Transfer and Dipole Formation at the Interface Between P3HT

and PCBM, Advanced Energy Materials. 1 (2011) 792–797.

doi:10.1002/aenm.201100074.

[20]   A. Pivrikas, N.S. Sariciftci, G. Juska, R. Osterbacka, A Review of Charge Transport

and Recombination in Polymer / Fullerene Organic Solar Cells, Progress in

Photovoltaics: Research and Applications. 15 (2007) 677–696. doi:10.1002/pip.

[21]   M. Al-Ibrahim, H.K. Roth, U. Zhokhavets, G. Gobsch, S. Sensfuss, Flexible large

area polymer solar cells based on poly(3-hexylthiophene)/fullerene, Solar Energy Materials and Solar Cells. 85 (2005) 13–20. doi:10.1016/j.solmat.2004.03.001.

[22]   D. Cahen, A. Kahn, E. Umbach, Energetics of molecular interfaces, Materials Today. 8 (2005) 32–41.

[23]   B.M. Dhar, R. Özgün, T. Dawidczyk, A. Andreou, H.E. Katz, Threshold voltage shifting for memory and tuning in printed transistor circuits, Materials Science and Engineering: R: Reports. 72 (2011) 49–80. doi:10.1016/j.mser.2010.11.001.

[24]   J.F.M. Hardigree, T.J. Dawidczyk, R.M. Ireland, G.L. Johns, B.-J. Jung, M. Nyman, et al., Reducing Leakage Currents in n-Channel Organic Field-Effect Transistors Using Molecular Dipole Mono layers on Nanoscale Oxides, Acs Applied Materials & Interfaces. 5 (2013) 7025–7032. doi:10.1021/am401278p.

[25]   I.N. Hulea, S. Fratini, H. Xie, C.L. Mulder, N.N. Iossad, G. Rastelli, et al., Tunable Fröhlich polarons in organic single-crystal transistors., Nature Materials. 5 (2006) 982–986. doi:10.1038/nmat1774.

[26]   T. Richards, M. Bird, H. Sirringhaus, A quantitative analytical model for static dipolar disorder broadening of the density of states at organic heterointerfaces., The Journal of Chemical Physics. 128 (2008) 234905. doi:10.1063/1.2937729.

[27]   J. Veres, S.D. Ogier, S.W. Leeming, D.C. Cupertino, S. Mohialdin Khaffaf, Low-k Insulators as the Choice of Dielectrics in Organic Field-Effect Transistors, Advanced Functional Materials. 13 (2003) 199–204. doi:10.1002/adfm.200390030.

[28]   S.G.J. Mathijssen, M.-J. Spijkman, A.-M. Andringa, P. a van Hal, I. McCulloch, M. Kemerink, et al., Revealing buried interfaces to understand the origins of threshold voltage shifts in organic field-effect transistors., Advanced Materials (Deerfield Beach,

113

Fla.). 22 (2010) 5105–9. doi:10.1002/adma.201001865.

[29]   K. Kim, S.G. Hahm, Y. Kim, S. Kim, S.H. Kim, C.E. Park, Realization of electrically stable organic field-effect transistors using simple polymer blended dielectrics, Organic Electronics. 21 (2015) 111–116. doi:10.1016/j.orgel.2015.03.005.

[30]   A. Nakajima, D. Fujii, Memory operation mechanism of fullerene-containing polymer memory, Applied Physics Letters. 106 (2015) 103302. doi:10.1063/1.4914881.

[31]   G.F. Burkhard, E.T. Hoke, Z.M. Beiley, M.D. Mcgehee, Free Carrier Generation in Fullerene Acceptors and Its E ff ect on Polymer Photovoltaics, The Journal of Physical Chemistry C. 116 (2012) 26674.

[32]   V. Mihailetchi, L. Koster, J. Hummelen, P. Blom, Photocurrent Generation in Polymer-Fullerene Bulk Heterojunctions, Physical Review Letters. 93 (2004) 216601. doi:10.1103/PhysRevLett.93.216601.

[33]   Z.-L. Guan, J.B. Kim, H. Wang, C. Jaye, D. a. Fischer, Y.-L. Loo, et al., Direct determination of the electronic structure of the poly(3-hexylthiophene):phenyl-[6,6]-C61 butyric acid methyl ester blend, Organic Electronics. 11 (2010) 1779–1785. doi:10.1016/j.orgel.2010.07.023.

[34]   S.M. Sze, M.-K. Lee, Semiconductor Devices: Physics and Technology, 3rd ed., John Wiley & Sons, Inc., 2012.

[35]   S. Lee, J.-H. Lee, K.H. Kim, S.-J. Yoo, T.G. Kim, J.W. Kim, et al., Determination of the interface energy level alignment of a doped organic hetero-junction using capacitance–voltage measurements, Organic Electronics. 13 (2012) 2346–2351. doi:10.1016/j.orgel.2012.06.039.

[36]   Y. Shen, L. Scudiero, M.C. Gupta, Temperature Dependence of Open-Circuit

Voltage and UPS Study for P3HT : PCBM Organic Solar Cells, IEEE Journal of Photovoltaics. 2 (2012) 512–518.

[37]   a. Wilke, P. Amsalem, J. Frisch, B. Bröker, a. Vollmer, N. Koch, Electric fields induced by energy level pinning at organic heterojunctions, Applied Physics Letters. 98 (2011) 123304. doi:10.1063/1.3571286.

[38]   L. Lindell, D. Çakır, G. Brocks, M. Fahlman, S. Braun, Role of intrinsic molecular dipole in energy level alignment at organic interfaces, Applied Physics Letters. 102 (2013) 223301. doi:10.1063/1.4809567.

[39]   H. Hoppe, T. Glatzel, M. Niggemann, a Hinsch, M.C. Lux-Steiner, N.S. Sariciftci, Kelvin probe force microscopy study on conjugated polymer/fullerene bulk heterojunction organic solar cells., Nano Letters. 5 (2005) 269–74. doi:10.1021/nl048176c.

[40]   E.J. Spadafora, R. Demadrille, B. Ratier, B. Grévin, Imaging the carrier photogeneration in nanoscale phase segregated organic heterojunctions by Kelvin probe force microscopy., Nano Letters. 10 (2010) 3337–42. doi:10.1021/nl101001d.

[41]   K. Maturová, M. Kemerink, M.M. Wienk, D.S.H. Charrier, R. a. J. Janssen, Scanning Kelvin Probe Microscopy on Bulk Heterojunction Polymer Blends, Advanced Functional Materials. 19 (2009) 1379–1386. doi:10.1002/adfm.200801283.

[42]   H. Ishii, N. Hayashi, E. Ito, Y. Washizu, K. Sugi, Y. Kimura, et al., Kelvin probe study of band bending at organic semiconductor / metal interfaces : examination of Fermi level alignment, Phys. Stat. Sol. (a). 1094 (2004) 1075–1094. doi:10.1002/pssa.200404346.

[43]   a. Doukkali, S. Ledain, C. Guasch, J. Bonnet, Surface potential mapping of biased pn

junction with kelvin probe force microscopy: application to cross-section devices, Applied Surface Science. 235 (2004) 507–512. doi:10.1016/j.apsusc.2004.03.249.

[44]   S. Cook, R. Katoh, A. Furube, Ultrafast Studies of Charge Generation in PCBM:P3HT Blend Films following Excitation of the Fullerene PCBM, The Journal of Physical Chemistry C. 113 (2009) 2547–2552. doi:10.1021/jp8050774.

[45]   J. Szmytkowski, Modeling the electrical characteristics of P3HT : PCBM bulk heterojunction solar cells : Implementing the interface, Semiconductor Science and Technology. 25 (2010) 015009. doi:10.1088/0268-1242/25/1/015009.

[46]   R.M. Jain, R. Howden, K. Tvrdy, S. Shimizu, A.J. Hilmer, T.P. Mcnicholas, et al., Polymer-Free Near-Infrared Photovoltaics with Single Chirality (6 , 5) Semiconducting Carbon Nanotube Active Layers, Advanced Materials. 24 (2012) 4436. doi:10.1002/adma.201202088.

[47]   M.J. Shea, M.S. Arnold, 1% Solar Cells Derived From Ultrathin Carbon Nanotube Photoabsorbing Films, Applied Physics Letters. 102 (2013) 243101. doi:10.1063/1.4811359.

[48]   D.J. Bindl, A.S. Brewer, M.S. Arnold, Semiconducting carbon nanotube/fullerene blended heterojunctions for photovoltaic near-infrared photon harvesting, Nano Research. 4 (2011) 1174–1179. doi:10.1007/s12274-011-0167-0.

[49]   D.J. Bindl, M.-Y. Wu, F.C. Prehn, M.S. Arnold, Efficiently harvesting excitons from electronic type-controlled semiconducting carbon nanotube films., Nano Letters. 11 (2011) 455–60. doi:10.1021/nl1031343.

[50]   D.J. Bindl, N.S. Safron, M.S. Arnold, Dissociating Excitons Photogenerated in Semiconducting Carbon Nanotubes at Polymeric Photovoltaic Heterojunction

116

Interfaces, ACS Nano. 4 (2010) 5657–5664.

[51] R.D. Mehlenbacher, M. Wu, M. Grechko, J.E. Laaser, M.S. Arnold, M.T. Zanni, Photoexcitation Dynamics of Coupled Semiconducting Carbon Nanotube Thin Films, (2013).

[52] M.T. Dang, L. Hirsch, G. Wantz, P3HT:PCBM, Best Seller in Polymer Photovoltaic Research, Advanced Materials. 23 (2011) 3597–3602. doi:10.1002/adma.201100792.

[53] T. Liu, A. Troisi, What makes fullerene acceptors special as electron acceptors in organic solar cells and how to replace them., Advanced Materials (Deerfield Beach, Fla.). 25 (2013) 1038–41. doi:10.1002/adma.201203486.

[54] B. Zhang, Y. Liu, S. Agarwal, M.-L. Yeh, H.E. Katz, Structure, sodium ion role, and practical issues for β-alumina as a high-k solution-processed gate layer for transparent and low-voltage electronics., ACS Applied Materials & Interfaces. 3 (2011) 4254–61. doi:10.1021/am2009103.

[55] B.M. Dhar, G.S. Kini, G. Xia, B.J. Jung, N. Markovic, H.E. Katz, Field-effect-tuned lateral organic diodes., Proceedings of the National Academy of Sciences of the United States of America. 107 (2010) 3972–6. doi:10.1073/pnas.0910554107.

[56] T.J. Dawidczyk, G.L. Johns, R. Ozgun, O. Alley, a. G. Andreou, N. Markovic, et al., Kelvin probe microscopic visualization of charge storage at polystyrene interfaces with pentacene and gold, Applied Physics Letters. 100 (2012) 073305. doi:10.1063/1.3684977.

[57] T.J. Dawidczyk, J.F. Martínez Hardigree, G.L. Johns, R. Ozgun, O.J. Alley, A.G. Andreou, et al., Visualizing and quantifying charge distributions correlated to threshold voltage shifts in lateral organic transistors., ACS Nano. 8 (2014) 2714–24.

117

doi:10.1021/nn4064067.

[58]   F. Xu, M.-Y. Wu, N.S. Safron, S.S. Roy, R.M. Jacobberger, D.J. Bindl, et al., Highly

         stretchable carbon nanotube transistors with ion gel gate dielectrics., Nano Letters. 14

         (2014) 682–6. doi:10.1021/nl403941a.

[59]   F. Schoppler, C. Mann, T.C. Hain, F.M. Neubauer, G. Privitera, F. Bonaccorso, et al.,

         Molar Extinction Coefficient of Single-Wall Carbon Nanotubes, (2011) 14682–14686.

[60]   F. MacHui, S. Langner, X. Zhu, S. Abbott, C.J. Brabec, Determination of the

         P3HT:PCBM solubility parameters via a binary solvent gradient method: Impact of

         solubility on the photovoltaic performance, Solar Energy Materials and Solar Cells.

         100 (2012) 138–146. doi:10.1016/j.solmat.2012.01.005.

[61]   W.C. Tsoi, D.T. James, J.S. Kim, P.G. Nicholson, C.E. Murphy, D.D.C. Bradley, et

         al., The nature of in-plane skeleton Raman modes of P3HT and their correlation to

         the degree of molecular order in P3HT:PCBM blend thin films, Journal of the

         American Chemical Society. 133 (2011) 9834–9843. doi:10.1021/ja2013104.

[62]   M.S. Dresselhaus, G. Dresselhaus, A. Jorio, A.G. Souza Filho, R. Saito, Raman

         spectroscopy on isolated single wall carbon nanotubes, Carbon. 40 (2002) 2043–2061.

         doi:10.1016/S0008-6223(02)00066-0.

[63]   H.H. Choi, W.H. Lee, K. Cho, Bias-stress-induced charge trapping at polymer chain

         ends of polymer gate-dielectrics in organic transistors, Advanced Functional

         Materials. 22 (2012) 4833–4839. doi:10.1002/adfm.201201084.

[64]   J. Lee, H.H. Choi, N. Park, H. Min, S. Han, H. Jeong, et al., Branched segments in

         polymer gate dielectric as intrinsic charge trap sites in organic transistors, Journal of

         Physical Chemistry C. 119 (2015) 7670–7677. doi:10.1021/acs.jpcc.5b01522.

[65]   J. Lee, H. Min, N. Park, H. Jeong, S. Han, S.H. Kim, et al., Gate-Bias Stability

Behavior Tailored by Dielectric Polymer Stereostructure in Organic Transistors, ACS

Applied Materials and Interfaces. 7 (2015) 25045–25052.

doi:10.1021/acsami.5b08414.

[66]   Y.-H. Chou, H.-C. Chang, C.-L. Liu, W.-C. Chen, Polymeric charge storage electrets

for non-volatile organic field effect transistor memory devices, Polym. Chem. 6

(2015) 341–352. doi:10.1039/C4PY01213E.

[67]   Y. Guo, G. Yu, Y. Liu, Functional organic field-effect transistors, Advanced

Materials. 22 (2010) 4427–4447. doi:10.1002/adma.201000740.

[68]   X. Qiu, Patterned piezo-, pyro-, and ferroelectricity of poled polymer electrets,

Journal of Applied Physics. 108 (2010) 0–19. doi:10.1063/1.3457141.

[69]   F. Hu, C. Qian, F. Liao, M. Shao, S.-T. Lee, Recent Advancements in Nanogenerators

for Energy Harvesting, Small. 11 (2015) 5611–5628.

doi:10.1002/smll.201501011View/save.

[70]   G. Horowitz, R. Hajlaoui, H. Bouchriha, R. Bourguiga, M. Hajlaoui, The Concept of

"Threshold Voltage" in Organic Field-Effect Transistors, Advanced Materials. (1998)

923–927.

[71]   H.E. Katz, Through Thick and Thin: Tuning the Threshold Voltage in Organic Field-

E ff ect Transistors, (2014).

[72]   W.L. Leong, N. Mathews, B. Tan, S. Vaidyanathan, F. Dötz, S. Mhaisalkar, Towards

printable organic thin film transistor based flash memory devices, Journal of Materials

Chemistry. 21 (2011) 5203. doi:10.1039/c0jm03974h.

[73]   K.J. Baeg, Y.Y. Noh, J. Ghim, S.J. Kang, H. Lee, D.Y. Kim, Organic non-volatile

memory based on pentacene field-effect transistors using a polymeric gate electret, Advanced Materials. 18 (2006) 3179–3183. doi:10.1002/adma.200601434.

[74]   H.E. Katz, X.M. Hong, A. Dodabalapur, R. Sarpeshkar, Organic field-effect transistors with polarizable gate insulators, Journal of Applied Physics. 91 (2002) 1572–1576. doi:10.1063/1.1427136.

[75]   J. a Caraveo-Frescas, M. a Khan, H.N. Alshareef, Polymer ferroelectric field-effect memory device with SnO channel layer exhibits record hole mobility., Scientific Reports. 4 (2014) 5243. doi:10.1038/srep05243.

[76]   M.A. Khan, J.A. Caraveo-Frescas, H.N. Alshareef, Hybrid dual gate ferroelectric memory for multilevel information storage, Organic Electronics: Physics, Materials, Applications. 16 (2015) 9–17. doi:10.1016/j.orgel.2014.10.034.

[77]   K.J. Baeg, D. Khim, J. Kim, B. Do Yang, M. Kang, S.W. Jung, et al., High-performance top-gated organic field-effect transistor memory using electrets for monolithic printed flexible nand flash memory, Advanced Functional Materials. 22 (2012) 2915–2926. doi:10.1002/adfm.201200290.

[78]   W. Wang, S.K. Hwang, K.L. Kim, J.H. Lee, S.M. Cho, C. Park, Highly Reliable Top-Gated Thin-Film Transistor Memory with Semiconducting, Tunneling, Charge-Trapping, and Blocking Layers All of Flexible Polymers, ACS Applied Materials and Interfaces. 7 (2015) 10957–10965. doi:10.1021/acsami.5b02213.

[79]   X. Zheng, Z. Guo, D. Tian, X. Zhang, W. Li, L. Jiang, Underwater self-cleaning scaly fabric membrane for oily water separation, ACS Applied Materials and Interfaces. 7 (2015) 4336–4343. doi:10.1021/am508814g.

[80]   C.-W. Tseng, D.-C. Huang, Y.-T. Tao, Organic Transistor Memory with a Charge

Storage Molecular Double-Floating-Gate Monolayer, ACS Applied Materials & Interfaces. (2015) 150428141813001. doi:10.1021/acsami.5b01625.

[81]   S.A. Lee, D.Y. Kim, K.U. Jeong, S.H. Lee, S. Bae, D.S. Lee, et al., Molecular-scale charge trap medium for organic non-volatile memory transistors, Organic Electronics: Physics, Materials, Applications. 27 (2015) 18–23. doi:10.1016/j.orgel.2015.08.020.

[82]   A. Nakajima, D. Fujii, M. Uchino, Excellent retention characteristics of nanocomposite gate insulator consisting of fullerene-containing polystyrene, Applied Physics Letters. 103 (2013) 1–5. doi:10.1063/1.4812840.

[83]   A. Khassanov, T. Schmaltz, H.-G. Steinrück, A. Magerl, A. Hirsch, M. Halik, Interface Engineering of Molecular Charge Storage Dielectric Layers for Organic Thin-Film Memory Transistors, Advanced Materials Interfaces. (2014) n/a–n/a. doi:10.1002/admi.201400238.

[84]   Y. Zhou, S.-T. Han, Y. Yan, L.-B. Huang, L. Zhou, J. Huang, et al., Solution processed molecular floating gate for flexible flash memories., Scientific Reports. 3 (2013) 3093. doi:10.1038/srep03093.

[85]   C.C. Shih, Y.C. Chiu, W.Y. Lee, J.Y. Chen, W.C. Chen, Conjugated polymer nanoparticles as nano floating gate electrets for high performance nonvolatile organic transistor memory devices, Advanced Functional Materials. 25 (2015) 1511–1519. doi:10.1002/adfm.201404329.

[86]   Y.-C. Chiu, C.-C. Shih, W.-C. Chen, Nonvolatile memories using the electrets of conjugated rod-coil block copolymer and its nanocomposite with single wall carbon nanotubes, J. Mater. Chem. C. 3 (2015) 551–558. doi:10.1039/C4TC02233E.

[87]   Y.H. Kim, M. Kim, S. Oh, H. Jung, Y. Kim, T.S. Yoon, et al., Organic memory

device with polyaniline nanoparticles embedded as charging elements, Applied Physics Letters. 100 (2012) 8–12. doi:10.1063/1.4704571.

[88]   Z.Q. Cui, S. Wang, J.M. Chen, X. Gao, B. Dong, L.F. Chi, et al., Direct probing of electron and hole trapping into nano-floating-gate in organic field-effect transistor nonvolatile memories, Applied Physics Letters. 106 (2015) 0–4. doi:10.1063/1.4916511.

[89]   Y.H. Chou, N.H. You, T. Kurosawa, W.Y. Lee, T. Higashihara, M. Ueda, et al., Thiophene and selenophene donor-acceptor polyimides as polymer electrets for nonvolatile transistor memory devices, Macromolecules. 45 (2012) 6946–6956. doi:10.1021/ma301326r.

[90]   L. Dong, Y.-C. Chiu, C.-C. Chueh, A.-D. Yu, W.-C. Chen, Semi-conjugated acceptor-based polyimides as electrets for nonvolatile transistor memory devices, Polym. Chem. 5 (2014) 6834–6846. doi:10.1039/C4PY00988F.

[91]   A.D. Yu, T. Kurosawa, M. Ueda, W.C. Chen, Polycyclic arene-based D-A polyimide electrets for high-performance n-type organic field effect transistor memory devices, Journal of Polymer Science, Part A: Polymer Chemistry. 52 (2014) 139–147. doi:10.1002/pola.26983.

[92]   H.Y. Chi, H.W. Hsu, S.H. Tung, C.L. Liu, Nonvolatile Organic Field-Effect Transistors Memory Devices Using Supramolecular Block Copolymer/Functional Small Molecule Nanocomposite Electret, ACS Applied Materials and Interfaces. 7 (2015) 5663–5673. doi:10.1021/acsami.5b00338.

[93]   M. Egginger, S. Bauer, R. Schwodiauer, Current versus gate voltage hysteresis in organic field effect transistors, Monatsh Chem. 140 (2009) 735–750.

doi:10.1007/s00706-009-0149-z.

[94] D.K. Hwang, K. Lee, J.H. Kim, S. Im, J.H. Park, E. Kim, Comparative studies on the stability of polymer versus SiO2 gate dielectrics for pentacene thin-film transistors, Applied Physics Letters. 89 (2006) 2004–2007. doi:10.1063/1.2345243.

[95] B.J. Kirby, P.A. Kienzle, B.B. Maranville, N.F. Berk, J. Krycka, F. Heinrich, et al., Phase-sensitive specular neutron reflectometry for imaging the nanometer scale composition depth profile of thin-film materials, Current Opinion in Colloid and Interface Science. 17 (2012) 44–53. doi:10.1016/j.cocis.2011.11.001.

[96] C.F. O'Donovan, K. V.; Ankner, J. F.; Berk, N. F.; Majkrzak, Kienzle, P. A.;, Http://www.ncnr.nist.gov/reflpak Accessed. (2015).

[97] K. Takimiya, S. Shinamura, I. Osaka, E. Miyazaki, Thienoacene-based organic semiconductors, Advanced Materials. 23 (2011) 4347–4370. doi:10.1002/adma.201102007.

[98] B. Bömer, C. Süling, J. König, H. Hespe, K. Heynemann, R. Weber, Use of styrene polymers for the preparation of optical system, 1984. doi:10.1017/CBO9781107415324.004.

CV

Olivia J. Alley was born in Willits, California in 1986. She received the only National Merit Scholarship in Mendocino County in 2004. She received her Bachelor of Science in Chemistry from California Institute of Technology in 2008, and joined the chemistry graduate program at University of California, Riverside to do research under Professor Leonard Mueller. In 2010, she received a Master of Science in Chemistry from University of California, Riverside, for her thesis titled "J-based spectral editing in solid state NMR". In 2011, she enrolled in the graduate program in Materials Science and Engineering at Johns Hopkins University in the lab of Professor Howard E. Katz, and on May 25, 2016, she successfully defended her PhD thesis. Important publications to date include:

Refereed Journal Articles:

O. J. Alley, E. Plunkett, T. S. Kale, X. Guo, G. McClintock, M. Bhupathiraju, B. Kirby, D. H. Reich, and H. E. Katz. Synthesis, Fabrication, and Heterostructure of Charged, Substituted Polystyrene Multilayer Dielectrics and Their Effects in Pentacene Transistors. Macromolecules **49**, 3478 (2016).

Y. Liu, K. McElhinny, **O. Alley**, P. G. Evans, and H. E. Katz. Reduced-temperature solution-processed transparent oxide low-voltage-operable field-effect transistors. MRS Comm. 5, 605 (2015).

O.J. Alley, M.-Y. Wu, J. F. Martínez Hardigree, N. Markovic, M.S. Arnold, and H. E. Katz. Substrate-Correlated Interface Polarity Reversal at a Carbon Nanotube/Fullerene Junction. 42nd IEEE Photovoltaic Specialists Conference Proceedings, 2015.

O. J. Alley, M.-Y. Wu, G. L. Johns, T. J. Dawidczyk, J. F. Martínez Hardigree, N. Markovic, M. S. Arnold, and H. E. Katz. Negative polarity of phenyl-C$_{61}$ butyric acid methyl ester adjacent to donor macromolecule domains. Applied Physics Letters 106, 033301 (2015).

T. J. Dawidczyk, J. F. Martínez Hardigree, G. L. Johns, R. Ozgun, **O. Alley**, A. G. Andreou, N. Markovic, and H. E. Katz. Visualizing and Quantifying Charge Distributions Correlated to Threshold Voltage Shifts in Lateral Organic Transistors. ACS Nano 8, 2714 (2014).

T. J. Dawidczyk, G. L. Johns, R. Ozgun, **O. Alley**, A. G. Andreou, N. Markovic, and H. E. Katz. Kelvin probe microscopic visualization of charge storage at polystyrene interfaces with pentacene and gold. Applied Physics Letters 100, 073305 (2012).

R. A. Nkansah, Y. Liu, **O. J. Alley**, J. B. Gerken, M. D. Drake, and J. D. Roberts. Conformational Preferences of 3-(Dimethylazinoyl)propanoic Acid as a Function of pH and Solvent; Intermolecular versus Intramolecular Hydrogen Bonding. Journal of Organic Chemistry 74, 2344-2349 (2009).