

VLSI Circuits for Bidirectional Neural Interfaces

by

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Abstract

Medical devices that deliver electrical stimulation to neural tissue are important clinical tools that can augment or replace pharmacological therapies. The success of such devices has led to an explosion of interest in the field, termed neuromodulation, with a diverse set of disorders being targeted for device-based treatment. Nevertheless, a large degree of uncertainty surrounds how and why these devices are effective. This uncertainty limits the ability to optimize therapy and gives rise to deleterious side effects. An emerging approach to improve neuromodulation efficacy and to better understand its mechanisms is to record bioelectric activity during stimulation. Understanding how stimulation affects electrophysiology can provide insights into disease, and also provides a feedback signal to autonomously tune stimulation parameters to improve efficacy or decrease side-effects. The aims of this work were taken up to advance the state-of-the-art in neuro-interface technology to enable closed-loop neuromodulation therapies.

Long term monitoring of neuronal activity in awake and behaving subjects can provide critical insights into brain dynamics that can inform system-level design of

ABSTRACT

closed-loop neuromodulation systems. Thus, first we designed a system that wirelessly telemetered electrocorticography signals from awake-behaving rats. We hypothesized that such a system could be useful for detecting sporadic but clinically relevant electrophysiological events. In an 18-hour, overnight recording, seizure activity was detected in a pre-clinical rodent model of global ischemic brain injury.

We subsequently turned to the design of neurostimulation circuits. Three critical features of neurostimulation devices are safety, programmability, and specificity. We conceived and implemented a neurostimulator architecture that utilizes a compact on-chip circuit for charge balancing (safety), digital-to-analog converter calibration (programmability) and current steering (specificity). Charge balancing accuracy was measured at better than 0.3%, the digital-to-analog converters achieved 8-bit resolution, and physiological effects of current steering stimulation were demonstrated in an anesthetized rat.

Lastly, to implement a bidirectional neural interface, both the recording and stimulation circuits were fabricated on a single chip. In doing so, we implemented a low noise, ultra-low power recording front end with a high dynamic range. The recording circuits achieved a signal-to-noise ratio of 58 dB and a spurious-free dynamic range of better than 70 dB, while consuming 5.5 μ W per channel. We demonstrated bidirectional operation of the chip by recording cardiac modulation induced through vagus nerve stimulation, and demonstrated closed-loop control of cardiac rhythm.

ABSTRACT

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Contents

Abstract	ii
Acknowledgments	v
List of Tables	xv
List of Figures	xvi
1 Introduction	1
1.1 Specific Aims	2
1.2 Contributions	4
1.2.1 Aim 1	4
1.2.2 Aim 2	5
1.2.3 Aim 3	6
1.3 Thesis Organization	7
2 Bidirectional Neural Interfaces – Applications and VLSI Circuit Im-	

CONTENTS

plementations	9
2.1 Applications	12
2.1.1 Neuroprostheses	12
2.1.1.1 Motor Neuroprostheses	12
2.1.1.2 Sensory Feedback	14
2.1.1.3 Comparison of CNS and PNS stimulation	20
2.1.2 Neuro-repair	22
2.1.2.1 Restorative Motor Prostheses	23
2.1.2.2 Restorative Cognitive Prostheses	25
2.1.2.3 Future for Neuro-repair Devices	26
2.1.3 Neurotherapeutics	28
2.1.3.1 Epilepsy	28
2.1.3.2 Movement Disorders	30
2.1.3.3 Benefit of Closed-Loop Neurotherapeutics	32
2.2 Very Large Scale Integration (VLSI) Implementations	34
2.2.1 VLSI Systems for Spike-Triggered Stimulation	34
2.2.2 VLSI Systems for Treatment of Epilepsy	36
2.2.3 Comparison of VLSI Systems	40
2.3 Conclusion	42
3 A Wireless EEG System for Freely Moving Rodents	45
3.1 System Design	47

CONTENTS

3.1.1	Neural Front-End	49
3.1.2	Wireless Telemetry	50
3.1.3	Digital Interface	51
3.1.4	System Integration and Packaging	52
3.1.5	Receiver Circuitry	54
3.2	Data Analysis	54
3.3	Results	55
3.3.1	Benchtop Characterization	56
3.3.2	In-vivo Experiments	57
3.3.2.1	System A	57
3.3.2.2	System B	59
3.4	Conclusion and Future Work	61
4	A CMOS Current Steering Neurostimulation Array with Integrated DAC Calibration and Charge Balancing	64
4.1	Circuit Design	67
4.1.1	Digital-to-Analog Converter	68
4.1.2	Calibration Circuit	70
4.1.3	Biphasic Current Source	71
4.2	Calibration Procedure	73
4.3	Matching	75
4.3.1	Charge Balancing	75

CONTENTS

4.3.2	Current Steering	77
4.4	Electrode Interface	78
4.5	Benchtop Characterization	79
4.5.1	DAC Calibration	81
4.5.2	Matching	81
4.5.3	Current Steering	84
4.6	In-vitro Results	85
4.7	In-vivo Results	86
4.8	Discussion	90
4.8.1	DAC Calibration	90
4.8.2	Matching	92
4.8.3	In-vivo results	93
4.9	Conclusion	94
4.10	Appendix: Calculation of γ for an R- β R splitter	95
5	A Bidirectional Neural Interface IC with Chopper Stabilized BioADC	
	Array and Charge Balanced Stimulator	99
5.1	Circuit Design	102
5.1.1	OTA	104
5.1.2	Comparator	106
5.1.3	Feedback DAC	106
5.1.4	Decimation Filter	107

CONTENTS

5.1.5	Mixed-Signal Servo Loop	108
5.1.6	Stimulator	110
5.1.7	Stimulation Artifact	112
5.2	Measurement Results	114
5.2.1	BioADC Characterization	115
5.2.2	Power Consumption and Noise Efficiency	121
5.2.3	<i>In-vivo</i> Measurements	122
5.3	Comparisons and Conclusion	125
6	Closed-loop Control of Cardiac Rhythm with a Custom Integrated Circuit	130
6.1	System Design	131
6.1.1	Heart Rate Detection Algorithm	133
6.1.2	PI Controller	133
6.2	Experimental Setup	134
6.3	Results	137
6.4	Discussion	140
6.5	Conclusion	141
7	Conclusions and Future Directions	142
7.1	A Wireless EEG System for Freely Moving Rodents	143
7.1.1	Future Directions	143

CONTENTS

7.2	A CMOS Current Steering Neurostimulation Array	145
7.2.1	Future Directions	146
7.3	A Bidirectional Neural Interface Chip	148
7.3.1	Future Directions	148
Bibliography		151
Vita		194

List of Tables

2.1	State-of-the-art bidirectional neural interface system specifications . .	41
4.1	Transistor sizing in the R- β R splitter	70
4.2	Transistor sizing in the current buffer	72
4.3	Effective DC measured in-vitro	86
4.4	Comparison of stimulator systems	91
5.1	BioADC input impedance across chopper frequencies	119
5.2	Bidirectional chip specifications and prior art	129

List of Figures

2.1	Types of bidirectional neural interfaces	11
2.2	Motor prosthetic sensory feedback	17
2.3	The Neurochip closed-loop stimulation system	33
2.4	On-chip signal processing techniques for neural data	37
2.5	Closed-loop seizure control	39
3.1	Block diagram architecture for the wireless ECoG system	48
3.2	The wireless ECoG system on untethered rats	53
3.3	<i>In-vivo</i> results for the UWB based wireless system	57
3.4	Simultaneous ECoG and accelerometer readings	60
3.5	Modulation of ECoG sub-band power during periods of high activity and inactivity	61
3.6	Seizure activity in a rodent model of cardiac arrest captured with the wireless system	62
4.1	Stimulator IC block diagram	68
4.2	DAC and calibration circuits	69
4.3	Current buffer circuits	71
4.4	Multiplexing multiple stimulators to the calibration circuit	73
4.5	Tripolar calibration	77
4.6	Cuff electrode impedance	78
4.7	Micrograph of the stimulator chip	79
4.8	DAC calibration results	80
4.9	Current matching for charge balancing results	82
4.10	Effects of noise and drift on charge balancing	83
4.11	Tripolar stimulation accuracy	84
4.12	Stimulator <i>in-vitro</i> results	85
4.13	Experimental setup for <i>in-vivo</i> testing of stimulator chip	87
4.14	Physiological effects of current-steering stimulation	88
4.15	Additional <i>in-vivo</i> responses to current-steering stimulation	89

LIST OF FIGURES

4.16	Schematic for an ideal R - βR splitter	95
4.17	The effective ladder resistance depends on β and the terminating resistor λ	96
4.18	Current splitting at the k^{th} tap	97
5.1	Block diagram of the bidirectional neural interface chip	101
5.2	BioADC block diagram schematic	103
5.3	OTA and comparator schematics	105
5.4	Second-order comb-decimator schematic	107
5.5	Mixed-signal servo-loop schematic	109
5.6	Stimulator architecture in the bidirectional neural interface chip	111
5.7	Micrograph of the bidirectional neural interface chip	113
5.8	Spectrum of the 1-bit bioADC output for a 24 Hz input tone	114
5.9	Frequency response for different settings of OSR	115
5.10	SNDR for the bioADC circuits	116
5.11	Noise PSD for the bioADC circuits	117
5.12	BioADC input impedance across chopper frequencies	118
5.13	Percent variation in the gain across channels	119
5.14	Crosstalk between the recording and stimulation blocks	120
5.15	In-vivo validation of the bioADC	123
5.16	Simultaneous recording and stimulation with the bidirectional neural interface chip	124
6.1	System level diagram of the for the neuromodulation system	132
6.2	Experimental setup for the closed-loop vagus nerve stimulation experiments	135
6.3	ECG and time-domain stimulation waveforms from the closed-loop experiment	136
6.4	Results of closed-loop heart rate control experiments	138
6.5	Measured heart rate and stimulation frequency during a > 1200 s closed-loop control trial	139

Chapter 1

Introduction

This thesis presents the development of neural interface circuits and systems for a wide ranging field of applications, from wireless neural monitoring in subjects with neural injuries, to therapeutic bidirectional systems with both sensing and stimulation capabilities. The innovative aspects of this thesis include a wireless electrocorticographic monitoring system for long-term recording in awake-behaving rodents, a very-large-scale-integration (VLSI) chip with current steering capabilities for targeted neural stimulation, and a bidirectional VLSI chip with both sensing and stimulation circuits for a closed-loop therapeutic interface with the nervous system. This introductory chapter serves three purposes. First, the specific aims of this work will be described. Second, the contributions to the state-of-the-art will be summarized. Finally, the organization of the remainder of the thesis will be explained.

1.1 Specific Aims

Aim 1: To combine a multichannel neural recording chip with a wireless module to form an electrocorticographic recording system suitable for untethered rats.

Rational: Physical tethers imposed on laboratory animals, such as head and body restraints, constrain the environment in which experiments take place and the types of behaviors that can be studied. Further, clinically relevant biomarkers may occur sparsely in time, yet catching such activity may be critical.

Approach: We will combine a highly power-efficient custom VLSI neural interface with a power-efficient telemetry chip to realize our system. Additionally, behavioral monitoring will be performed via an accelerometer, which will provide quantitative measurements of the subjects' activity.

Expected Results: We expect the system will provide high quality electrocorticographic recordings in untethered rats and will allow detection of sparse, clinically relevant biomarkers.

Aim 2: To design a custom VLSI neural stimulation chip with on-chip charge balancing and the ability to steer currents *in-vivo*.

Rational: Electrical stimulation of neural tissue is a widely used tool in basic and clinical neuroscience and neuroengineering. Major challenges for neurostimulation devices include achieving charge balanced stimulation waveforms for safety, and creating stimulation waveforms that can activate targets with some specificity. Thus

CHAPTER 1. INTRODUCTION

there is a need for compact circuits to measure currents within and across stimulation channels to ensure charge balanced and current-steerable waveforms.

Approach: We propose an architecture that includes a shared auxiliary circuit for 1) digital-to-analog converter calibration, 2) matching the anodic and cathodic currents within channels for charge balancing, and 3) matching anodic and cathodic currents across channels for current steering.

Expected Results: We expect our chip will provide accurate charge balanced stimulation with high resolution digital amplitude selection and across channel current steering.

Aim 3: To design a custom VLSI bidirectional neural interface chip with a mixed-signal recording front-end and a current-steering neural stimulator.

Rational: Bidirectional neural interfaces – systems that combine both recording and stimulation into a unified system – have potential to advance the state of the art in a broad set of fields. This motivates and necessitates the design of VLSI chips with the entire recording pipeline – signal conditioning through digitization – alongside neural stimulation circuits.

Approach: We will develop a bidirectional chip for power-efficient acquisition and digitization of biopotential signals alongside the current-steering stimulator from Aim 2. We will build upon previous works that use a $\Delta\Sigma$ loop to directly generate the digitized output. For maximum area efficiency, an array of stimulators will be fabri-

CHAPTER 1. INTRODUCTION

cated on the same die, and a digital controller will facilitate the coordination of the two modules with an external programmable device.

Expected Results: We expect this chip will provide a low-noise and low-power recording front-end alongside the flexible stimulation platform from Aim 2, which will enable a closed-loop stimulation system.

1.2 Contributions

1.2.1 Aim 1

Two versions of a wireless ECoG system were developed by integrating a VLSI neural interface chip with a wireless transmitter¹. The first system utilized an ultra-wideband (UWB) transmitter module, fabricated in a 0.5 μm silicon-on-sapphire (SOS) technology². Along with a microcontroller to coordinate their operations, the system amplified, filtered, digitized and transmitted 16 channels of neural data at a rate of 1 Mbps. Combined with a 200 mAh battery, the system weighed 24 g and could be chronically mounted on small animals. The system drew 4.8 mA from a 3.7 V battery, and could record continuously for up to 40 hours. The second version made use of a commercial telemetry chip and also included an accelerometer for quantitative behavioral data. Combined with a 400 mAh battery, the system weighed

¹This contribution was performed in collaboration with Mohsen Mollazadeh

²The UWB chip was provided by Wei Tang and Prof. Eugenio Culurciello of Yale University

CHAPTER 1. INTRODUCTION

29 g, and drew 5.1 mA from a 3.7 V battery. This system acquired simultaneous ECoG and behavioral data from a pre-clinical rodent model of cardiac arrest and provided evidence of seizure activity 14 hours into the recording. *IEEE Transactions on Biomedical Circuits and Systems* vol. 5(2), pp. 112–119, 2011. *IEEE Biomedical Circuits and Systems Conference (BioCAS)*, 2011, pp. 237-240.

1.2.2 Aim 2

An 8-channel current steerable, multi-phasic neural stimulator with on-chip current DAC calibration and residue nulling for precise charge balancing was designed. Each channel consisted of two sub-binary radix DACs followed by wide-swing, high output impedance current buffers providing time-multiplexed source and sink outputs for anodic and cathodic stimulation. A single integrator was shared among channels and served to calibrate DAC coefficients and to closely match the anodic and cathodic stimulation phases. Following calibration, the differential non-linearity was within ± 0.3 LSB at 8-bit resolution and the two stimulation phases were matched within 0.3%. Individual control in digital programming of stimulation coefficients across the array allowed altering the spatial profile of current stimulation for current steering. Combined with the self-calibration and current matching functions, the current steering capabilities integrated on-chip support use in fully implanted neural interfaces with autonomous operation for highly selective and adaptive stimulation under variations in electrode and tissue conditions. Current steering stimulation

CHAPTER 1. INTRODUCTION

through a multi-channel cuff electrode on the sciatic nerve of a rat was demonstrated.

IEEE Biomedical Circuits and Systems Conference (BioCAS), Oct 2013, pp. 89-92.

Manuscript submitted to IEEE Transactions on Biomedical Circuits and Systems.

1.2.3 Aim 3

A bidirectional neural interface with a 4-channel biopotential analog-to-digital converter (bioADC) and a 4-channel current-mode stimulator in 180nm CMOS was designed. Each bioADC channel comprised a continuous-time first-order $\Delta\Sigma$ modulator with a chopper-stabilized OTA input and current feedback, followed by a second-order comb-filter decimator with programmable oversampling ratio. Each stimulator channel contained two independent digital-to-analog converters for anodic and cathodic current generation. A shared calibration circuit matched the amplitude of the anodic and cathodic currents for charge balancing. Powered from a 1.5V supply, the analog and digital circuits in each recording channel drew on average 1.54 μA and 2.13 μA of supply current, respectively. The bioADCs achieved an SNR of 58 dB and a SFDR of >70 dB, for better than 9-b ENOB. Intracranial EEG recordings from an anesthetized rat were shown and compared to simultaneous recordings from a commercial reference system to validate performance *in-vivo*. Additionally, bidirectional operation was demonstrated by recording cardiac modulation induced through vagus nerve stimulation, and performing closed-loop control of cardiac rhythm. *IEEE Biomedical Circuits and Systems Conference (BioCAS)*, Oct

2015, pp. 14. *Manuscript submitted to IEEE Transactions on Biomedical Circuits and Systems.*

1.3 Thesis Organization

Chapter 2 introduces applications and circuit architectures for bidirectional neural interfaces. It provides a broad background for the types of problems to which the technologies developed in the remainder of the dissertation can be applied³.

Chapter 3 describes the design of our wireless ECoG system and presents the *in-vivo* data collected with the system from untethered rodents.

Chapter 4 details our stimulator architecture and the CMOS design of the stimulator chip. Both benchtop characterizations, and *in-vivo* demonstrations of the circuits are presented.

Chapter 5 presents the circuit design of the $\Delta\Sigma$ recording front-end, and the integration of the stimulator from Chapter 4. The front-end is characterized in terms of signal-to-noise-and-distortion (SNDR) ratio, input-referred noise, input impedance and common-mode rejection ratio (CMRR). Intracranial EEG (iEEG) recordings collected simultaneously with a commercial system are presented, and *in-vivo* bidirectional operation is demonstrated as well.

Chapter 6 extends the work of Chapter 5 and details a closed-loop neuromodulation system. Cardiac rhythm in anesthetized rodents is controlled by implementing a

³This chapter was written in collaboration with Matthew Masters

CHAPTER 1. INTRODUCTION

proportional-plus-integral controller on a PC in real-time with the bidirectional chip.

Finally, Chapter 7 summarizes the dissertation and discusses future directions. Important improvements that could be made to the developed technologies are discussed, and the importance and potential impact of the work is described.

Chapter 2

Bidirectional Neural Interfaces – Applications and VLSI Circuit Implementations

Implantable devices that interface with the nervous system are becoming increasingly viable treatment options in prosthetic and therapeutic applications. Motor prosthetic devices record the electrical activity of the cerebral cortex,^{1,2} or of peripheral nerves,³ to decode movement intention and actuate a robotic device. Modern neurotherapeutic devices stimulate the nervous system to treat epilepsy,^{4,5} to treat chronic pain,⁶ and to aid rehabilitation following spinal cord injury.^{7,8}

In the aforementioned applications, natural neural activity is *either* recorded *or* perturbed. The purpose of this chapter is to review evidence that bidirectional inter-

CHAPTER 2. BIDIRECTIONAL NEURAL INTERFACES

faces – systems that combine both recording and stimulation into a unified system – have potential to advance the state of the art in a broad set of fields.

We define systems as “bidirectional” from a device engineer’s point of view. For the purposes of this chapter, a system is “bidirectional” if it processes information extracted from a biological system and delivers information back to the biological system, regardless of the nature of that information. For example, a system that processes information from an efferent branch of the nervous system, and delivers stimulation back to the efferent branch is bidirectional by our definition, even though the information flow is unidirectional.

Specifically, the devices covered will fall into one of three categories illustrated schematically in Fig. 2.1: 1) neuroprosthetic, 2) neuro-repair, and 3) neurotherapeutic. The first category, neuroprosthetic systems, consists of devices that restore motor function. Neuroprosthetic devices are being improved upon by providing the user with sensory information conveyed through electrical stimulation of the nervous system (Fig 2.1(a)). The second category, neuro-repair, consists of systems that facilitate rehabilitation from brain injuries such as stroke and traumatic brain injury (TBI). These devices pair recorded brain activity with stimulation to modulate connections of neuronal populations or circumvent a damaged region (Fig 2.1(b)). The third category, neurotherapeutic systems, consists of devices that treat nervous system disorders (Fig. 2.1(c)). The debilitating effects of epilepsy can be mitigated in some patients using a device that detects seizure activity and truncates it with elec-

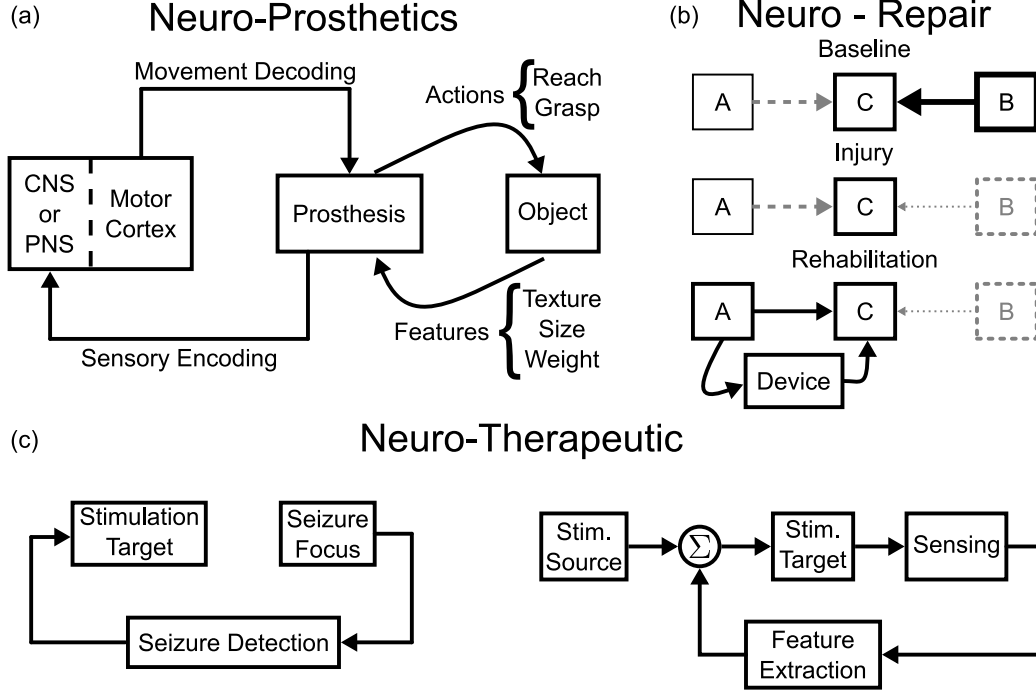


Figure 2.1: Block diagram illustrations of three classes of bidirectional neural interfaces covered in this review. (a) Bidirectional neuroprosthetic devices decode movement intention and deliver sensory information to the user, or drive muscle or nerve stimulation. (b) Neuro-repair devices pair neural stimulation with recorded neural activity. A, B, and C represent different neuronal populations. Dark arrows represent strong connections, and gray arrows represent weak connections. The weak connection between A and C is strengthened through hebbian mechanisms¹⁰ after injury to B. (c) Neurotherapeutic devices treat neurological disorders. This could entail delivering stimulation to truncate a detected seizure (left), or altering the pattern of stimulation delivered to the sub-thalamic nucleus (STN) for treatment of PD (right).

trical stimulation.⁹ Additionally, bidirectional neurotherapeutic devices may improve the efficacy of open-loop deep-brain stimulation by modulating stimulation parameters based on biomarkers detected in real time.

This chapter is organized as follows. In Section 2.1 we discuss in detail how bidirectional prostheses are currently being applied to the variety of clinical needs mentioned above. Then, in Section 2.2, we describe implementations of these systems,

and highlight unique design considerations and challenges for these systems.

2.1 Applications

2.1.1 Neuroprostheses

The following subsections present recent advancements in the field of neuroprostheses as pertaining to motor neuroprostheses and providing sensory feedback to users of such systems.

2.1.1.1 Motor Neuroprostheses

Brain-machine-interfaces (BMIs) traditionally decode movement intention from neural signals to control an artificial device such as a robotic arm or computer cursor. However, an alternative strategy is to use decoded signals to drive spinal, peripheral nerve, or muscle stimulation. These systems contain both neural sensing and electrical stimulation capabilities.

Moritz *et al.* trained non-human primate (NHP) subjects to control the firing rate of single neurons, which was used to control graded functional electrical stimulation (FES) of wrist muscles paralyzed by a peripheral nerve block.¹¹ This created an artificial pathway between the subjects' cortex and the muscles, allowing them to control flexion and extension of the wrist despite compromised neural pathways. Ethier *et*

CHAPTER 2. BIDIRECTIONAL NEURAL INTERFACES

al. expanded on this strategy, and restored grasping ability in two NHP subjects by translating population activity in motor cortex into FES of multiple muscle groups.¹² Finally, Nishimura *et al.* used local field potentials (LFPs) to control spinal stimulation. Additionally, the authors showed that a “recurrent” artificial connection could be used to restore some functionality lost due to injury. An NHP with partial upper limb paralysis collected juice rewards by producing and maintaining wrist torques of sufficient magnitude to cross an experimenter-defined threshold. In several sessions, the threshold was set such that the NHP could not naturally produce the torque necessary to collect rewards, due to the injury. The authors applied spinal stimulation upon detection of weak EMG signals in the paretic muscle. The EMG-triggered spinal stimulation amplified native muscle activity, restoring the subject’s ability to complete the task.¹³

The aforementioned systems are bidirectional in the sense that they record and stimulate neural tissue. However, for patients in which sensory pathways are not intact, these systems still suffer from the same drawback as traditional BMIs, in that they rely solely on a feed-forward control strategy – they do not provide sensory feedback. Bidirectional strategies can overcome this limitation by involving the somatosensory system, and are covered in the following subsections.

CHAPTER 2. BIDIRECTIONAL NEURAL INTERFACES

2.1.1.2 Sensory Feedback

Coordinated movements are facilitated by a rich set of sensory data communicated to the brain.¹⁴ Such movements, therefore, are impaired in patients lacking sensory feedback.¹⁵ In such cases, visual feedback alone is often relied upon in neuroprosthetic control for goal-directed movements.^{1,2} Although it has been shown that vision provides feedback adequate for some enhancement of movement accuracy in these patients,¹⁶ other evidence suggests that somatosensory feedback would further enhance control of a prosthetic device.¹⁷

In 1983 it was shown that natural sensory perception can be reproduced by electrically stimulating peripheral nerves.¹⁸ Experimental work in the late 1990s and early 2000s offered strong evidence that providing somatosensory feedback, via electrical stimulation, was possible.¹⁹ These findings have been replicated and supported by other contemporary work and work that has followed more recently.²⁰⁻²² These pioneering studies provided a firm scientific basis for future bidirectional motor prosthetic systems.

The studies mentioned and referenced above demonstrated the viability of providing somatosensory information via cortical and peripheral nerve stimulation. The following sections present recent work performed in (1) cortical and (2) peripheral nerve stimulation.

Sensory Feedback via Cortical Stimulation

In 2011, O'Doherty *et al.* demonstrated a system that provided sensory informa-

CHAPTER 2. BIDIRECTIONAL NEURAL INTERFACES

tion via cortical stimulation in a bidirectional motor prosthesis.²³ Using temporally patterned intracortical microstimulation (ICMS), they provided tactile feedback as part of a brain-machine-brain interface. The authors presented NHP subjects with multiple visually identical objects on a screen as subjects initially used a manual joystick to explore a virtual environment. As the cursor or virtual arm touched objects, different patterns of ICMS were applied to somatosensory cortex (S1) in an effort to convey different textures. After training the NHPs in this paradigm, O’Doherty and colleagues engineered a complete closed-loop brain controlled system. They simultaneously decoded movement signals from the motor cortex and delivered one of three ICMS patterns (null, low frequency or high frequency) to S1 to represent the texture of the objects in the virtual space.

One hurdle in simultaneously decoding motor signals and providing sensory feedback via ICMS lay in the recording artifacts caused by stimulation, which can be several orders of magnitude larger than the signals being recorded. To circumvent this issue, O’Doherty *et al.* used alternating 50 ms intervals dedicated solely for either neural decoding or ICMS delivery. In this way, they guaranteed sufficient neural data would be available for decoding.

To extend this sensory feedback paradigm and provide more intuitive feedback with ICMS, investigations of stimulation parameters and strategies were conducted by Tabot *et al.*²⁴ The authors hypothesized that stimulation applied in a way that attempts to reproduce the natural neural encoding of somatosensation would provide

CHAPTER 2. BIDIRECTIONAL NEURAL INTERFACES

intuitive sensory feedback for a neuroprosthetic user. Contact location information was conveyed through precise stimulation of the regions with corresponding receptive fields in S1, pressure information was conveyed by stimulation amplitude, and the timing of object interaction was presented through phasic stimulation at the onset and offset of object interaction.

Furthermore, the group used a standard psychophysical paradigm to quantify the relationship between electrical stimulation amplitude and perception in two NHP subjects. With data from similar experiments using mechanical stimulation, they mapped perceived magnitudes of mechanical stimuli to perceived magnitudes of electrical stimuli to create a psychometric equivalence function.^{24,25} The authors then conducted two experiments to test whether stimulation amplitude, scaled in this manner, would be interpreted naturally. First, they applied mechanical stimulation to a prosthetic hand equipped with sensors, and converted the mechanical stimulation magnitude to electrical stimulation magnitude using the psychometric equivalence functions. The accuracy with which the subjects performed a discrimination task with the artificial sense of touch was similar to their natural ability. Second, the authors verified their psychometric equivalence function by having the subjects compare the amplitudes of mechanical stimulations with those of electrical stimulations, showing that subjects made errors in discriminating between stimuli as expected when the sensations being delivered were most similar. In conclusion, this work provides a framework to transform pressure sensor data from a prosthetic hand into patterned ICMS that can be

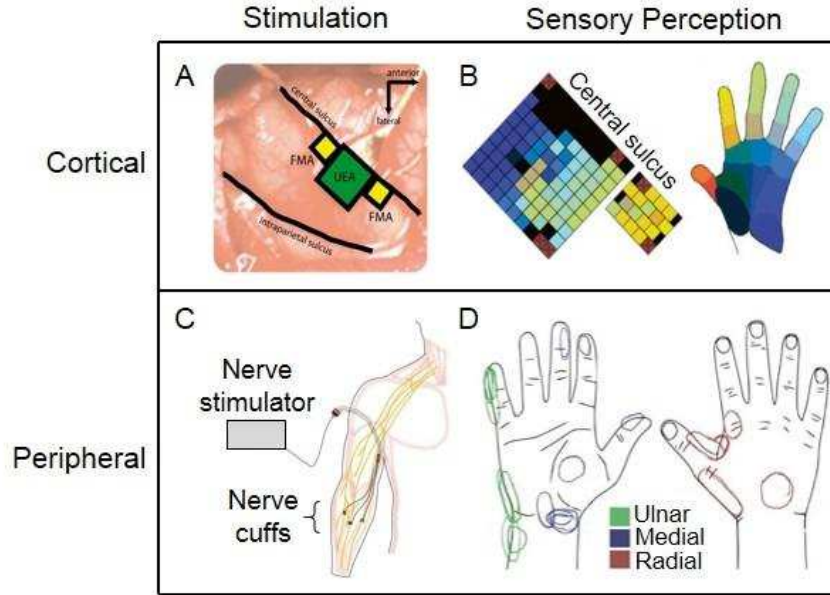


Figure 2.2: Depiction of the two major sensory feedback paradigms: cortical and peripheral neural stimulation. (a) Cortical stimulation site.²⁴ (b) Somatosensory map in the stimulated region of the cortex along with perception locations on the NHP's hand.²⁴ (c) Peripheral nerve stimulation setup with nerve cuff electrodes implanted in the forearm of the human amputee subject.²⁶ (d) Sensory perception location on the subject's phantom hand elicited by peripheral nerve stimulation.²⁶ Adapted with permission from.^{24, 26}

interpreted naturally.

Sensory Feedback via Peripheral Nerve Stimulation

A multitude of peripheral nerve stimulation techniques exist. Perhaps the most general categories of these techniques are penetrating and non-penetrating. Within the category of nerve-penetrating stimulation are longitudinal intrafascicular electrodes (LIFEs),^{27, 28} and transverse intrafascicular electrodes (TIMES).²⁹ Non-penetrating systems include standard nerve cuff electrodes^{30, 31} and flat interface nerve electrodes (FINEs).^{32–34} A few significant studies will highlight the latest development of these

CHAPTER 2. BIDIRECTIONAL NEURAL INTERFACES

systems.

In 2005, Dhillon and Horch successfully used four to eight LIFEs in six long-term upper limb human amputees to produce graded, discrete sensations of touch and movement of their phantom hands as feedback to a neurally controlled artificial arm.²⁷ Similar work was performed by Rossini *et al.* in 2010.²⁸ This team implanted four LIFEs into the median and ulnar nerves of an amputee, and was able to detect movement related nerve activity over a period of four weeks. A critical note is that, although nerve signals were recorded for the duration of the experiment, stimulation efficacy decayed after 10 days. This study also demonstrated real-time control of motor output for three actions, localized and reproducible hand/finger sensations through selective stimulation, reversal of plastic changes in the primary motor cortex following sensory stimulation, and the alleviation of phantom-limb syndrome. Although this study presents many impressive results which might recommend the use of intrafascicular electrodes, the decay of stimulation efficacy illustrates one of the major obstacles of using the electrodes for long-term recording and stimulation. The tissue response following device insertion significantly impacts these functions.³⁵

More recently, Raspopovic *et al.* demonstrated a peripherally interfaced bidirectional prosthetic system using TIMEs, allowing an amputee to control a prosthetic hand and receive somatosensory feedback.²⁹ The group used surface EMG recordings of the residual limb to decode movement intention and simultaneously electrically stimulated peripheral nerves to provide sensory feedback. The prosthetic

CHAPTER 2. BIDIRECTIONAL NEURAL INTERFACES

hand was outfitted with pressure sensors on the index and little fingers. Raspopovic and colleagues linearly transformed readings from the sensors into stimulation currents, scaled in such a way as to prevent the stimulation currents from reaching pre-determined pain limits, and ensuring the sensor output exceeded some minimum threshold before any stimulation was applied. The authors report that an amputee subject was able to use the bidirectional prosthesis to control three levels of force applied by a prosthetic hand (low, medium and high), and to discriminate between objects based on their composition (wood, plastic, or cotton) and shape (cylinder, large sphere, small sphere), without visual or auditory feedback.

In contrast to the nerve-penetrating LIFE and TIME electrodes, nerve-cuff electrodes are placed around the nerve. Clippinger *et al.* performed pioneering work with nerve cuff electrodes around the median nerve of amputees in 1974.³⁰ More recently, Polasek *et al.* showed that nerve-cuff electrodes were both safe and stable in human subjects over periods spanning up to three years.³¹ The FINE electrode is a nerve cuff electrode designed to flatten the nerve to spread out the fascicles. Using FINEs, Tyler and Durand demonstrated better access to nerve fibers for more selective stimulation and recording abilities than traditional nerve cuff electrodes.³² Schiefer and colleagues applied an eight-contact FINE to the human tibial nerve, which allowed selective activation of those muscles responsible for dorsiflexion, plantarflexion, ankle inversion, and ankle eversion - a level of specificity likely not achievable with a circular nerve-cuff electrode.³³

CHAPTER 2. BIDIRECTIONAL NEURAL INTERFACES

Most recently, Tan *et al.* implanted two eight-contact FINEs and one four-contact spiral electrode around the median, ulnar, and radial nerves of two 46 year old trans-radial amputee subjects.³⁴ By varying the location and pattern of stimulation, the group produced repeatable, stable, and naturalistic touch perceptions at many locations on the phantom extremity of their subjects. The group reported consistent threshold and impedance measures twelve months post-implantation. These aspects, along with the ability to selectively stimulate the nerves at 19 of the 20 available contacts, provide strong support for the chronic use of multi-contact FINEs for neural feedback in the PNS.

2.1.1.3 Comparison of CNS and PNS stimulation

Cortical and peripheral stimulation methods have distinct advantages and challenges. They also tend to serve different patient populations. For example, a patient suffering from a complete spinal cord injury would not benefit from peripheral nerve stimulation but would require cortical stimulation techniques to receive sensory feedback.

A benefit exploited by cortical stimulation is the highly organized structure of the tactile somatosensory cortex (Brodmann’s area 3b). In low-level somatosensory cortex, it is straightforward to map stimulation location to percept location (Fig. 2.2). The somatotopy of the brain, however, can reorganize itself following injury, leading to a drastic change in cortical representation of the affected and neighboring

CHAPTER 2. BIDIRECTIONAL NEURAL INTERFACES

body parts.^{36,37} In cases with substantial cortical remapping, it may be difficult to artificially induce a percept in a part of the body that is no longer strongly represented on the cortex.

Compared with the somatosensory cortex, the fibers within a peripheral nerve are not arranged with a clear somatotopic map. Activating a large portion of a nerve produces a feeling of paresthesia, a tingling or slight burning sensation.^{30,34} However, the PNS is not completely chaotic. Stewart showed that afferent and efferent nerve fibers innervating similar regions of skin or muscle are generally grouped together “in accord with the somatotopic organization of the motor and sensory pathways in the central nervous system”.³⁸ Another complication is the fact that large nerve fibers are more easily activated by stimulation than small fibers. It has been proposed, though, that selective stimulation of even the smallest nerve fibers may be achievable by novel electrode design. Weber and colleagues advocate for high-density, nerve-penetrating microelectrode arrays with feature sizes on the order of microns.³⁹ Lacour *et al* developed a microchannel nerve interface which separated nerve fibers by promoting their growth into individual microchannels.⁴⁰ Fitzgerald *et al.* showed that a microchannel design could facilitate selective stimulation of individual nerve fibers.⁴¹

One likely benefit of peripheral nerve stimulation is that signals can be accessed before they are subjected to the significant processing performed by the somatosensory system which transforms sensory input into perception of texture and shape.⁴² It is likely that an artificial stimulus would be more naturally perceived if the signal

CHAPTER 2. BIDIRECTIONAL NEURAL INTERFACES

undergoes the natural processing of the nervous system, beginning with the activation of the lowest order sensory neurons in the peripheral nervous system.

Finally, due to the invasiveness of both methods, the majority of research has been performed on NHP subjects until very recently. However, the barrier to human subject testing is diminishing, particularly for peripheral interface systems. For example, Tan *et al.* developed a safe and reliable nerve interface technology, which allowed them to derive biomimetic stimulation patterns by implanting multichannel electrode arrays and having the subject directly describe the sensations produced.³⁴

2.1.2 Neuro-repair

Restoring function or at least compensating for deficits following brain injury or disease is a potential application for bidirectional neural interfaces. Such interfaces are being developed to treat motor and cognitive deficits.^{43–47} The strategies used to implement these two types of restorative prostheses (motor and cognitive) can be subtly different. In both cases, neural stimulation is provided in response to recorded activity. However, the goal of restorative motor prostheses is to induce plastic changes in the brain that allow injured subjects to regain lost function. In contrast, in the cognitive prostheses discussed here, a biomimetic model is constructed to bypass a damaged region of brain.

In the subsections to follow, we first discuss major results from bidirectional neural interfaces applied to the motor system (Section 2.1.2.1), and then describe the

CHAPTER 2. BIDIRECTIONAL NEURAL INTERFACES

advances being made to enable memory prostheses (Section 2.1.2.2).

2.1.2.1 Restorative Motor Prostheses

The following process has been hypothesized to facilitate the recovery of functions lost to brain injury: activity recorded at one electrode acts as a “trigger” for stimulation at a different, “target” electrode. Mavoori *et al.* first developed such a device, called the Neurochip,⁴⁸ and soon after, Jackson *et al.* showed that it could induce plastic changes in neural connectivity *in-vivo*.¹⁰

In a series of experiments, this group implanted autonomously operating Neurochips on freely behaving NHP subjects over periods of days, and characterized the changes in functional connectivity that resulted.^{10,49,50} Interestingly, the nature of the device-induced reorganization, as well as the time-course of the effects, differed depending on the locations of trigger and target. For example, Jackson *et al.* used a trigger and stimulation target both within motor cortex. The Neurochip shifted the efferent properties of the trigger network in the direction of the target network, and the effect was maintained for more than a week after the device was deactivated.¹⁰ Alternatively, Lucas *et al.* used muscle activity as a trigger, and motor cortex as the stimulation target; the Neurochip reorganized the connectivity of neurons in M1 associated with the trigger muscle, but these effects extinguished within 24 hours of device deactivation.⁴⁹ Finally, Nishimura *et al.* used a trigger within motor cortex, and a target within spinal cord. The authors selectively strengthened or weakened the

CHAPTER 2. BIDIRECTIONAL NEURAL INTERFACES

corticospinal connections under study by varying the timing of the stimulus relative to the trigger.⁵⁰ The durations of plastic effects were mixed; some changes lasted up to two days after stimulation ceased. A complete description of these works, which lay a neuroscientific foundation for the clinical application we describe next, is beyond the scope of this paper, interested readers are directed to,^{44,51} which provide more comprehensive treatments of these studies.

Since the initial work from 2006,¹⁰ a number of labs have independently used this closed-loop stimulation paradigm to demonstrate similar results.^{52,53} These findings have fueled speculation that bidirectional neural interfaces could aid in the rehabilitation process from various brain injuries.^{43,44,54,55} Guggenmos *et al.* used a rodent model of TBI to test the hypothesis that a bidirectional neural interface that delivers “spike-triggered” stimulation can facilitate rehabilitation.⁵⁶ To enable this study, the authors created a custom device modeled after the Neurochip.⁴⁸ Azin *et al.* designed an application-specific integrated circuit (ASIC) that contained recording and stimulating circuits as well as signal processing circuits implementing the algorithm described above.^{57,58}

Guggenmos and colleagues mounted the device on injured rats, and could deliver closed loop stimulation continuously for 24-hours before requiring a change of battery. Then, during recovery from brain injury, the authors provided one group of rodents with closed-loop, spike-triggered stimulation, and provided another group with constant frequency, open-loop stimulation. Over the course of recovery, rats regularly

CHAPTER 2. BIDIRECTIONAL NEURAL INTERFACES

performed a reaching task to quantify forelimb dexterity. The performance of rats in the closed-loop group improved at a faster rate than those in the open-loop group. The authors analyzed the spiking activity recorded in both groups, and their results suggested different mechanisms mediating recovery in the two cases. This research represents an encouraging step forward, and successful replication of the results in higher order animal models may clear the way for new therapies for human brain injury.

2.1.2.2 Restorative Cognitive Prostheses

One strategy for cognitive prostheses is to replace a damaged region of the brain with a biomimetic model. This model mimics how that region translates the spatial and temporal characteristics of neural firing at its input into a unique pattern at its output. Berger *et al.* developed a bio-inspired multiple-input, multiple-output (MIMO) model that could mimic the input-output relationship of a region of brain. The model parameters were obtained by recording spike trains from neurons projecting into the region concurrently with spike trains from neurons projecting out.^{47,59} While this model is general, in the sense it could be applied to any region of brain, the authors focus on the hippocampus and behavioral tests of memory.

Using a delayed nonmatch to sample (DNMS) paradigm with rats, Berger *et al.* showed that the MIMO model could predict, in real time, when the subject was likely to make an error due to poor encoding of the stimulus location.⁶⁰ The authors then

CHAPTER 2. BIDIRECTIONAL NEURAL INTERFACES

stimulated the hippocampus during the task, which improved performance. Critically, the stimulation patterns were derived from the MIMO model. Furthermore, the authors created a pharmacological lesion in the hippocampus that impaired performance in the DNMS task. Berger and colleagues restored performance to nearly baseline levels by stimulating with model-derived patterns online.⁶⁰ More recently, Hampson *et al.* demonstrated similar results in non-human primate models,⁶¹ and Opris *et al.* applied the same principles to prefrontal cortex.⁶²

2.1.2.3 Future for Neuro-repair Devices

The experimental evidence supporting a role for bidirectional interfaces in rehabilitation from brain injury is largely speculative and preliminary. Neural implants may one day improve rehabilitation outcomes for patients with brain injuries such as TBI and stroke. However, more evidence is needed supporting the beneficial effects of closed-loop stimulation. Previous failures in this field can partially be attributed to a rush to clinical trials in humans.⁵⁵

Here we’ve seen bidirectional systems applied to both the motor system and the limbic system. In the case of motor rehabilitation, both closed loop and open loop stimulation have beneficial effects, albeit by seemingly different mechanisms. Modeling by Kerr *et al.* indicate that open-loop stimulation restores a general drive signal.⁶³ In memory prostheses however, the application of stimulation was not enough to improve performance;⁶⁰ the spatio-temporal properties of stimulation were critical, just

CHAPTER 2. BIDIRECTIONAL NEURAL INTERFACES

as timing was critical to reshaping neural connectivity as shown by Jackson *et al.*, Lucas *et al.*, and Nishimura *et al.*^{10,49,50} These plastic changes induced by closed-loop electrical stimulation may underlie some of the results seen with memory prostheses. Interestingly, Hampson *et al.* demonstrated that over time, stimulation with MIMO model-derived patterns improved DNMS task performance on single trials when stimulation was not performed.⁵⁹ This indicates stimulation induced some fundamental change within the underlying biology. Once stimulation was stopped permanently, these changes decayed over a timescale of days.⁵⁹

The works discussed above all represent exciting milestones in technological development and experimental applications. Several questions regarding the use of bidirectional neuro-repair devices require further study. For restorative motor prostheses, would temporally non-regular open loop stimulation also be an effective therapeutic option in place of closed loop⁵⁶? This option should be explored because it could reduce system complexity. Perhaps the biomimetic modeling approach would benefit restorative motor prostheses. Berger *et al.* demonstrated a moderate benefit of “generic” stimulation patterns, derived from data from multiple animals.⁶⁰ System complexity could further be reduced if the online implementation of the computationally expensive biomimetic modeling could be bypassed. One strategy would be to use a model to derive appropriate stimulation patterns offline, then, a simpler algorithm be used to decide online, when to stimulate. Finally, further miniaturization and full implantation of the devices, as opposed to the head-mounted approach, may result

CHAPTER 2. BIDIRECTIONAL NEURAL INTERFACES

in more robust systems, as the interface between the electrodes and the electronics in some cases can lead to device failure.⁵⁶

2.1.3 Neurotherapeutics

Electrical stimulation has been used for many years to treat a variety of neurological disorders. A large clinical trial, conducted 20 years ago, validated the ability of vagus nerve stimulation (VNS) to reduce the frequency of seizures. VNS therapy, for more than 15 years, has been an FDA approved therapy.^{4,64} Deep-brain stimulation (DBS) has had major success treating movement disorders such as essential tremor (ET) and Parkinson’s disease (PD).⁶⁵ Likewise, DBS has been demonstrated to mitigate symptoms of obsessive-compulsive disorder and depression.^{66,67}

These clinical successes were all based on open-loop stimulation. In the following subsections, we will show how bidirectional neural interfaces might improve upon these conventional therapies. In Section 2.1.3.1 we discuss an FDA approved device for the treatment of epilepsy, and in Section 2.1.3.2 we discuss progress made in improving deep-brain stimulation therapy.

2.1.3.1 Epilepsy

Vagus nerve stimulation was the first FDA approved stimulation therapy for epilepsy. Morris and colleagues recently reviewed available clinical data, and affirmed the therapeutic benefits of VNS and even suggests that VNS efficacy may improve

CHAPTER 2. BIDIRECTIONAL NEURAL INTERFACES

over time, though this conclusion may be confounded by the uncontrolled effects of medication.⁶⁸

Of course, VNS is not universally effective and has undesirable side-effects like hoarseness, voice change, throat pain and cough.⁴ Hence, much research has been directed at developing alternative stimulation strategies for reducing seizure frequency. These strategies include thalamic stimulation⁵ and cortical stimulation.⁶⁹

Fisher *et al.* demonstrated the benefits of open-loop thalamic stimulation in clinical trials. The authors implanted electrodes bilaterally in a thalamic nucleus mechanistically implicated in seizure propagation.⁷⁰ Stimulation reduced median seizure frequency by 40%, compared with 14.5% in the control group.⁷¹ Interestingly, both groups saw immediate seizure reductions of around 20% in the month following surgery.

A bidirectional approach was recently approved by the FDA. This commercial device, the Responsive Neurostimulator System (RNS[®]) (NeuroPace, Mountain View, CA), continuously records intracranial EEG, extracts features from these signals, and triggers stimulation on detection of epileptiform activity. Both the detection and stimulus parameters are tailored by a physician to an individual patient's needs.⁹ The electrode placement is patient-dependent, and may be located within the brain, or on its surface.⁷²

A multicenter clinical trial of this device showed a significant decrease in average seizure frequency of 37.9% compared with 17.3% in the control group during the

CHAPTER 2. BIDIRECTIONAL NEURAL INTERFACES

blinded period.⁷² Following the blinded period, the stimulator was activated for all subjects, and after two years, the median reduction in seizure frequency was 53%. Note, that the effect size for closed-loop stimulation was similar to that of open-loop stimulation discussed previously.

2.1.3.2 Movement Disorders

Another promising application is on-line detection and treatment of movement disorders like PD. Implanted electrodes are used to record LFP, and computations on those recordings are performed to detect patterns indicative of a diseased state. This information would then be used either to 1) adjust the stimulation parameters to more efficiently ease symptoms^{73,74} or 2) apply therapeutic stimulation.⁷⁵

Quantitative biomarkers of Parkinson’s disease are of great interest as they could provide a metric to automate evaluation of the therapeutic effects of stimulation. Patients implanted with deep brain stimulators currently offer scientists and clinicians brief windows of time to record from the brains of awake behaving human subjects using implanted electrodes.⁷⁶ This has implicated characteristic neural rhythms associated with movement disorders. Electrodes recording LFP in the sub-thalamic nucleus (STN) in PD patients have been shown to exhibit abnormally high power in the β band (10-35 Hz) that can be modulated by dopaminergic drugs^{77–80} or DBS.^{81,82} In addition to signals from deep brain structures, cortical signals also seem to be affected by PD. For example, Silberstein *et al.* showed that coherence in the β band

CHAPTER 2. BIDIRECTIONAL NEURAL INTERFACES

is correlated with motor deficits, a trend reversed by application of DBS.⁸³ Additionally, de Hemptinne *et al.* demonstrated that surges of γ band power (50-300 Hz) in motor cortex appear phase-locked to β rhythms recorded from STN; here too, DBS decreased the magnitude of this feature.⁸⁴

These insights open the door for a responsive neurostimulator applied to movement disorders. In fact, Rosin *et al.* used a closed-loop stimulation strategy in a non-human primate model of Parkinson’s disease, and showed it was *more* effective at reducing Parkinson’s symptoms than a standard open-loop DBS strategy.⁷⁵

Rosin *et al.* treated two NHP subjects with the neurotoxin MPTP to induce a Parkinson’s like pathology. Following the application of MPTP, subjects lose the ability to make volitional movements. This group mounted accelerometers on the subjects’ limbs to quantify motor symptoms, and used the standard deviation of the accelerometer signals as a measure of motor activity. The authors then evaluated a number of different closed-loop stimulation strategies almost identical to the those discussed in Section 2.1.2.

Activity in motor cortex acted as the “trigger” which led to initiation of a train of DBS pulses. Open-loop and closed-loop stimulation strategies increased the subjects’ ability to make volitional movements. However, the closed-loop strategy saw statistically significant improvements over standard DBS. In addition to behavioral improvements, closed-loop stimulation induced reductions in disease-state biomarkers.

2.1.3.3 Benefit of Closed-Loop Neurotherapeutics

In the clinical trial for open-loop thalamic stimulation, the device delivered $90\ \mu s$, $5\ V$ pulses at $145\ Hz$; the stimulation envelope had a 17% duty cycle, on for 1 minute and off for 5, which translated to 240 min/day.⁷¹ For closed-loop strategies, the amount of stimulation delivered varies from patient to patient, and from day to day. The median amount of stimulation delivered by the RNS[®] System was found to be 4.7 min/day.⁹ The closed-loop strategy therefore stimulates almost 50 times less often than the open-loop strategy.

This increased power efficiency is a great benefit to implantable devices in two ways. For battery powered devices, the decreased power burden allows for the use of lower capacity and thus physically smaller batteries – this can significantly decrease the size of the implant. Additionally, lower power consumption confers a longer battery lifetime. When the battery in an implanted device dies, surgery is then required to replace the battery. Therefore, longer battery lifetime means a decreased probability for needing an additional surgery in older patients, and fewer additional surgeries over the course of their life for younger patients. To develop closed-loop stimulation paradigms that hold a therapeutic advantage over their open-loop counterparts will require combinations of modeling⁸⁵ and *in-vivo* studies.⁷⁵

Bidirectional devices for treating neurological disorders, such as Parkinson's, would also benefit greatly from improved power efficiency for the same reasons. Additionally however, closed-loop systems might provide a means to automate selection of

CHAPTER 2. BIDIRECTIONAL NEURAL INTERFACES

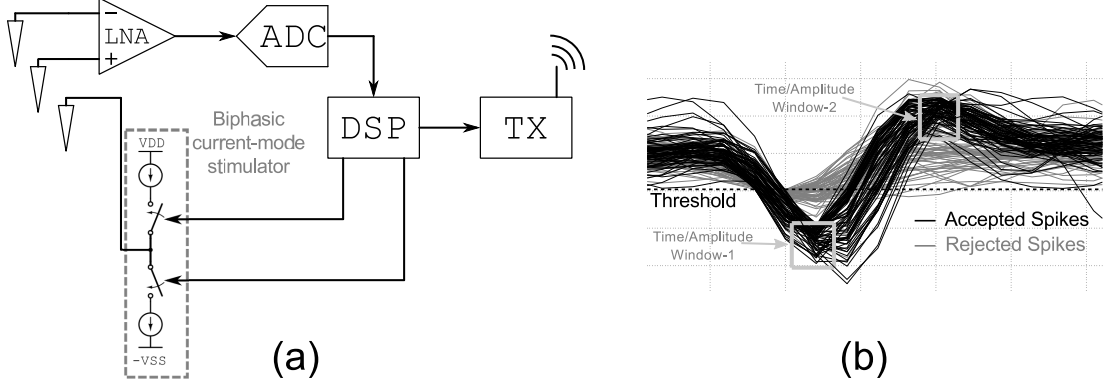


Figure 2.3: (a) Conceptual block diagram of the bidirectional neural interface used to induce plastic changes *in-vivo* in freely moving NHPs.^{10, 48–50} A low-noise amplifier (LNA) extracts neural signals, which are then digitized and passed to an analog-to-digital converter (ADC). A digital signal processing unit (DSP) runs a spike-discrimination algorithm and triggers stimulation and transmits data. (b) Graphical depiction of the spike detection algorithm: Upon passing through a threshold, the recorded signal is compared with two predefined time-amplitude windows. Waveforms that pass through both windows are classified as spikes. Two types of signals cross the threshold in this example, the black traces are counted as spikes while the grey traces are ignored.⁴⁸

DBS parameters. The parameter space for DBS is extremely large; it includes amplitude, frequency, pulse width, and temporal pattern.^{86–89} Tuning of these parameters in practice must be performed manually by a highly trained neurologist to obtain acceptable tradeoffs between alleviation of symptoms, severity of side-effects and battery life.^{90–92} Automated algorithms for the optimization of stimulation parameters are therefore being explored.⁹³

2.2 Very Large Scale Integration (VLSI) Implementations

There are numerous published examples combining recording and stimulation into a single system. In addition to the applications described above, it is a classical approach used in basic science research^{94,95} and allows for bidirectional bionic interactions.^{96–98} Here, we restrict our focus to miniaturized or implantable systems designed to treat diseases of, or injuries to, the nervous system.

Implantable systems face extremely tight constraints on both power and size.⁹⁹ In bidirectional systems, these constraints become even more difficult to satisfy due to the need for signal processing algorithms to run in real time with the recording hardware, and the adulteration of micro-volt neural signals caused by stimulation. Having established the utility of bidirectional interfaces, we turn in this section to hardware implementations of bidirectional neural interface systems.

2.2.1 VLSI Systems for Spike-Triggered Stimulation

VLSI systems intended for the applications described in Section 2.1.2 require a signal processing block capable of discriminating neural spikes in real time. For some applications, a single, tunable amplitude threshold may suffice. This requires a

CHAPTER 2. BIDIRECTIONAL NEURAL INTERFACES

low-resolution DAC to set the threshold level, and a comparator to detect threshold crossings.¹⁰⁰ Alternatively, a number of groups have used the Teager Energy Operator (TEO), an algorithm that estimates the energy of a signal,¹⁰¹ for on-chip spike detection. This method detects transient rises in signal energy above the background noise level, and can be implemented with analog¹⁰² or digital circuits.^{103,104}

The spike-detection algorithm used by Mavoori *et al.* (discussed in Section 2.1.2) is depicted graphically in Fig. 2.3(b). A state-machine waits for the input signal to cross a baseline threshold. A waveform is classified as a spike if it passes through two programmably defined time-amplitude windows (W1 and W2).⁴⁸ These time-amplitude windows are set manually based on the signals available after electrode implantation. As discussed in Section 2.1.2, pairing the output of this algorithm with electrical stimulation induces plasticity *in-vivo*.

Figure 2.3(a) depicts a block diagram of the Neurochip system discussed in Section 2.1.2. Mavoori *et al.* designed the original Neurochip system from discrete components. The authors amplified and filtered neural signals using commercial operational-amplifiers, and used a mixed-signal microcontroller to perform digitization, run the spike discrimination algorithm, and trigger a biphasic stimulator. On-board memory stored segments of recordings and spike detection statistics; the authors used an IR link to download the data. Azin *et al.* designed an eight-channel system similar to the Neurochip in a $0.35\mu m$ CMOS process. Each channel contained (1) a recording front-end with an input-referred noise of $3.42\mu V_{rms}$ in a $5.1kHz$ bandwidth, (2) a

CHAPTER 2. BIDIRECTIONAL NEURAL INTERFACES

10-bit successive-approximation (SAR) analog-to-digital converter (ADC), and (3) a constant-current biphasic stimulator. A digital processing block, shared among four channels, implemented a high-pass filter and the spike discrimination algorithm described above and in Fig. 2.3(b). Detected spikes, or patterns of spikes, autonomously triggered ICMS delivery. This processing unit consumed $12\mu W$ of power, and processed data from 4 channels, yielding an effective overhead of $3\mu W$ per channel.⁵⁷ Azin and colleagues then integrated the custom chip with a minimal set of off-chip components to comprise a fully autonomous system. The final system weighed under 2 g and had 24 hours of battery lifetime, amenable for use in unrestrained rodents.^{56,58}

2.2.2 VLSI Systems for Treatment of Epilepsy

Detection of biomarkers for both seizures and movement disorders requires more powerful digital processors than those described above. Usually, detection can be accomplished by calculating time and/or frequency domain features of a continuous EEG stream, and feeding those data to a classifier, trained on patient specific data.^{110–112}

Stanslaski *et al.* demonstrated three design innovations that make it possible to extract frequency domain features, even in the presence of a large stimulation artifact.¹¹⁰ First, the authors aimed to prevent sensor saturation. They performed differential sensing symmetrically around the monopolar stimulating electrode to maximize the common-mode nature of the stimulus artifact. They also used external passive filter-

CHAPTER 2. BIDIRECTIONAL NEURAL INTERFACES

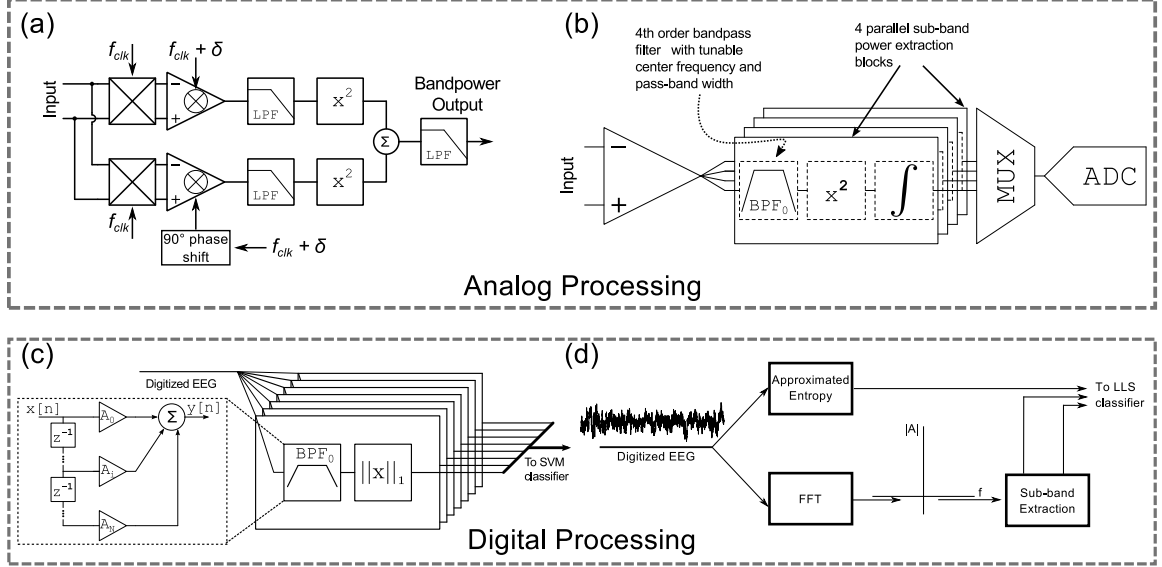


Figure 2.4: Four architectures for on-chip signal processing of neural data. (a) In,¹⁰⁵ by altering the frequency and phase of the chopping clock at various points within the front-end architecture, the authors produce an output signal that represents the power within a programmably set frequency band. (b) Sub-band power can be extracted after amplification and filtering using tunable analog bandpass filters.¹⁰⁶ (c) Alternatively, a bank of digital filters can be used to extract band power after digitization of neural signals, the vector of sub-band power can then be used as the input to a classifier.^{107,108} (d) An alternative method for extracting sub-band power is to perform an FFT on digitized signals. This, along with other features, such as signal entropy, can be inputs into a classifier for seizure detection.¹⁰⁹

ing to attenuate common-mode signals, which prevented the stimulus artifact from exceeding the common-mode input range of the amplifier. Secondly, Stanslaski and colleagues mitigated spectral contamination of the sensed signal by judicious choice of stimulation parameters. The authors analyzed how the harmonics of the chopping waveform (chopper stabilization was used to remove $1/f$ noise in the front-end amplifier) interact with the harmonics of the stimulation waveform. This analysis provided guidelines for how to choose stimulation parameters to minimize contamination of

CHAPTER 2. BIDIRECTIONAL NEURAL INTERFACES

the frequency band of interest. Finally, biomarker classification was performed with a support vector machine that used the state of stimulation (on or off) as a feature.

On-chip spectral analysis techniques have received considerable attention; analyzing the energy within specific signal bands of interest can be accomplished with either analog or digital circuits (Fig. 2.4). One analog-domain method merged the spectral extraction capabilities into the front end amplifier.¹⁰⁵ Fig. 2.4(a) illustrates a simplified block diagram of how this was done. Avestruz *et al.* used chopping to remove low-frequency noise from the front-end amplifier. By manipulating the frequency and phase of the chopping clocks at various points within the circuit, the authors produced an analog output that represented the power in a band of interest. The center and width of this band could be tuned in a robust manner. Alternatively, Zhang *et al.* used four parallel switched-capacitor filters to extract the signal component in four different frequency bands of interest (Fig. 2.4(b)). The filter architecture allowed for band centers and widths to be digitally tuned. The authors then used a squaring circuit and switched-capacitor integrator to produce an output representing the energy in the respective signal band.¹⁰⁶ Finally, digital bandpass filters (BPFs) have been used by a number of groups to approximate the energy in different sub-bands.^{107,108,113} Yoo *et al.* designed an eight channel seizure detection IC.¹⁰⁷ Each channel contained seven digital BPFs to aid in the classification of seizure activity.

A complete bidirectional SoC for closed-loop epilepsy treatment was described and validated by Abdelhalim *et al.*¹¹⁴ The chip contained 64 low-noise amplifiers

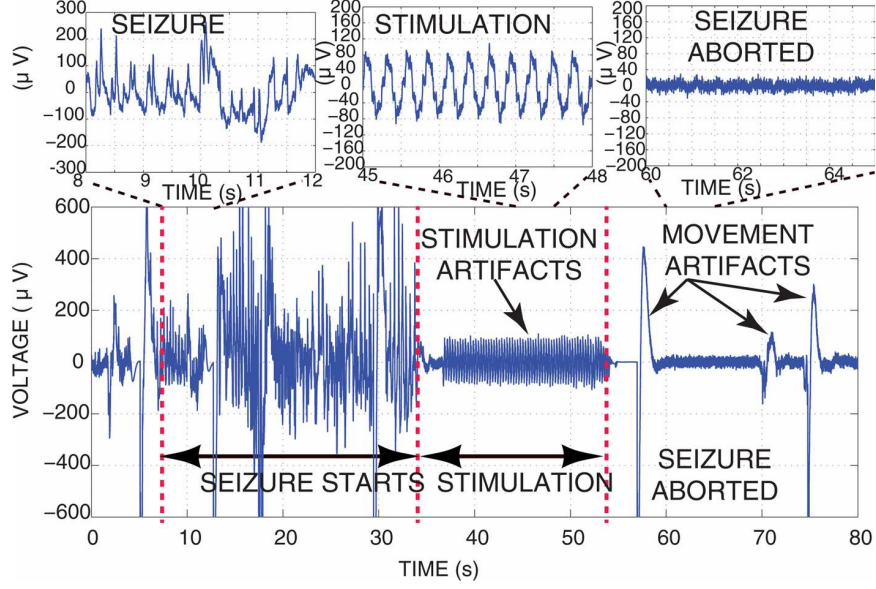


Figure 2.5: Closed-loop seizure control. Seizure activity induced by injection of kainic acid begins around $t = 8$ s (left inset). This abnormal activity can be efficiently detected by analyzing the phase relationships between pairs of channels. After detection, a 5 Hz, $100 \mu A$ pulse train is triggered (center inset). Soon after, LFP activity returns to low-amplitude desynchronized activity (right inset). Adapted with permission from.¹¹⁴

and stimulators. An innovative resource-sharing scheme allowed for the massive integration of 64-channels. Each channel could be configured as a recording channel or a stimulator. Depending on this setting, an in-channel DAC would be used either within a SAR ADC, or to set the stimulation current. Likewise, the SAR logic was re-purposed to set the pulse-width of the stimulator. Further, the authors used two sets of FIR filters to separate the in-phase and quadrature components of the input signals. Resource-sharing eliminated the need for hardware multipliers within the FIR filters, as the multiplications operations were merged directly into the ADC's SAR logic.¹¹⁵ The in-phase and quadrature components of channel pairs were passed

CHAPTER 2. BIDIRECTIONAL NEURAL INTERFACES

to on-chip CORDIC cores to extract a feature useful for seizure detection, the phase locking value (PLV). Abdelhalim and colleagues designed a feedback loop that triggered bisphasic stimulation pulses when the PLV for a given channel pair exceeded a programmable threshold. This is illustrated in Fig 2.5; the authors induced seizure activity in a rat by injection of kainic acid.

The large number of channels present in a single chip has important practical implications. For example, during the clinical trials for the RNS[®] System, issues with lead placement and damage occurred in a few patients.⁹ Increased channel count would allow physicians to cast a wide net in capturing the seizure focus and potentially increase the proportion of patients responsive to the treatment.

2.2.3 Comparison of VLSI Systems

Table 2.1 compares several academic and commercial bidirectional neural interfaces. Applications such as spike-triggered stimulation (STS), memory prostheses, treatment of epilepsy, or closed-loop DBS are represented. In cases where the signal processing is performed by an external programmable device, the application is listed as “general,” as the application is not fixed.

Direct comparisons of total system power consumption across designs are difficult for bidirectional systems. System power dissipation will depend on the stimulation rate and amplitude, factors that may vary greatly from patient to patient. In fact, this variation across patients translates to a nearly 2-year difference in the system lifetime

Table 2.1: Comparison of state-of-the-art bidirectional neural interface systems.

Reference	48		116		57		47,117,118		110,119,120		114		121		122		109		123	
Year	2005		2011		2011		2012		2012		2013		2014 ^a		2014		2014		2015	
Technology	Discrete		Discrete		0.35 μ m		0.18 μ m		0.8 μ m, discrete		0.13 μ m		-		0.18 μ m		0.18 μ m		65nm	
Application	STS ^{β}		STS		STS		Memory		General		Epilepsy		Epilepsy		CL-DBS ^{γ}		Epilepsy		STS	
# Stim Chan	1		3		8		8		8		64		8		2,8		1		8	
Stim Res (bits)	5		-		6		-		8		8		-		6		1		6	
Stim Range (mA)	0.1		0.2/5		0.945		-		25.5		1.09		11.5		4.1/0.116		0.03		0.9	
Stim Supply Voltage (V)	14		$\pm 15/\pm 50$		5		± 3.3		± 10		3.3		12		5		10		8.7	
# Rec Chan	1		3		8		16		4		64		4		4		8		64	
Front-end BW (Hz)	500-5k		10-7.5k		1.1-12k		200-2k		0.05 – 120 ^{δ}		1-5k		-		0.64-6k		0.5-7k		10-8k	
Front-end Noise (μV_{rms})	6		2.7		3.12		4.24		1.1 ^{δ}		5.1		-		6.3		5.23		7.5	
ADC Type	Delta-sigma		-		SAR		SAR + Dual Slope		-		SAR		-		Pipeline (log)		Delta-modulated SAR		SAR	
ADC Res. (bits)	8		8		10		12		-		8		-		8		10		10	
Processing	Spike discrimination		Spike discrimination and sub-band power extraction		Digital Spike discrimination		HPF, Digital spike sorting, non-linear MIMO neural network		BPF, analog sub-band power extraction and SVM		Sub-band PLV		Line-length, area detector, or band-pass detector		Digital LPF/HPF, sub-band power extraction, and PI controller		FFT, Sub-band power extraction ApEn, LLS classifier		Spike discrimination	
Telemetry	Infrared		Infrared		FSK		-		Inductive		UWB		Inductive		Backscatter transceiver		MedBand OOK transceiver		-	
Power Supply	Battery		Battery		Battery		-		Battery		Battery		Battery		RF power harvesting or battery		Inductive coupling or battery		-	
Power Consumption (mW)	40-120 ^{ϵ}		284-420 ^{ϵ}		0.375 ^{ϵ}		-		0.04 ^{ζ}		1.4 ^{ζ}		0.062 ^{ϵ}		0.468 ^{ϵ}		2.8 ^{ζ}		0.193 ^{ζ}	

^a Data here taken from user manual published online in 2014. ^{β} STS = Spike-triggered stimulation. ^{γ} CL-DBS = Closed-loop deep-brain stimulation. ^{δ} The noise and bandwidth figures are from.¹¹⁹ When the IC is used in spectral extraction mode, a noise-penalty is incurred, but the bandwidth is also narrowed, allowing for a minimum detectable signal of $1\mu V_{rms}$.^{105,110} ^{ϵ} Power figure includes power consumed by active stimulators. ^{ζ} Power figure does not include power consumed by active stimulators.

for patients in the 5th percentile versus the 95th percentile for the RNS[®] System.¹²¹ Hence, where possible, the power consumption listed in Table 2.1 does not include power dissipated from the stimulator. In cases where the power figure does include the stimulation block, details on amplitude and frequency can be obtained from the references.

2.3 Conclusion

Bidirectional neural interfaces are enabling treatment and therapy with diverse and important applications. Significant advancements are needed in our understanding of neural processing and coding so that more effective therapeutic closed-loop strategies can be developed. Newman *et al.* have created an open-source, closed-loop experimentation platform,^{124,125} making the means to investigate such strategies widely available. For such systems to be widely adopted at the clinical level, performance of neural interfaces needs improvement in areas such as size, power consumption, implant life-time, and cost. Therefore, for these systems to become a clinical reality, we need a more complete understanding of the underlying neural mechanisms as well as smaller, more power efficient and smarter sensors. Above all, the future of these systems depends on interdisciplinary collaborations. We believe that the challenges described above can only be solved via synergistic cooperation among scientists, clinicians and engineers. In this way, it will be possible to progress rapidly

CHAPTER 2. BIDIRECTIONAL NEURAL INTERFACES

from scientific discoveries to novel and appropriate technologies and finally to clinical validation and deployment.

This review is limited in certain ways. Non-invasive neural stimulation methods such as transcranial magnetic stimulation (TMS),¹²⁶ transcranial direct current stimulation (tDCS)¹²⁷ and transcranial focused ultrasound (tFUS)¹²⁸ have been ignored. These methods are beginning to be seen as effective tools for studying neural function in humans, and there are ongoing efforts to translate them to clinical use.^{129–131} A drawback shared among all non-invasive stimulation methods is their attainable spatial resolution. With TMS for example, the focality of stimulation is limited to regions on the order of 1 cm^2 .¹³² Localization of the stimulation electrode is of paramount importance; hence the spatial resolution of non-invasive methods could preclude their use in all cases. Further, noninvasive methods can only be applied sporadically for acute studies or treatments. Unlike implanted systems, these technologies are not available 24/7 over extended durations. Nevertheless, due to safety concerns associated with implanted systems, noninvasive neural modulation methods will likely always have a major clinical role.

Also, all optical methods, optical sensing and optogenetic stimulation have not been included. Clinically relevant information can be gleaned from optical methods,¹³³ however, a complete treatment of these methods is beyond the scope of this article, for an in-depth review see.¹³⁴ Optogenetic stimulation has astounding potential given its ability to selectively target cell types, and has been used in animal

CHAPTER 2. BIDIRECTIONAL NEURAL INTERFACES

models in bidirectional treatment of seizures.¹³⁵ The major impediments to human use are also beyond the scope of this article, however, significant progress is being made, especially with regards to optogenetic-based retinal prostheses.¹³⁶

In this chapter, a diverse set of fields in which bidirectional neural interfaces are advancing the current state of the art have been discussed. Neuroprosthetic devices may soon endow the user with chronic biomimetic sensory feedback, allowing artificial devices to feel like natural extensions of the body. Neuro-repair devices are envisioned to accelerate and enhance recovery in patients following stroke or TBI, restoring pre-injury levels of function. Finally, neurotherapeutic devices are poised to treat the symptoms of neurological diseases in a patient-specific manner to more efficiently ease symptoms. Advances in the engineering of VLSI systems, including the development of fully integrated systems, are helping to drive the field from the laboratory to the clinic.

Chapter 3

A Wireless EEG System for Freely Moving Rodents

The operation of bidirectional and closed-loop neurotherapeutic systems is predicated on the ability to detect relevant biomarkers to influence stimulation. The success of these systems hinges on the discovery of signals that provide information about disease. Preclinical models of diseases in rodents can be used to discover electrophysiological correlates of recovery from global ischemic brain injury for example.¹³⁷ However, current recording systems for laboratory animals are only capable of sporadic recordings, making it difficult to correlate activity in the electrocorticogram (ECoG) with subjects' behaviors and outcomes, especially when biomarkers of interest are sporadic. These challenges demand significant technological progress to enable wireless recording of neural activity from untethered and behaving subjects.

CHAPTER 3. WIRELESS EEG

Over the past several years, a number of systems have been designed to record neural activity in awake behaving animals.^{48,103,138–143} Santhanam *et al.*¹³⁹ designed a system which stores the spike-sorted neural data onto a flash memory card, bypassing the need for a wireless transmitter. A later version of the same system,¹⁴¹ employed a custom neural recording VLSI chip with on-board FSK telemetry.¹⁴² This system was mounted on a rhesus monkey and used to record spike signals from one channel continuously for six days. A similar version of this system was also employed to record spikes and electromyography (EMG) in freely moving insects.¹⁴³ Hampson *et al.*¹⁴⁰ reported on a custom-built system with Bluetooth technology which could transmit 16 channels of neural data from awake and freely moving rats. This system achieved a transmission rate of approximately 150 Kbps and could record for over five hours while being powered by a 40 gram battery pack. Chae *et al.*,¹⁰³ reported on a 128 channel neural recording IC with an on-board ultra-wideband (UWB) transmitter capable of transmitting data at up to 90 Mb/s. This system was validated on excised snail neural tissue and offered on-board spike-sorting, emphasizing the ability to perform digital signal processing alongside analog acquisition and RF telemetry. Szuts *et al.*¹⁴⁴ reported on a 64 channel system designed to record and transmit neural spikes and local field potentials. The system had a telemetry range of 60 m and consumed 645 mW. It was used to record neural activity from a rat in a $10 \times 10 \text{ m}^2$ outdoor environment.

The previous reports mainly focus on recording single-unit activity as opposed

CHAPTER 3. WIRELESS EEG

to ECoG or electroencephalogram (EEG) signals, which offer a more global view of ongoing brain activity. Recording instrumentation for these signals have different bandwidth and noise requirements than the instrumentation required for recording spike signals. Little work has focused on designing head-mounted systems for recording ECoG signals in small animals. Lapray *et al.*¹⁴⁵ described a system for wireless recording of one channel of ECoG activity in awake rats at distances up to 3 m.

Here, we present a recording system for wireless monitoring of neural and behavioral activity from awake behaving animals. The system allows long-term multichannel recording of neural signals and quantitative activity measures from tetherless subjects with high fidelity in a small footprint. We have implemented the system to record ECoG activity in freely moving rats.

Section 3.1 describes the functional and physical design of the system. Results of benchtop characterization and *in-vivo* testing in awake subjects follow in Section 3.3, and Section 3.4 concludes the chapter.

3.1 System Design

The wireless recording system described in this chapter takes on two versions referred in the following text as System A and System B. The core elements of both systems include a multichannel VLSI neural recording interface, a wireless transmitter, a microcontroller, and a battery. System A makes use of a UWB transmitter

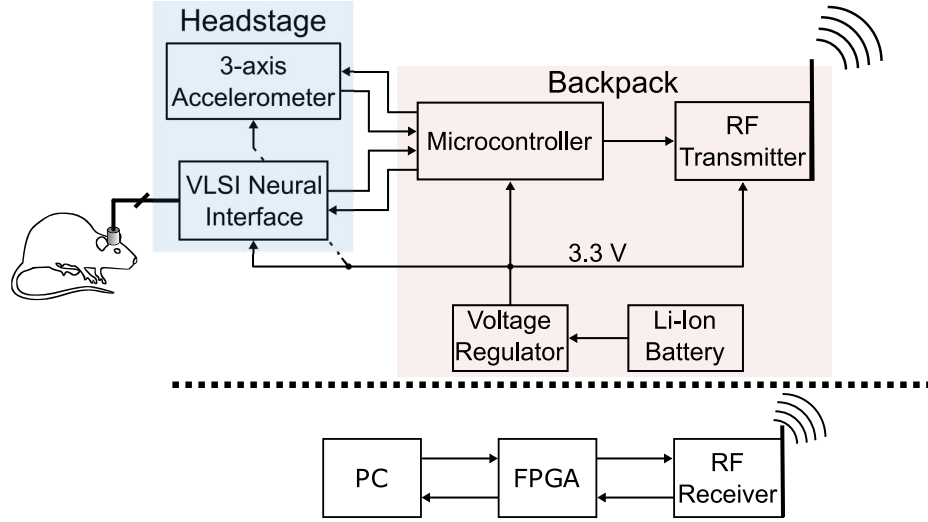


Figure 3.1: Functional block diagram of the developed neural monitoring system. Neural signals are amplified, filtered and digitized by a custom-designed VLSI chip that was designed by Mollazadeh *et al.*^{146,147} A microcontroller packages the data and sends it to a wireless transmitter. Signals are detected by a receiver circuit and read into the computer using an FPGA-USB interface.

designed by Tang and Culurciello,¹⁴⁸ whereas System B transmits data with a commercial off-the-shelf frequency-shift-keying (FSK) transmitter (nRF24L01+, Nordic Semiconductor, Trondheim, Norway). System B additionally includes a MEMs accelerometer (ADXL345, Analog Devices, Norwood, MA) to quantify physical activity. Fig. 3.1 illustrates a block diagram of the architecture valid for both System A and B. Neural activity is amplified, filtered, and digitized by the VLSI neural interface. Digitized data are transmitted in bit-serial format to a microcontroller which reformats and packages the data, and sends it to the wireless transmitter. Power is supplied with a rechargeable Li-ion battery.

The neural interface board mates with an electrode connector affixed to the skull, and is housed in a 3D-printed plastic enclosure. In System B, the accelerometer

CHAPTER 3. WIRELESS EEG

is stacked on top of the neural interface board within the plastic enclosure. These components are referred to as the headstage. The digital interface, transmitter, and battery were held in a pouch secured to the body, and is referred to as the backpack stage. At the receiving end, an RF receiver is interfaced to a field-programmable gate array (FPGA) on a development board with a USB interface (XEM 3010, Opal Kelly, Portland OR). Received data is displayed in real-time using a custom graphical user interface (GUI) written in LabView.

3.1.1 Neural Front-End

Each channel of the neural front-end contains a bandpass amplifier with tunable bandwidth, a programmable analog-to-digital converter (ADC), and bit-serial readout circuitry. The bandpass amplifier in the recording front-end provides fixed gain (40 dB) amplification with tunable lowpass filtering from 140 Hz to 8.2 kHz. The amplifier has less than $3 \mu\text{V}_{rms}$ input-referred noise and each channel draws less than $12.5 \mu\text{A}$ of current from the power supply (dependent on the bandwidth settings). Each channel also contains a configurable incremental G_m -C $\Delta\Sigma$ ADC, which offers programmable resolution from 8 to 12 bits and digital gain of 1 to 4. With the ADC clocked at 1 MHz, the oversampling ratio (OSR) set to 2^{10} , and digital gain set to 1, an inherent low-pass (anti-aliasing) filter is implemented by the G_m -C integration. Finally at the end of OSR clock cycles, the digital outputs of each channel are clocked into and out of a parallel-in serial-out shift register with the output of all channels connected

to each other in a daisy chain fashion. These circuits were fabricated in a $0.5\ \mu\text{m}$ 2P3M CMOS process and occupied $3\ \text{mm} \times 3\ \text{mm}$ of silicon area. A comprehensive description of this system can be found elsewhere.^{146,147}

3.1.2 Wireless Telemetry

In System A, the transmitter consists of a voltage-controlled ring oscillator (VCRO) as a compact pulse generator and an output buffer as the modulator. The transmitter is capable of generating pulses with 1 ns width and the pulse rate can be controlled between 90 MHz and 270 MHz. The UWB chip can reach a maximum of 14Mbps and consumes 10-20 mW of power from 3.3 V supply depending on the transmission distance. The UWB circuit was fabricated in a $0.5\ \mu\text{m}$ silicon-on-sapphire (SOS) process and occupies $420\ \mu\text{m} \times 420\ \mu\text{m}$ of silicon area.

In System B, an nRF24L01+ (Nordic Semiconductor, Trondheim, Norway) transceiver is used for telemetry. There are two tradeoffs made in using the commercial device. First, the commercial transmitter is less power efficient; it consumes $>36\ \text{mW}$ from a 3.3 V supply during transmission when operating with a data rate of 1 Mbps. However, it provides a more robust data link when the rodent is active and moving about its cage. Second, the commercial chip operates with a carrier frequency of 2.4 GHz, permitting the use of a very small ($2.2 \times 6.5\ \text{mm}^2$) chip antenna and decreasing the system size and weight.

3.1.3 Digital Interface

The two VLSI circuits described above as well as the commercial transmitter offer a range of programmable parameters for various operating conditions. However, the bit-serial output of the neural interface cannot be directly connected to either telemetry chip. In System A, the telemetered data needs to be formatted in packets in order to remove spurious RF interferences from data at the receiver side. In System B, communication with the transmitter chip must be established with SPI communication protocol. Hence, a digital interface module is needed to coordinate the operations between all the modules. This interface is implemented using a power efficient microcontroller, PIC18F24J11 (Microchip, Chandler, AZ).

On system start-up, the microcontroller programs the neural interface chip to the desired bandwidth and ADC settings (e.g. 0.1 Hz to 1 kHz bandwidth, 10 bit resolution, and digital gain of two for recording ECoG signals). The microcontroller then sends a “start” command to the neural interface chip to commence data acquisition, and awaits reception of the digitized data.

In System A, the microcontroller appends a 16 bit header to the beginning of the block and serially outputs the data to the UWB chip. The packaged data is shifted out serially to the UWB chip at a rate of 1 Mbps. A block of data is one conversion cycle from all channels (i.e. 16 channels digitized at 12 bits totaling 192 bits). In System B, a data packet of both neural data and accelerometer data are sent to the transmitter chip which independently appends a header to the beginning of the data

CHAPTER 3. WIRELESS EEG

packet and a CRC error checking word to the end.

Because the system is powered by a battery and available power is limited, particular care was taken in programming the microcontroller. When not reading in samples from the neural interface or accelerometer, the microcontroller operates in a low-power idle mode, in which peripherals continue to operate while the CPU stops executing instructions. We use the two serial communication channels of the enhanced universal synchronous asynchronous receiver transmitter (EUSART) peripheral to receive data from the neuropotential chip and transmit data to the telemetry chip. The microcontroller consequently operates almost exclusively in a lower power idle state. Finally, to further minimize the power consumption of the discrete components, we attempted to minimize the instruction clock frequency. The $\Delta\Sigma$ ADC in the VLSI neural front-end requires a 1MHz input clock, and this determined the minimum frequency at which we could run the microcontroller. We use a 4 MHz crystal, which provides a 1 MHz instruction clock cycle. This in turn limited the data transmission rate of the UWB module to 1 Mbps. Although this rate is lower than the maximum rate the UWB transmitter can provide, it suffices the needs of our recording system.

3.1.4 System Integration and Packaging

The headstage consists of a $2.2 \times 1.2 \text{ cm}^2$ printed circuit board (PCB). The neural interface chip was directly wirebonded to the head-stage PCB and connects to the electrodes with a custom made connector that mates directly with the electrode

CHAPTER 3. WIRELESS EEG

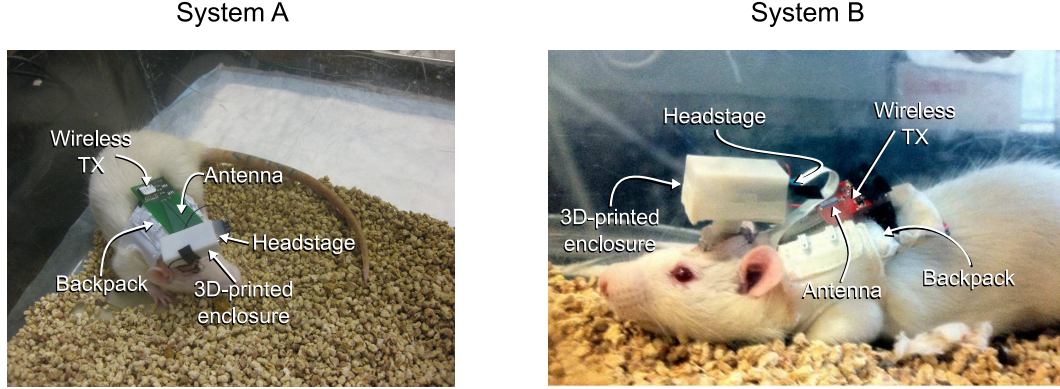


Figure 3.2: The two versions of the wireless ECoG recording systems described in this chapter. Both systems consisted of a headstage element in a 3D-printed enclosure as well as a backpack. Both backpacks contained a battery, microcontroller, and wireless transmitter. System B additionally contained an accelerometer mounted within the headstage (not shown).

pedestal and screw-electrodes (PlasticsOne, Roanoke, VA), which are affixed via dental cement to the rodent's head. The headstage PCB and accelerometer sit inside a custom-made plastic enclosure which was rapid prototyped in a fused deposition modeler.

In both systems, the backpack consists of a $3 \times 3 \text{ cm}^2$ PCB housing the battery and the microcontroller. System A contains an additional $4.6 \times 2.3 \text{ cm}^2$ PCB housing the UWB transmitter and antenna which is etched into the PCB, while System B contains a $2.0 \times 2.3 \text{ cm}^2$ PCB housing the FSK transmitter chip. The battery and digital interface board sit inside a pouch that connects via hook-and-loop to a rat jacket (Lomir, Malone, NY). The head-stage and backpack are connected with a custom-made cable consisting of eleven 36 gauge wires in System A and an FFC cable in System B. Images of both systems can be found in Fig. 3.2.

3.1.5 Receiver Circuitry

The UWB receiver used in System A consists of an RF energy detector (ADL5519), a comparator (LMV7239), a digital-to-analog converter (DAC) (AD7398), and the FPGA integration module. The RF detector reconstructs the energy envelope from the UWB impulse sequences, and the output is digitized through comparison with the tunable reference voltage set by the DAC. The digitized data stream is synchronized to the FPGA's system clock, and the incoming bitstream is compared with the expected 16 bit header appended to each packet of data. Once the header is detected, the FPGA reads the sixteen channels worth of data plus a checksum. The data is then transferred to a computer through the USB interface and displayed in real-time with custom software written in LabVIEW (National Instruments, Austin, TX). For System B the receiver circuits were replaced with the same transceiver used in the backpack stage as a transmitter; the other components remained the same.

3.2 Data Analysis

The inclusion of an accelerometer in System B allowed quantification of relationships between recorded ECoG and behavioral state in untethered animals. The 3-axis accelerometer signals (a_x, a_y, a_z) were reduced to a single vector magnitude $|r|$

$$|r| = \sqrt{a_x^2 + a_y^2 + a_z^2} \quad (3.1)$$

Behavioral state was quantified by computing the variance of $|r|$ in 10 second

CHAPTER 3. WIRELESS EEG

sliding windows overlapping by 5 seconds. This provided a measure of power in the accelerometer signal after subtracting out the mean of 9.8 m/s^2 due to gravity.

ECoG channels were processed offline in MATLAB (MathWorks, Natick, MA). A common-average reference (CAR) filter was first applied to remove common-mode artifacts. Decomposition into the beta and high-gamma sub-bands was accomplished by applying a set of FIR filters with passbands of 12 - 30 Hz (beta) and 50 - 90 Hz (high-gamma). Filters were designed to have a 100 dB stopband attenuation, a 0.1 dB passband ripple. Signals were filtered in the forward and reverse direction for zero phase distortion. Power from the sub-band signals was extracted using the same procedure used for the accelerometer data.

3.3 Results

The head-mounted component of System A includes the neural interface circuitry and a plastic enclosure, and weighs 5 g. The backpack component, which includes a digital interface, the ultra-wideband transmitter, and a 6 g battery, weighs 19 g. In System B, the headstage weighs 6 g (due to the inclusion of the accelerometer) and the backpack weighs 23 g (due to a higher capacity battery).

3.3.1 Benchtop Characterization

The benchtop characteristics of each VLSI chip have been previously reported in.^{146–148} Here, signal-to-noise-and-distortion (SNDR) measurements were made to quantify any degradation in the recording front-end.

The power spectrum of the wirelessly received digital output of one channel was measured, while a $500 \mu V_{pp}$ 25 Hz sine wave was presented to the front-end amplifier input, with the ADC gain and resolution set to 1 and 10 bits respectively. The total harmonic distortion (THD) of the recorded output increased from 0.05% in the wired condition to 0.1% in the wireless condition. SNDR decreased from 56 dB in the wired case to 54 dB in the wireless case.

System A consumes, on average, 4.8 mA, while System B consumes 5.1 mA. The substantial reduction in power consumption, compared to a previous version of the system,¹⁴⁹ was achieved by reducing the frequency of the microcontroller’s instruction clock by a factor of 10. This current consumption figure can be broken down as follows: 1) the head-mounted analog front-end board consumes 2.1 mA, 2) the digital interface board consumes 1.68 mA while the microcontroller is running and 1.18 while the microcontroller is in idle mode, and 3) the wireless module consumes 1 mA in System A and 1.3 mA in System B. The power consumption of the accelerometer was negligible compared with the rest of the components.

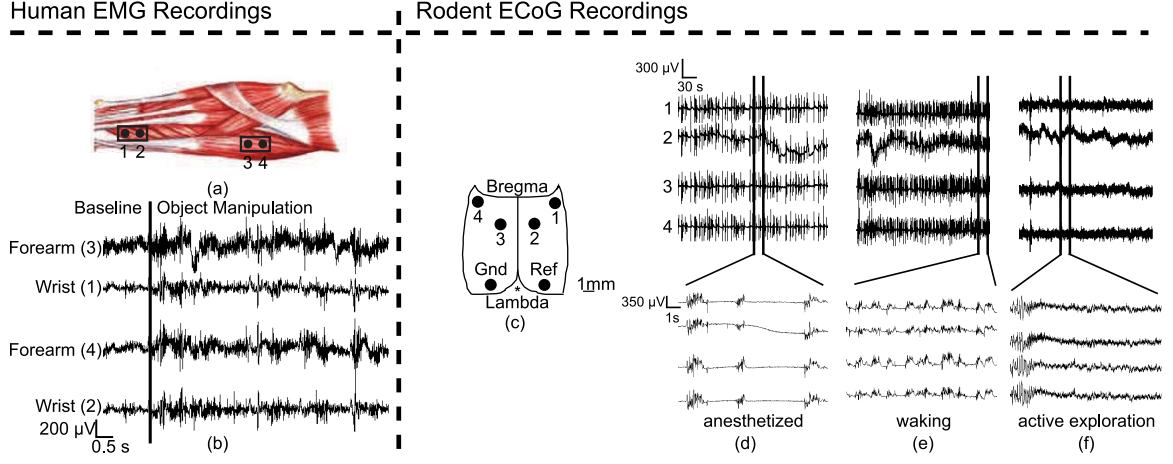


Figure 3.3: (a) Electrodes were placed on the forearm and wrist of a human subject in the numbered locations. (b) EMG activity was recorded during a single trial of manipulating a pair of scissors. (c) Illustration of the electrode locations relative to anatomical landmarks of the skull. Four channels of wireless ECoG activity were recorded from somatosensory cortex in a rat. Three behavioral states were observed: (d) anesthetized (e) waking and (f) active exploration.

3.3.2 In-vivo Experiments

3.3.2.1 System A

First, we evaluated the system by recording EMG activity from a human subject. Before electrode placement, the arm was cleaned with a Nuprep abrasive skin preparation gel from D.O. Weaver & Co. (Aurora, CO). Four EMG bipolar Ag–AgCl electrodes from Myotronics-Noromed (Tukwila, WA) were placed on the subject’s forearm. Two were placed more proximally, closer to the elbow, while the other two were placed more distally, closer to the wrist (Fig. 3.3(a)). Two Cleartrace LT electrodes from ConMed Corporation (Utica, NY) were used as reference and ground electrodes. The reference electrode was placed on the proximal part of the olecranon

CHAPTER 3. WIRELESS EEG

and the ground electrode was placed on the clavicle. In this experiment, the amplifier bandwidth was set to 8 kHz. The ADC gain and resolution was programmed to be 1 and 10 bits respectively; this provided a sampling rate of 1 kHz. Fig. 3.3(b) shows an example of the recorded and telemetered EMG signal while the subject manipulated a pair of scissors. The recorded signals show that EMG activity can be recorded with high quality in single trials of natural movement.

Thereafter, we used the system to record ECoG activity in three rats via transcranial screw electrodes implanted into the skull. The surgical procedures used for implantation were approved by the Johns Hopkins Animal Care and Use Committee. The subjects (250 g female Lewis rats) were anesthetized with a ketamine mixture via intra-peritoneal administration. Six burr holes were drilled into the exposed part of the cranium, using a standard dental drill (Fine Science Tools, North Vancouver, BC, Canada). Four of these holes corresponded to the somatosensory area for hind limbs and forelimbs on each hemisphere, shown in Fig. 3.3(c). Forelimb sites were located 0.2 mm posterior to bregma and 3.8 mm laterally from the bregma, and hind limb sites were located 2.3 mm posterior to bregma and 2.5 mm laterally from the bregma. The fifth and sixth holes were drilled 3 mm to the right and left of lambda, to serve as an intracranial reference and ground, respectively. The transcranial screw electrodes (E363/20, PlasticsOne, VA) were then screwed into the holes such that the ends made contact with the dura. The distal end of each electrode was inserted into a slot of an electrode pedestal (MS363, PlasticsOne, VA) which connected to the

CHAPTER 3. WIRELESS EEG

neural interface board.

For the following experiments, the bandwidth of the amplifiers was set to 8 kHz. The gain and resolution settings of the ADC were set to 2 and 10 bits respectively; corresponding to a sampling rate of 500 Hz. Animals were recorded continuously during three distinct conditions: anesthetized, waking and active exploration. First, the subjects were anesthetized under isoflurane. Burst suppression, a well-known phenomenon occurring in anesthetized subjects which includes periods of silence interspersed with pronounced activity¹⁵⁰ is clearly present on the recorded signal, shown in Fig. 3.3(e). Anesthesia was subsequently withdrawn, and the subject was allowed to wake up. In the waking state (Fig. 3.3(f)), five minutes after anesthesia was withdrawn, suppression patterns evolve into slow oscillations in the 1-2 Hz range. Once fully awake, the subject roamed about its cage. In this last state, active exploration was characterized by desynchronized low amplitude ECoG signals (Fig. 3.3(g)).

3.3.2.2 System B

Fig. 3.4 illustrates a 30 minute block of simultaneous 4-channel ECoG and accelerometer power, computed as described in Section 3.2. The insets show ECoG during inactive and active periods with a finer time resolution.

Fig. 3.5(top) depicts ECoG power in the beta and high-gamma bands along with the accelerometer power over the entire 14 hour recording. Power for all signals was normalized to the mean value, and smoothed and downsampled over 1 minute

CHAPTER 3. WIRELESS EEG

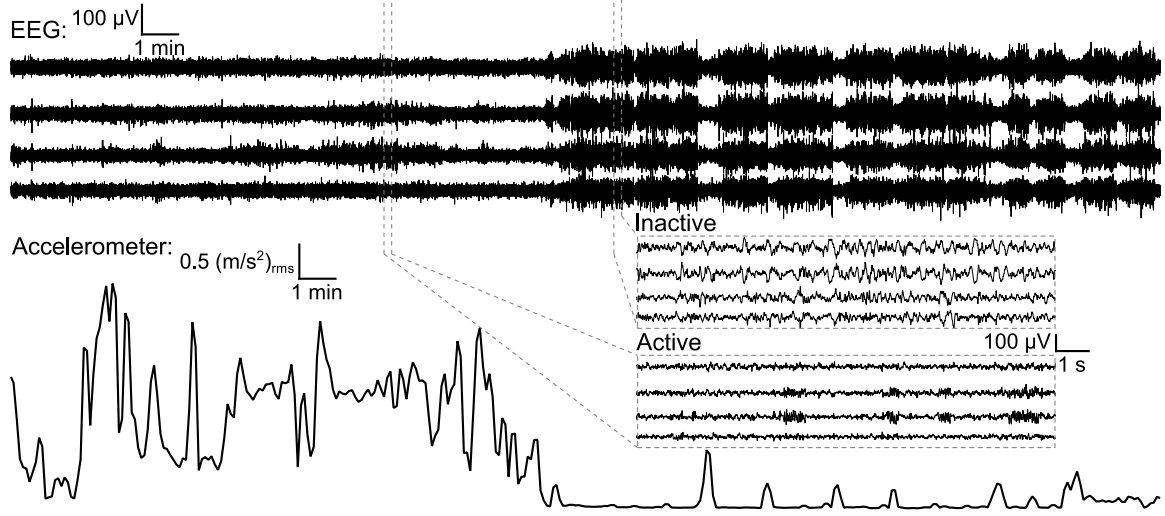


Figure 3.4: A 30 minute segment of simultaneous ECoG and accelerometer data illustrating both data sets during active and inactive periods. Accelerometer data plotted here as an RMS value calculated as described in Section 3.2. Insets illustrate ECoG patterns during active and inactive periods on a finer time scale.

intervals. Fig. 3.5(bottom) shows a scatter plot of the log-transformed data from two rats.

Lastly, System B was used to monitor ECoG and activity in a rodent model of cardiac arrest.¹⁵¹ Fig. 3.6 shows concurrent ECoG and accelerometer data more than 14 hours post-resuscitation. High-amplitude synchronous spiking waveforms can be observed on all channels along with high-amplitude oscillatory accelerometer readings. This animal was found to be suffering convulsive seizures approximately four hours later, and the recordings were stopped.

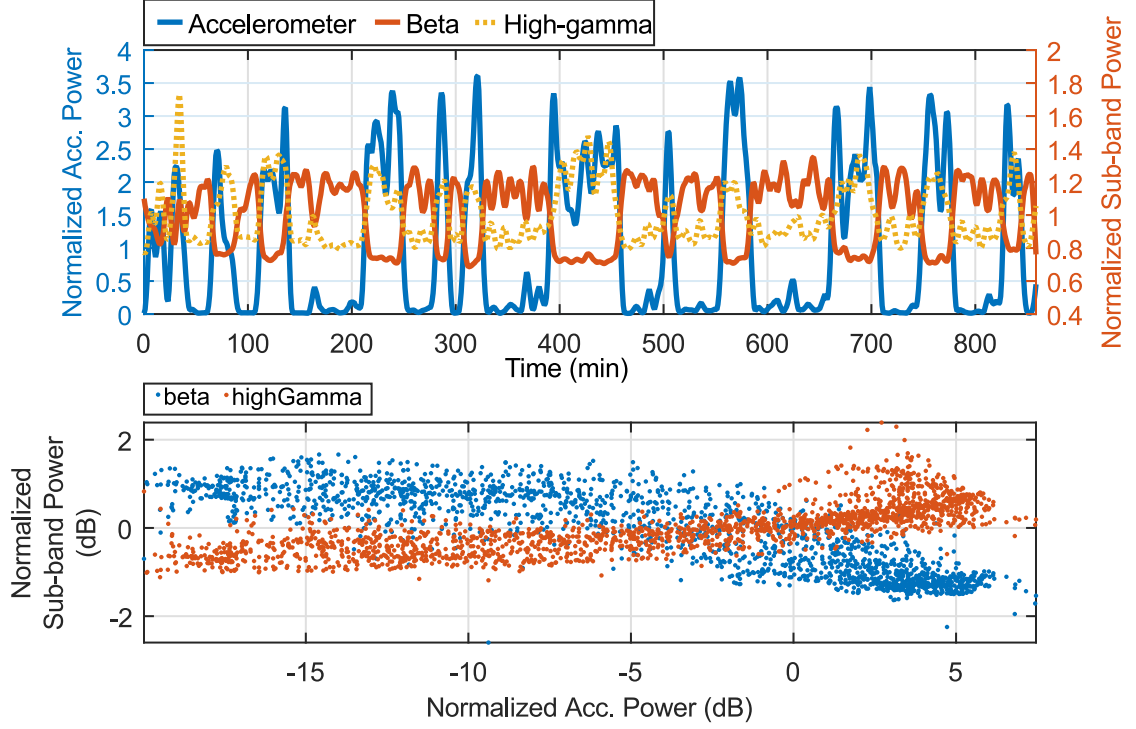


Figure 3.5: Modulation of ECoG sub-band power during periods of high activity and inactivity. (top) Power in the accelerometer signal along with power in the beta (12 - 30 Hz) and high gamma (50 - 90 Hz) bands. Power in all signals was normalized to the average value over the recording. (bottom) Scatter plots of accelerometer power versus ECoG sub-band power.

3.4 Conclusion and Future Work

This chapter presented a miniature, light-weight, and low-power stand-alone VLSI recording system with wireless telemetry for monitoring neural activity in awake behaving subjects. The VLSI neural interface module offers programmable bandwidth setting for isolated recording of various neural modalities. Each channel of the neural interface also offers a programmable ADC which in turn can be optimized for various neural signals. The wireless modules offer low power, high rate data transfer, suitable

CHAPTER 3. WIRELESS EEG

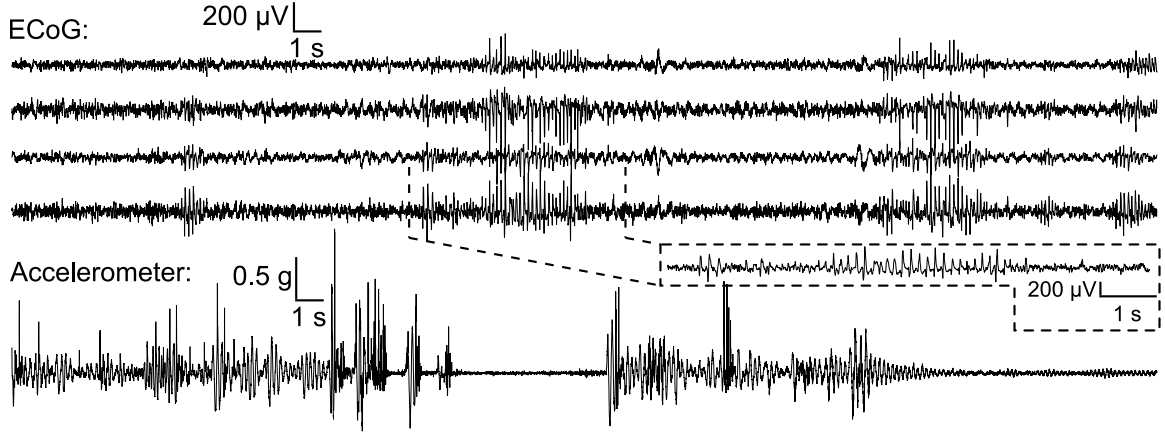


Figure 3.6: Seizure activity in a rodent model of cardiac arrest captured with the wireless system. The top four traces show ECoG bandpass filtered between 2-90 Hz. The concurrent accelerometer magnitude vector $|r|$ is at bottom. The high amplitude oscillations on ECoG, interspersed with the oscillations in movement provide evidence of an ongoing seizure.

for neural recording in small animals. System A weighed 24 grams and consumed 4.8 mA of current from a 3.7 V battery. System B weighed 29 grams and consumed 5.1 mA from a 3.7 V battery.

We successfully performed benchtop as well as *in-vivo* operations of the system from awake rats. The inclusion of an accelerometer in System B allowed simultaneous capture of behavioral and neural activity. To our knowledge, this is the first time a VLSI interface and telemetry has been used to record ECoG activity with concurrent activity measures from awake behaving rats. Compared to two previous designs for recording from rats,^{144, 152} our design consumes less power. We have traded off telemetry range and channel count for gains in battery lifetime, arguably the most important parameter for performing uninterrupted chronic studies.

The presented system addresses the emerging need for studying neural activity

CHAPTER 3. WIRELESS EEG

in untethered awake behaving subjects. Our system allows for the uninterrupted recording of ECoG activity following cardiac arrest in rats. In doing so, we were able to capture seizure activity, a biomarker of brain injury after cardiac arrest,¹⁵³ in an untethered rat. Therefore, these systems can enable exploratory studies of electrophysiological biomarkers in rodent models of brain injury and disease.

Chapter 4

A CMOS Current Steering Neurostimulation Array with Integrated DAC Calibration and Charge Balancing

Electrical stimulation is a widely used tool in basic and clinical neuroscience and neuroengineering. Common stimulation targets lie within the central and peripheral nervous system. Stimulation of the central nervous system (CNS) has been used to probe the functional role of populations of neurons^{20,154} and provide sensory feedback to users of a neuroprosthetic device.^{23,24} Clinically, CNS stimulation is used to ameliorate symptoms of Parkinson's disease,¹⁵⁵ and epilepsy.⁹ Stimulation of the

CHAPTER 4. A CMOS CURRENT STEERING NEUROSTIMULATION ARRAY

peripheral nervous system (PNS) has also been used to provide sensory feedback to users of prosthetic devices.^{29,156} Emerging applications of PNS stimulation include treatment of hypertension,¹⁵⁷ inflammatory disorders,¹⁵⁸ and heart failure.¹⁵⁹

Designing neurostimulator circuits with very-large-scale-integration (VLSI) technology allows for the development of miniaturized, fully implantable systems,¹⁶⁰ while simultaneously permitting the integration of extremely large numbers of channels,¹⁶¹ and increased functionality. Increased functionality means gains can be made in domains such as stimulation efficacy without compromising device size. This can be used to overcome limitations of electrical stimulation such as non-specificity.

It is straightforward to deliver electrical stimulation to target organs or neurons by placing electrodes within the proximity of the target. However, cell-types or tissue components cannot be selectively stimulated with electrical methods as robustly as they can be with optical methods, which poses a challenge for therapeutic stimulation systems. Modifying the stimulus pulse shape or duration is one method for achieving more selective stimulation.^{162,163} Another degree of selectivity comes from the limited spatial extent of the induced electric field within tissue. Spatial patterns of stimulation, such as bipolar and tripolar, can be used to shape the electric field *in-vivo* to target groups of cells that are topographically segregated.^{164–166} This has been leveraged in many neuroprosthetic applications such as cochlear implants,^{167,168} vestibular prostheses,¹⁶⁹ visual prostheses,¹⁷⁰ spinal stimulators,^{171,172} deep-brain stimulators,^{155,173} and peripheral nerve prosthetics.¹⁷⁴ Due to its widespread use, VLSI neurostimulator

CHAPTER 4. A CMOS CURRENT STEERING NEUROSTIMULATION ARRAY

systems should be designed to accurately stimulate in modes other than the standard monopolar and bipolar.^{175–177}

Additionally, circuits can be integrated with stimulator systems to ensure safety at the electrode-electrolyte interface. Chronic electrical stimulation can be damaging to both the electrode and tissue either through excitotoxic or electrochemical means.¹⁷⁸ Existing neural stimulators have addressed minimization of harmful electrochemical effects in several ways. Precise discrete components, or a capacitor in series with the output stage is one way to ensure no DC current flows through the electrode.^{179,180} A variety of ways amenable to VLSI implementation have also been proposed. Passive discharge is achieved by shorting the electrode to a reference voltage through a MOS switch, but due to the large RC time-constant associated with the electrode this can be a very slow process. An active discharge approach, i.e. driving the electrode to a reference voltage through a buffer, has similar effects as passive discharge, but limits the current that flows during the discharge phase.¹⁸¹ Very precise charge balancing can be obtained using feedback that measures and dynamically matches the anodic current.¹⁸² An alternative strategy is to monitor the electrode voltage after stimulation, and use a feedback controller to update stimulation parameters or apply compensatory pulses.^{183–185} By ensuring the electrode potential stays within safe limits, this approach prevents harmful charge buildup. In addition to the overhead required to implement the feedback loop, controller parameters must be tuned to obtain an acceptable transient response.

We introduce an architecture that includes a single calibration circuit that is shared across all channels in the array. This support-circuitry performs three functions. First, it accurately ratios the currents across channels. Second, within channels, it matches the anodic and cathodic phases for charge balancing. Finally, it allows for referenceless calibration of each channel’s digital-to-analog converter (DAC). Here we provide results from a circuit fabricated in a commercial 180 nm CMOS process. Additionally, we use the proposed circuits to stimulate the sciatic nerve of anesthetized rats. By measuring the induced electromyogram (EMG), we demonstrate *in-vivo* effects of spatially patterned nerve stimulation.

4.1 Circuit Design

The block diagram of a single channel of our circuit is illustrated in Fig. 4.1. Two independent current-mode DACs supply biases to the current sources. The output of either DAC can be mirrored into the calibration circuit by closing switch D or E. Switches A and C activate anodic and cathodic stimulation respectively. Switch G disconnects current sources from electrodes. Closing switches A, C and F causes the difference in the anodic and cathodic currents to flow into the calibration circuit. Switch H shorts the stimulation electrode to a reference voltage (V_{short}) to bleed off residual charge from the stimulation electrode.

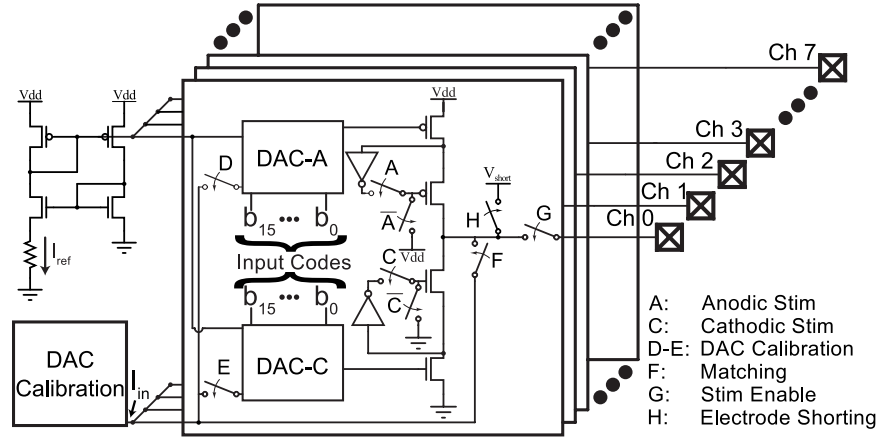


Figure 4.1: A block diagram for a single channel of the neural stimulator. Anodic and cathodic current sources have independent DACs which are routed to a calibration circuit for coarse calibration (switches D and E). When both current sources are simultaneously on, closing switch F allows the mismatch between the anodic and cathodic currents (the error current) to be measured by the calibration circuit. Switch H shorts the electrode to a reference voltage.

4.1.1 Digital-to-Analog Converter

DAC topologies used for neurostimulators include current steering DACs, implemented with binary¹⁸⁶ or unary¹⁷⁷ weighted current source arrays, and R-2R ladders.¹⁸¹ An advantage of current steering DACs is that only the current sources needed for stimulation are switched on, whereas in a splitter the entire current is consumed regardless of the selected code. However, the area consumed by the weighted arrays increases exponentially with the number of bits, whereas the area of a splitter increases linearly. So for large number of bits, the weighted arrays occupy prohibitive amount of area.

Both DACs (Fig. 4.2(a)) are 16-bit variations of the MOST R-2R structure.^{187,188} The PMOS switches in Fig. 4.2(a) ($M_{P,SW}$) operate as switched cascodes. This helps

CHAPTER 4. A CMOS CURRENT STEERING NEUROSTIMULATION ARRAY

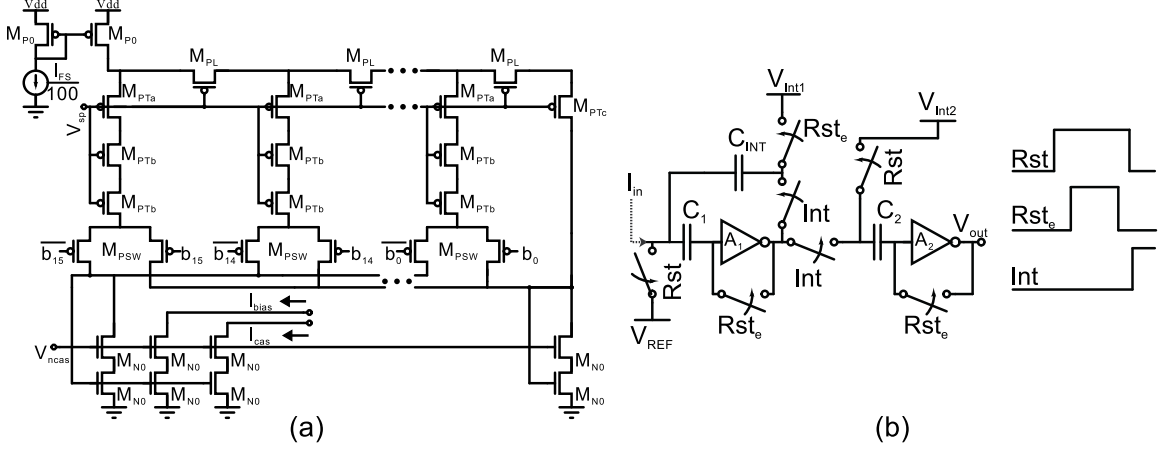


Figure 4.2: (a) Circuit diagram for the R- β R splitter. (b) The calibration circuit consists of an integrator and comparator for an analog-to-time-to-digital conversion.

reduce the sensitivity of the tap currents to the digital input code, which is important for the calibration procedure described later. Further, the increased lengths of the transistors in the vertical branches yield an R- β R structure; choosing $\beta=2.5$ provides a radix of 1.86 (derivation of the DAC radix as a function of β is provided in an appendix to this chapter, Section 4.10). At each node of an infinitely long R- β R ladder, if $\beta > 2$ (and the radix is < 2), more current flows laterally than vertically through the respective tap. This introduces redundancies into the input-output relationship.¹⁸⁹ These redundancies can be removed via digital calibration.¹⁹⁰

An external resistor sets the current reference to $1/100^{th}$ of the fullscale stimulation level (I_{FS}). This current is mirrored with unity-gain into each DAC. Two copies of the programmed current are mirrored out (I_{bias} and I_{cas} in Fig. 4.2) to generate the voltage biases used in the output current buffer in Fig. 4.3. The total current consumed by the DAC and biasing network is $2 \times I_{FS}/100 + 8 \times I_{stim}/100$. Transistor

Table 4.1: Transistor sizing in the R- β R splitter

Transistor	W/L (μm)
M_{P0}	$4 \times 3.6/3.6$
M_{PL}	$0.84/0.4$
M_{PTa}	$0.84/0.4$
M_{PTb}	$0.84/0.3$
M_{PTc}	$0.84/0.52$
M_{PSW}	$2 \times 0.84/0.6$
M_{N0}	$2 \times 2.36/2.36$

sizing for the devices in Fig. 4.8 can be found in Table 4.1.

4.1.2 Calibration Circuit

The calibration circuit, shown in Fig. 4.1(b), consists of an integrator and a comparator described previously.^{146,191} Briefly, when Rst and Rst_e are high, the offsets of the inverters (common-source amplifiers, A_1, A_2) are stored on the capacitors in series with their inputs, the inverters are reset to their tripping point, and the integration capacitor is precharged. The offsets between Rst and Rst_e are to mitigate errors due to charge injection.¹⁹² When Int goes high, C_{INT} appears in parallel with A_1 , and the input current is integrated. When the output of A_1 passes through V_{Int2} , A_2 trips. The time it takes for A_2 to trip is quantified with a counter, digitizing the input current.

$V_{Int1,2}$ are generated off-chip and set to 800 mV and 2.5 V to keep all devices in saturation during the integration. Their precise values do not matter, so they could be

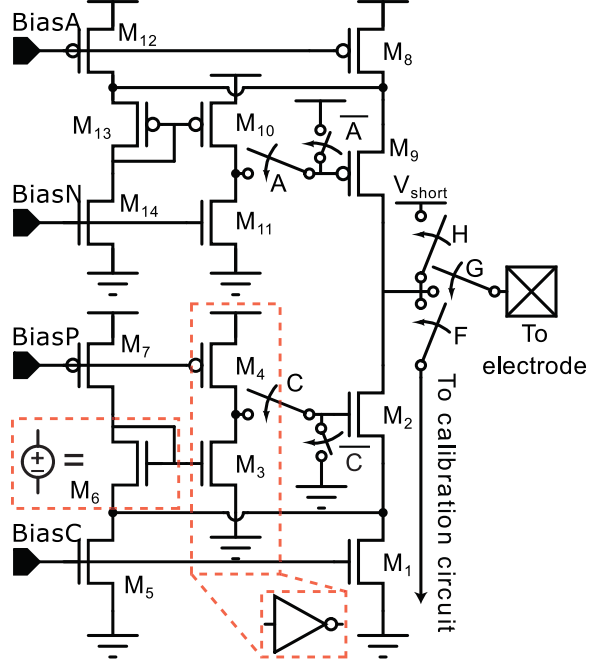


Figure 4.3: A modified regulated cascode, described in,¹⁹² serves as the output current source.

generated on-chip using a resistor string and a pair of buffers to drive the offset-storage capacitor and integration capacitor. The integration capacitor is 4.5 pF, providing an integration times greater than 3 μ s. This analog-to-time-to-digital conversion is used in a calibration procedure described in Section 4.2, and allows for the removal of the redundancies of the R- β R ladder. Additionally, Section 4.3 describes how the measurement can be used to match the anodic and cathodic stimulation phases.

4.1.3 Biphasic Current Source

The output current sources are regulated cascodes; an additional branch (M5-M7 in Fig. 4.3) increases the output swing.¹⁹² The gate of M3 is the input to a

CHAPTER 4. A CMOS CURRENT STEERING NEUROSTIMULATION ARRAY

Table 4.2: Transistor sizing in the current buffer

Transistor	W/L (μm)	Transistor	W/L (μm)
$M_{1,2}$	$200 \times 1.5/1.4$	$M_{8,9}$	$300 \times 0.95/0.71$
M_5	$2 \times 1.5/1.4$	M_{12}	$3 \times 0.95/0.71$
M_3	$4 \times 2/2$	M_{10}	$16 \times 1/1$
M_6	$12 \times 2/2$	M_{13}	$48 \times 1/1$
M_4	$2 \times 1/2.5$	M_{11}	$15 \times 1/5$
M_7	$1/2.5$	M_{14}	$5 \times 1/5$

common source amplifier that provides output impedance boosting. Typically, this is connected to the drain of M1, which must stay in the vicinity of V_{th} , so that M3 is at least weakly inverted.

M7 and M4 are biased to source $I_{stim}/100$ and $I_{stim}/50$ respectively, and M5 is an additional finger of M1. M6 acts as a level-shifter, which allows the drain of M1 to drop to $V_{ds,sat}$. Since $V_{ds,1}$ is set to a value equal to the difference in V_{gs} between M3 and M6, the aspect ratios of $M_{3,6}$ are set to provide sufficient $V_{ds,1}$ for all output currents. The output swing of the current source is $2V_{ds,sat}$ from each supply rail, and the devices were sized to give a $V_{ds,sat}$ of 120 mV and 150 mV for the NMOS and PMOS devices respectively. Maximizing output swing was a major concern, as large voltages can be developed across the electrode-electrolyte interface.

The feedback in regulated cascode circuits can lead to instability. M2 and M9 in Fig. 4.3 are driven by the feedback amplifiers, and are sized with a very large W/L (Table 4.2) to minimize their $V_{ds,sat}$. The large gate area provides a large load capacitance (400fF - 1pF depending on bias condition) to the feedback common-source

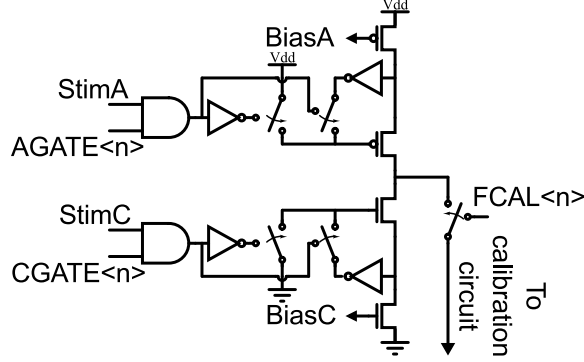


Figure 4.4: The signals that activate the current sources, and connect the current sources to the calibration circuit are gated by a set of registers that are programmed serially.

amplifier which stabilizes the circuit.⁵⁷

In practice, the signals that turn on the current sources (A and C in Fig. 4.3) are gated by the bits within two serially loaded registers, AGATE<0:7> and CGATE<0:7>. This configuration, shown in Fig. 4.4, permits the generation of arbitrary spatial stimulation patterns.

4.2 Calibration Procedure

A sub-binary radix DAC can produce an analog output x , scaled from -1 to 1, from an n -bit binary code (here, $n = 16$) found through n iterations of the algorithm of Eqn. 4.1.¹⁹³ In Eqn. 4.1, r_k represents the residue at the k^{th} step, and is initialized to be x , b_k is the k^{th} bit in the binary code, and γ_k is the radix at the k^{th} step.

$$b_k = \text{sign}(r_{k-1}) \quad (4.1)$$

$$r_k = \gamma_k r_{k-1} - b_k$$

CHAPTER 4. A CMOS CURRENT STEERING NEUROSTIMULATION ARRAY

For Fig. 4.8(a), γ_k is the ratio of currents flowing in adjacent vertical branches (tap currents). Therefore, to calibrate the DAC, we first obtain estimates of the tap currents.

The time Δt for a DC current source I_{in} to charge a capacitor C_I from V_{Int1} to V_{Int2} is:

$$\Delta t = C_I(V_{Int1} - V_{Int2})/I_{in} \quad (4.2)$$

$$I_{in} = \sum_{j=0}^{N-1} i_j b_j = \mathbf{b}^T \mathbf{i} \quad (4.3)$$

Here, \mathbf{b} is a column vector of zeros and ones corresponding to the input binary code, and \mathbf{i} is the column vector of tap currents. Combining Eqns. 4.2 and 4.3 gives Eqn. 4.4, where $C_I(V_{Int1} - V_{Int2})$ can be replaced by a single constant c_1 .

$$\mathbf{b}^T \mathbf{i} = c_1(\Delta t)^{-1} \quad (4.4)$$

Eqn. 4.4 contains 16 unknowns (the 16 elements in \mathbf{i}). For M DAC currents, the inverse of the integration times (Δt), obtained using the calibration circuit described in Section 4.1.2, are stored in a vector \mathbf{f} and the corresponding M input codes are stored in an $M \times 16$ matrix \mathbf{B} . With $M > 16$, the system can be solved in the least squares sense. In practice, we make use of all 2^{16} measurements for each DAC.

We chose to fit our solution to the differential linearity since it is much less affected by global nonlinearities which are approximately linear at small scales. Therefore, the inverse times in \mathbf{f} and the rows of \mathbf{B} are sorted in ascending order and adjacent values differenced yielding \mathbf{f}_Δ and \mathbf{B}_Δ respectively.

Then, the least squares estimate of the tap current coefficients, $\hat{\mathbf{i}}$ is found by solving $\mathbf{B}_\Delta \mathbf{i} = c_1 \mathbf{f}_\Delta$

$$\hat{\mathbf{i}} = c_1 (\mathbf{B}_\Delta^T \mathbf{B}_\Delta)^{-1} \mathbf{B}_\Delta^T \mathbf{f}_\Delta \quad (4.5)$$

Since each γ_i is a ratio of the elements of $\hat{\mathbf{i}}$, the constant c_1 cancels, except in the case of the MSB. For that case, γ_{15} is obtained by taking the ratio of i_{15} to the sum of the other elements of $\hat{\mathbf{i}}$. The precise values of γ_i do not matter if they are <2 , providing a degree of insensitivity to the mismatch in the R- β R ladder of Fig. 4.2.

Here, the calibration procedure is initiated by an external FPGA which monitors and times the output of the comparator (V_{out} Fig. 4.2(b)). Integration times are uploaded to a PC which obtains the least-squares solution. In practice, the system need not be connected to a PC. Calculation of the DAC coefficients ($\gamma_0 - \gamma_{15}$) could be performed once by a low power FPGA or microcontroller using the recursive least-squares algorithm (RLS). With the calculated γ 's, the proper input code for a given output is obtained from 16 iterations of Eqn 4.1.

4.3 Matching

4.3.1 Charge Balancing

Matching the two stimulation phases is performed by activating both current sources and closing switch F in Fig. 4.1. The difference between the two currents,

CHAPTER 4. A CMOS CURRENT STEERING NEUROSTIMULATION ARRAY

the error current, will flow into the integrator in Fig. 4.8(b). The matching procedure consists of two steps.

First, V_{Int1} and V_{Int2} are set equal, and an integration is triggered. The state of V_{out} reflects the polarity of the error current. For example, if the anodic current is larger than the cathodic current, the output of the integrator will fall, and V_{out} will hit the positive rail ($V_{out} = 1$). Likewise, if the cathodic current is larger, the output of the integrator will rise and V_{out} will hit the negative rail ($V_{out} = 0$).

Next, $V_{Int1} \neq V_{Int2}$; if at the end of step 1, $V_{out} = 1$, then $V_{Int1} > V_{Int2}$, and vice versa. When an integration is triggered, the time it takes for the comparator to trip is inversely proportional to the error current. Therefore, the error current integration is timed and the input code to one of the DACs is adjusted until the error current is minimized.

The integration time for matching is bounded only by leakage currents, which should cause the comparator to trip over time scales of seconds. Therefore, in software a timeout of 150 ms is enforced. Furthermore, to facilitate a quick matching procedure, a successive approximation strategy is used, where the outcome of step 1 is used to determine the state of a given bit in the binary code, and at the end, the code with the maximum integration time is selected.

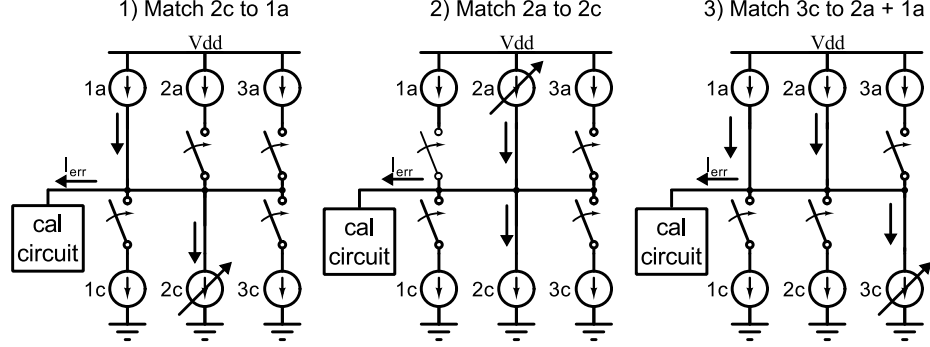


Figure 4.5: The calibration circuit can be used to generate spatial stimulation patterns. Here, a triphasic pattern can be generated by first matching the anodic phases of two channels, then matching the cathodic phase of a third channel to their sum.

4.3.2 Current Steering

The above procedure can be generalized to match stimulation across channels, allowing the circuit to operate in bipolar stimulation mode, or to create complex current-steering stimulation patterns. Fig. 4.4, illustrates a single stimulator channel with the control signals that are arrayed across all channels. An 8-bit serially loaded register FCAL controls the switches (switch F in Fig 4.1) that route currents to the calibration circuit. Along with the gating discussed in Section 4.3, arbitrary combinations of channels can be matched by connecting all active channels to the calibration circuit simultaneously, and asserting the required gating bits.

For example, a tripolar configuration consists of one cathodic channel sinking a current of I_c , counterbalanced by two anodic channels, each sourcing a current $I_a = I_c/2$. Fig. 4.5 depicts how a tripolar stimulation pattern can be generated in three steps. In steps 1 and 2, the anodic channels (1a and 2a) are indirectly matched to each other. In the third step, the cathodic channel (3c) is matched to their sum.

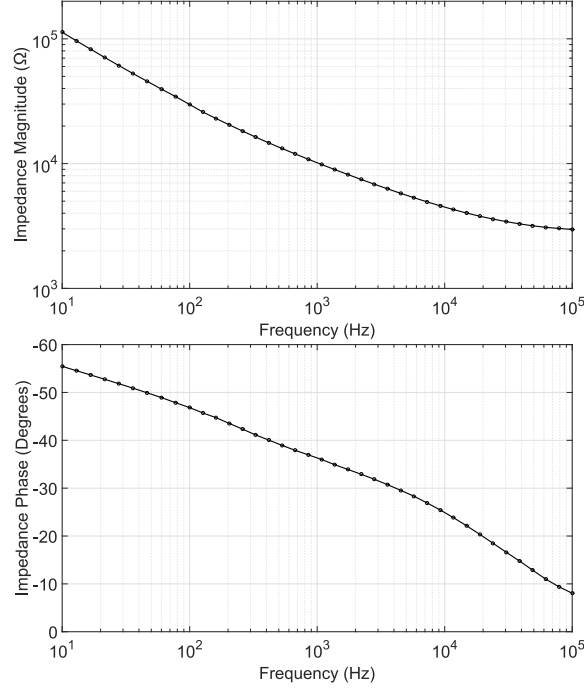


Figure 4.6: Impedance data for a stainless-steel cuff electrode used to interface the stimulator in-vivo.

This procedure fixes the digital codes for the anodic sources of channel 1 and 2, and the cathodic source of channel 3. The complementary DACs must then be tuned for in-channel charge balance.

4.4 Electrode Interface

We interfaced our stimulator to concentric cuff electrodes (MicroProbes for Life Science, Gaithersburg, MD). Each cuff contained nine $125 \mu\text{m}$ diameter stainless steel contacts, with three groups of three electrodes arranged circumferentially, 90 degrees apart, and with each group spaced 2.5 mm apart (Fig. 4.13 (inset)). These electrodes,

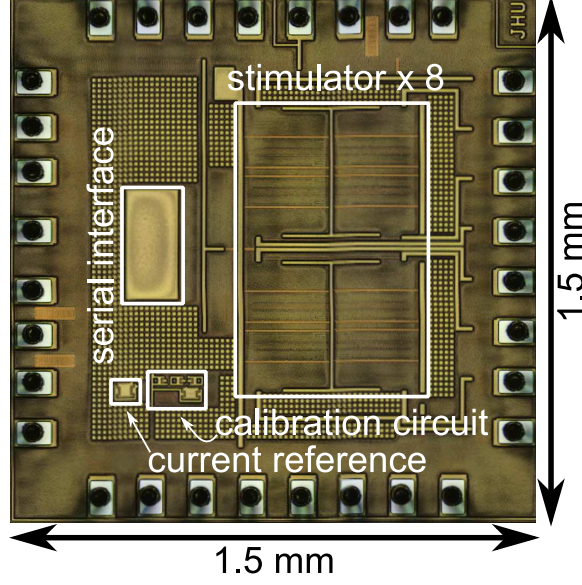


Figure 4.7: Micrograph of an eight-channel stimulator, fabricated in a $0.18\ \mu\text{m}$ CMOS process. The die size including pads measures $1.5 \times 1.5\ \text{mm}^2$.

when used for acute, small-animal studies, and at low current levels ($\leq 250\ \mu\text{A}$), do not require high voltage transistors or special circuit techniques to prevent oxide breakdown or hot-carrier effects. Figure 4.6 illustrates typical magnitude and phase data for these electrodes.

4.5 Benchtop Characterization

An eight channel version of the neural stimulator was fabricated in a $0.18\ \mu\text{m}$ CMOS process. A micrograph of the $1.5\ \text{mm} \times 1.5\ \text{mm}$ chip is illustrated in Fig 4.7. Each stimulator channel, including DACs, occupied an area of $290\ \mu\text{m} \times 220\ \mu\text{m}$, and the calibration circuit occupied $200\ \mu\text{m} \times 70\ \mu\text{m}$. Additionally, an SPI interface was synthesized from a standard cell library. The remaining area consists of metal fill to

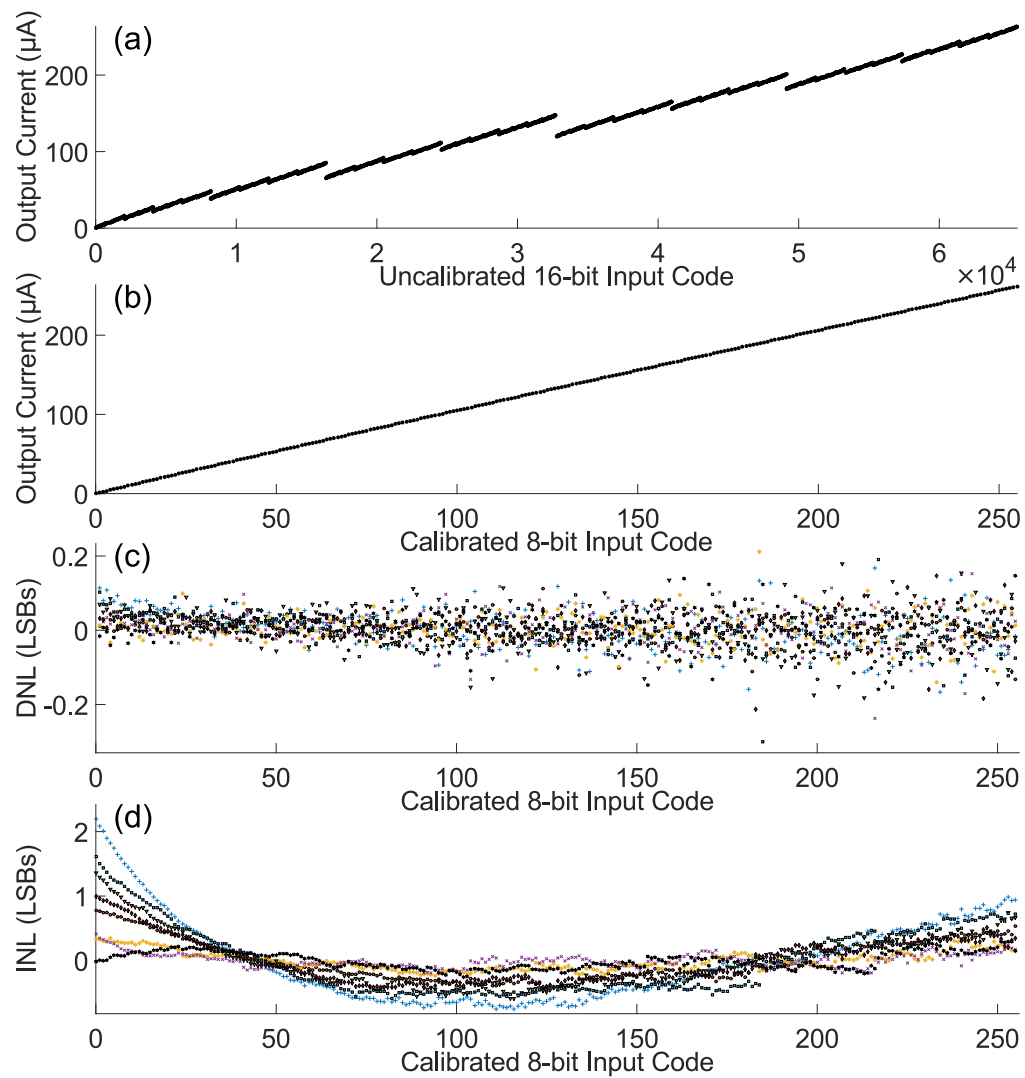


Figure 4.8: Input output relationship of the DAC before (a) and after calibration (b). Linearity is quantified by the differential non-linearity (DNL)(c) ≤ 0.3 LSBs and the integral non-linearity (INL)(d) < 3 LSBs. Points represent data across 8 channels.

meet foundry density requirements.

4.5.1 DAC Calibration

Fig. 4.8(a,b) shows the digital input - analog output relationship before and after calibration for a single channel. The pre-calibration non-monotonicity is by design and clearly evident, and the procedure described in Section 4.2 was used to remove the redundancies. The measured differential non-linearity (DNL) and integral non-linearity (INL) for all channels are summarized in Fig. 4.8(c,d). The worst case DNL was 0.3 LSBs, and the mean absolute value was <0.04 LSBs. INL was defined as the difference between the actual output and the best-fit line. The worst case INL was measured to be 2.2 LSBs, and the mean absolute value was <0.3 LSBs. Currents were measured with a Keithley 6430 Source Measurement Unit.

Integration times ranged from $3\ \mu\text{s}$ to 30 ms, and the calibration process for each DAC took less than 9 seconds on average. Calibration of all 16 DACs took 140 seconds.

4.5.2 Matching

The matching error was determined by measuring the mean residual voltage left on a 100 nF capacitor following four biphasic $200\ \mu\text{s}$ pulses, and normalizing that value to the peak capacitor voltage at full-scale. The capacitor voltage was buffered by an

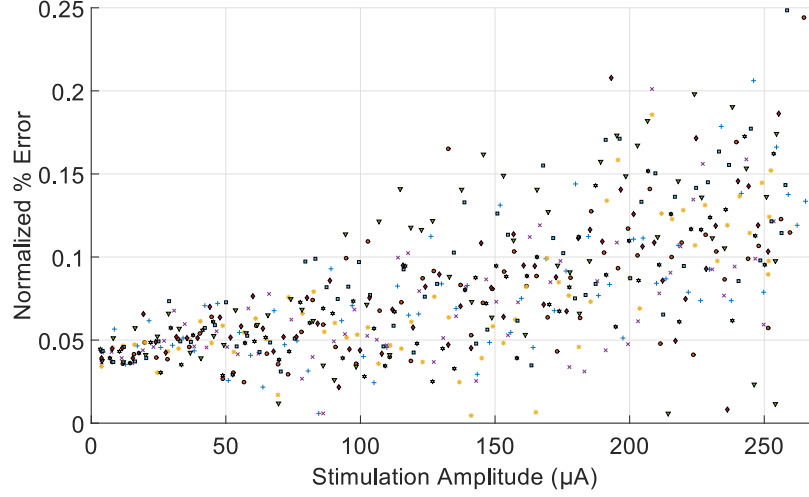


Figure 4.9: The difference between the anodic and cathodic currents normalized to the full scale current.

off-the-shelf CMOS op-amp (AD8608, Analog Devices, Norwood, MA), and digitized by a DAQ with a 16-bit A/D converter (NI USB 6251, National Instruments, Austin, TX). The capacitor voltage was sampled at 1 MHz for 150 μ s before and after each biphasic pulse. Each set of 150 samples were averaged, and the difference gave the voltage error, which was then referred back to an equivalent error current. For each measurement, to mitigate the effects of measurement noise, the dynamic range of the DAQ was set to the minimum necessary voltage to accommodate the peak capacitor voltage. This ranged from ± 0.1 V (the device minimum) to ± 1 V.

Fig. 4.9 illustrates the error currents after matching, normalized to the full-scale current output. We performed this measurement only on a subset of calibrated DAC values. For each channel 64 measurements were made instead of all 256. The worst-case error is less than 0.3% of the full-scale current, comparable with other state-of-

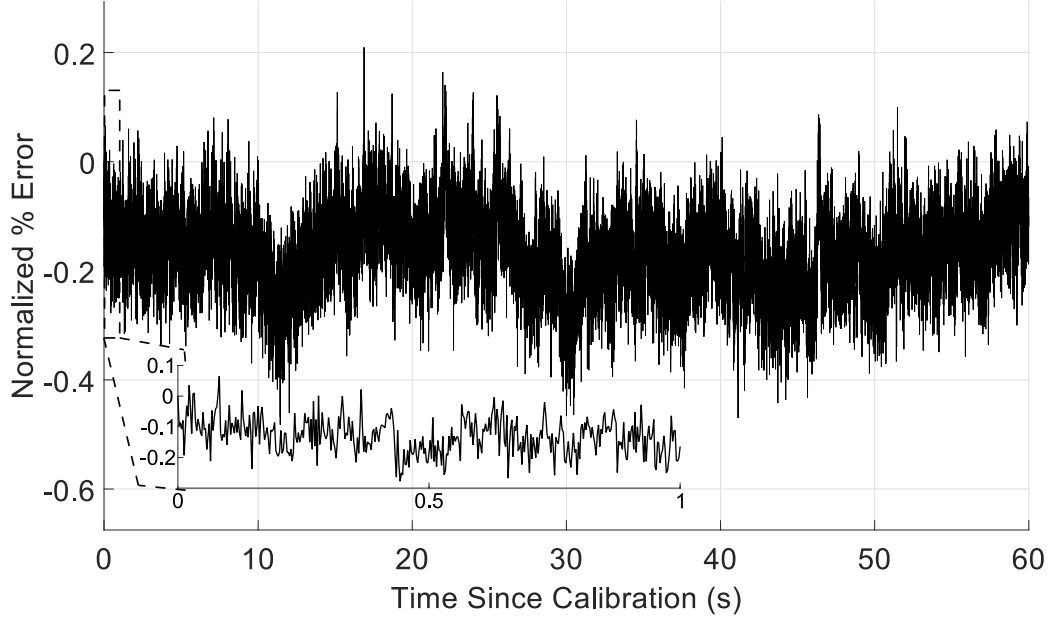


Figure 4.10: Variation in the matching between anodic and cathodic currents over time.

the-art designs.^{161,194} It typically takes less than 200 ms to find the closest match. One advantage of this design is that once matching is performed, the parameters can be stored digitally. However, this also leads to a potential limitation in its sensitivity to $1/f$ noise. To evaluate this possibility, we continuously applied $250\ \mu\text{A}$ pulses to a capacitor over the course of 60 seconds, measuring the residual voltage after each pulse. The pulse widths were $200\ \mu\text{s}$, and the pulse rate was 400 Hz, for a total of 24,000 pulses. After each pulse, a $200\ \mu\text{s}$ delay was added to allow calculation of the residual voltage in post-processing, and then the shorting switch was closed to bring the capacitor voltage back to baseline before the next pulse.

Fig 4.10 shows the residual capacitor voltage, normalized to the peak voltage, over time. The error over all 24,000 pulses had a mean and standard deviation of

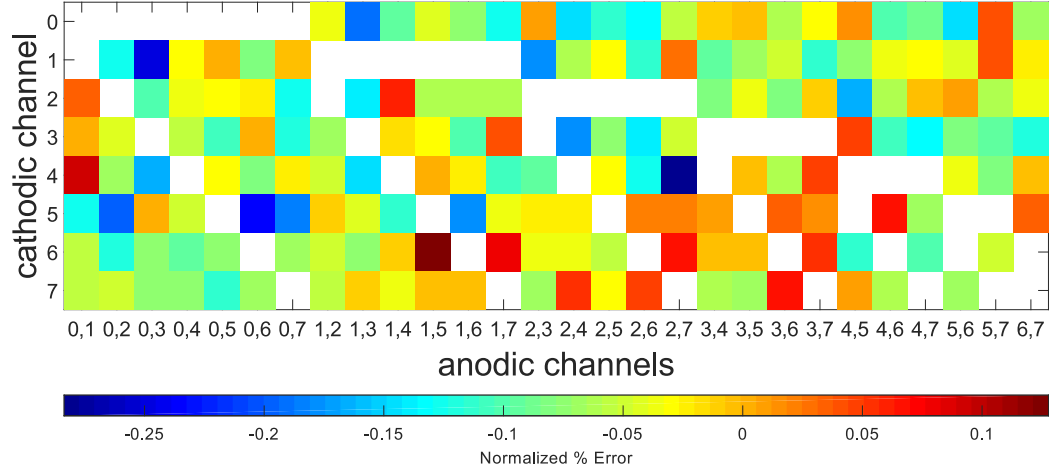


Figure 4.11: The percent difference between the stimulating cathodic current and a pair of anodic channels. The y-axis indicates the channel selected as the cathodic source, and the x-axis corresponds to the different pairs of channels that complete the tripolar unit. White entries correspond to combinations where the cathodic channel and anodic pair conflict.

0.17% and 0.07%; over the first 400 pulses (Fig. 4.10 inset) the mean and standard deviation were 0.12% and 0.06%.

4.5.3 Current Steering

The accuracy of matching, when performed across channels, was also evaluated. Here, error was determined by shorting all channels to a single 10 nF capacitor and measuring the voltage on the capacitor during the inter-pulse interval. Fig. 4.11 shows the measured error from matching a tripolar configuration (Fig. 4.5). The rows of Fig. 4.11 correspond to the channel selected as the cathodic sink ($I_c = 250 \mu\text{A}$). The columns correspond to different channel pairs that complete the tripolar unit. There are 28 possible pairs of channels, 7 of which include the channel used as the cathodic

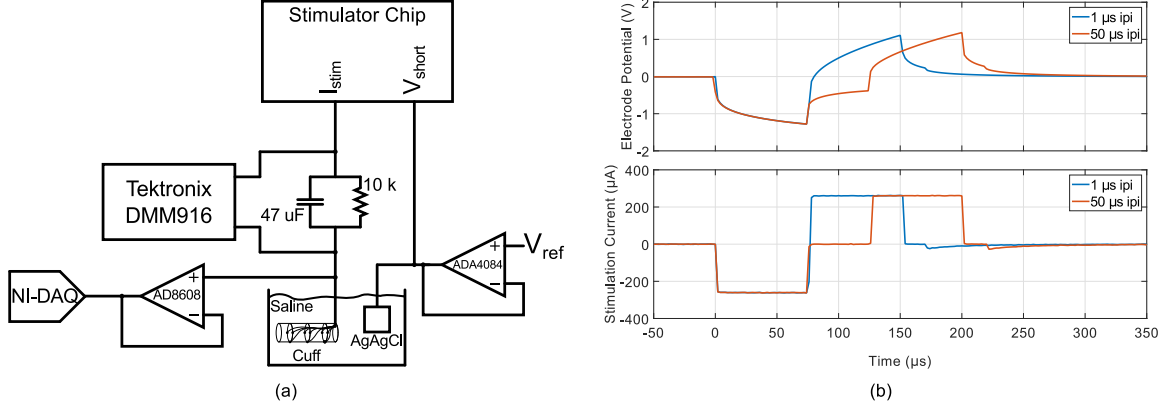


Figure 4.12: (a) Experimental setup for *in-vitro* testing. A parallel RC was placed in series with the stimulator and the cuff electrode array submerged in saline along with an AgAgCl return electrode. A Tektronix digital multi-meter (DMM) measured the average voltage across the RC to record the effective DC current. (b) The electrode potential time-domain waveform and current profile. A CMOS input op-amp was used to buffer the electrode waveform and digitized with a 16-bit NI-DAQ. Two waveforms are shown, one with a 1 μs inter-pulse interval (ipi) and the other with a 50 μs ipi. The current profile was measured by replacing the parallel RC with a single 100 Ω resistor, adding a second buffer, and feeding the two buffered waveforms into the DAQ to be read differentially.

sink (white entries). As with charge balancing, the errors were measured $< 0.3\%$.

4.6 In-vitro Results

We used the setup depicted in Fig. 4.12(a) to evaluate the effective DC current when stimulating through electrodes. We measured the effective DC level for 250 μA , 75 μs stimulation at 500, and 1000 Hz, with two inter-pulse-intervals (1 μs and 50 μs). Matching was performed immediately before the pulse train started, and the shorting switch was activated in between biphasic pulses. No re-calibration was made during this interval. Fig. 4.12(b) shows the time-domain stimulation waveform recorded

Table 4.3: Effective DC measured in-vitro

Frequency (Hz)	Inter-pulse interval (μs)	DC (nA)	Current density (nA/mm ²)
500	1	2	163
500	50	3	244
1000	1	3	244
1000	50	5	407

during this measurement. The DC measurement was given 1 minute to settle; the values listed in Table 4.3 lists the maximum DC measured by the DMM thereafter as well as the current density given the 0.0123 mm² electrode surface area. To evaluate the effect of $1/f$ noise *in-vitro*, the 1000 Hz, 50 μs ipi measurement was taken out to 10 minutes. Throughout the test, the maximum and minimum measurement was 5 nA and 3 nA respectively, with the mean shifting slightly from 5 nA to 4 nA after 5 minutes.

4.7 In-vivo Results

To test the stimulator *in-vivo*, we interfaced the cuff electrode described in Section 4.4 to the sciatic nerve of rats, and recorded electromyogram (EMG) signals from the tibialis anterior (TA) and gastrocnemius (GM) muscles of the lower leg (Fig. 4.13). Male Wistar rats weighting 300-320 g were used in this experiment. All procedures were approved by Johns Hopkins Medical Institute Animal Care and Use Committee (ACUC). Each rat was implanted under 2% isoflurane anesthesia with a nose cone.

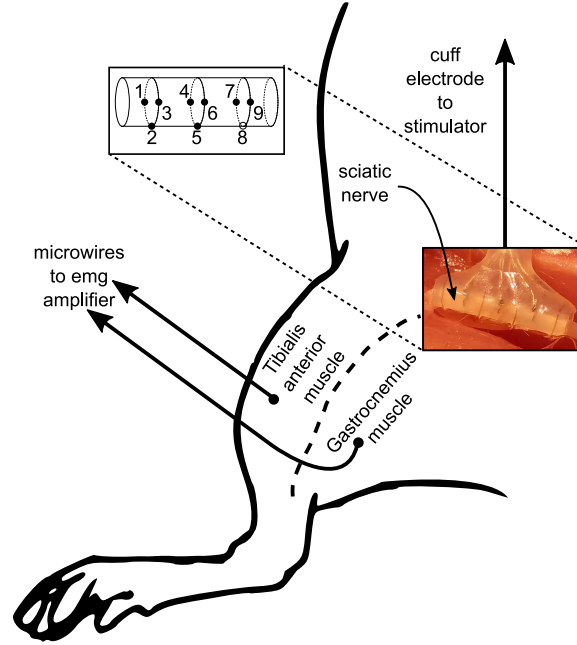


Figure 4.13: Experimental setup for *in-vivo* testing. A multi-channel concentric cuff was interfaced to the sciatic nerve of rats. The electrode consisted of three concentric triplets for a total of nine electrodes, and eight of the nine electrodes (solid circles in inset) were connected to the neurostimulator chip. Microwires were inserted into two muscle groups (tibialis anterior and gastrocnemius) to record intramuscular EMG in response to stimulation.

After swabbing the dissection area with 70% ethanol, the skin was cut along the back of the thigh. The left sciatic nerve was dissected at the midthigh and carefully freed from surrounding tissues from the sciatic notch to the knee. The cuff electrode was opened and placed around the sciatic nerve avoiding compression and stretch. To record EMG activity, pairs of fine wire hook electrodes (two 40-gauge Teflon-coated steel wires in a 27-gauge 12.5 mm hypodermic needle) were implanted in the left gastrocnemius (GM) and tibialis anterior (TA) muscle; signals were amplified and digitized with an RA16PA preamplifier (Tucker-Davis Technologies, Alachua, FL). All EMG responses plotted in Figs. 4.14, 4.15 are averages of five responses.

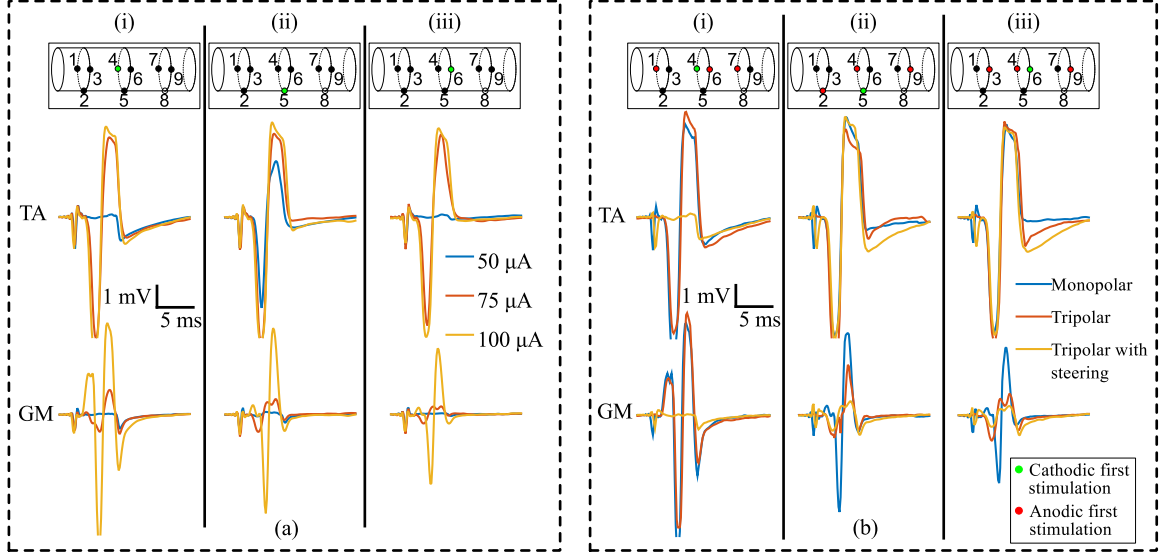


Figure 4.14: *In-vivo* recorded physiological response to spatially patterned nerve stimulation in an anesthetized rat. In all plots, cuff schematics indicate the electrodes used, and the polarity of stimulation at those sites. Green indicates cathodic first, and red indicates anodic first. (a) EMG response of the tibialis anterior (TA) muscle (top row) and the gastrocnemius (GM) muscle (bottom row) to monopolar stimulation of the three center-ring electrodes at three levels of stimulation. (b) EMG response of TA (top row) and GM (bottom row) to three patterns of stimulation at $100 \mu\text{A}$.

The EMG response from monopolar stimulation of each of the center triplet's contacts is depicted in Fig. 4.14(a). Stimulation consisted of single pulses with a $75 \mu\text{s}$ pulse width, and a $50 \mu\text{s}$ inter-pulse interval. The current's return path was through a stainless steel needle electrode in the neck. Electrode 5 showed the highest sensitivity for TA; a $50 \mu\text{A}$ pulse was sufficient to evoke an EMG response, while no response was seen in GM. A $75 \mu\text{A}$ pulse was needed at electrodes 4 and 6 to evoke a response, but each site still appeared selective to TA. At each site, the non-specificity of stimulation prevented the stimulator from inducing the maximal response from TA without activation of GM.

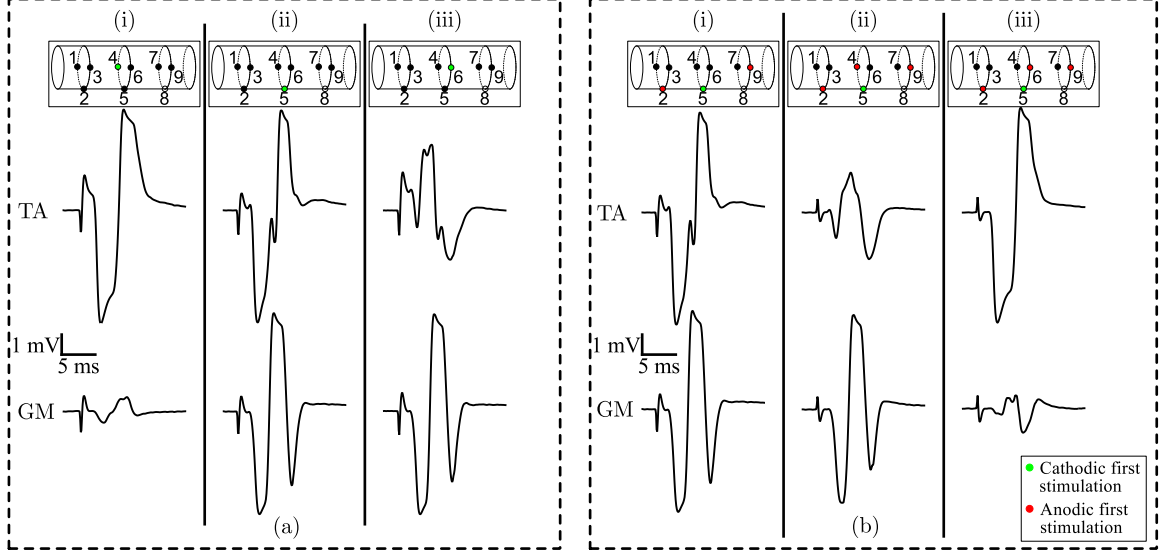


Figure 4.15: EMG response to stimulation of the sciatic nerve in the TA (top row) and GM muscles (bottom row). (a) Columns i-iii show responses due to monopolar stimulation at the three center contacts. (b) Column i shows the response to a tripolar stimulation pattern, with electrode 5 used as the cathodic contact, and columns ii-iii show the altered response when an anodic steering contact is added at electrodes 4 and 6 respectively. The anodic contact at electrode 4 attenuates the TA response while the anodic contact at electrode 6 attenuates the GM response.

Current steering stimulation patterns were applied to assess how EMG responses might be altered. Fig. 4.14(b) compares the EMG response to three stimulation patterns, monopolar, tripolar, and tripolar with an additional current steering contact. The tripolar pattern consisted of the middle contact activated cathodic first (primary electrode), and the two adjacent electrodes activated anodic first, calibrated with an amplitude of $1/2$ as described in Section 4.3. The tripolar with current steering pattern was identical to the tripolar pattern, but with an additional second center contact activated anodic first with an amplitude matched to the primary electrode. Patterned stimulation at electrodes 5 and 6 had a clear effect on the evoked response.

At electrode 4, the additional anodal contact suppressed an EMG response within both muscles; while not useful in practice, it is shown here for completeness.

Fig. 4.15 illustrates another example of the physiological effects of using the circuit for current steering stimulation. In this experiment, performed in a different rat, stimulation again consisted of single pulses. We used a $50\ \mu\text{s}$ pulse width, and a $50\ \mu\text{s}$ inter-pulse interval. Due to the decreased pulse width selected a slightly higher amplitude of $150\ \mu\text{A}$ was required to evoke maximal EMG responses. Fig. 4.15(a) shows the effects of monopolar stimulation to the three center contacts. Contact 4 is preferential to the TA muscle, contact 6 is preferential to the GM muscle, and contact 5 exhibits no preference. Fig. 4.15(b) illustrates the effects of steering. Columns i-iii depict the EMG response to tripolar stimulation with (i) no steering contact, (ii) electrode 4 as an anodic steering contact, and (iii) electrode 6 as an anodic steering contact. Steering with electrode 4 suppressed the EMG response in the TA muscle, while steering with electrode 6 suppressed the EMG response in the GM muscle.

4.8 Discussion

4.8.1 DAC Calibration

The post-calibration resolution of the DACs is limited to 8-bits. One likely cause is that the tap currents vary significantly with the input code. Interestingly, we have found the lower order bits seem to provide no additional benefit here. For example,

Table 4.4: Comparison of this work with the state-of-the-art

Parameter	This Work	195	177	186	194	196	161	183	182
Year	2016	2015	2015	2014	2014	2013	2013	2012	2007
Technology	0.18 μm	0.18 μm HV	0.5 μm HV	65 nm	0.35 μm HV	0.18 μm HV	65 nm	0.35 μm HV	0.7 μm HV
Supply Voltage (V)	3.3	18	12	3	15	12	± 2.5	20	+6/-9
Number of Channels	8	1	16	256	2	8	512	2	1
Max I_{stim} (mA)	0.25	1.05	1.45	0.465	1	0.504	0.05	1	1
Resolution (ENOB)	8 (7.4)	7 (-)	9 (8)	5 (4.3)	5 (4.6)	6 (-)	5 (-)	5 (-)	7 (-)
Charge balance architecture	biphasic + calibration	H-bridge	current mirror	dynamic current mirror	dynamic current mirror	asymmetric H-bridge	biphasic + calibration	pulse insertion, offset regulation	dynamic current mirror
Matching (%)	0.3	<0.01	3.6 ± 2.5	0.5	0.1	0.05	2.24	N.A.	0.4
Stimulation Modes	multipolar	monopolar, bipolar	multipolar	multipolar	monopolar	bipolar	monopolar	monopolar	monopolar

running the algorithm on the upper 12 bits, leaving the lower 4 bits set to 0 provides the same level of accuracy and precision. However, presently, this is not much of a concern as most neurostimulator designs make use of only 5 to 6 bits (Table 4.4). Given that the precision of matching can exceed 0.3%, the lower bits do provide a benefit for charge balancing.

A limitation of the proposed calibration technique is that a linear regression is required to compute DAC coefficients. While an on-chip implementation of the recursive least squares algorithm is not prohibitive, it would be far more economical to have an FPGA or microcontroller compute the coefficients in the background and communicate them back to the stimulator chip.

4.8.2 Matching

The offline calibration strategy proposed here achieves a precision of 0.3% in matching of the anodic and cathodic phases. The use of an interpulse delay allows charge stored in the double-layer capacitance to be lost through faradaic reactions, but the inclusion of a passive discharge switch compensates.

The $1/f$ noise in the current sources and biasing network increases the variance of this measurement. To assess the long-term implications, we directly measured the DC current flowing through a cuff electrode *in-vitro* over ten minutes,^{197,198} and found only a 1 nA shift in the baseline. Reported safe current densities for effective DC *in-vivo* range from 230 nA/mm²¹⁹⁹ to 750 nA/mm².²⁰⁰ The maximum effective

DC level measured here (407 nA/mm^2) falls within this range. With recalibration performed every 10 minutes and 200 ms required per channel, the calibration circuit would need to operate with a duty cycle of only 0.27%.

4.8.3 In-vivo results

The results of Section 4.7 demonstrated altered physiological responses to current steering stimulation patterns. The parameter space for current steering stimulation is extensive, and we have not undertaken an exhaustive search for optimal patterns. The stimulation patterns tested here were based off of previous studies in similar animal models that have rigorously demonstrated the enhanced selectivity obtained through current steering.^{164,165,174} This is an active and promising area of research, and progress will likely rely on both novel hardware as well as mathematical modeling of the electric field profile in tissue.¹⁶⁶

One limitation was large variability between the two animals tested. For the first rat, we were unable to find any configurations (neither monopolar nor multipolar) that were selective for GM. The results from the second rat show that multi-electrode arrays themselves can offer some degree of selectivity. For the second rat both monopolar and multipolar configurations could be selective for GM and TA. Therefore, these results only serve to demonstrate feasibility.

Inter-animal variability was likely due to a combination of variations in nerve cuff electrode orientation and fine-wire electrode placement within the muscles of

interest. In particular, fine-wire electrodes have a small conduction volume that can sensitively collect even individual motor unit action potentials. Therefore, despite consistent placement within a specific muscle of interest, variations in the composition of motor units, in terms of muscle type and patterns of activation, may influence the output recorded by a fine-wire electrode. Future experiments could mitigate this effect through the use of multiple fine-wire electrodes, and taking either averaged measurements across the electrodes or differences between electrodes to capture higher conduction volumes. Additionally, prior work in the field have used cuff electrodes with contacts spanning the entire circumference of the nerve,^{164, 165, 174} whereas here the arrays used covered 75% of the nerve circumference, in the future, histological examination of the stimulated tissue should be made to validate.

4.9 Conclusion

We have presented an architecture for a current-steering neurostimulator array. An on-chip calibration circuit facilitates spatial patterning of the electric field *in-vivo* and additionally is used to calibrate an 8-bit current-mode DAC for each channel, as well as charge balance biphasic stimulation. The calibration circuitry is shared across channels, and therefore the architecture is particularly suited for high channel-count systems. Further, since charge balancing is achieved without off-chip components the system is amenable to implantable systems. Spatial patterning of electrical stimu-

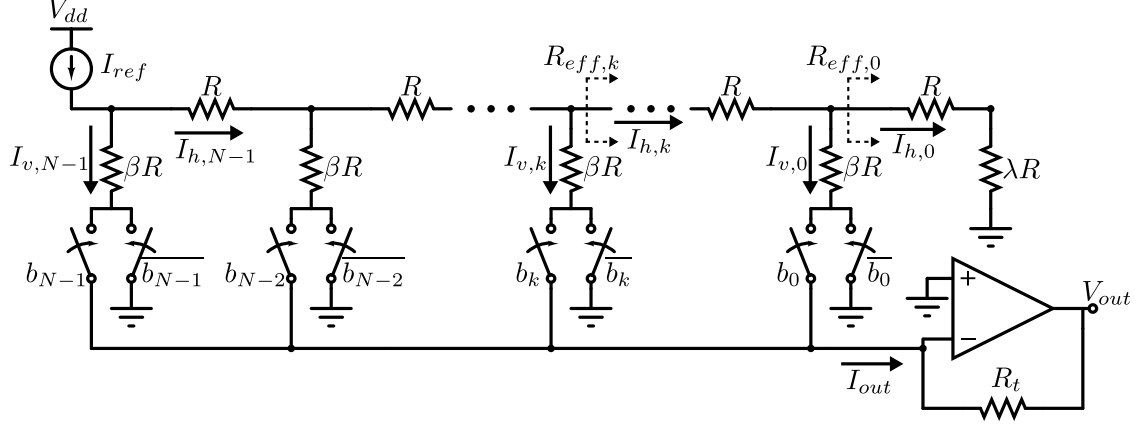


Figure 4.16: Schematic for an ideal R - βR splitter. At each tap, current splits off into a horizontal (I_h) and a vertical component (I_v) that depends on the value of β and the effective resistance looking down the remainder of the ladder, R_{eff} .

lation offers a method to activate specific targets *in-vivo*, a major obstacle in the development of low-side-effect neurotherapeutic stimulation systems

4.10 Appendix: Calculation of γ for an R - βR splitter

Fig. 4.16 illustrates an ideal resistor ladder DAC with horizontal and vertical components with resistances R and βR respectively. Each vertical branch is referred to as a tap, and the currents flowing in each vertical branch are referred to as tap currents. At the k^{th} tap, current divides into a horizontal component ($I_{h,k}$) and a vertical component ($I_{v,k}$) in proportions that depend on the geometry of the splitter. This is due to a current division between the vertical resistance, βR , and the effective

CHAPTER 4. A CMOS CURRENT STEERING NEUROSTIMULATION ARRAY

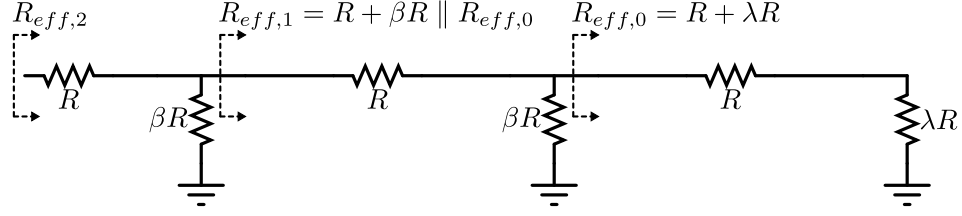


Figure 4.17: The effective ladder resistance depends on β and the terminating resistor λ . λ can be chosen such that $R_{eff,k}$ are the same for all k .

resistance looking down the remainder of the ladder at the k^{th} tap, $R_{eff,k}$. The amplifier serves to hold the current summing node at virtual ground, and converts the output current to a voltage through R_t , but this will be ignored moving forward.

In a mixed-radix number system, the radix at the k^{th} position is the ratio of the weight of the k^{th} position to the weight of the $k+1^{th}$ position. In an $R - \beta R$ splitter, the weights are the tap currents that get selected by the digital input code, and therefore the radix of the k^{th} tap, γ_k is given by the ratio:

$$\gamma_k = \frac{I_{v,k+1}}{I_{v,k}} \quad (4.6)$$

Note, that the radix at the MSB is undefined.

To find an expression for γ_k in terms of β , it is assumed that $R_{eff,k}$ is the same for all taps, and this is true if the proper value of λ is selected (or if the ladder is infinitely long). From Fig. 4.17, the effective resistance looking past the final (0^{th}) tap is $R_{eff,0} = R + \lambda R$. If λ is such that $\beta R \parallel (R + \lambda R) = \lambda R$, then the resistance looking past the 1^{st} tap, $R_{eff,1}$ is identical to $R_{eff,0}$, and so forth for *every* tap.

$$R_{eff,k} = R + \lambda R \quad (4.7)$$

CHAPTER 4. A CMOS CURRENT STEERING NEUROSTIMULATION ARRAY

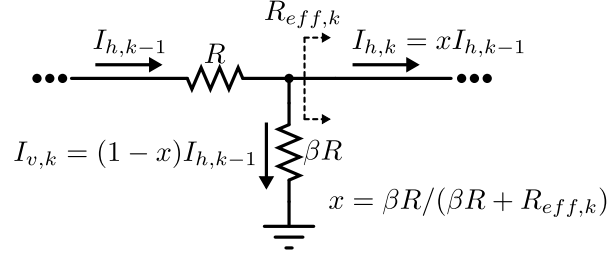


Figure 4.18: At the k^{th} tap, the incident current $I_{h,k-1}$ divides into a vertical and horizontal component. A fraction, x , continues horizontally, and the remainder, $(1 - x)$, exits vertically.

Using the equation for parallel resistors, the condition on λ that makes Eqn. 4.7 true for all k is

$$\frac{\beta R(R + \lambda R)}{\beta R + R + \lambda R} = \lambda R \quad (4.8)$$

Cancelling R , rearranging, and solving a quadratic equation for λ gives

$$\lambda = \frac{\sqrt{1 + 4\beta} - 1}{2} \quad (4.9)$$

With the resistance looking down the ladder the same at each tap, the input current to each tap splits in identical proportions at each tap. This is illustrated in Fig. 4.18. At the k^{th} tap, $xI_{h,k-1}$ continues horizontally and $(1 - x)I_{h,k-1}$ exits vertically. The currents in the horizontal and vertical branches at the k^{th} tap are given by the following equation in terms of the reference current I_{ref} , and the number of bits N .

$$\begin{aligned} I_{h,k} &= x^{N-k} I_{ref} \\ I_{v,k} &= (1 - x)x^{N-k-1} I_{ref} \end{aligned} \quad (4.10)$$

CHAPTER 4. A CMOS CURRENT STEERING NEUROSTIMULATION ARRAY

Plugging Eqn. 4.10 into Eqn. 4.6 gives

$$\gamma_k = \frac{1}{x} \quad (4.11)$$

The value of x can be found from Fig. 4.18 using the current divider equation and simplified with Eqn. 4.7.

$$x = \frac{\beta R}{\beta R + R_{eff,k}} = \frac{\beta}{\beta + 1 + \lambda} \quad (4.12)$$

Finally, plugging Eqns. 4.9,4.11 into Eqn. 4.12 gives

$$\gamma = \frac{1 + 2\beta + \sqrt{1 + 4\beta}}{2\beta} \quad (4.13)$$

With $\beta = 2.5$, the radix for the DAC used in the stimulator circuits can be found to be

$$\gamma = \frac{6 + \sqrt{11}}{5} = 1.86 \quad (4.14)$$

Chapter 5

A Bidirectional Neural Interface IC with Chopper Stabilized BioADC Array and Charge Balanced Stimulator

Biomarker extraction from physiological signals such as the electrocorticogram (ECoG) and local field potentials (LFP) is of paramount importance to the diagnosis and therapy for a large number of neurological disorders. This is nowhere more clear than for closed-loop neuromodulation therapies that drive stimulation or update stimulation parameters based on information obtained from detected biopotentials.²⁰¹ These types of systems hold potential to drastically improve the efficacy of open-loop

CHAPTER 5. A BIDIRECTIONAL NEURAL INTERFACE CHIP

neuromodulation, in applications such as deep-brain stimulation for Parkinson’s disease⁷⁵ and cortical stimulation for epilepsy.⁷² The success of closed-loop platforms will depend on the ability to process biopotential signals in real time, and use the information to tailor therapy. Ultra-low power processing of neural signals can be performed in the analog domain,¹⁰⁵ but the flexibility inherent to digital processing makes its use much more common.^{107, 108, 202} With closed-loop systems, like all implantable systems, a holistic approach is necessary as sensitivity, power consumption, and system size are all critical parameters.

A traditional biopotential measurement system adheres to a three step sequence: 1) low noise amplification and high pass filter, 2) variable gain amplification and bandpass or anti-aliasing filter, and finally 3) analog-to-digital conversion.²⁰³ If a single ADC is time-multiplexed across multiple channels, then an additional buffer per channel is required to drive the input capacitance of the ADC. Interestingly though, an increasingly popular design choice is to integrate an ADC into every channel.¹⁴⁶ This choice becomes even more favorable when designing with deep sub-micron processes, where very high power efficiency and very low area designs are obtained.^{204, 205} Nevertheless, these designs still abide by the standard paradigm of amplify, filter, then quantize, and each step requires power and silicon area.

The bidirectional interface presented here builds upon previous bioADC designs^{146, 207} for sensing functionality, and integrates everything from front-end sensing to back-end digital decimation in a single circuit per channel (Fig. 5.1). Without explicit volt-

CHAPTER 5. A BIDIRECTIONAL NEURAL INTERFACE CHIP

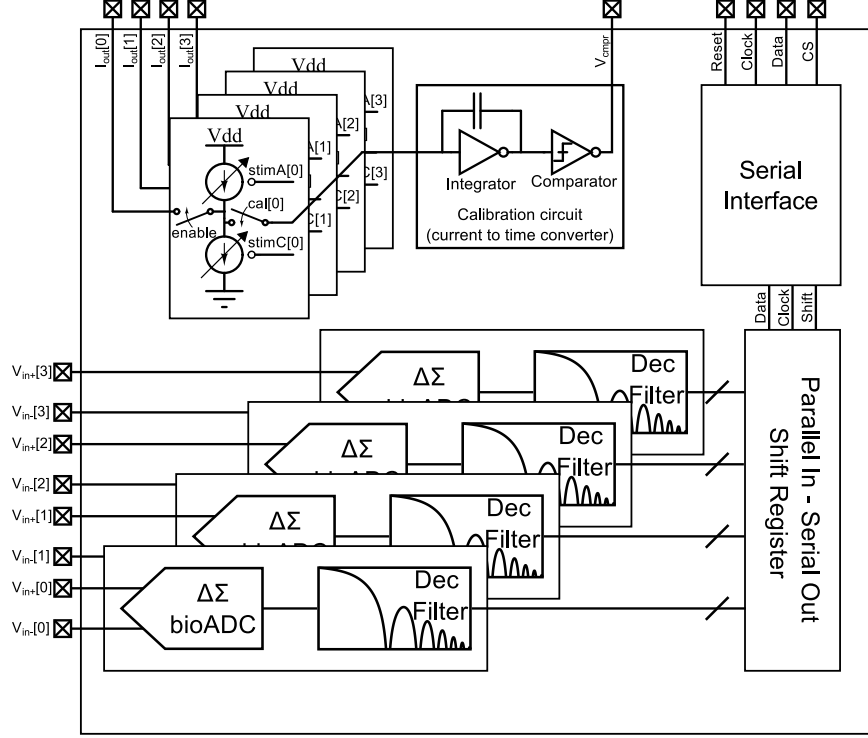


Figure 5.1: Overview of the proposed circuits. The designed chip contains four channels of recording and stimulation. An additional calibration circuit is used to match the anodic and cathodic current sources for charge balancing.²⁰⁶ A serial interface facilitates communication between this chip and an external processor.

age amplification, this circuit digitizes microvolt level neural signals. Compared with previous works, we demonstrate 1) an improvement in bit resolution by decimating a first-order noise-shaped bit stream with a second-order decimation filter, and 2) an improvement in noise-power efficiency through chopper-stabilization. For stimulation functionality, we integrated additional circuits for digitally controlled current stimulation.²⁰⁶ Four channels of both sensing and stimulation were fabricated on a single $1.5 \times 1.5 \text{ mm}^2$ chip, and offers a versatile platform for closed-loop neuromodulation.

The organization of this chapter is as follows. In Section 5.1 we describe the

core elements of the $\Delta\Sigma$ bioADC. The stimulator architecture is briefly described in Section 5.1.6, but has been described in detail in Chapter 4. Section 5.2 contains characterizations of the bioADC in terms of SNDR, input-referred noise, common-mode rejection ratio (CMRR), and input impedance, and Section 5.2.3 presents *in-vivo* demonstrations. Finally, Section 5.3 provides a comparison of this work with the state of the art, and concludes the paper.

5.1 Circuit Design

The schematic for a single channel in Fig. 5.2(a) illustrates the main components of the system. An operational transconductance amplifier (OTA), loaded with a large output capacitor (13 pF), operates as a $G_m - C$ integrator. A latched comparator is used as a 1-bit quantizer, which drives an auxiliary transconductor supplying a feedback current to the integration capacitor, implementing a 1-bit digital-to-analog converter (DAC). As shown in Fig. 5.2(b), the loop operates as a continuous-time, first-order $\Delta\Sigma$ ADC which have inherent anti-aliasing properties.²⁰⁸ The bitstream generated by the comparator (Q) is decimated by a second-order comb filter with a transfer function given by $((1 - z^{-N})/(1 - z^{-1}))^2$. The second-order decimation filter substantially extends the bit resolution obtainable from the first-order $\Delta\Sigma$ noise shaping, offering 1.5 bits for each two-fold in oversampling ratio (OSR) rather than a single bit per two-fold OSR for a conventional first-order (counter) decimator or

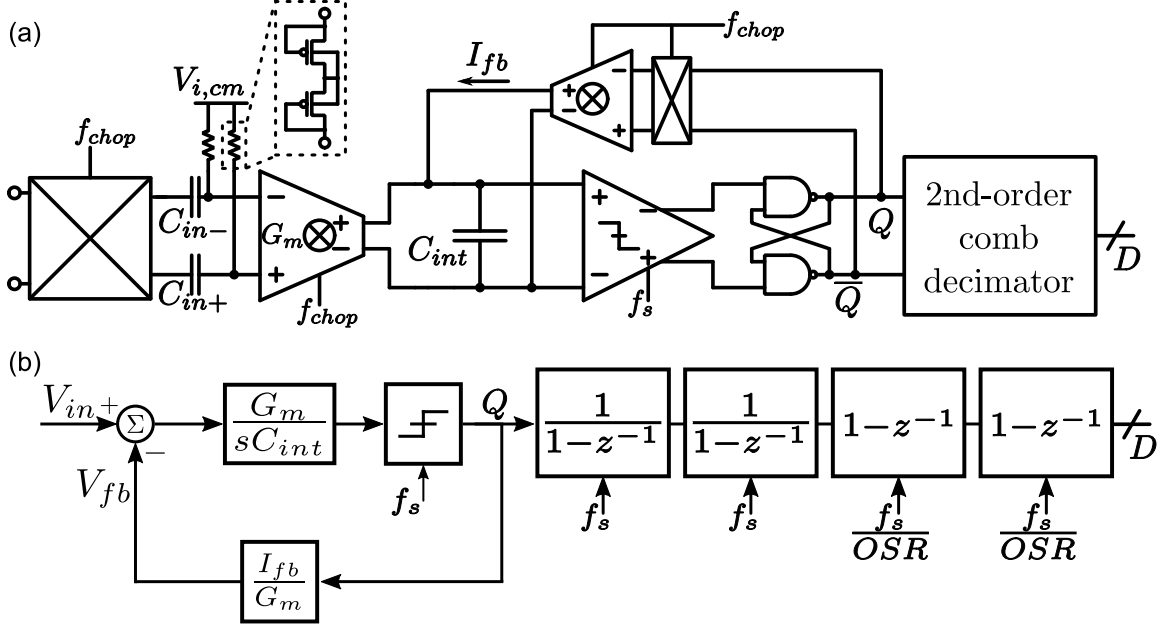


Figure 5.2: (a) Schematic of the system, consisting of a $G_m - C$ integrator, a latched comparator, a transconductor as a 1-bit DAC, and a decimation filter. Chopping switches before and within the OTA are used to reduce $1/f$ noise. (b) Block diagram representation of the system, with the DAC current referred back to the input. The second-order comb digital decimation filter implements two accumulators at the system clock f_s followed by two differentiators at the decimated clock f_s/OSR . It is realized in an alternative form for higher area and energy efficiency.

incremental ADC.²⁰⁹ Hence 10-b resolution can be obtained with just 128 rather than 1,024 OSR.

Chopping switches are placed before and within the front-end OTA to mitigate $1/f$ noise. Chopper-stabilized amplifiers, when interfaced to electrodes, must remove the large differential DC offset of the electrodes that is up-modulated to the chopping frequency.^{119,203} This design uses the method of Muller *et al*;²⁰⁵ the 1-bit output of the $\Delta\Sigma$ is filtered by a discrete-time integrator, and the output is fed back to the input through a $\Delta\Sigma$ DAC.

CHAPTER 5. A BIDIRECTIONAL NEURAL INTERFACE CHIP

The frequency response of this circuit can be tuned as follows. The low-pass cutoff frequency is set by programming the oversampling ratio, and trades off resolution for bandwidth.¹⁴⁶ The high-pass cutoff frequency is set by the servo loop.²⁰⁵ In this chip the cutoff frequency is fixed at 0.2 Hz but could be programmably tuned as described in Section 5.1.5

The chip additionally contains a four-channel neural-stimulation module and calibration circuit detailed in Chapter 4. The calibration circuit can be used to charge-balance the stimulation waveform within each channel, spatially pattern stimulation into bipolar and tripolar patterns, and calibrate current DAC coefficients within each channel.

5.1.1 OTA

A fully differential, telescopic OTA, shown in Fig. 5.3(a) is used in the $G_m - C$ integrator. Chopping switches are placed before capacitors C_{in} , to up-modulate signals of interest, and within the OTA at the sources of cascodes $M4 - M7$, such that the chopper works by switching currents.¹¹⁹ The chopping switches at the input in Fig. 5.2 are composed of complementary devices, while the switches in the OTA (Fig. 5.3(a)) are composed of either NMOS or PMOS devices. A common-mode control signal (V_{cmc}) is derived using a standard circuit consisting of two differential pairs (not shown).²¹⁰ Bias voltages V_t , V_{tcas} , V_{ncas} , and V_n are generated on-chip, using a replica-biasing scheme. To maximize noise/power efficiency of the OTA, the

CHAPTER 5. A BIDIRECTIONAL NEURAL INTERFACE CHIP

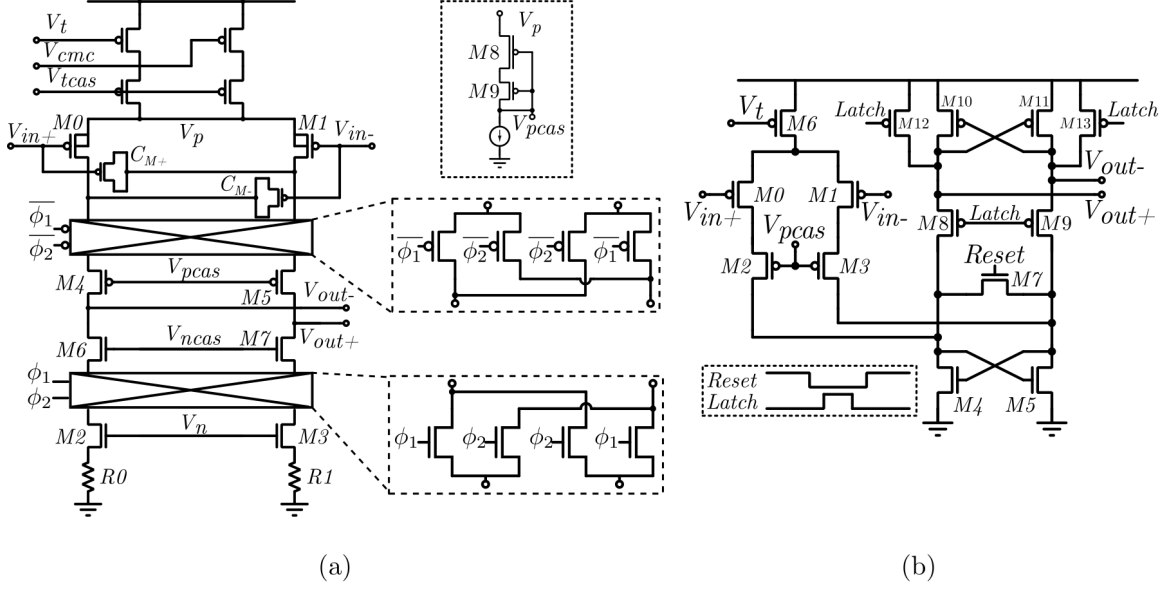


Figure 5.3: (a) Transistor-level schematics of the OTA and chopping switches. (b) Schematic and timing diagram for the latched comparator.

input pair operate in subthreshold ($W/L = 213\mu/0.95\mu$), and the NMOS load ($W/L = 95\mu/3.6\mu$) are source degenerated. All other devices are sized with large W/L to maximize headroom as their contributions to noise are negligible compared to that of the input pair and the active loads.

Capacitors C_{in+}/C_{in-} (30 pF) and pseudoresistors form high-pass filters that set the common-mode input level of the OTA. To avoid a voltage division between $C_{in,+}$ and the parasitic input capacitance of the OTA, capacitive neutralization is used, where MOS capacitors C_{M+}, C_{M-} cancel the Miller multiplied C_{gd} of the input pair.^{210, 211}

Finally, to increase CMRR, the bias voltages for M4/M5 are set as a function of the source-coupled node voltage V_p . A small current source is used to drop a voltage

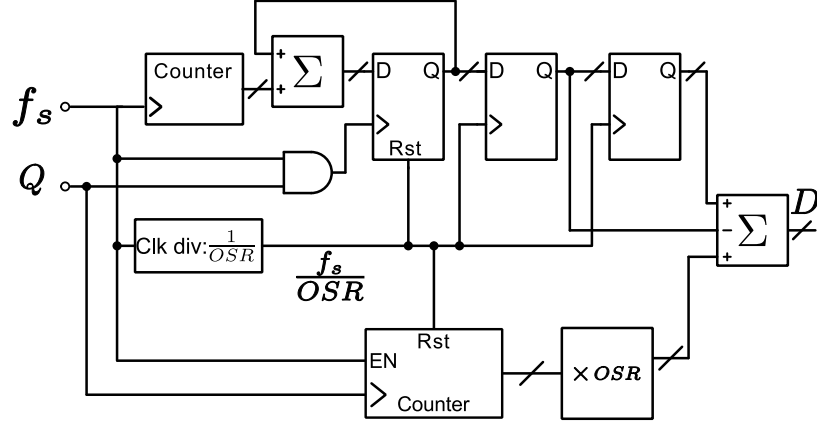
consisting of $V_{gs,4}$ and $V_{ds,0}$. This works to keep the V_{ds} across the input pair constant in the presence of a common mode input.²⁰³

5.1.2 Comparator

The latched comparator shown in Fig. 5.3(b) is based on that of Yin *et al.*,²¹² which operates in three stages: reset, amplify and latch. During reset, the differential pair sets a small voltage difference across the reset switch that tracks the difference at the input. With a falling edge on reset, both reset and latch are low, and the differential pair with a cross-coupled NMOS load amplifies the difference at the input. A rising edge on latch causes the cross-coupled inverters to amplify further and bring the outputs to the supply rails. An S-R latch is used to hold the comparator result after the comparator is reset. The cascodes hold the drain of the input pairs relatively fixed which helps to reduce kickback noise during the latch phase. The offset and noise of the comparator are noise-shaped by the $\Delta\Sigma$ loop, hence the constraints on this block are fairly relaxed, so no additional pre-amplification or offset-reduction techniques are necessary.

5.1.3 Feedback DAC

A transconductor converts the comparator outputs to a feedback current, implementing a 1-bit DAC. As illustrated in Fig. 5.2(b), the magnitude of this current can


 Figure 5.4: Decimation filter schematic.²⁰⁹

be referred back to the input through the OTA's G_m , and sets the full-scale range of the ADC. The current is set with an on-chip programmable bias generator.²¹³

5.1.4 Decimation Filter

The simplest option to decimate the output of a 1-bit $\Delta\Sigma$ is a counter, reset after OSR cycles. However, this filter is approximately OSR times less effective at suppressing out of band quantization noise compared with an ideal filter.²⁰⁹ A second order filter can be obtained by cascading an accumulator after the counter, which attenuates the out of band quantization noise to a level comparable to an ideal filter.

The impulse response of this filter can be obtained by taking the inverse z-transform of the transfer function, or graphically by convolving two rectangular pulses. This triangular impulse response can be implemented in a hardware-efficient manner as illustrated in Fig. 5.4.²⁰⁹ The positive ramp weighted sum is obtained

CHAPTER 5. A BIDIRECTIONAL NEURAL INTERFACE CHIP

with a counter and a data-gated accumulator (Fig. 5.4 top left). The negative ramp weighted sum is obtained by subtracting a positive ramp weighted sum from a rectangular weighted sum. A data-gated counter (Fig. 5.4 bottom) implements the rectangular weighted sum, and the positive ramp weighted sum is subtracted from it.

5.1.5 Mixed-Signal Servo Loop

An on-chip passive high-pass filter consisting of input capacitors and high resistance MOS pseudoresistors are used to set the common-mode input voltage. However, with chopping activated the system becomes DC-coupled, and large differential DC offsets at the electrodes can saturate the front-end. Several bioamplifier designs have used an active feedback loop to sense the DC level and cancel it at the input.^{119, 203, 214} These designs use switched-capacitor integrators in the feedback loop to extract the DC level, and subtract it at the input. Mixed-signal designs, directly digitize each channel and can therefore use digital processing and DACs to filter out the DC component.^{204, 205} Here, a DC-servo loop consists of a digital low-pass filter to extract the DC level, and a $\Delta\Sigma$ DAC subtracts that DC value from the input.

Referencing Fig 5.5, V_e represents the differential input signal at the electrodes, while V_{in} represents the differential input signal seen by the OTA in Fig. 5.3(a). The $\Delta\Sigma$ ADC encodes V_{in} in Q , a 1-bit signal representing values of $\pm A_{fs}$, where A_{fs} is half the full-scale voltage. Q is filtered by a discrete time integrator with a transfer function of shown in Fig. 5.5. Because the integrator treats Q as ± 1 , an implicit

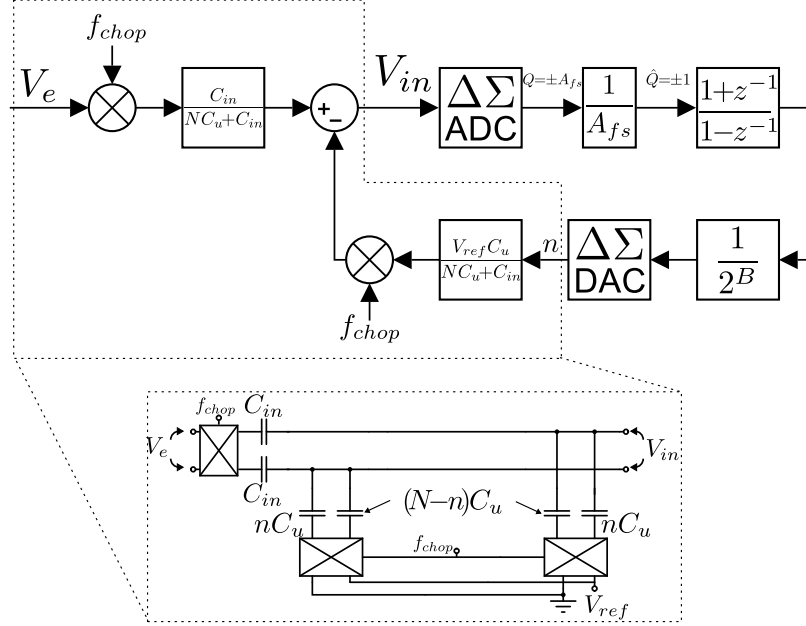


Figure 5.5: Mixed-signal servo-loop schematic. The 1-bit digital output of the ADC (Q) is low-pass filtered by a discrete-time integrator to extract the very low frequency content of the electrode signal (V_e). The low-frequency content is subtracted before the ADC through a capacitive, $\Delta\Sigma$ encoded DAC, implementing a high-pass characteristic.

scaling of $1/A_{fs}$ takes place.

The integrator output is scaled by a constant right-shift, and fed to a $\Delta\Sigma$ DAC. The DAC is a 5-bit, thermometer-coded capacitor array with $N=31$ unit capacitors C_u . The output of the $\Delta\Sigma$ (n in Fig. 5.5), switches n unit capacitors to a reference voltage V_{ref} , and $N - n$ unit capacitors to ground. Data-weighted averaging is used for mismatch error shaping.²⁰⁹ On a given cycle, with $n > 0$, capacitors $C_i - C_{i+n-1}$ are switched to V_{ref} . For the following cycle, i is incremented to $i + n$ such that a different subset of capacitors are used for the next DAC value. As a result, errors due to mismatch are translated into high-frequency noise.

CHAPTER 5. A BIDIRECTIONAL NEURAL INTERFACE CHIP

In Fig 5.5, treating the ADC and DAC as unity gains, the loop gain seen by V_{in} can be written as,

$$H(z) = K \frac{1 + z^{-1}}{1 - z^{-1}} \quad (5.1)$$

With K given by,

$$K = \frac{1}{A_{fs}} \frac{1}{2^B} \frac{V_{ref}}{2^{R-1}} \frac{NC_u}{NC_u + C_{in}} \quad (5.2)$$

Here, R is the DAC input word length. The maximum DC offset that can be canceled, $V_{os,max}$, is set by the voltage division of V_{ref} by NC_u and C_{in} . K can be rewritten as:

$$K = \frac{V_{os,max}}{A_{fs} 2^B 2^{R-1}} \quad (5.3)$$

With the loop closed:

$$H(z) = \frac{1 - z^{-1}}{1 + K + (K - 1)z^{-1}} \quad (5.4)$$

The cutoff frequency, F_c , can be found by taking $z = e^{j2\pi f/F_s}$, where F_s is the sampling rate. With $F_c \ll F_s$, and $K \ll 1$, the cutoff frequency is approximated as:

$$F_c \approx \frac{F_s}{\pi} K \quad (5.5)$$

With $F_s=128$ kHz, $V_{FS} = 5$ mV, $B = 3$, and $V_{os,max} = 30$ mV, a cutoff frequency of ≈ 0.2 Hz is obtained. Here, B is fixed as constant right shift of 3, but offers a mechanism to programmably control the cutoff frequency.

5.1.6 Stimulator

The stimulator architecture implemented on this chip was previously fabricated as an 8-channel stand-alone neurostimulator, and is described in Chapter 4. In this work,

CHAPTER 5. A BIDIRECTIONAL NEURAL INTERFACE CHIP

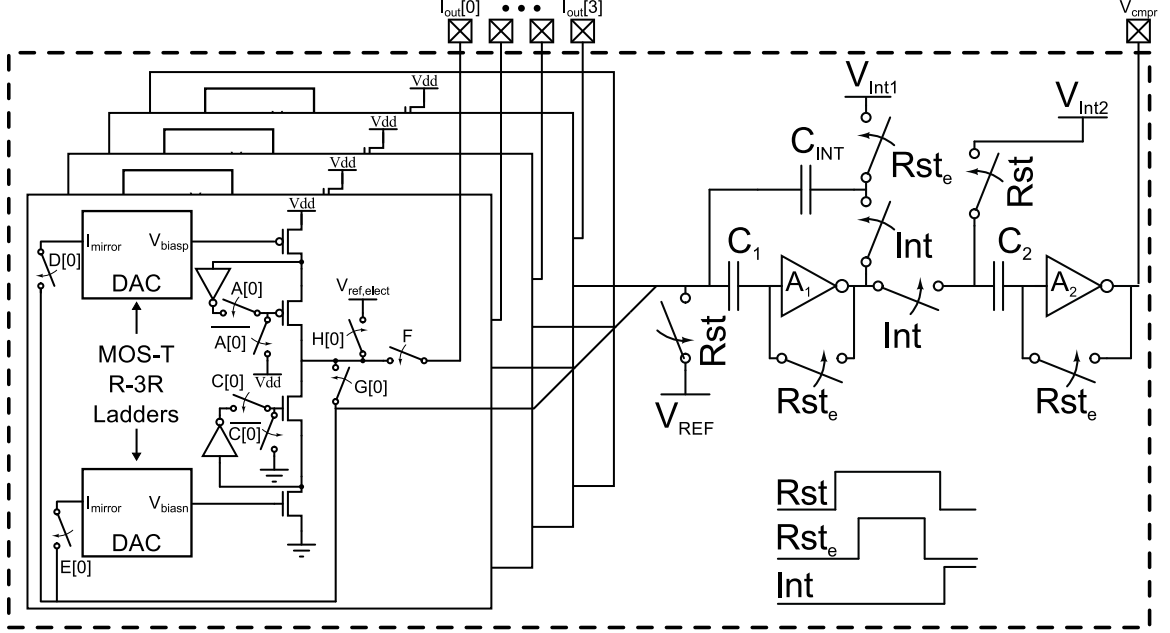


Figure 5.6: Schematic of the stimulator architecture used in this design.²⁰⁶ Each channel contains a biphasic regulated current source with independent sub-binary radix DACs. Switches A and C turn on the anodic and cathodic current sources respectively. Switches D and E mirror the DAC currents to the calibration circuit to linearize the DACs using the procedure described in Chapter 4. Switch F is used to disconnect the stimulator channel from the electrodes during calibration. Switch G routes the channel to the calibration unit, and switch H is used to short the electrode to a reference voltage ($V_{ref,elect}$) after each biphasic pulse to bleed off residual charge.

a four channel version has been integrated on chip to enable bidirectional operation on the same silicon circuit. The salient features relevant to the present bidirectional interface are illustrated in Fig. 5.6.

Each stimulation channel contains two independent, sub-binary radix, current-mode DACs that supply biases to regulated cascode current sources. The DACs are MOST R- β R ladders with $\beta > 2$.¹⁸⁹ This structure provides redundancies in the input-output relationship making it robust to mismatch. The redundancies can be removed by a digital calibration method.^{193,206} A calibration circuit is shared across

CHAPTER 5. A BIDIRECTIONAL NEURAL INTERFACE CHIP

channels and consists of an integrator and comparator. This provides an analog-to-time-to-digital conversion; the time it takes for the integrator output to trip the comparator is digitized with an external counter. The output of the comparator was routed to a pad (V_{cmpr} in Fig. 5.6.) and this timing is performed externally. Because an external device is required to program the chip and read out data, the overhead needed to perform the timing externally is negligible. With both current sources simultaneously activated, the difference between the source and sink, or residue, is routed to the calibration circuit and digitized by an off-chip counter. Either DAC can then be incremented to minimize this difference for charge balanced stimulation.

Importantly, with the calibration unit shared across channels, the residue nulling procedure described above can be applied to multiple channels at once. As a result, the stimulation currents can be matched and even ratioed to allow multipolar stimulation patterns. Multipolar stimulation can be used to shape the electric field *in-vivo* for targeted electrical stimulation. This feature is particularly important for future closed-loop neurostimulation applications, where the electrophysiological effects of stimulation can be monitored and used to update stimulation parameters autonomously.

5.1.7 Stimulation Artifact

Simultaneous stimulation while sensing can induce artifacts in the recordings. Artifacts can be the result of intrinsic cross-talk between the stimulator and record-

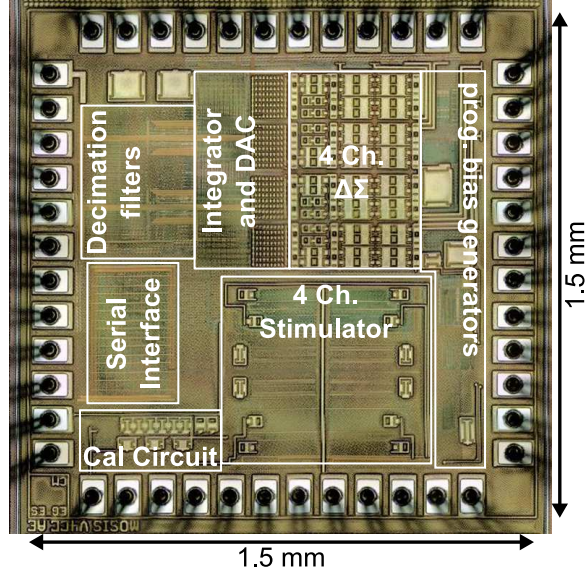


Figure 5.7: Micrograph of the fabricated circuits.

ing circuits as well as direct coupling through volume conduction *in-vivo*. Both the recording and stimulation blocks are enclosed by guard rings to minimize cross-talk through the chip substrate. Otherwise, artifact removal or mitigation circuits have not been implemented on this chip. Therefore, the hardware may not be suitable for simultaneous recording and stimulation from a single electrode array. However, for distant recording and stimulation electrodes, the artifact is predominantly a common-mode signal. In Section 5.2.1 characterizations of the intrinsic crosstalk are presented. In Chapter 6, characterization of the artifact measured *in-vivo* is presented.

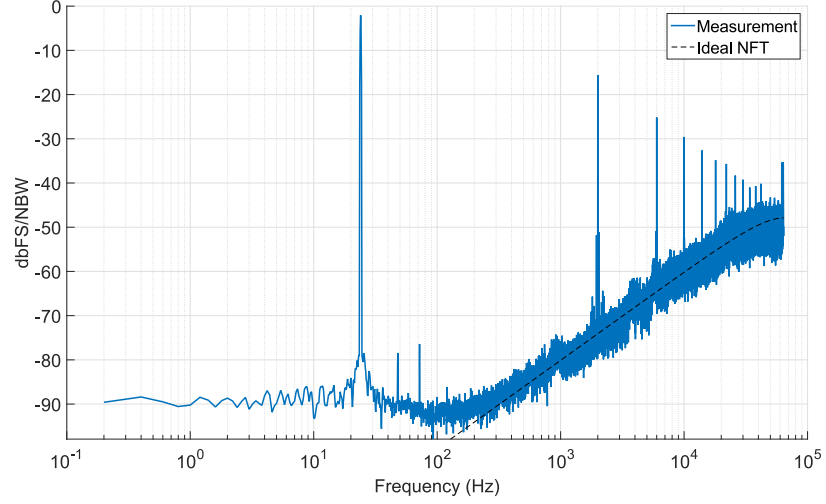


Figure 5.8: Raw output of bioADC for a 24 Hz tone, along with the ideal NTF for a first-order $\Delta\Sigma$ in black.

5.2 Measurement Results

The circuits were fabricated in a $0.18\ \mu\text{m}$ 6M1P CMOS process (Fig 5.7). The chip contains four channels; the analog circuits of Fig 5.2(a) occupy $320\ \mu\text{m} \times 580\ \mu\text{m}$, the mixed-signal servo loops occupy $380\ \mu\text{m} \times 580\ \mu\text{m}$ and the decimation filters and output shift registers occupy $220\ \mu\text{m} \times 400\ \mu\text{m}$. The input, AC-coupling capacitors as well as the integration capacitor were realized with MIM devices. The active circuits were placed underneath these components, effectively cutting the required area in half. An additional layer of metal (M4) was sacrificed to shield the MIMs and distribute power.

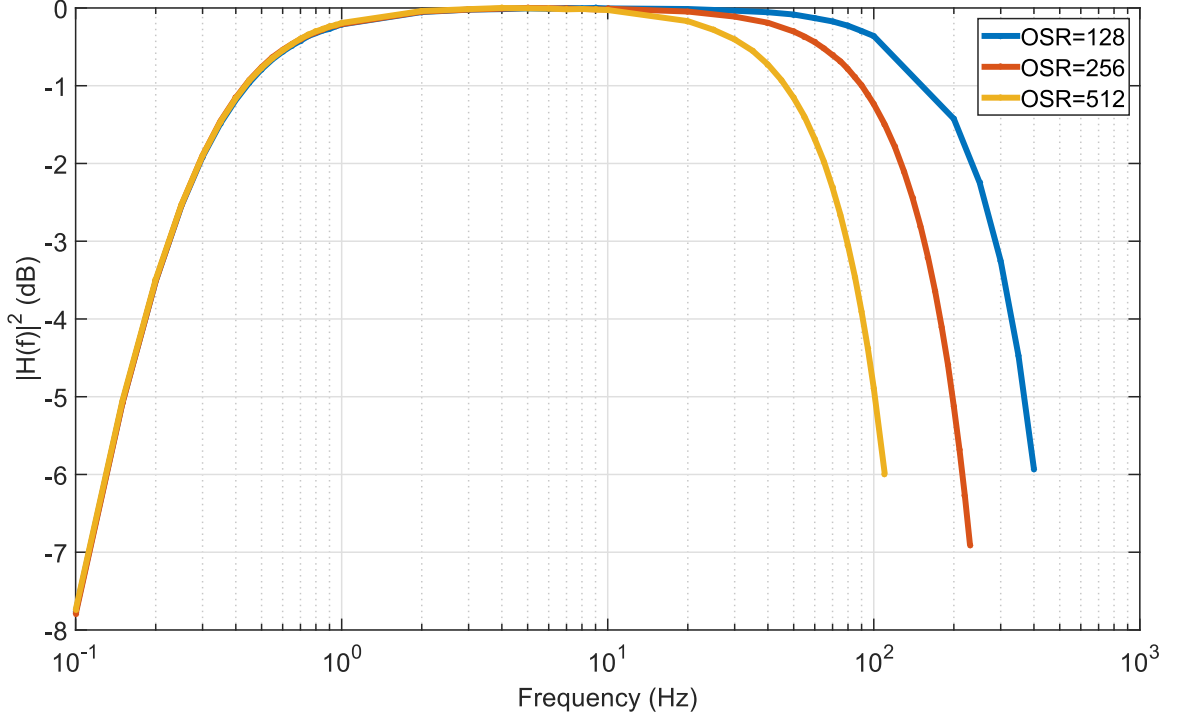


Figure 5.9: Frequency response for different settings of OSR.

5.2.1 BioADC Characterization

Fig. 5.8 shows the output spectrum of a tone test along with the theoretical NTF for a first-order $\Delta\Sigma$. At low frequencies, the resolution is noise-limited, but at high frequencies ($f > F_s/64$) the noise-shaping is clearly visible, and follows the theoretical curve very closely. Furthermore, tones at the chopping frequency and its harmonics can be seen. Note though, since the chopping frequency is a factor of the sampling frequency, the decimation filter nulls these peaks, and no aliasing of the chopper ripple is observed.

Fig. 5.9 illustrates the measured the frequency response of the circuit with the

CHAPTER 5. A BIDIRECTIONAL NEURAL INTERFACE CHIP

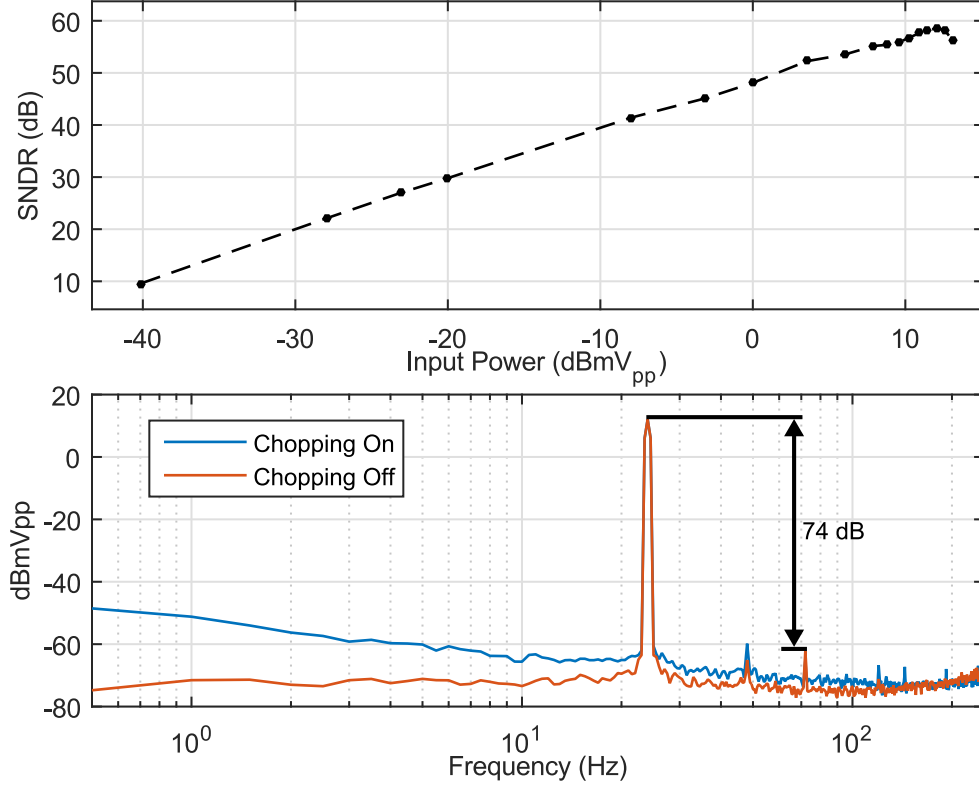


Figure 5.10: (top) Measured SNDR as a function of the input amplitude. (bottom) Output spectrum corresponding to the peak SNDR measurement ($4mV_{pp}$) with and without chopping.

OSR programmed to 128, 256, and 512. The decimation filter does provide attenuation in the passband. For the SNDR and noise measurements that follow, an equalizer was used to undo these in-band effects of the filter.

Fig. 5.10 shows the results of a tone tests for signal-to-noise-distortion-ratio (SNDR) measurements. The system clock was set to 128 kHz and the oversampling ratio set to 256, which gave a decimated data rate of 500 Hz. The input tone frequency was set to 24 Hz. Peak SNDR was measured to be 58.5 dB, at an input amplitude of 4 mV_{pp} . Fig. 5.10 illustrates that SNDR was limited by thermal noise

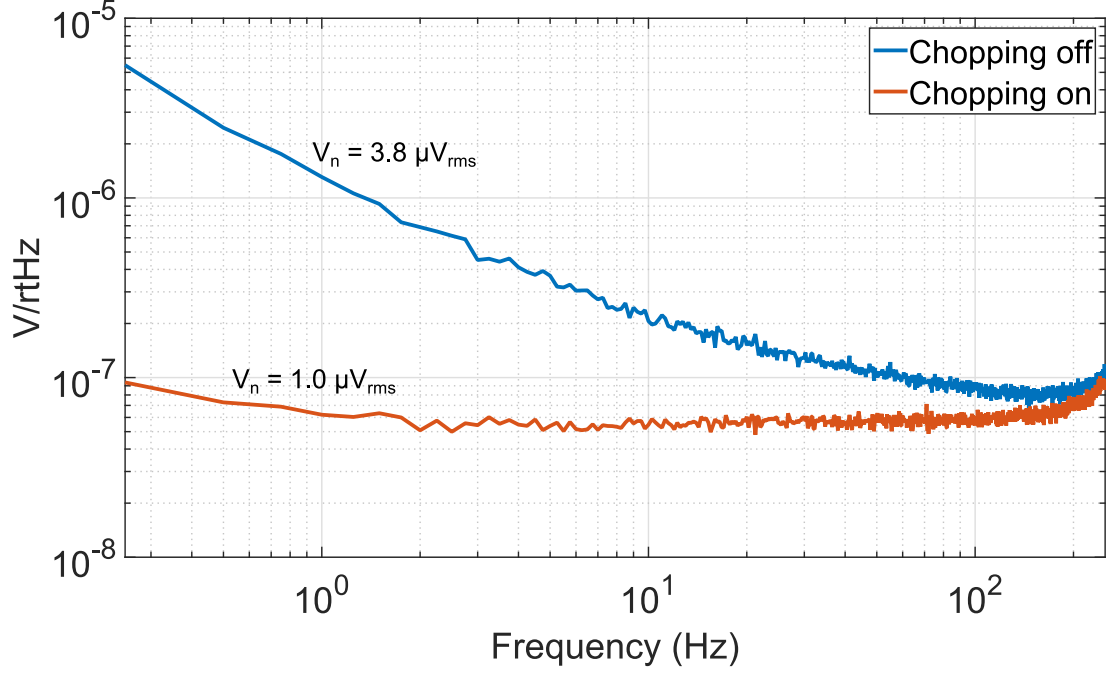


Figure 5.11: Input referred voltage noise PSD.

and power in the 3^{rd} harmonic, which is attributed to the tanh characteristic of the OTA's differential pair in subthreshold. There is no need to linearize the circuit for greater spurious-free dynamic range (SFDR) since 4 mVpp is already above the range of most biopotentials. Fig. 5.10(b) also compares the spectrum recorded with and without chopping. In addition to the reduction of $1/f$ noise, chopping mitigates even-order distortions which are due to mismatch in the differential pair.

To measure the inherent circuit noise, the inputs of all channels were shorted to ground. Fig. 5.11 shows the measured power spectral density (PSD) referred back to the input with and without chopping. Chopping significantly improves noise performance, and the dominant in-band noise source is thermal noise. The thermal

CHAPTER 5. A BIDIRECTIONAL NEURAL INTERFACE CHIP

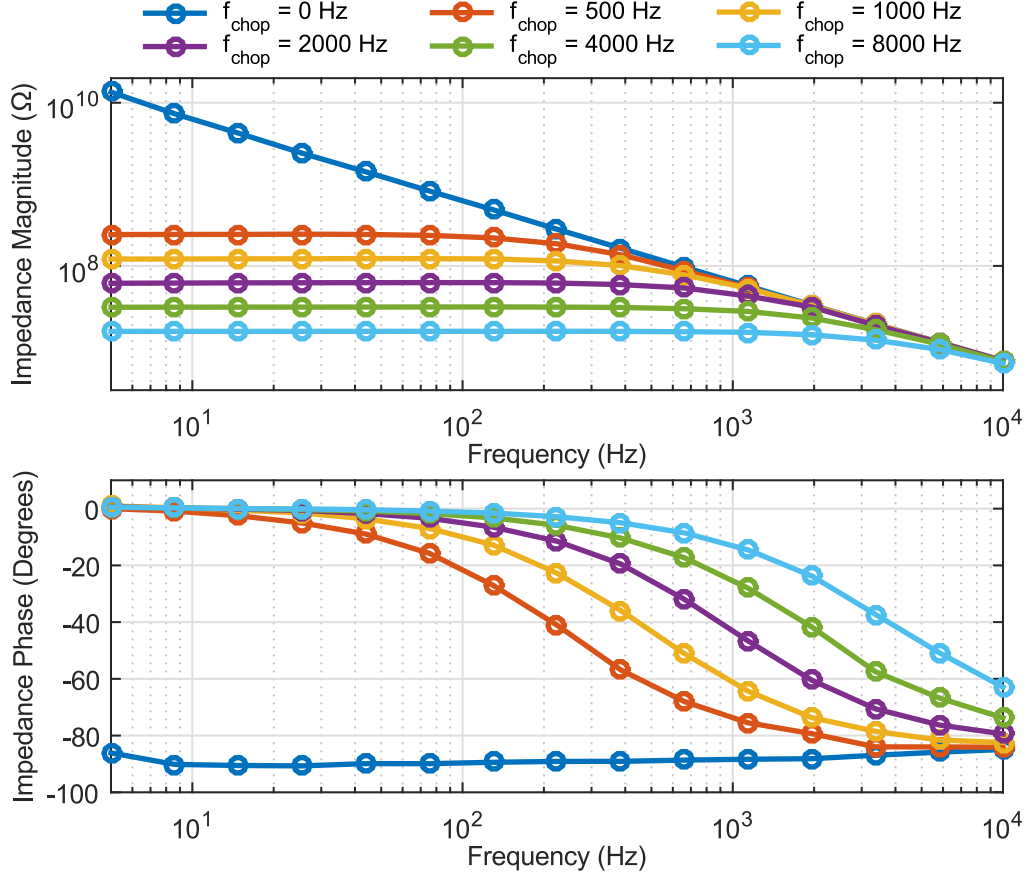


Figure 5.12: BioADC differential input impedance across chopper frequencies.

noise level appears approximately at $60 \text{ nV}/\sqrt{\text{Hz}}$. Though it appears from Fig. 5.11 that the $1/f$ noise corner is below 1 Hz, this is not the case, as the HPF attenuates signals below 1 Hz. At higher frequencies, the $\Delta\Sigma$ quantization noise can be seen to rise above the thermal noise floor. This includes the quantization noise from the ADC and DAC. Integrating under the curve from 0.25 Hz to 250 Hz yields a total input referred noise of $1.0 \mu V_{rms}$.

The differential input impedance of the bioADC was measured for chopping fre-

CHAPTER 5. A BIDIRECTIONAL NEURAL INTERFACE CHIP

Table 5.1: Input impedance magnitude at 76 Hz across chopper frequencies.

Chopping Frequency (Hz)	0	500	1000	2000	4000	8000
Input Impedance ($M\Omega$)	827	237	123	62	31	16

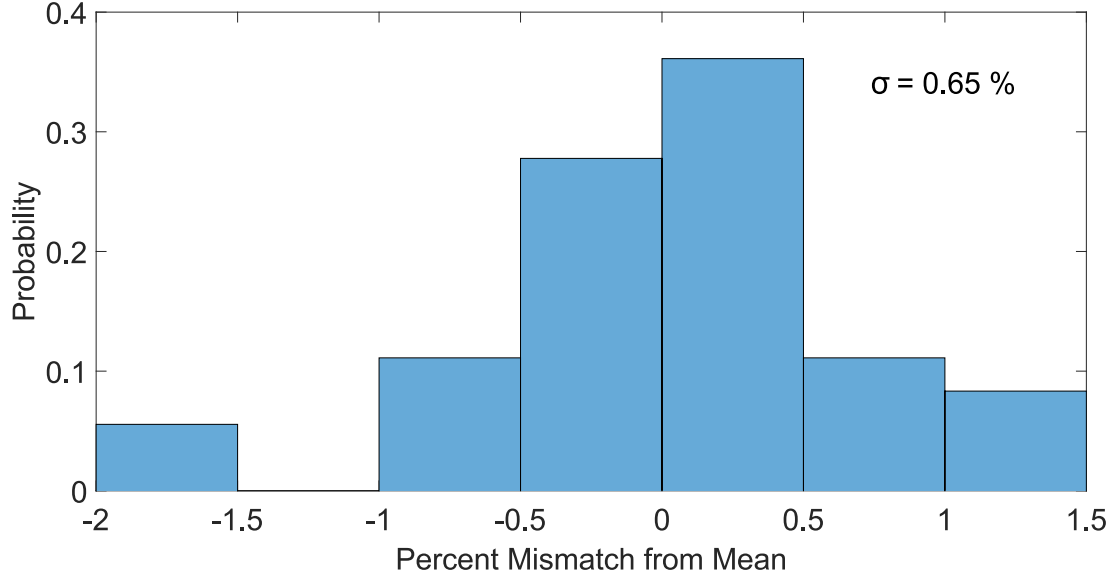


Figure 5.13: Percent variation in the gain across channels. Data accumulated from 9 chips for a total of 36 measurements. Data from each chip was normalized to the chip average.

quencies ranging from 500 Hz - 8 kHz. Fig. 5.12 shows the magnitude and phase plots of the input impedance as a function of frequency and Table 5.1 lists the measurement magnitude results at 76 Hz.

Common-mode rejection of the bioADC was measured without chopper stabilization and with chopping at 2 kHz. The measurement was made by applying a 90 mV_{pp} 50 Hz signal to both inputs. Without chopping, CMRR was measured to be 77 dB and increased to 97 dB with chopping enabled.

The use of an open-loop G_m stage leads to mismatch across channels. This mis-

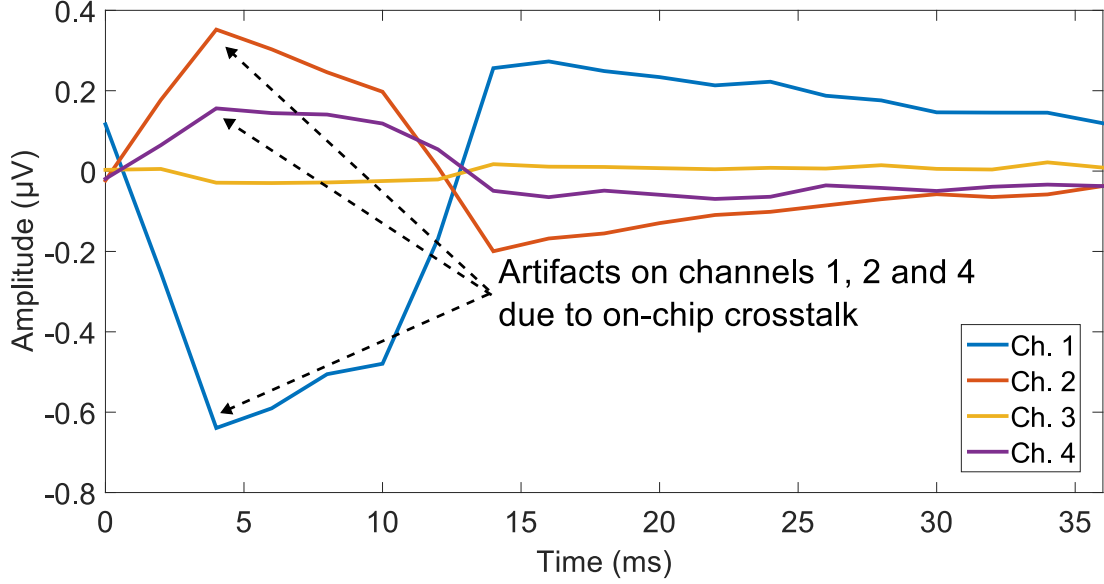


Figure 5.14: Crosstalk between the recording and stimulation blocks. Biphasic pulses with 10 ms cathodic-first pulse widths were applied to a resistive load (4.7 k Ω) on all four stimulator channels with the recording front-ends tied to ground. Recordings were time aligned to the onset of stimulation pulses ($t=0$) and averaged, extracting artifacts on channels 1, 2 and 4.

match was characterized by applying a 2.5 mV_{pp} tone to all channels and comparing the peak heights in amplitude spectra. This parameter was measured in the four channels across nine chips. Within chip variation was bounded by $\pm 2\%$, and a histogram of the across channel variation, normalized to the average for each chip is illustrated in Fig 5.13.

Crosstalk between the bioADC and the stimulator blocks was measured by tying the front-end inputs to ground while pulsing the fullscale current through a dummy load (4.7 k Ω) on all channels with a pulse width of 10 ms and a 25 Hz frequency. Recordings from each channel were then time aligned to the onset of each stimulation pulse and averaged across 7500 pulses to extract any measurable crosstalk. Fig 5.14

illustrates the waveforms after averaging. Channels 1, 2 and 4 show a detectable artifacts, but the worst case is less than $1 \mu V_{pp}$.

5.2.2 Power Consumption and Noise Efficiency

The average static current consumption of the analog components in Fig 5.2(a) was $1.41 \mu A$ with the following breakdown: $1.05 \mu A$ for the OTA (including CMFB and V_{pcas} generation), $30 nA$ for the feedback transconductor, and $330 nA$ for the comparator. The comparator, S-R latch, and digital buffers (not shown) also consumed a small amount of dynamic power. During operation, the analog components consumed $1.54 \mu A$ on average. The decimation filters, discrete-time integrator and $\Delta\Sigma$ consume comparable amounts of power. Each channel drew an additional $2.13 \mu A$ from the digital supply to power the decimation filters, integrator, $\Delta\Sigma$ DAC, and for clock distribution. Both analog and digital circuits were powered from a $1.5 V$ supply, yielding a total power consumption of $5.5 \mu W$.

To quantify the design's power and noise performance, we can calculate the noise efficiency factor (NEF) and the power efficiency factor (PEF). Furthermore, we can consider separately the front-end amplifier and the system as a whole. By considering only the power consumed by the front-end OTA ($1.05 \mu A$ at $1.5 V$), and taking the bandwidth to be equal to the Nyquist rate, we calculate an NEF of 2.5, and a PEF of 9.4. For the total system, with a current draw of $3.67 \mu A$, and a $1.5 V$ supply voltage, the NEF and PEF are 4.7 and 33 respectively. The system level NEF is comparable

to another state-of-the-art design,²⁰⁵ while the PEF suffers due to the relatively high supply voltage of 1.5 V.

5.2.3 *In-vivo* Measurements

Two sets of measurements were performed *in-vivo* to validate the performance of the circuits in a biomedical setting. All surgical procedures were approved by the Johns Hopkins Animal Care and Use Committee. In the first experiment, stainless-steel screw electrodes were implanted in the skull over the somatosensory cortex of a rat, and an additional screw was implanted over the occipital region to serve as a reference. Simultaneous intracranial EEG (iEEG) recordings were made with a commercial, bench-top neurophysiology system (Tucker-Davis Technologies, Alachua, FL), as well as the proposed circuits (Fig. 5.15(a)). Fig. 5.15(b) shows two 5-second clips of iEEG from a rat under isoflurane anesthesia. The signals obtained with the bioADC (red) were overlaid on the recordings from the reference system (blue). When deeply anesthetized, the iEEG displays a prominent burst-suppression waveform in which periods of quiescence are punctuated by high amplitude bursts of activity;²¹⁵ this pattern is observed in Fig. 5.15(b)(top). However, under light sedation, the iEEG becomes continuous and of lower amplitude. Fig. 5.15(c) compares the spectrograms recorded from the two systems. Power in each frequency bin was normalized to the median power over the entire recording.

We used the chip in a second experiment to demonstrate simultaneous sensing and

CHAPTER 5. A BIDIRECTIONAL NEURAL INTERFACE CHIP

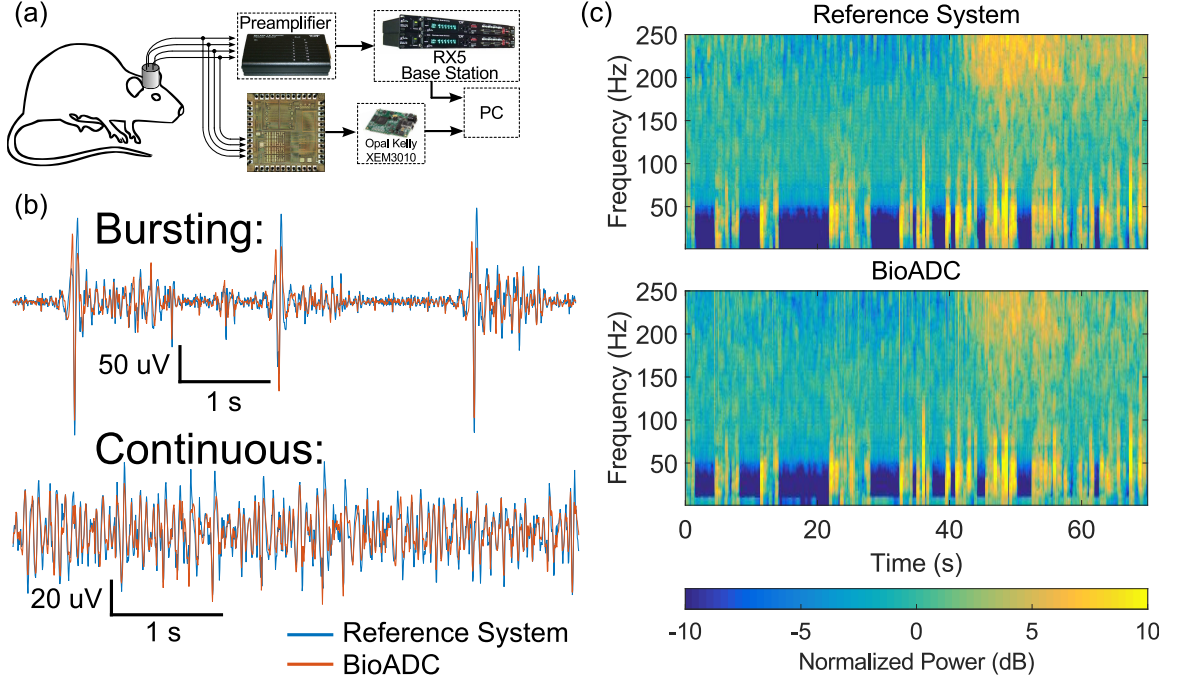


Figure 5.15: (a) Setup for in-vivo validation of the proposed circuits. A commercial electrophysiology workstation and the fabricated circuits were connected to screw electrodes implanted in a rat's skull, and the electroencephalogram was recorded while the rat was under anesthesia. (b) Comparison of time domain EEG. Burst suppression patterns (top) were recorded while the rat was heavily sedated. Continuous EEG was recorded during light sedation. (c) Frequency domain comparison.

stimulation capabilities. Illustrated in Fig. 5.16(a), we simultaneously stimulated the vagus nerve to artificially increase the parasympathetic input to the heart, and measured the resulting effects on heart rate by measuring the electrocardiogram. A male Wistar rat was anesthetized with 2% isoflurane in a 50:50 N₂:O₂ mixture through a nosecone. A ventral incision was made in the neck, muscles were retracted and the left carotid sheath was exposed. Then, the left cervical vagus nerve was carefully dissected from the carotid sheath. Fig. 5.16(a) illustrates the experimental setup. Electrical contact was made with the vagus nerve using a stainless steel, bipolar

CHAPTER 5. A BIDIRECTIONAL NEURAL INTERFACE CHIP

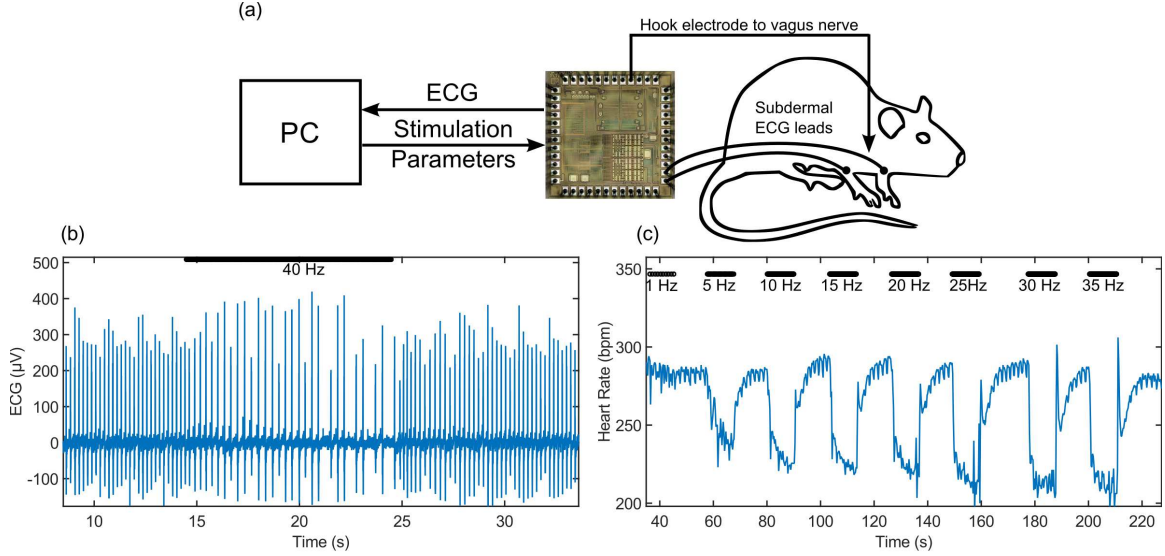


Figure 5.16: (a) Experimental setup to test the recording and stimulation capabilities simultaneously. A hook electrode was interfaced to the vagus nerve of an anesthetized rat and two subdermal needle electrodes were inserted at the left and right forepaws to measure resulting ECG changes. (b) Recorded ECG during vagus nerve stimulation (VNS). Black bar corresponds to the onset of VNS at a 40 Hz frequency. (c) Measured heart rate, extracted from recorded ECG, over time as VNS frequency was steadily increased. Over several trials we increased the stimulation frequency from 1 Hz to 35 Hz. The onset of each trial is indicated by the presence of a black bar, with the corresponding stimulation frequency labeled. Increases in stimulation frequency have a stronger effect on reducing heart rate as expected.²¹⁶

hook electrode. A single stimulator channel was connected to one of the hooks, and the other hook was connected to 1.5 V to bias the rodent and for the stimulation current's return path. The electrode was made from 250 μm stainless steel wire, with a 1 mm hook diameter, and 0.8 mm spacing (FHC, Bowdoinham ME), and had an impedance of 2 $\text{k}\Omega$ at 1 kHz. Biphasic pulse trains (cathodic first) were delivered through the electrodes with the following parameters: 250 μA amplitude, 50 μs pulse width, and 10 s pulse train duration. The electrocardiogram (ECG) was measured differentially across the two forepaws using a single bioADC channel.

Figure 5.16(b) shows measured ECG before, during and after a 40 Hz stimulation train delivered to the vagus nerve. The heart rate responds almost immediately at the onset (black bar) and offset of stimulation. Increasing the frequency of VNS progressively slows heart rate.²¹⁶ Fig. 5.16(c) shows the calculated heart rate versus time as VNS frequency was increased. Each black bar indicates the onset of a 10 second train of stimulation, and annotated below the bar is the stimulation frequency. Stimulation frequency was stepped up in 5 Hz increments from 5 Hz to 35 Hz; at 30 Hz the effect saturated at an approximately 30% decrease in heart rate.

5.3 Comparisons and Conclusion

We have presented a low-power, low-noise, biopotential acquisition system with integrated stimulator²⁰⁶ suitable for closed-loop electrocortical neuromodulation systems. Table 5.2 summarizes the recording front-end specifications of the reported circuits and compares the results with state-of-the-art designs. For fair comparisons across designs we use a “system-level” NEF that considers the current consumption of the entire recording chain including ADC. This design achieves improvement in system-level NEF compared with prior-art. The PEF is substantially higher here than the design of Muller and colleagues²⁰⁵ due to our relatively high supply voltage of 1.5 V compared with 0.5 V.

We also propose an additional figure of merit (FoM) for bioADC systems based

CHAPTER 5. A BIDIRECTIONAL NEURAL INTERFACE CHIP

on a traditional figure of merit in ADCs.

$$\text{FoM}_{\text{bioADC}} = \frac{\text{Power}}{F_s \cdot 2^{\text{ENOB}'}} \quad (5.6)$$

$$\text{ENOB}' = \frac{20 \cdot \log_{10}\left(\frac{A_{fs}/\sqrt{2}}{V_{n,rms}}\right) - 1.76}{6.02} \quad (5.7)$$

The front-end amplifiers and back-end ADCs of many biopotential acquisition systems are characterized separately. This FoM allows fair comparisons between systems such as that proposed here and more traditional systems by taking into account the effect of front-end noise and gain on the effective SNR in practice.

Note that though the bioADC presented here obtains an ENOB of 9 bits, this is with a dynamic range of 5 mV, which is much larger than the dynamic range of most biopotential signals. Therefore, the ENOB for signals of interest is lower. For example, Fig. 5.10 illustrates that for a signal range of 1 mV_{pp} , an ENOB of 7.7 is obtained. However, the high dynamic range has significant value. For example, in practical EEG/ECOG systems on awake behaving subjects, movement artifacts can be very large. Therefore, the increased dynamic range gives a degree safety for artifactual signals to prevent saturation

SAR ADCs are typically the best choice for energy efficient analog-to-digital conversion. The work in Table 5.2 that achieves the best (lowest) FoM is a SAR ADC. In this case the FoM is driven low by the relatively low power despite very high sampling frequency.¹¹⁴ However, SAR ADCs are prone to aliasing distortion in the presence of high-frequency noise. This is of particular concern in bidirectional sys-

CHAPTER 5. A BIDIRECTIONAL NEURAL INTERFACE CHIP

tems, as high frequency stimulation artifacts alias into the frequency bands relevant to biopotential sensing.¹¹⁰ The oversampling in $\Delta\Sigma$ ADCs, as well as the inherent anti-aliasing properties of the continuous-time (CT) integrator make CT- $\Delta\Sigma$ ADCs particularly suited for this application. The integrated second-order decimator offers substantial improvement in resolution without the area and power expense of second-order noise shaping. While VCO based ADCs also provide inherent anti-aliasing, $\Delta\Sigma$ architectures offer enhanced linearity.

The proposed circuits were designed specifically for EEG/ECoG recording as demonstrated in Fig. 5.15. The major limitation in using the proposed circuit for spike recording is the power required to increase the sampling rate to one suitable to acquire action potentials. Typical commercial hardware sample at >20 kHz, and to achieve this sampling rate at the current 256 OSR, would require a 5.12 MHz clock rate. In the current implementation this would consume an unsuitable amount of power from the digital circuits.

The performance of the proposed circuits has benefited greatly from process scaling. Previous designs^{146,207} were fabricated in a $0.5\ \mu\text{m}$ process, so the inclusion of the second order filter was prohibitive in terms of area. Implementation in a 180 nm processes permitted integration of the second-order decimation filter in-line with the CT- $\Delta\Sigma$. This further permitted reduction in the sampling clock frequency, which brought down power consumption proportionally.

Further, a major challenge with integrating chopper stabilization into a biopo-

CHAPTER 5. A BIDIRECTIONAL NEURAL INTERFACE CHIP

tential amplifier is the electrode DC differential offset which is addressed with a well-known and commonly used servo-loop technique. The single bit output of the CT- $\Delta\Sigma$ makes the mixed-signal approach²⁰⁵ attractive due to both the challenge of filtering the noise shaped signal in the analog domain and the simplicity of filtering a single-bit signal in the digital domain.

Interestingly, digital power consumption dominates total system power consumption in this design. This could be addressed in two ways. First, two power domains could be utilized, a 1.5 V supply for the analog circuits and a <1 V supply for the digital circuits; minimal overhead in the form of level shifters would be the only requirement. Alternatively, further performance and energy efficiency improvements can be obtained by migrating the design to state-of-the-art 65nm technology.

Table 5.2: Comparison of this work with prior art

Parameter	This Work	205	114	207	146	203
Year	2016	2015	2013	2010	2009	2008
Technology	180nm	65nm	130nm	0.5 μm	0.5 μm	0.5 μm
Power/ch. (signal cond. + ADC) (μW)	5.5	2.3	10	20	72.6	14.2
Max Offset (mV)	± 30	± 50	AC-coupled	AC-coupled	AC-coupled	± 45
Input Referred Noise (μV_{rms})	1.0	1.29	5.1	2.65	1.65	0.59
Bandwidth (Hz)	0.25-250	1 - 500	1 - 5k	1-1024	0.5 - 140	0.5 - 100
NEF (system level)	4.67	4.77	8.0	7.95	79.5	4.95
PEF (system level)	33	11	77	209	629	73.6
CMRR (dB)	97	88	75	-	76	128
ADC Architecture	$\Delta\Sigma$	VCO	SAR	$\Delta\Sigma$	$\Delta\Sigma$	SAR
Sampling Rate per ch. (Hz)	500	1k	28k	512	500	1k
Resolution (ENOB)	16 (9.4)	15 (-)	8 (7.6)	10 (9.5)	10 (8.8)	11 (10.5)
SNDR (dB)	58.5	-	47.5 ^{α}	59	55	64.9 ^{α}
SFDR (dB)	74	52	51	59	60	-
bioADC FoM (pJ/conv)	7.6	10.3	5.5	91.7	444	38.6
Stim Channels	4	-	64	-	-	-
Stim Supply Voltage	5	-	3.3	-	-	-
Max Current (mA)	0.25	-	1.2	-	-	-

 ^{α} measurement for ADC alone

Chapter 6

Closed-loop Control of Cardiac Rhythm with a Custom Integrated Circuit

Autonomic nervous system dysfunction is concomitant with cardiovascular disorders such as heart failure, hypertension and arrhythmias.^{217,218} Beta-adrenergic blockers (β -blockers) are antagonists for epinephrine, and are prescribed for these disorders as they block the activity of the sympathetic nervous system.²¹⁹ In heart failure patients it has been hypothesized that increasing parasympathetic activity may also offer benefit in addition to the reduction of sympathetic input inherent to β -blockers.²¹⁹

However, recent clinical trial disappointments have underscored the need to better

CHAPTER 6. CLOSED-LOOP CONTROL OF CARDIAC RHYTHM

understand the mechanisms of action of neuromodulation therapies.^{159,220} Research grade implantable devices for small animal models can greatly help in that regard. The size, power, and noise constraints on implantable biomedical devices are severe, so it is often necessary to use application specific integrated circuits (ASICs) to meet required specifications. This chapter details the development of a closed-loop neurocardiac interface using the custom very-large-scale integration (VLSI) chip from Chapter 5 to record and stimulate bioelectric activity.

Quantitative understanding of the effect of vagal activity on the heart has been well developed over the past century.^{216,221,222} However, previous demonstrations of closed-loop control of this system have used standard benchtop instrumentation.^{223,224} Here, all recording and stimulation circuits are contained within a single 1.5 mm \times 1.5 mm integrated circuit (IC). Signal processing is performed on a PC, but the algorithms used are simple enough to implement on an FPGA or synthesize in a next-generation ASIC.

6.1 System Design

Fig. 6.1 illustrates a block diagram of the system designed and implemented. The bidirectional neural interface chip (BNIC) described in Chapter 5 records the electrocardiogram subdermally from the chest and streams data to an FPGA development board (XEM3010, Opal Kelly). The FPGA packages and transmits data to

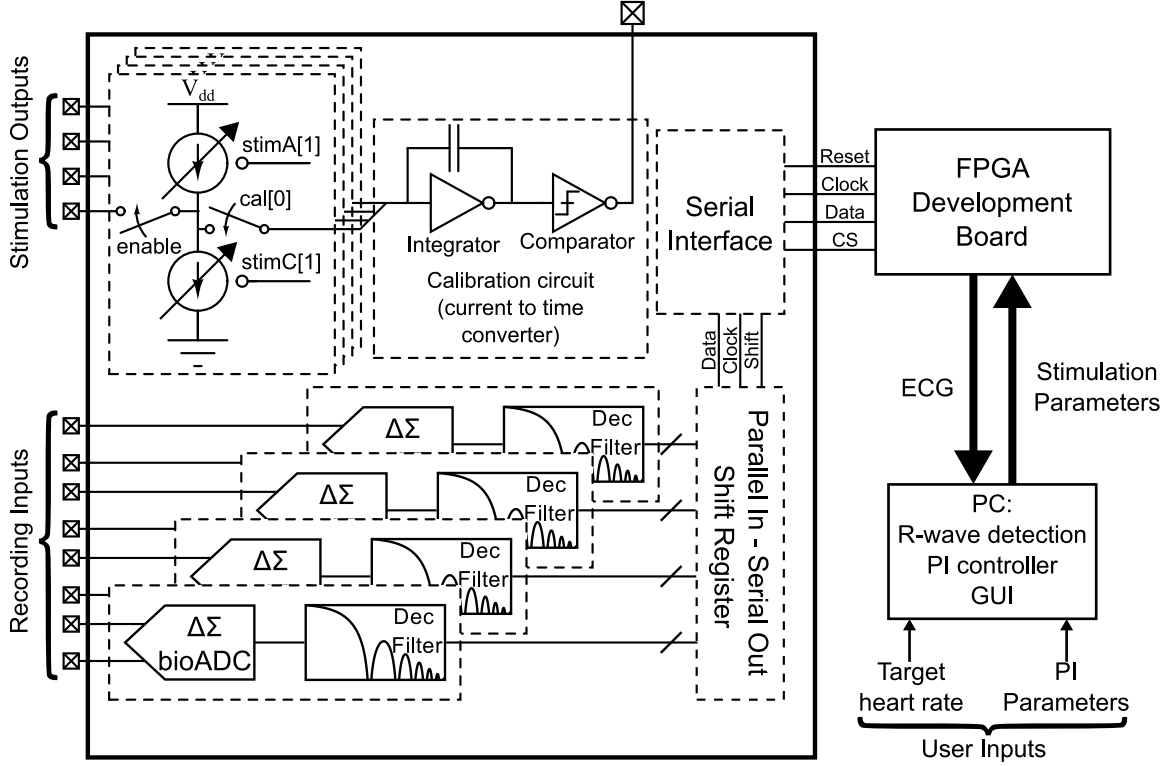


Figure 6.1: System level diagram of the for the neuromodulation system. A custom integrated circuit containing recording and stimulation circuits acquires and digitizes ECG, and delivers constant-current stimulation to the vagus nerve. An FPGA streams data from the ASIC and delivers parameters, and communicates with a PC over USB. Finally a PC calculates heart rate through R-wave detection, and updates stimulation frequency through a PI controller.

a personal computer (PC) via a USB interface and sends stimulation commands to the BNIC that control stimulation amplitude, pulse width, frequency and duration. A PC runs a graphical user interface (GUI) written with LabWindows CVI (National Instruments, Austin, TX), and allows the experimenter to input a “target” heart rate. An R-wave detection algorithm is used to calculate heart rate in real-time, and a proportional-plus-integral (PI) controller modulates vagus nerve stimulation (VNS) frequency. Stimulation parameters are sent back to the FPGA which updates

stimulation frequency.

6.1.1 Heart Rate Detection Algorithm

Calculation of heart rate was performed with a simple algorithm that detects the R-wave of the ECG through crossings of an adaptive threshold. The threshold is set by shifting ECG data into a 4-second long window and taking the threshold to be 40% of the maximum.²²⁵ As the R-wave crosses through this threshold, the time between the current crossing and previous crossing gives the R-R interval. However, if the current time exceeds that of the previously calculated R-R interval, the heart rate estimate is decremented. This is to avoid sudden drops in our estimate of heart rate, and allows the system to respond to the slowing of the heart, without waiting for the next R-wave, avoiding overstimulating the vagus. Finally, the instantaneous heart rate estimates produced by this algorithm were smoothed using a moving average filter.

6.1.2 PI Controller

The GUI allows the experimenter to set a target heart rate. Upon activation of the controller, an error signal is computed as the difference between the target and the calculated heart rate. The stimulation frequency at time t is set as

$$f[t] = K_p e[t] + K_i \sum_{t'=0}^t e[t'] \quad (6.1)$$

CHAPTER 6. CLOSED-LOOP CONTROL OF CARDIAC RHYTHM

Two heuristic modifications were made to this controller. First, in pilot experiments it was found that stimulation above 40 Hz tended to cause arrhythmias. Secondly, efforts here were only made to lower heart rate from a baseline value. Therefore, the output of Eqn. 6.1 was constrained to be positive and less than 40. Thus, the effective stimulation frequency can be written as

$$f[t] = \max \left(0, \min \left(K_p e[t] + K_i \sum_{t'=0}^t e[t'], 40 \right) \right) \quad (6.2)$$

Lastly, selection of gain coefficients K_p and K_i is non-trivial. One group has used a computational model of the cardiovascular system *in-silico* to find the optimal parameters that minimized a cost function consisting of terms proportional to the mean squared error, overshoot, and rise time.²²⁴ A heuristic approach was taken here, resulting in $K_p = 0.05$ and $K_i = 1\text{e-}3$.

6.2 Experimental Setup

The following experiment was carried out on male Wistar rats under a protocol approved by the Johns Hopkins Animal Care and Use Committee. Anesthesia was given with 2% isoflurane in a 50:50 N₂:O₂ mixture through a nosecone. A ventral incision was made in the neck, muscles were retracted and the left carotid sheath was exposed. Then, the left cervical vagus nerve was carefully dissected from the carotid sheath.

Electrical contact was made with the vagus nerve with a tripolar micro-cuff elec-

CHAPTER 6. CLOSED-LOOP CONTROL OF CARDIAC RHYTHM

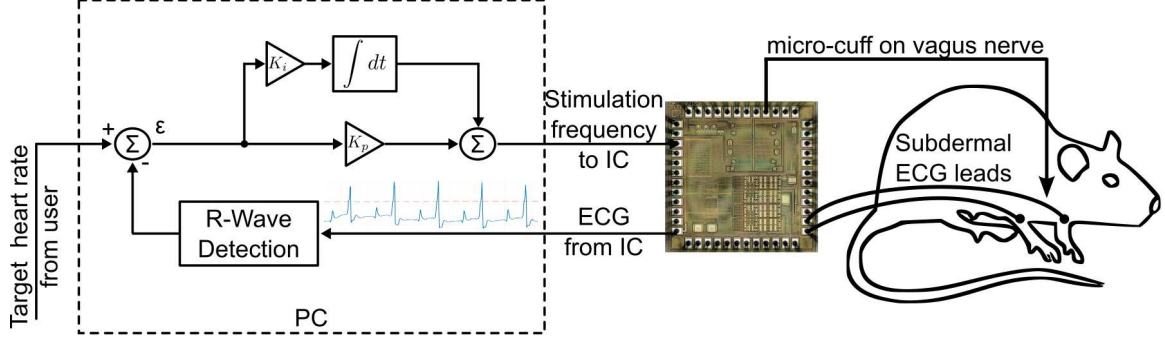


Figure 6.2: Experimental setup for the closed-loop vagus nerve stimulation experiments. A tripolar micro-cuff electrode was placed on the vagus nerve through a ventral incision in the neck. ECG was recorded differentially from two subdermal needle electrodes at the right forepaw (RF) and left forepaw (LF), a third ground electrode (not shown) was placed at the right hindpaw.

trode (Microprobes, Gaithersburg, MD). The cuff consisted of three $50\ \mu\text{m}$ platinum/iridium contacts spaced $0.5\ \text{mm}$ apart, embedded in a $300\ \mu\text{m}$ diameter silicone rubber tubing. Biphasic pulse trains (anodic first) were delivered through the electrodes with the following parameters: $110\ \mu\text{A}$ amplitude, $225\ \mu\text{s}$ pulse width. Two of the distally located electrodes were stimulated with adjacent stimulator channels, while the third, proximal electrode was used for the currents return path.

For ECG recording, stainless steel needle electrodes were inserted subdermally in the left and right forepaws (LF and RF respectively), and a ground electrode was inserted in the right hindpaw (RH). Recordings were made differentially between RF and LF, analogous to Lead I in a standard clinical ECG. Fig. 6.2 illustrates electrode locations.

We attempted four levels of control corresponding to 5% - 25% decreases in heart rate from baseline, in 5% steps. In each trial, we recorded one minute of baseline data,

CHAPTER 6. CLOSED-LOOP CONTROL OF CARDIAC RHYTHM

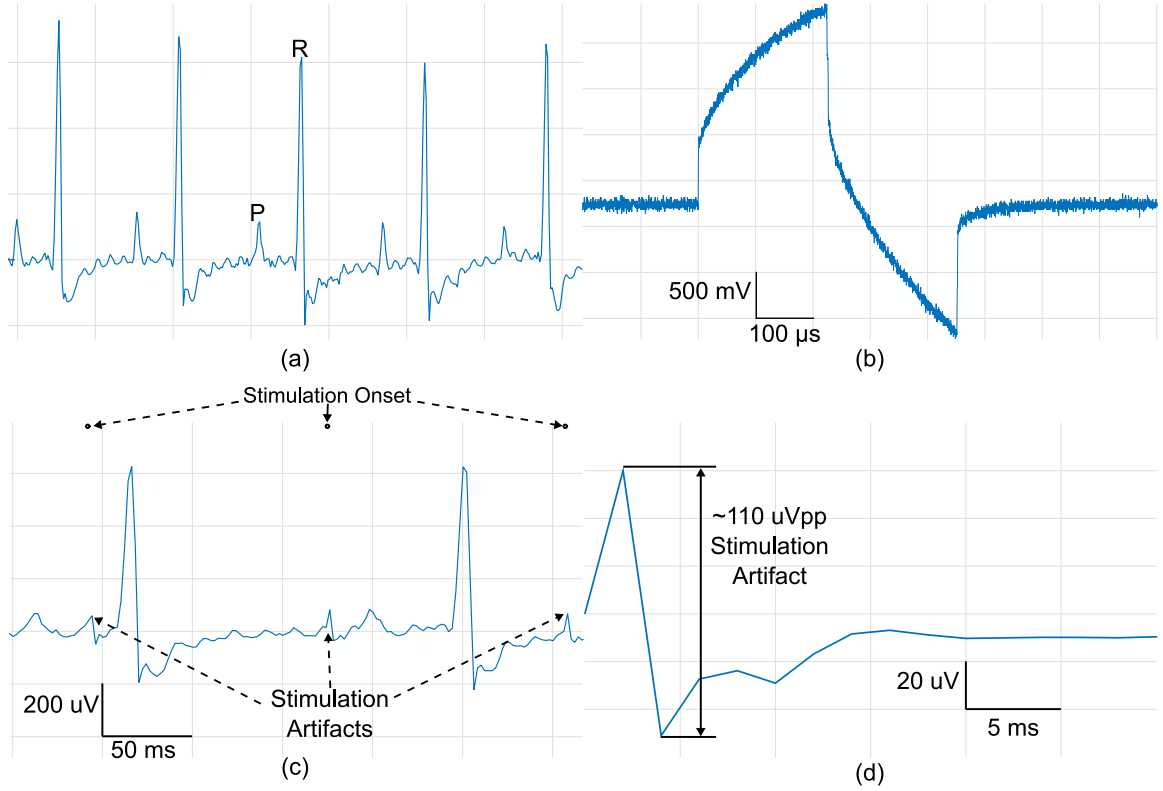


Figure 6.3: (a) Raw ECG acquired with the BNIC during a baseline period. (b) Potential recorded by an oscilloscope from the stimulating micro-cuff electrode during a stimulation pulse. The electrode potential was buffered through a MOS-input amplifier to avoid loading the stimulator.

then activated the PI controller. Once the measured heart rate hit the target, the system was allowed to run for an additional three minutes (this resulted in non-equal trial durations across the different targets), after which stimulation was turned off and heart rate was allowed to return to baseline. In an additional trial, we set the target to a 10% decrease from baseline, and allowed the system to run for 20 minutes.

6.3 Results

Fig. 6.3(a) shows representative ECG captured during baseline; the P and R waves are clearly evident. Fig. 6.3(b), depicts the time-domain potential across one of the micro-cuff electrodes during stimulation, exhibiting both a resistive (faradaic) and capacitive component of the electrode impedance. Due to the relatively low level of stimulation current ($110 \mu\text{A}$), and anodic first stimulation, only 2.5 V of positive headroom and 1.5 V of negative headroom are needed. Stimulation artifacts could be detected in the ECG recordings, and are depicted and annotated in Fig. 6.3(c). Recordings were time-aligned to all stimulation pulse onsets and averaged across the entire experiment. The extracted waveform illustrated in Fig. 6.3(e) has a peak-to-peak amplitude of $110 \mu\text{V}$. While noticeable in the ECG recordings, the artifact amplitude is much lower than the R-wave peaks and thus has no impact on the performance of the closed-loop system.

Fig. 6.4 illustrates results from the short closed-loop trials. The measured heart rate over time for all five trials is illustrated in (a), with the time of PI controller activation set to 0. Different color traces correspond to different trials with different targets. The dashed black lines illustrate the target level for each trial. The corresponding stimulation frequency computed autonomously by the PI controller is depicted in Fig. 6.4(b). Again, different color traces correspond to the different trials.

In each trial, the large initial error was slowly reduced over the course of 60 seconds by the PI controller, as the stimulation frequency was titrated up from 0 Hz to 2 -

CHAPTER 6. CLOSED-LOOP CONTROL OF CARDIAC RHYTHM

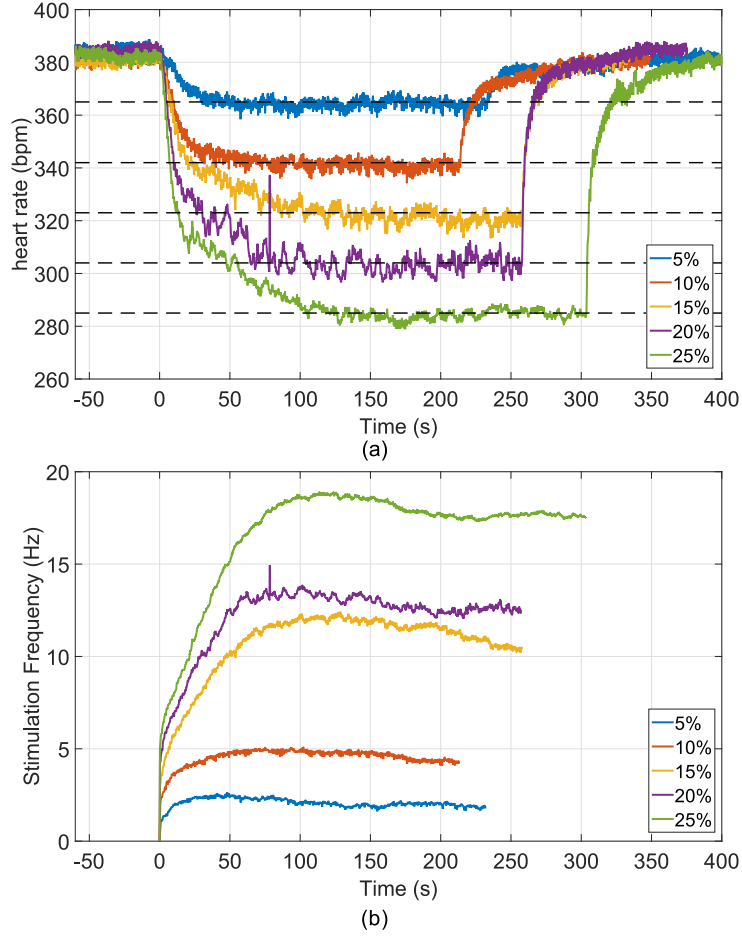


Figure 6.4: Results of closed-loop heart rate control experiments. (a) Measured heart rate during five trials with heart rate targets (black dashed lines) ranging from 5% - 25% decreases from baseline. (b) Delivered stimulation frequency calculated autonomously by the PI controller during each trial.

20 Hz, depending on the target. After an initial convergence period, heart rate was held within ± 10 bpm of the target for the duration of the trials. One exception to the accuracy of control was a brief arrhythmia during the 20% decrease trial (spike in the purple trace of Fig. 6.4(a) around $t = 75$ s). This also produced a spike in the stimulation frequency due to K_p in Eqn. 6.2.

Fig. 6.5 depicts the measured heart rate and stimulation frequency during the

CHAPTER 6. CLOSED-LOOP CONTROL OF CARDIAC RHYTHM

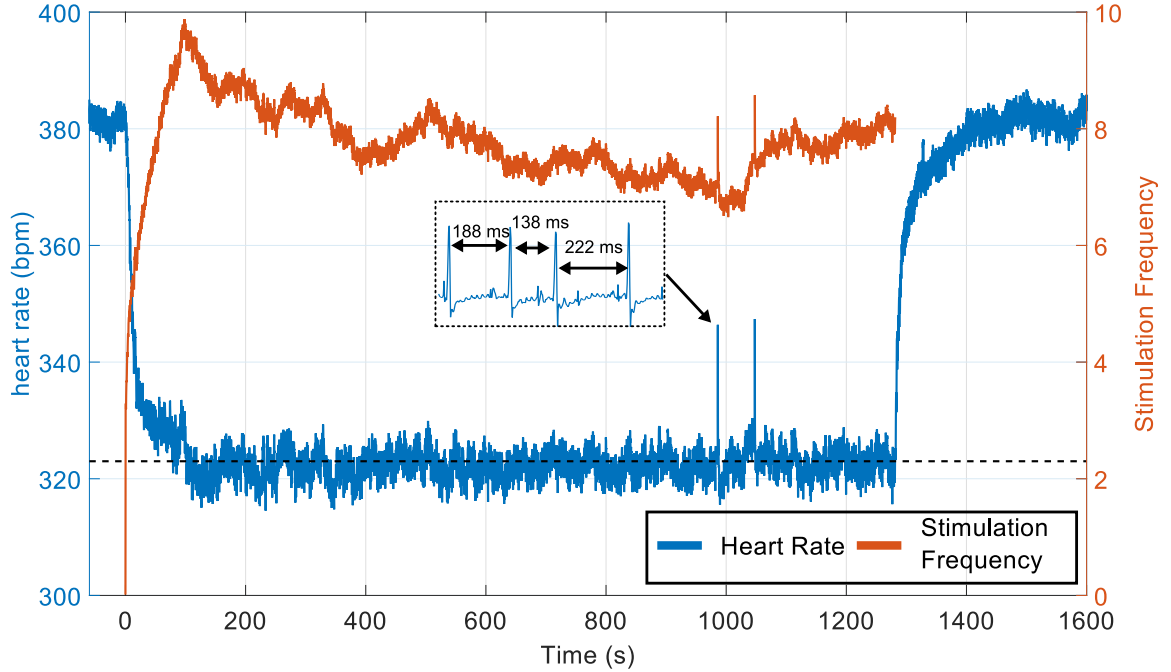


Figure 6.5: Heart rate (blue) and stimulation frequency (red) during a > 1200 s closed-loop control trial. The target (dashed black line) was set 10% lower than the baseline heart rate. After an initial convergence period of 100 seconds, heart rate was maintained within ± 10 bpm of the target, with the exception of two brief arrhythmias. The inset shows the ECG and R-R intervals corresponding to the first spike in heart rate, confirming the spikes are not artifacts. Note also that in the heart rate data, the magnitude of the arrhythmia is attenuated due to the smoothing applied to the heart rate data.

longer, 20 minute trial. Again, the difference between heart rate and target decreases over the course of 120 seconds. Here, the mean heart rate is maintained around the target for the entire 20 minute duration. This trial also produced brief jumps in instantaneous heart rate. As illustrated in the inset, this was not artifactual; in each case, heart rate momentarily jumped above baseline and then rebounded back (the actual amplitude of the change is attenuated in the plots due to the moving average filter described in section 6.1.1). As in the shorter trials this produced brief spikes in

the stimulation frequency as well.

6.4 Discussion

There are several limitations with the proposed system that present opportunities for future work. Stimulation amplitudes were limited to $110\ \mu\text{A}$ per electrode due to the voltage compliance of the stimulator and electrode impedance (7k at 1 kHz). The power supply was limited to 0 - 5V by the process used for chip fabrication. This almost certainly limits the degree to which heart rate can be reduced, requiring relatively high frequencies of stimulation (18 Hz for 20% reduction in heart rate). For example, in one study, 2 ms pulses of 2 mA were used, and could depress heart rate by 50% at $< 8\ \text{Hz}$.²²² Other studies have used a variety of parameters: $\pm 10\ \text{V}$ stimulation, synchronized to ventricular depolarization could depress heart rate by 30%,²²⁶ 10 mA stimulation was used and 15% decreases in heart rate could be controlled,²²⁶ and between 0.4 - 1 mA pulses, synchronized to ventricular depolarization, were used to effect a 10% change in heart rate.²²⁴ A second limitation is that all signal processing has been performed on a PC, so the system is not completely integrated. This could be addressed by writing the algorithms in a hardware-description language, and synthesizing the circuits on chip using a standard-cell library. The algorithms used (R-wave detection and PI controller) are suitable for on-chip implementation.^{122, 227}

Further, Figs. 6.4 and 6.5 show that paroxysmal arrhythmias can arise during

CHAPTER 6. CLOSED-LOOP CONTROL OF CARDIAC RHYTHM

stimulation. Hence, future work will need to address more robust control strategies capable of classifying potentially hazardous states and titrating stimulation appropriately.

Lastly, it can be seen in Fig. 6.5 that stimulation frequency begins to increase from $t=1000s$ until the end of the trial. Whether this trend would have continued had the session not ended is of great interest; the chronic cardiovascular effects of VNS on an intact autonomic nervous system should be further explored. As there are physiological feedback loops working to maintain homeostasis,²²⁸ the effects of artificial electrical stimulation could potentially wane after periods of hours. These issues warrant further study, and mathematical models of the underlying physiology could help in this regard.²²⁴

6.5 Conclusion

This chapter described the implementation of a closed-loop vagus nerve stimulation platform using a custom CMOS chip for both biopotential recording and stimulation. The system is a powerful platform that can enable investigation of novel cardiac function modulation strategies. Future work will be required to integrate signal processing capabilities into a stand-alone miniaturized system, but doing so will enable the investigation of chronically operating closed-loop neuro-cardiac interfaces.

Chapter 7

Conclusions and Future Directions

This thesis presented three contributions to the field of bidirectional neural interface technologies. First, we developed a wireless electrocorticographic monitoring system for rats. Second, we designed an 8-channel CMOS neurostimulator chip with on-chip charge-balancing and current steering circuits. Third we designed a bidirectional neural interface chip with four channels of both sensing and stimulation.

This chapter will summarize the main contributions and then describe opportunities for future research directions.

7.1 A Wireless EEG System for Freely Moving Rodents

Chapter 3 presented a wireless multi-channel neural recording interface for rats and other small laboratory animals. The system weighed less than 30 grams, and consumed 5.1 mA. Due to its small size and low power consumption, this technology allows long-term recording in freely moving animals. For example we showed seizure activity could be detected with the system in a rodent model of global ischemic brain injury. This technology holds tremendous value in the context of bidirectional neural interfaces as it enables exploratory studies in animal models of disease for discovery of electrophysiological biomarkers that may be used to tune stimulation parameters on-line.

7.1.1 Future Directions

The specifications for the wireless system were conceived with medium sized (300 - 400 g) rats in mind. This led to a maximum weight of 10% of their total body weight, 30 - 40g. By distributing the weight between the head and body, this size was very well tolerated by healthy rats. However, an under-appreciated factor was that when studying brain activity in rats post cardiac arrest, the injury drastically compromised the tolerability of any external device. Therefore, further reduction in system weight would be beneficial. The subdivision of the system into a head-stage

CHAPTER 7. CONCLUSIONS AND FUTURE DIRECTIONS

and backpack stage was advantageous as it allowed the recording front-end to sit directly on the electrodes minimizing the physical distance between electrodes and amplifiers. Any length of wire separating the two makes the system more susceptible to interference from the mains and movement artifacts. However, the inclusion of the backpack made the device vulnerable to mechanical failure. For example, if the backpack was secured too tight, it would interfere with the mobility of the animal. However, too loose and often healthy rats could free themselves.

Therefore, removal of the backpack stage in future iterations of the device would be enormously helpful in improving the robustness of the system. This would require stacking the wireless transmitter on top of the neural interface board within the headstage, removing the requirement of the microcontroller, and reducing the battery size such that it fits within the headstage. The nontrivial efforts here include removing the requirement of the microcontroller and reducing the battery size. However, the purpose of the microcontroller was to synchronize the operations of the neural interface and wireless module. Hence minor modifications to the digital read-out circuits in the neural interface would obviate the need for the microcontroller. Further, Section 3.3.1 showed, 20-30% of the system power budget was consumed by the microcontroller. Noting that integration of the microcontroller's duties into a custom integrated circuit would most likely cut that power consumption down to a negligible amount, it is clear that this strategy would result in improvements in both size and power. Lastly, reducing the battery size would result in a lower system lifetime, however, in practice,

replacing a battery once per day would not be too burdensome. Hence, for 24 hour operation, given system power consumption of 5 mA, the system would require a 120 mAh battery. As described in Chapter 3 we have used 200 - 400 mAh batteries, hence, even with no further power savings reducing battery size is still possible.

7.2 A CMOS Current Steering Neurostimulation Array

Neurostimulation devices are limited in size due to the need for external components to ensure safe, charge-balanced stimulation, and limited in specificity due to current spread *in-vivo*. Chapter 4 described the design of a CMOS neurostimulator chip where specific design innovations were introduced to address these issues. Our architecture included a channel-multiplexed calibration circuit that matched the anodic and cathodic stimulation phases to better than 0.3%, matched and ratioed currents across channels with the same precision for current steering, a technique that can be used to enhance the selectivity of electrical stimulation, and calibrated the current DACs to 8-bit resolution. Further, we used the chip to stimulate the sciatic nerves of anesthetized rats to test the current steering capabilities *in-vivo*, and saw the spatial stimulation pattern alter evoked muscle responses.

7.2.1 Future Directions

Technological improvements could be made to the existing design in terms of voltage compliance and power efficiency. It is generally accepted that constant current stimulation is the preferred method for therapeutic systems as it maintains a constant level of charge injection independent of the electrode impedance which can vary over time, and can vary from channel to channel. However, it is not a power efficient method of delivering charge to tissue because a large proportion of the power dissipated during stimulation is dissipated within the current sources not the load.²²⁹ Additionally, for electrodes that do not engage in irreversible faradaic reactions, the injected charge is stored on the electrode and can be recovered,²³⁰ but in general it is wasted during the charge-balancing phase of stimulation. Power efficiency in the stimulator output current buffer can be improved by allowing the power rails to step up during stimulation such that a minimum “saturation” voltage is dropped across the current sources, but no more.¹²³

For large stimulus intensities or large electrode impedances, high voltages can be generated across the electrodes. The chips fabricated as part of this dissertation could only make use of supply voltages as high as 3.3 - 5 V due to process restrictions. Gate-oxide breakdown and hot-carrier effects are phenomena that irreversibly damage MOS devices if the voltage differences across terminals of the device exceed certain values. For example, gate-oxide breakdown limits the gate-to-source voltage, and hot carrier effects limit the drain-to-source voltage. There are two ways to obtain

CHAPTER 7. CONCLUSIONS AND FUTURE DIRECTIONS

higher compliance voltages for the stimulation circuits. The simplest solution is to migrate the design to a process with a high-voltage transistors. The output current buffer would be composed of these devices could operate from ± 10 V supply rails. Alternatively, there are circuit design techniques that permit high voltage supply rails but stack devices in a way that limits the gate-source and source-drain voltages for individual transistors.¹⁶¹

The ability to tune spatial patterns of stimulation digitally offers tremendous opportunities for future *in-vivo* experimentation that could further contribute to the field of neuromodulation. In Chapter 4 we used our neurostimulator chip to apply current-steering patterns to the sciatic nerve in anesthetized rats. Different spatial patterns of stimulation activated different muscle groups in the hind-paw. We used stimulation patterns that have been used by others for selective neurostimulation.^{164,165,174} A more powerful approach, demonstrated by Kent and Grill for the pudendal nerve,¹⁶⁶ would be to create a model of the sciatic nerve and its fascicles, use finite-element methods to simulate the electric field distribution within tissue for different stimulation patterns, and then use computational methods to find spatial stimulation patterns that maximize selectivity. Applying these methods to the vagus nerve would also be of interest, as the location of monopolar stimulation itself has been shown to enhance selectivity.²³¹ The chip designed in Chapter 4 would be a powerful tool to test such predictions.

7.3 A Bidirectional Neural Interface Chip

Lastly, we designed a bidirectional neural interface chip containing four channels of bioelectric sensing and four channels of stimulation. The sensing circuits achieved state-of-the-art performance when considering power consumption, noise performance, and dynamic range. This chip was used to modulate cardiac rhythm with a closed-loop controller. Prior work has used bench-top and commercial instruments to perform such experiments whereas here, *for the first time*, this was done using a single integrated-circuit to perform *both* recording and stimulation.

7.3.1 Future Directions

One important aspect of bidirectional systems not addressed in this work was mitigation of the stimulation artifact in recordings. In Chapters 5 and 6 this issue was circumvented by applying the circuits to paradigms in which 1) stimulation and recording electrodes were physically separated and as a result the stimulation artifact was mostly a common-mode signal, suppressed by the CMRR of the front-end sensing channel, and 2) the feature of interest (R-wave) was much higher in amplitude than the residual stimulation artifact. However, the inclusion of additional artifact-suppression circuits would make the chip more broadly applicable.

Two strategies could be implemented for artifact-rejection; the artifact can be removed either after or before it is processed by the first stage in the sensing chain.

CHAPTER 7. CONCLUSIONS AND FUTURE DIRECTIONS

The most critical consideration is saturation. If the stimulation artifact saturates the front-end sensing circuits, it becomes impossible to recover any information from the recording channels. If removing the artifact after the first stage, external, passive bandpass filtering may be necessary to limit the artifact amplitude.¹¹⁰ Without external passive filtering, a very high dynamic range input stage would be necessary. Removing the artifact before the first stage relaxes the dynamic range requirements on the sensing architecture. In Chapter 5 the very large DC electrode offset voltage was directly subtracted at the input to the bioADC preventing saturation. This same principle can be applied for stimulation artifact rejection. In this case the artifact waveform must be “learned,” which can be accomplished with an integrated adaptive filter.²³²

A promising future direction would be to combine closed-loop stimulation with current steering. For example, the bradycardic effects of vagus nerve stimulation are undesirable in many applications. With a bidirectional system it may be possible to titrate up and down “steering” stimulation channels to block cardiac effects while maintaining constant stimulus strengths. The addition of other sensing modalities into the system, such blood-pressure monitoring, might permit even further specificity.

To conclude, the research described in this dissertation has contributed to the state of the art in bidirectional neural interface systems by developing new techniques for wireless neural recording in small animals, IC design of neural stimulators, and IC design of low-power, low-noise biopotential recording circuits. Aim 1 resulted in a

CHAPTER 7. CONCLUSIONS AND FUTURE DIRECTIONS

system that can enable exploratory research on neural biomarkers, the discovery of which can be leveraged in bidirectional neurotherapeutic systems. Aim 2 produced a neurostimulator IC with on-chip charge balancing and current steering calibration. Finally aim 3 incorporated aspects of the first two aims and resulted in a custom chip that integrated the novel neurostimulation platform of aim 2 with state-of-the-art sensing capabilities. This bidirectional interface chip is a powerful testbed for neuromodulation research. The technologies developed here will be useful in discovering and testing new neuromodulation paradigms in pre-clinical animal models of disease, and those discoveries could one day impact the health of patients.

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