On the Characterization and Manipulation of Interfaces in Organic and Hybrid Electronic Devices

by

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Abstract

Organic electronics comprises a field of study at the intersection of chemistry, physics, electrical engineering, and materials science focused on the development of electronic devices in which the active charge transporting materials are composed of organic conjugated molecules. This field has grown out of an interest in harnessing many attributes of organic materials not readily available to inorganic semiconductors, including: low synthesis temperatures for organic compounds; a nearly infinite combination of chemical moieties with similar conjugated character; and ease of fabricating thin films of organic compounds through both vacuum and solution processes. These properties make the fabrication of low-cost, highly-customizable electronics commercially viable, despite their inferior carrier transport to crystalline inorganic semiconductors. This key hurdle—understanding charge transport in organic molecules and thin films made from them—has become a primary research objective in the field.

Understanding charge transport in organic electronic devices spans analysis across various size scales, each contributing to the observed behavior of an electronic device:

- The chemical structure of the constituent conjugated molecules (Ås)
- The arrangement of these molecules into ordered and disordered regions within a thin film (10s of Ås)
- The configuration of the thin film within the working device (100s of Ås)

At each of these scales, the concept of an interface acquires new meaning, scaling from van der Waals forces between molecules, to grain boundaries in polycrystalline materials, and incrementally to device-scale junctions between dissimilar materials. Because each of these interfaces can promote or inhibit carrier transport within an electronic device, a complete understanding of carrier transport in organic semiconductors (OSCs) demands comprehensive characterization of interfaces at each of these scales.

The subject of this thesis is a critical examination of the insulator-OSC interface in the context of several electronic device architectures. The properties of this interface are of paramount importance in organic field-effect transistors (OFETs), where the low intrinsic carrier mobilities of OSCs renders them highly susceptible to even the most marginal deviations from an ideal interface. As a result, transistor switching characteristics quickly carry through to circuit-level reliability and power consumption. This dissertation aims to demonstrate the use of existing materials in new ways for exercising nanoscale control over this interface, with an eye towards understanding their individual and collective charge transport behavior.

Chapter 1 reviews the state of the art in control over the threshold voltage of OFETs, of which two methods—dipolar self-assembled monolayers (SAMs) and electrostatic poling—are considered in the subsequent chapters. Chapter 2 details the use of SAMs of dipolar alkylsilanes as a surface treatment for tuning V_T, reducing leakage currents, and improving switching efficiency. Increases in field-effect transconductance in SAM-treated OFETs are shown to be consistent with the presence of additional surface states.

Chapter 3 details an approach to decouple the relative contributions of the insulator/SAM and SAM/OSC interfaces from the capacitive responses of the OFET multilayer, and is compared to recent theoretical predictions of increased energetic disorder in SAM-treated OSC layers. Increased mobility of equilibrium carriers as measured with charge extraction are compared to OFET measurements and are shown to further reinforce the notion that larger molecular dipoles contribute to enhanced carrier transport through changes in the energetic disorder at the insulator/OSC interface. In Chapter 4 electrostatic poling, or gate stressing, of lateral OFETs is explored. A Poisson's equation model is applied to surface potential images of stressed lateral OFETs and shown to accurately predict the observed threshold voltage shift. Lastly, Chapter 5 presents future directions for the study of SAM-treated interfaces using charge extraction, with a focus on the use of SAMs as remedial layers for marginal quality OSCs. In addition, the potential of surface potential-derived charge densities for sensing applications is discussed.

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Chapter 1 : Introduction to Metal-Insulator-Semiconductor (MIS) Diodes and Organic Field-Effect Transistors

Semiconductors are a class of materials whose electrical conductivity can be modified across a wide range, from that of an insulator to that of a metal. A broad spectrum of electronic devices harness these changes in a semiconductor's conductivity through illumination (solar cells), heating and cooling (thermoelectric generators), the adsorption of chemical species (gas sensors), and the application of an electric field (diodes, transistors, light-emitting diodes). In each device, the material is designed to achieve the greatest change in conductivity for the given external input. Understanding the structure of a semiconductor is critical if control is to be exercised over its electronic properties.

An inorganic semiconductor consists of atoms arranged in a periodic 3-dimensional lattice. The periodicity of the crystal results in an overlap of the electron orbitals of each individual atom, which collectively create bands of allowed energy ranges, separated by regions of forbidden energy ranges. This forbidden energy range is termed the *bandgap*. In an intrinsic semiconductor at a temperature of 0 K, all of the electrons in the semiconductor reside in the lowest energy band, called the valence band. The next available allowed energy band, called the conduction band, is completely empty at 0 K. As the temperature increases, electrons in the valence band will acquire thermal energy, which at room temperature is equivalent to 26 meV.

For many inorganic semiconductors, whose bandgaps can range from ~0.6 - 1.5 eV, it would be impossible for an electron to be thermally excited across the bandgap. However, impurities in the material can create localized states with energies that fall within this bandgap. If the energy of this impurity state is located sufficiently close to the valence band, an electron within the valence band may acquire enough energy to occupy that state, leaving behind an empty state in the valence band below. This absence of an electron in the valence band is called a hole, and the impurity that traps the electron is called an acceptor. Similarly, if an impurity state in the bandgap is located sufficiently close to the conduction band, an electron from the impurity may acquire enough energy to populate a state in the conduction band; these impurities are called donors. Precise control over the type and density of these impurities is known as doping, an illustration of which is shown in Fig. 1.1.

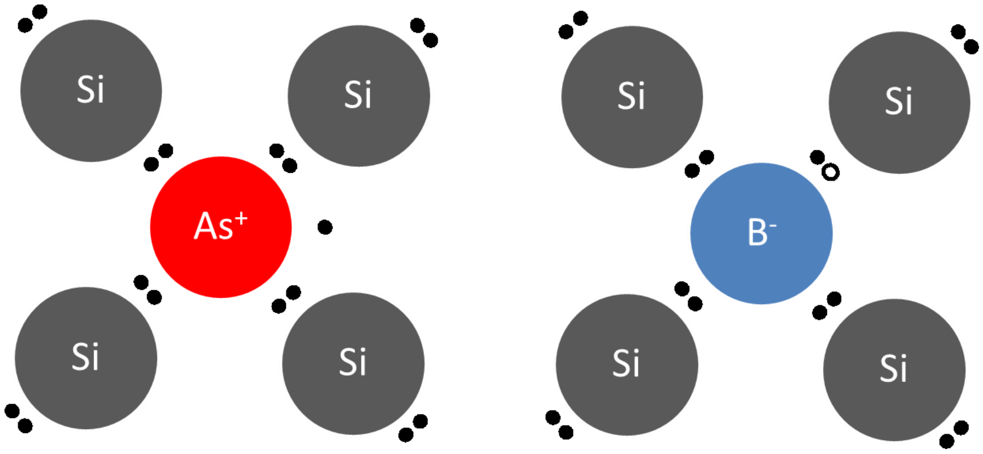


Figure 1.1 Substitutional doping of silicon with arsenic (**boron**) to make silicon more n-type (**p-type**).

As a consequence of doping, not only is the quantity of free carriers changed, but also the *type* of carrier, as an increase in impurities just above the valence band will yield an excess of (+) holes, and an increase in impurities just below the conduction band will yield an excess of (-) electrons, relative to the intrinsic semiconductor. These two types of doping yield films that are referred to as p-type and n-type, so called for the abbreviation of the sign (positive/negative) of mobile charge carrier whose concentration they increase.

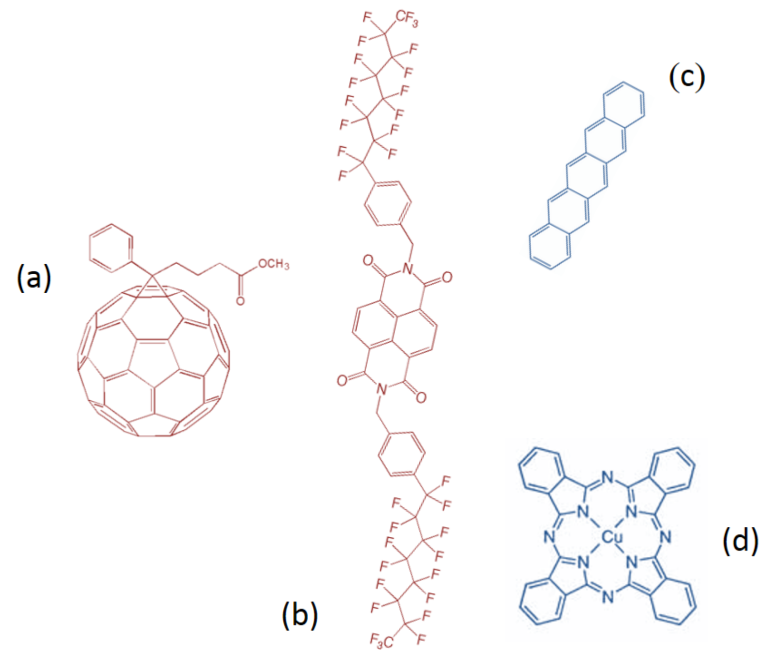


Figure 1.2 Several electron transporting (red) and hole transporting (blue) small molecules typically employed in OSC thin films. (a) phenyl-C_{61}-butyric acid methyl ester (PCBM); (b) 8-0-Bn naphthalene tetracarboxylic diimide (NTCDI); (c) pentacene; (d) copper phthalocyanine (CuPC).

By contrast with inorganics, organic semiconductors (OSCs, Fig. 1.2)—thin films of conjugated organic molecules—do not have a large number of intrinsic free carriers. Because of their much larger bandgaps (typically 2-3 eV), electrons cannot be easily thermalized from the highest occupied molecular orbitals (HOMO) to the lowest occupied molecular orbitals (LUMO). Whereas a thin film of intrinsic Si might contain carriers at a concentration of ~10^{10} cm^{-3}, and a Si film found in an operational electronic device might contain carrier concentrations of 10^{18} cm^{-3} or greater, typical intrinsic carrier levels in OSCs might be as low as 10^{1}-10^{5} cm^{-3}, and unintentional doping due to impurities[1] might increase this density to 10^{14} cm^{-3}.

The first organic materials to show promising charge transport were polymers such as polyacetylene, for which Alan Heeger, Alan MacDiarmid, and Hideki Shirakawa were awarded the Nobel Prize in Chemistry in 2000. Charge transport in these polymers was achieved by chemically doping the films with compounds that chemically reduced the conjugated chains. Heeger and co-workers used the vapors of binary halides such as Br_2 and I_2 to dope films of polyacetylene[2]. By introducing these electron-accepting dopants and making available sites with electronic resonance along the chains, carrier mobility was increased from negligibly low (10^{-4}

S/cm) to industrially relevant (~1 S/cm). This approach has been employed in the fabrication of the now ubiquitous conductive inks poly(3,4-ethylenedioxythiophene):polystyrene sulfonate (PEDOT:PSS)[3]. Although still below the mobility of doped Si (10^2 - 10^3 S/cm), the ability to control the conductivity of thin films of conjugated organic compounds has fueled the study and design of thin films and materials for OSCs.

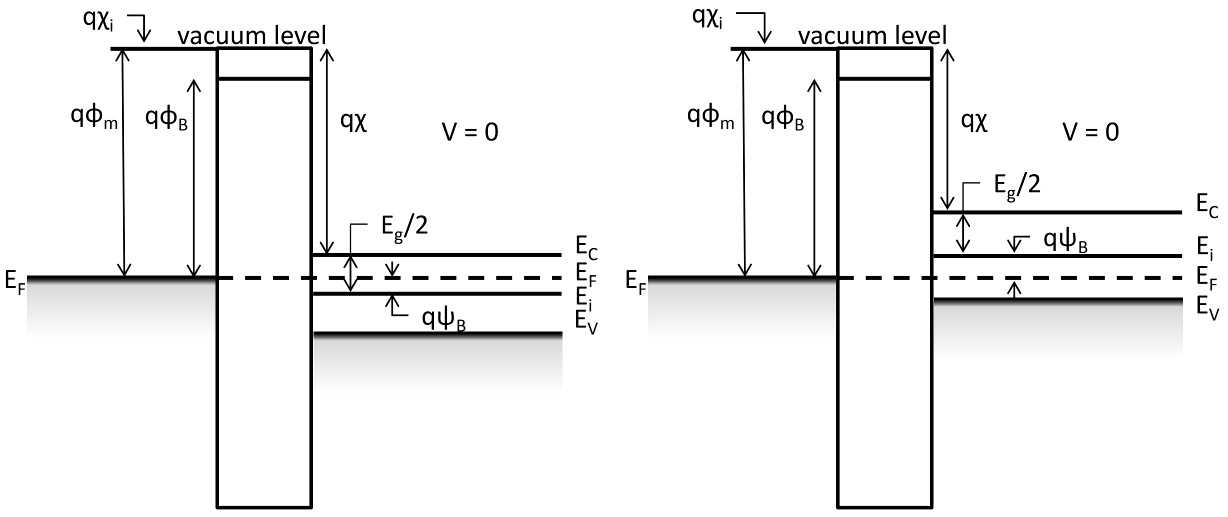
Coupled with low intrinsic carrier densities in pristine OSCs is the low degree of carrier delocalization within these films, which can range from just a few conjugated cores to several nm within the OSC[4]. Films made of highly-ordered semicrystalline polymers such as P3HT and recently PBTTT, as well as prototypical acenes like pentacene and di-imides like NTCDI, have been well modeled with traditional concepts from the inorganic lexicon. However, investigations of carrier transport in many of these polymers and other disordered organic materials has been demonstrated to not follow band-like behavior with few exceptions[5] substantially below room temperature.

Instead, transport is more accurately described by a hopping mechanism[6-8], which defines carriers as existing in a 3-dimensional Gaussian density-of-states (DOS) through which they sample the space under the influence of an electric field. The presence of grain boundaries as well as chemical impurities all act to change the landscape through which carriers hop. Polymorphs (in the case of evaporated semicrystalline small molecules) can also affect inter-molecular distances between conjugated cores[9], with greater core-to-core distances reducing the probability of a hop. In a recent report, it has been shown that the thermal motion between two neighboring pentacene molecules in a crystal reduces the hopping probability between neighboring molecules[10], negatively impacting the carrier mobility of the film. Such behavior may appear contrary to inorganics, where thermal excitation of the lattice at room temperature promotes carriers from dopant atoms to their target bands, increasing the conductivity of the semiconductor. Through advances in understanding unconventional, disordered semiconductors such as amorphous silicon[11], quantities including the mobility[7] and carrier diffusivity[12-14] have been modeled within this framework with satisfactory results.

Despite the differences between charge transport mechanisms within inorganic and organic semiconductors, the design and synthesis of OSCs that preferentially transport holes or electrons has enabled the fabrication of electronic devices with properties analogous to those of inorganic materials. As a result, the characterization tools used to evaluate inorganic devices have been heavily borrowed, occasionally indiscriminately, to the characterization of those based on OSCs. In the following section, the basic operation of a field-effect transistor is discussed, starting with fundamental operating principles derived for inorganic materials. Where appropriate, differences in operation between organic and inorganic field-effect transistors is discussed.

Organic Field-Effect Transistors

One of the main considerations for OSCs is their use in digital logic, the main component of which is the transistor. The main transistor architecture investigated in the context of OSCs—and a main subject of this dissertation—is the field-effect transistor (FET). A conventional [inorganic semiconductor] FET derives its name from the concept of a "transfer resistor," and builds on the concept of a metal-insulator-semiconductor (MIS) junction.



(a) n-type semiconductor

(b) p-type semiconductor

Figure 1.3 Energy band diagrams of a metal-insulator-semiconductor (MIS) junction at vacuum level for (a) n-type and (b) p-type semiconductors. Energy level for the conduction (E_C) band is determined by the electron affinity (χ). Energies corresponding to the semiconductor's Fermi (E_F), intrinsic (E_i), and valence (E_V) bands are shown for n-type and p-type semiconductors. Alignment between E_F and the workfunction (φ_m) are illustrated. Barrier heights between the metal and insulator (φ_b) and between the Fermi and intrinsic levels (ψ_B) are referenced to the metal work function and semiconductor Fermi levels, respectively.

In an MIS junction (Fig. 1.3), a wide band-gap insulator separates a conductive metal contact from a semiconductor thin film. The metal is defined by its work function φ_m, which is the energy required to remove an electron from the surface of the metal. This value is assumed to be a material constant, but can vary by several tenths of an eV depending on the crystallographic facet facing the surface, as well as any impurities at the surface[15]. The semiconductor is defined by its valence and conduction bands. These bands arise from the delocalization of electrons within the semiconductor crystal lattice, and represent the energy levels which charge carriers may occupy within the material.

The gap between the valence (E_V) and conduction band (E_C) energies is termed the bandgap (E_g), and represents energies which carriers are forbidden to occupy (in the absence of doping). The intrinsic energy E_i is the average energy of an electron in an intrinsic semiconductor, and is roughly halfway in the bandgap. As suggested in the previous section, doping introduces atoms of a greater or lower valence than the host semiconductor atoms, at energy levels within the bandgap. This additional population of states changes the electrochemical potential of electrons in the semiconductor—that is, the Fermi energy E_F. Since these gap levels can be populated thermally, they can be modeled using Maxwell-Boltzmann statistics. Assuming non-degenerate doping levels, the Fermi level is approximated by the relation

$$E_F - E_C = kTln\frac{N_C}{N_D}\text{, (n-type)} \qquad [1.1]$$

$$E_F - E_V = kTln\frac{N_V}{N_A}\text{, (p-type)} \qquad [1.2]$$

where N_C and N_V are the density of states for the conduction and valence bands, respectively, and N_D and N_A are the densities of dopant donor and acceptor atoms, respectively. As the physics of doping falls outside the scope of this thesis, the reader is referred to Ref. [16].

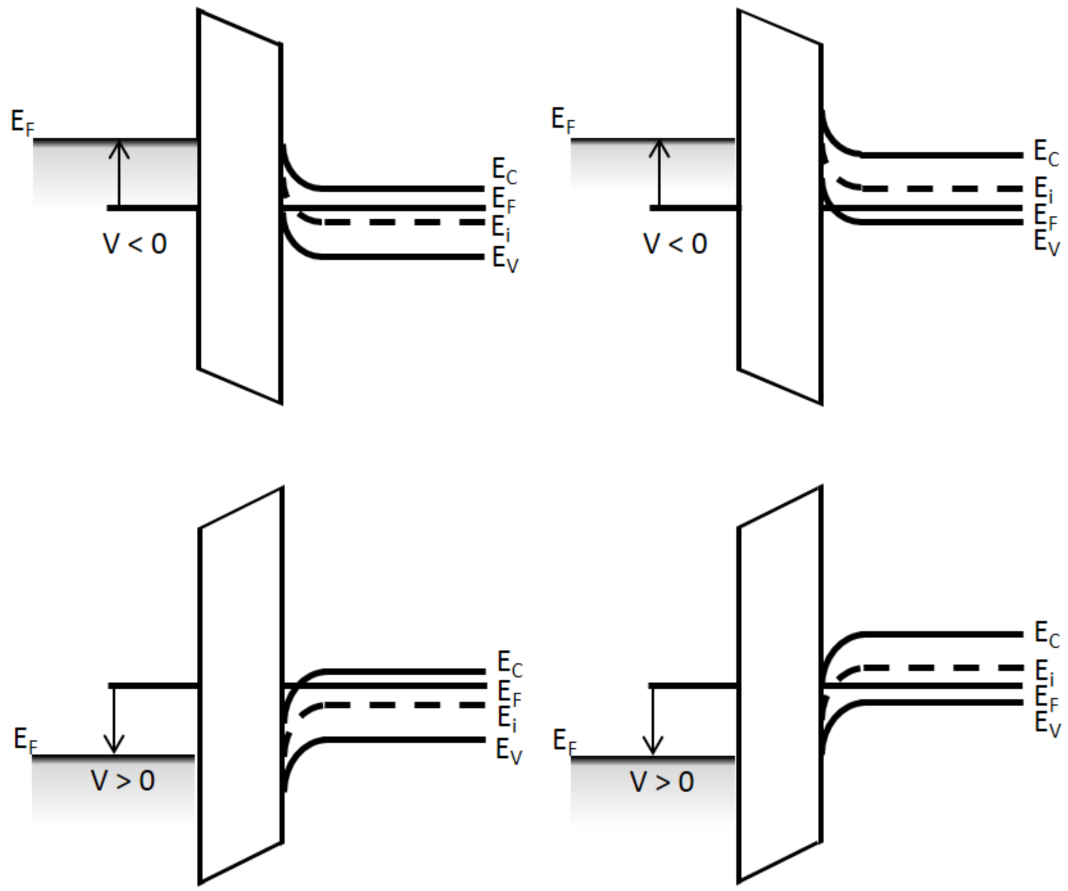
In an ideal MIS structure, the very low density of conducting states in the insulator makes it impossible for carriers in the semiconductor and metal directly in contact on either side to transit the insulator to reach equilibrium. This lack of available states in the insulator results in a pinning of the vacuum-level ionization and electron affinity energies at the insulator/semiconductor interface. As illustrated in Fig. 1.3, the energy difference between the metal and semiconductor at vacuum level is given as

$$\varphi_{ms,N} = \varphi_m - \left(\chi + \frac{E_C - E_V}{2q} - \psi_B\right) \qquad [1.3]$$

$$\varphi_{ms,P} = \varphi_m - \left(\chi + \frac{E_C - E_V}{2q} + \psi_B\right) \qquad [1.4]$$

where the sign difference of the semiconductor barrier ψ_B between Eqs. 1.3 and 1.4 reflects the relative potential difference from the intrinsic level E_i for n-type and p-type semiconductors.

When the materials are connected electrically in a circuit and allowed to reach electrochemical equilibrium (both sides are grounded), the mobile carriers in the semiconductor re-distribute themselves to offset the built-in potential fixed by the difference between the metal work function and the Fermi energy in the semiconductor, as illustrated in Fig. 1.4. Because the electron affinity and ionization potentials are a fixed material property[16], the difference between the valence and conduction band energies E_C and E_V, also remains constant. The difference between E_C and E_V relative to E_F within the proximity of the interface reflects the carrier re-arrangement due to the built-in potential and any interfacial dipoles[15]. This re-arrangement is known as band-bending, and is illustrated by the curves adjacent to the insulator. The insulator itself, having no mobile charge carriers, behaves like a resistor. As a result, the electric field across it is distributed linearly between its two surfaces.



(a) n-type semiconductor (b) p-type semiconductor

Figure 1.4 Energy band diagrams of a metal-insulator-semiconductor (MIS) junction for **(a)** n-type and **(b)** p-type semiconductors.

Upon application of a potential difference between the metal and semiconductor sides, the mobile charge carriers in the semiconductor will again redistribute themselves to offset the applied potential. In doing so, the carrier bands near the insulator interface may bend upwards, downward, or lay flat. The latter case is known as flat-band, and is the device state representative of the vacuum-level energy alignment in the device seen in Fig. 1.3. The effect of bands bending upwards or downwards depends on the polarity/doping type of the semiconductor, as seen in Fig. 1.4.

To achieve generality in our discussion, we refer instead to the following device states: accumulation, flatband, and depletion/inversion. In accumulation, the applied potential shifts the

Fermi energy of the semiconductor at the insulator interface closer towards the majority carrier type, while in depletion, the applied potential shifts the Fermi energy closer to the minority carrier type. The concept of inversion, most applicable to inorganic semiconductors, occurs when the bands are bent past the point of depletion until insulator-semiconductor junction is populated by a greater density of minority carriers than of the semiconductor's majority carriers. It is important to note that this thesis concerns itself only with OSC-based devices operating in accumulation mode.

Transistor Operation

An FET structure can be conceptually represented as an MIS diode with an additional electrode at the semiconductor interface. Whereas with one electrode, a density of carriers could be accumulated at the insulator-semiconductor interface, an additional electrode affords the opportunity to extract this charge from the interface as a current. Since the potential difference between the semiconductor and the metal determines the degree of band bending (as in Fig. 1.4), the accumulated charge and hence current extracted at the third electrode will be influenced by this potential difference. The result is illustrated in Fig. 1.5.

To gain a further understanding of the transistor structure, some notational convention is in order. We denote the two electrodes at the semiconductor interface the Source and Drain, and the metal contact at the insulator interface the Gate. Thus, the potentials between the three contacts are denoted V_S, V_D, and V_G, respectively. It is assumed that the potential between the Source and the Gate is set to 0 V (grounded). The area between the source and drain electrodes is called the transistor channel; the source-to-drain distance is denoted the channel length L, and the extent of the electrodes is denoted the channel width W.

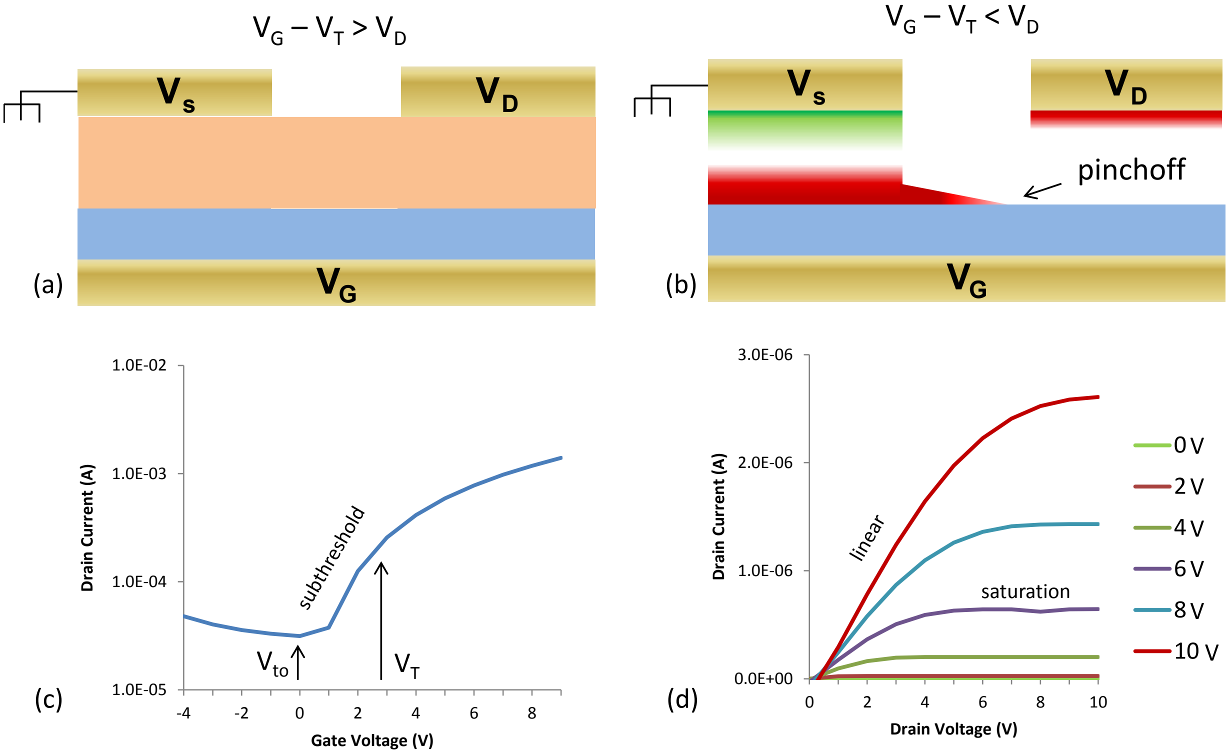


Figure 1.5 Illustration of a bottom gate/top-contact n-channel accumulation-mode OFET on 100nm SiO2. **(a)** FET in the linear regime.The gate-drain field (or V_G - V_D) is smaller than the gate-source field (V_G - V_S). The carrier concentration in the transistor channel is mostly uniform throughout when $V_D < V_G - V_T$, the threshold voltage. **(b)** Formation of a space-charge region near the drain contact when $V_D = V_G - V_T$. Saturation occurs when $V_D > V_T$. **(c)** Transfer curve for the same device. **(d)** Output curve for the same n-channel accumulation-mode OFET, with linear and saturation regimes identified.

The transistor, as a steady-state device, can be in one of several states. In the OFF state, the gate potential V_G is grounded, and hence $V_G = V_S$. While there may exist a potential difference between source and drain, the potential differences relative to the gate are not sufficient to induce significant charge (Fig. 1.5(c), subthreshold regime). In the ON state, the gate potential V_G is set to accumulate carriers at the insulator-semiconductor interface (Fig. 1.5(b)). As a result, a charge density accumulates in the channel between source and drain, and the gradient of that charge is a function of the potential differences among the three terminals.

The current flowing between source and drain is related to the accumulated charge at the interface, which is given as

$$Q(x) = n_{channel}(x)qd = C_i(V_G - V(x)) \qquad [1.5]$$

where $n_{channel}(x)$ is the charge density as a function of the source-drain distance, q is the fundamental charge, and d is the thickness of the charge transporting layer. The charge along the transistor channel length is then just the difference in potential relative to the gate voltage V_G, multiplied by the insulator capacitance C_i.

As will be discussed in the following section, FETs exhibit a particular voltage at which the conductance between the source and drain electrodes rises very quickly. This voltage is termed the threshold voltage (V_T). Although a cursory glance at the MIS structures in the previous section would suggest that V_T should be 0 for a device, the presence of defects and impurities in the semiconductor and surface states at the insulator-semiconductor interface will act to trap charges that would otherwise contribute to mobile charge. The net result is a shifting of the V_T from 0 V. To account for this deviation, we adjust Eq. 1.5 by replacing V_G with $V_G - V_T$.

As Eq. 1.5 clearly suggests, a linear gradient in the charge density at the interface should appear along the transistor channel, from the source where $V_D = 0$, through to the drain electrode where the drain voltage is V_D. Thus, for small drain voltages V_D, one expects that

$$Q(x) = C_i(V_G - V_T - V(x)) = C_i\left(V_G - V_T - \frac{V_D}{2}\right) \qquad [1.6]$$

Following the simplified argument presented in Ref. [17], and a more detailed argument in Ref. [16],we can write Ohm's law for the conductance of the transistor channel as

$$\frac{I_D}{Wd} = V_D\frac{\sigma_{channel}}{L} = V_D\frac{\mu\, n_{channel}q}{L} \qquad [1.7]$$

where I_D is the current at the drain electrode, $\sigma_{channel}$ is the channel conductivity derived from Eq. 1.5, and μ is the charge carrier mobility. Rearranging Eq. 1.7 gives us an expression for the drain current I_D in the linear regime as

$$I_D = \mu C_i\frac{W}{L}\left(V_G - V_T - \frac{V_D}{2}\right)V_D\,. \qquad [1.8]$$

When the drain voltage $V_D = V_G - V_T$, there is no effective potential difference between the drain and the gate. The characteristic current plateau of the source-drain current in the ON state is associated with the creation of a space-charge region in the transistor channel. The onset of this regime of operation is known as pinch-off, and biasing above pinch-off falls within the saturation regime, so-called for the plateauing of the source-drain current. The absence of free carriers in this region increases the resistance to carriers under the influence of the source-drain electric field. The carrier-poor region extends further into the channel in the direction of the source electrode with increasing V_D. This regime of operation is termed saturation, and an expression for I_D can be obtained by substituting V_D for its value at pinch-off, yielding the expression

$$I_D = \mu C_i \frac{W}{L}\left(V_G - V_T - \frac{V_D}{2}\right) = \mu C_i \frac{W}{2L}(V_G - V_T)^2 \qquad [1.9]$$

In practice, the OFF states are not current-free. The small but significant drift mobility of carriers within the semiconductor channel will contribute to a small but occasionally non-negligible source-drain current in the OFF state. This current is known as subthreshold leakage (Fig. 1.5(c)), because it is current that leaks through when the gate voltage is less than V_T (control over which is discussed in further detail in the latter half of this chapter). In addition, the high electric fields arising from the sub-micron gate stack dimensions result in non-negligible current between the gate and drain electrodes in the OFF state. This current is known as gate leakage. Both of these spurious currents, and materials and device design approaches to address these, are described in greater detail in Chapter 2.

Deviations from inorganic theory

The preceding discussion of MIS and FET structures suggests two key requirements for band bending in MIS diodes: (i) the presence of a large number of mobile charge carriers that can redistribute to offset the built-in potential, and (ii) a continuous (though in practice atomically discrete) distribution range away from the insulator interface. However, OSCs are known to have a very low intrinsic number of mobile carriers, and most as-deposited OSCs are not doped. In addition, the 2-D crystal growth behavior of many small-molecule OSCs yields evaporated thin films that consist of lamellar sheets of OSC islands.

One framework for estimating the charge accumulation in OSC thin films at the insulator-semiconductor interface has been proposed by Horowitz[18] in which charge is confined to discrete molecular layers, akin to a series of capacitors. This model has accurately predicted several known issues in OSC-based transistors and diodes, namely the observation that carrier mobility increases with OSC film thickness[19,20] and that the first layer of OSC is critical to the charge transport of the entire film[9].

The presence—or absence—of band bending has been the subject of numerous investigations into the carrier redistribution and charge transport within an OSC. As discussed in the previous section, even band transport has been questioned in the context of OSCs, with recent experiments demonstrating evidence of band transport below room temperature. Despite the low intrinsic carrier densities, the existence of chemical impurities in the form of dissimilar molecular isomers or environmental contaminants as well as the presence of grain boundaries and crystalline polymorphs, can create sufficiently high trap densities that are accurately represented by band-bending in OSC MIS junctions[1,21].

Equilibrium vs. Kinetics in Transistors

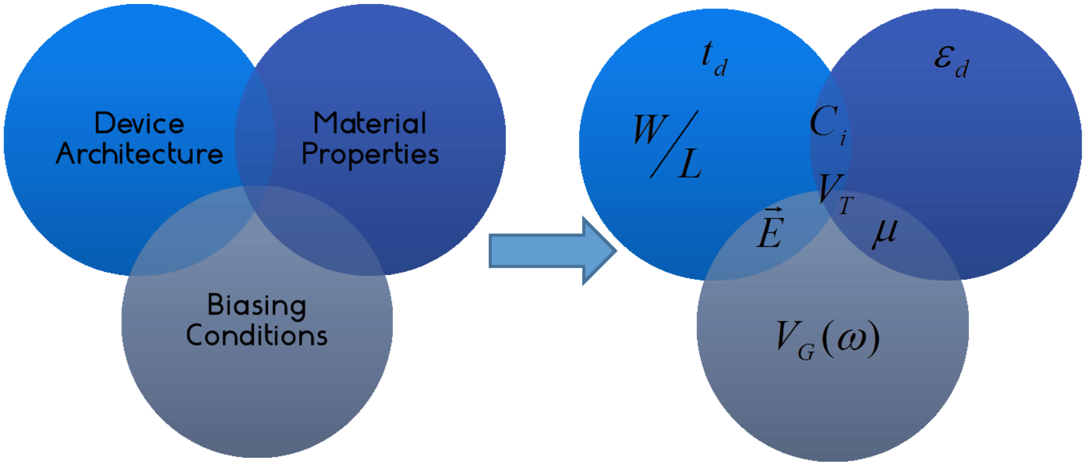


Figure 1.6 Venn diagram illustrating the relationship between the various parameters that determine the operation of an FET.

General analysis of the MIS diode is based on the equilibrium picture of energy level alignment within the structure. However, charge transport depends as much on the kinetics of charge transport (and trapping), as on the device architecture and processing of materials, as illustrated in Fig. 1.6. A prominent example is charge trapping at the dielectric-semiconductor interface. In the equilibrium model for an OFET, the insulating layer consists of a perfect dielectric with negligible transport pathways across it. However, it has been observed that prolonged biasing of the transistor results in a shift of the device’s threshold voltage (V_T), known as gate bias stress. While this problem has been observed in traditional inorganic FETs, its effects are far more severe in amorphous Si- and OSC-based devices. This shift has been associated with accumulation of charge at the dielectric-semiconductor interface, with recent reports identifying charges trapped in the dielectric as the main contributors.

To gain better insight of the details underlying gate bias stress, a suitable analogy for the dielectric-semiconductor interface is in order. Assume that you're standing outside on a hot sunny day before a large concrete wall. If you were to splash a cup of water on the concrete wall, it would remain wet for a few seconds, but would quickly return to its original state. Now if you were to approach the wall with a fire hose and spray it for 30 seconds, the wall would remain wet substantially longer, and perhaps suffer minor damage to the surface. You could instead build a small reservoir in front of the wall—akin to a fountain basin—and allow the water to maintain contact with the wall for a week. When you emptied the reservoir, you'd observe that the concrete could take a day or more to return to a dry state.

The insulator in an MIS structure is not unlike this concrete wall. In the idealized state, the insulator is a perfect dielectric medium, impenetrable to charge and perfectly polarizing. In practice, the insulator is imperfect. It may have a large number of surface states physically and chemically dissimilar from its bulk, which may capture charges approaching the surface within traps of varying energy potentials. When mobile charges (like the water in our analogy) are pushed against the insulator for extended periods of time, the prolonged electric field across the insulator may push charges spatially deeper from the surface into the bulk, where internal defects and impurities may create delocalized charge transport states across it. In some cases, the insulator may return to its original state. In others, the high electric field (pressure) may result in irreversible damage to the insulator.

Like in our water analogy, understanding the role of interfaces in controlling both the equilibrium and kinetic behavior of MIS structures is of paramount importance to the design of functional, reproducible electronic devices. The nature of this trapping is greatly dependent on a number of factors, including the dielectric constant of the insulator[22], the magnitude of the biasing voltage (or electric field)[23], the length of biasing time[24], the frequency/rate of the biasing[25,26], and the energy level overlap between the semiconductor transport states and the trap density of states in the insulator[27]. This critical dependence on both the magnitude and timescale of application of electric fields across the insulator highlights the non-equilibrium nature of the semiconductor-dielectric interface, requiring a kinetic approach to understanding its behavior.

Understanding how these parameters are interconnected would enable proper attribution of each on the accumulation of interfacial charge and hence on their effect on the threshold voltage shift. The *Account* below highlights a number of techniques used to modify the threshold voltage in OFETs, which were major motivators behind the work presented in Chapters 2 and 3.

Tuning the Threshold Voltage in Organic Field-Effect Transistors

This section was published in Accounts of Chemical Research on March 31, 2014, under the title "*Through Thick and Thin: Tuning the Threshold Voltage in Organic Field-Effect Transistors*." It has been edited to incorporate figure, equation, and reference numbers with the rest of the Introduction, and a subsection titled "*Physisorbed Layers*" has been added for completeness.

Through Thick and Thin: Tuning the Threshold Voltage in Organic Field-Effect Transistors

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Conspectus

Organic semiconductors (OSCs) constitute a class of organic materials containing densely-packed, overlapping conjugated molecular moieties that enable charge carrier transport. Their unique optical, electrical, and magnetic properties have been investigated for use in next-generation electronic devices, from roll-up displays and radiofrequency identification (RFID) to biological sensors. The organic field-effect transistor (OFET) is the key active element for many of these applications, but the high values, poor definition and long-term instability of the threshold voltage (V_T) in OFETs remain barriers to realization of their full potential because the power and control circuitry necessary to compensate for overvoltages and drifting set points decrease OFET practicality. The drifting phenomenon has been widely observed and generally termed "bias stress." Research on the mechanisms responsible for this poor V_T control has revealed a strong dependence on the physical order and chemical makeup of the interfaces between OSCs and adjacent materials in the OFET architecture.

In this Account, we review the state of the art of tuning OFET performance via chemical designs and physical processes that manipulate V_T. This parameter gets to the heart of OFET operation, as it determines the voltage regimes where OFETs are either ON or OFF, the basis for the logical

function of the devices. One obvious way to decrease the magnitude and variability of V_T is to work with thinner and higher permittivity gate dielectrics. From the perspective of interfacial engineering, we evaluate various methods that we and others have developed, from electrostatic poling of gate dielectrics to molecular design of nanoscale side chains. Corona charging of dielectric surfaces, a method for charging the surface of an insulating material using a constant high-voltage field, is a brute force means of shifting the effective gate voltage applied to a gate dielectric. A gentler and more direct method is to apply surface voltage to dielectric interfaces by direct contact or post-process biasing; these methods could also be adapted for high throughput printing sequences. Dielectric hydrophobicity is an important chemical property determining the stability of the surface charges. Functional organic monolayers applied to dielectrics, using the surface attachment chemistry made available from "self-assembled" monolayer chemistry provide local electric fields without any biasing process at all. To the extent that the monolayer molecules can be printed, these are also suitable for high throughput processes. Finally, we briefly consider V_T control in the context of device integration and reliability, such as the role of contact resistance in affecting this parameter.

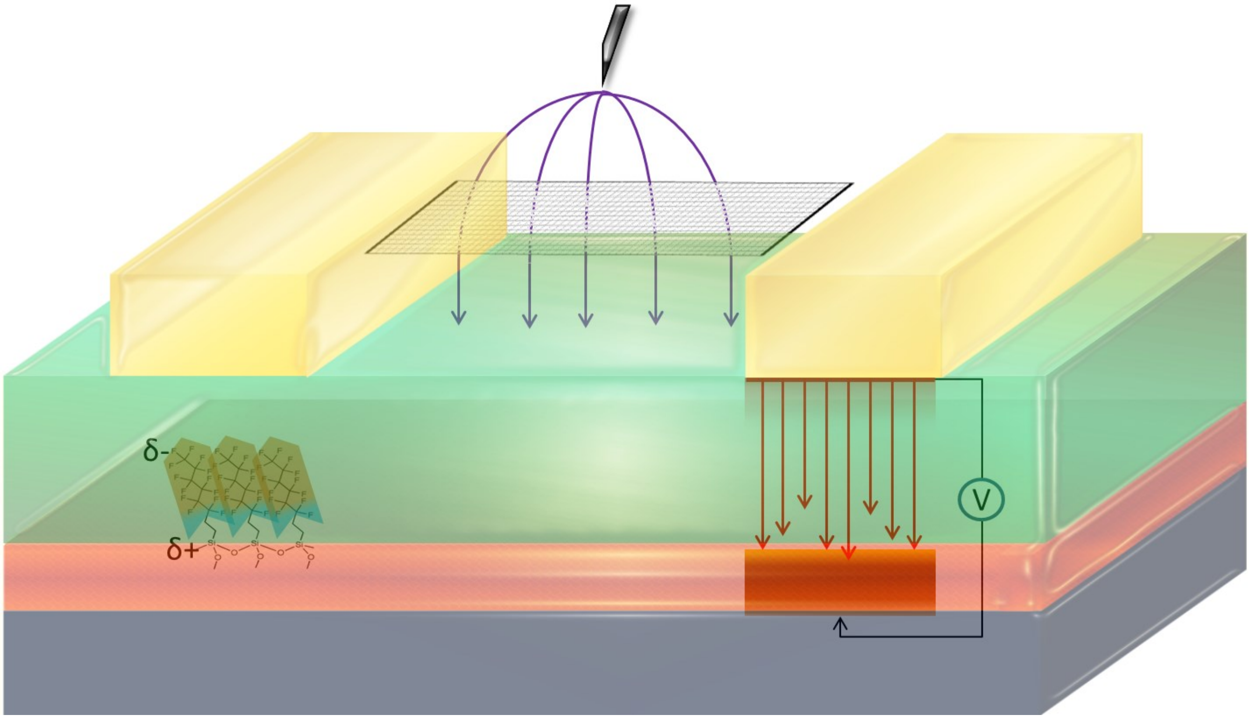

Figure 1.7 Cross-section of an organic field-effect transistor (OFET) with idealizations of several methods for controlling the threshold voltage. Interfacial molecular dipoles (left), corona/triode charging (center), and gate bias stressing (right).

Introduction

Organic semiconductors (OSCs) have been the subject of intense research for their combination of optical, electrical, and magnetic properties. Conjugated moieties in close contact enable the overlap of molecular orbitals, facilitating carrier transport in OSC films consisting of small molecules and/or polymers. From a fabrication standpoint, their solubility in a wide spectrum of solvents and low sublimation and melting temperatures make them an attractive addition to the materials palette and ideal candidates for low-cost electronic devices. Organic field-effect transistors (OFETs) figure prominently in OSC research as the potential basis of digital logic for all-organic electronic systems. The requirements for OFETs in appropriate applications are similar to those of inorganic complementary metal-oxide-semiconductor (CMOS) transistors: low and stable operation voltage, high ON-OFF ratio, fast switching, and minimal OFF-current leakage.

Low-voltage operation is critical for most conceivable applications of organic electronics, namely radio-frequency identification (RFID), mobile displays, and implantable medical devices. In the digital sense, the operation of a transistor consists of switching from a logical 0 (OFF) to a logical 1 (ON). We recall that the current flowing in the ON state is given by the saturation regime approximation[16] as shown in Eq. 1.9.

$$I_D = \mu C_i \frac{W}{2L}(V_G - V_T)^2 \qquad [1.9]$$

Here the current I_D is the current flowing between the source and drain terminals; W and L are geometric terms for the electrode extent and separation, respectively; μ is the majority charge carrier mobility; C_i is the capacitance of the dielectric, given as $C_i = \varepsilon_i\varepsilon_0/t_i$, where ε_i is the relative dielectric constant of the gate dielectric, ε_0 is the permittivity of free space, and t_i is the thickness of the dielectric; V_G is the voltage applied to the gate electrode and V_T is the threshold voltage at which the transistor turns ON. Low-voltage organic circuitry relies on OFETs that exhibit considerably larger drain current in the ON state relative to their OFF state, with application of a minimal gate voltage. Initial approaches to increasing I_D have focused on reducing the transistor channel length, increasing the capacitance of the gate dielectric, and developing high-mobility OSCs.

In addition to low voltage operation, the control and stability of the V_T are critical for proper device operation. For an n-type (**p-type**) transistor, the ON state is maintained by keeping the Source electrode at ground, and the Gate and Drain at a high positive (**negative**) voltage. In this state, the dielectric is subjected to a high static electric field across its thickness. Maintaining the transistor in this state for extended periods of time results in a gradual shifting of the V_T toward higher accumulation voltages, requiring greater $|V_G|$ to achieve the same I_D. This V_T shift in a digital circuit ultimately leads to circuit failure, as the transistor requires more voltage to switch than its driving transistor can provide. This phenomenon has been termed "gate bias stress," and is associated with the buildup of charge and/or creation of dipoles at the OSC-dielectric interface,[28,29] capturing majority carriers in the OFET channel that would otherwise contribute to the net I_D. In this Account we explore various physical and chemical methods that enable control over the value and stability of the V_T by modifying the OSC-dielectric interface.

One of the materials challenges associated with fabricating all-organic OFETs has been the development of high dielectric constant insulators.[30] Work by Acton *et al.*[31] employed an HfO_2 sol-gel dielectric (ε~16-25), and our own group has developed a sol-gel sodium beta-alumina-like dielectric[32] with ε~170. However, most organic insulators have relatively low dielectric constants (ε~2-3), requiring V_G as high as |100 V| to turn on an OFET on a 100 nm-thick dielectric, with a significant fraction of this potential constituting an overvoltage. While reducing the dielectric thickness seems a logical method towards reducing the threshold voltage, the greater current leakage arising from pinholes and other defects[33] in sub-20 nm films makes this approach impractical for many polymer dielectrics.

Several methods for reducing the overvoltage of thick organic dielectrics rely on using large electric fields to shift V_T closer to zero. Triode-corona charging, borrowed from the electret community, functions as a dielectric preparation technique prior to OSC-deposition. For fully-fabricated devices, floating gates and electrostatic pre-polarization of the OFET facilitates lower

V_T via charge injection into the gate dielectric. Each technique leverages mechanisms ranging from dielectric polarization to direct charge injection, as discussed below.

Triode-corona charging

Corona discharge is a method for charging the surface of an insulating material using a constant high-voltage field. The typical experimental setup for corona discharge relies on a three-electrode setup—or triode—consisting of a bottom plate and top emitting electrode held at a high voltage (~5-10 kV), and a grid electrode between these two that creates a potential difference between the grid and bottom plate (~10's of V), as shown in Fig. 1.8. This grid ensures that only charges with energy equivalent to the grid potential can strike the bottom plate on which the device substrate is placed. Typical grid potentials for pre-polarizing dielectrics range from as low as 15 V to as high as 1000 V, but this voltage must not be so high as to cause dielectric breakdown. The sign of the grid potential is selected to be equivalent to a large top-surface depletion potential: for an n-type (**p-type**) transistor, the grid potential should be held at a high positive (**negative**) voltage relative to the grounded bottom electrode.

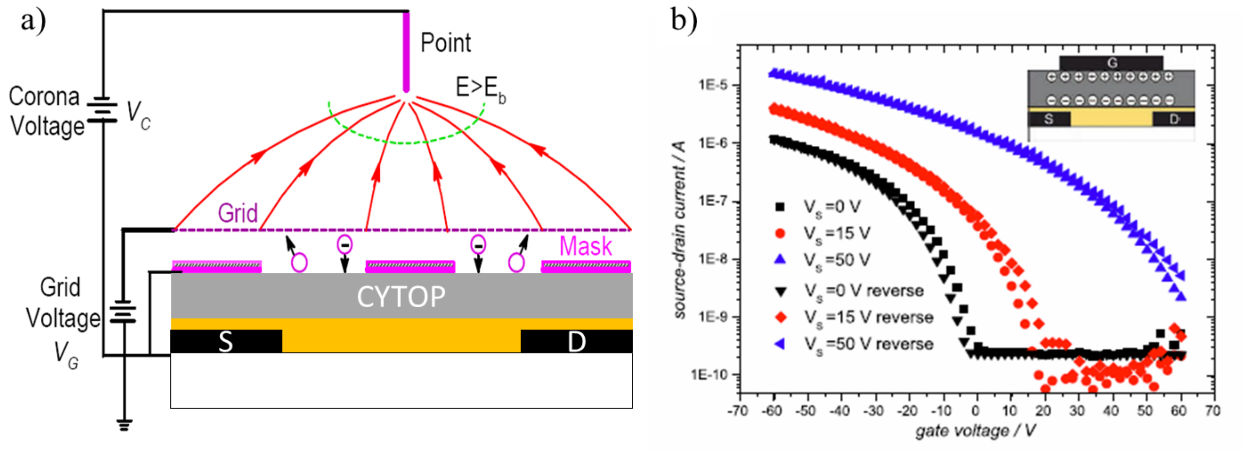

Figure 1.8 (a) Illustration of triode corona charging of an organic dielectric.The corona voltage V_C between the top and bottom electrodes (as high as -8 kV), and the grid voltage V_G between the grid and bottom electrode (0-60 V), satisfy the relation $V_C \gg V_G$. **(b)** Output curves for OFETs without corona pre-polarization (hollow squares) and with a dielectric pre-polarized with V_C = -8 kV, V_G = -50 V, showing much larger I_D under equal biasing conditions. Adapted image from Refs. 34 and 35.

The long retention times from corona-implanted charging make it an attractive technique for devices requiring long operating lifetimes: the method has been used for decades in the manufacture of electret materials for piezoelectric applications such as microphones and speakers, using methods developed by Sessler and West,[36] and Giacometti and Gross.[37] Corona charging has been investigated on hydrophilic polymers such as poly(vinyl alcohol) (PVA);[38] hydrophobic polymers such as polystyrene (PS) derivatives,[39] poly(acrylonitrile-co-butadiene-co-styrene[40] (ABS), and polyethylene[41] (PET); and amphiphobic polymers including Teflon, poly(tetrafluoroethylene) (PTFE),[42] and Cytop.[35,43] Techniques such as thermally-stimulated discharge current (TSDC) have been used to probe the quantity of stored charge and the energy levels where it resides in these dielectrics as a function of temperature.[41] Molinié and others have suggested that the presence of charge injection in the film over polarization is a function of the applied electric field strength.[44] In addition, infrared spectroscopy has been used to identify molecular-level changes of PVDF dielectrics,[45] indicating enhancement of CH_2 rocking modes consistent with an increase in polymer crystallinity.

In our group, Huang *et al.*[34] performed corona charging in air on a 1 μm-thick layer of poly(phenyl-methyl-silsesquioxane), a partially cross-linked glass resin (see Figure 1). In this study, x-ray photoelectron spectroscopy (XPS) did not identify any changes in chemical composition to suggest ion implantation, and contact-angle characterization of the films before and immediately after charging did not reveal any differences in surface hydrophobicity. Nevertheless, differences in the dielectric's effective surface potential of as much as |45 V| were observed, enabling controllable threshold voltage shifts of the same magnitude. Our group has also exploited corona charging in a number of device architectures, including dielectric bilayers.[46] Work by Deshmukh[43] utilized a dielectric bilayer of SiO_2 and Cytop, enabling stable charge trapping at the dielectric/dielectric interface. Scharnberg and others have also developed "dual-gate" architectures in which bottom gate/bottom contact pentacene OFETs were encapsulated with a Teflon electret layer that was charged to create a second static gate.[33]

Pre-polarization by Gate stressing

Post-fabrication approaches for modifying the V_T to enable low-voltage operation have sought to apply the reverse of a gate bias, polarizing the dielectric in a manner that decreases the $|V_G|$ required to switch the transistor. In a method developed by Katz *et al.,*[47] bottom-gate/top-contact n-type (**p-type**) OFETs were fabricated with an organic dielectric 1-2 µm thick. After fabrication, the source and drain electrodes were grounded and the gate was biased to a high negative (**positive**) voltage in the transistor's depletion regime. This large "charging voltage" is believed to draw minority carriers through the OSC towards the dielectric layer. There, they serve to neutralize majority-carrier traps present at the OSC-dielectric interface, so that subsequent application of V_G results in greater net accumulation of majority carriers at the OSC-dielectric interface that can contribute to I_D. The absolute shifts in the V_T of these devices, ranging up to |60 V|, contribute to the lower V_T. Similar use of a large V_G to pre-polarize the dielectric has been applied to OFETs with ferroelectric polymer dielectrics[48,49] and hydrophilic polymers such as PVA.[38,39]

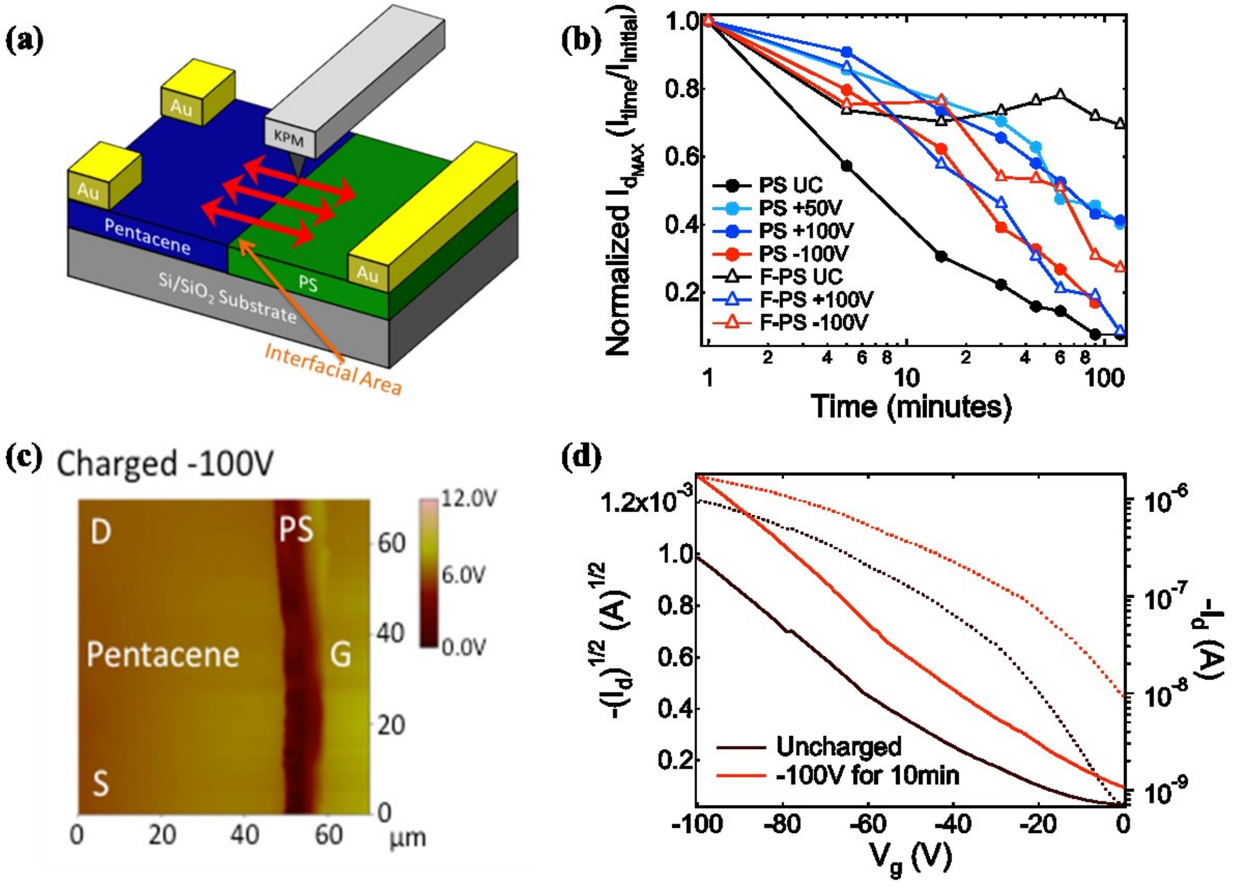

Figure 1.9 **(a)** Schematic of a lateral OFET structure in which interfacial potentials can be probed with scanning Kelvin-probe microscopy (SKPM). **(b)** SKPM surface potential image of lateral OFET, with S, D, and G labeling the Source, Drain, and Gate electrodes, respectively. **(c)** Decay of the V_T in lateral OFETs with pristine and pre-polarized polystyrene (PS) and poly(2-trifluoromethyl styrene) (F-PS) dielectrics. **(d)** Transfer curves for pristine and pre-polarized OFET with a PS dielectric shown in (b), indicating a decrease in the $|V_T|$ towards 0 V. Adapted images from Ref. 23.

A recent study by Dawidczyk *et al.*[50] applied scanning Kelvin-probe microscopy (SKPM) to the visualization of charge stored at the OSC-dielectric interface by this gate stressing method (Fig. 1.9). Fabricated using a previously-reported method,[51] layers of ~50 nm thickness of pentacene and PS were deposited laterally, with two top-contact Au electrodes spaced 250 μm apart and located equidistant from the junction. Application of a large voltage (200 V) between the electrodes resulted in a shift in the surface potential in the PS layer of more than 10 V over an extent of several μm into the PS layer, suggesting that these charges are within the dielectric material. In a follow-up investigation[23] we have fabricated lateral transistors using an analogous pentacene-PS-Au gate stack. Two-dimensional SKPM scans of the transistors revealed a polarization of the entire 3-15 μm lateral span of the organic dielectric. Furthermore, dielectrics consisting of poly(2-trifluoromethyl styrene) exhibited greater V_T stability than PS in the pristine state, while pre-polarization enhanced the V_T stability of PS relative to its fluorinated analogue. These data suggest a strong influence of molecular structure and steric effects on charge and/or polarization stability, consistent with previous studies.[45] Moreover, the correlation of greater V_T stability in polymers with HOMO-deepening fluorinated species is in agreement with recent theoretical studies of gate bias stress.[27]

Floating and Dual Gates

Another method that has achieved notable success in manipulating the V_T of OFETs has been the use of floating gates[52-54]. In the floating gate architecture, as shown in Fig. 1.10, an additional metal+dielectric layer is placed in series between the OFET gate dielectric and OSC layers. Upon application of a writing voltage, carriers may be written onto the floating gate layer via thermionic emission or tunneling, where they remain trapped between the floating gate metal and thin encapsulating dielectric. The effect of these trapped carriers on the floating gate is as a screening of the gate voltage, enabling a shift in the gate voltage required to turn on the OFET.

Architectures extended by Chan[55] and Murata[56] employ double- and triple-layer dielectric stacks in a gate stressing scheme to pre-polarize an organic dielectric, eliminating the floating gate metal and instead relying on states at the dielectric-dielectric interface for charge storage and V_T modification.

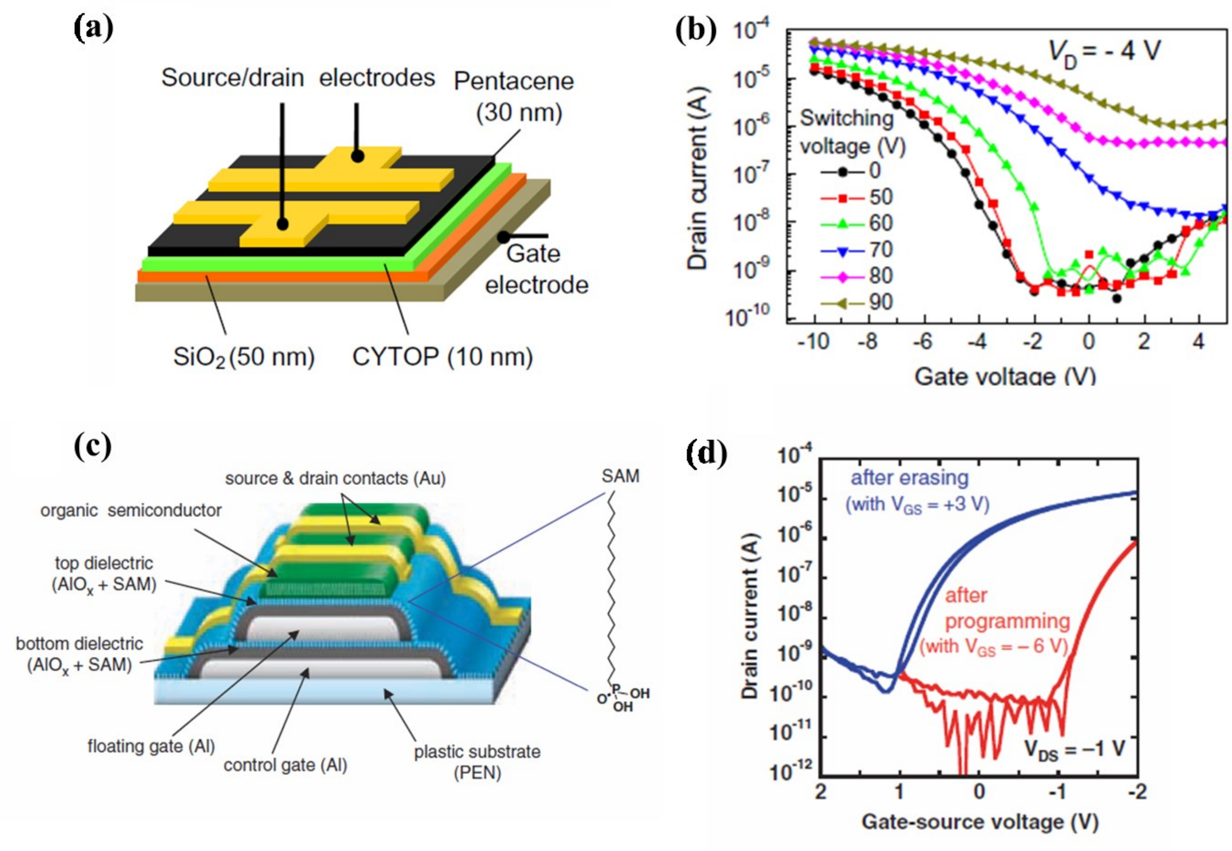

Figure 1.10 **(a)** Device diagram of a double-dielectric structure utilizing a CYTOP organic dielectric layer, and **(b)** transfer characteristics for various writing voltages in a p-channel OFET. Adapted images from Ref. 56. **(c)** Schematic of a floating gate structure using Al-AlOx for both device and floating gates, and **(d)** transfer characteristics for a p-channel OFET after programming and erasing steps. Adapted images from Ref. 52.

Self-assembled monolayers

As discussed previously, there are often significant constraints on the materials, processing parameters, and dimensions of dielectrics used in OFETs. In many cases the best solution may be to modify an existing dielectric surface to make OFET operation viable. An area of active research for dielectric enhancement is the use of self-assembled monolayers (SAMs). Although not a strict classification, SAMs are molecules that **(a)** form a covalent bond with a surface (in contrast to most Langmuir-Blodgett films) and **(b)** form an ordered single layer of molecules on said surface. It is important to note here that while grafted oligomers and brush polymers have also been used extensively to modify polymer and inorganic surfaces, they generally do not make well-ordered molecular layers, and as such fall outside the scope of this Account.

The processes used to adsorb SAMs on a surface should yield densely-packed, well-ordered layers, although OFETs with a glasslike organization of SAM headgroups has been reported.[57] The low molecular weight of most SAMs allows them to be deposited from either a vapor or solvent solution. For both processes, post-attachment annealing promotes layer crystallinity and structural stability at high post-processing temperatures[58] required for device fabrication. A notable method developed by the Bao group yields very smooth crystalline SAMs upon annealing in an ammonia vapor.[59]

The simple processing requirements for SAM modification of dielectrics have stimulated the development of a wide array of complementary dielectric-SAM systems that can be employed in OFETs. There are now a number of commercially available SAM molecules with reactive anchor groups compatible with attachment to the surface oxides of the most commonly used inorganic dielectrics, as shown in Table 1.1. In addition, a number of groups have designed platforms that enable the construction of multilayer SAMs. Among these, the Marks group has developed self-assembled nanodielectrics (SANDs),[60] which exploit a type of reaction pioneered by Katz[61] to build multilayer molecular dielectrics interconnected with metal oxide groups including SiO_2, Al_2O_3, ZrO_2, and HfO_2 groups. For a detailed description of the chemistry and materials selection criteria for SANDs we refer the reader to a recent Account on the subject.[62]

Table 1.1 Some of the most commonly used oxide dielectrics and compatible SAM anchor groups. For an illustration of SAND layers see Fig. 1.11.

SAM/Reactive Group	Surface
$-SiCl_3$, $-Si(OCH_3)_3$, $Si(OC_2H_5)_3$	SiO_2
-CO(OH)	SiO_2, Al_2O_3 ITO, ZTO
$-PO(OH)_2$, SANDs	SiO_2, Al_2O_3, ZrO_2, TiO_2, HfO_2

The interdependence of device properties like mobility and V_T on the surface energy and molecular disorder at the OSC-dielectric interface is well documented[9]. A recent investigation by Chung *et al.* examined the bond dipole difference between chemically similar octylphosphonic acid and octyltriethoxysilane SAMs, effectively decoupling the influence of OSC morphology on the electronic properties of the fabricated OFETs[63]. Moreover, properties of the SAM that influence V_T, such as the monolayer polarizability, depend on the cooperative interactions between individual molecules.[64,65] This observation has stimulated the investigation of the properties of mixed monolayers as a way to tune V_T controllably.[66-69] Recently, the Klauk group has demonstrated nearly continuous tuning of the threshold voltage in OFETs employing varying surface concentration ratios of octadecylphosphonic acid and its fluorinated counterpart.[70]

The use of dipolar SAMs to shift the V_T, as well as the nature of this V_T shift, has been the focus of numerous investigations.[71-74] To ascertain whether the SAM dipole induces charge in the OSC, Podzorov and coworkers have used electron spin resonance (ESR) to identify signatures of free electrons in single-crystal rubrene treated with FTS.[75] This V_T shift has been associated with a Helmholtz potential, V_{SAM}, that arises from the intrinsic dipole of the constituent molecule.[76] The Halik group recently investigated the role of this intrinsic dipole on the V_T shift for a broad range of dipolar SAMs and n- and p-type OSCs, and observed a linear relationship between the dipole moment and the shifted V_T.[77] Additionally, de Leeuw's group has demonstrated that a change in the trap density at the OSC-dielectric interface resulting from SAM modification is responsible for the observed V_T shift in OFETs.[78] The potential V_{SAM} has been measured using scanning Kelvin-probe microscopy,[79] and recently the Österbacka group and our own have applied charge extraction in a linearly-increasing voltage (CELIV) to measure V_{SAM} on native alumina.[80]

Our group has exploited the polarity of commercially available silanes to tune the V_T of OFETs.[81] Huang fabricated p-channel OFETs of 5,5'-bis(4-hexylphenyl)-2,2'-bithiophene (6PTTP6) on SAM-treated 300 nm-thick SiO_2, and observed V_T shifts as small as -5 V for the non-polar phenyltrimethoxysilane (PTS) and as high as +80 V for the dipolar perfluorodecyltrichlorosilane (FDTS). Leveraging the large V_T difference between the two

SAM-treated OFETs enabled operation of unipolar inverters with a switching voltage of -20 – 30 V and gains as high as 7, demonstrating the feasibility of single-OSC digital logic.

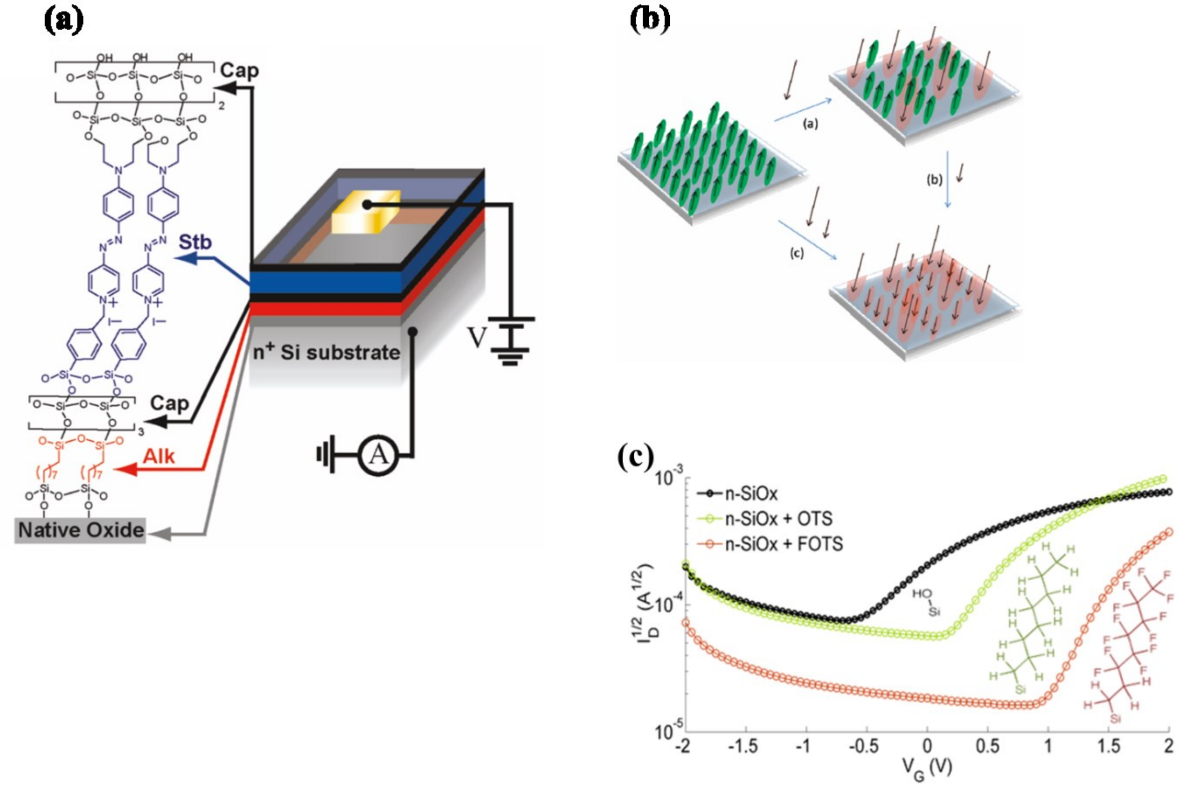

Figure 1.11 (a) A metal-insulator-semiconductor structure utilizing a self-assembled nanodielectric (SAND) consisting of alkyl and stilbazolium interlayers. Adapted image from Ref. 82. **(b)** Application of monolayers of OTS and FOTS to a nanoscale silicon oxide shifts V_T with increasing dipole magnitude, and results in a decrease of the subthreshold leakage for FOTS. Adapted image from Ref. 83. **(c)** Schematic illustrating the tunability of a substrate surface potential with mixed monolayers of opposite dipoles. Adapted image from Ref. 65.

In addition to modifying the V_T, our group has sought to address gate leakage, the unwanted current flow from gate to source or drain that contributes to a circuit's power consumption. We recently demonstrated the use of dipolar SAMs of octyl- (OTS) and perfluorooctyltriethoxy silane (FOTS) as electrostatic barriers for reducing leakage in n-channel OFETs fabricated on a marginal quality 10 nm SiO_2 dielectric.[83] Both SAMs were shown to reduce gate leakage by an order of magnitude, as compared to OFETs fabricated on bare oxide (Fig. 1.11). Most notably, comparison of OFF currents revealed that FOTS reduced subthreshold leakage by more than three orders of magnitude, while OTS only reduced it by an order of magnitude. In addition, the switching efficiency of the transistors was greatly increased by SAM modification. Analysis of this switching behavior indicated an increase in the trap density at the OSC-dielectric interface, consistent with recent reports by de Leeuw.[78] The reduction of subthreshold leakage with increasing molecular dipole—coupled with V_T shifts that follow the same trend—opens up new possibilities for the use of SAMs as interfacial tuning agents.

As discussed above, the threshold voltage can be influenced by parameters such as morphology and interface traps at the OSC-dielectric interface. Additionally, another interface that can influence the operating voltage of an OFET is that between the active layer OSC and the Source/Drain electrodes, the site of the contact resistance R_C. An increase in the R_c causes the requirement of a higher circuit driving voltage V_{DD} to ensure proper switching at subsequent circuit stages, and consequently also increases the power consumption of the circuit. When the materials at this interface have the same compositions and morphologies as the bulk regions of those materials, then the physical origin of the contact resistance[84,85] is an energy offset between the Fermi level of the electrode metal and the highest-occupied molecular orbital (HOMO) or the lowest-unoccupied molecular orbital (LUMO) of the OSC. This resulting voltage barrier is related to the change in work function of the electrode metal when an OSC is deposited thereon. On the other hand, when the OSC composition or morphology is different near the electrode interface, then the R_C element can be modeled as an OFET in its own right, in series with the main channel, and having its own mobility and V_T.[18]

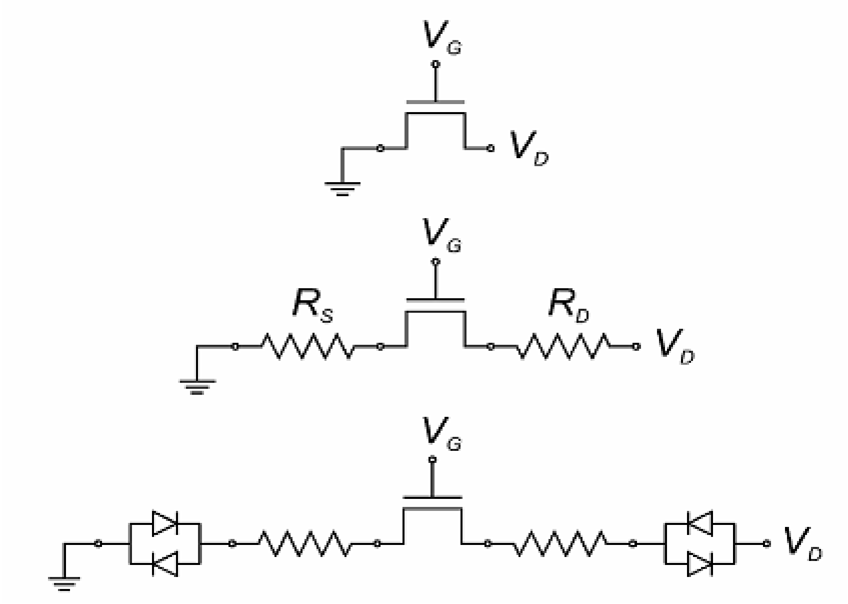

Figure 1.12 Circuit model incorporating contact resistances at source (RS) and drain (RD) electrodes. Diodes in series with contact resistances account for non-linear injection at the electrode. Image adapted from Ref. 18.

Several groups have employed SAMs to modify the contact resistance (Fig. 1.12) of p-channel OFETs in both bottom-gate/bottom-contact and top-gate/bottom-contact geometries.[86,87] In particular, the aforementioned chemical selectivity of SAM anchor groups enables controlled modification of source/drain electrodes without modifying the dielectric surface.[88] Our group has extended use of this SAM toolbox to n-channel NTCDI OFETs,[89] assessing the effect of both SAM-modified dielectrics and Au electrodes. Bottom-contact OFETs using electrodes treated with perfluorooctylthiols resulted in performance similar to top-contact OFETs, which typically exhibit superior performance.[90] De Leeuw and coworkers have used OFET structures to investigate Au electrodes treated with perfluorodecane- and perfluorohexadecanethiol SAMs, assessing their relative impact on morphology and contact resistance[91] In that work, it was demonstrated that the tunneling barrier seen by carriers traversing the SAM at the Au electrode was responsible for the increased contact resistance observed in OFETs with SAM-treated electrodes. A comparable method for treating electrodes to tune their work functions combines the advantages of polymer processing with the thin polarizable layers associated with SAMs. This method developed by Kippelen and coworkers exploits the degree of protonation in ultrathin aliphatic amine polymers spin-cast from different pH solutions to effect work function changes tunable by more than 1 eV.[92] Notably, this method overcomes the limitations of surface-specific binding required for SAM-treatment of electrodes, enabling the use of electrode materials inaccessible to direct SAM chemisorption. It is relevant to mention that while SAM site-specific binding may appear to limit their incorporation in devices with organic substrates, a successful chemical approach for SAM treatment of a poly(ethylene terephthalate) (PET) surface has been demonstrated by Xiang and coworkers[93] by creation of a polysiloxane layer onto which silane SAMs could chemisorb.

Physisorbed layers

Physisorbed interfacial layers can offer an additional degree of control over OFET device properties, and form an invaluable part of the device engineer's toolbox. These layers—typically deposited at the OSC-insulator, OSC-air, or OSC-OSC interface—can offer a straightforward method to tune the V_T via a charge-transfer layer.[94,95] Abe *et al*. deposited F_4-TCNQ, an organic acceptor, onto the surface of pentacene top-contact OFETs.[96] Controlling the relative length of the resulting charge-transfer layer as a fraction of the full transistor channel length enabled tunable shifts in V_T of more than 40 V. Similar doping schemes have been accomplished by evaporating a small-molecule dopant layer under the top-contact electrodes of pentacene[97] and graphene OFETs.[98]

In addition to organics, elemental layers can be used to tune OFETs. Recently, Ireland *et al*. used a thin layer of Te to modulate the mobility of both n- and p-channel top-contact OFETs fabricated on a 100 nm SiO_2 gate dielectric. The net effect of Te on the OFET was shown to depend on the interface where the layer was deposited. In NTCDI devices, 10 nm of Te sandwiched between the dielectric and OSC yielded p-channel transistors (in the NTCDI depletion region) similar to accumulation-mode Te devices with greater contact resistance[99], while overlaid Te on NTCDI yielded only accumulation-mode n-channel behavior. In OFETs with Te above 6PTTP6 the accumulation-mode was entirely ohmic—indicative of a heavily doped 6PTTP6 layer, in agreement with energy level alignment predicted in Fig. 1.13. Despite the marked differences in microstructure of Te on various OSCs, surface potential measurements of Te-treated pentacene and 6PTTP6 offer evidence in support of this hypothesis[100].

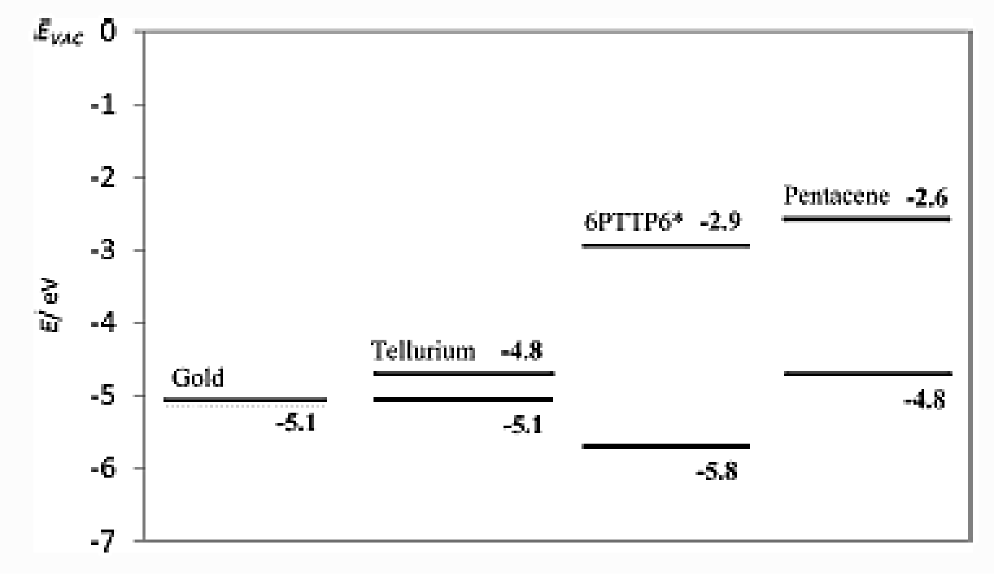

Figure 1.13 Vacuum-level energy band diagram for hybrid organic/Te OFETs. Image adapted from Ref. 100.

Challenges Ahead and Outlook

Although each of these methods offers unique ways to modify device properties, their viability beyond the laboratory in large-scale, high-throughput fabrication of OSC-based electronics must also be considered. The corona method has enabled mass-production of electrets for audio applications, but integration with circuit fabrication presents a few challenges. First, because corona charging is routinely done in an air environment, its effectiveness is highly dependent on relative humidity[101] and charging temperature,[102] placing restrictions on post-charging fabrication processes. In addition, the corona itself only extends a few mm radially from the top point electrode. To address this particular issue, our group has demonstrated a direct-write technique for implanting charge using a low energy electron beam,[43] analogous to corona charging. However, this writing procedure is by nature a serial process, and will require additional engineering to meet the needs of high-throughput fabrication methods.

Gate stressing, by comparison, has the advantage that the method is independent of any particular fabrication technique, and could be applied using high-throughput stamping. The challenges associated with its full-scale implementation center on circuit design, as the writing of the V_T demands additional logic stages that can access a high driving voltage V_{DD} to write to the OFET gate. This arrangement is suitable in organic memories,[47] but still relies on complementary gates with stable V_T. Fabrication of multi-stage logic blocks that leverage the addressability of field-programmable gate arrays (FPGAs) could make this technique viable for high-sensitivity analyte sensors.

SAMs may offer the most practical solution for writing the V_T of many gates simultaneously. Zhu and coworkers have employed spiropyran SAMs with light-switchable dipoles that enable optical control over the threshold voltage,[103] making possible large-scale optical memories. Fabrication methods that integrate the ability to tune both n- and p-channel OFETs with adsorption of a single dipolar SAM moiety will come at the cost of additional processing steps. Fortunately, the development of low temperature solution processes may enable roll-to-roll processes in which SAM modification entails only marginal addition of processing equipment. Additionally, the broad materials palette available to newly-developed polymer-based methods for modifying device electrodes may prove even better candidates for integration with organic and hybrid electronic device fabrication.

Ultimately, refining our understanding of the physical mechanisms that underlie each of these methods will allow us to harness their full potential to independently tune the V_T, mobility, and leakage currents in OFETs, and direct us towards the clearest path to bringing OFET-based electronics into the mainstream.

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Chapter 2 : Reducing Leakage Currents in n-Channel Organic Field-effect Transistors Using Molecular Dipole Monolayers on Nanoscale Oxides

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Introduction

Organic field-effect transistors (OFETs) are often touted as flexible, low-cost alternatives to silicon technology where the device area need not be microscopic. Applications where OFET circuitry might be useful, such as in mass produced displays[1,2], radio-frequency identification tags[3,4], and sensors[5,6], often require that power consumption and input voltage be minimized. However, the typical OFET test architecture—the organic semiconductor (OSC) film on 100-300 nm of SiO_2 deposited on a conductive Si gate with >100 µm spacing between source and drain electrodes—requires tens of volts to achieve effective switching. In the last decade, many groups have studied high–capacitance dielectric layers in order to decrease operating voltages and enable closer source-drain separations than are typical for Si-SiO$_2$ substrates[7]. They used very thin amorphous polymers[8], monolayer-treated[9-12] or polymer-treated inorganic dielectrics[13], polymer electrolyte dielectrics[14], and high-k inorganic dielectrics[15]. An ultimate solution would be to produce OFETs from single layers of molecules that include both a dielectric side chain and a conjugated subunit; this has been attempted previously,[16,17] and we have recently reported the first demonstration of OSC molecular segments within a multilayer film contributing to gate capacitance, acting substantially as gate materials in series with very thin oxide films.[18] Still, the apparently insufficient dielectric strength in those devices allowed considerable gate leakage current and limited the ON/OFF ratio. It is not known whether this leakage was the result of pinhole defects in the oxides or dielectric breakdown.

Although flexible substrates with a variety of metal/dielectric systems have been developed for organic electronics applications, the Si-SiO$_2$ platform remains attractive for organic semiconductor device testing and characterization because of its flatness, standardization, and relatively dense oxide coverage compared to alternative ultrathin dielectric films on metals. Another advantage is the ability to functionalize the oxide surfaces with monolayers that can tune surface energy and local electric fields. When degenerately doped, Si is sufficiently conductive to allow easy equilibration of remotely applied gate voltages (V_G) with arrays of OFETs. However, based on our previous observations, thin oxides grown from highly-doped wafers yield less-insulating dielectrics than do thicker or chemical vapor-deposited SiO$_2$. High gate leakage has a detrimental effect on transistor performance, resulting in high OFF currents, low ON/OFF ratios, and increased power consumption, all of which negate the potential advantages of low-power OSC-based electronics. As a result, reducing the gate leakage in thin bottom gate-top contact OFETs is a technological priority for the study and development of OSC-based devices. In this paper we discuss the use of dipolar silane self-assembled monolayers (SAMs) to reduce the gate leakage in a thin-oxide OFET fabricated on highly-doped silicon, as illustrated in Figure 2.1. While other examples of SAMs used to shift OFET threshold voltages (V_T) have been reported by us and others[19-21], this is the first study of a SAM dipole being used specifically to lower gate leakage current. We employed two organosilanes, OTS and FOTS, with calculated gas-phase dipoles[22] of -0.31 D and -3.49 D, respectively. An explicit contribution of the SAM dipole to the lowering of this current is demonstrated. We chose to work with an electron-transporting OSC, namely 8-2-Bn naphthalenetetracarboxylic diimide (NTCDI, Fig.

1.1b) to further bolster our understanding of this class of compounds, as they are particularly crucial for complementary organic logic circuits[23-25]. We also noted a surprising difference in the effect of one of the silanes on n-Si versus p-Si oxides. Conclusions drawn from this work will be applicable to dielectric films made from other materials with nanoscale thicknesses, including other metal-oxide combinations and polymers, which have been recently shown to be amenable to work function tuning by surface modification with SAMs[26].

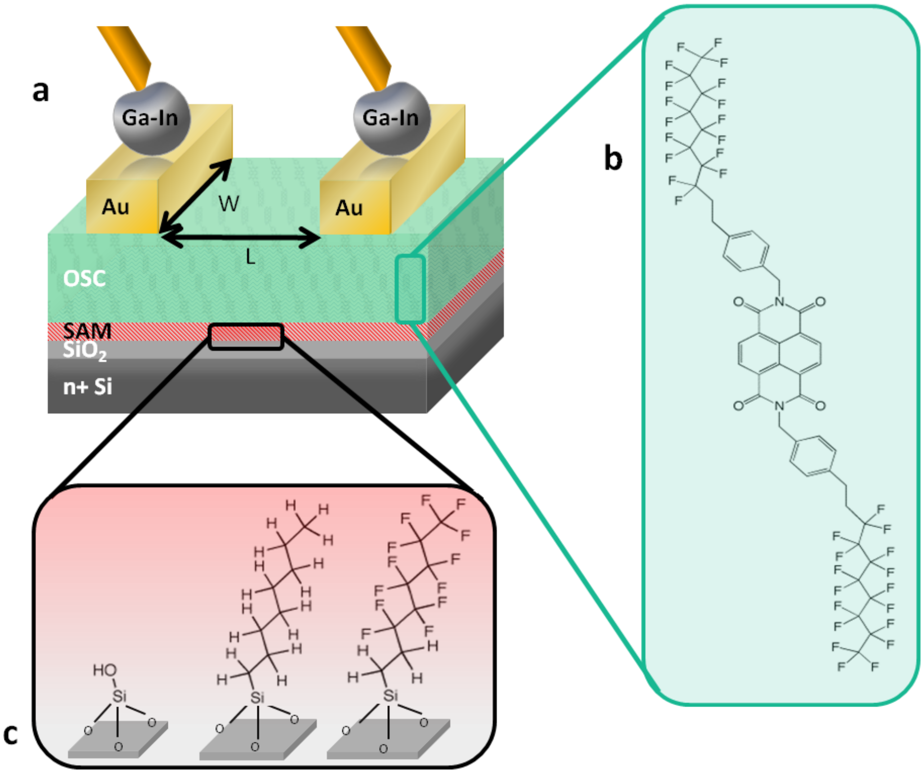

Figure 2.1 Experimental platform for probing the effect of a molecular dipole. **(a)** OFET fabricated on a plasma-grown 10 nm minimal oxide with a SAM at the dielectric/OSC interface. **(b)** Chemical structure of 8-2-Bn NTCDI. **(c)** Bare oxide and SAM-functionalized oxide with OTS and FOTS.

Results and Discussion

OFET Device Performance

Typical output curves of OFETs on thin plasma-grown oxides are shown in Figure 2.2. Devices were fabricated in four separate experiments with 8-2-Bn, and device performance was reproducible and consistent with what is presented herein. In addition, OFETs fabricated with 8-0-Bn, a shorter NTCDI moiety with no CH_2 groups between the fluorocarbon and phenyl groups[18], displayed similar trends in output and leakage. Devices with different W/L ratios exhibit similar trends as those reported here for W/L=53.3. Bare n-Si oxide devices exhibit gate leakage currents of 88 nA with a 2 V potential between gate and source terminals. Taking the area through which the source-gate current flows to be the area of one electrode and half of the channel, and a thickness of 10 nm for the oxide, these values correspond to leakage current densities of 2.6 μA cm^{-2} at 2 MV cm^{-1}. While these leakage currents and electric fields are below those expected for dielectric breakdown, this relatively high leakage may be the result of tunneling across the oxide, possibly enhanced by the high concentration of dopant atoms within the oxide and at the Si/oxide interface.[27] The leakage currents in the ON state are roughly an order of magnitude lower than the ON currents, indicating that the ON current is primarily lateral, even with this minimal dielectric. The gate leakage currents (I_G) at zero drain voltage (V_D=0, intercept of the curves with the vertical axis) are reliable values because at that biasing condition $V_D = V_S$, and therefore the lateral OFF current is zero. The value of I_G when V_D=2V is complicated by the difference in electrode-gate potentials near the source and drain, respectively, and by possible charging currents. Notably, the bare oxide devices did not show saturation with V_G at 2 V, though we will see shortly that the SAMs enabled saturation under this condition.

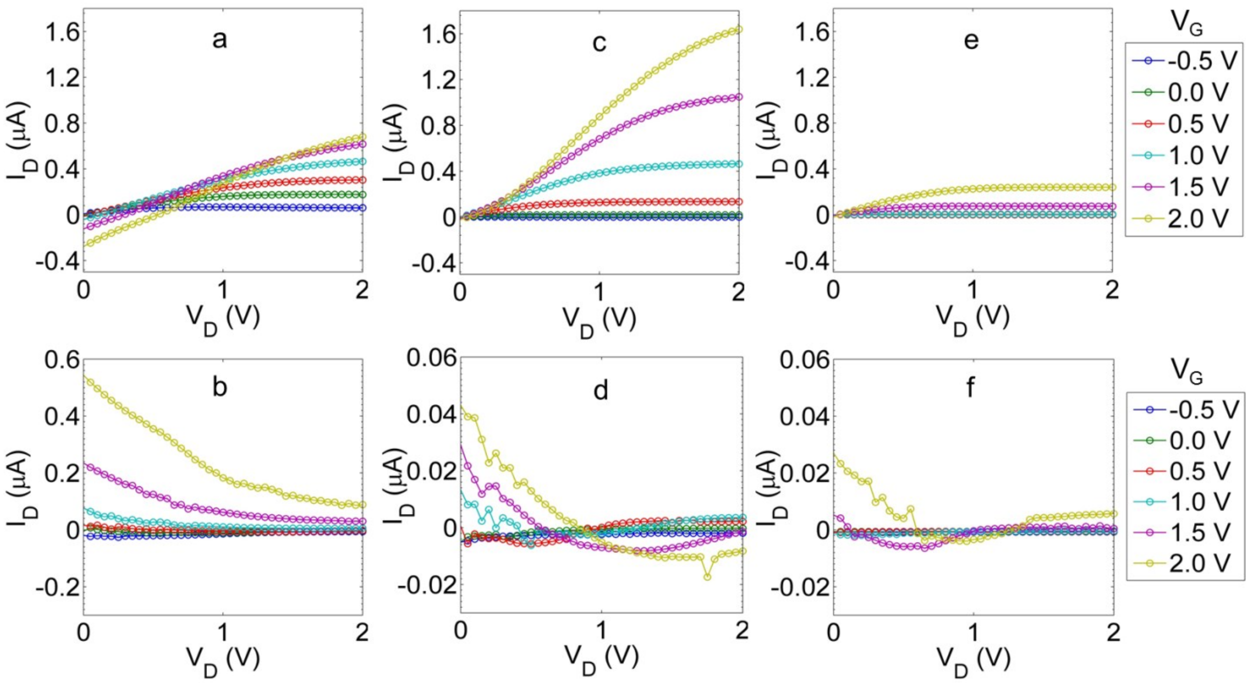

Figure 2.2 Output (top panels) and leakage (bottom panels) characteristics of 8-2-Bn NTCDI OFETs fabricated on highly-doped n-type silicon with 10 nm plasma-grown oxide. **(a-b)** Devices on bare oxide. **(c,d)** Devices on OTS. **(e,f)** Devices on FOTS; inset shows rescaled output curve. Each curve is of data from averages of three devices on the same substrate for each wafer type. Device W/L ratio is 53.3. Note that the scale for b is 10x the scale for d and f.

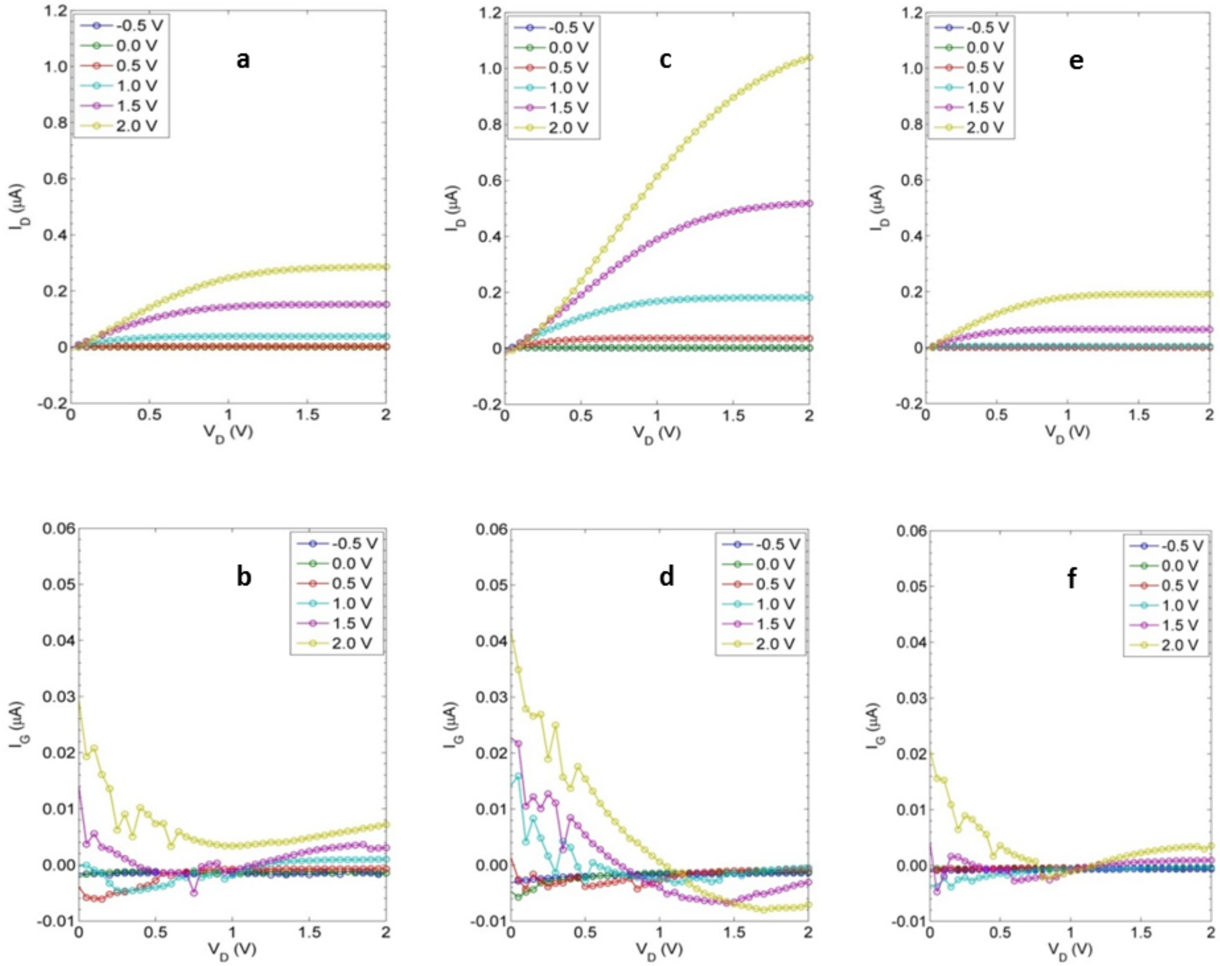

Figure 2.3 Output (top panels) and leakage (bottom panels) characteristics of 8-2-Bn NTCDI OFETs fabricated on highly-doped p-type silicon with 10 nm plasma-grown oxide. **(a-b)** Devices on bare oxide. **(c,d)** Devices on OTS. **(e,f)** Devices on FOTS; inset shows rescaled output curve. Each curve is of data from averages of three devices on the same substrate for each wafer type. Device W/L ratio is 53.3.

Addition of OTS and FOTS at the n-Si-oxide/NTCDI interface has a significant effect on device output and gate leakage currents, as seen in Fig. 2.2(c-f). Relative to the bare oxide, OTS treatment results in increased output current, while addition of FOTS decreases output current. Experiments on p-type silicon (Fig. 2.3) show a similar trend in output current, though leakage current is observed to increase slightly for OTS devices; this observation is addressed in further detail in Chapter 3. The trends for both output and leakage in n- and p-type silicon were observed in numerous iterations of this experiment. The FOTS trend was also observed on devices fabricated on 100 nm thermally-grown SiO_2 (Figure 2.4).

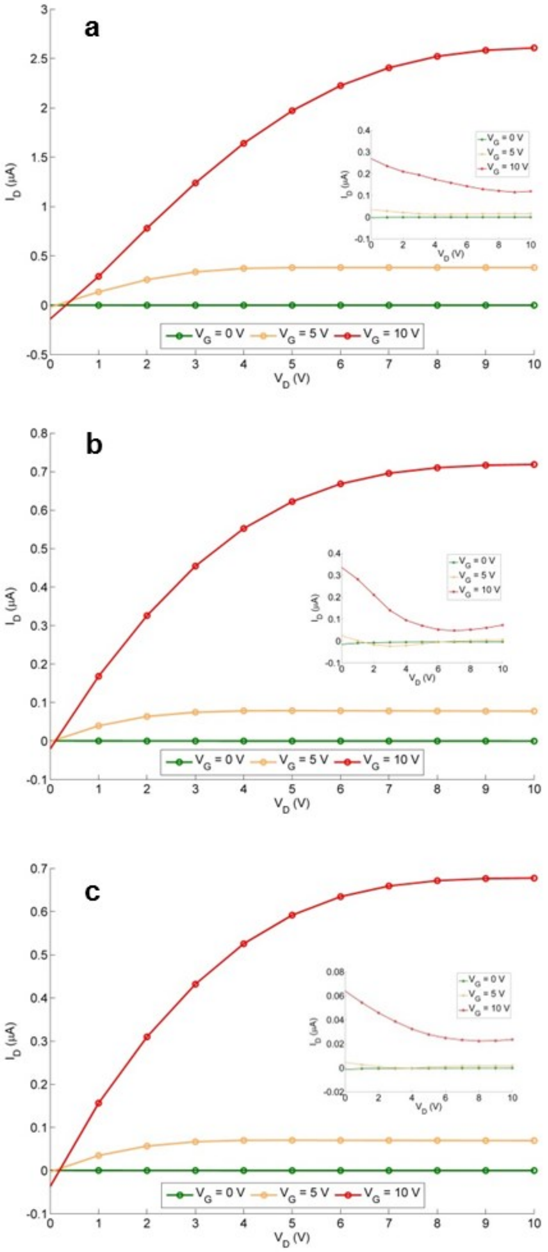

Figure 2.4 OFETs fabricated with 8-2-Bn NTCDI on highly-doped nSi with 100 nm thermally-grown oxide with **(a)** no treatment and SAM treatments of **(b)** OTS and **(c)** FOTS. Insets display leakage current.

One factor that could have accounted for these OFET performance differences is the quality of the first few OSC layers[28], where most of the field-accumulated charge resides in the OFET channel[29]. Images of NTCDI films of 40 nm thickness captured with AFM show similar morphology on the three kinds of dielectric surfaces (Fig. 2.5). However, 40 nm corresponds to approximately 11 monolayers of 8-2-Bn NTCDI, raising the possibility that AFM is portraying a morphology not exactly indicative of the dielectric interface[30]. To ascertain how much the SAM treatments influenced the growth and morphology of the bottom-most layers, samples with 15 nm (~4 monolayers) of NTCDI were vacuum deposited. AFM Images (Fig. 2.6) show bare oxide and FOTS surfaces leading to similar NTCDI domains, whereas OTS surfaces resulted in slightly larger NTCDI grains, consistent with observations reported elsewhere for OSCs on OTS-treated surfaces[31]. It is likely that the greater connectivity of the NTCDI on OTS-treated oxide is responsible for the larger output current in our OTS transistors.

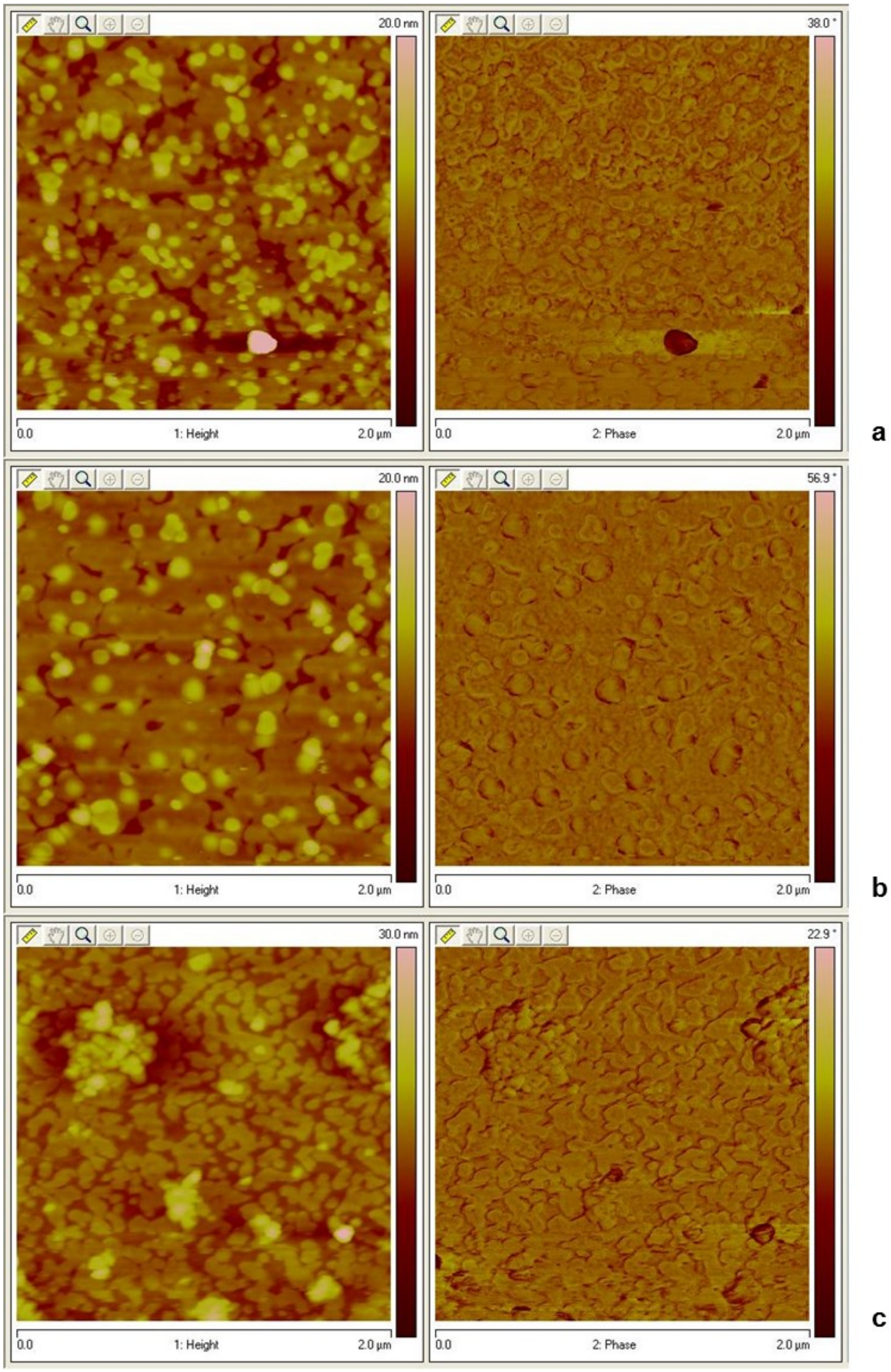

Figure 2.5 AFM height and phase images of 15 nm of 8-2-Bn NTCDI on n-Si. **(a)** NTCDI on 10 nm oxide. **(b)** NTCDI on OTS-treated oxide, displaying a large degree of connectivity between grains. **(c)** NTCDI on FOTS-treated oxide. NTCDI growth tracks underlying oxide hillocks.

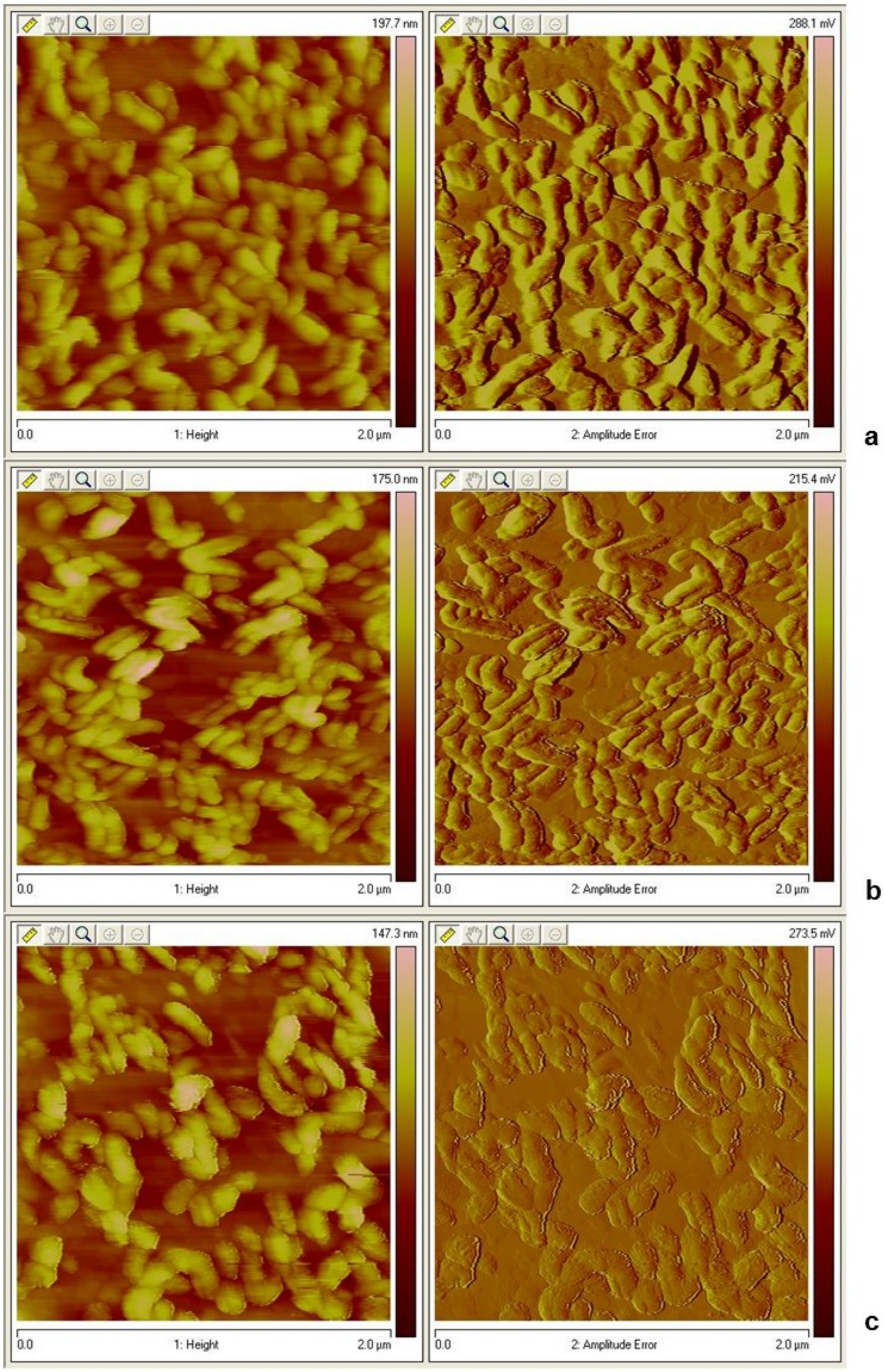

Figure 2.6 AFM height and amplitude error images of 40 nm of 8-2-Bn NTCDI on n-Si.**(a)** NTCDI on 10 nm oxide, showing a high degree of polycrystallinity. **(b)** NTCDI on OTS-treated oxide. **(c)** NTCDI on FOTS-treated oxide. Amplitude error images of SAM-treated oxides show underlying patches of NTCDI islands.

The addition of SAMs to the n-Si-oxide surface results in a substantial reduction in leakage for both OTS and FOTS devices. Comparison of Figs. 2.2(b, d, f) indicates that FOTS-treated OFETs display weaker gate voltage dependence of gate leakage than either bare oxide or OTS-treated devices. To elucidate leakage current details, we consider four device operation regimes representative of electronic logic biasing. Hereafter, the ON state refers to the regime where the gate voltage is high (V_G = 2 V). The source voltage is always grounded (0 V), and the drain voltage V_D is held at 2 V. The first leakage current we examine is the ON state gate leakage, which arises from the source-gate potential difference. Both OTS and FOTS decrease the ON gate leakage by 15-20x as compared to bare oxide devices. The second leakage current of interest is the case where V_G is 0 V—where the effective bias is between the drain electrode and the gate—this biasing condition is the reverse of that for the ON state gate leakage.

As compared to bare oxide, both SAM treatments result in a comparable 6x reduction in OFF state gate leakage. The similar leakage reduction in the ON state for both SAM treatments suggests this leakage is reduced simply by the addition of dielectric material to the total gate thickness. We also examined the gate leakage with a small negative gate voltage. Under this biasing, OTS treatment reduces leakage by a factor of 3, whereas FOTS reduces this leakage by nearly one order of magnitude. The observation of only a marginal increase in the gate leakage for FOTS devices as a result of changing the gate voltage from 0 V to -0.5 V, compared to a 6x increase for OTS devices, is consistent with the effect of a larger dipole on FOTS limiting the flow of electrons from gate to drain. Similar magnitudes and trends in leakage current were observed in n-SiOx-Au diode structures. Finally, we investigate the sub-threshold drain leakage, which is the drain current in the V_G = 0 V state, and is a combination of source-drain and gate-drain currents. Sub-threshold leakage is reduced by an order of magnitude with OTS, and by more than 400 times with FOTS. This leakage reduction for FOTS is remarkable considering that ON output currents for these OFETs were fully half of that of bare oxide devices. This effect has never been explicitly utilized to enable and enhance low-voltage OFET switching.

Table 2.1 Leakage currents in n-channel NTCDI OFETs on bare and SAM-treated n-Si and p-Si oxides. I_G currents are gate leakage under several biasing conditions. [1]OFF drain current measured from I_D-V_D curves. [2]OFF drain current measured from I_D-V_G curves.

OFET dielectric/ (nA)	I_G – ON	I_G – OFF (V_G = 0 V)	I_G – OFF (V_G = -0.5 V)	I_D – OFF[1]	I_D – OFF[2]
n-SiOx	88	-2.9	-6.1	176	479
n-SiOx + OTS	-3.7	-0.3	-1.9	17.5	3.5
n-SiOx + FOTS	5.7	-0.5	-0.7	0.4	0.4
p-SiOx	7.2	-1.5	-1.5	0.2	1.1
p-SiOx + OTS	-7.1	-1.2	-1.4	2.1	5.4
p-SiOx + FOTS	3.5	-0.4	-0.7	0.3	0.2

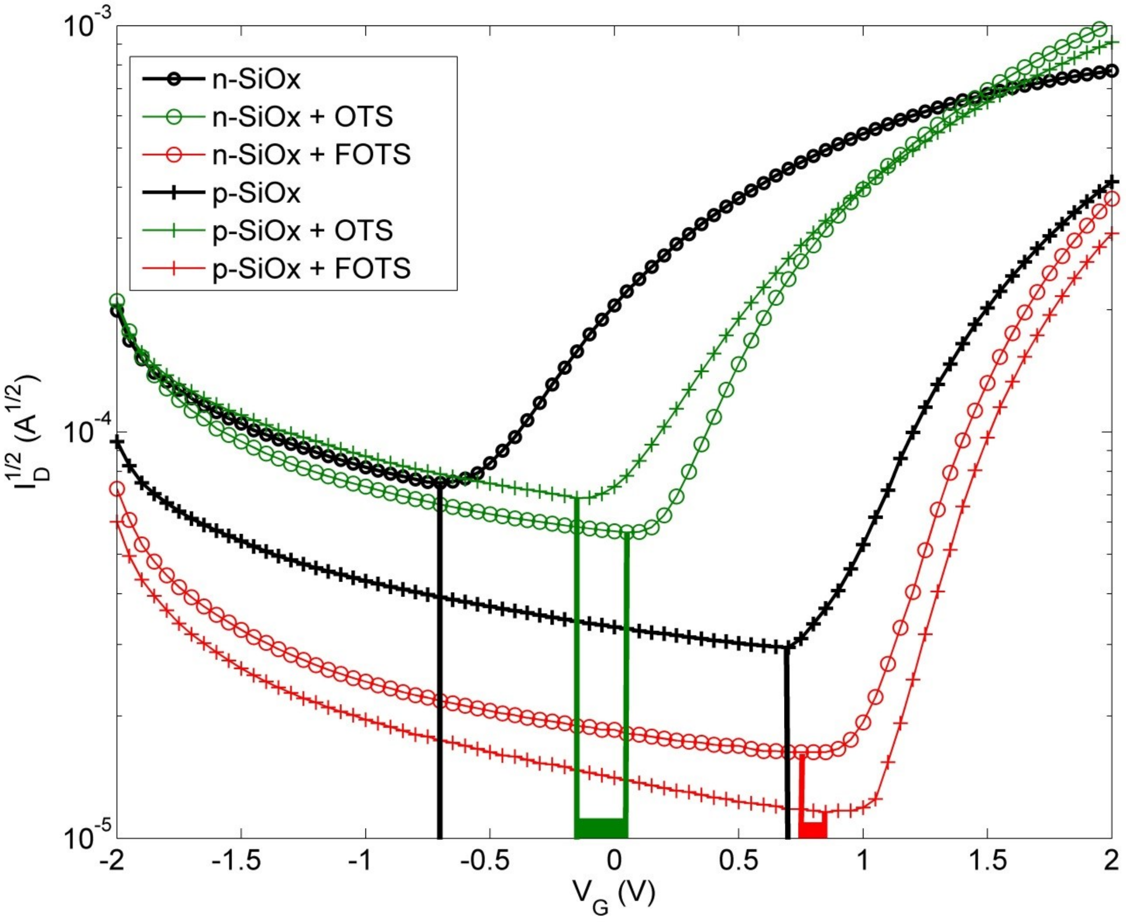

Figure 2.7 Effect of a molecular dipole on sub-threshold leakage. $I_D^{1/2}$ vs. V_G plot for OFETs with bare oxide, OTS, and FOTS on n-Si and p-Si. Vertical lines for bare oxide (black), OTS- (green), and FOTS- (red) treated OFETs show similar turn-on voltages for SAM-treated OFETs.

Threshold Voltage Shifts

Surface treatments with OTS and FOTS also result in noticeable (and for FOTS, expected) shifts in the threshold voltage V_T, as shown in Fig. 2.7. Threshold voltages were extrapolated from square-root transfer curves, over a linear region of 0.5 V above the turn-on voltage. This method ensured that the extrapolated threshold voltage was not influenced by contact resistance at higher voltages, where the slope of the plot deviated from linearity. Bare oxide OFETs on n-Si displayed V_T = -0.58 V, while V_T = +0.21 V for OTS, and V_T = +1.25 V for FOTS. These data indicate that addition of SAMs at the n-Si/dielectric interface turns devices more OFF, and suggest that the lower sub-threshold leakage in SAM-treated devices is related to this threshold voltage tuning. The increase in V_T and decrease in ON output current for FOTS devices is consistent with this interpretation. Figure 2.7 shows that although OTS devices turn on at more positive voltages, their sub-threshold leakage in the depletion regime ($V_G < 0$) is nearly identical to that of bare oxide. By comparison, FOTS devices have an order of magnitude lower sub-threshold leakage. It is possible that the marginally better quality of the NTCDI film on OTS may result in a greater number of mobile carriers at the OSC/dielectric interface, negating the effects of the OTS dipole. Nevertheless, there appears a net effect of the larger FOTS dipole on the leakage characteristics of our n-channel OFETs.

The trend established for n-Si devices alone would suggest that the greater magnitude of the FOTS dipole results in a larger threshold voltage shift versus bare oxide than does OTS, but in the same direction. However, OFETs on p-SiOx display threshold voltages for bare oxide (V_T = +1.03 V) that are between OTS- (V_T = +0.24 V) and FOTS- (V_T = +1.29 V) treated oxides. The effects of OTS on gate leakage current are also different for p-SiOx compared to n-SiOx. To understand why the OTS dipole effects for p-SiOx differ from that observed for n-SiOx, we first address the differences between the bare oxide surfaces. The difference in turn-on voltages for our OFETs on n-Si and p-Si devices of roughly 1.5 V arises from their respective Fermi level alignment with the top Au (source/drain) electrode in the MIS cross-section of the OFET device. This shift, though slightly larger, is in reasonable agreement with recent results from Yaffe[32] *et al.*, in which a 1.1 V difference between highly-doped n- and p-Si diodes with a single alkyl SAM as a dielectric was observed.

Qualitatively, the discrepancy in the direction of the V_T shift (and the difference in effects on leakage current) for devices fabricated on SAM-treated n-SiOx and p-SiOx appears at odds with the notion that a surface-attached molecule acts purely as an electrostatic dipole; under that assumption, we would have expected OTS to also shift the V_T of devices on p-SiOx more positive. Instead, Fig. 2.7 shows that devices made on both OTS- and FOTS-treated SiOx display very similar switching characteristics regardless of whether the underlying substrate is n-Si or p-Si. These data appear to suggest that a factor other than the silane-chain dipole makes an additional contribution to SAM-induced V_T shifts. We hypothesize that the SiOx-organosilane bonding itself makes a separate contribution to the silane-induced surface dipole, and that this contribution is different for OTS on n-Si and p-Si, while the contribution of the in-chain dipole of FOTS is similar on both oxides.

Finally, we attempted Kelvin-probe microscopy (SKPM) experiments to measure the surface potential differences between bare and SAM-treated oxides. We observed potential differences of -150mV to -200 mV for both OTS and FOTS surfaces relative to both n-SiOx and p-SiOx, though the uncertainties among them were on the order of 100 mV, likely due to differences in humidity or surface contamination in our open-air system. The sign of this voltage, which we obtained in three separate experiments including different surface preparation processes (as explained in the Experimental Section) would be consistent with the effects of the silanes, except for the exceptional case of OTS on p-Si, where the silane-oxide bonding contribution may be somehow compensated in the SKPM experiment. A vacuum SKPM study performed with the NTCDI layer deposited on the substrates will be the topic of a future investigation of the SAM-OSC interfacial dipole.

Switching Behavior

Devices treated with OTS and FOTS show *much better switching characteristics* than devices on bare oxide, as evidenced by their improved sub-threshold swing ($S_{s\text{-}th} = \partial V_G/\partial lnI_D$) and reduced gate leakage. Table 2.2 summarizes these results for three devices on each surface treatment; sets of devices with smaller W/L ratios, all fabricated in parallel, exhibited similarly dampened gate leakage and switching characteristics effected by dipolar SAMs. As seen in Fig. 2.7, the sub-threshold swing $S_{s\text{-}th}$ for FOTS-treated devices is more than 1200 mV/dec lower than for bare oxide devices, and more than 700 mV/dec lower than OTS devices, indicating a smaller voltage range transition from intrinsic to field-effect mobility in the OFET channel. In addition, SAM-treated devices exhibit an increase in the voltage range between V_T and their turn-on voltage V_{to}. The increase in this voltage difference $|V_T - V_{to}|$ with SAM treatment has been reported previously[19], and is associated with an increase in the trap density at the dielectric/SAM interface[33,34], which—along with the interface dipole—contributes to the lower gate leakage in addition to the interface dipole. The trap density N_{trap} can be estimated as $N_{trap} = C_i|V_T – V_{to}|/e$ where C_i is the specific capacitance of the dielectric, and e is the fundamental charge. The values of C_i for each of the three surfaces—shown in Table 2.2—are the average of twelve devices, fabricated with 50 nm gold contacts using the same shadow masks as for OFET source/drain electrodes. For bare oxide devices we find a trap density $N_{trap,bare} = 4.9\text{x}10^{10}$ cm^{-2}. By comparison, SAM-treated oxides yield trap values of $N_{trap,OTS} = 1.2\text{x}10^{11}$ cm^{-2} and $N_{trap,FOTS} = 3.0\text{x}10^{11}$ cm^{-2}. However, we caution that estimation of the trap density in the bare oxides, given their relatively large leakage currents and small potential differences $|V_T - V_{to}|$, may require a more comprehensive treatment of dopant gap levels in the thin oxide. It is reasonable to say that at the very least, SAM treatment enables better estimation of the dielectric interface trap density.

Unlike in devices fabricated on thick oxides, the relatively high leakage in our OFETs precludes an analysis of the transistor channel conductivity that excludes the contribution of the gate leakage to the drain current. In Fig. 2.8 we present the currents associated with the square-root transfer curves of Figs. 2.3 and 2.4: drain (I_D), gate (I_G), and source (I_S). During these measurements, $V_D = 2$ V, and the gate was swept from -2 V to +2 V. We see that for n-SiOx transistors, in the OFF state the gate current $\mathrm{I_G}$ remained a factor of 2 higher than I_D and I_S. Upon reaching the threshold voltage at roughly -0.6 V, both I_D and I_S were larger than I_G by nearly one order of magnitude, with this difference becoming smaller as the gate voltage approaches 2 V (note that near $V_D = 2$ V, the drain-gate voltage approaches zero as V_D increases). This decreasing difference in current is observed in the output curves of Fig. 2.2(a), in which the OFETs fail to reach saturation due to increased leakage.

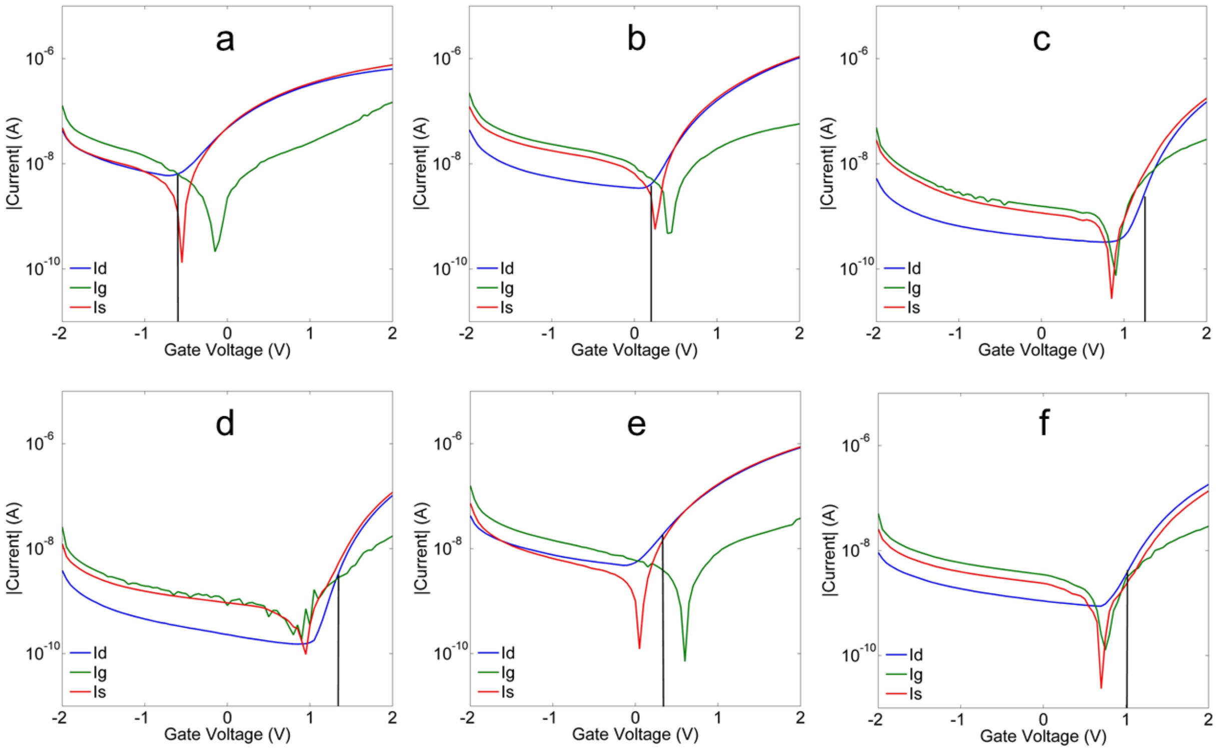

Figure 2.8 Terminal currents for high-leakage OFETs on n-SiOx (top panels) and p-SiOx (bottom panels). **(a-c)** Devices on bare, OTS-, and FOTS- treated n-Si oxide, respectively. **(d-f)** Devices on bare, OTS-, and FOTS-treated p-Si oxide. Vertical lines indicate the V_T as listed in Table 2.2.

By comparison, both OTS- and FOTS-treated oxides exhibit OFF-state currents I_S and I_G of comparable magnitude which are a factor of 5 larger than I_D. In addition, the value of I_G for the SAM-treated oxides is lower than for bare oxide devices. In the ON state, I_D and I_S are of the same magnitude, and increase at a faster rate than I_G. This observation is consistent with the improved saturation behavior of the SAM-treated OFETs on n-SiOx. For p-SiOx devices, FOTS reduced leakage and improved saturation, while devices on OTS display larger I_G for negative gate bias. For both bare and SAM-treated oxide devices, V_T corresponds to the voltage at which the source-drain current increases rapidly relative to the gate current.

Due to the ~1 eV work function difference between n-Si and Au, electrons accumulate at the oxide/NTCDI interface at equilibrium. Any additional negative surface charge on the oxide due to a SAM-dipole would serve to deplete electrons from the oxide+SAM/OSC interface. This effect manifests itself as an increase in the effective n-SiOx work function, moving further from vacuum towards that of p-Si. Comparison of the current characteristics of n-SiOx+FOTS and bare p-SiOx transistors in Figs. 2.8(c, d) supports this hypothesis, as their currents and switching behavior more closely resemble each other.

In the case of p-channel OFETs on an OTS- or FOTS-treated oxide, we expect to observe incremental accumulation of holes at the oxide interface, consistent with reports by Huang[20], Chung[12], Takeya[35], and others. Our observations indicate that while some gate leakage is reduced by simply adsorbing an alkyl to the oxide, the gate and subthreshold leakage decrease with increasing depletion in the channel due to the SAM dipole. As a result, we expect that reduction of leakage current using a dipolar SAM should be extendable to p–channel OFETs by employing a SAM with a positive dipole like aminotripropyl silane, which would deplete the channel of holes at the oxide/OSC interface.

Capacitance measurements

Capacitance values for Si/oxide/Au and Si/oxide+SAM/Au structures are shown in Table 2.2. Deviations in these values from ideal thickness dependences may reflect variations in oxide thicknesses, and are not important to the main conclusions of the paper. A more suitable metric that does not require the MIS-measured capacitance values is sheet transconductance, given by the mobility × capacitance product μC. This figure-of-merit has been used to compare performance of OFETs across various material and processing parameters[13]. Sheet transconductance, as well as threshold voltage V_T and μ_{meas}, were extrapolated from $I_D^{1/2}$ vs. V_G plots using the saturation-regime equation for drain current in an FET: $I_D = \mu C(V_G - V_T)^2 W/2L$.

Sheet transconductance is two times greater for OTS and FOTS-treated devices on n-SiOx, while the transconductances are approximately equal for the three p-SiOx transistors. This increase in μC on SAM-treated n-SiOx reflects an enhancement of charge carrier accumulation, likely resulting from a reduction in carriers lost at the OSC/dielectric interface to leakage current. Notable for a single SAM layer on thin oxide, these transconductance values are comparable to reported multi-layer SAM-on-native oxide OFETs.[36]

Table 2.2 Comparison of OFET device parameters for bare and SAM-treated oxides. Threshold voltages, mobility μ_{meas}, and sheet transconductance values were extrapolated from $I_D^{1/2}$ vs. V_G plots. Specific capacitance was measured at 100 Hz, using an electrode area of $3.03\text{x}10^{-2}$ cm^2. ON/OFF ratios were measured from V_{to} to 2 V. Device W/L ratio is 53.3.

Surface	V_T (V)	$S_{s\text{-}th}$ (mV/dec)	$\mu C/A$ (10^{-9} S/V)	μ_{meas} ($10^{-2}cm^2/Vs$)	C_i (nF/cm^2)	ON/OFF (from V_{to})
n-SiOx	-0.58 ± 0.12	1480	4.4 ± 0.3	2.1 ± 1.0	192 ± 17	106
n-SiOx + OTS	$+0.21 \pm 0.03$	607	9.4 ± 0.4	4.7 ± 1.9	131 ± 53	303
n-SiOx + FOTS	$+1.25 \pm 0.04$	230	9.0 ± 0.6	4.5 ± 2.5	103 ± 16	460
p-SiOx	$+1.03 \pm 0.11$	360	9.1 ± 3.6	3.0 ± 1.6	188 ± 5	208
p-SiOx + OTS	$+0.36 \pm 0.06$	544	11.0 ± 3.7	3.9 ± 1.3	149 ± 4	175
p-SiOx + FOTS	$+1.29 \pm 0.09$	226	9.5 ± 4.4	3.3 ± 2.1	141 ± 3	673

Summary and Conclusions

These results demonstrate the effect of a molecular dipole as an electrostatic barrier, as well as the origin of a series contribution to the gate voltage, at the dielectric/OSC interface of an OFET. The selection of two SAMs of similar shape and length and different dipole magnitudes enabled a decoupling of the dielectric and dipolar contributions to OFET performance. Although both SAM treatments resulted in a more than 15-fold reduction in gate leakage current, the larger dipole of FOTS on n-type Si effected greater increase in the ON/OFF ratio, and significantly reduced sub-threshold leakage and swing. A comparison of OFETs on n- and p-type Si indicated that the tuning of the sub-threshold leakage by dipolar SAMs may depend on the relative surface potential of the SAM with respect to its underlying substrate, and may also include a contribution from the silane-oxide bonding itself. This work broadens the available electronic device properties that can be selectively tuned with inexpensive molecular layers. Moreover, the choice of a leaky oxide of marginal quality provided a platform on which to probe the utility of a molecular dipole for improving a poor dielectric. This surface engineering approach can be used to enhance other inorganic and polymer materials that may be considered unsuitable for electronic dielectrics.

Experimental Section

Oxides

Highly doped n-Si (As-doped) and p-Si (B-doped) wafers (SI-Tech, Process Solutions, ρ=0.001-0.005 Ω-cm) were sonicated in warm acetone and IPA, and dried in a stream of dry nitrogen. Wafers initially had thermally-grown 100 nm oxide layers. To obtain thinner layers, the original oxide layers were completely etched in a dilute 1:10 HF solution in deionized (DI) water, and rinsed thoroughly in DI water prior to drying with dry nitrogen. Thin oxides were grown using a Technics PE II-A oxygen plasma system at 400 mTorr and 500W for 2 minutes, and placed in an oven in air at 200 °C for 2 hours. Octyltriethoxysilane (OTS, also used to refer to the resulting layer on the oxide) and 1H,1H,2H,2H-perfluorooctyltriethoxysilane (FOTS) were used as purchased from Sigma Aldrich, and stored in nitrogen at 4 °C when not in use. Self-assembly was achieved by placing 0.05 mL of each solution in a small scintillation vial centered within a 6-inch Pyrex crystallization dish containing several evenly-spaced wafer pieces. Dishes were covered with aluminum foil and placed in a vacuum oven at 125 °C overnight under house vacuum at 45 cm Hg. Substrates were rinsed in hot toluene and dried with nitrogen prior to organic deposition.

Bare and SAM-treated oxides were characterized with x-ray photoelectron spectroscopy (XPS), ellipsometry, water contact angle, and atomic force microscopy (AFM). Carbon 1s spectra obtained via XPS shows an enhancement of the CH_2 bond at 284.5 eV for OTS, and FOTS samples show the double peaks at 291 eV and 293 eV with a ratio of ~5:1, in agreement with the ratio of CF_2-CF_3 species[37] (Fig. 2.9). Spectra of the Si 2p core electrons (Supporting Fig. S5b) for p-SiOx are at roughly 0.625 eV above those for n-Si, roughly equivalent to the expected workfunction difference between n-Si and p-SiOx[32]. Notably, we observed that although the peak maxima for Si 2p and O 1s electrons in bare p-SiOx were also roughly 0.7 eV higher than in n-SiOx, these shifts were not observed in the p-SiOx+OTS or p-SiOx+FOTS surfaces.

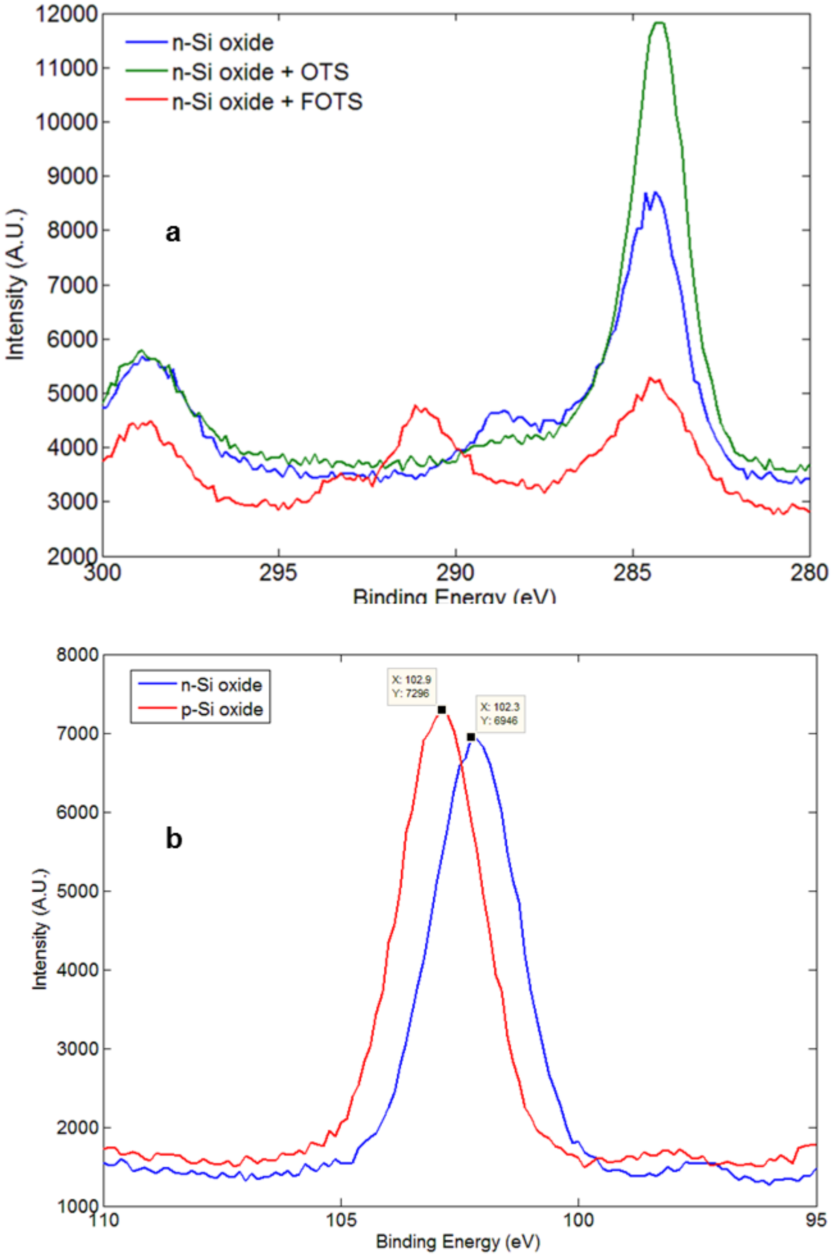

Figure 2.9 Carbon 1s and Silicon 2p X-ray Photoelectron Spectra of bare and SAM-treated oxides on n-Si. **(a)** OTS samples show an increase in the peak at 284.5, corresponding to the CH$_2$ bond. FOTS samples show a distinct double peak at 293 eV and 291 eV, corresponding to the CF$_3$ and CF$_2$ bonds. The ratio of the peaks, approximately 5:1, is consistent with the number of CF$_2$ and CF$_3$ species on the FOTS molecule. **(b)** The core Si 2p electrons for p-Si are observed to lie 0.625 eV above those of n-Si. The experimental resolution of the XPS unit is 0.125 eV.

The bare oxide thickness was measured by Brewster angle imaging ellipsometry (Accurion Nanofilm EP3) with 532 nm laser light, scanning between 55 and 85 degrees using a 5-point region-of-interest scan with n_{ox} = 1.462, and yielded a value of 11.5 ± 0.1 nm. Ellipsometric measurement of OTS and FOTS layers on oxide was obtained with a 5-point region-of-interest measurement using a multilayer model assuming the previous value of the oxide thickness, a range of 0.5 nm to 2 nm for the SAM thickness as a fitting parameter, and with $n_{SAM} = n_{ox}$,yielding monolayer thicknesses of 1.35 nm and 1.02 nm, respectively, with accuracy within 0.1 nm. Static contact angles (Ramé-Hart) with de-ionized water droplets were 67.5° ± 2° for bare oxide, 88.7° ± 0° for OTS and 100.5° ± 0° for FOTS, consistent with reported values in the literature for full coverage of these vapor-deposited SAMs on silicon oxide[37,38]. The contact angle for our oxides, which is higher than the 28° angle generally observed for bare oxides, reflects the rough nature of our oxide surfaces. Images of bare and SAM-treated oxides were obtained with a Nanoscope V (Digital Instruments) AFM (Figs. 2.10 and 2.11).

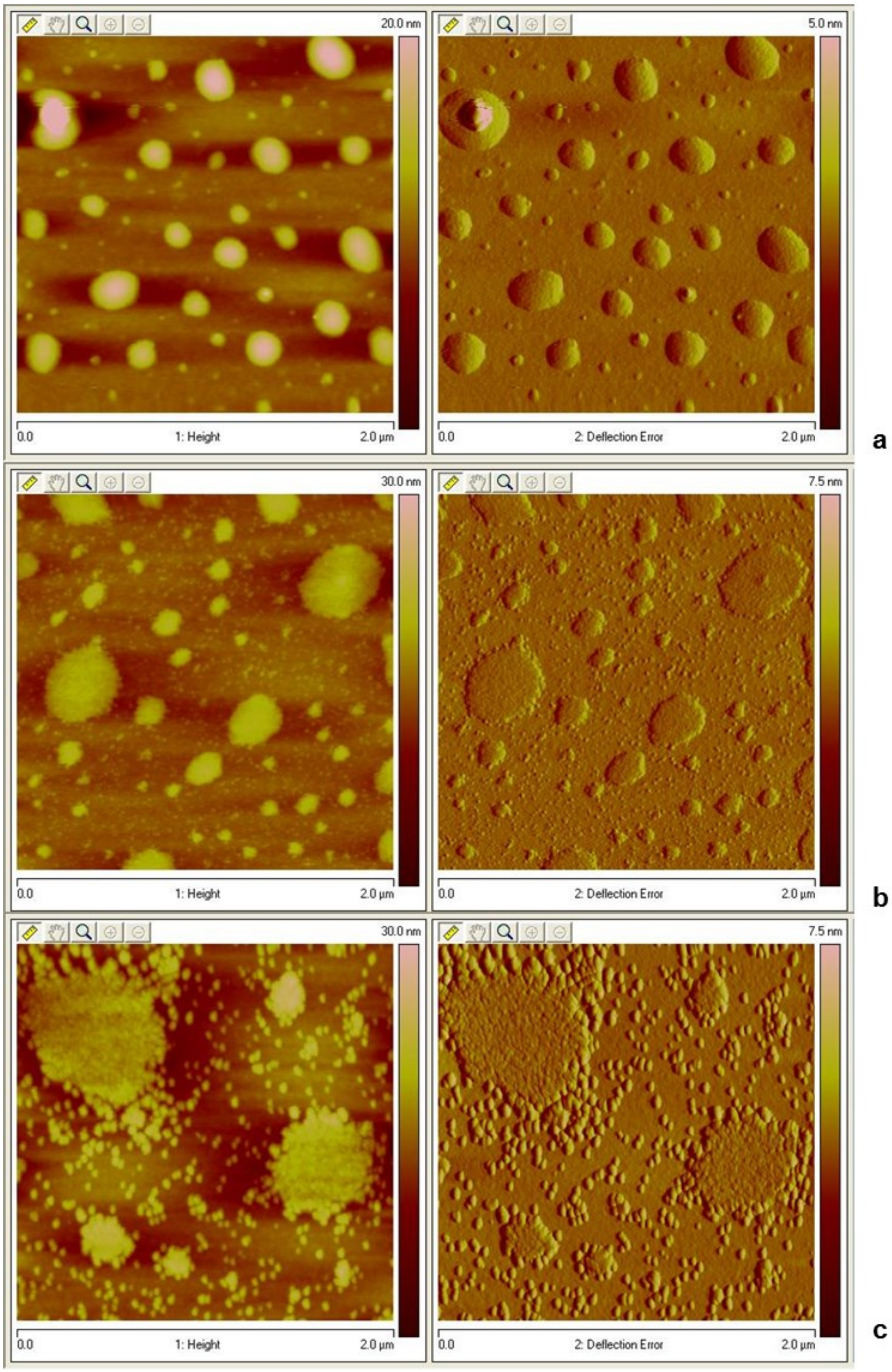

Figure 2.10 AFM height and deflection error images of rough n-Si oxide surfaces. **(a)** Rough 10 nm oxide. **(b)** Rough oxide with OTS treatment. **(c)** Rough oxide with FOTS treatment, showing SAM domains on oxide hillocks of 2-3 nm height. Larger FOTS-coated oxide hillocks show roughness of ~ 1-2 nm.

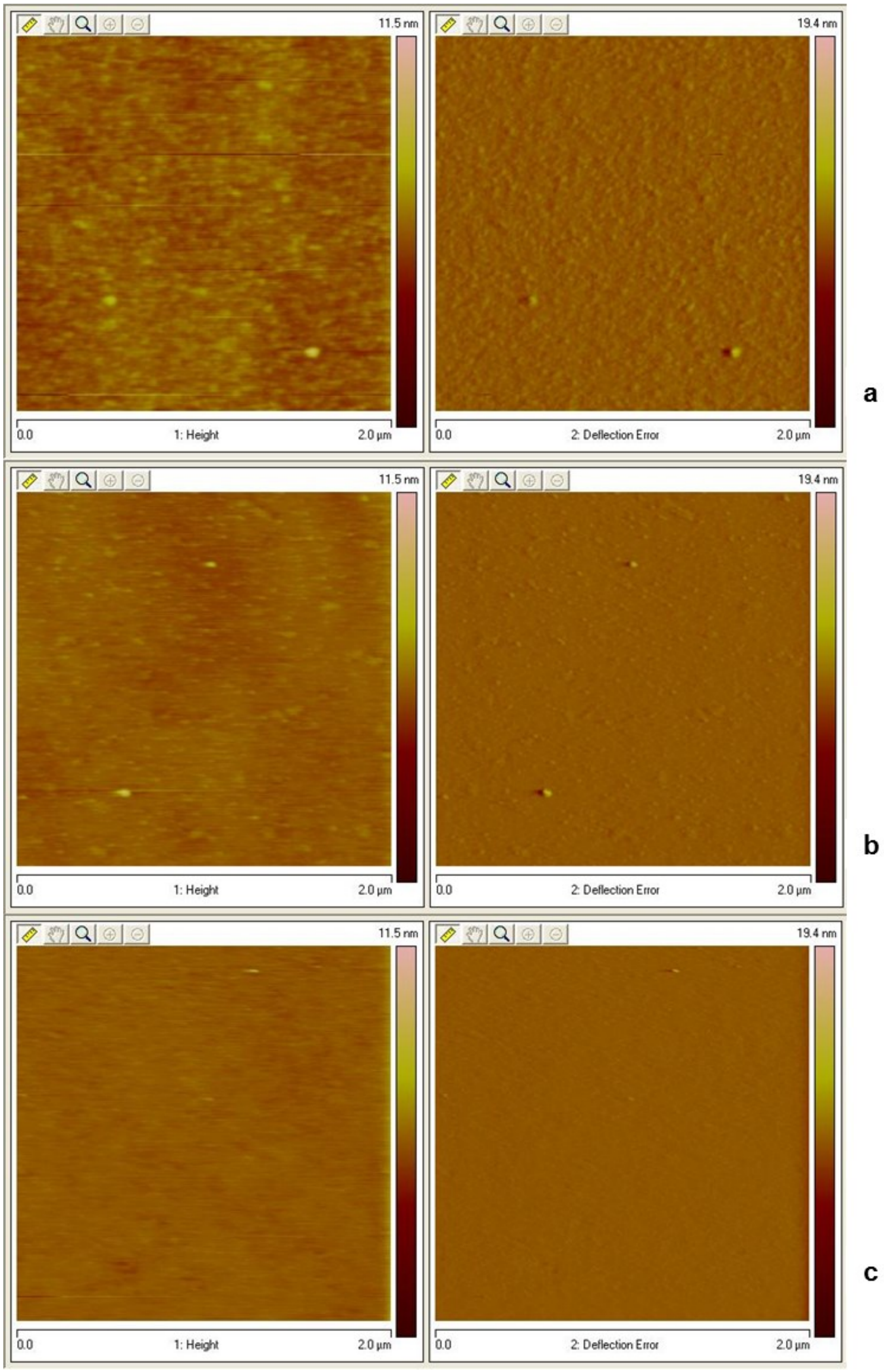

Figure 2.11 AFM height and deflection error images of smooth n-Si oxide surfaces pre- and post-SAM-treatment. **(a)** Rough 10 nm oxide. **(b)** Rough oxide with OTS treatment. **(c)** Rough oxide with FOTS treatment.

OFETs

Active layers consisting of 40 nm of 8-2-Bn naphthalenetetracarboxylic diimide (NTCDI), synthesized in our laboratory (Fig. 2b), were deposited at a rate of 0.2-0.4 Å/s in an Edwards thermal evaporation system at a base pressure below 3x10^{-6} Torr, at a substrate temperature of 75 °C. Gold contacts 50 nm thick were deposited at the same base pressure through shadow masks, at a rate of 0.3-0.6 Å/s, during which substrate temperature did not exceed 60 °C. With the exception of the HF etch and plasma oxidation, all processes were carried out in an ordinary (non-cleanroom) environment using ACS reagent-grade solvents.

Each wafer type consisted of 12 devices, with three devices each of four different W/L ratios (80, 53.3, 40, and 32). All electrical characterization was performed on an Agilent 4155C Semiconductor Parameter Analyzer using a medium integration time (16.7 ms), under ambient fluorescent lighting conditions, in air. Si gates were scratched with a diamond scribe and contacted with Ga-In eutectic (Sigma-Aldrich). To prevent puncturing the thin oxide layers, devices were probed with low-resistance probes from Micromanipulator, onto which small (~200 μm) drops of Ga-In eutectic were placed for contacting source and drain electrodes.

Surface Potentials

Several surface junctions were prepared for surface potential characterization using scanning Kelvin-probe microscopy (SKPM). For one set of samples, bare oxides were placed under vacuum for SAM attachment. After rinsing in hot toluene, substrates were patterned using S1813 photoresist (Microposit) on an EX620 UV aligner, and patterns were developed with trimethylammonium hydroxide (CD26, Microposit). The surfaces were placed in an oxygen plasma at 100W for 60 s at a pressure of 400 mTorr to remove the SAM layer. The plasma power and time was chosen so as to not grow additional oxide on the exposed areas. Substrates were rinsed in acetone to remove the photoresist hard mark prior to SKPM characterization. For the second set of samples, bare oxide substrates were spin-coated with S1813 photoresist, patterned, and developed. Wafers were coated with an electron beam-deposited layer of Cr/Au (10 nm/ 50 nm, respectively), and left overnight in acetone for photoresist liftoff. Wafers were placed under vacuum for SAM treatment, and rinsed in hot toluene for 2 hours. Surface potentials were measured along the Au/oxide/Au and Au/oxide+SAM/Au interfaces. For the third set of samples, gold patterns with 150 μm linewidths were thermally evaporated (Edwards E306) at 10^{-6} Torr onto bare oxide substrates. Wafers were placed under vacuum for SAM treatment, and rinsed in hot toluene for 2 hours, followed by a hot bath of ethanol for Au liftoff from the oxide. Surfaces were then dried in a stream of nitrogen with a 0.22 μm filter and placed on a hot plate at 125 °C for 20 minutes prior to measurement. Surface potential measurements of oxide/oxide+SAM interfaces were carried out in air on a Veeco AFM using a NanoScope IIIa extender and a MultiTap-75G Cr/Pt tip (BudgetSensors) using a tip voltage of 2 V and a liftoff distance of 100 nm. Surface potentials for OTS- and FOTS-treated surfaces were 150-200 mV more negative than bare oxides, for both n-SiOx and p-SiOx.

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Chapter 3 : Characterizing Self-Assembled Monolayer-treated oxides within a Metal-Insulator-Semiconductor Junction

Self-assembled monolayers (SAMs) comprise a range of small molecules that can be chemisorbed onto a surface into single layers exhibiting short- to long-range spatial order. The ability to tailor the SAM's reactive tail group, main chain, and headgroup has enabled the surface functionalization of a wide array of materials employed in organic field-effect transistors. The result has been highly precise tuning of device interfaces, effectively yielding control over various interconnected properties including organic semiconductor (OSC) morphology, carrier mobility μ, the threshold voltage (V_T), and gate and subthreshold leakage currents.[1]

Dipolar SAMs have attracted considerable attention for their ability to controllably tune the V_T of OFETs,[2-5] as described in Chapter 1. Typical V_T's of OFETs fabricated on 300nm SiO_2 range as high as 100 V, making them impractical for most low-power, mobile applications. To reduce this high V_T, SAMs with large molecular dipoles have been employed at the OSC-dielectric interface, where they can tune the V_T by as much as |60 V|. The mechanism by which dipolar SAMs modify V_T is has been the subject of some of the most intense research in organic electronic device physics of the last two decades since the development of SAMs by Nuzzo and Whitesides.[6] Many models have been applied to a variety of SAM/substrate systems to assess the effect they have on the electrostatic properties of the interface at which they bind, some of which we discuss below.

Measuring Molecular Dipoles

Dipolar SAMs are so called because the constituent molecules possess an intrinsic, fixed dipole. Molecular dipoles arise from a gradient in charge density across the molecule. This difference in charge density can arise due to the presence of formal charges, such as an ionized amine group. Typical examples of such molecules would be amino-propyl-triethoxysilane (APTES), a commonly used surface treatment. Charge density differences arise in the presence of atoms with higher electronegativity (χ) than neighboring atoms, as is the case for fluorinated or chlorinated organic molecules. Molecules like perfluorooctyl silane (FOTS), commonly used in OFET applications as in the previous chapter, are an example of electronegativity-driven dipoles, where individual bond dipoles can add constructively if pointing in the same direction, yielding a large net dipole across the molecule.

The simplest model to represent the effect of a charge density gradient is a point-dipole model, consisting of two point charges separated in space. The Coulombic interaction between these point charges gives rise to an electrostatic potential, given as

$$\psi(r) = \frac{1}{4\pi\varepsilon_r\varepsilon_0}\frac{\hat{\boldsymbol{r}}}{r^2} \qquad [3.1]$$

where ε_r and ε_0 are the relative and vacuum permittivities, respectively, and r is the distance between the point charges. This type of model is generally appropriate for linear zwitterionic molecules that possess formal charges at opposite ends, or one anchor group and a formal charge at the opposite end.

Molecular dipoles were originally measured using a heterodyne apparatus, effectively measuring the change in dielectric constant of a dilute vapor of the molecule of interest as a function of applied frequency and temperature.[7] By contrast with dilute solutions, SAMs possess a very high degree of spatial order and rigid anchoring to one surface. The properties of the ordered adsorbed state as a SAM are markedly different from the disordered gas phase. To assess the effects of surface formation on the electrostatic properties of a monolayer[8] Kronik assembled a density-functional theory (DFT) model of an aromatic SAM consisting of several benzene subunits with a thiolate anchor group. Their simulations showed that molecules within a layer act to depolarize the internal benzene units of their neighbors. Their work, together with that of Cahen[9] have helped establish the notion that even the HOMO and LUMO levels of SAMs are different from their constituent molecules, and should be considered unique layer orbitals.

The prevalent model for relating the surface potential due to a molecular dipole is based on the concept of the electric double layer, formalized by Kirkwood[10] and employed as early as 1995 by Mirkin in early investigations of alkanethiol monolayers on Au.[11] A SAM layer is modeled by the Helmholtz potential,

$$\Delta V_{SAM} = \frac{N\mu_{\perp}}{\varepsilon_{\mathrm{SAM}}\varepsilon_0} \qquad [3.2]$$

where N is the areal dipole density, ε_{SAM} is the dielectric constant of the SAM layer, and ε_0 is the vacuum permittivity. The parameter $\mu_\perp$ is the component of the SAM dipole μ_{SAM} component perpendicular to the surface. Measurements of OTS and FOTS using SKPM reveal that OTS does not sit perpendicular on the surface, but at a small angle relative to the surface.[12,13] As a result, the net surface dipole $\mu_\perp = \mu_{SAM} \cos\theta$, where θ is the angle relative to the substrate normal.

In experimental work aimed at relating SAM properties to those measured in gas-phase, Ellison and coworkers[12] applied scanning-kelvin probe microscopy (SKPM detailed in the next Chapter) to measure the surface potential difference between bare and SAM-treated silicon oxide. Substrates subjected to a dilute gas of alkyl silanes enabled the formation of small SAM islands (10s-100s of nm) across which surface potential scans could be acquired. Using the Helmholtz model above, they determined values for SAM dipoles for OTS and FOTS of -0.02 D and -1.29 D, respectively, however these values were less than 50% of those measured in the gas phase, further confirming the simulation studies of Kronik.

Relating the SAM-induced surface potential difference to changes in the threshold voltage of an OFET has been the subject of many investigations. The link between μ_{SAM} and V_T is of particular interest because the typical changes in surface potential due to SAM adsorption are on the order of 0.1 V, yet ΔV_T can range up to several dozen volts. This clearly suggests that the relationship is more complex than $\Delta V_T = \Delta V_{SAM}$.

As a result, researchers have sought a direct relationship between ΔV_T and ΔV_{SAM} in the context of the transistor output current (Eq. 1.9), where it is understood that the drain current I_D scales with the capacitance of the insulator. Instead, the Helmholtz potential is often combined with Gauss' Law, expressed as

$$\Delta Q_{SAM} = C_i \Delta V_{SAM} \qquad [3.3]$$

where C_i is the capacitance of the insulator and ΔV is the voltage change across the insulator. For a transistor with a Si oxide insulator, the quantity $\Delta Q_{SAM} = C_i N \mu_\perp / \varepsilon\varepsilon_0$ is in the range of 10^{11} - 10^{12} cm^{-2} for a perfluorinated alkyl SAM such as FOTS, and has been shown to correspond to ΔV_T to within a factor of 2. These observations have prompted researchers to ask how the ΔV_T due to a SAM could be cancelled out—by an offsetting voltage, or by an offsetting electric field. Various investigations have separately demonstrated data in support of both.

The Batlogg group investigated the SAM-induced ΔV_T in pentacene transistors on various thickness oxides, and concluded that offsetting the effect of the SAM dipole required an offsetting electric field.[14] In addition investigations by our group[1,15] have shown this V_T shift to scale with the substrate thickness. However, a report by the Bao group with OFETs fabricated on 4 - 9 nm of AlOx found that ΔV_T was nearly equal to SKPM-determined ΔV_{SAM} for the same surface[16]. In this case observation of $\Delta V_T \approx \Delta V_{SAM}$ is likely the result of a large C_i for thin AlOx, which yields a very low V_T (+0.35 V), within the same order of magnitude as ΔV_{SAM}. Although this work demonstrated that ΔV_{SAM} acted like a vacuum-level shift, it does not appear to contradict the idea that ΔV_{SAM} acts to change the surface charge of the oxide as in Eq. 3.2, of which the effect on the transistor would be a change in the required electric field (not voltage) to turn on the device. Research by Ou-Yang *et al.* sets forth a model in which the V_T shift in an OFET with a SAM-treated dielectric is due to the creation of an interfacial electric field that propagates throughout the entire device structure.[17] The main assumption of this work is that the OSC—in this case pentacene—may be treated as a dielectric once mobile carriers have been extracted from the device. Their conclusions further support the notion that the effect of the SAM is distributed across the insulator, implying the requirement of an offsetting electric field.

Work carried out by the de Leeuw group on the nature of SAM-mediated ΔV_T has provided new evidence[18,19] in support of the mechanism implied by Eq. 3.2. In an effort to understand how SAMs change a transistor's resilience to bias stress, SAMs were deposited on a bottom-gate/bottom-contact oxide substrate, atop which a p-type poly-triaryl amine (PTAA) OSC layer was deposited. After subjecting the transistor to a large gate bias stress, the PTAA layer was removed and the insulator surface potential measured using SKPM. Insulators treated with dipolar SAMs like OTS and FOTS retained their "stressed" surface potentials for a longer time, suggesting that the SAMs act as charge traps at the insulator-SAM interface.

Along the same line of investigating surface state modification by SAMs, the Heremans group conducted theoretical work on the effect of OTS and FOTS layers on the onset voltages of OFETs[20] fabricated on SiO_2. Their molecular dynamics (MD) simulations suggest that SAMs act to broaden the energetic disorder of the *organic semiconductor*, which in turn modifies the number of carriers found at the Fermi level in the layer, as depicted in Fig. 3.1. In addition, the deep trap states referenced by de Leeuw would also play a role. Together with the simple yet general model of Ou-Yang, it is clear that interactions at both the insulator-SAM and SAM-OSC interfaces are important in determining overall device performance threshold voltage shifts.

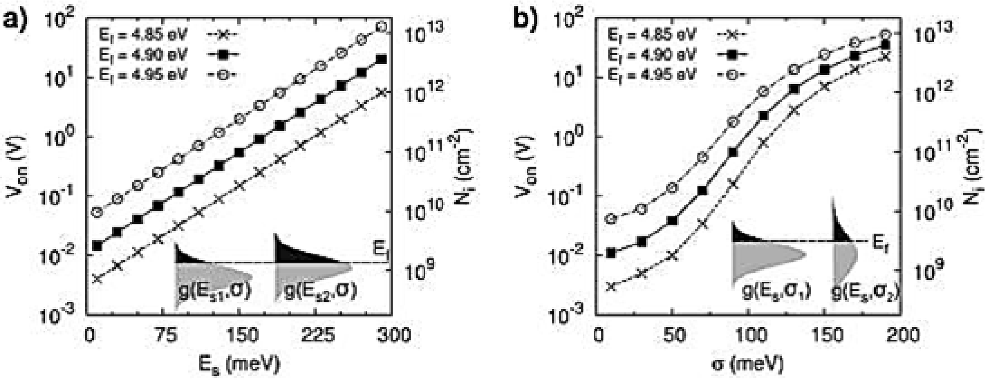

Figure 3.1 A dipolar SAM layer on an OFET insulator creates energetic disorder at the SAM-OSC interface.Onset voltage V_{on} and equilibrium charge carrier density N_i for OSC with Gaussian DOS where they are have **(a)** the same energetic disorder σ (standard deviation) and different electrostatic interaction E_s; and where they have **(b)** identical E_s and different energetic disorders. The resulting change in the Fermi level within the OSC is partially responsible for the ΔV_T exhibited in OFETs fabricated on SAM-treated insulators. Image from Ref. 20.

Understanding SAM-induced surface states

Capacitance has long been a useful technique for understanding the impact of surface states on the behavior of MIS diodes and OFETs. One method for determining the difference in the number of surface states between bare and SAM-treated oxides relies on using the transfer curve of an FET, a method illustrated in Chapter 2. As explained in Chapter 1, V_T should be the voltage at which the device is at flatband condition (V_{to}), which is determined by any built-in potential due to work function differences between the metal and semiconductor. However, the presence of surface states will contribute to the shift of V_T relative to V_{to}. Conversely, the difference between the turn-on and threshold voltages can be used to estimate the number of interface states as

$$N_{ss} = \frac{C_i}{q}(V_T - V_{to}) \qquad [3.4]$$

where N_{ss} is the areal surface state density. In Chapter 2, the trap densities for SAM-treated oxides within an 8-2-Bn NTCDI MIS diode were found using the capacitance of the bare oxide insulator. These values were found to be within the same order of magnitude as the charge density expected from the Helmholtz potential in Eq. 3.2, suggesting a close correspondence between the density of surface states and the areal molecular density at the interface.

Capacitance-voltage (CV) data is a complementary tool to OFET measurements for estimating the density of surface states. Measurements of the gate stack of the OFETs measured in Chapter 2 were conducted at frequencies ranging from 25 Hz to 10 kHz, in order to capture the device behavior in a range of application-relevant frequencies. In addition, diodes of identical geometry were fabricated without the NTCDI layer, with an Au layer deposited directly atop the bare or SAM-treated silicon oxide. Data presented herein are averages of 10-12 devices for each surface treatment, except where noted otherwise.

Oxide + SAM MIS Diodes

The importance of measuring OSC-free structures arises from the fact that the heavily-doped nSi used as the gate in the OFETs of the previous chapter is not a perfect metal, and so must first be analyzed as a Si/Oxide/Au MIS structures. Testing this structure affords us greater insight into the effect of the SAM layer on the underlying oxide surface.

Measurements of OSC-free MIS structures using bare oxide as the insulator layer (Fig. 3.2(b)) below yield behavior qualitatively similar to that of an ideal MIS diode at low frequencies (Fig. 3.2(a)). At negative gate voltages we expect to observe only the capacitance of the oxide, which in this case is ~400 nF/cm^2, equivalent to roughly 2.2 nm of SiO_2. At 25 Hz we notice a dip in the capacitance towards what would be the minimum device capacitance, C_{min}, which at 225 nF/cm^2 is equivalent to 3.9 nm of SiO_2. This minimum in the capacitance is expected below 100 Hz for Si/SiO_2/metal junctions[21]. In an ideal MIS diode, the decrease in capacitance near 0 V reflects the formation of a small space charge region at the Si/SiO_2 interface, as the majority carriers (electrons) in the nSi are drawn away from the interface. At low frequencies the minority carriers (holes) can be generated at a rate than enables charge exchange within the space charge region, and so the capacitance can return to near the value of just the oxide. However, as the frequency increases, minority carriers in the space charge region cannot be generated quickly enough to recombine with the majority electrons, and as a result the capacitance remains at the value of the minimum capacitance C_{min}.

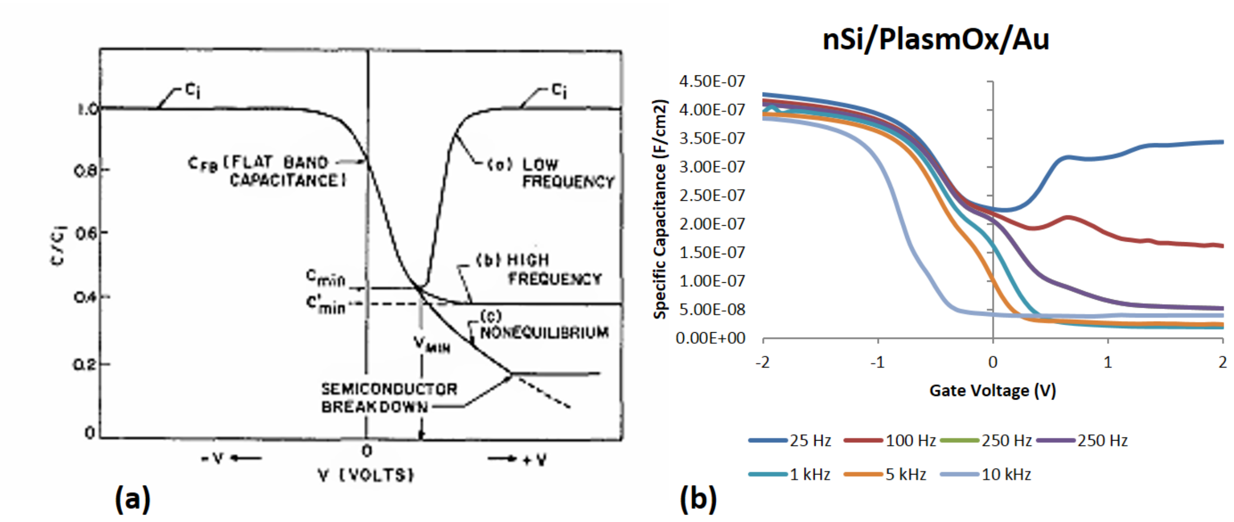

Figure 3.2 (a) Capacitance-voltage (CV) curve for an ideal MIS diode, adapted from Ref. 21. **(b)** CV curves for ultrathin marginal quality oxide from Chapter 2. *Note*: In the semiconductor literature, V_G is referenced as the voltage on the top Au electrode, and not the Si bulk. As we have used the Si contact as the gate in our transistor measurements, we define $V_G = V_{Si}$. Thus, while on first glance it would appear that our capacitor is p-type by conventional notation, this graph indicates the V_{Si} as the gate voltage. As a result, the capacitance is highest when electrons are pushed to the Si/SiO_2 interface, in agreement with the MIS theory.

However, this transition in our devices is accompanied by a continual decrease of C_{min} with increasing frequency. As Fig. 3.2(a) suggests, this transition marks the onset of non-equilibrium charges in the device being measured. In this case, it is more than likely that the poor quality of the SiO_2 layer is enabling high leakage current across the device. This is supported by the measured dissipation factors for the capacitors, which begin to exceed 0.2 above 100 Hz, clearly indicative of high conduction across the device. A possible reason for these high dissipation values, which would also explain the thinner oxide values as compared to previous measurements, is the direct evaporation of Au onto the interface. It is likely that a number of conduction pathways in the low quality oxide could be enhanced by the presence of an adjacent Au layer, as compared to the OFET architecture where the oxide is in contact with a much lower conductivity NTCDI layer.

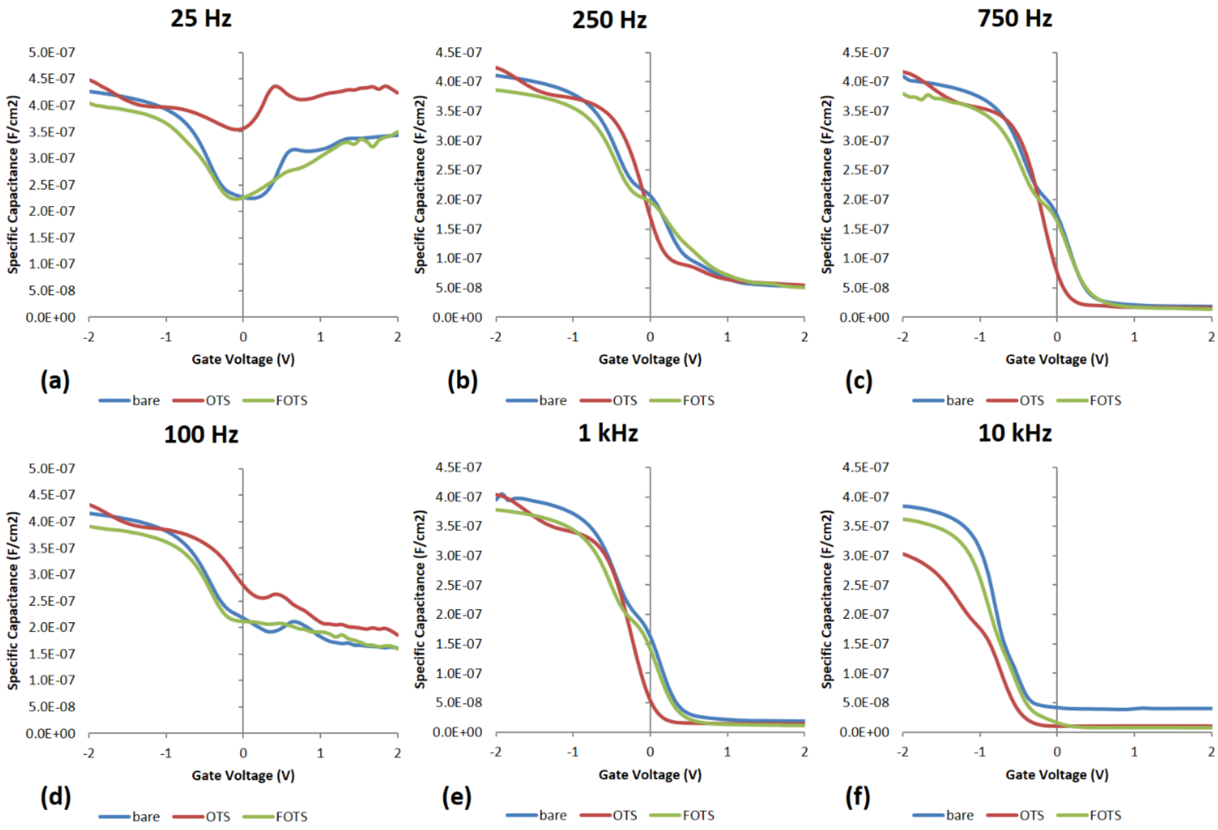

Figure 3.3 Specific capacitance of MIS Diodes of nSi/PlasmOx+SAM/Au at **(a)** 25 Hz, **(b)** 250 Hz, **(c)** 750 Hz, **(d)** 100 Hz, **(e)** 5 kHz, and **(f)** 10 kHz.

Bare oxide capacitors with OTS and FOTS treatments, respectively, were tested at the same operating voltages and frequencies as the bare oxide capacitor, as shown in Fig. 3.3. At low frequencies the capacitors display characteristics similar to the ideal MIS diode, approaching a C_{min} value of approximately 200 – 225 nF/cm^2, or 13-15 nm of SiO_2. Increasing frequency reveals a decrease in C_{min} similar for all three substrates. There is a clear difference in C_i relative to the bare oxide even in the presence of high dissipation (leakage current). We can estimate the resulting parallel conductivity $\sigma_{\parallel}$ of the oxide using the relation

$$\sigma_{\parallel} = 2\pi f C_i D l \qquad [3.5]$$

where f is the frequency of the AC signal, C_i is the specific capacitance, D is the measured dissipation factor, and l is the sample thickness. Since we know the contact area of the device, we have converted to conductivity in order to compare our measurements later to conductivity values determined from diode measurements. It should be noted, however, that this conductance reflects the *entire* gate stack. At low frequencies, the bare and FOTS-treated diodes share similar conductivity, and OTS-treated diodes exhibit higher conductivity. At 1 kHz and 10 kHz, the OTS and FOTS diodes have similar shapes qualitatively, but OTS diodes exhibit a pronounced conductivity at negative gate voltages. The exponential increase in the current for the bare diodes at 1 kHz and 10 kHz is attributed to diode-like leakage across the oxide.

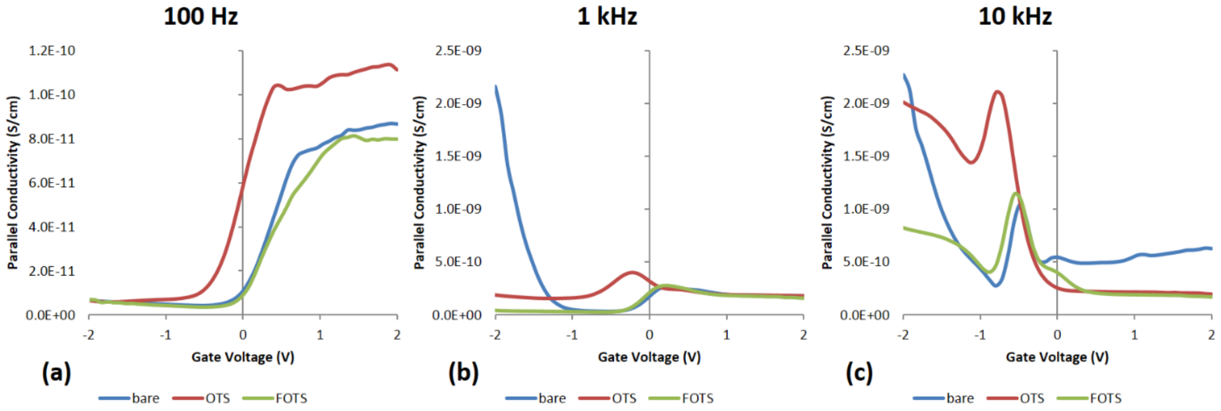

Figure 3.4 Parallel conductivity $\sigma_{\parallel}$ of the nSi/PlasmOx+SAM/Au MIS diode at **(a)** 100 Hz, **(b)** 1 kHz, and **(c)** 10 kHz. Note that the scale of (a) is an order of magnitude smaller than (b) and (c).

The suppression of parallel conductivity at positive gate voltages is consistent with the presence of a barrier to electrons at the oxide/SAM interface. As V_G becomes more negative and approaches $V_G = 0$ V, all three devices display a large change in conductivity, with a region of differential negative resistance (DNR). The observation of DNR is generally attributed to a mismatch in carrier mobility across a small region or interface. In the curves of Fig. 3.4(b,c) we see that the onset of this region is approximately the same for all the devices, though the peak potential at which the conductivity again decreases is shifted slightly for FOTS ($\Delta V = -0.1$ V) and for OTS ($\Delta V = -0.4$ V). The fact that this change is observed for all three devices and that it occurs at $V_G > V_{FB}$ makes it reasonable to assume that the change in parallel conductivity reflects conduction across a small depletion region at the Si/SiO_2 interface formed at $V_G > V_{FB}$.

As V_G becomes more negative $\sigma_{\parallel}$ begins to increase again, though much more rapidly for the bare oxide device. This point coincides closely with $V_G = -1 \text{ V} \approx V_{FB}$, determined by the ~1eV offset between $E_{F,nSi}$ and φ_{Au}. Therefore, this current reflects the flow of electrons from the e-rich nSi across the oxide (and additional depletion) layer as they are attracted to the positive potential at the Au electrode.

The lower $\sigma_{\parallel}$ of the SAM-treated structures at negative gate voltages and medium to high frequencies is consistent with the gate leakage measurements presented in Chapter 2. In these devices, it is only above 1 kHz and $V_G < -1$ V where SAM-modified oxide devices display lower conductivity. By comparison, the OFET leakage measurements showed a suppression of current even at $V_G = -0.5$ V at a testing frequency equivalent to 62.5 Hz. Since the Si/SiO_2 interface is unchanged for the three devices, it is fair to assume that differences between the three arise from differences at the SiO_2/SAM interface.

J-V Characteristics of SAM-treated MIS Diodes

Current density-voltage (J-V) measurements offer insights into the differences between OTS and FOTS current reduction at $V_G < V_{FB}$. The conduction mechanisms of SAMs have been intensively researched over the last two decades, in a wide array of testing architectures ranging from nanoscale scanning-tunneling microscopy (STM) imaging and break-tunnel junctions, to microscopic (~100 µm) Hg and E-GaIn soft metal contacts,[22] and lastly macroscopic diodes like those presented here.[9,23,24] While these techniques would be complementary for most electronic device studies, the small scale of SAMs makes their electrical characterization subject to a large number of potential surface defects which can considerably alter the interpretation of results.[25] Nevertheless, this study focuses on the properties of SAMs that can be derived from studying macro-scale devices, which implies a degree of averaging across ideal and potentially defective SAM-treated surfaces.

There are a number of models that have been successfully employed to describe charge conduction across SAMs.[25,26] Many of these have been borrowed from early investigations of charge conduction in insulators[21], and have also been applied to the study of conduction in organic semiconductors, many of which—given their wide band gaps and structural disorder—have properties in common with insulators. The models screened against the OTS and FOTS monolayers should reflect what we know about them: (a) they trap or inject charge at an interface;[18] (b) they can modify the surface potential of an oxide surface;[12] (c) they modify charge injected through the surface at which they are chemisorbed.[27]

We also aim to restrict our analysis to that which we can accurately quantify. Several tunneling mechanisms have been investigated to model charge transport across SAMs. However, the current in those models is exponentially dependent on the thickness of the monolayer. Thus, being able to produce a highly ordered SAM is just as important as accurately characterizing its thickness across the entire device area. While the models below do depend on knowledge of the electric field, which is itself dependent on the oxide(+SAM) interface which cannot be known exactly, an estimate of the insulating region of order ~7-10 nm is less sensitive to a 10% change in the effective thickness. Given the experimental limitations of quantifying the SAM thickness to sub-nm scale, and our overarching interest in SAMs as *remedial* layers for poor quality, non-uniform oxides, we exclude models that rely on highly accurate SAM thicknesses to derive barrier heights. With this in mind, we focus our attention on three processes that are suitable models for charge traps and interface barriers in this MIS structure.

Models for MIS Diode Conduction

The MIS diode under investigation consists of three interfaces and four materials, each of which will contribute its own conduction mechanism to the device-level behavior. The simplest mechanism within the structure is Ohmic conduction within the Au layer. Physical vapor-deposited Au layers on a low roughness surface at room temperature and thickness above ~20 nm have been shown to exhibit bulk metal conduction, which is described by the relation (Ohm's Law) $J/\mathbf{E} = \sigma$.

Space-Charge Limited Conduction (SCLC)

The presence of a thin oxide layer just above the heavily-doped nSi substrate will create a region of high $\boldsymbol{E}$ in its vicinity when a voltage is applied. At $V_G > V_{FB}$ this voltage will create a space-charge region as electrons are drawn from the As^+ dopant ions in the Si lattice. The current arising from SCLC is given as

$$J = \frac{8\varepsilon_i \mu}{9d} E^2 \qquad [3.6]$$

where ε_i is the dielectric constant of the insulating region, μ is the mobility of the carriers in the space charge region, and d is the thickness of the space charge region. A plot of J vs. $\boldsymbol{E}$ should yield a linear fit, and the mobility of the carriers in this space charge region can be determined. It should be noted that in addition to the space charge region that forms at the Si/SiO$_2$ interface, the very thin oxide layer will also act as a space charge region. Although it is known that large dopant ions such as As^+ are too large to fit in the SiO$_2$ network and are displaced during thermal oxide growth,[28,29] it is possible that the rapid oxygen plasma process used to grow our oxides may result in these ions trapped within the oxide layer.

Schottky Emission

Schottky emission has been used extensively to characterize the energy barriers at metal-semiconductor junctions. An electron near a metal surface will attract positive charge in the metal, and in doing so create a so-called image potential on its surface. Schottky modeled the interaction of the metal with an electron at a distance x as if it were a positive charge at a distance $-x$ (inside the metal). The force of the interaction between the virtual positive charge and the electron, across a distance $r_0 = 2x$, is given as

$$F(x) = \frac{-q^2}{4\pi r_0 \varepsilon_0} = \frac{-q^2}{16\pi\varepsilon_0 x^2} \qquad . \qquad [3.7]$$

The potential energy of this force acting on the electron is found by integrating the force, from a distance at infinity, as

$$U_{image}(x) = \int_{\infty}^{x} \frac{-q^2}{4\pi r_0 \varepsilon_0} = \frac{-q^2}{16\pi\varepsilon_0 x} \qquad . \qquad [3.8]$$

If this electron is subjected to an electric field $\boldsymbol{E}$, then its potential will be modified by an amount

$$U_{total} = U_{image}(x) + q\boldsymbol{E}x = \frac{-q^2}{16\pi\varepsilon_0 x} + q\boldsymbol{E}x \, . \qquad [3.9]$$

The distance at which these two potentials cancel each other is found by minimizing the energy of the system, as

$$\frac{\partial U_{total}}{\partial x} = 0; \qquad x_m = \sqrt{\frac{q}{16\pi\varepsilon_0 \boldsymbol{E}}} \qquad . \qquad [3.10]$$

At the distance x_m, the potential of the electron relative to the image potential from the metal is reduced by an amount

$$\Delta\varphi = \sqrt{\frac{qE}{4\pi\varepsilon_0}} = 2\boldsymbol{E}x_m \qquad . \qquad [3.11]$$

The value $\Delta\varphi$ is the quantity that the original barrier φ_b is reduced in the presence of an electric field. It is a useful metric for characterizing interfacial phenomena such as surface states and dipoles, all of which can act to increase or decrease the energy barrier to charge transport across an interface. The values Δφ between a semiconductor and a metal can be determined from the *J-V* characteristics of a diode using the thermionic emission equation

$$J = A^{*}T^{2}e^{\frac{-q}{kT}\left(\varphi_b - \sqrt{\frac{q}{\pi\varepsilon}}\sqrt{\boldsymbol{E}}\right)} \quad , \qquad [3.12]$$

where A^{*} is the effective Richardson constant. Schottky and thermionic emission theory assess the probability that an electron can overcome the barrier φ_b between a semiconductor and a metal (or vacuum) by acquiring a sufficiently high velocity via thermal excitation. The Richardson constant captures the product of several fundamental constants that arise from the integration of the current that arises from thermal motion of a charge carrier in 3 dimensions, and is given as $A^* = 4\pi q m^* k^2/h^3$, where m^* is the relative mass of the charge carriers from their injection site. Since our diodes contain a thin oxide layer, we have used the value of the electron effective mass[30] in SiO_2 $m^*=0.42m_0$, where m_0 is the free electron mass. For a more thorough treatment of thermionic theory, the reader is referred to Ref. 21.

Frenkel-Poole

The Frenkel-Poole model was originally derived[31] to explain the observed enhancement of charge conduction in insulators with increasing temperature. The main hypothesis underlying this model is that insulators consist of a network of highly localized atomic potentials. Upon application of a large electric field, the shape of the atomic potential well is distorted in the direction of the field, thereby reducing the energy barrier required for a hop to the next localized state. That is, for a Coulomb potential with an initial barrier energy φ_b, the change in the potential upon application of an electric field $\boldsymbol{E}$ is given as

$$\Delta U = e\boldsymbol{E}r_0 + \frac{q^2}{\pi\varepsilon r_0} \qquad [3.13]$$

where r_0 is the distance from the center of the potential well to where the barrier φ_b is maximum. The distance at which the carrier can overcome the barrier is

$$e\boldsymbol{E}r_0 = \frac{q^2}{\pi\varepsilon {r_0}^2} \qquad [3.14]$$

so that rewriting the potential in terms of $\boldsymbol{E}$ yields

$$\Delta U = \sqrt{\frac{q}{\pi\varepsilon}}\sqrt{\boldsymbol{E}} \quad . \qquad [3.15]$$

Assuming that free electrons material of interest can be thermally excited from the traps (in the case of true Coulombic potentials, the atoms can be thermally ionized). Since thermalized ions follow Maxwell-Boltzmann statistics, the full energy description of the barrier energy in the presence of a field is given as

$$\Delta U = \varphi_b - \sqrt{\frac{q}{\pi\varepsilon}}\sqrt{\boldsymbol{E}} \qquad [3.16]$$

$$\frac{J}{V} = \sigma = \sigma_0 e^{\frac{-q}{kT}\left(\varphi_b - \sqrt{\frac{q}{\pi\varepsilon}}\sqrt{\boldsymbol{E}}\right)} \qquad [3.17]$$

The last assumption is of particular importance to our analysis, since the SAMs examined here do not possess readily ionizable species. Moreover, the very large bandgaps of OTS and FOTS (~ 7eV) preclude thermal excitation from HOMO to LUMO within the molecule. Nevertheless, if one is to assume that traps reside at the Si-O bonds between the SAM silane anchor and the oxide Si-O network, then this assumption is appropriate. Comparison of Eqs. 3.12 and 3.17 reveal that the Poole-Frenkel mechanism is quantitatively similar to that of Schottky emission, differing by only a factor of 2 in the prefactor to $\sqrt{\mathbf{E}}$. The reason for this is that the potential well for a Coulombic trap must also account for the immobile countercharge at the trap center. This difference in underlying mechanisms has led some researchers in molecular electronics to classify Poole-Frenkel as a bulk conduction mechanism, and Schottky emission (as well as certain coherent tunneling mechanisms) as purely interfacial processes.[26]

Diode Analysis

Diodes with an MIS structure consisting of nSi/PlasmOx(+SAM)/Au were fabricated. The results are shown in Fig. 3.5. The diodes are well modeled by SCLC in the high-field regime, at $V_G > +1$ V. From the slopes of these curves we can calculate the carrier mobility in the drift mobility in the space charge region $\mu_{SCLC} \sim 4.5\times10^{-14}$ cm^2/Vs. We can determine the field-dependent conductivity of the diode using the extrapolated mobility, given as

$$\sigma_{SCLC} = \frac{\varepsilon_i \mu_{SCLC}}{d}\boldsymbol{E} \, . \qquad [3.18]$$

Although the value of d is not precisely known, we use approximate it as the oxide (+SAM) thickness. The estimated conductivity σ_{SCLC} is plotted in Fig. 3.5(b), and is found to be in very good agreement with the AC conductivity measurements shown in Fig. 3.4. These values are also in close agreement with the reported conductivity[28] of thin RF oxygen plasma-grown SiO_2.

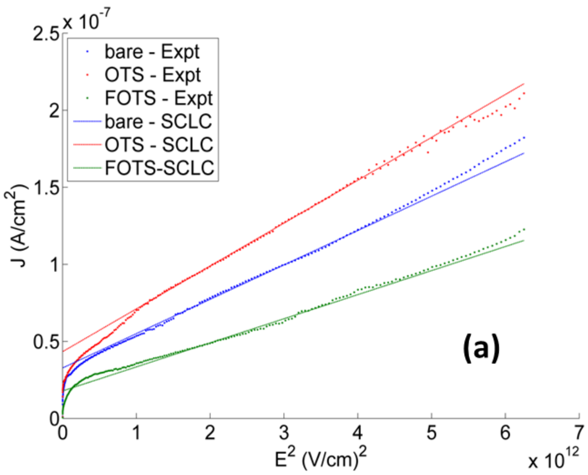

Figure 3.5 Space charge-limited current (SCLC) analysis of nSi/PlasmOx(+SAM)/Au MIS diodes. **(a)** Current characteristics plotted on a J vs. E^2 plot as per Eq. 3.6. **(b)** Conductivity obtained from plots of (a) using Eq. 3.18.

The J-V characteristics of the diodes were fit using the Frenkel-Poole (FP), Schottky (SH), and SCLC models discussed in the previous section. It is worth noting that a useful attribute in fitting the FP and SH models to the data is that the prefactors to $\sqrt{\boldsymbol{E}}$, that is, the quantities $\sqrt{\frac{q\boldsymbol{E}}{\pi\varepsilon_i}} = 3.8\text{x}10^{-4}\ (\text{cm/V})^{1/2}$ (in FP) and $\sqrt{\frac{q\boldsymbol{E}}{4\pi\varepsilon_i}} = 1.9\text{x}10^{-4}\ (\text{cm/V})^{1/2}$ (in SH) should be the same for all three devices. Thus, one can fit the log (J/E) data at the range of $\boldsymbol{E}$ where the slope of the current is equal to the prefactor for FP or SH, respectively. In these devices, it is known that at low frequency (DC bias) ε_i changes by a small amount, as seen in the CV data of Fig. 3.3. However, keeping this quantity fixed for all three devices effectively bundles the differences in $\boldsymbol{E}$ and ε_i into the barrier value φ_b, enabling us to compare the *effective* differences in device operation due to the SAM layer. For FP and SH fits, 7-point moving average was used to evaluate the gradient of the data, and a region that minimized the difference relative to the above prefactor was used for the linear extrapolation. For SCLC devices, the same range of $\boldsymbol{E}$, equivalent to ($-1 \leq V_G \leq 1.5$ V) was used to fit all three devices.

Comparison of the Frenkel-Poole and Schottky models illustrates the form that the transformed current for each device should take, using Eqs. 3.12 and 3.17 as follows:

$$\frac{-kT}{q}\ln\left(\frac{J}{E}\right) = \varphi_{\mathrm{FP}} - \sqrt{\frac{q}{\pi\varepsilon_i}}\sqrt{E} \qquad [3.19]$$

$$\frac{-kT}{q}\ln\left(\frac{J}{A^*T^2}\right) = \varphi_{\mathrm{SH}} - \sqrt{\frac{q}{4\pi\varepsilon_i}}\sqrt{E} \qquad [3.20]$$

As can be seen in Fig. 3.6, the slope of the current is positive for data transformed into the Frenkel-Poole form, yielding an unphysical slope approximately equal to $-(2.1 - 2.7) \times 10^{-4}$ $(\mathrm{cm/V})^{1/2}$ and hence diodes in which current decreases with applied voltage. The negative slope is roughly 75% of the expected value. The fact that it is negatives raises the question of whether the behavior is true or pure coincidence. Observation of negative differential resistance in Ag/SiO_2/Pt junctions for resistive memory has been recently reported,[32] with devices exhibiting a differential negative resistance (DNR) over a range of several volts. The DNR is attributed to charging/discharging of Ag nanocrystals at the Ag/SiO_2 interface, where a high concentration of nanocrystalline grain boundaries act to trap charges that flow across the creation of charge-conducting filaments in the ultrathin SiO_2 layer. In light of the ultrathin, marginal quality SiO_2 layer in our devices, it is conceivable that a similar mechanism may be at work in our devices, reflected in the F-P curves and in the extracted barriers. However, the fact that the data only agree at very low fields indicates that FP isn't the dominant mechanism in this diode. Data transformed into $\log[J/(A^*T^2)]$ vs. $\boldsymbol{E}$ (Schottky) plots have slopes of the correct sign, with values for the field-lowering parameter of $\sim 2.2 - 2.4 \times 10^{-4}$.

All three devices do exhibit clear SCLC behavior at high fields ($V_G < -1$ V). The largest difference is seen in the voltage at which the onset of SCLC is observed for the three devices. The bare devices (Fig. 3.6(a)) are properly described by SCLC down to approximately -0.6 V, while for the SAM-treated oxides this value is successively higher for OTS (-0.90 V) and FOTS

(-1.10 V), respectively. Below -0.6 V, bare devices exhibit behavior some SH behavior. By comparison, OTS devices appear to follow the SH current more closely at lower voltages.

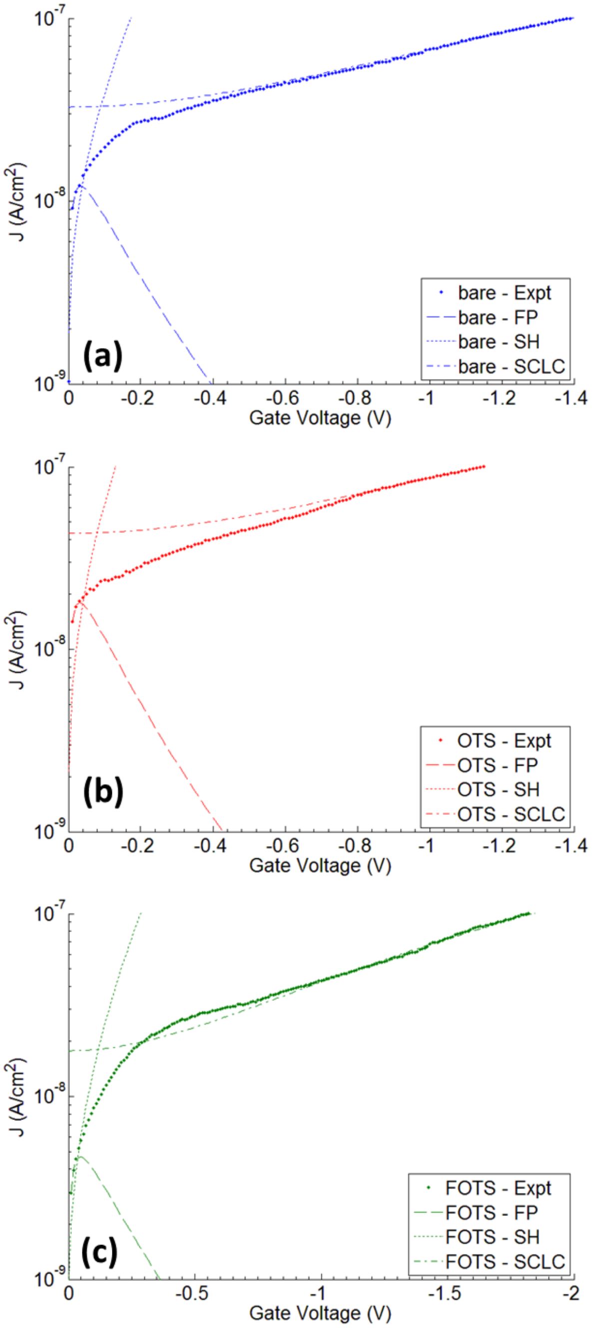

Figure 3.6 Analysis of nSi/PlasmOx(+SAM)/Au diodes using various conduction models for **(a)** bare, **(b)** OTS- , and **(c)** FOTS-treated plasma-grown oxides. Abbreviations *FP* – Frenkel-Poole; *SH* – Schottky; *SCLC* – Space charge-limited current. Note that V_G is negative.

Table 3.1 Comparison of extracted parameters for bare, OTS-, and FOTS-treated oxide MIS structures. Abbreviations *FP* – Frenkel-Poole; *SH* – Schottky; *SCLC* – Space charge-limited current.

Oxide surface	**φ_{SH} (meV)**	**$\Delta\varphi_{SH}$ (meV)**	**φ_{FP} (meV)**	**$\Delta\varphi_{FP}$ (meV)**	**σ_{sclc} (at 0 V) (S/cm) x10^{-12}**	**V_{sclc} (V)**	**ΔV_{sclc} (V)**
Bare	915	--	694	--	2.62	-0.63	--
OTS	912	-2.36	681	-1.25	3.46	-0.90	-0.27
FOTS	937	+22.2	727	+33.7	1.42	-1.10	-0.47

Notably, the barrier height differences $\Delta\varphi$ for SH are small for both OTS and FOTS, on the meV range, as seen in Table 3.1. The difference in signs for the two barriers, (-) for OTS and (+) for FOTS, are peculiar, because the OFETs presented in the last chapter indicated a trend of increasing V_T with increasing dipole (OTS → FOTS). However, we recall that OFETs fabricated on pSi, where $V_{bi} \approx 0$ V, also displayed current characteristics where OTS current was enhanced relative to bare oxides, while FOTS current was suppressed. Although these diodes are not at flatband condition like as they would be in on a pSi substrate, it is conceivable that the net effect of OTS on a surface may at times yield a negligibly positive effective dipole, the observation of which is obscured by various competing mechanisms within the full gate structure. This issue will be revisited in the following section when we estimate the density of surface states from CV characteristics of the gate stack.

8-2-Bn NTCDI OFET Gate Stack

To probe the influence of the SAM at the OSC interface, CV analysis of MIS diodes consisting of nSi/PlasmOx(+SAM)/40 nm 8-2-Bn NTCDI/Au was also conducted, as shown in Fig. 3.7. The most notable characteristic of these diodes is that above 25 Hz, the FOTS-treated devices exhibit greater capacitance than both bare and OTS-treated gate stacks, by as much as 15%. In addition, the OTS devices display a characteristic minimum near 0 V. In the case of inorganic MIS diodes, this feature would be associated with the formation of a depletion region at the semiconductor-oxide interface. The coinciding increase in the measured dissipation factor will be discussed in further detail below.

It is evident that the CV characteristics of the gate stack are not even qualitatively similar to those of the OSC-free structure, as now the Si gate serves the function of the metal in the MIS structure. In this structure, at $V_G < 0$ the Si/SiO$_2$ layer is biased so as to yield its highest capacitance. At the same time, $V_G < 0$ places the n-channel 8-2-Bn NTCDI semiconductor into depletion at the oxide/OSC interface. Conversely, $V_G > 0$ places the nSi/PlasmOx system in depletion, while accumulating carriers at the PlasmOx/OSC interface.

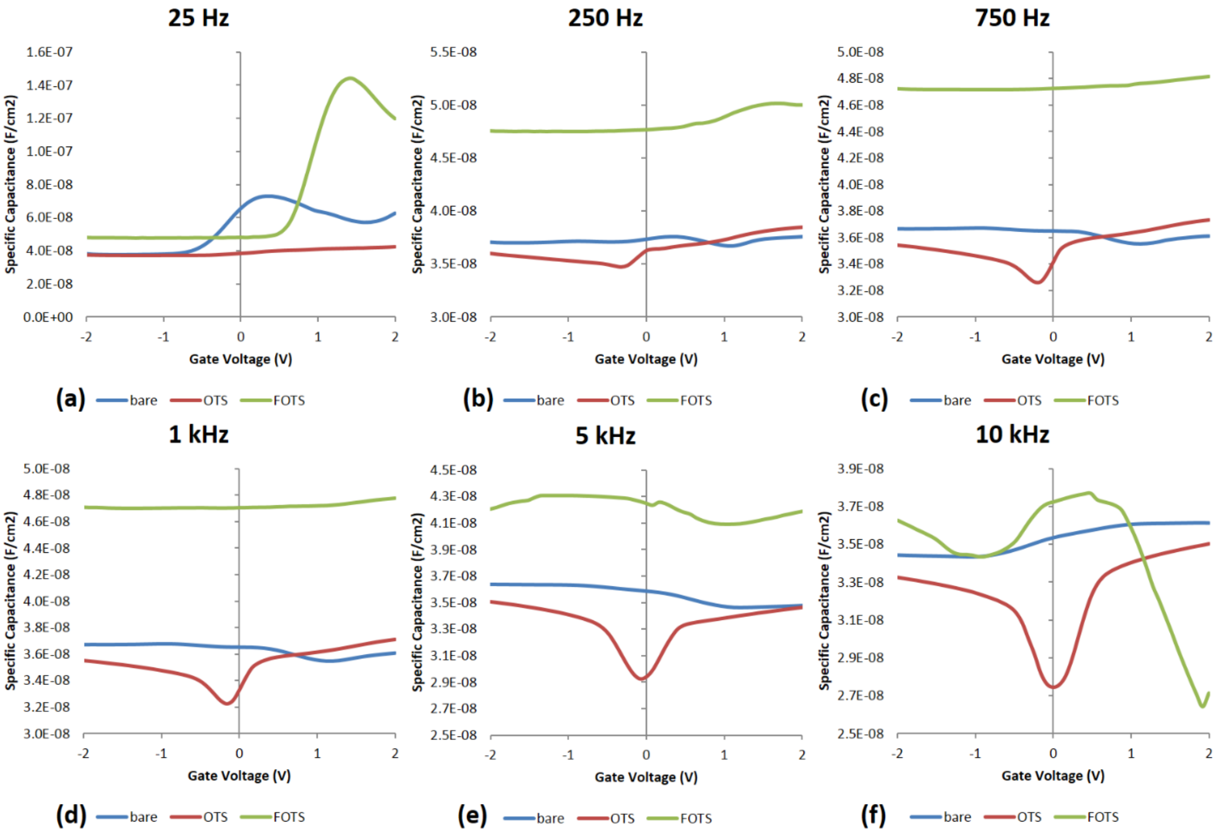

Figure 3.7 MIS diodes of 8-2-Bn NTCDI OFET gate stack. **(a)** 25 Hz, **(b)** 250 Hz, **(c)** 750 Hz, **(d)** 1 kHz, **(e)** 5 kHz, **(f)** 10 kHz.

One consideration in CV measurements of multilayer stacks is the response time of each layer to a rapidly applied field. The dielectric relaxation time is the amount of time it takes for an electronic carrier in a material to respond to this field. If the field varies on a time scale $(2\pi f)^{-1}$ smaller than the dielectric relaxation time, the carriers within the material will not be able to redistribute themselves to respond to the field. This value τ_d is determined by the ratio of the dielectric constant to the electrical conductivity, as

$$\tau_d = \frac{\varepsilon\varepsilon_0}{\sigma} \quad . \qquad [3.21]$$

For highly-doped nSi, $\tau_d \approx 10^{-12}$ s. For an OSC such as NTCDI, which contains a very small number of intrinsic carriers and few populated traps, $\tau_d \approx 10^{-4} - 10^{-5}$ s. This time constant implies a cutoff frequency for the 8-2-Bn NTCDI layer to respond to an AC field at ~15 kHz. Therefore, at frequencies above 15 kHz, we should expect that the 8-2-Bn NTCDI layer will behave more like an insulator, and the field will fall mostly linearly across the combined SiO_2(+SAM)/OSC layer, implying a greater contribution of any Si/SiO_2 depletion region to the CV characteristics. Below this cutoff frequency, we can expect that both the SiO_2/8-2-Bn NTCDI and Si/SiO_2 interfaces contribute to any capacitive interfacial effects. However, the poor quality of the oxide layer, as confirmed in the CV data from the previous section, suggest that the oxide would likely conduct before the electric field across it was sufficient to create a depletion region at the Si/SiO_2 interface.

Table 3.2 Device and material parameters for MIS structures investigated. *d* is the layer thickness, μ_{FET} is the field-effect mobility, μ_i is the intrinsic mobility, and ε is the dielectric constant of the film.

Material	*d* (nm)	μ_{FET} (cm^2/Vs)	μ_i (cm^2/Vs)	ε
nSi	∞	1200	11.9	11.9
SiO_2	2-15	$< 10^{-10}$	3.9	3.9
8-2-Bn NTCDI	40	10^{-1}	10^{-4}	2-4
5FPE NTCDI	100	10^{-1}	10^{-5} - 10^{-4}	2-4

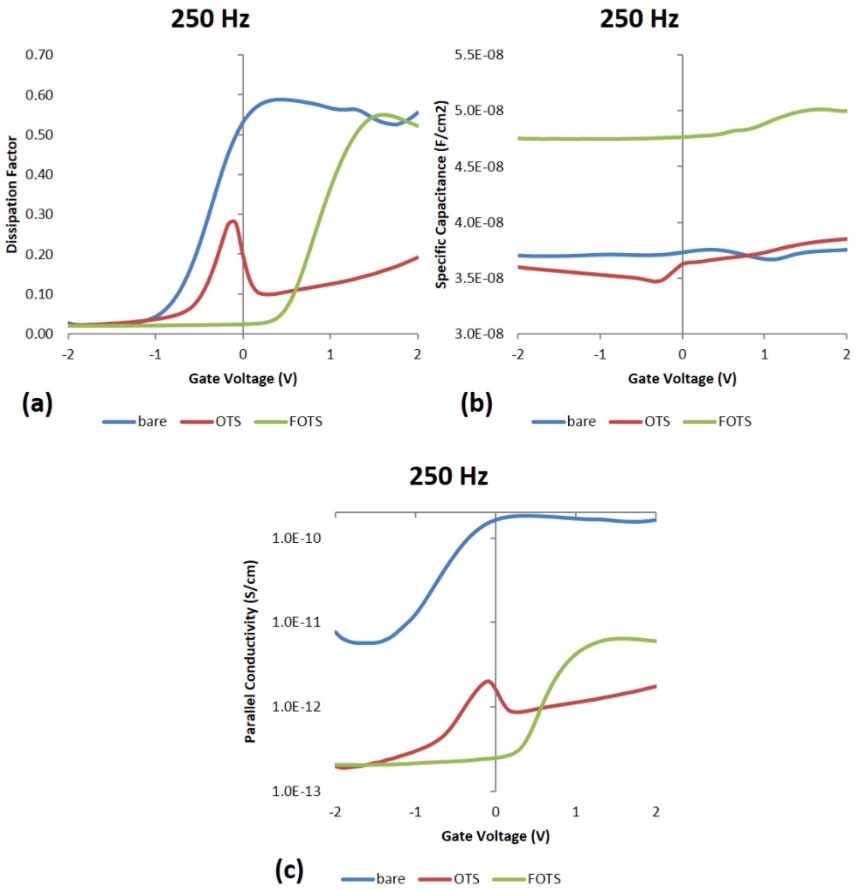

Figure 3.8 (a) Dissipation, **(b)** capacitance, and **(c)** parallel conductivity of 8-2-Bn NTCDI gate stack at 250 Hz.Note that dissipation increases above -1V for the bare device, consistent with the expected V_{FB} of the full structure.

In the case of the bare oxide structure, it is expected that the 8-2-Bn NTCDI layer will be in accumulation at equilibrium (0 V), due to the built-in potential between the $E_{F,\ nSi}$ (~4 eV) and φ_{Au} (~5 eV). At $V_G \approx -1$ V, the gate stack should be at its flatband voltage (V_{FB}). In the bare oxide devices in Fig. 4.8 we see a large increase in the dissipation near $V_G = -1$ V, with this point at more positive voltages for OTS and FOTS, respectively. This trend in the shift of the onset of dissipation is qualitatively similar to the shift in V_{to} for the OFETs discussed in the previous chapter. Increases in dissipation factor reflects an enhancement of conductive behavior across the device (Eq. 3.5), and so it is reasonable to assume that this indicates conduction across the oxide at $V_G > V_{FB}$. In effect, this trend reflects a shifting of the V_{FB} in the SAM-treated device, and is in reasonable agreement with the findings of the Bao group on Al/AlOx OFETs.[16]

A minimum in the capacitance is observed for the OTS layers near -0.25 V (Fig. 3.8). In doped elemental semiconductors like Si, this capacitance minimum is attributed to the formation of a depletion layer within the structure,[21] created as majority carriers are drawn from regions experiencing high electric fields as in the vicinity of the Si/SiO_2 interface. We can eliminate the Si/SiO_2 interface as the source of this depletion region, as the only C_{min} valley observed in the OSC-free diodes was at very low frequencies, while this C_{min} in OTS devices is seen at up to 10 kHz. The absence of this feature in the dissipation of FOTS devices suggests a difference in mechanism by which the two SAMs modify the oxide-SAM interface.

Side note: Morphology vs. Dipoles

One possible explanation is proposed in the work by the Heremans group discussed previously. Their simulations of the electrostatic effect of SAMs at the SiO_2/OSC interface within pentacene OFETs indicated that while both SAMs reduce V_{to} and V_T, the calculated channel carrier densities for the SAM-treated devices varied widely. Namely, devices with FOTS-treated SiO_2 displayed 10^2 more channel carriers than in OFETs on bare oxide, while OTS-treated devices showed a 50x reduction in carrier density relative to bare oxide.[20] One aspect considered by Heremans is that OTS and FOTS may change the energetic DOS within the OSC at the interface, thereby changing the effective Fermi level there. However, a decrease in carrier concentration is only consistent with a shifting away from the E_F of the OSC, suggesting that more than one mechanism may be at work in the case of OTS-treated devices.

The possibility that V_T could be reduced in OTS devices without the addition of carriers supports the growing body of evidence[5,33,34] that a major component of the effect of OTS on OSC electronic properties arises from the changes in morphology at the SAM-OSC interface. First, the measured surface potential for OTS-treated oxides measured by our group and others[12] has been shown to be quite small, on the order of ~10mV as compared to the ~10x larger FOTS surface potential. In addition AFM images in Chapter 2 of NTCDI on OTS-treated substrates indicated larger and more interconnected grains within the 1st and 2nd layers at the surface. Larger grain sizes would reduce the number of grain boundaries and other structural imperfections that would trap carriers, it would be plausible for this morphological effect to be improperly attributed to a dipole. As the Horowitz group has pointed out that traps have a similar effect as bend bending in OSCs,[35] a reduction of traps could be interpreted as the presence of an interface dipole.

This argument is further supported by the measurements of mobility of bare-, OTS-, and FOTS-oxide OFETs. Increases in the field-effect mobility for NTCDI (Chapter 2) and pentacene[20] show a marginally higher mobility for OTS devices than for FOTS. Since these mobilities reflect conductance *along* the insulator/OSC interface, grain boundaries will adversely impact the channel conductivity.[33,34] If we are to believe the model of Heremans, then a higher net mobility with a lower density of carriers suggests a large increase in apparent mobility. This conclusion is supported by work by the Horowitz group, which has modeled the effect of grain boundaries on the mobility of holes in pentacene assuming a tunnel-emission barrier for the grain boundary,[36] of the form

$$\mu = \frac{qL_G}{h}\sqrt{\frac{2q}{\pi C_i V_G}}\,e^{-\frac{2L_{GB}}{\hbar}\sqrt{2m^*E_b}} \qquad [3.22]$$

where fundamental quantities are: q, the fundamental charge; h and $\hbar$ are Planck's constant and reduced Planck's constant, respectively; and m^* is the carrier effective mass. Device and material parameters are the mobility μ, the grain length L_G, the specific capacitance C_i, gate voltage V_G, and grain barrier energy E_b. This model indicates a linear increase in the mobility with grain size (L_G), but an exponential decrease in mobility with grain barrier length (L_{GB}) and grain boundary energy barrier (E_b). Assuming an identical type of grain boundary of fixed length, then reducing the number of grain boundaries increases L_G nearly exponentially. This helps partially explain the increase in mobility with improved morphology. Tuning of the barrier height E_b by any interface dipole will also play a significant role in tuning the mobility. However, decoupling morphology from interfacial dipole effects requires measurements on single crystals,[37] the fabrication of which remains an area of intensive engineering effort.

Depletion regions arise in a semiconductor where the local carrier mobility is lower than in the rest of the material. As a result, resistivity in that region is higher than in the rest of the bulk. Revisiting the AFM images of the previous chapter, we see that the morphology of NTCDI on FOTS-treated substrates at ~15nm consists of small grains, similar to bare-oxide devices. Considering that at 40 nm all three devices appear to have similar morphology, it is fair to assume that the bare and FOTS devices consist of one uniform morphology, while OTS devices consist of a smooth NTCDI film in series with a rougher one on top. This mobility mismatch could create a depletion region within an internal boundary in the NTCDI.

Diodes Comparison

Diodes if the 8-2-Bn gate stack were fabricated and tested over a range of voltages similar to that used in the OFET structures. The results are shown in Fig. 3.9. The diode measurements reveal a large degree of hysteresis in the curves, both in the voltage corresponding to J_{min} as well as in the magnitude of the currents at $V_G < 0$. All the curves clearly display a region of DNR just below the J_{min} when swept from $V_G = +2V$ → -2 V. The fact that this DNR is present in all of the devices indicates that it arises from traps in the oxide, as suggested in the analysis of the OSC-free diodes. As a consequence the hysteresis of the position of J_{min} is likely attributable to a charging of the oxide layer.

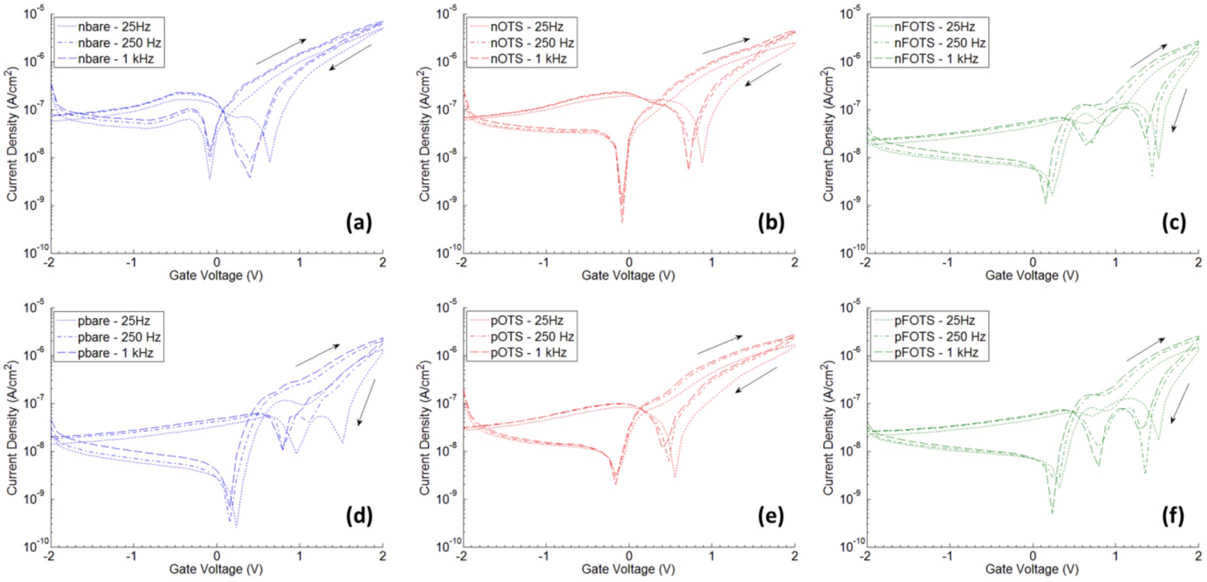

Figure 3.9 Diodes of Si/PlasmOx(+SAM)/40 nm 8-2-Bn/Au. **(a)** nSi/PlasmOx, **(b)** nSi/PlasmOx+OTS, **(c)** nSi/PlasmOx+FOTS, **(d)** pSi/PlasmOx, **(e)** pSi/PlasmOx+OTS, **(f)** pSi/PlasmOx+FOTS. Initial point is $V_G = -2$ V. Averages of 9-12 devices each.

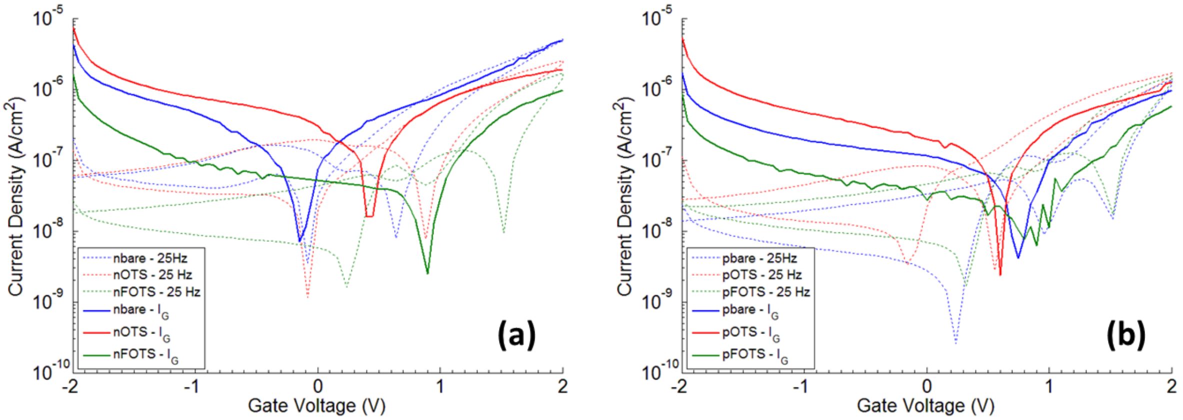

Figure 3.10 Comparison of leakage current density JG and diodes from Fig. 3.9 on **(a)** nSi, and **(b)** pSi.

This finding is consistent with the idea that the gate materials used—heavily-doped Si with a thin oxide—act as two diodes at the interface. The most telling feature of this behavior can be seen in the locations where the current density J is minimum (J_{min}). We first examine nSi devices. When V_G is swept from negative to positive, J_{min} is approximately the same for bare and OTS devices (near -0.1 V), and only marginally larger for FOTS (+0.1 V). When swept from positive to negative, J_{min} is shifted to +0.5 V for bare devices, +0.8 V for OTS, and +1.5 V for FOTS.

The most notable result is that the curves for the gate stack diodes share a striking similarity to the transfer curve leakage I_G of OFETs, shown in Fig. 2.8 of Chapter 2. Comparison to the I_G curves of Fig.2.8 is shown in Fig. 3.10, revealing that $I_{G,min}$ occurs at a value about equal to the averages of J_{min} for positive and negative sweeps. It appears peculiar that the leakage current density I_G closely tracks the average of the forward and reverse diode currents at $V_G > 0$, but is much higher than the diode currents at $V_G < 0$. The most obvious difference between these two structures is that in the OFET, the effective area of electrostatic interaction between the top contact and the Si gate is necessarily equal to the effective area of the Au contact pad at all voltages, as there is a potential gradient across the OFET channel between the source and drain electrodes. Consequently, when $V_G < 0$ the Gate-Drain structure will be in forward bias, and electrons flowing from the Si layer across the oxide will feel a potential both below the Au contact pad and at a distance within the channel, so that the effective contact area for gate leakage is larger near the drain electrode.

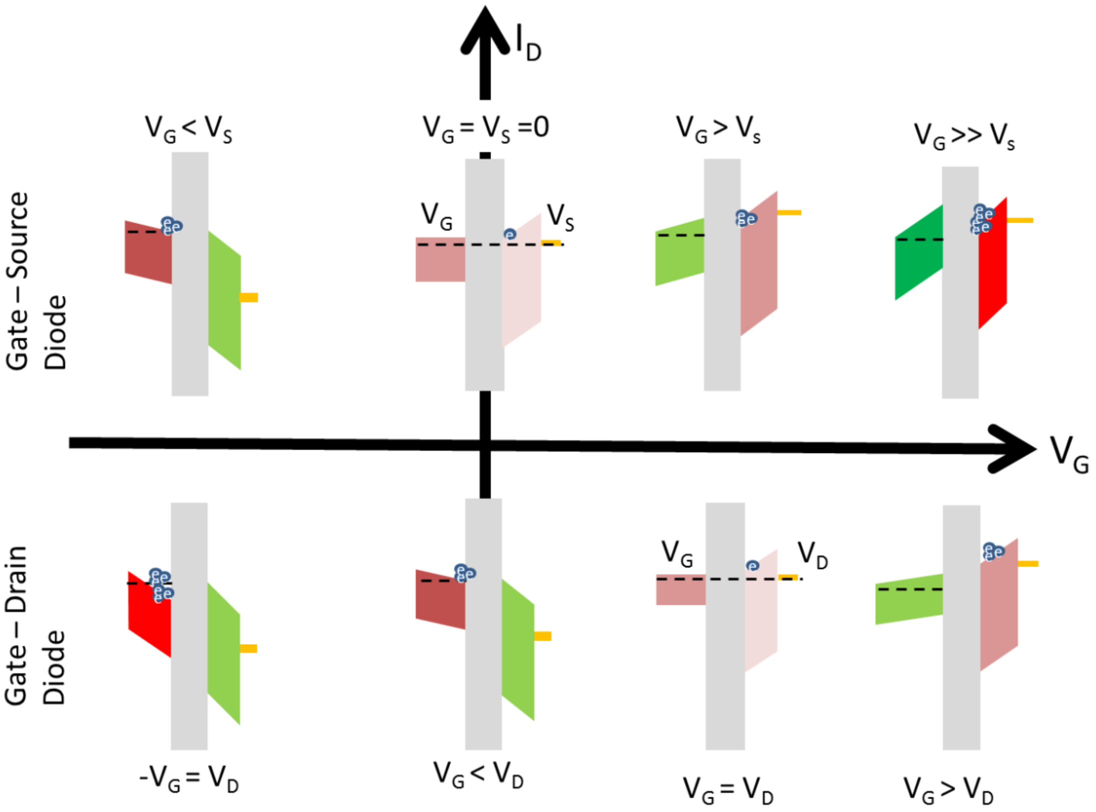

Figure 3.11 Illustration of Gate-Source and Gate-Drain diodes during biasing in a transfer curve measurement. Brighter red indicates greater negative charge (electron accumulation), and brighter green indicates greater positive charge (electron depletion). As V_G is swept from negative to positive, the Gate-Source structure forces the NTCDI into greater accumulation than at the Gate-Drain electrode. In addition, the nSi is more depleted of electrons at the oxide interface, creating a greater positive space charge under the NTCDI than at the Gate-Drain electrode.

A significant finding in these diode measurements is the observation of frequency dependence in both the value of J_{min} and its corresponding voltage. An increase in the V_G pulsing frequency results in a negligible shift in the J_{min} when swept toward positive V_G, but a much more pronounced (~0.2 V) shift in J_{min} when swept towards negative V_G. For every device studied, the measurements at 25 Hz result in a shifting of J_{min} towards more positive V_G. As the frequency increase, carriers are bypassing trap states with long time scales. It is notable that this shift is reduced in the devices with SAM-treated oxide. Because this shift occurs when moving the device from NTCDI accumulation ($V_G > 0$) towards negative V_G, it is associated with an effect of the SAM layer on carriers within the NTCDI attempting to cross into the oxide.

This conclusion is supported by observation of a 2nd region of DNR where $0.75\ \mathrm{V} \leq V_G \leq 1.5\ \mathrm{V}$. As previously discussed, one underlying cause for DNR is the formation of a depletion region within a section of material along the path of carrier transport. The evidence of this region in the bare pSi (Fig. 3.9(d)) is a useful control, since the Si/Au structure should be near flatband condition at equilibrium. This feature corresponds to the onset of electron injection from NTCDI into the oxide, as the difference in potential relative to 0 V is nearly equal to the expected potential difference between the NTCDI LUMO (-4 eV) and the pSi/Au energy levels (~ -5 eV). Thus, the presence of this region in the nSi-FOTS diode can be interpreted as a vacuum level shift in the energy at which the NTCDI interface is equilibrated with the oxide surface. However, the diodes of pSi-FOTS are inconsistent with interpretation of the SAM dipole as strictly a vacuum level shift, since they appear to have the same V_{FB} as pSi devices—a result reflected in the similar V_T's of pSi-bare and pSi-FOTS OFETs in the previous chapter.

5FPE NTCDI Gate Stack

In a separate set of experiments, comparable gate stacks consisting of nSi/PlasmOx(+SAM)/100 nm 5FPE NTCDI/Au were fabricated and tested across a similar range of frequencies. However, as these devices were intended for charge-extraction measurements (discussed in detail in the next section), there are several differences relative to the OFET gate stacks. First, the PlasmOx layer was grown thicker (~10-15 nm instead of 7-10 nm) in an O_2 plasma for 10 minutes instead of 5 min, but with a similar post-plasma anneal at 200 °C for 2 hrs. The OSC layer consists of 5FPE NTCDI (Fig. 3.12); this semiconductor was chosen because it was more readily available—and in larger quantities—than the 8-2-Bn used in the previous experiments. The thickness of the NTCDI layer is 2.5x greater than in the OFET experiments, as charge extraction requires a greater film thickness as will be detailed below. However, the HOMO and LUMO levels of 5FPE NTCDI are approximately the same as those of 8-2-Bn, and previous research by our group[38] has shown that it also follows 2-D island growth morphology under similar physical vapor deposition conditions.

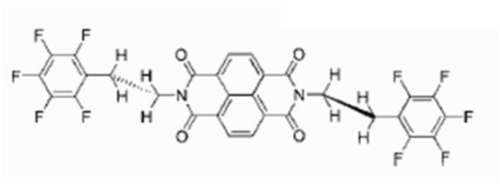

Figure 3.12 The n-channel small molecule 5FPE NTCDI.

Measurements of capacitance and dissipation in these 5FPE NTCDI MIS diodes revealed similar behavior to the 8-2-Bn NTCDI devices, as shown in Fig. 3.13. Although scanned across a smaller voltage range than the 8-2-Bn diodes, we note that dissipation in SAM-treated devices increases at higher voltages than for bare oxide devices. In addition, all three device types exhibit an area of rapid change in dissipation with a trend that follows the magnitude of the SAM dipole, as bare (-0.35 V), OTS (-0.2 V), and FOTS (-0.1 V). Insofar as the dissipation reflects conduction across the gate stack, these features demonstrate a shifting in the conduction across the gate stack with application of molecular dipoles.

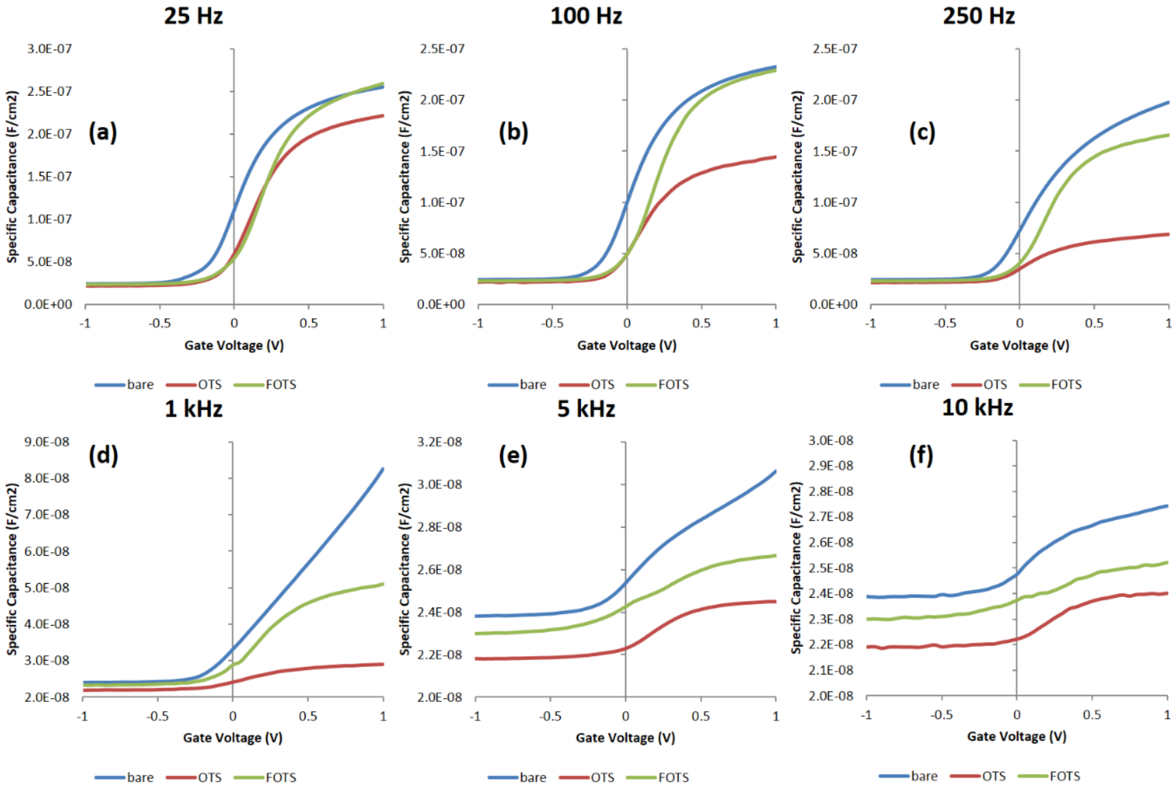

Figure 3.13 Capacitance measured for MIS Diodes with 100 nm 5FPE. **(a)** 25 Hz, **(b)** 100 Hz, **(c)** 250 Hz, **(d)** 1 kHz, **(e)** 5 kHz, **(f)** 10 kHz. Data corresponds to capacitors using capacitor electrodes (larger device).

In contrast to the 8-2-Bn gate stacks, the 5FPE MIS diodes display capacitive responses that are highly similar at low frequencies with the exception of a voltage shift between the bare and SAM-treated devices. This kind of shift in the CV characteristics of an MIS diode is generally attributed to the presence of surface states at the semiconductor-insulator interface.[21] We can estimate the density of surface states at the interface from CV data by rewriting Eq. 3.3 in terms of surface states as

$$\Delta Q_{ss} = C_i \Delta V \qquad [3.23]$$

where ΔQ_{ss} is the total charge on surface states, and ΔV is the voltage difference between two capacitance curves. To obtain the ΔV values for this analysis, we take C_i to be the capacitance of the "pristine" bare device, and subtract the voltage difference between the bare and SAM-treated devices at the same capacitance. By taking the derivative of the resulting curve with respect to the applied voltage we can obtain a density of surface states per unit energy N_{ss}, given as

$$N_{ss} = \frac{1}{q}\left(\frac{\partial Q_{ss}}{\partial \psi_s}\right)_V \qquad [3.24]$$

where ψ_s is the reference surface voltage of the pristine bare oxide device. In order to calculate the ΔV versus V curves numerically, MATLAB was employed to perform a reverse interpolation using a cubic spline to generate equally-spaced points on the capacitance axis. For each frequency, the capacitance range for these interpolated points was determined by the minimum and maximum capacitances of the bare,OTS and FOTS set. After finding the differences ΔV, the numerical gradient of each ΔV vs V curve was used to generate plots of N_{ss}. These N_{ss} plots were then fit to model consisting of two Gaussian distributions, as

$$N_{ss} = \sum_{i=1}^{m} N_i e^{-\left(\frac{\left(\varepsilon-\varepsilon_{0,i}\right)^2}{2\sigma_i^2}\right)} \qquad [3.25]$$

where N_i is the initial surface state concentration, $\varepsilon_{0,i}$ is the energy center of the i^{th} Gaussian, and $\sigma_{0,i}$ is standard deviation, also known as the energy broadening parameter. A 2-Gaussian model would be suitable to assess effects at the two interfaces of interest: the oxide/SAM interface and the SAM/OSC interface. However, the fact that the CV data are not perfectly offset, combined with high leakage currents at low voltage, precludes from analysis the CV data presented in Fig.

3.7. Surface state densities from capacitance curves at 25 Hz for round capacitor contact pads (those of Fig. 3.13) are presented in Fig. 3.14.

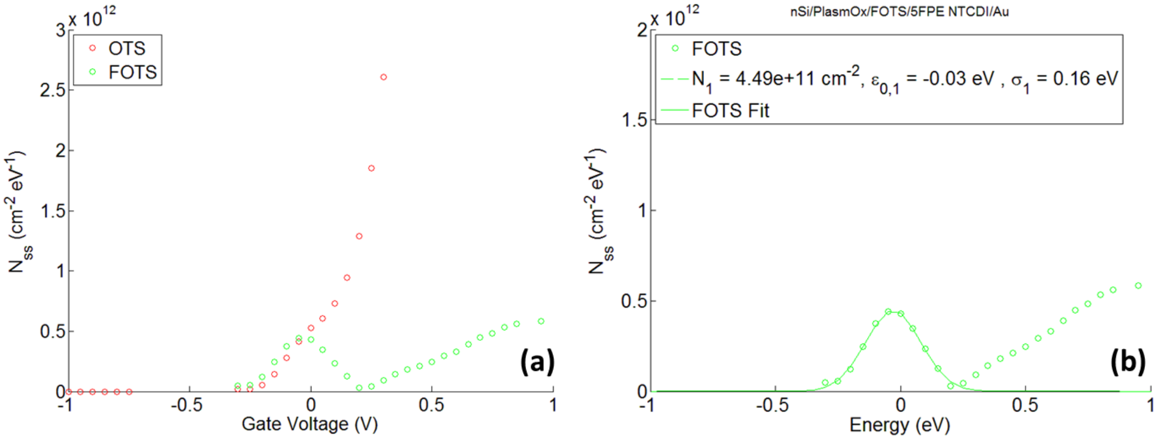

Figure 3.14 Surface state density calculated from Eq. 3.6 using CV data at 25 Hz presented in Fig. 3.13. **(a)** OTS and FOTS surface states. **(b)** FOTS fit to a single Gaussian model. Energy is referenced to the gate potential V_G (V on Si substrate). Data corresponds to round capacitor pads (large device).

The calculated N_{ss} distribution FOTS is shown in Fig. 3.14(b) and is suitably described by a single Gaussian. The calculated density of 4.5x10^{11} is quantitatively comparable to calculated values for the SAM-treated surface state density in Chapter 2. While this distribution is centered very close to zero, the standard deviation of the distribution is found to be 0.16 eV. While a direct quantitative comparison with the work of Heremans has not been undertaken for the n-channel NTCDI system, these values fall within a reasonable range for SAM-introduced energetic disorder. We also observe an increase in the surface states near 0.25 V. This potential marks a crossover point where the measured capacitance of FOTS devices increases relative to the bare devices (Fig. 3.13(a)). By comparison, the extracted N_{ss} for OTS devices is not well modeled by a Gaussian, as the capacitance does not follow a shape similar to the bare devices, but instead pleateaus at a lower value (Fig. 3.13(a)).

To examine the reproducibility of this data, OFETs were fabricated with the same structure as these. The only major difference between these two sets of data is the smaller contact area of the OFET capacitors (0.03 cm^2) compared to the capacitors examined in Fig. 3.13 (0.07 cm^2). The results are presented in Fig. 3.14, for which it was possible to obtain fits at 100 and 250 Hz (CV data is not shown). Within this set of data, both OTS and FOTS display similar surface state densities comparable to both our calculated values in Chapter 2 using the OFET V_T data, as well as with others' work.[12] It is seen that the surface state concentration of OTS devices is marginally higher than for FOTS at both frequencies, an observation that matches the extracted trend in V_T for OFETs tested on this film sample. Data at 250 Hz show that both OTS and FOTS display nearly identical σ and ε values, with the only difference being a larger initial surface state concentration N (Fig. 3.15(f)).

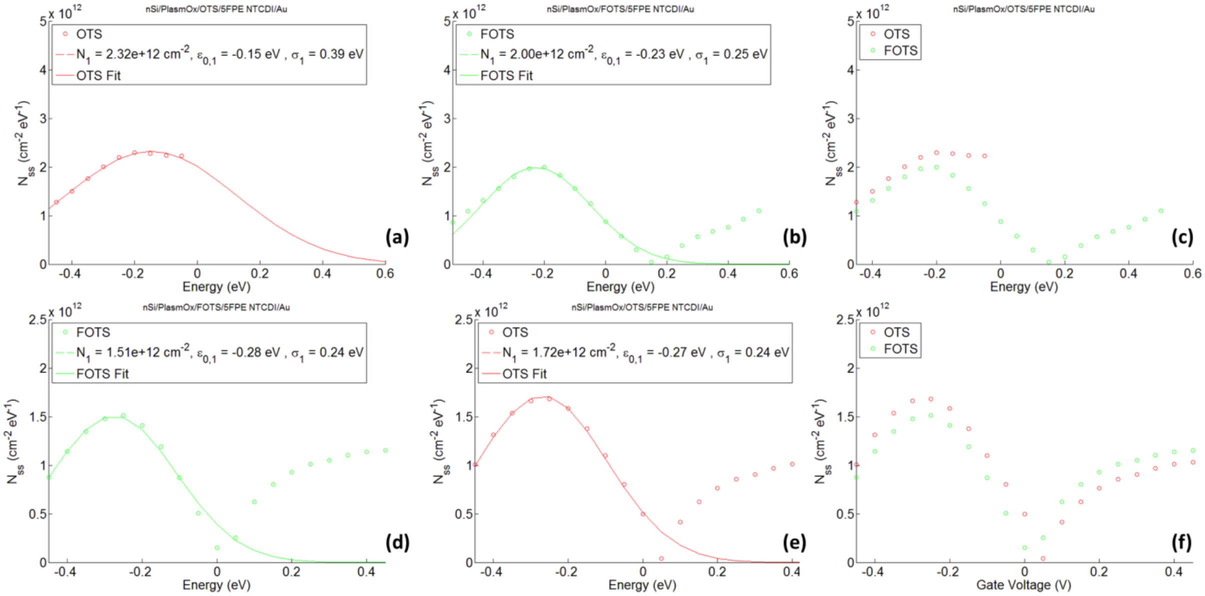

Figure 3.15 Fits of CV data presented in Fig. 3.13 using Eq. 4.25. **(a)** OTS, 100 Hz, **(b)** FOTS, 100 Hz, and **(c)** comparison of OTS and FOTS, 100 Hz. **(d)** OTS, 250 Hz, **(e)** FOTS, 250 Hz, and **(f)** comparison of OTS and FOTS, 250 Hz. Data corresponds to capacitors using OFET (smaller) electrodes.

The finding that in these samples the only notable difference between OTS and FOTS is the surface state density is in good agreement with OFET-based estimates of SAM-induced trap densities. However, it should be noted that this analysis assumes that the oxide surface states are unchanged with SAM adsorption. Measurements at 25 Hz, while at a low voltage sampling density, suggest that the OTS and FOTS surface state energetic disorder and energy centers are in fact different. Unfortunately, this low sampling density at intermediate frequencies between 25 and 250 Hz restricts our ability to make definitive conclusions about the frequency dependence of these parameters. However, work by Jung[39] and Ireland[40] in our group, as well as by the

Podzorov[41] group, has demonstrated a frequency dependence of the charge carrier mobility and channel transconductance in OFETs. In these works, the increased frequency of V_G was found to reduce the time-averaged charge carrier density at the insulator/OSC interface, enabling carriers to avoid deeper, long-lived trap states as compared to the OSC bulk. In the OFET-electrode devices of Fig. 3.15, the differences in surface state density only found at lower frequencies would hint at a frequency-dependence of the SAM-induced trap states.

In spite of the rich information that can be determined about a surface using OFETs,[42] most of the information that can be extracted from transfer measurements relate to differences in carrier transport *parallel* to the insulator/OSC interface, and as such do not capture changes in the vertical mobility of charge carriers. In the next section we explore the use of charge extraction to evaluate changes in the drift mobility of electrons in NTCDI on bare and SAM-treated oxides.

Charge Extraction in a Linearly-Increasing Voltage

Charge extraction in a linearly increasing voltage (CELIV) is a technique that leverages the characteristics of the transient current of a device to obtain information about the equilibrium charge carriers and dynamics in a two-terminal electronic device. In a CELIV measurement, a voltage ramp A with a maximum voltage U_{max} is applied over a time t_{pulse}, as shown in Fig. 3.17. The response voltage is measured on an oscilloscope in parallel with a resistor of a known value, so that the response current density is

$$j = \frac{U_{max}}{R_{laod}S} \qquad [3.26]$$

where R_{load} is the known resistance and S is the device area. The starting voltage of the ramp can be selected by choosing an appropriate U_{offset}, so that the range of the pulse is from $U_{offset} \rightarrow U_{max} - U_{offset}$, as shown in Fig. 3.16(a). The current response of the device yields two components, as indicated by Fig. 3.16(b). The lower square response current indicates a charging of the device, effectively the geometrical capacitance of the device. This current serves as the reference current in the analysis, and is called $j(0)$. The additional "hump" of current above $j(0)$ corresponds to the extraction of equilibrium carriers in the device, and is called Δj.

It should be noted that there are very strict requirements on device characterization using CELIV. First, one of the electrodes must be blocking. That is, the work function or E_F of the electrode should be selected so as to present a barrier to charge transport across it, effectively accumulating carriers. As the potential at the opposite electrode is swept, these accumulated carriers can be extracted. In the case of our MIS structures, the V_{bi} between nSi and Au forces accumulation of carriers in the NTCDI layer at the oxide interface. The oxide interface, although leaky, does provide a high degree of blocking, as seen from the effective accumulation of carriers in our OFET devices.

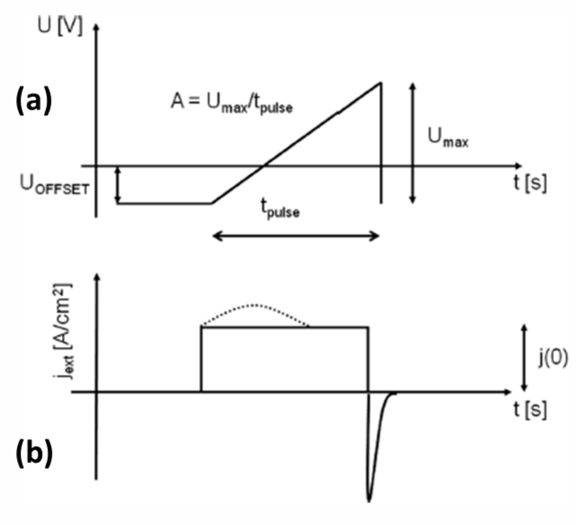

Figure 3.16 (a) Energy schematic of a CELIV measurement. **(b)** Current response of the applied voltage ramp *A*. Image adapted from Ref. 43.

Developed by Juška as a complementary method to time-of-flight measurements of highly conductive materials[44] including amorphous Si, the CELIV technique has recently been widely applied in the study of bulk-heterojunction photovoltaics. By applying a pulse of light prior to the application of the voltage ramp *A*, researchers have employed the CELIV framework to understand the role of intrinsic traps[37,38] that determine the efficiency of organic solar cells,[45,46] as well as the effect of externally-induced traps such as oxygen and moisture degradation.[47] Recently, Juška also reported the use of CELIV to investigate both the vertical and channel mobilities in hole-transporting OFETs.[48]

In collaboration with the Österbacka group, we have applied the technique to the study of electron transporting organic MIS diodes on an Al/AlOx to measure the vacuum-level shift of two dipolar self-assembled monolayers (SAMs), octyl-triethoxysilane (OTS) and perfluorooctyl-triethoxysilane (FOTS) (See Appendix B). In our previous study, the thickness of the native

AlOx was sufficiently small so as to enable a high [leakage] current across the insulator. This large current, arising from a high number of trap states in the oxide, resulted in current transients consisting of only displacement currents—that is, we could only observe the charging of the thin oxide. Differences in the measured displacement currents revealed a fixed voltage shift between bare, OTS, and FOTS treated oxides of roughly +0.45 V and +0.75 V, respectively. As a consequence, the absence of an extraction current of equilibrium charge carriers precluded analysis of how the SAMs affect the vertical charge transport in the OSC. In this section, we assess the effect of SAMs at the oxide/OSC interface using CELIV.

The capacitors tested in the previous section, consisting of nSi/PlasmOx(+SAM)/100 nm 5FPE/Au, were tested under vacuum (< 10^{-5} Torr) and in complete darkness in a Janis vacuum probe station. CELIV pulses were applied with an Agilent 33220A Function Generator and measured using an Agilent DSO3062A digital oscilloscope 1200 points per measurement. The delay time between pulses was set to 1s, to ensure that the device was equilibrated at U_{offset} prior to application of the voltage ramp. Each measurement was averaged over 20-25 samples. The measurements presented are the average of 6-7 devices for each substrate type.

In the absence of a lock-in amplifier, a load resistor of 50 kΩ was used to ensure that the voltages measured across R_{load} were sufficiently high to be measured on the oscilloscope. Using the CV measurements from the previous section, the RC time constant of the structure was estimated to be 0.6-1 ms. By comparison, the expected transit time $t_{tr} = \frac{d^2}{\mu_{drift} U_{max}}$, for our device thickness d = 100 nm, and a drift mobility ~1×10^{-6} is in the same range of 0.5 ms. Our estimates of the drift mobility μ_{drift} are from calculations based on Au-NTCDI-Au diode measurements ($\sigma_{drift} = 1 \times 10^{-6}$ S/cm) and our findings for 5FPE in the Al/AlOx/5FPE/Au system ($\mu_{drift} = 3 \times 10^{-5}$ cm^2/Vs). It is known that the field-effect mobility μ_{FET} in OSCs is as much as 10^6 greater than μ_{drift}, and calculations of the mobility from OFETs fabricated with the same vertical structure yielded $\mu_{FET} = 1 - 3 \times 10^{-2}$ cm^2/Vs. As such, our estimate of t_{tr} is near the threshold requirement for CELIV that $t_{tr} < \tau_{RC}$.

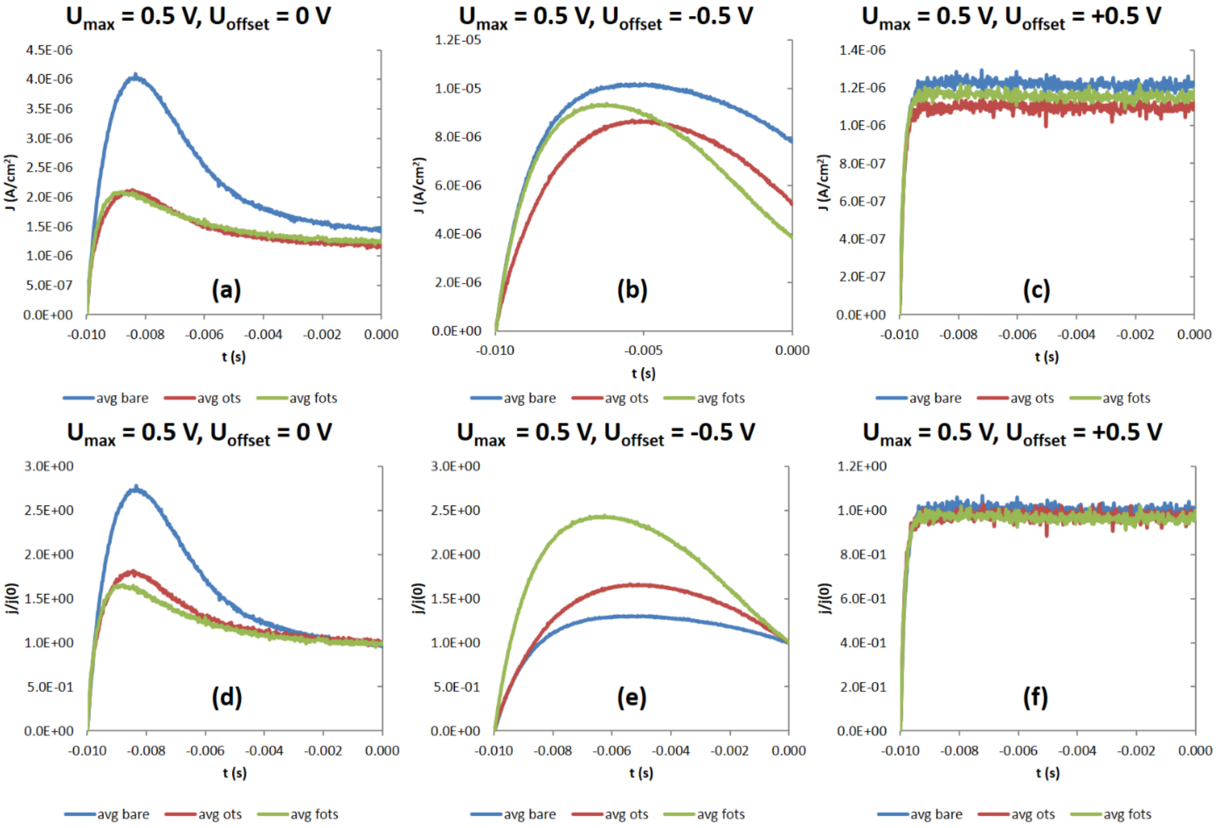

Figure 3.17 Extracted current transients for nSi/PlasmOx(+SAM)/100 nm 5FPE/Au structures. Voltage ramps of U_{max} = 0.5 V for **(a)** 0V, **(b)** -0.5 V, and **(c)** +0.5 V, respectively; and currents are normalized by the current j(0) **(d)** 0V, **(e)** -0.5 V, and **(f)** +0.5 V, respectively. All voltages are relative to the top Au contact.

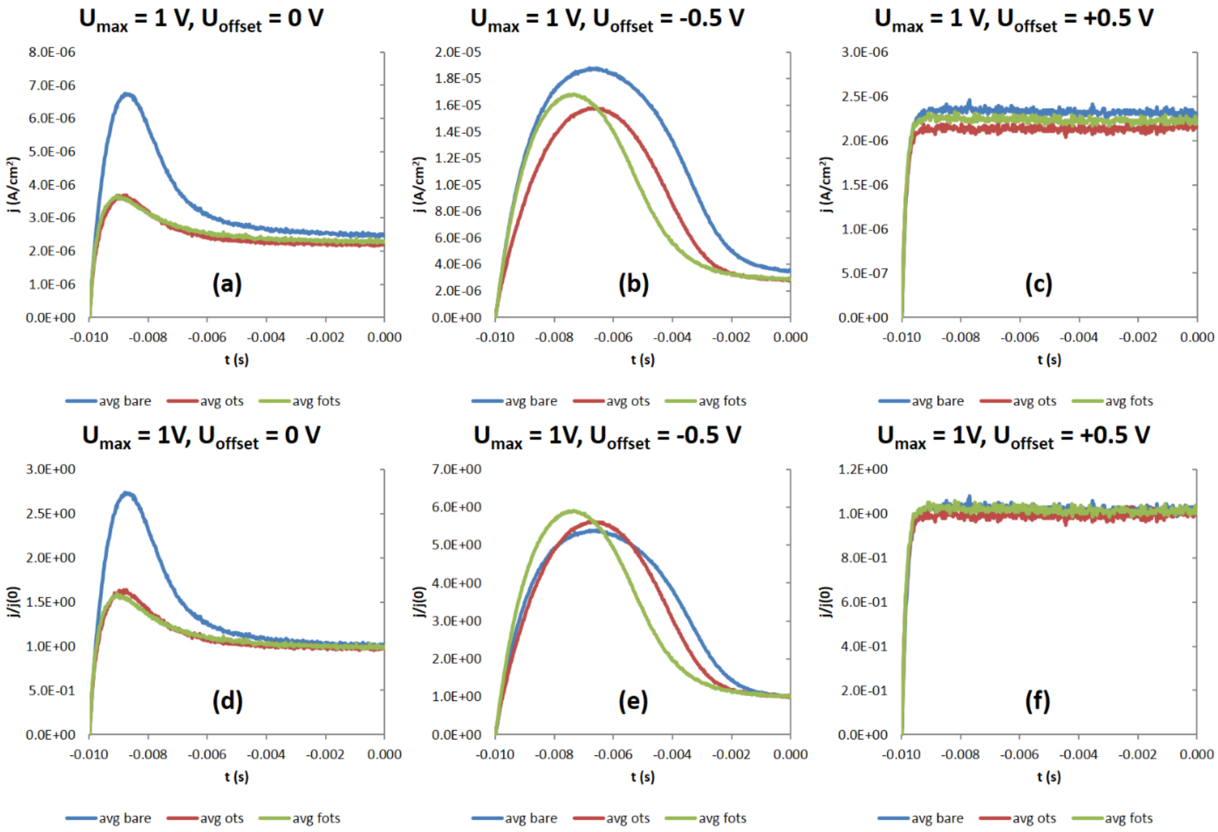

Figure 3.18 Extracted current transients for nSi/PlasmOx(+SAM)/100 nm 5FPE/Au structures. Voltage ramps of U$_{max}$ = 1 V for **(a)** 0V, **(b)** -0.5 V, and **(c)** +0.5 V, respectively; and currents are normalized by the current j(0) **(d)** 0V, **(e)** -0.5 V, and **(f)** +0.5 V, respectively. All voltages are relative to the top Au contact.

As clearly seen from Fig. 3.17, at 0 V both the OTS and FOTS layers display a markedly reduced extraction current as compared to the bare oxide devices at equilibrium (0V offset, Fig 17(a, d)). In addition, the time t_{max}, corresponding to the maximum current j_{max}, is shifted to smaller times for FOTS and OTS, respectively. This shift can be related to a difference in mobility, as calculated by Juška[44] for the condition where $\Delta j = j(0)$, as

$$\mu = \frac{2d^2}{3At_{max}^2\left[1+0.36\frac{\Delta j}{j(0)}\right]} \qquad . \qquad [3.27]$$

Using the fact that $\Delta j \approx j(0)$ as seen in Fig. 3.17 (d-e), we can employ Eq. 3.26 to find the differences in drift mobility for NTCDI on bare and SAM-treated oxides, summarized in Table 3.3 below. Although using only two ramp rates *A*, a clear trend emerges for the mobility as a function of ramp rate and offset voltage. At equilibrium (U_{offset} = 0V), the OTS and FOTS yield higher mobilities for the 5FPE, with FOTS yielding a 2 – 2.5x increase for both ramp rates. Upon equilibration at U_{offset} = -0.5V, we see a smaller increase in the mobility for FOTS (20-40%), but observe a small decrease in the mobility for OTS devices at both ramp rates relative to bare oxide.

Table 3.3 Extracted vertical drift mobility for gate stack structures with 100 nm 5FPE NTCDI. Note: $A = U_{max}/t_{pulse}$ = (1 V/10 ms) and (0.5 V/10 ms). μ_{FET} is extracted from OFET measurements on similar gate stacks.

Material	$\mu_{U_{offset} = 0\text{ V}, A=100\text{ V/s}}$ **(cm^2/Vs)**	$\mu_{U_{offset} = -0.5\text{ V}, A=100\text{ V/s}}$ **(cm^2/Vs)**	$\mu_{U_{offset} = 0\text{ V}, A=50\text{ V/s}}$ **(cm^2/Vs)**	$\mu_{U_{offset} = -0.5\text{ V}, A=50\text{ V/s}}$ **(cm^2/Vs)**	μ_{FET} **(cm^2/Vs)**
Bare	2.3 x10^{-7}	2.2 x10^{-8}	2.4 x10^{-7}	4.2 x10^{-8}	3.2 x10^{-2}
OTS	3.0 x10^{-7}	2.0 x10^{-8}	3.3 x10^{-7}	3.9 x10^{-8}	1.9 x10^{-2}
FOTS	4.8 x10^{-7}	3.1 x10^{-8}	6.0 x10^{-7}	5.1 x10^{-8}	1.0 x10^{-2}

Comparison of Figs. 3.17 (c,f) and 3.18 (e,f) show the current flowing when U_{offset} is positive, which corresponds to V_G = - U_{offset}. We can calculate the geometrical capacitance with the simple relation $C_i = j(0)/A$, and find values of 22-25 nF/cm^2, in excellent agreement with the CV data presented in Fig. 10. Although a slight reduction in mobility is observed when the ramp rate is doubled, it must be noted that OFET behavior is dominated by μ_{FET} which is ~10^5 larger, and was observed to increase by nearly an order of magnitude with increased V_G pulsing from a static V_G sweep up to 400 Hz. Thus, it seems reasonable to assume that the marginally lower vertical mobility is more than compensated by increased μ_{FET}.

Transistors fabricated in parallel with these capacitors did exhibit values of μ_{FET} that decrease with the expected dipole magnitude of the SAM layer, as shown in Table 3.3. Such observations are not uncommon in OFETs with SAM-treated oxides,[49] where minor differences in processing conditions,[33] exposure to oxygen and moisture in the air,[20] and even variability in the SiO_2 substrate[50] can yield a wide range of device behavior and adversely impact reproducibility. In addition, differences between 8-2-Bn and 5FPE NTCDI in their sensitivity to these effects may also be significant contributors.

Conclusions and Future Prospects

The Si/PlasmOx(+SAM)/NTCDI system comprising the gate stack of Chapter 2 has been extensively characterized using OFET, CV, diode, and CELIV-derived measurements. Each of these techniques offer complementary information on device performance, from changes in channel transconductance, to insight into the microscopic mechanisms that dominate charge trapping as the device is turned on and off. The orthogonality of these measurements enable an assessment of which interfaces prove the most critical, whether through improved charge accumulation in the OSC layer, or through reduced charge transfer across the interface.

Characterization of the MIS diode constituting the gate metal and insulator in our OFETs revealed space charge-limited conduction as the dominant mechanism for gate leakage in our devices, albeit with small contributions due to fixed ion trapping in the form of Frenkel-Poole traps. The application of dipolar SAMs to the oxide interface significantly tuned the charge transport across the oxide, though maintaining the same SCLC behavior at high electric fields. Investigation of this OSC-free structure at low fields ($|V_G| < 0.5$ V) could provide crucial information on transitions in the conduction mechanism across these ultrathin oxide/SAM interfaces. Deeper understanding of these conduction transitions are critical for broadening the use of SAMs as active, functional electronic materials, beyond their use as remedial layers for improving the OSC or electrode work function.

Diodes with an active OSC layer of electron-transporting NTCDI revealed a subtle interplay between the depletion and accumulation of the nSi and NTCDI layers. Analysis of this full gate stack was compared to gate leakage measurements of the OFETs of Chapter 2, demonstrating that the reduction in leakage is consistent with the improved rectification of the oxide/SAM diode. Capacitance data confirmed the directionality of these diodes, and comparison of device dissipation with diode and transistor behavior indicate a clear shift in the potential at which FOTS and OTS devices begin to conduct across the oxide at levels comparable to SAM-free structures.

The clear shifting of CV characteristics in these devices has enabled the estimation of densities of trap states at the oxide(+SAM)/OSC interface which, despite the broad scatter of device performance parameters characteristic of many SAM-based devices, are remarkably self-consistent. Modeling the surface state density with a single Gaussian distribution provided good fits to the estimated trap DOS, a function which has recently become the focus of research into the underlying energetics of SAM dipoles. Although a clear connection between the individual components of N_{ss} will be the focus of future efforts on this project, some general trends do seem obvious to point out.

First, in the case of 5FPE structures with small contact areas (OFET electrodes), a trend in the decrease of surface states relative to bare oxide is observed with increasing frequency of V_G. This reduced density of surface states parallels observations of the increased mobility with increasing frequency of V_G reported by our group and others. Second, the presence of a narrow distribution centered at -0.28 eV for both OTS and FOTS devices, could be attributed to trap sites at the oxide common to both OTS and FOTS. Obtaining clear voltage-shifted CV characteristics for these gate stacks at smaller frequency and voltage intervals will enable a thorough comparison to the frequency dependence of diode conductivity and OFET transconductance.

The use of charge extraction to quantify the vertical carrier mobility in the OFET gate stack further points to the role of trap distributions at the insulator/OSC interface, and further analysis may provide insights into the character of how these traps contribute to gate bias stress, the subject of the next chapter.

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Chapter 4 : Visualizing and Quantifying Charge Distributions Correlated to Threshold Voltage Shifts in Lateral Organic Transistors

Foreword

This chapter appeared as titled in *ACS Nano* on February 18, 2014. It was jointly authored with T. J. Dawidczyk, with equal contributions to the text and analysis as reflected in the publication authorship. The original manuscript for this work constitutes the first half of this chapter, and was authored by T. J. Dawidczyk. Much of the text and all of the surface potential images can be found in his dissertation, "*Interfacial Fields in Organic Field-Effect Transistors and Sensors*, Chapter IV: *Correlating the Surface Potential to Threshold Voltage Shifts*." I authored the second half of this chapter, beginning in the section *"Quantitative relationship between SKPM-derived and V_T-shift-derived charge densities."* I made only minor modifications to the first half. On word count T.J. Dawidczyk and I contributed nearly equally, with the original manuscript containing 2,947 words, and the accepted paper containing 6,540 words (including references, and excluding supporting information presented as Appendix B).

My participation in this work began while writing the *Accounts* review included in the Chapter 1, during which time I was reviewing T. J. Dawidczyk's publication "*Kelvin probe microscopic visualization of charge storage at polystyrene interfaces with pentacene on gold"* for inclusion as a gate-stressing method for controlling V_T in OFETs with polymer insulator layers. The observation that SKPM scans provided both energetic as well as spatial information formed the basis for several discussions with T. J. Dawidczyk and H. E. Katz regarding application of an electrostatic model to describe the surface potential differences at the pentacene-PS interface. My contribution to this manuscript is the numerical analysis of the surface potential data contained in the first half, implementing Poisson's equation to calculate the charge density responsible for the surface potential differences observed in the lateral transistors. I also included comparisons to work by Podzorov to justify our observations of the differences in gate bias stress between the polystyrene layers studied. The article is presented in its entirety as interpretation of the latter half requires presentation of the former.

Visualizing and Quantifying Charge Distributions Correlated to Threshold Voltage Shifts in Lateral Organic Transistors

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Introduction

Organic field-effect transistors (OFETs) are an emerging technology that allows for flexible devices with cheaper processing costs for a variety of applications.[1,2] OFETs are now being considered for active matrix backplanes,[3] radiofrequency identification (RFID) tags,[4] and chemical[5] and biological[6] sensing. To design circuits containing OFETs more effectively, the threshold voltage (V_T) should be precisely tuned.[7] Means of shifting V_T include dipolar monolayers[8,9] or chromophores[10] at the OSC-dielectric interface, electrostatic charging of the dielectric,[11] charging of an interface within the gate material[12], and ferroelectric materials.[13]

An additional V_T shift in OFETs is routinely observed during normal device operation, a phenomenon known as bias stress.[14-21] A major consequence of this phenomenon is poor performance—and ultimately, failure—of circuitry that relies on precisely-tuned voltages for operation. The physical origin of this V_T instability has been widely debated in the literature, with agreement on charge trapping as the prevalent mechanism but disagreement on whether mobile charges were being trapped in the OSC or in the dielectric. Recent work by Lee and coworkers[22] has demonstrated the origin of this bias stress to be the buildup of static charge within the material serving as the dielectric at the OSC-material interface, mainly the result of majority carrier drift in the high electric fields subtended across the OFET gate stack. By purposely embedding static charges within the gate material, the influence of the original interfacial potential at the OSC-material interface can be usefully superseded, allowing for improved V_T stability and enabling controllable selection of the V_T value for a desired application.[23] These reasons motivate the mapping of interfacial potentials in the OFET to identify static charge trapped in the gate material.

In the conventional ("vertical") device geometry, the gate dielectric is very difficult to probe without altering one of the layers. On the other hand, when using a lateral architecture, an edge of the gate dielectric/OSC interface is exposed, allowing for direct measurements across the interface and along one face of the bulk dielectric. Previous work with lateral transistors did not allow for imaging of the gate dielectric/OSC interface.[24] In this work, we visualize the charge stored at the interface between an OSC and a gate material for the first time, using pentacene as semiconductor and polystyrene, poly(3-trifluoromethylstyrene), and poly(methyl methacrylate) (PS, F-PS, and PMMA, respectively) as gate materials. The charge was imaged under ambient conditions using Scanning Kelvin Probe Microscopy (SKPM) as described in our previous work.[25,26] This imaging technique offers insight into the operation of OFETs where charge is stored inside the gate material layer, and has been used to study the role of water in bias stress at an SiO_2 interface[27] and the static charging of an OSC single crystal.[28] More specifically, we show in this study that the quantity of stored charge in the PS calculated from a Poisson's equation treatment of the SKPM data is of the same quantitative order as the charge that should have led to the V_T shifts, based on the lateral capacitance of the region between the gate and OSC. This is the first in-situ observation of stored static charge related to V_T shifts in OFETs, providing direct experimental evidence of charge carrier drift from the OSC into the gate material and furnishing a needed example of the correlation of SKPM measurements with independent parameter determinations.[29]

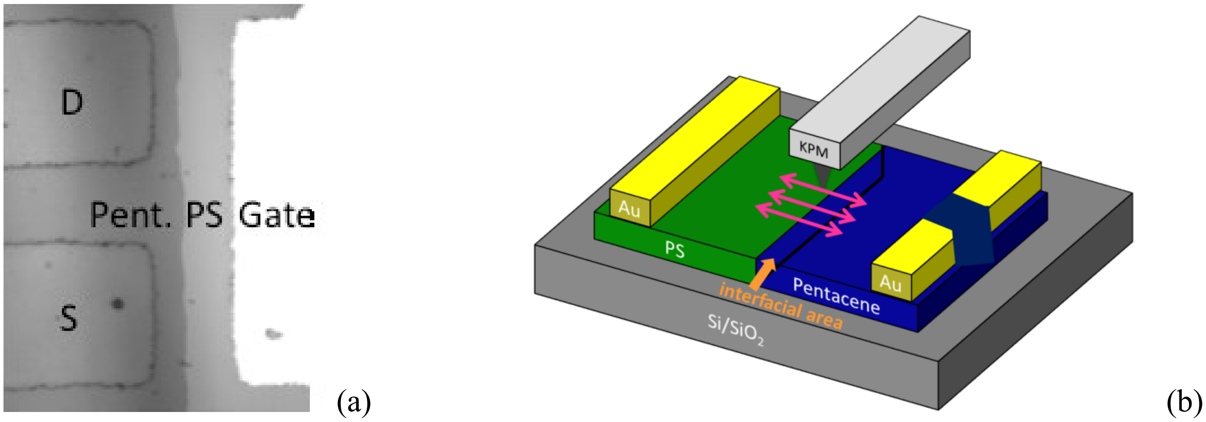


Figure 4.1 (a) An optical microscope picture of the lateral OFET. Note that the distance between source and drain electrodes is 30 µm and the distance between the source/drain and gate electrodes is 30 µm. About half (+/- a quarter) of the source/drain to gate distance is taken by the PS region. **(b)** Schematic of the SKPM scanning direction “x”, parallel to the double arrows.

Results and Discussion

Lateral PS OFET measurements

The lateral OFETs (Fig. 4.1(a)), made using procedure explained in Appendix B Fig. B.1) were imaged with the SKPM (Fig. 4.1(b)) under ambient conditions at three different stages: before the transistor electrical measurements were performed, after the transistor electrical measurements were performed, and after charging the gate material.

The SKPM images shown in Fig. 4.2 are of two separate PS samples at the three stages of measurements, following height scans as shown in Appendix B Fig. B.2. All measurements were performed with no electrical contacts to the transistors, *i.e.* the devices were left floating. The samples were removed from the SKPM between scans, resulting in slight changes in orientation for each scan. The first scan was performed on the pristine lateral OFET before any transistor measurements were made, the second scan was performed after the transistor was electrically tested, and the final SKPM scan was of a ‘charged’ lateral OFET. Additional sample SKPM scans can be seen in the supplementary information (Appendix B Fig. B.3). The initial surface potential difference is small, on the order of a few hundred mV, but after transistor operation the PS displayed a much more positive surface potential than the pentacene side, of roughly 3-5 V. The static charge, a form of “bias stress” in this sample, is concentrated at the semiconductor/gate material interface with less charge apparent closer to the gate electrode. Note that it *is not possible to visualize charge distribution between the gate electrode and OSC in the* *usual vertical architecture, but with our lateral architecture, such evaluations are possible on unaltered OFETs.* The change in surface potential is due to the accumulation and trapping of the positive charge carriers inside the PS gate material layer from the channel of holes being transported from source to drain. This trapping was seen with all the samples tested and can be related to earlier results that show the positive charge carriers altering the surface potential by becoming trapped in a hexamethyldisilazane-modified SiO_2 gate layer[8,14]. This gate biasing effect has been studied in great detail and is one of the major remaining hurdles in commercialization of OSCs.

When the sample is intentionally charged, this surface potential difference between the PS and pentacene can be increased, as in the case of positive charging from the source and drain, or it can be reversed and the surface potential can be made more negative, as in the case of negative charging. In virtually all cases, 10 minutes of charging resulted in a shift in PS surface potential in the charging direction. Note that the inter-electrode distances in these devices are higher (and less easily controlled) than typical for vertical OFETs, so the operational voltages are high as well. However, the fields created by our voltages, if established in vertical OFETs with typical fabrication dimensions, would correspond to applications of the order of 1 V.

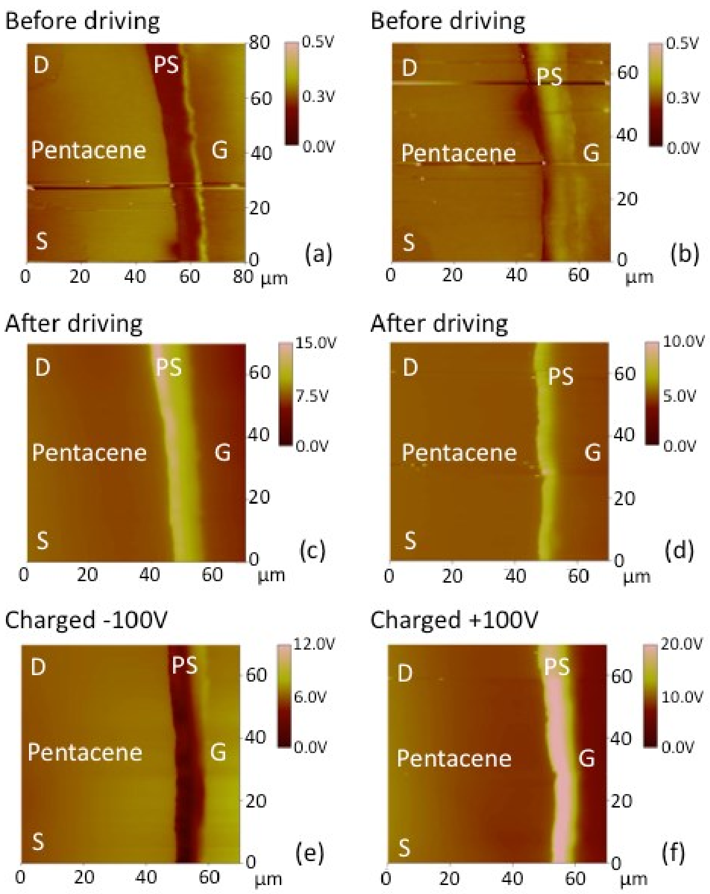


Figure 4.2 SKPM surface potential scans of lateral PS transistors. The source and drain electrodes, though difficult to see, are always at the left of the image and the gate is at the far right. The pentacene is on the left and the PS on the right of the interface. Images **(a,c,e)** and **(b,d,f)** correspond to individual samples. The samples are first imaged before electrical testing (a,b). After the transistor electrical measurements, the samples are scanned (c,d). The samples were then charged to -100 V (e) and +100 V (f) for 10 minutes and rescanned. The correspond height scans can be seen in Appendix B Figure B.2.

Transistor electrical measurements were performed before and after charging, which was conducted under conventional fluorescent laboratory lighting. The threshold voltage V_T was obtained by plotting the square root of the drain current I_d vs. gate voltage V_g (Fig. 4.3) and linearly extrapolating the curve between V_g = -60 V and -100 V to zero current, an arbitrary but objective definition. Negative charging resulted in positive V_T shifts, meaning the device was easier to turn on, while positive charging resulted in negative V_T shifts, making the device harder to turn on. The positive charging can be considered as a prolonged accumulation biasing, with more positive charges injected into the PS from the pentacene. Figure 4.3 shows transfer curves for the two samples from Fig. 4.2 before and after charging. Corresponding output curves are shown in Fig. 4.4. When the devices were positively charged, the on/off ratio increased, while negative charging resulted in lowered on/off ratios. Leakage current varied by device and was approximately 10% of source-drain current. Note that only a fraction of the applied charging voltage drops across the PS-pentacene interface because of the PS series resistance, and this fraction also varied from sample to sample because of the limited precision with which the interface can be positioned between the gate and source-drain electrodes.

The observation that both positive (accumulation) and negative (depletion) charging results in noticeable V_T shifts as seen in Fig. 4.3 suggests that a transfer of both holes and electrons from the pentacene layer into the PS are possible. These data are consistent with measurements reported by Podzorov and Gershenson[21] for single-crystal rubrene OFETs, where a similar shift in the onset voltage was associated with photogenerated carriers drifting into a perylene material during charging in the presence of illumination. The asymmetry of the V_T shift in our pentacene OFETs for equal charging voltages as shown in Fig. 4.3 are also qualitatively similar to those of Podzorov and Gershenson, with depletion voltages resulting in larger ΔV_T than accumulation voltages. Given these data and the presence of ambient lighting during our charging experiments, the observed V_T shifts could have been partly the result of photoassisted implantation of photogenerated carriers, However, additional experiments that we had described in Reference 25, Dawidczyk et al., showed fairly analogous polystyrene interface charging behavior whether the interface was polystyrene-pentacene or polystyrene-gold, suggesting that photoactivation of carriers in the pentacene would not be a requirement for charging.

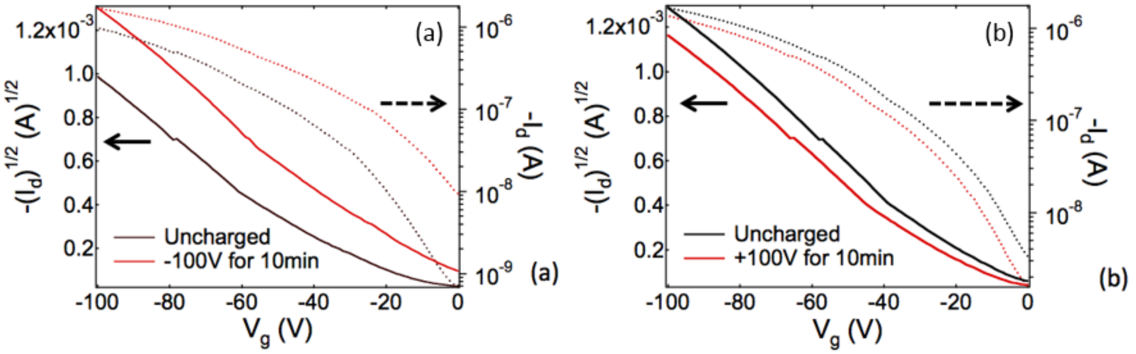


Figure 4.3 Transfer curves for the samples shown in Fig. 4.2. The black curves were obtained before the samples are charged, while the red curves were from samples after charging. The dashed line corresponds to the log scale while the solid line is the square root of the drain current. The samples were charged to -100 V **(a)** and +100 V **(b)**.

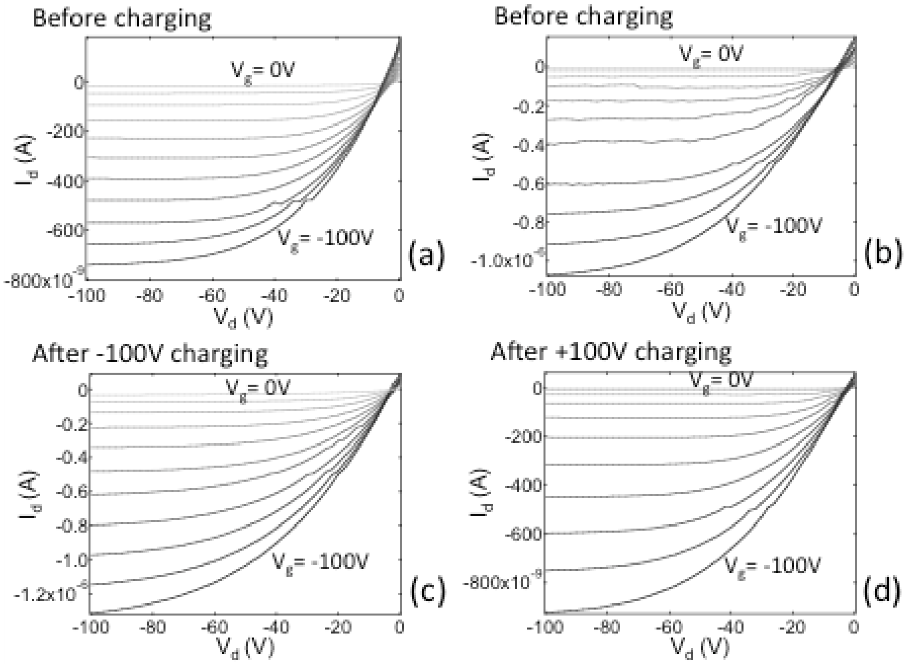


Figure 4.4 Output curves for the transistors in Fig. 4.2, before **(a)** and after **(c)** -100 V charging and before **(b)** and after **(d)** +100 V charging.Note the slightly different y-axes. The gate voltage was stepped from 0V to -100V in -10V increments.

Individual lateral OFETs were charged to varying voltages ranging from ±25V to ±125V. Generally, negative charging gave a greater shift in V_T compared to positive charging, but the directions of V_T shift were nearly always consistent with the charging voltage signs. We have previously shown that the negative charging results in greater shifts in surface potential, thus having greater influence on V_T.[26] Figure B.4 (Appendix B) shows the dependence of V_T on the charging voltage. For charging voltages between -25 and -90V, the V_T shifts and charging voltages are correlated, while because of the previously discussed lower stability of injected positive charges, positive charging voltages are not correlated, except by sign, with V_T shifts. At voltages with magnitudes above 100 V there is the possibility of breakdown and we see that some lateral OFETs show signs of degradation, resulting in smaller V_T shifts. The thickness of the gate material layer (the distance from the gate electrode to the OSC/material interface) varies from device to device, as mentioned above, which will also add uncertainty to the total charge stored in the gate material layer.

Quantitative relationship between SKPM-derived and V_T-shift-derived charge densities

The surface potential scans acquired with SKPM afford the opportunity to quantify the charge trapped in the PS layer after electrostatic charging. As each linescan along the scan direction *x* (Fig. 4.1) measures the surface potential *V(x)*, changes in the surface potential along the scan direction can be understood within the framework of Poisson's equation,

$$\frac{\partial^2}{\partial x^2} V_s(x) = -\frac{\rho_s}{\varepsilon\varepsilon_0} \qquad [4.1]$$

where $V_s(x)$ is the surface potential, ρ_s is the charge density at the surface of the material, ε is the dielectric constant, and ε_0 is the permittivity of free space. By taking the Laplacian of the surface potential, the surface charge of the PS layer can be estimated numerically, as discussed in the Methods section.

As discussed in further detail in Appendix B, the pentacene near the PS interface exhibits a sharp topographical feature, the result of the fabrication process. In order to estimate the location of the actual PS interface (and not this ridge), surface profile plots were created using a contouring algorithm.[30] The main topographical features of the plots were created by extracting the features with the largest area density in each image (see Methods at the end of this chapter). The PS-pentacene interface was determined to be at the edge of multiple closely-spaced contour lines of constant height taken near the expected PS-pentacene interface location. Contour lines become closely spaced at the edge of sharply rising features. The location of this extra PS edge is roughly 1-2 um left of the highlighted interface, as shown in Fig. 4.5.

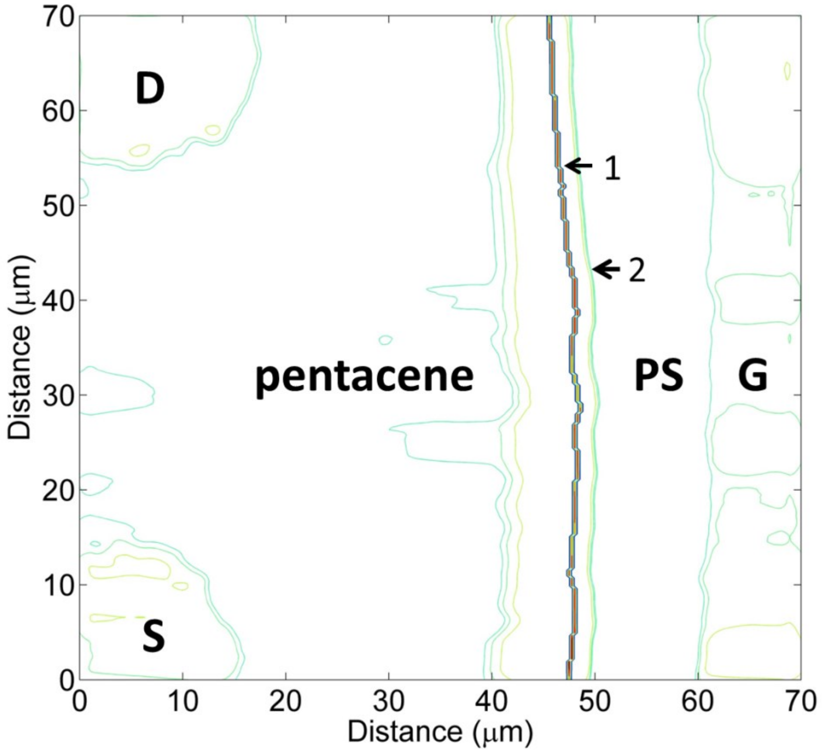


Figure 4.5 Illustration of height profile contour of the OFET illustrated in Fig. 4.2. The line indicated by 1 corresponds to the sharp ridge at the PS-pentacene interface indicated by the height scan. The line indicated by 2 corresponds to the edge of the PS-pentacene interface as approximated by the contouring algorithm.

Surface charge density (ρ_s) plots were also created using the same contouring algorithm and the results of the Poisson's equation analysis. To illustrate changes in charge density as a function of driving and charging time, surface charge density plots were overlaid onto height profile plots captured during the same scan as the surface potential images. Figure 4.6 shows the surface charge density ρ_s overlaid onto the height profile for the OFETs illustrated in Fig. 4.2. To distinguish surface profile features from charge density features, all surface profile features are traced in black, while all ρ_s features are traced in color. The three frames in Fig. 6 correspond to the calculated ρ_s in the lateral OFET before driving, after driving, and after charging at -100 V for 10 min, respectively. The physical orientation is the same as for all other images in this paper. The colored contours correspond to areas of constant and high charge density, as scaled by the colorbar on the right of each image. The black and gray contours correspond to the physical features of the surface, similar to the profile illustrated in Fig. 4.5.

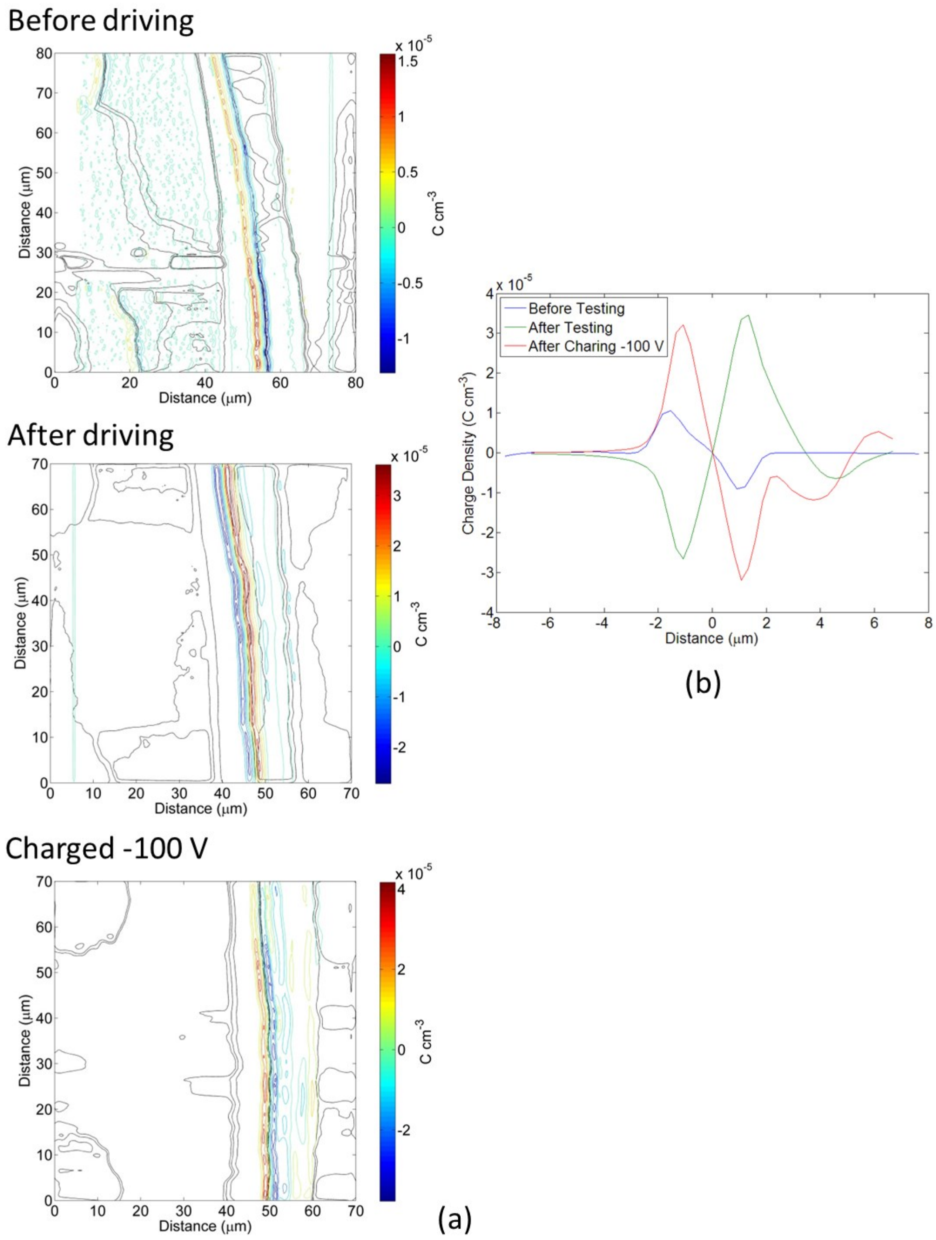


Figure 4.6 (a) Charge Density Maps of OFET from Fig. 4.2.Before driving, the device shows a small amount of charge at the PS-pentacene interface, consistent with its surface potential plot. Before driving, the PS near the pentacene interface is more negative than the adjacent pentacene layer. After driving, the PS at the interface becomes more positive than the pentacene, the result of driving holes into the PS layer. Upon charging to -100 V for 10 min, the PS layer is more negative than the adjacent pentacene layer, and has significant charge extending into the PS. **(b)** Corresponding cross-section of charge density illustrated in (a).

Comparison to V_t data

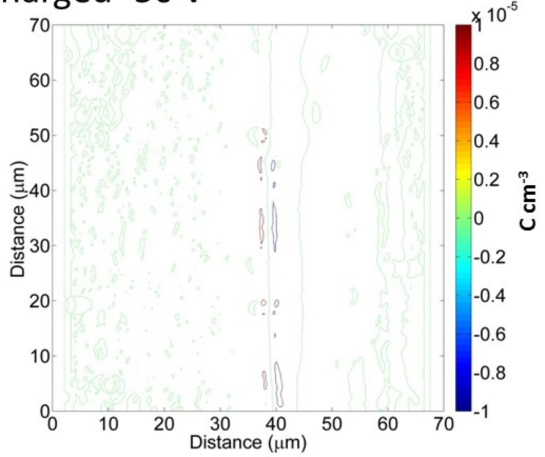
We can calculate the change in charge density at the PS-pentacene interface that results from OFET charging from the data in Fig. 4.6. Before driving, the charge density derived from the Poisson's equation analysis at the PS-pentacene interface is roughly 10 μC cm^{-3} positioned about 2-3 μm perpendicular to the interface (in the *x* direction) on the pentacene side. We can integrate the volumetric charge density illustrated in Fig. 4.6(b) along the x-direction over a range of 2.73 μm into the pentacene layer, changing the units from coulombs to electron charges, yielding an interfacial positive charge density $\sigma = 9.7\text{x}10^{9}$ cm^{-2}, where the area units refer to the cross-sectional interfacial area shown in Fig. 4.1. Much of this charge is compensated by apparent negative charges dispersed elsewhere in the pentacene. By comparison, after charging at -100 V for 10 min the peak charge density increases to 30-40 μC cm^{-3} over the same spatial extent, and integration of Fig. 4.6(b) yields a value of $\sigma = 2.5\text{x}10^{10}$ cm^{-2}, with little apparent compensating charge in the pentacene.

To assess whether this change in interfacial charge density is consistent with the observed V_t shifts, we employ a common estimate for the areal charge density at the semiconductor-polymer interface in an OFET as a function of threshold voltage shift, given by the simple relation

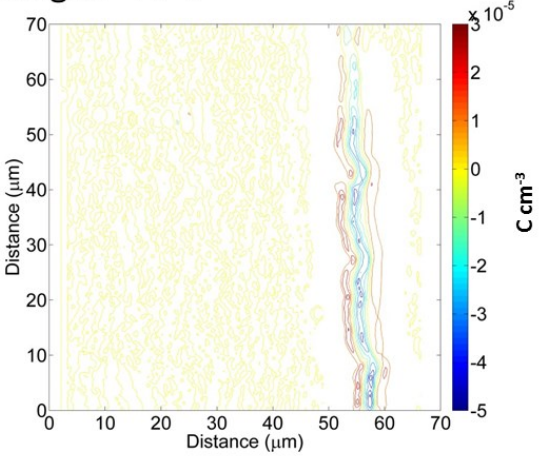
$$\sigma_{cap} = \frac{C_i}{e}\Delta V_t \qquad [4.2]$$

where *e* is the fundamental charge, ΔV_t is the threshold voltage change $|V_t - V_{t,0}|$, σ_{cap} is the resulting interfacial charge density, and $C_i = \varepsilon\varepsilon_0 / t_i$ is the specific capacitance of the polymerlayer—again keeping in mind that the "area" of the capacitor is the interfacial area and the "thickness" t_i of the gate material layer is in the *x* direction parallel to the substrate (refer again to Fig. 4.1). For the transistor that had been charged to -100V, the "gate material thickness" is approximately 7.6 +/- 0.9 μm, corresponding to a specific capacitance of ~0.30 nF cm^{-2}, and the value of ΔV_t is -18 V. Substituting these values into Eq. 4.2 and again working in units of electron charge yields $\sigma_{cap} = 3.4\text{x}10^{10}$ cm^{-2} for the charged device, in good agreement with the Poisson's equation analysis discussed above, each value within 15-20% of 3.0 $\text{x}10^{10}$ cm^{-2}.

Charged -50 V



Charged -75 V



Charged -100 V

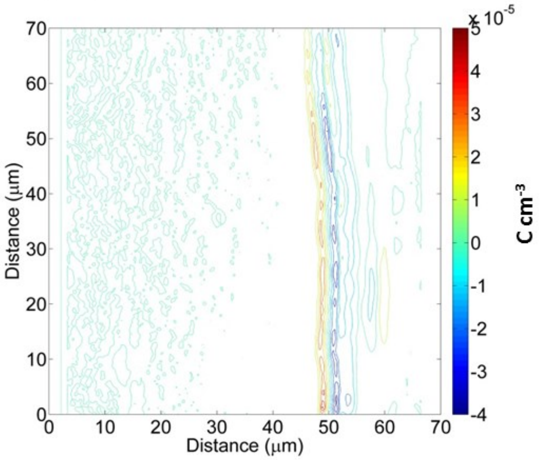


Figure 4.7 Comparison of charge density distribution for OFETs charged to -50 V, -75 V, and -100 V, respectively. All images have been contoured using 13 levels, spaced in 10 μC cm^{-3} increments from -60 to 60 μC cm^{-3}.

We examined two of our other samples at this level of detail, one charged at -50 V and one at -75 V. Because the plots from all three charging values use identical contours spaced between -60 and 60 μC cm^{-3}, the differences in absolute charge density near the PS-pentacene interface are readily observed, revealing a clear increase in ρ_s with increasing charging voltage. A comparison between the charge density calculated from the two methods discussed above is shown in Table 4.1. For the -50 V charged OFET, the values calculated from both methods—σ_{SKPM} and σ_{cap}—differ by less than 15% from the average of the two. Considering the numerous uncertainties in defining the positions of charges and interfaces, and the possibility of static charge arising from impurities, this agreement is remarkable. The third sample was an OFET charged to -75 V that also happened to have a much lower "gate material thickness". In this case, the much thinner gate material results in a higher estimate of the charge from Eq. 4.2 as compared to the integrated charge density ρ_s. Some of the negative charge in the PS layer at the PS-pentacene interface is likely compensated or screened by positive charge injected from the [opposite] PS-Au interface, resulting in a lower charge density on the pentacene side than the capacitor approximation would predict. The thinner material might have also been more generally unstable to this level of charging voltage.

Table 4.1 Geometric and electrostatic parameters for charged OFETs. t_i is the material thickness, C_i is the material specific capacitance, ΔV_t is the threshold voltage shift, σ_{SKPM} is the charge density estimated from the Poisson analysis of the pentacene-side charging and σ_{cap} is the charge density estimated from the capacitor approximation. The charge density derived from SKPM data is the charge density integrated on the pentacene side within 2.73 μm from the PS-pentacene interface, as shown in Fig. 4.8.

Charging Voltage	t_i (μm)	C_i (nF cm^{-2})	ΔV_t (V)	σ_{SKPM} (cm^{-2})	σ_{cap} (cm^{-2})
-50 V	14.2 ± 0.9	0.16	5.3 V	6.8 x10^{9}	5.3 x10^{9}
-75 V	2.3 ± 0.4	1.00	15.9 V	1.5 x10^{10}	9.9 x10^{10}
-100 V	7.6 ± 0.8	0.30	18.0 V	2.5 x10^{10}	3.4 x10^{10}

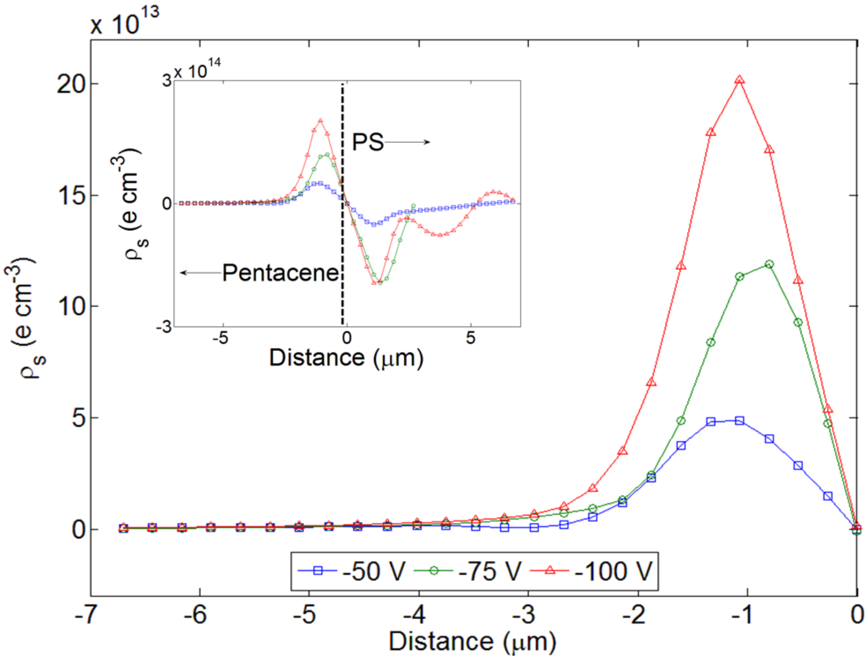


Figure 4.8 Charge density on the pentacene side, and (inset) across the PS-pentacene interface in each charged OFET (median of 256 linescans per OFET).The increase in accumulated positive charge density in the pentacene layer with increasing charging voltage is consistent with the observed V_t shift for these OFETs.

As illustrated in Table 4.1 and discussed above regarding Fig. B.4 (Appendix B), OFETs subjected to increasingly greater charging voltages generally displayed greater ΔV_t, the result of the V_t shifts being associated with greater charge accumulated in the semiconductor channel. This charge density is of the same order of magnitude (10^{10} cm^{-2}, from integrating the curves on the pentacene side) as the negative charge density in the PS, with the 50 V charging giving 5 x 10^9 cm^{-2}, in excellent agreement with σ_{cap}. In addition, the -100 V device showed greater total negative charge on the PS side (including the region farther from the interface) than the -75 V sample, as would be expected.

To investigate the dependence of stability and chargeability on the gate material structure, we used F-PS and PMMA instead of PS. Previous studies have shown that fluorinated dielectrics help prevent bias stress. [31] Figure 4.9 shows SKPM scans for the F-PS system; note that unlike the PS sample, the charge stored inside the F-PS after transistor operation did not penetrate nearly as deeply, and is of a much lower magnitude. material This observation is consistent with the model developed by Lee and coworkers,[22] in which the gate material charging is the result of charge transfer from the OSC highest-occupied molecular orbitals (HOMO) into localized tail states in the gate material. The lower HOMO of fluorinated polymers such as F-PS as compared to PS would result in tail states with a greater energy offset from the pentacene HOMO, leading to reduced gate material charging.

PMMA lateral OFET images are shown in Fig. B.6, Appendix B. The surface potential of the PMMA region closest to the pentacene was more positive after device operation and could be made more positive with positive charging and more negative with negative charging, just as with the polystyrenes. However, the PMMA devices exhibited much greater leakage currents (in some cases close to 1/3 the I_d, where leakage current is defined as the current from the gate to the source electrode) than either the PS or F-PS. PMMA showed less capacity to store static charge and also gave less consistent device currents and changes in response to charging of particular signs relative to PS, as could be expected from the greater polarity of PMMA. Other work has shown that the increased polarity of PMMA over PS increases the energetic disorder at the interface.[32] It has also been shown that hydrophobic and non-polar materials like PS help increase the non-volatile memory performance of OFETs.[33]

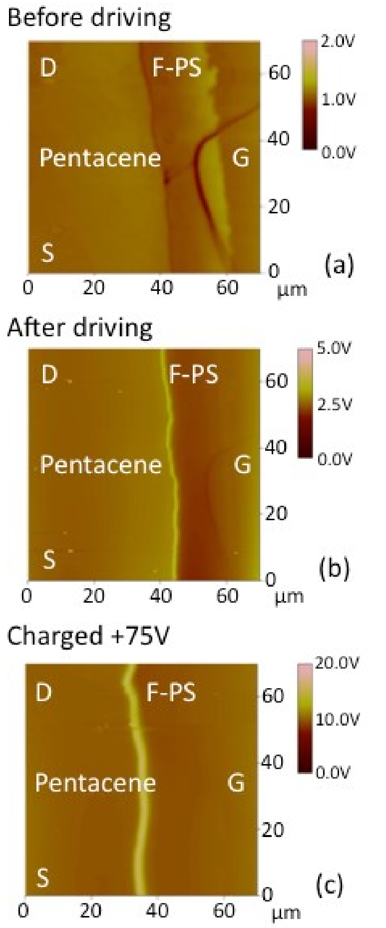


Figure 4.9 SKPM surface potential scans of the F-PS lateral transistors. The interface has the pentacene on the left and the F-PS on the right. The electrodes are oriented in the same manner as Fig. 4.2. **(a)** The samples are first imaged before electrical testing. **(b)** After the transistor electrical measurements the samples are scanned. **(c)** The sample was then charged to a value of +75V for 10 minutes and rescanned. The corresponding height scan can be seen in the Appendix B, Fig. B.5.

To compare the bias stress behavior of the PS and F-PS transistors we prepared conventional ‘vertical’ devices with and without pre-charged gate materials (see Appendix B, Fig. B.7 for procedure and additional data). The uncharged F-PS showed a greatly improved resistance to bias stress compared to PS (Fig. 4.10), while charging greatly improved PS bias stress resistance to a level at least as good as F-PS at short times, pointing to a means of improving bias stress stability in a polymer that might have other desirable attributes such as processability or surface functionality. Charging had little effect on F-PS bias stress at short times and may have been detrimental at long times, possibly suggesting a change in the energy offset between the pentacene HOMO and the F-PS tail states as a result of partially filling the F-PS tail band.

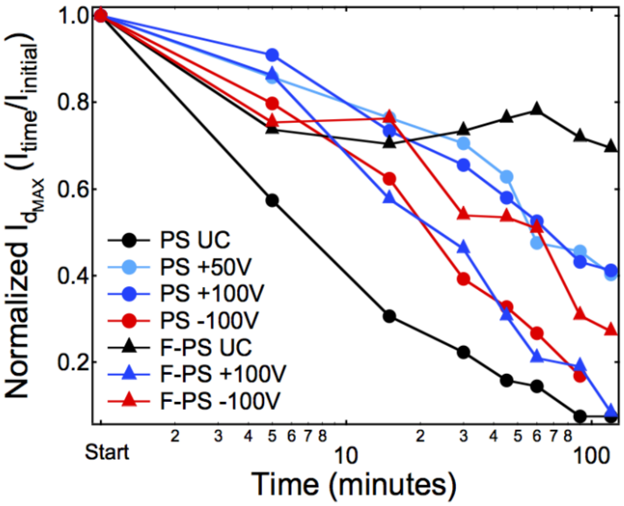


Figure 4.10 Bias stress behavior of PS (circles) and F-PS (triangles) OFETs.The level of positive charge in the PS samples did not seem to change the gate bias behavior of the OFETs. Positive charging helped the PS sample more than the F-PS. The F-PS performed best with no charging.

In addition to the PS, F-PS and PMMA gate materials, we also investigated lateral “control” OFETs with an air gap gate (omitting the PS/F-PS). Output curves from some no-PS devices before and after charging are shown in Fig. 4.11. Although the air gap did lower the leakage current to sub-nA levels, these control devices showed poorer on/off ratios, field effect over a more limited range, no saturation behavior, and different V_T shifts from charging. These data offer clear—all evidence that the PS or F-PS, when present, is the principal gate material in these kinds of devices. After negative charging, the “air gap” OFETs would show lower source-drain current and a negative shift in V_T. Positive charging resulted in higher source-drain currents. This may be due to the charges remaining inside the pentacene and not being injected into the gate material layer, as shown in work by Podzorov *et al*.[34]

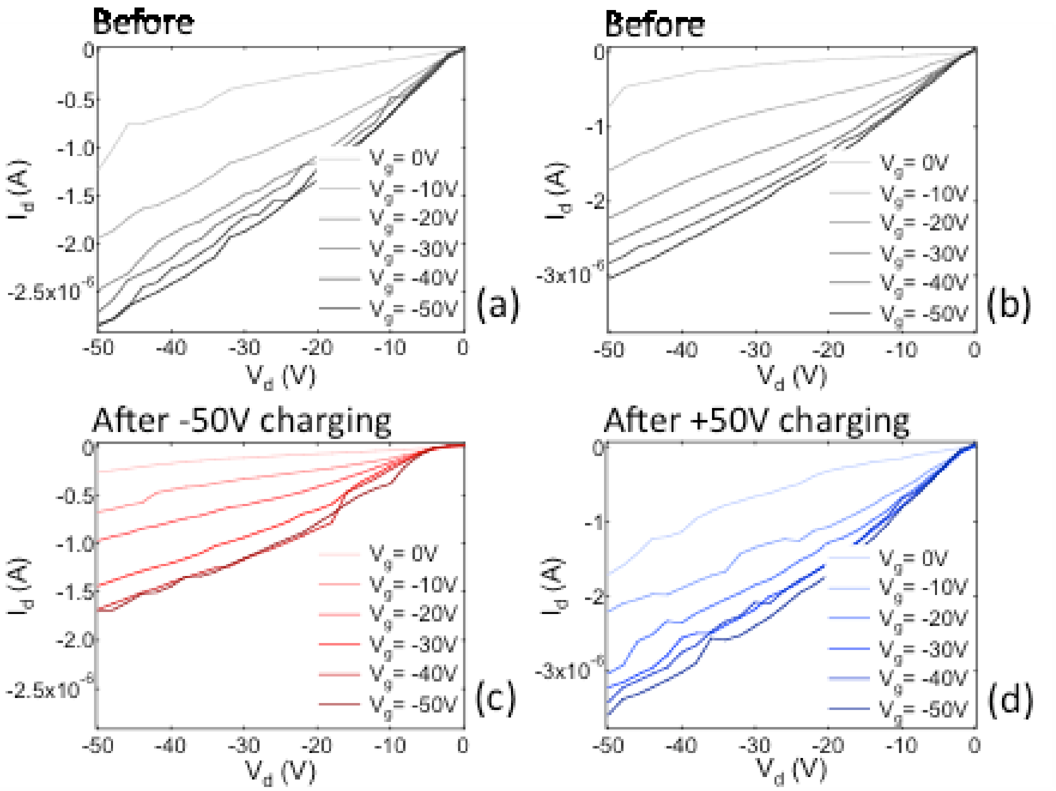


Figure 4.11 Output curves for lateral OFETs without a polymer gate material layer.A sample was tested before **(a)** and after **(c)** charging at -50V for 10 minutes, and before **(b)** and after **(d)** charging at +50V for 10 minutes. Now that the lateral OFETs have no gate material layer the charging voltage reverses the change in output current, with the negative charging giving lower current and the positive charging giving higher current.

Conclusions

We showed that lateral OFETs can be used to visualize charge accumulation inside a gate material in a way not possible with conventional vertical devices, and that this charge accumulation is quantitatively correlated to OFET V_T shifts and influences bias stress stability. The PS can be positively or negatively charged, resulting in a V_T shift. Negative charging voltages resulted in greater V_T shifts with PS than did corresponding positive charging. PS, F-PS and PMMA show strikingly different charge penetration properties, with the polar PMMA also showing increased leakage current and the nonpolar F-PS showing superior intrinsic bias stress stability. Charging improved the bias stress stability of PS. In addition to visualizing gate material polarization and charge injection from semiconductors into gate materials, this technique can be used with other combinations of materials to reveal potential differences across regions of various lateral devices during operation.

Methods

Experimental

The bottom contact lateral OFETs were fabricated with a method very similar to one we described for our previous work, with the fabrication of the lateral transistors requiring the use of a fluorinated polymer barrier layer.[26] A schematic of the fabrication process is in Appendix B, Fig. B.1. The devices were made on highly doped Si with 300 nm of thermally grown SiO_2. 50 nm of Au with a 5 nm Cr adhesion layer was deposited on substrates patterned by photolithography. Atactic PS (50,000 g/mol molecular weight), F-PS, (synthesized in house and having 80,000 g/mol molecular weight) or PMMA (120,000 g/mol molecular weight) was deposited by spin coating at 2000 RPM for 1 minute followed by annealing on a 95°C hotplate for 10 minutes. Cytop (Asahi Glass Co.) was then deposited on top of the gate material layer by spin coating at 2000 RPM for 1 minute and annealing at 95°C for 10 minutes. A mask protected the portion of the polymer nearest the gate electrode, while the unprotected region was etched away with oxygen plasma (4 minutes at medium power). 50 nm of pentacene was thermally deposited and the residual Cytop layer was removed using perfluorodecalin. After that, the underlying gate polymer between the gate electrode and the pentacene, including the interface between the polymer and pentacene, was exposed. An optical image is shown in Fig. 4.1, along with a device schematic showing the orientation relative to SKPM scans. The OFET gate material layer was "charged" by grounding the gate electrode and applying an equal voltage to both the source and drain electrodes for 10 minutes. The scanning direction for each image is perpendicular to the PS-pentacene interface, from the gate to the source-drain side of the device, as shown in Fig. 4.1(b).

Numerical Estimation of Charge Density

The potential gradient was evaluated using a 1-D central-difference method, and applied line-by-line in the same direction in which the data was collected (indicated by the double arrows in Fig. 4.1). This approach is consistent with the line-by-line data collection of the instrument; each 2D image consists of 256 lines covering a 70 µm x 70 µm area, resulting in lateral lines spaced 273 nm apart and 273 nm between points probed along each line. As seen in Fig. 4.2, small sparse surface contamination can contribute to abrupt changes in surface potential within one or two linescans in the image, and not representative of the entire sample. As a result, the alternative application of a 2-D gradient method, not used here, amplifies the spatial extent of these artifacts, inconsistent with the original surface potential measurement.

Small differences in the surface potential V_s are also observed near the start and end of each scan line. These differences in V_s arise from rapid changes in the tip speed near the scan edge when the tip changes scan direction. As a result, these surface potential differences manifest themselves as a band or charge density roughly 2 µm for the edge of the image on all sides. To eliminate these bands, 10 points at the start and end of each line were flattened. To identify the main topographic features in a height contour plot, each height image was contoured into 256 levels, and the area corresponding to each contour level converted into a histogram of unique height values. The three most prominent height values were selected and plotted as a height contour. These height values roughly correspond to the Au electrodes, pentacene, and PS layers. This approach is consistent with the observation that the electrodes were evaporated simultaneously and are approximately the same height, and the PS and pentacene layers are of different height.

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Chapter 5 : Conclusions and Future Prospects

Our growing understanding of interfacial phenomena in organic and hybrid electronics continues to transform our perception of them, transforming charge traps and so-called "defects" into controllable methods for device design and control. The efforts of this dissertation have focused squarely on understanding the role of interface states—in the form of charge traps and electric dipoles—at the insulator/organic semiconductor (OSC) interface.

Self-Assembled Monolayers

Using an array of devices including diodes, capacitors, and transistors, the net effect of a self-assembled monolayer (SAM) dipole on the lateral and vertical charge transport properties of NTCDI has been investigated, adding to the device engineer's toolbox additional design alternatives for hybrid electronic devices. The use of SAMs to reduce leakage currents in marginal quality OFET dielectrics expands on initial work by Halik[1] and Klauk[2] aimed at fully molecular transistor architectures. The results detailed in Chapters 2 and 3 offer a new perspective on leakage reduction with SAMs, with the intent of harnessing not just the lengths and high packing density of these molecules, but also their *dipole*s to reduce leakage currents. Notably, subthreshold leakage was found to be reduced by two orders of magnitude more than gate leakage, clearly suggesting a shift in the energy level alignment at the oxide interface. The use of both p- and n-Si substrates with differing Fermi levels further supported this vacuum-level shift at the oxide/OSC interface, affording quantitative comparison to research by Cahen and coworkers on the energy level alignment of alkyl monolayers on oxide-free Si.[3] In addition, MIS diodes free of any OSC displayed an increase in the onset of space-charge limited current with increasing SAM dipole, demonstrating that the interface dipole at the oxide/SAM interface is effective in tuning transport in the Si across the oxide, also in agreement with work by Cahen.

With these insights in hand, CELIV, a key experimental techniques commonly used to characterize photovoltaics, was successfully applied to MIS structures on both Si/SiO_2 and Al/AlO_x substrates to measure the equilibrium, vacuum-level shifts arising from SAM dipoles at the oxide/OSC interface. These results were in close quantitative agreement with values obtained from steady-state measurements of OFET threshold voltage shifts, displaying a roughly 2:1 ratio in the equilibrium offset voltages of the structures. This same ratio was observed in V_T shifts and the onset of space-charge limited current, despite the ratio of the dipole of FOTS relative to OTS measured to be a factor of 3 – 20. Several key directions that could greatly expand on our findings and the utility of SAMs to the broader scientific and engineering community are outlined below.

The use of SAMs at the SiO_2/NTCDI surface has provided a much needed investigation of the effect of dipolar SAMs on n-channel OSCs. An overwhelming amount of work on SAM/OSC interactions has been conducted on p-channel OSCs, largely stemming from the greater commercial availability and characterization of these materials. However, if the full promise of organic electronics is to be realized using complementary circuitry, control of n-channel OFETs using SAMs must be explored and investigated to the same depth. A first step in bridging this gap is the fabrication of diodes and OFETs on SAM-treated oxides using single-crystal n-channel semiconductors. As seen in the AFM images of Chapter 2, SAMs introduce small but non-negligible changes in the morphology of vapor-deposited OSCs within the critical first few layers of the semiconductor. While measurements of OFETs on SAM-treated oxides show an enhancement of the field-effect mobility, from these values it is difficult to decouple contributions from the dipole and from surface energy-induced morphological differences. The coupling of carrier transport to OSC morphology makes the attribution of changes in device performance arising from SAM treatment merely an exercise in engineering and optimization, and can be highly device-specific.

Work by Podzorov on the injection of charges in rubrene[4] by dipolar SAMs greatly benefited from the absence and/or reduction of internal defects in the OSC layers. Although single crystal fabrication is nowhere near commercial scale at the time of writing, measurements on single crystal devices offer an excellent framework for differential device analysis. Recent advances on identifying the location of charges responsible for gate bias stress have relied on OSC single crystals to definitively rule out internal OSC defects as contributors to gate bias stress. Additionally, the de Leeuw group has employed the peelable p-channel polymer polytriarylamine (PTAA) to isolate internal OSC defects from interfacial charges responsible for gate bias stress. Testing of similar SAM-treated device architectures with n-channel single crystals or easily-peeled polymers will enable proper comparisons to the p-channel OSC literature, where the internal defects of the OSC are decidedly either zero or constant.

Beyond gate bias stress, recent theoretical work by Heremans has suggested that the surface and trap states induced by SAM dipoles can be attributed jointly to the electrostatic interaction with the semiconductor as well as the energetic disorder introduced to the OSC carrier density of states.[5] Decoupling energetic disorder and electrostatic interaction is complicated in OSCs by the presence of grain boundaries and other structural defects, which can result in the creation of deep Frenkel-Poole-type traps within the OSC film.[6] Consequently, device measurements that exploit OSCs with a fixed trap density will be best suited to extrapolating the electrostatic and disorder contributions of SAM dipoles to OSC carrier mobility and OFET performance.

Nevertheless, an equally fascinating area of interest to the engineering community would be afforded by doing the exact opposite—fabricating highly disordered OSC films. While this dissertation has focused on using SAMs as a remedial layer targeting mediocre insulators, it may serve just as well as a remedial layer for intentionally mediocre OSC layers. The improved morphology of OSC films deposited on alkyl SAMs such as OTS have been documented so widely that HMDS or OTS treatment has all but become standard in substrate preparation protocols. However, because these studies have focused on achieving high mobilities for OFET, sensing, or OPV properties, much care has been taken to deposit these active layers at very slow controlled rates that yield high quality, lamellar OSC films.

By the same token, physical vapor-deposited OSC films may provide a suitable method for the fabrication of device structures with highly disordered OSCs in which charge transport is severely hampered by a high concentration of internal defects. Probing the effect of a SAM dipole on improving the charge transport in these defective OSCs would provide equally useful insights on the effect of SAM-induced energetic disorder in bypassing internal electronic defects in the OSC. Figure 5.1 shows a comparison of two sets of devices in which a layer equivalent to 100 nm of 5FPE was deposited at a rate of 0.2 Å/s and 1.0 Å/s, respectively.

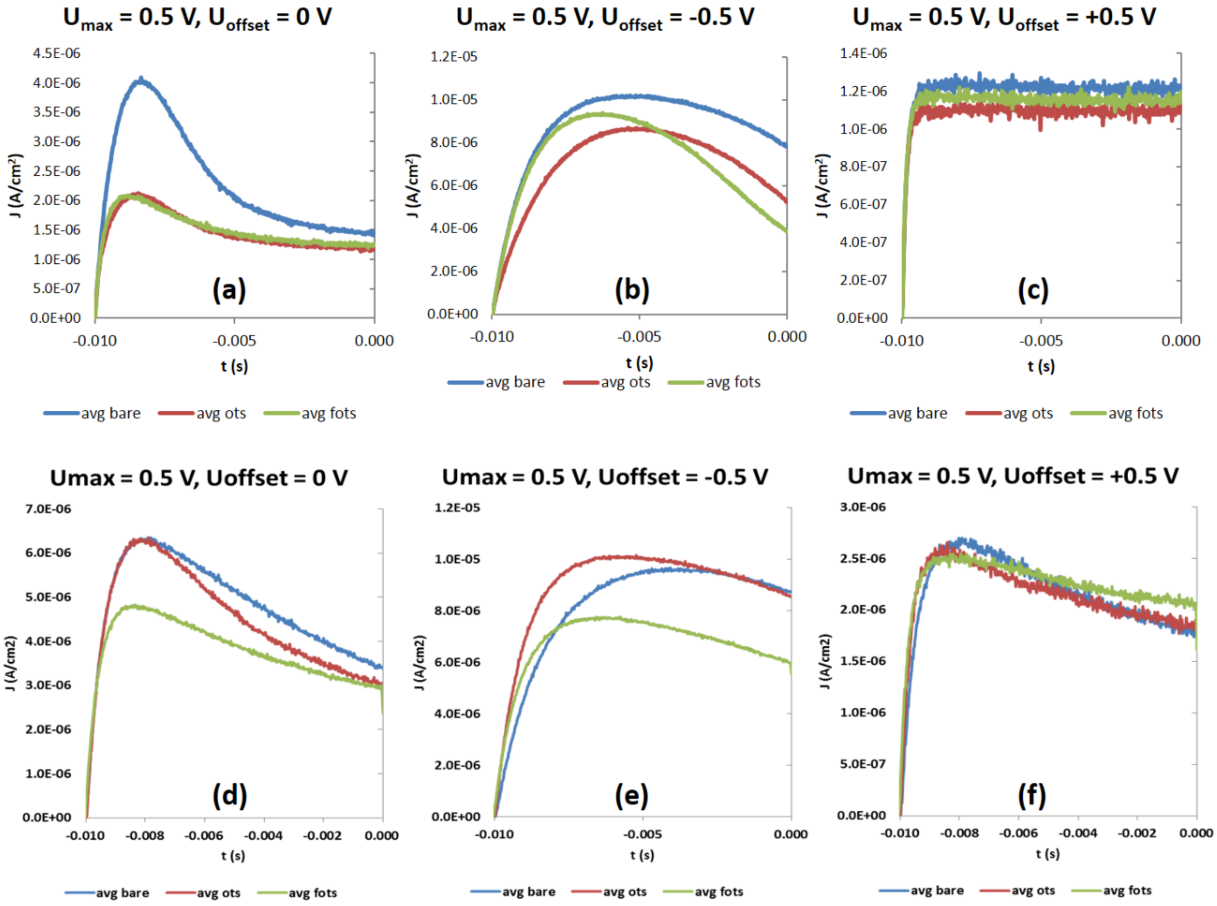

Figure 5.1 Comparison of charge extraction measurements of 100nm 5FPE-NTCDI diodes in which the 5FPE was deposited at 0.2 Å/s **(a-c)** and at 1 Å/s **(d-f)**.

As seen in Fig. 5.1(d-f), the current responses indicate a longer decay time than for slowly deposited, “good” films. This slow response time is likely the consequence of a very high trap density. The greater current at similar offset voltages (Fig. 5.1 a/d, b/e. and c/f pairs) suggests that this bulk trap density dominates charge transport, possibly exceeding the trap density of the oxide/OSC interface. It should be noted that this current response is qualitative similar to that observed for SAM-treated diodes on Al/AlOx (Appendix A), which were deposited at 1 Å/s in an effort to eliminate morphology differences as a variable in the analysis. In particular, the greater extracted current for OTS at $U_{offset} < 0$ than for bare and FOTS devices was a key feature in that investigation, coupled with a lower FOTS current at nearly every value of U_{offset}. We note that at $U_{offset} > 0$, all of the devices appear to decay towards their geometrical capacitance within the same current range, suggesting that differences in the oxide thickness can be excluded. As an important next step in this work, further investigation of the OSC morphology dependence on the observed SAM dipole effect will provide critical bounds on their utility as remedial layers for fabrication processes that may exploit higher operating vacuum pressure or faster OSC deposition rates to reduce processing costs.

Polymer Insulators

Part of the long-term technological goal of the organic semiconductor community is the fabrication of all-organic electronic devices, from substrate to electrode. Advances in both the fabrication of ultrasmooth paper and the development of high-T_g polyimides have moved the possibility of roll-to-roll printable electronics a step closer to reality. Conductive inks that rival or exceed the conductivity of the PEDOT:PSS system have recently come to market. Successes in the inkjet printing of small molecule and polymer OSCs have left one notable void in the search for all-organic transistors: the polymer insulator.

The use of scanning Kelvin-probe microscopy (SKPM) to infer the charge density in electrostatically poled thin film insulators will be an indispensable tool for characterizing the next generation of polarizable polymer gate materials. In Chapter 4, a simple Poisson's equation model was applied to identify the accumulated charge at the pentacene/PS interface in lateral OFETs. Despite the high aspect ratio and very thin (~50 nm) PS layer, the calculated values were found to be in excellent agreement with parallel plate estimates for the gate bias-induced charge. Nevertheless, wire-plate models, as well as other geometry-specific charge density models could be used to accurately quantify charges in a host of device configurations.

One area that could benefit from our approach quantifying charge in a lateral device geometry is in OSC-based environmental sensors, of which the Katz group has recently developed devices sensitive to liquid and gas-phase analytes. Surface potential measurement of lateral OFETs and diodes subjected to a low-concentration target vapor analyte could be compared to transfer curve V_T shifts, enabling quantification of analyte sensitivity based on adsorbed—not *delivered*—analyte concentrations. Such applications would expand scanning probe measurements akin to those designed by Ginger and coworkers in the in-situ study of photoabsorption in organic bulk heterojunctions.[7]

In closing, the study of interfacial phenomena holds great promise for the development of organic and hybrid electronics. The insights to be gained from controlled, targeted studies of materials and devices in this context will help elucidate the various interactions that dominate device behavior across a range of scales from the atomic to the molecular, and from the thin film to the macroscopic circuit.

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Appendix A: Measuring SAM Dipoles using Charge Extraction

This article appeared in *Applied Physics Letters* on December 10, 2013. The main text was authored by M. Nyman. I fabricated all of the MIS structures, and conducted device testing together with M. Nyman and O. Sandberg at Åbo Akademi University during a three-month research visit at the university's Center for Functional Materials. This chapter is included as an appendix because in it the co-authors and I established the first use of CELIV as a technique for probing an MIS structure and determining the effective vacuum-level shift of a SAM dipole. This technique forms part of the basis of our approach to understanding the SAM layer on the Si/SiO$_2$ system discussed in Chapter 3. The figure labels have been edited to reflect dissertation formatting. In addition, supplementary information consisting of J-V curves of the Al/AlO$_x$(+SAM)/NTCDI structures is presented to complement the diode analysis of Si/PlasmOx/NTCDI/Au structures in Chapter 3.

Voltage dependent displacement current as a tool to measure the vacuum level shift caused by self-assembled monolayers on aluminum oxide

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Organic small molecules and polymers offer the possibility of flexible, cheap and light weight electronic devices operating at low voltages. To achieve low voltage operation, it is essential to have the turn-on voltage as close to zero as possible. In addition, the gate dielectric should be as thin as possible but still blocking enough to avoid gate leakage. Aluminum oxide (AlO_x) has been considered an affordable option as a high-κ gate dielectric for transistors that is compatible with flexible substrates. However, aluminum oxide has been shown to be unreliable due to gate leakage and significant charge trapping.[1,2] T. W. Hickmott has showed that the trap density in anodic AlO_x can be as high as 10^{19} cm^{-3}. The large intrinsic trapped carrier density leads to significant polarization. The amount of trapped charge and the polarization current is seen to depend on the anodizing electrolyte.[1] Weber et al have performed theoretical calculations on native defects in Al_2O_3 and their impact on III-V/Al_2O_3 devices showing that the most important native defects are oxygen vacancies. The trap levels due to oxygen vacancies were calculated to be between roughly 4 and 5 eV.[2] These gap states cause trap-assisted conduction leading to gate leakage.

Surface modification using various self-assembled monolayers (SAMs) has gathered much attention due to the possibility of tuning the interfacial properties. Calhoun et al showed that forming a layer of (tridecafluoro-1,1,2,2-tetrahydrooctyl)trichlorosilane on rubrene can result in an increase of the surface conductivity by up to four orders of magnitude.[3] Martínez Hardigree et al showed that gate leakage through 10 nm of SiO_2 can be significantly reduced by growing a SAM on the oxide. A shift of the turn-on voltages was also seen.[4] Björklund et al showed that the turn-on voltage in OFETs with aluminum/aluminum oxide as gate/dielectric and poly(tri-arylamine) (PTAA) as the semiconductor can be tuned precisely by mixing different SAMs.[5]

The mechanism that causes the turn-on voltage shifts and gate leakage reductions is still under debate. It has been shown that the threshold voltage shifts scale with the intrinsic dipole moment of the SAM molecules both when the SAM is inserted between the gate electrode and the dielectric[6] and when the SAM is between the dielectric and the semiconductor[7]. In contrast, Ellison et al showed by using Kelvin probe force microscopy that the increase in surface conductivity in rubrene is due to an interfacial dipole at the SAM/semiconductor interface caused by ground state charge transfer over the interface.[8]

Using the turn-on voltage as an assay of the SAM-induced interfacial dipole is problematic since the turn-on voltage also depends on other factors besides the potential difference between gate and source, such as morphology. Chung et al used SAMs with different anchor groups but with the same head groups to minimize the effect of the morphology. The results show that the built-in potential is shifted by 0.41 – 0.5 eV in agreement with the difference in the surface potential and the shift on the turn-on voltage.[9] This is consistent with an interfacial dipole formation at the dielectric/SAM interface, and indicates that there can be an interfacial dipole at the dielectric/SAM interface as well as at the SAM/semiconductor interface as shown by Ellison *et al*[8]. Thus, it is generally insufficient to only probe either of the interfacial dipoles or the intrinsic molecular dipole moment in order to determine the overall effect on the device. In addition, SAMs have been shown to both increase the density of trapped charge (in the semiconductor) in PTAA-based transistors[10] and decrease the density of trap states in pentacene based transistors[11]. In order to elucidate the charge trapping dynamics the charge extraction by a linearly increasing voltage (CELIV) is a useful method.[12,13] CELIV can be used to differentiate between current transients due to extraction of a charge reservoir and displacement currents due to polarization.

In this paper, we demonstrate and clarify the trapping mechanism in AlO_x. We use CELIV to quantify the displacement current due to trapping in AlO_x. We apply different steady state offset potentials to establish equilibrium before applying the linearly increasing voltage (probe) pulse. The results are interpreted using a model based on the findings of Hickmott and Weber *et al.*[1,2]

Our model system is a diode with gold (Au) as top contact and aluminum (Al) with a layer of native oxide as the bottom contact. The organic semiconductor is N,N′-bis(2-(pentafluorophenyl)ethyl)-1,4,5,8-naphthalenetetracarboxylic acid diimide (5FPE-NTCDI). The aluminum oxide (AlO_x) surface is modified with triethoxy(octyl)silane (OTS) and 1H,1H,2H,2H-perfluorooctyltriethoxysilane (FOTS). 5FPE-NTCDI is one of a class of n-type small molecule organic semiconductors (naphthalenetetracarboxylic acid diimides, NTCDIs) synthesized by Katz and others.[14-16] 5FPE-NTCDI is expected to have roughly the same energy levels as the NTCDIs in (Ref. 15), i.e. LUMO ~ -3.7 eV and HOMO ~ -7.0 eV. Typical I-V characteristics show that the charge transport is highly contact limited (currents are two to three orders of magnitude lower than the space charge limited current).

A schematic view of the CELIV method is given in Fig. A.1. A linearly increasing voltage is applied over a sample with blocking contacts. The resulting current transient consists of two parts, a displacement current $j(0)$ and an extraction current Δj due to extraction of charge carriers in the bulk. If there are no (or very few) mobile carriers in the device $j(0)$ is simply given by:

$$j(0) = CA \qquad [A1]$$

where C = the geometrical capacitance and $A = U_{max}/t_{pulse}$, the voltage rise speed. The steady state potential over the device can be tuned by applying an offset voltage U_{OFFSET}.

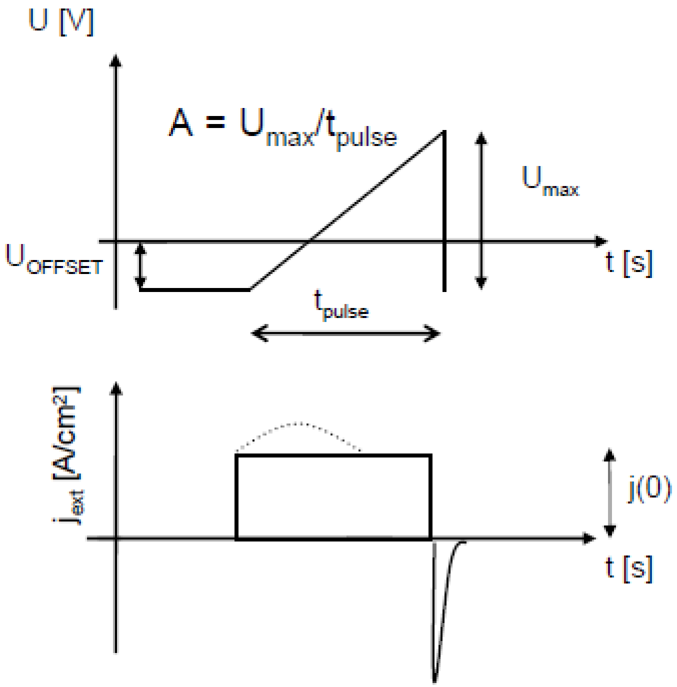

Figure A.1 Schematic view of the CELIV method.

The effect on the CELIV current transient of an insulator trap state density can be clarified by the following simplified analysis. Consider a constant continuous distribution of trap states in the oxide layer, as shown in Fig. A.2. When the quasi-Fermi level lies well within the trap distribution, that is $E_t < E_{Fn} < E_t + \Delta E_t$, the density of occupied traps n_t can be approximated by:

$$n_t \approx \frac{N_t}{\Delta E_t}(E_{Fn} - E_t) \qquad [A2]$$

where N_t is the total number of trap states in this distribution. By applying a potential over the metal, traps in the oxide layer will be filled. Assuming that the trapping and release times are much faster than the times associated with the applied voltage pulse (the voltage pulse is slow enough to maintain quasi equilibrium), and the quasi-Fermi level is determined by the applied voltage, we may approximate: $E_{Fn} \approx qU(t) - E_F = q(U_{OFFSET} + At) - E_F$. Where $U(t)$ is the voltage at time t and E_F is the Fermi level at thermal equilibrium ($U_{OFFSET} = 0$). The rate of electrons transferred between the oxide trap states and the metal is then given by:

$$\frac{dn_t}{dt} \approx \frac{qN_tA}{\Delta E_t} . \qquad [A3]$$

This can be seen as a charging of the oxide layer and the corresponding displacement current may be written as:

$$j_{D,t} = q\delta \frac{dn_t}{dt} = \frac{q^2\delta N_t A}{\Delta E_t} . \qquad [A4]$$

The total displacement current is then given by $j_D = j_{D,t} + j(0)$. When $E_{Fn} \rightarrow E_t + \Delta E_t$, $n_t \rightarrow N_t$, $j_{D,t} \rightarrow j(0)$ and $j_D = 0$.

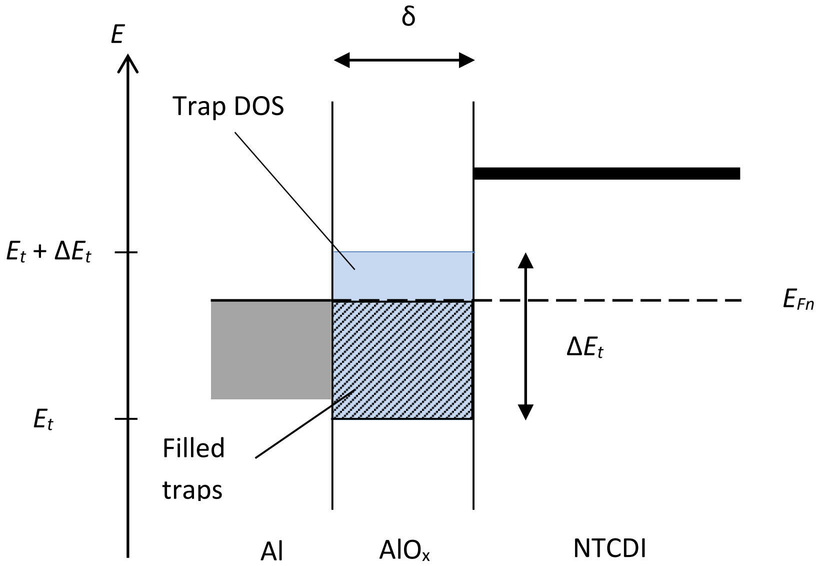

Figure A.2 Schematic of the trap DOS in AlOx under flatband conditions.E_{Fn} is the quasi Fermi level, E_t is the lowest lying trap level, ΔE_t is the width of the trap distribution and δ is the thickness of the oxide.

Figure A.3(a) shows the CELIV current transients at different offset voltages for an Al/AlO_x/5FPE-NTCDI/Au device. The offset and extraction voltages are applied to the gold contact, the voltage rise speed was A= +0.5V/10ms. One can see that when a positive offset voltage of +1 V is applied, the CELIV current transient corresponds well to the calculated $j(0)$ using equation (1), where the geometrical capacitance is given by the reciprocal sum of the capacitance of the organic layer and the oxide layer which is ~ the capacitance of the organic layer. This implies that $j_{D,t}$ is zero and the traps are filled due to the applied (steady state) offset voltage. When going from an offset voltage of + 1V towards negative offsets (that is, the quasi Fermi level is moved downward through the DOS), the CELIV transients increase in magnitude until finally they almost saturate at an offset of -0.25V. The trap DOS is then mostly emptied out by the offset voltage so when the CELIV pulse is switched on (with positive polarity) the trap DOS fills up as the quasi Fermi level moves up through the trap DOS and the total displacement current is then given by $j_D = j_{D,t} + j(0)$. The displacement current is only determined by the effective potential over the device as is evident from the applied potential at time 10 ms for U_{OFFSET}= -0.5V being the same as the applied potential at time 5 ms for the U_{OFFSET} = -0.25V, the effective potential being 0V for both cases, and their corresponding value of *j(0)* is also the same.

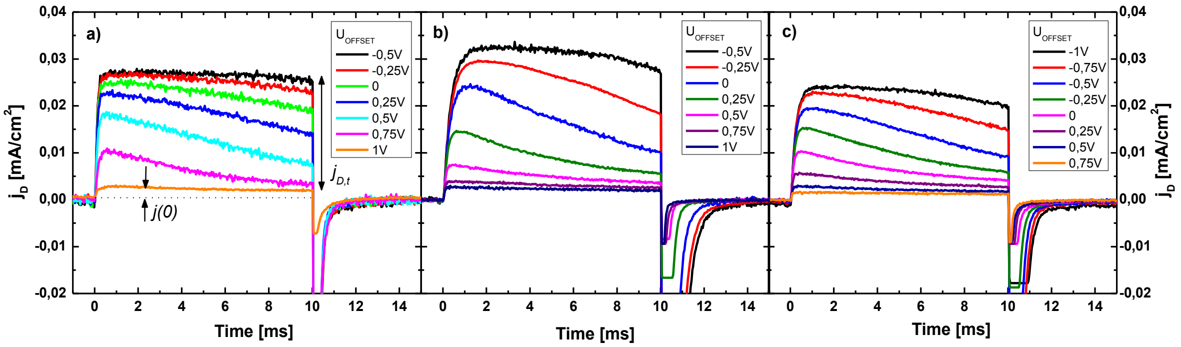

Figure A.3 CELIV current transients at different offset voltages for **(a)** an Al/AlO$_x$/NTCDI/Au device **(b)** an Al/OTS/AlO$_x$/NTCDI/Au device and **(c)** an Al/FOTS/AlO$_x$/NTCDI/Au device. The voltages are applied to the Au contact and A = +0,5V/10ms.

The same holds for U_{OFFSET} = -0.25V and U_{OFFSET} = 0V and so on. When the U_{max} is kept the same but the pulse length is lowered by a factor of ten (i.e. A is increased by a factor of ten), then the displacement current is exactly a factor ten larger and the shape of the curves stays the same. This indicates that quasi equilibrium is maintained during the ramp-up voltage pulse. It should be noted that extraction of equilibrium charge reservoirs[17] and injected charge reservoirs[18] looks very different. In particular, Sandén et al showed that the time at which the CELIV transient reaches its maximum value (t_{max}) shifts when the offset voltage is varied. This is not seen here, the transients reach their maximum value regardless of the offset around $t = \tau_{RC}$ (where τ_{RC} is the RC-time constant which is seen from the capacitor discharge when the CELIV pulse ends). Effectively the transients reach their maximum value directly the CELIV pulse is turned on, the t_{max} is shifted from zero only by the RC-time constant. The current transient for U_{OFFSET} = -0.5V is almost flat, it is thus fair to assume that the trap DOS is constant when going from -0.5V to 0V. Insertion of the experimental values $j_{D,t}$ = 0.026 mA/cm^2, ΔE_t = 0.5 eV and $\delta \approx 2$ nm into Eq. (2) gives a value for $N_t \sim 8\times10^{18}$ cm^{-3} in excellent agreement with the results obtained by Hickmott[1].

Figure A.3(b) shows the CELIV (A = +0.5V/10ms) current transients at different offset voltages for an Al/AlO$_x$/*__OTS__*/5FPE-NTCDI/Au device. The transients show similar behavior as for the bare oxide case, only slightly shifted towards more negative offset voltages. For the bare oxide case an offset voltage of +1 V is required to fill all the traps ($j_{D,t} \rightarrow 0$) while a voltage of +0.75 V is sufficient in the OTS case, as the additional +0.25 V is effectively furnished by the SAM. Conversely, OTS requires a higher negative offset in order to empty out the trap DOS (U_{OFFSET} ~ -0.5V as compared to ~ -0.25V for the bare case). Figure A.3(c) shows the CELIV (A = +0.5V/10ms) current transients at different offset voltages for an Al/AlO$_x$/*__FOTS__*/5FPE-NTCDI/Au device. Similar behavior is seen as for the previous two cases, but the shift towards negative voltage is even larger than for the OTS device, about 0.5 V as compared to the bare oxide case.

Due to the high trap density in the oxide, one can assume that all of the potential over the device drops over the oxide (when the Fermi level is within the trap DOS). Hence, a potential shift in the displacement current behavior by introducing the monolayer is equal to an applied potential or a vacuum level shift. This provides a method of directly probing the vacuum level shifts caused by the introduction of the SAMs in operating devices. In order to obtain more accurate values of the vacuum level shifts one can plot the displacement currents in Fig. A.3 as a function of applied voltage instead of time (Fig. A.4). If we assume that the shape of the DOS is not changed by the introduction of SAMs rather it is the position of the quasi Fermi level that is moved up or down, then the displacement currents in Fig. A.4 should be representative of the trap DOS. The saturation of the high and low displacement currents are apparent, though not easily quantifiable numerically. Instead, we quantify the potential at which the $j_{D,t}$ reaches half of its maximum value, and suggest that the amount by which this potential shifts with introduction of SAMs can be used as an assay of the vacuum level shift. From figure 4 one obtains a shift of ~ 0.45 V for OTS and ~ 0.85 V for FOTS towards more negative potentials on the Au electrode. When the displacement currents are shifted with the aforementioned potentials they are seen to overlap nicely confirming the validity of the assay and indicating that the shape of the trap DOS is not affected by the SAMs. This shift is also in agreement with prior observations by our group and others that these SAMs shift transistor turn-on voltages in corresponding ways.

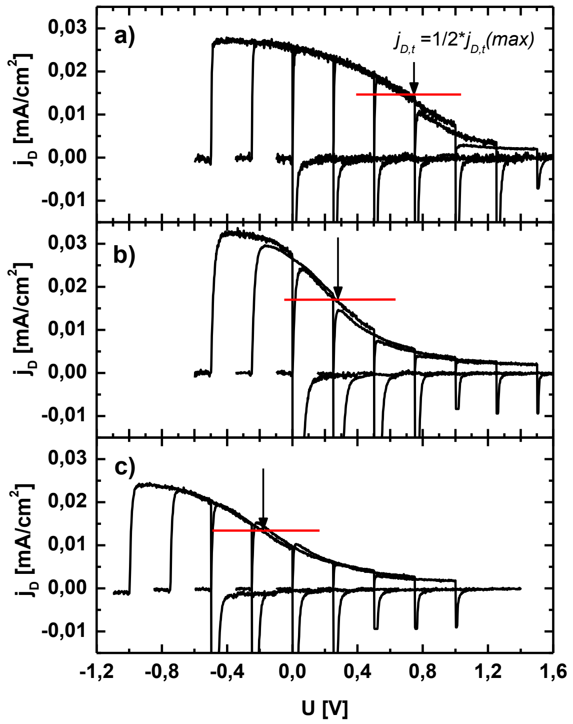

Figure A.4 The displacement current as a function of voltage for **(a)** an Al/AlO$_x$/NTCDI/Au device **(b)** an Al/OTS/AlO$_x$/NTCDI/Au device and **(c)** an Al/FOTS/AlO$_x$/NTCDI/Au device. The voltages are applied to the Au contact and A = +0.5V/10ms.

While the steady state voltage dependence of the displacement current reveals the vacuum level shift caused by interfacial SAM layers, it does not provide insights into the mechanisms of the dipole formation. The observed vacuum level shifts do not scale with the intrinsic dipole moments of the SAM molecules since the internal dipole moment for FOTS is roughly ten times that of OTS in the gas phase.[8] It is clear that interfacial dipoles due to ground state charge transfer, formation of polar Si-O-Al linkages, and/or Van der Waals interactions between the SAM and semiconductor affect the overall vacuum level shift observed.

Scanning Kelvin probe microscopy (SKPM) was carried out to see if the voltage shifts obtained in the CELIV measurements could be understood as a vacuum level shift caused by an interfacial dipole at the oxide/SAM interface. However, the shifts were very small (~ 100 meV) and cannot account for the potential shift observed in Fig. A.4. Thus we conclude that the observed vacuum level shifts must be at least in part due to an interfacial dipole at the SAM/semiconductor interface in agreement with Ellison *et al.*[8]

We note that the fairly large trap DOS demonstrated here has implications for the operation of thin film transistors using thin AlO_x as dielectric. Care needs to be taken when choosing materials for the device; if the turn on voltage corresponds to a potential where the quasi Fermi level is within the trap DOS, the turning on and off of the transistor will be associated with emptying and filling of the trap DOS (for n-channel devices). Furthermore, a filled trap DOS will result in high gate leakage due to trap-assisted conduction through the oxide. This is not limited to AlO_x, as initial studies on devices with 10 nm silicon oxide as dielectric show similar results.

In conclusion, we have performed CELIV measurements on Al/AlO_x/NTCDI/Au devices and modified the AlO_x surface with two different SAMs, OTS and FOTS. Results show a large displacement current due to an electron trap density on the order of 10^{19} cm^{-3} located around 4-5 eV below vacuum in the oxide layer. The filling of the traps when the Fermi level is moved through the trap DOS is seen as a displacement current which is on the order of 15 times the geometric capacitance. When the traps are filled, the displacement current saturates to the geometrical capacitance value. The displacement current behavior on the applied potential shifts towards more negative voltages on the Au when the self-assembled monolayers are introduced, is consistent with a vacuum level shift. The shift is ~ 0.45 V for OTS and ~ 0.85 V for FOTS. The shifts cannot be explained completely by the intrinsic dipole moment or by an interfacial dipole at the oxide/SAM interface, leading to the conclusion that an interfacial dipole at the SAM/semiconductor interface must play a role.

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Appendix B: Fabrication of Lateral Transistors

This appendix includes all of the supplementary information included in the publication of Chapter 2 in ACS Nano. It was written by T. J. Dawidczyk in its entirety, and is included only for the reader's benefit when interpreting the results of Chapter 2, as relates to the uncertainties in interface location and surface potentials arising from fabrication procedures. A much more detailed description of the fabrication of lateral transistors is available in T. J. Dawidczyk's dissertation "Interfacial Fields in Organic Field-Effect Transistors and Sensors", Copyright T. J. Dawidczyk.

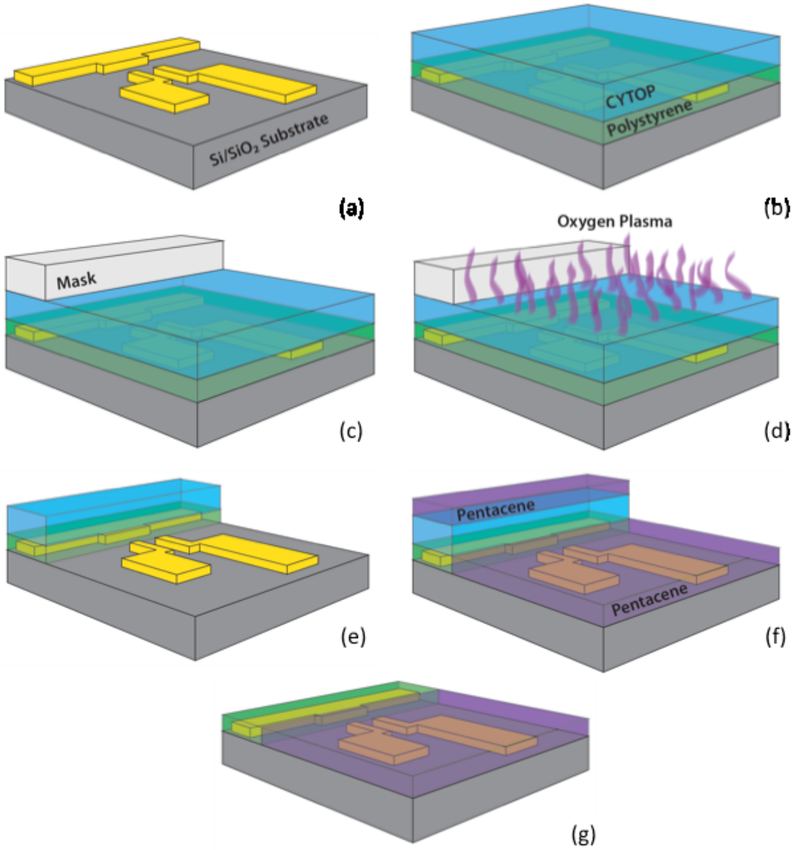


Figure B.1 Schematic of the fabrication process for the lateral OFETs. **(a)** 50 nm gold electrodes with a 5 nm Cr adhesion layer are deposited on the Si/300 nm SiO_2 substrate via photolithography. **(b)** Atactic polystyrene (MW 50,000g/mol) (20 mg/mL in toluene) or poly (3-trifluoromethyl)styrene, (F-PS, 10 mg/mL in tetrahydrofuran) or poly(methyl methacrylate) (PMMA, 20 mg/mL in chlorobenzene, heated at 80 °C to dissolve) is then deposited via spin coating at 2000 RPM for PS and PMMA, and 1000 RPM for F-PS. The sample is annealed at

95°C for 10 minutes and allowed to cool to room temperature. Cytop is deposited via spin coating at 2000 RPM and annealed at 95°C for 10 minutes. **(c)** A physical mask is placed on the substrate so that the edge of the mask is in the gap between the source/drain electrodes and the gate electrode. **(d)** Oxygen plasma at medium power is used to remove the unmasked polymer layers. **(e)** Once the organic layer has been removed from above the source/drain electrodes the OSC can be deposited. **(f)** 50 nm of pentacene is thermally evaporated at 0.3 Å/s. **(g)** The Cytop layer is then removed with perfluorodecalin, exposing the interface between the polymer and pentacene.

Experimental Procedure

Multiple samples were prepared on the same Si wafer, so the wafer was cleaved to get one or two samples per section. All KPM scans had 256 points and the retrace height for the surface potential was 100 nm. After the KPM scans the transistor measurements were performed. Each lateral OFETs was tested in the same manner, with the output curves taken first, followed by the transfer curves. Only these two measurements were taken, to keep the charges injected in the PS dielectric more consistent.

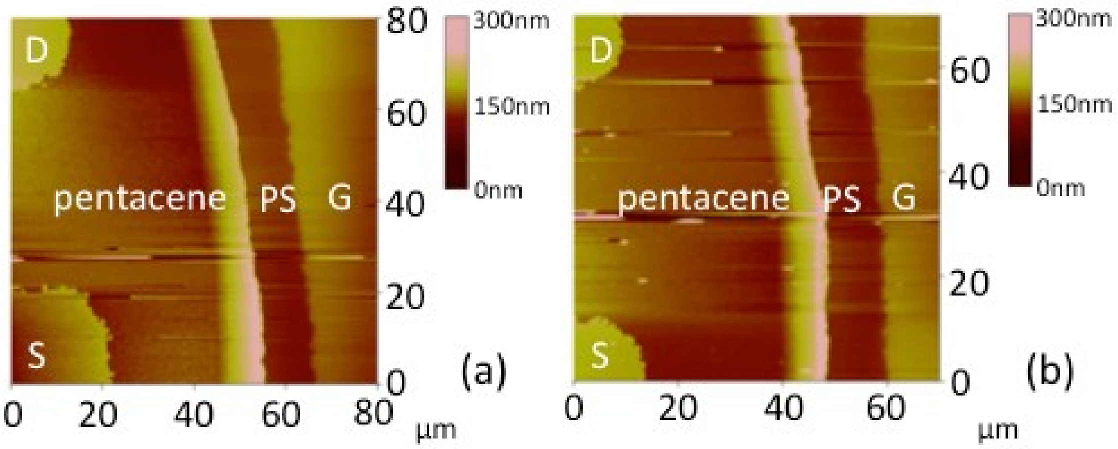


Figure B.2 Height scans of the two samples from Figure 2 in the main text. The source (S), drain (D) and gate (G) are indicated in addition to pentacene and PS. Note that the edge of the pentacene closest to the PS has a slight height increase.

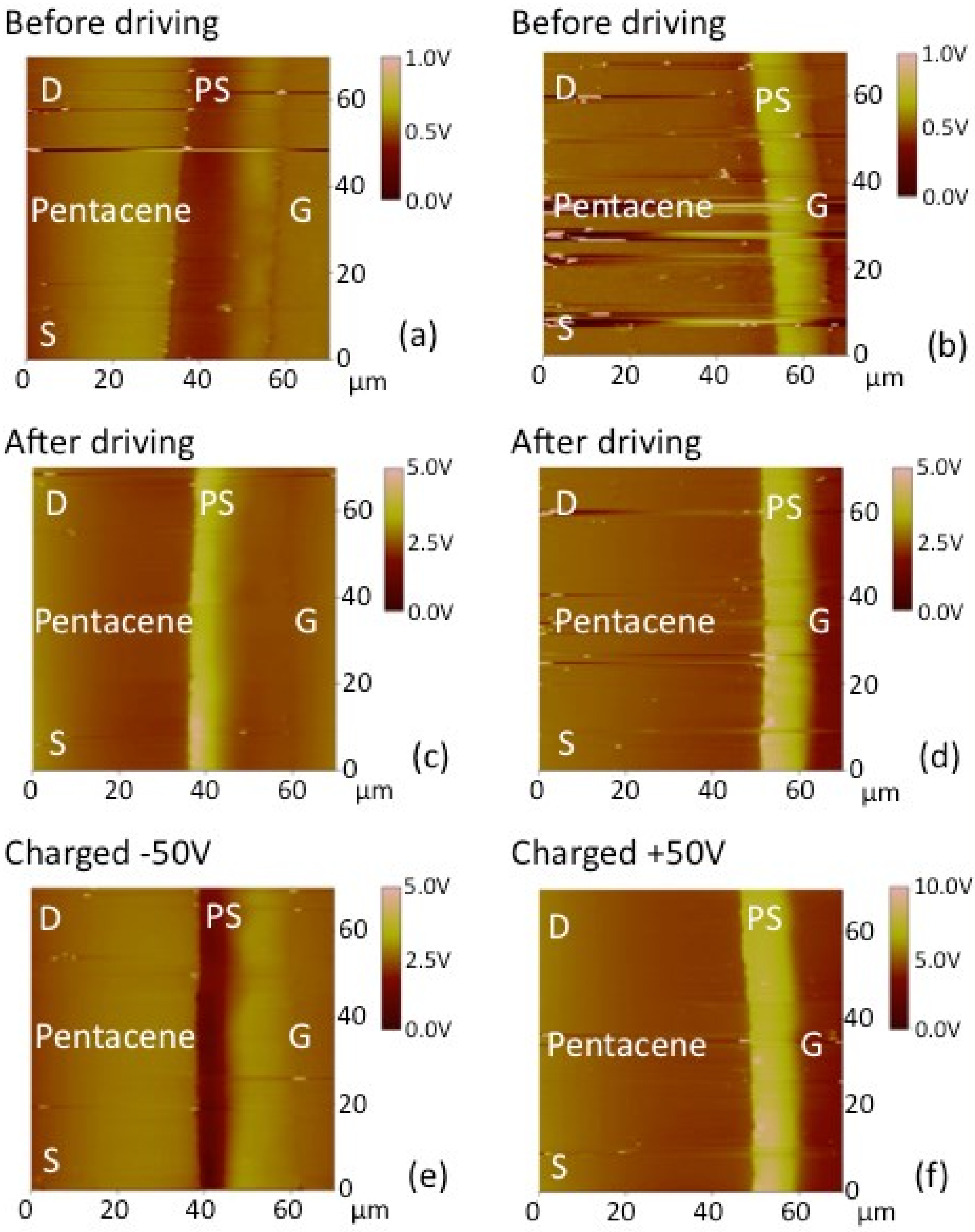


Figure B.3 KPM scans of two separate samples (a,c,e) (b,d,f)**.** In all images the source and drain electrodes are on the top and bottom of the left side while the gate electrode is on the right side. The samples are first imaged before electrical testing **(a,b)**. After the transistor electrical measurements the samples are scanned **(c,d)**. The samples were then charged to -50 V **(e)** and +50 V **(f)** for 10 minutes and rescanned.

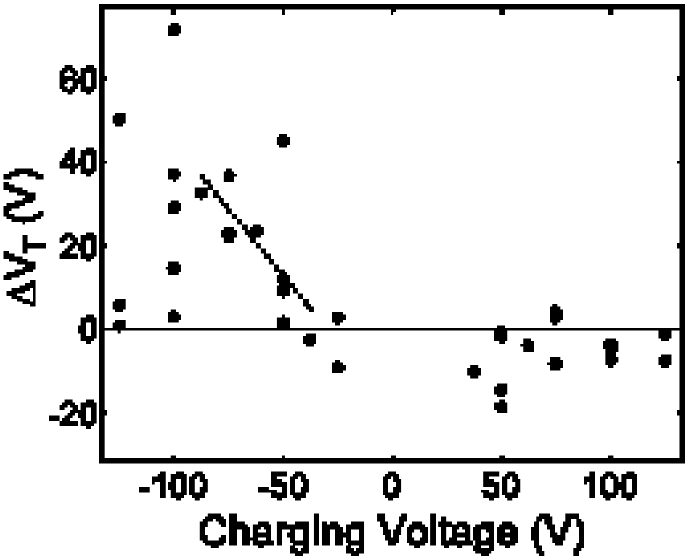


Figure B.4 Dependence of VT shift on charging voltage. The dotted line indicates the region where the correlation is strong. Above 100 V, the devices break down. At positive charging voltages, the correlation is poorer than for negative charging voltages.

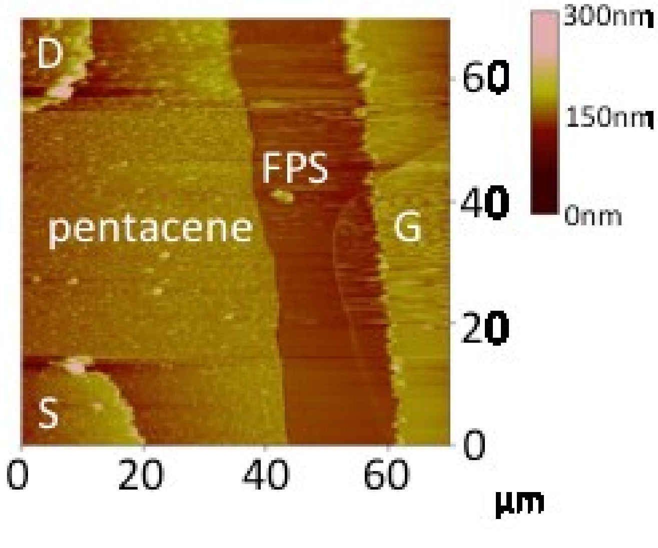
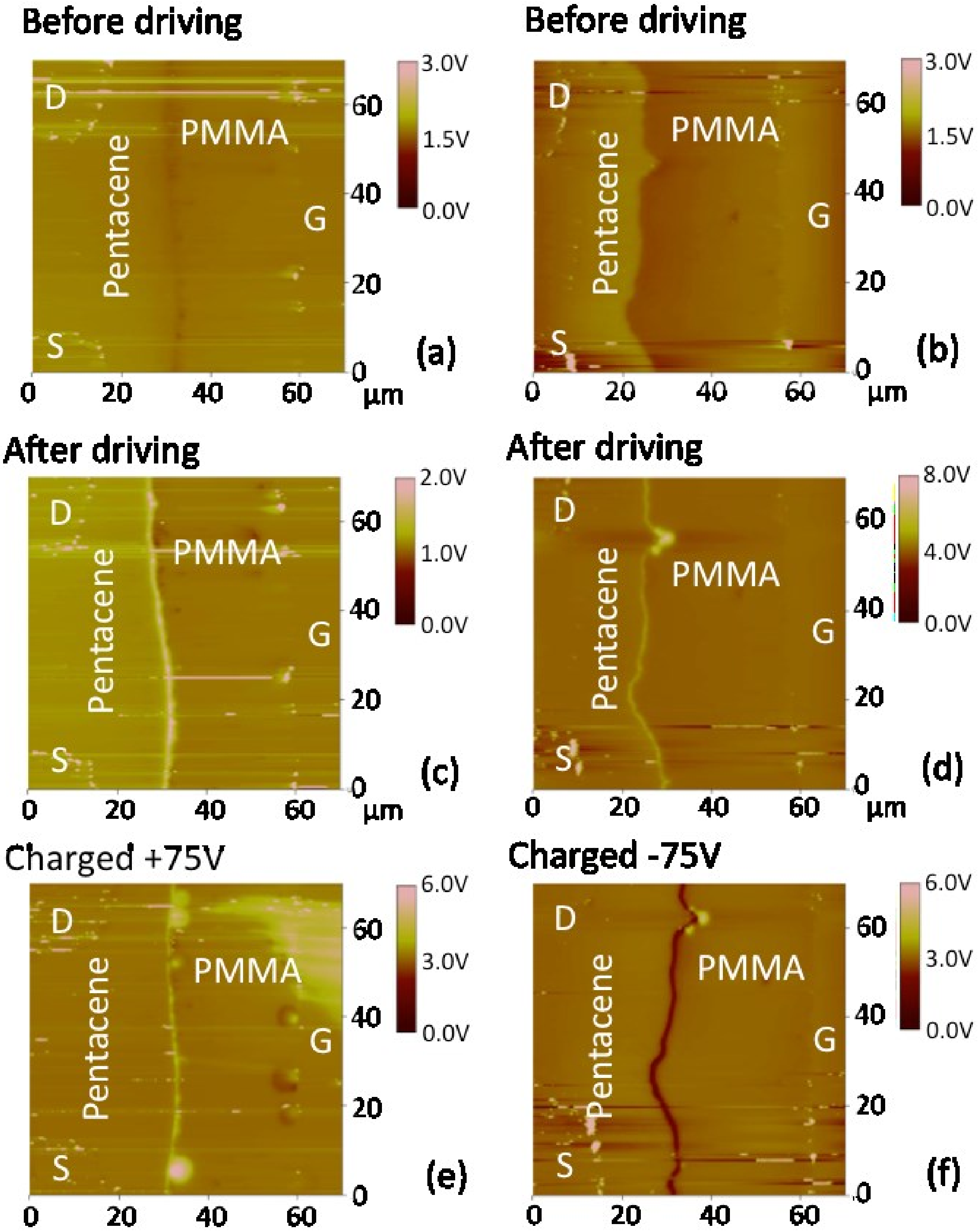


Figure B.5 KPM height scan from the F-PS sample (Figure 9 main text) with all the features labeled.



Before driving

Before driving

After driving

After driving

Charged +75V

Charged -75V

Figure B.6 KPM scans of two separate PMMA samples (a,c,e) (b,d,f). In all images the source and drain electrodes are on the top and bottom of the left side while the gate electrode is on the right side. The samples are first imaged before electrical testing **(a,b)**. After the transistor electrical measurements the samples are scanned **(c,d)**. The samples were then charged to +75 V **(e)** and -75 V **(f)** for 10 minutes and rescanned.

Bias stress experimental procedure

Conventional "vertical" OFETs were fabricated to see the bias stress behavior of pentacene on PS and F-PS. Polymer dielectric solutions were deposited by spin coating on heavily n-doped Si wafers with 100nm thermally grown oxide. PS and F-PS were deposited by spin coating at 2000 RPM for PS and 1000 RPM for F-PS, the same manner as with the lateral transistors. To pre-charge the dielectrics the samples were corona charged with the indicated grid potential as in out previous work [6]. 50 nm of Pentacene was thermally evaporated at a rate of 0.3 Å/s. Top contacts of 50 nm of gold were thermally evaporated using a shadow mask at a rate of 0.5 Å/s. The OFET transfer and output curves were taken, then the device was subjected to a bias stress with V_g and V_d held at -45 V while V_s was grounded.

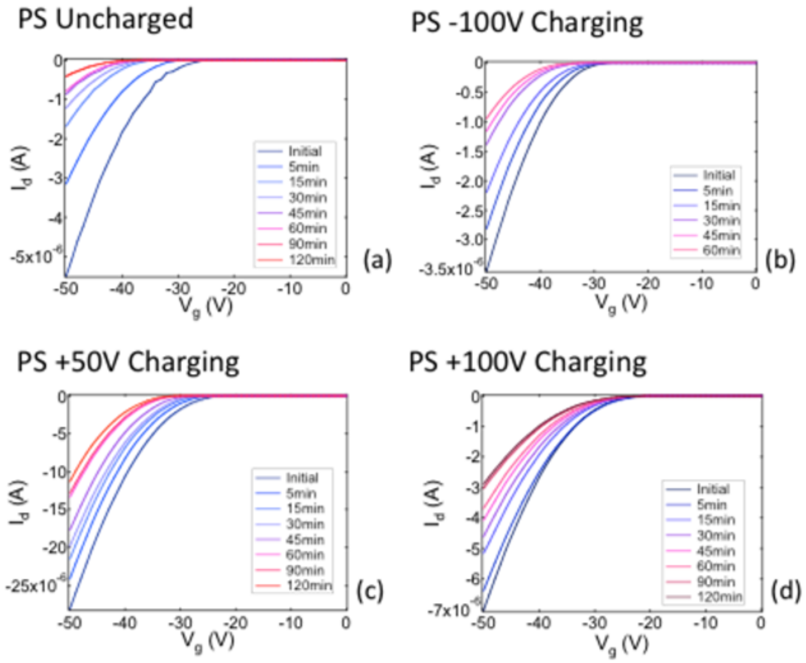


Figure B.7 Bias stress behavior of PS dielectrics at various charging levels: uncharged **(a)**, -100 V **(b)**, +50 V **(c)**, and +100 V **(d)**. Note the difference in scales.

Curriculum Vitae

Josué F. Martínez Hardigree was born April 10, 1985 in Mayagüez, Puerto Rico. During high school he developed an interest in laboratory science, undertaking his first project studying snail-transmitted bacteria at Inter-American University under the tutelage of Prof. Freddy R. Medina Rodriguez. Following an interest in robotics, he worked on modeling the motion of a mechanical turtle robot arm at Universidad Metropolitana with Dr. Juan Arratia, the results of which he presented at the 2002 IEEE Junior Engineering and Science Conference. The following summer Josué enjoyed the opportunity to study magneto-optically active thin films at University of Michigan under the guidance of Prof. Roy Clarke as part of the NASA SHARP Plus program. Seeking a better preparation in mathematics after this experience, he transferred to Centro Residencial para Oportunidades Educativas en Mayagüez (CROEM), a residential science magnet high school for his senior year.

Josué graduated in 2003 from CROEM and left Puerto Rico to pursue undergraduate studies at Massachusetts Institute of Technology. While at MIT, Josué became actively engaged in the Undergraduate Research Opportunities Program from the first week of freshman year, joining the Smart Architectural Surface group with Prof. V. Michael Bove at the MIT Media Lab. Following a summer internship at California Institute of Technology studying hot-wire chemical vapor deposition for amorphous silicon photovoltaics in the Harry Atwater group, Josué shifted his attention to the study of electronic materials. He subsequently worked with Prof. Vladmir Bulovic's group studying charge trapping at metal/organic interfaces in organic light-emitting diodes and memories. To round out his experience with electronic materials, Josué worked with Prof. Eugene Fitzgerald on the fabrication of AlInGaP waveguides as part of his undergraduate thesis. Following his graduation in 2007, Josué opted to step away from the laboratory and pursue his interests in global finance at the MIT Investment Management Company as their first entry-level analyst. Despite the unparalleled learning experience gained during the ongoing financial crisis, he found himself longing to develop his own engineering skillset with an eye towards commercializing organic electronics. In 2009 he joined the Howard Katz group at Johns Hopkins University where he has since studied organic semiconductors in an array of electronic devices and architectures.