

A front-end PFC stage for improved performance of flexible induction heating appliances

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Abstract. Flexible cooking surfaces, eg. fully active surfaces, have gained lately an increasing importance in the domestic induction heating. Multi-inverter structures are a cost-efficient solution to develop this technology. However, they add control restrictions that can be solved with a power factor corrector (PFC) stage as proposed in this work.

The proposed converter and modulation strategy work with zero voltage switching (ZVS), decreasing the switching losses, enabling a higher working frequency and, therefore, decreasing the magnetic devices size. The bus voltage is controllable and can be increased, easing the load power control and decreasing current through load and inverter and, so, the power losses. Besides, the switching frequency is constant in the mains cycle and can be modified to synchronize the load inverter and the PFC stage avoiding intermodulation noise. A 3.6 kW prototype has been implemented fulfilling the EMC requirements. The experimental waveforms and efficiency have been measured to prove the feasibility of this proposal.

Keywords: Power factor corrector, resonant power conversion, zero voltage switching, home appliances, induction heating

1. Introduction

In recent years, induction heating (IH) technology has become a reality in our homes [1–5]. This cooking technology has been developed in depth, and it has revolutionized the cooking way. In comparison with typical technologies, such as gas, electric or halogen, IH is more efficient, faster, cleaner and safer [6].

Recently, flexible cooking surfaces have taken importance in the domestic IH technology [7]. There are different types of surfaces with concentric coils or with coils spread along the whole surface, which are denominated fully active surfaces (Fig. 1). These allow heating several pots, no matter the size or shape of these.

The coils from a typical IH cooktop are supplied by an inverter, usually a half-bridge, which is the most common topology in these applications. However, the development of flexible cooking surfaces has brought an increase of the manufacturing cost due to the increased number of coils and power electronics devices. In order to achieve a cost-effective implementation, some multi-inverter structures have been

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Fig. 1. Fully active surface [17].

proposed recently [8–10]. However, these structures add control restrictions and complicate the power control in the induction loads [2].

In order to overcome these restrictions, a power factor corrector (PFC) front-end stage has been proposed. The PFC stage assures a power factor close to the unity, a low harmonic distortion and generates a controllable DC voltage bus. This stage allows separating the mains from the multi-inverter structure, fulfilling EMC requirements [11–16] and making easier the control of the output power in the pot [17–19]. Besides, the bus voltage can be increased, decreasing the current through IH inverter and IH load, and, therefore, decreasing losses in these devices.

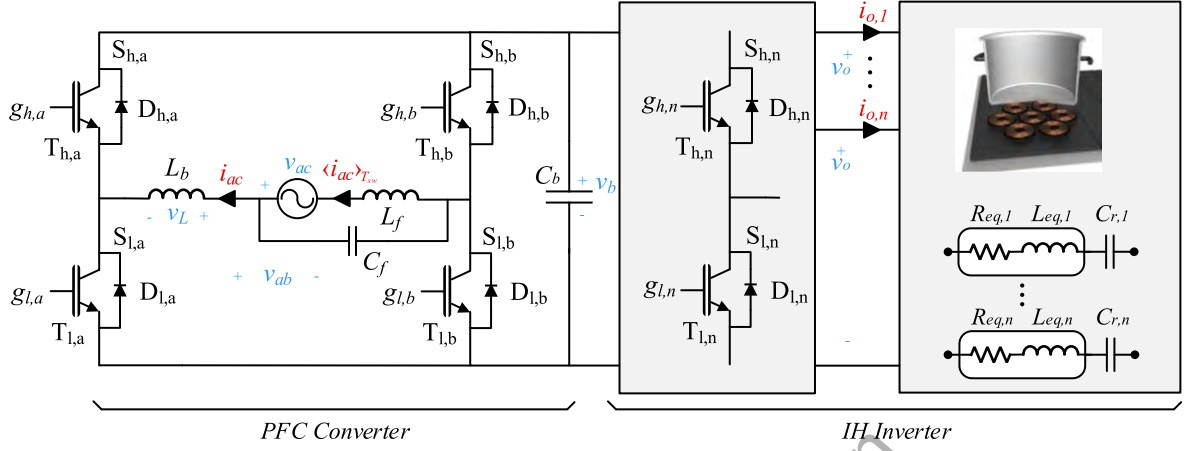
Furthermore, having into account that induction heating cooktops with fully active surfaces have usually two isolated electronic board because they are powered from two mains phases, and in order to reduce manufacturing cost implementing multi-inverter structures, it is interesting to join both electronic boards. This idea can be implemented with a front-end PFC to get a common DC bus. In this way, the total board size and several components such as DC-DC, relays, digital electronic components or heatsinks can be reduced.

The paper is structured as follows. The next section presents the topology of the converter and the operation mode, the control strategy section describes how the converter control is performed. After that section, the implementation and the experimental results are shown and, finally, the main conclusions of this work.

2. Converter topology and operation mode

2.1. Converter topology

The proposed PFC converter is shown in Fig. 2. It is based on the boost converter and it is composed of two half-bridge legs, a and b, which allow short-circuiting the boost inductance, L_b , with the mains voltage, v_{ac} , with a period T_{ac} , and/or the bus voltage, v_b . Each half-bridge is composed of two switching devices, S_h and S_l , implemented with IGBTs, T_h and T_l , and antiparallel diodes, D_h and D_l . A filter between the mains and the PFC stage is placed, supplying the medium frequency currents and removing the high ripple of the boost coil current, i_{ac} . In the proposed implementation, an inductor, L_f , and a capacitor, C_f , are used for filtering. Besides, a capacitor, C_b , filters the bus voltage, which powers the IH inverter. The set is composed of as many half-bridge branches, $S_{h,n}$ and $S_{l,n}$, as IH loads. Each IH load [20] is composed of the series equivalent resistance, $R_{eq,n}$, and inductance, $L_{eq,n}$, and the resonant capacitor, $C_{r,n}$.

Fig. 2. PFC IH topology with n IH-loads [19].

2.2. Operation mode

The PFC converter works in full-bridge configuration in order to get Zero Voltage Switching (ZVS) and fixed-frequency Continuous Conduction Mode (CCM) as is shown in Fig. 3. In this way, the $T_{h,a}$ device and the $T_{l,b}$ device are activated simultaneously, and vice versa. Therefore, the boost voltage, v_L , according to the activated devices is

$$v_L = \begin{cases} v_{ac} - v_b, & T_{h,a}, D_{h,a}, T_{l,b}, D_{l,b} : \text{ON} \\ v_{ac} + v_b, & T_{l,a}, D_{l,a}, T_{h,b}, D_{h,b} : \text{ON} \end{cases} \quad (1)$$

For each branch, the duty cycle can be defined as

$$D_a = \frac{1}{2} \left(1 + \frac{v_{ac}}{v_b} \right), \quad D_b = \frac{1}{2} \left(1 - \frac{v_{ac}}{v_b} \right). \quad (2)$$

This operation mode has several advantages. Firstly, the zero-crossing distortion of the current is avoided because the duty cycle is 0.5 when the mains voltage is zero ($v_{ac} = 0$), simplifying the converter control and fulfilling EMC requirements. Secondly, this modulation strategy works with ZVS switching, decreasing the switching losses, enabling a higher working frequency, and, therefore, decreasing the value of magnetic devices: the boost inductance and the filter inductance. Besides, the switching frequency is constant along the mains cycle and can be modified to synchronize the load inverter and the PFC stage avoiding intermodulation noise. The main disadvantage is the current through the boost inductance and switching devices of the PFC converter is higher, increasing conduction losses in these components.

3. Control strategy

The converter control consists on generating a sinusoidal reference current, $i_{f,ref}$, in phase with the mains voltage and with the desired RMS current value, $I_{f,rms}$. The regulator adjusts the mains current, i_f , to follow the reference exactly. The main advantage of using the control of the current managing the duty cycle, D_a , is the converter can work at constant frequency avoiding intermodulation noise between IH inverter and PFC stage. This duty cycle must be controlled in order to get a sinusoidal mains current

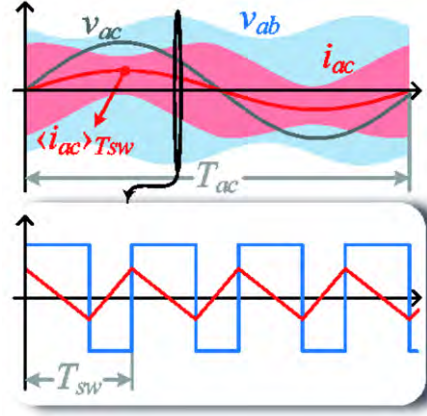


Fig. 3. ZVS and fixed-frequency CCM modulation strategy [17].

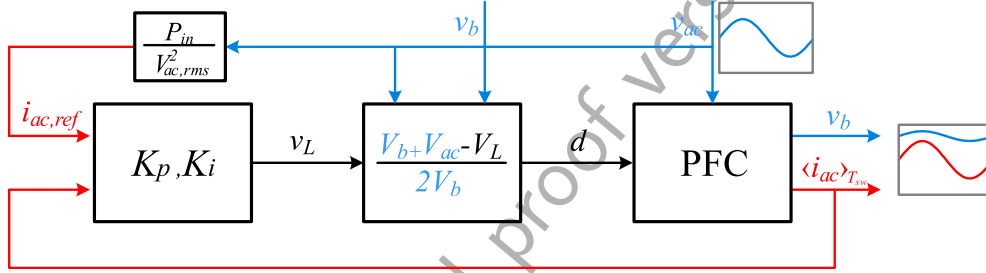


Fig. 4. Control scheme where the calculated action is the boost inductance voltage, V_L , which is used to calculate later the duty cycle by using the converter parameters [18].

waveform in phase with the mains voltage. In this way, a good power factor and a low total harmonic distortion of the current is achieved.

In order to control the system and to eliminate the stationary error, a proportional, K_p , and integral, K_i , regulator is proposed. In typical control schemes, the action calculated by the regulator is directly the duty cycle, D_a , applied to the PFC stage. However, this system is difficult to control using this scheme because its non-linearity which depends strongly on the mains voltage, the bus voltage, and the induction load.

To overcome this issue, using the boost coil average voltage, V_L , as controller output action is proposed, as it is shown in Fig. 4. When the average voltage in an inductance differs from zero, it means a lineal variation of its average current according to the differential equation that models the boost coil behavior. Consequently, the V_L voltage makes possible to control the boost coil average current, I_b , linearly and, therefore, the mains current, i_f , can be properly shaped. Keeping in mind Eq. (2), the duty cycle can be calculated in a second step as

$$D_a = \frac{V_b + V_{ac} - V_L}{2V_b}, \quad D_b = 1 - D_a, \quad (3)$$

where V_{ac} and V_b are the mains and the bus average voltage in a switching cycle, respectively.

In order to perform this control, the input voltage, v_{ac} , the input current, i_f , and the bus voltage, v_b , must be measured.

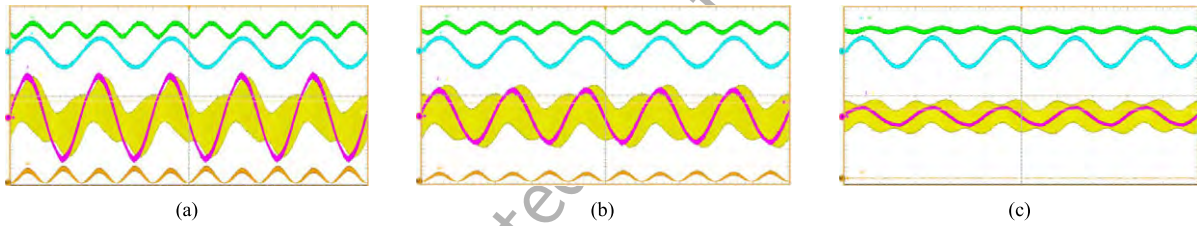


(a)

PARAMETER	VALUE
Mains voltage, $V_{ac,rms}$	230 V RMS, 50 Hz
Input power range	750-3600 W
Operating frequency range	20-30 kHz
Filter capacitor, C_f	6,6 μ F
Filter coil, L_f	200 μ H
Bus capacitor, C_b	60 μ F
Boost coil, L_b	150 μ H
Resonant capacitor, C_r	536 nF
IH-load equivalent inductance, L_{eq}	170 μ H
IH-load equivalent resistance, R_{eq}	6 Ω

(b)

Fig. 5. Experimental prototype (a) and converter design parameters (b).

Fig. 6. Main waveforms of the converter input and PFC stage delivering (a) 3.600 W, (b) 2.300 W and (c) 750 W: boost coil current, i_b , (30 A/div, yellow), mains voltage, v_{ac} , (400 V/div, blue), mains current, i_f , (10 A/div, purple), bus voltage, v_b , (400 V/div, green), and input power, p_{in} , (10 kW/div, brown). Time: 10 ms/div.

4. Implementation and experimental results

4.1. Prototype

In order to prove the feasibility of the proposed topology, a 3.6 kW prototype with one IH load has been designed and implemented. The operating frequency has been set to be higher than 20 kHz to avoid acoustic noise. The final prototype is shown in Fig. 5. It is composed of a three-phase module, FS150R12PT4, with three half-bridges on parallel using 1200-V Infineon IGBTs. A Spartan-6 FPGA from Xilinx is used to implement the control architecture. Besides, the whole system can be managed from the PC through a Wi-Fi module and a PC application has been developed using Visual Basic.

The 150 μ H boost inductance, L_b , and the 200 μ H filter inductance, L_f , have been implemented as 10 cm diameter air core toroids with 43 and 50 loops, respectively. The current is measured with the CDS4050 magneto-resistive current sensors from Sensitec and the voltage is measured using resistive dividers. The analog to digital conversion is performed using a 10-bit and 1-MSPS ADCS7477 converter from Texas Instruments.

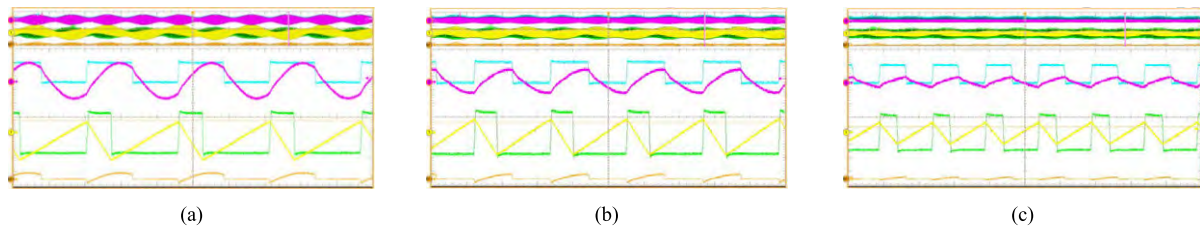


Fig. 7. Detail of the main waveforms of the converter output and PFC stage delivering (a) 3.600 W, (b) 2.300 W and (c) 750 W: boost coil current, i_b , (30 A/div, yellow), load voltage, $v_{o,c}$, (400 V/div, blue), load current, i_l , (30 A/div, purple), voltage between a and b half-bridges, $v_{o,ab}$, (400 V/div, green), and output power, p_{out} , (50 kW/div, brown). Time: 20 μ s/div.

4.2. Experimental results

The experimental results proving the proper operation of the converter are shown in Fig. 6 and Fig. 7 at different powers: 3.600 W in (a), 2.300 W in (b) and 750 W in (c), with a 400-V DC bus voltage. The main waveforms of the PFC stage are shown in Fig. 6, including the bus voltage, v_b , the mains voltage, v_{ac} , the boost coil current, i_b , and the mains current, i_f , whereas a zoomed detail of the load and PFC stage waveforms are shown in Fig. 7. The ZVS operation can be seen for both cases.

At maximum power, the converter is working at 20.5 kHz achieving a 92.5% efficiency. The EMC harmonic emissions for A-class devices are below the maximum limit. The achieved power factor is 99.7% while the current harmonic distortion, THDi, is 2.9%.

5. Conclusions

In this paper, a PFC front-end stage, its operation mode and its control strategy have been proposed to improve the flexible cooking surfaces. This stage allows controlling and increasing the bus voltage, easing the output power control and decreasing the power losses in the IH inverter due to the current through the IH load and inverter is lower.

The proposed operation mode and control strategy work with zero voltage switching (ZVS), decreasing the switching losses, enabling a higher working frequency and, therefore, decreasing the magnetic devices size. Besides, the switching frequency is constant in the mains cycle and can be modified to synchronize the load inverter and the PFC stage avoiding intermodulation noise. Finally, a 3.6 kW prototype has been implemented fulfilling EMC requirements and proving the feasibility of this proposal.

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