A 1.8 V Gm-C Highly Tunable Low Pass Filter for Sensing Applications

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***Abstract*—This paper presents a fully integrated, first-order Low Pass Filter with 2-tuning points giving a wide versatility to the filter. It allows for a fine/thick tuning with a cutoff frequency that spans over several orders of magnitude, from 220 mHz to 39.1 kHz. The G_m-C filter proposed is designed in a 180 nm CMOS technology with a total power consumption of 1.08 µW for a 1.8 V power supply and a dynamic range up to 73 dB. The proposed filter is a very competitive solution compared with previously reported works, meeting the requirements for portable on chip sensor interfaces based on impedance spectroscopy and biosignal front-end interfaces.**

Keywords— Analog Low Pass Filter (LPF); impedance spectroscopy; sub-Hz frequency; G_m-C; low-voltage low-power; programmable filter.

I. INTRODUCTION

The growing demand of portable sensing devices for a wide variety of applications has raised the interest in minimizing the power and area consumption of every element that compose these devices. Within such fully integrated front-end interfaces, Low Pass Filters (LPF) are key building blocks extensively used in portable devices to process different physiological signals [1-3], as well as being a critical block in the readout stage of Electrochemical Impedance Spectroscopy (EIS) systems [4, 5].

The motivation of this paper is the design of a low pass filter with a wide range of frequencies, covering the ranges of several biological signals as well as the sub-Hz ranges of EIS, while at the same time keeping a high dynamic range and low area and power consumption, so that it can be used as a reconfigurable high-performance LPF within portable sensing device platforms capable of measuring a wide variety of signals.

Most of the biological signals recovered from techniques such as electrocardiogram (ECG) [1] or cell evaluation [4], operate at frequencies below the tens of kHz [6]; in this case LPFs are required to eliminate the contribution of signals at higher frequencies (Fig. 1a). Table I presents a brief review of different biological signals with the standard sensors employed to measure the signals and the frequency range at which they work. For electrochemical impedance spectroscopy, LPFs are employed as DC extractors placed at the end of a readout chain of sensor interfaces, in this case requiring sub-Hz cutoff frequencies, such as in Lock-In Amplifier (LIA) based systems (Fig. 1b).

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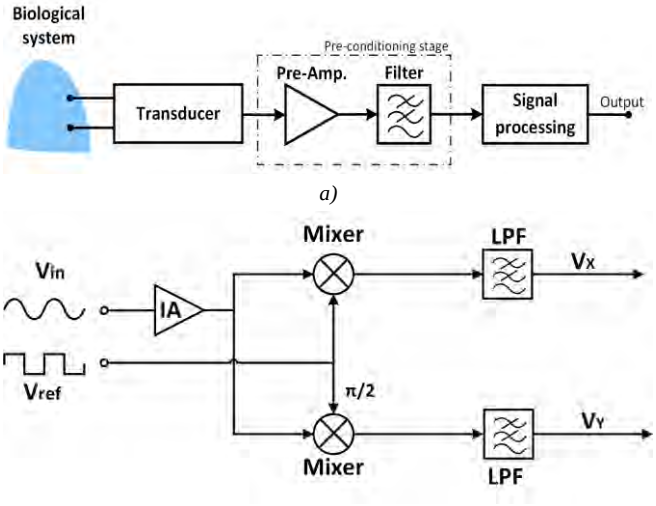

Fig. 1. Block diagram of: a) general-purpose biosignal front-end interface; b) Dual-Phase Lock-in Amplifier.

Lock-in Amplifiers are based on a technique known as phase sensitive detection (PSD), that through synchronous demodulation at a reference frequency f_o extracts the amplitude and phase (V_x and V_y from Fig. 1b) of very small signals even in noisy environments. This makes it an interesting technique for a wide variety of non-organic markers (gas detection) [5, 7] and biomarkers (proteins, cells, DNA, etc.) [4, 8, 9]

The complexity of designing a fully integrated Low Pass Filter with such a wide frequency range -from sub-Hz to tens of kHz- preserving high performance and low-voltage low-power (LVLP) operation, has led to typically implement these LPFs as external passive RC elements, hindering the achievement of SoC miniaturized solutions, or to design an integrated LPF with fixed f_c for each application.

Previously reported works present either very low cutoff frequencies [10, 11] or certain range of programmability, but they fail to put together both characteristics: to have a programmable frequency range from the sub-Hz to the kHz range, with a low-voltage low-power consumption and a reduced area topology to comply with the requirements of portable devices.

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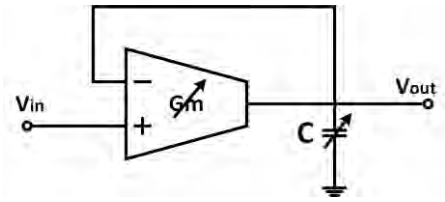
TABLE I. REVIEW OF BIOLOGICAL SIGNALS AND THEIR RANGE OF OPERATION [6]

Biological signal	Frequency range	Standard sensor
ECG	0.01 – 250	Skin electrodes
EMG	10 – 150	Needle electrodes
Nerve potential	DC – 10k	Surface or needle electrodes
Blood flow	DC-20	Electromagnetic or ultrasonic
Phonocardiography	5 – 2k	Microphone

A review of the literature shows that the most common technique to achieve a fully integrated CMOS LPF is to use a G_m-C structure (Fig. 2). To achieve sub-Hz frequencies, C is maximized (up to 50 pF due to technology limitations) and G_m minimized. With these values, the transconductance needs to be in the order of nS, requiring transconductance reduction techniques.

In this paper, we present an active G_m-C Low Pass Filter integrated in a 180 nm CMOS technology. It includes two different tuning techniques to adjust the transconductance and therefore, the cutoff frequency of the filter, as well as two different digitally programmable load capacitors (5 pF and 50 pF), to further expand the cutoff frequency –in our particular case increasing by an order of magnitude the maximum cutoff frequency-. In this way, a multi-decade frequency tuning low pass filter is proposed covering the ranges of a great number of applications. Besides, it exhibits a high dynamic range, with minimum noise and high input common range, while at the same time satisfies the low-voltage low-power and minimum area constraints of portable devices, being a very competitive general purpose reconfigurable solution.

The paper is organized as follows. Section II describes the proposed G_m-C structure and the techniques used to provide programmability to f_c. In Section III, post-layout simulation results are summarized. Finally, conclusions are drawn in Section IV.



$$f_c = G_m/2\pi C \quad (1)$$

Fig. 2. Single-ended G_m-C integrator; both G_m and C can be varied to adjust the cutoff frequency.

II. ACTIVE FILTER STRUCTURE

In this section, it will be firstly introduced the core of the structure. Then, the two G_m-tuning strategies will be presented together with the full schematic view of the proposed G_m–C basic structure.

A. Input stage

The core structure of this design is a classic mirrored OTA (Fig. 3a) with a PMOS input differential pair degenerated with a fixed resistor R of 50 kΩ [12]. The input pair drain nodes are connected to the low impedance nodes A and B, as shown in Fig. 3b, of NMOS high swing cascode current mirrors.

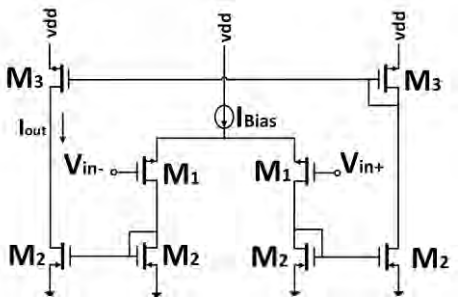
B. Copy factor tuning (CF-tuning)

The first programmable technique is introduced at the high swing NMOS cascode current mirrors stage made of transistors M2-$M2_C$ (Fig. 3b).

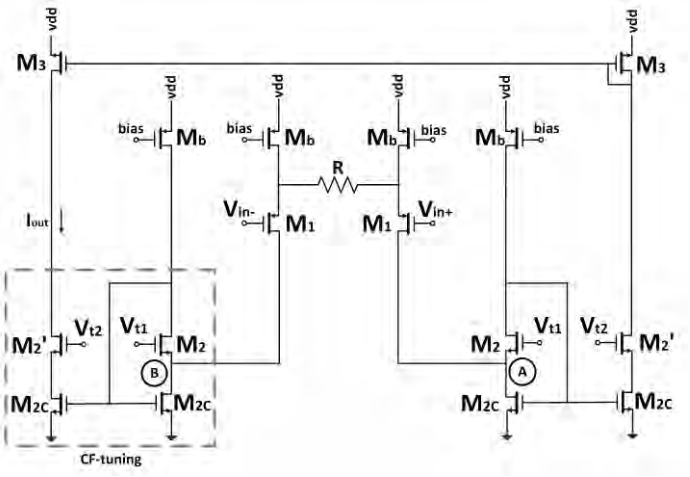
By controlling the cascode voltages V_{t1} and V_{t2}, it is possible to keep transistors $M2_C$ in triode region. Then, by setting $V_{t2} \leq V_{t1}$ the complementary currents generated at the input stage are copied through these current mirrors with an scaling ratio.

C. Current-Steering technique (CS-tuning)

The second proposed technique is based on a current steering approach introduced at the M3 output stage of the OTA. For that, a current-steering gain-tuneable M3–$M3_C$ PMOS high swing cascode current mirror, as shown in Fig. 4, substitutes the M3 PMOS current mirror from Fig. 3b.



a)



b)

Fig. 3. a) Classic Mirrored OTA; b) Modified input stage with CF-tuning.

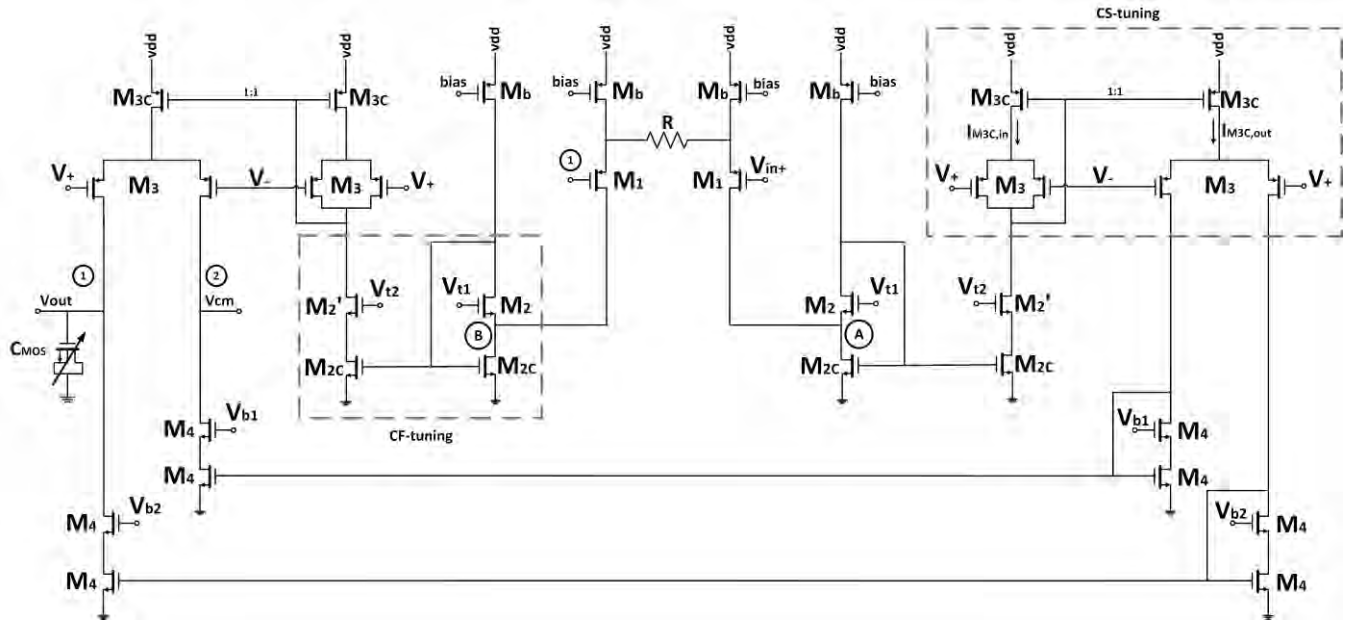


Fig. 4. Complete structure of the G_m-C proposal; in grey the tuning techniques applied.

The current copy of transistors $M3_C$ has a 1:1 ratio, and as both transistors of the current mirror have the same gate to source voltage, V_{gs}, and drain to source voltage, V_{ds}, the current mirror operates properly rendering unity gain current, $I_{M3c,out}=I_{M3c,in}(=I_{M3c})$.

Transistors M3 are split into two transistors–both at the output and input current mirror branches for symmetry– of equal size driven instead of by a constant V_C voltage, by complementary gate voltages $V_{\pm}=V_C\pm V_{gc}$ [13], resulting in two output branches, named 1 and 2. Thus, the output current is divided into two complementary currents $I_{out}=I_1+I_2$, with $I_1=(1-k)I_{M3c}$ and $I_2=kI_{M3c}$, being k a fractional value between 0 and 1 dependent on the differential control voltage V_{gc}. Output 1 is chosen as the output of the unity gain integrator while output 2 is set to V_{cm} for symmetry.

The complete schematic of the proposed structure is shown in Fig. 4, highlighted in grey the two techniques employed. Transistor sizes in (µm/µm) are M1=6/4, M2=2/4, M2'=4/4, $M2_C$=2/4, M3=3/4, $M3_C$=6/4, M4=0.5/4, Mb=6/4. Notice that M2' is two times M2 as the current through it is $2I_{M2}$. The voltage supply is 1.8 V, the common mode is set to 0.9 V and a 50 nA bias current is introduced through a 1:1 current mirror to Mb. Thus, the total power consumption is 1.08 µW.

III. Post-Layout Simulation Results

The G_m-C structure proposed in Fig. 4 has been designed in a 180 nm CMOS technology from TSMC. The total active area of the G_m–C structure is 0.0156 mm^2.

Voltage V_C=1.2 V; the tuning voltage V_{gc} can be varied from -100 mV to 170 mV while ensuring a maximum DC gain error below 0.5 dB. Voltages V_{t1} and V_{t2} are initially set to 0.6 V; then, V_{t2} can be varied from 0.6 V to 0.35 V.

Fig. 5 shows the different cutoff frequencies achieved over all the V_{gc} range with V_{t2} equal to 0.35 V, 0.4 V and 0.6 V, at both maximum (50 pF) and minimum (5 pF) load capacitance. The cutoff frequency, with C_L=50 pF, ranges from 220 mHz (V_{gc}=144 mV, V_{t2}=0.35 V) up to 3.72 kHz (V_{gc}=-100 mV, V_{t2}=0.6 V). This maximum cutoff frequency can be increased up to 39.1 kHz by reducing the load capacitance down to 5 pF.

From Fig. 5 a thick/fine-tuning relationship between both CS/CF-tuning techniques can be appreciated. Thick-tuning refers to the CS-technique: through the ~270 mV range of V_{gc} is possible to adjust the cutoff frequency of the filter to the order of magnitude of the target frequency. Thick-tuning as shown in Fig. 6, is provided by the CF-technique: with the ~250 mV range of V_{t2}, it is possible to tune the cutoff frequency over an order of magnitude, accurately adjusting the cutoff frequency through a smaller step (Hz/mV).

A clear visualization of this thick/thin relationship comes from the estimation of the step (Hz/mV) for each of the tunings. In Fig. 5 the f_c ranges from 3.72 kHz down to 0.69 Hz (V_{t2}=0.6 V, C_L=50 pF), for a V_{gc} range of ~270 mV, giving a ~13.8 Hz/mV step. The thin-tuning step, from Fig. 6, is 0.54 Hz/mV (V_{gc}=74 mV) and 0.01 Hz/mV (V_{gc}=144 mV).

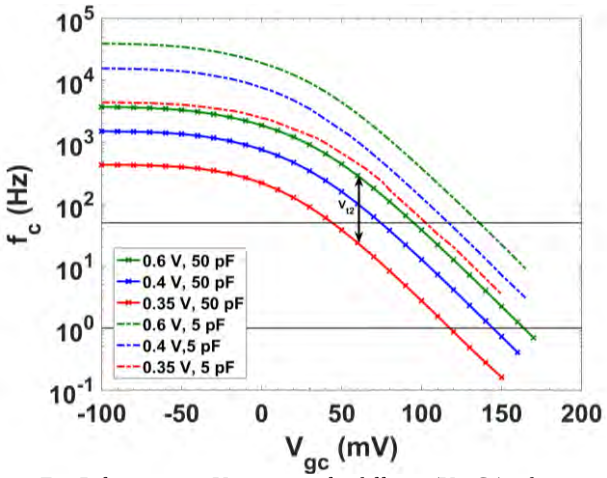


Fig. 5. f_c range over V_{gc} variation for different (V_{t2}, C_L) values.

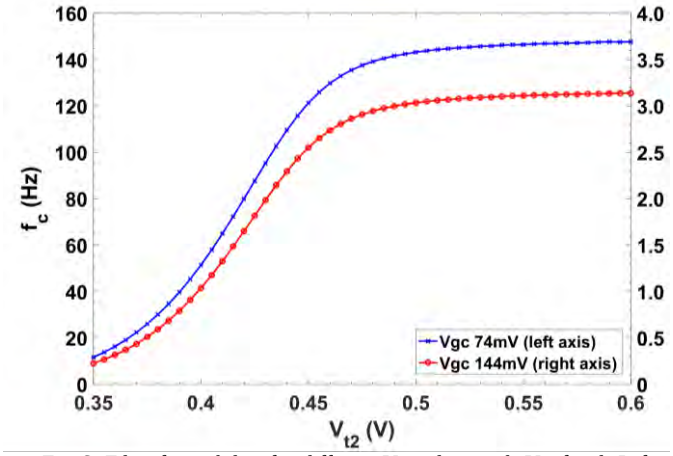


Fig. 6. Filter f_c tunability for different V_{t2} values with V_{gc} fixed. Left axis for V_{gc} 74 mV (blue), and right axis for V_{gc} 144 mV (red).

In order to characterize the proposed filter, we are going to focus on two different cutoff frequencies, 1 Hz and 50 Hz, with a C_L=50 pF. As the same f_c can be achieved through different combinations of (V_{t2}, V_{gc}), it has been characterized for both, V_{t2} maximum and minimum (0.6 V and 0.35 V). Table II shows post-layout simulation results for those two frequencies for the static input-output characteristic (ICMR), the total harmonic distortion (THD), integrated noise and dynamic range (DR).

The static input-output characteristic (ICMR) is shown in Fig. 7. Note that MOS capacitors require a minimum voltage to keep the capacitance, limiting the minimum output voltage to ≥0.45 V. While the total harmonic distortion (THD) is presented in Fig. 8, for both cutoff frequencies 1 Hz and 50 Hz. With an input signal of frequency $f_{in}=f_c/5$.

TABLE II. SIMULATION RESULTS COMPARISON FOR CUTOFF FREQUENCIES 1&50 HZ

f_c (Hz)	**1**		**50**	
(V_{gc}, V_{t2})	(118 mV, 0.35 V)	(164 mV, 0.6 V)	(45 mV, 0.35 V)	(96 mV, 0.6 V)
ICMR (V)	59.8 m–1.41	59.8 m–1.38	52.8 m–1.45	52.8 m–1.45
Linearity (V_{pp}) (THD≤1%)	0.706	0.559	1.24	0.642
Input noise (μV_{rms})	131	44.3	186	57.5
DR (dB)	65.6	73.0	67.4	71.9

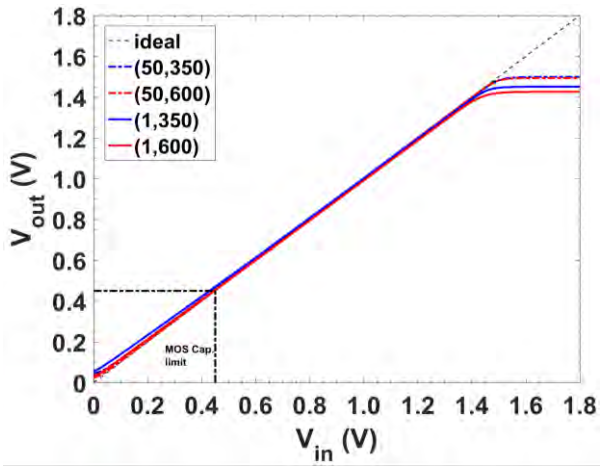


Fig. 7. V_{in}-V_{out} characteristic for different (f_c, V_{t2}) values.

To adjust de cutoff frequency, the methodology followed is: first approximate through V_{gc} (thick-tuning) with $V_{t2} \approx 0.4$ V. Then, V_{t2} (thin-tuning) is modified to improve the accuracy over the target frequency.

In order to optimize the performance, among the different possible combinations of (V_{gc}, V_{t2}) that provide the same f_c, those with the highest V_{t2} and lowest V_{gc} provide the best performance in terms of DR and input noise. This is because as V_{t2} increases and V_{gc} decreases, the OTA proposed (Fig. 4) becomes more symmetrical as the value of V_{t2} approaches V_{t1} and $V_{\pm}$ approaches V_c.

Thanks to the wide tunability of the system, it is possible to compensate any variation that may appear over the f_c due to PVT (Process, Voltage and Temperature) variations.

If the application requires it, the frequency ranges can be further extended with simple modifications to the circuit, such as C_L reduction to move up the cutoff frequency. The same can be achieved by an increase on the bias current. In addition, an increase on R would decrease the overall G_m at the expense of higher noise.

Finally, the main parameters are summarized in Table III. This work presents a wide tuneable cutoff frequency range, preserving low power and area consumption while higher dynamic range and ICMR are observed compared with previously reported works with similar cutoff frequencies.

IV. CONCLUSIONS

In this paper, a low pass filter with tuneable cutoff frequency that spans over several orders of magnitude and capable of achieving sub-Hz frequencies has been presented. Two tuning techniques implemented as thick/fine-tuning allows for an accurate selection of the cutoff frequency, while at the same time provides competitive performances in terms of area-power consumption, dynamic range and input–output DC characteristic. All of this makes the proposed filter highly suitable for portable on chip sensor interfaces based on impedance spectroscopy and biosignal front-end interfaces.

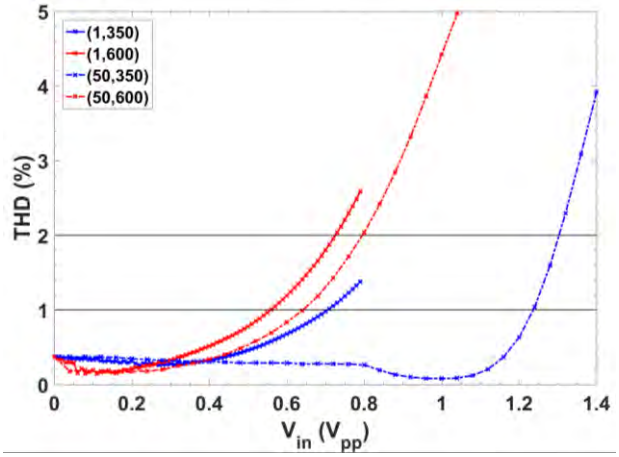


Fig. 8. THD vs input signal amplitude (peak-to-peak) for $f_{in}=f_c/5$ for different (f_c, V_{t2}) values.

TABLE III
G_M-C PERFORMANCE COMPARISON WITH SIMILAR WORKS

Parameter	**This work**	**[3]**	**[11]**	**[14]**	**[15]**
Results	Post-layout	Exp.	Exp.	Post-layout	Exp.
Technology (µm)	0.18	0.35	0.35	0.18	0.35
Order	1	4	1	2	2
V_{supply} (V)	1.8	0.6	1	1	1.8
I_{Bias} (nA)	50	1.5–4.5	0.2/1–4/20 [(d)]	0.25–25	14.9–182.3
I_{Total} (nA)	600	NA*	NA	NA	60–730
Power (µW)	1.08	0.0009-0.0027	0.005 [(e)]	0.009–0.9	0.1–1.31
Area (mm^2)	0.0156	0.168	0.07	0.0388	0.12
C_{Total} (pF)/pole	50	NA	40	78	NA
Tuneable	Thick/fine-tuning	I_{bias}	I_{bias}	I_{bias}	I_{bias}
f_c (Hz)	0.22–39.1k	101–272	0.002–90	0.73–76	2k–20k
ICMR (V)	0.06–1.38; 0.05–1.45 [(a)]	NA	0.4–0.55	NA	NA
Linearity (V_{pp}) THD@1%	0.706–0.559; 1.237–0.642 [(b)]	NA	0.14@f_c=f_{in}=1 Hz	0.54 @f_c=0.73 Hz	0.216; 0.294
Input noise (μV_{rms})	133–44.3; 186–57.3 [(b, c)]	46.6-46.8	32@f_c=1 Hz	177.4@f_c=0.73 Hz	86.3; 84.3
DR (dB)	65.5–73.0; 67.4–72.0 [(b)]	47	64	>64	58.9; 61.8

* NA= Not Available. [(a)] worst case for f_c=1&50 Hz; [(b)] V_{t2}=0.35&0.6 V for f_c=1&50 Hz; [(c)] integrated noise from 10 mHz to 10 kHz; [(d)] It has 2 different bias currents; [(e)] Power for nominal cutoff frequency without external clock and tuning.

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