ASIC Layout Design-Space Exploration of Pan-and-Tompkins Pre-Processing Algorithm for High Efficiency Electrocardiogram Monitor

ABSTRACT

— Cardiovascular diseases (CVDs) is the leading cause of the death globally. Ambulatory Electrocardiogram (ECG) and mobile monitoring is very important for early heart disease detection and prevention, but its measurement normally contains various types of noise which affect the analysis accuracy. Moreover, long hour ECG monitoring requires an efficient architecture to support real-time processing and low power consumption. This paper presents an application specific integrated circuit (ASIC) design of Pan-and-Tompkins ECG pre-processing algorithm which aims to remove several unwanted noise to increase analysis accuracy. The complete design flow covers high-level algorithm modelling in Matlab, followed by synthesizable design at Register Transfer Level (RTL) until logic synthesis, physical synthesis and static timing analysis to produce VLSI layout. Several power optimization techniques as well as different ASIC process technology libraries in terms of SilTerra's 180nm CMOS Logic Generic Library (CL180G) and Synopsys 32nm Generic Library (SAED32) are deployed for design-space exploration to study the design trade-off in terms of power consumption, timing performance, and the logic area usage. Results show that the clock gating technique is able to reduce 32.4% of dynamic power in design using CL180G generic library, whereas the integration of several power optimization techniques using SAED32 generic library is able to reduce 43.82% of dynamic power, 91.21% of leakage power and 91.25% of total power.