Multichannel time-to-digital converters with automatic calibration in Xilinx Zynq-7000 FPGA devices

Yu Wang, Wujun Xie, Haochang Chen, and David Day-Uei Li

***Abstract*—This paper proposes a weighted histogram calibration method and an automatic calibration architecture to implement high-linearity time-to-digital converters (TDCs) in low-cost ARM-based System-on-Chips (SoCs). The proposed method significantly reduces the nonlinearity introduced by nonuniform bins. It offers automatic calibration without manual interventions using ARM processors. Besides, our design is cost-effective in hardware consumption. We implemented and evaluated a 16-channel TDC system in a low-cost Zynq-7000 ARM-based SoC, in which the programable logic is equivalent to a 28 nm Artix-7 FPGA. The proposed TDC offers a resolution of 9.83 ps with good uniformity, achieving an averaged DNL_{pk-pk} of 0.38 LSB, and an averaged INL_{pk-pk} of 0.63 LSB.**

***Index Terms*—Time-to-digital converter (TDC), carry chains, field-programmable gate array (FPGA).**

I. Introduction

TIME resolved measurements are popular in many research fields, for example, light detection and ranging (LiDAR) for autonomous vehicles [1], [2], 3-D reconstruction [3], [4], surveying [5], enhanced Gigabit Ethernet [6], temperature sensing [7], quantum communications [8], [9], particle physics [10], space sciences [11], true random number generation [12], Raman spectroscopy [13], and medical physics such as positron emission tomography (PET) [14], optical reflectance spectroscopy [15], and fluorescence lifetime imaging microscopy (FLIM) [16], [17]. Time-to-digital converters (TDCs) are simply high-precision stopwatches, converting the time interval (TI) between two events into a digital code. They are gaining attention both in scientific instruments and industrial applications [18]–[21].

A growing research trend is to improve the TDC resolution (also called the least significant bit, LSB; it is the minimum measured TI). However, linearity and precision are also important parameters in TDC designs and determine the TDC system's accuracy. TDCs' nonlinearity can be characterized by differential nonlinearity (DNL) and integral nonlinearity (INL). They are defined as Eqs (1) and (2), where $W[k]$ is the k-th bin's bin-width, and Q is the averaged bin-width. DNL and INL can be evaluated by code density tests [22].

$$DNL[k] = \frac{(W[k]-Q)}{Q}, \quad (1)$$

$$INL[k] = \sum_{n=0}^{k} DNL[n], \quad (2)$$

The precision (σ) shows the repeatability of measurements and can be assessed by time interval tests:

$$\sigma^2 = \frac{1}{N-1}\sum_{i=1}^{N}(x_i - \mu), \quad (3)$$

where x_i is the i-th output's bin number and μ is the averaged value of N measurements.

TDCs can be realized in application-specific integrated circuits (ASICs) and field-programmable gate arrays (FPGAs). With recent advances in complementary metal-oxide-semiconductor (CMOS) technologies, both ASIC-TDCs and FPGA-TDCs can achieve picosecond resolutions. Compared with ASIC-TDCs, FPGA-TDCs are cheaper and have shorter developing cycles. However, due to large nonlinearity and the lack of automatic calibration methods, there are only a few commercial FPGA-TDCs [23]. On the contrary, ASIC-TDCs dominate commercial time-correlated single-photon counting products [24]–[26], as they show better linearity and precision due to the careful placement and routing strategies.

The tapped delay line (TDL) structure is the mainstream approach to build TDCs in FPGAs because cascaded carry-chain modules are common in modern FPGAs, for example, CARRY4 modules in Xilinx 6-series and 7-series FPGAs [27] and CARRY8 modules in UltraScale and other more advanced FPGAs [28]. The TDL-TDC's resolution is determined by the delay module's propagation delay, limited by CMOS processes. Wave union (WU) methods [29], multichain interpolation methods [30], vernier delay lines (VDLs) [31] and delay matrix structures [32] have been proposed to enhance the resolution.

However, due to clock skews and process variations, TDLs are uneven, resulting in large nonlinearity. Look-up table (LUT) based bin-by-bin calibration [33] methods can reduce the INL. Won and Lee proposed the tuned-TDL structure [34] to improve linearity by changing the output pattern of carry-chain

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modules and suggested a pattern 'SCSC' for Kintex-7 and Virtex-6 devices and 'SCSS' for the Spartan-6 devices. A block random access memory (BRAM) based mixed calibration method [35] improves TDCs' linearity by a two-step calibration, including bin compensation and width calibration. With the mixed calibration method, a 5.0 ps 96-channel TDC was proposed [35], achieving an averaged peak-to-peak DNL (DNL_{pk-pk}) = 0.27 LSB and peak-to-peak INL (INL_{pk-pk}) = 0.59 LSB, comparable with ASIC-TDCs. The BRAM-based structure is efficient and flexible. A 128-channel resolution-adjustable TDC for LiDAR applications was implemented [36] using BRAM-based mixed-binning methods. However, calibration coefficients stored in BRAMs are pre-calculated on PCs based on code density tests, making it time-consuming, especially for multichannel designs. Due to nonlinearity and time-consuming channel-by-channel or chip-by-chip calibration, FPGA-TDCs require proper calibration algorithms for broad commercial applications that force a trade-off between the number of channels and area occupancy [37], [38]. This work aims to tackle this problem.

The main contributions of this works are:

1) We proposed a single-step weighted histogram calibration method that can ease ultra-wide bin problems caused by bins whose width is less than 5 LSB, which is more efficient than the previously reported mixed calibration method [35].
2) We proposed an automatic calibration (AC) architecture using ARM-based System-on-Chips (SoCs), without manual calibration.
3) We implemented and tested a 16-channel AC-WU TDC in an ARM-based SoC device: the Xilinx Zynq-7000 SoC (Xilinx XC7Z020).

II. Architecture and Design

The TDL architecture is the backbone for the proposed TDC, implemented with CARRY4s in a low-cost Xilinx Zynq-7000 SoC (XC7Z020, ZedBoard development board). Fig. 1a is the system architecture of the proposed TDC. The whole system is composed of a programmable logic (PL, equivalent to Artix 7 FPGA) and a processing system (PS, dual-core ARM Cortex-9 inside) [39]. PL is for implementing TDCs, including TDLs, encoders, and calibration modules. Histogramming modules were also implemented in PL to correct biased timestamps caused by background noise and device jitter [36]. PS is for calculating calibration coefficients. The channel selector in PL is for multichannel applications, transferring data between the TDC channels and the ARM core. The advanced eXtensible interface (AXI) is the data bus for communications between PL and PS [40].

To further improve TDC's performance, techniques, like WU methods [29], sub-TDL structures [35] and tuned TDL methods [34], were also applied in our study.

A. Wave Union Method and Sub-TDL Architecture

The concept of the WU method is shown in Fig. 1b. When a hit signal arrives at the TDC's input port, a look-up table (LUT)-based WU launcher generates a rising and a falling transitions separately. These two transitions (0-1 and 1-0) propagate along the TDL, and the TDL's outputs are sampled by D-type flip-flops (DFFs) simultaneously in every tap. With two transitions, the TDC conducts two measurements for the same TI in one clock period, and the WU TDC's resolution can be defined as [41]:

$$LSB_{WU} = \frac{T}{N_r + N_f} = \frac{LSB_r \times LSB_f}{LSB_r + LSB_f}, \quad (4)$$

where T is the period of the sampling clock, N_r and N_f are bin numbers of the plain TDC with a rising transition and a falling transition, respectively. Several studies indicate that WU is efficient in enhancing the resolution, but it also exacerbates bubble problems (unexpected transitions of logic states, for example, unexpected zeros among a series of ones), causing encoding failures [29], [42], [43]. Moreover, although the bin realignment method can remove bubbles when only one transition exits in the TDL [44], it is difficult to achieve the same result in WU TDCs due to the speed difference between rising and falling transitions [41].

The sub-TDL [35] method (or the decomposition method [45]) can remove bubbles. Mismatches and large clock skews lead to bubble errors [45], [46]. A study [47] reports that the largest clock skew within a clock region is around 19 ps in Xilinx Kintex-7 FPGAs. However, the typical delay time between two neighboring delay cells (see Fig. 1c, highlighted in yellow) in 7-series FPGAs is around 10 – 15 ps [48], [49]. Furthermore, the sub-TDL structure elongates time intervals between taps by decomposing sampling taps. For example, in our design, the interval highlighted in blue is four times longer than the interval highlighted in yellow (see Fig. 1c). Therefore, the sub-TDL structure can minimize the impact of clock skews and mismatches and remove bubbles. Meanwhile, interpolations with four sub-TDLs maintain the TDC's resolution. Therefore, the sub-TDL structure can remove bubbles efficiently without trading off the resolution.

B. CARRY4 and Tuned-TDL Architecture

As shown in Fig. 1c, the TDL is constructed with cascaded CARRY4s, and each CARRY4 contains four cascaded delay elements. Each delay element has two direct outputs named *C* and *S* ports, respectively, and neighboring delay elements are connected through internal routing resources [50]. In [34], Won and Lee reported that TDCs' linearity could be improved by changing output patterns. To find the best sampling pattern for Zynq-7000 SoC, we conducted similar experiments. The results are summarized in Table I, indicating that the pattern "SCSC" performs the best linearity in Zynq-7000 SoCs.

Table I.
SAMPLING PATTERNS COMPARISON

Pattern (LSB = 9.83 LSB)	DNL (LSB)	INL (LSB)
CCCC	[-0.99, 4.32], 5.32	[-5.44, 4.17], 9.61
SSSS	[-0.91, 3.26], 4.17	[-5.32, 4.71], 10.03
CSCC	[-0.98, 3.25], 4.23	[-5.29, 5.19], 10.48
CSCS	[-0.95, 5.07], 6.02	[-7.40, 5.28], 12.68
SCSS	[-0.97, 3.26], 4.24	[-7.18, 5.27], 12.45
SCSC	**[-0.89, 2.94], 3.84**	**[-5.73, 4.96], 10.69**

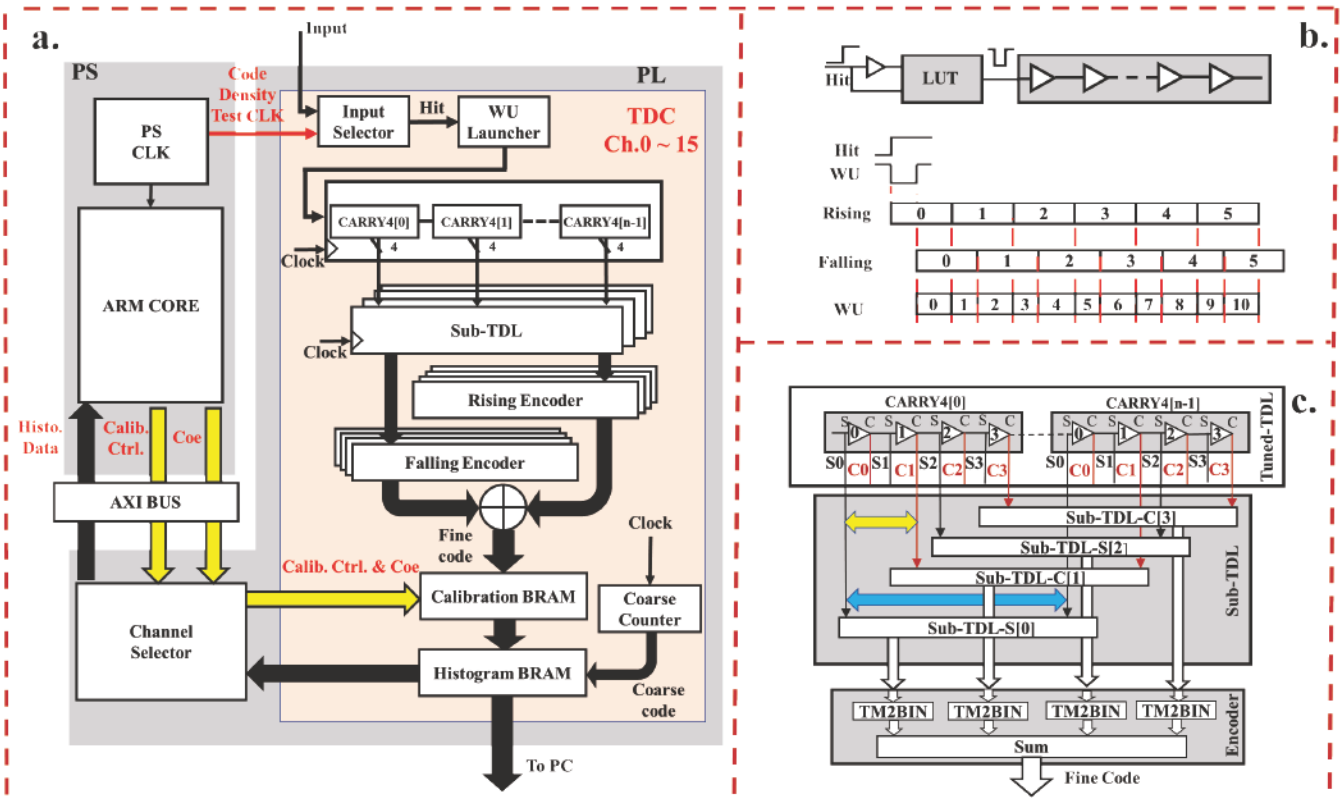

Fig. 1 (a) The block diagram of the proposed TDC system. (b) The concept of the WU method. (c) The block diagram of the tuned-TDL architecture and sub-TDL architecture.

C. Weighted Histogram Calibration Method

Although the tunned-TDL method can improve linearity, ultra-wide and ultra-narrow bins still exist and contribute to nonlinearity. To ease ultra-wide bin problems, Chen and Li proposed the mixed calibration method [35] to achieve excellent linearity, comparable with ASIC-TDCs. The mixed calibration method contains two steps: bin compensation and width calibration. Code density tests are required for each step to calculate correction factors. In the bin compensation, small bins are compensated by large bins by address factors (BCF_m and BCF_c) (see Fig. 2a). The width calibration performs like the bin-by-bin calibration [33] and further enhances linearity. However, the mixed calibration method cannot ease ultra-wide bin problems caused by bins with a bin width > 2 LSB. When dealing with ultra-wide bins (e.g., Bin [n] highlighted in blue in Fig. 2a), the mixed calibration method introduces missing codes, like Bin [M+1] highlighted in red in Fig. 2a, and degrades the resolution. Moreover, the two-step mixed calibration method is unsuitable for automatic calibration. Therefore, we propose a new calibration method, the single-step weighted histogram calibration method. Unlike the mixed calibration method, the proposed method (Fig. 2b) can ease ultra-wide bin problems, detailed below.

Figure 3 shows the hardware implementation of the proposed weighted histogram calibration method. To achieve the histogramming function, the adders in Fig. 3 perform like accumulations. Like the mixed calibration method, the proposed method contains two parts (the bin compensation and width calibration). In the proposed method, three pairs of address factors (*Addr L*, *Addr M*, and *Addr R*) and width factors (*Coe L*, *Coe M*, and *Coe R*) are stored in a calibration BRAM module, and the results are stored in three Histogram BRAM modules. There are three possible cases for bin compensation in the proposed calibration method, as shown in Figs 4a-c:

Case A: $W[k] \leq 1$ LSB,

Case B: 1 LSB $< W[k] \leq 2$ LSB,

Case C: 2 LSB $< W[k] \leq 3$ LSB.

$W[k]$ is the bin width of the k-th actual bin. Figure 5 shows the pseudo-codes for calculating address factors. Ideally, with three pairs of factors, the proposed method can ease ultra-wide bin problems caused by bins whose width is less than 5 LSB. Figure 2b is an example of this scenario: Bin [n] is the ultra-wide bin ($W[n] \leq 5$ LSB) neighbored by two wide bins, Bin [n-1] and Bin [n+1]. Bin [n] can be only remapped to three ideal bins (Bin [M-1], Bin [M], and Bin [M+1]). However, with the factors *Addr R* [n-1] and *Addr L* [n+1], the ideal bins (Bin [M-2] and Bin [M+2]) are fulfilled by the actual bins (Bin [n-1] and Bin [n+1]). Therefore, the ultra-wide bin problem caused by Bin [n] ($W[n] \leq 5$ LSB) can be eased with the proposed method, which is more efficient than the mixed calibration method in [35].

Calculations for width factors follow similar rules shown in Fig. 4. In Case A, only *Coe L* is valid and can be expressed as:

$$Coe\ L[k] = \frac{Width[k,n]}{W[k]}, \tag{5}$$

where $Width[k,n]$ is a portion of Bin [k] in the actual TDL which should be in Bin [n] in the ideal TDL (highlighted in red in Fig. 4a).

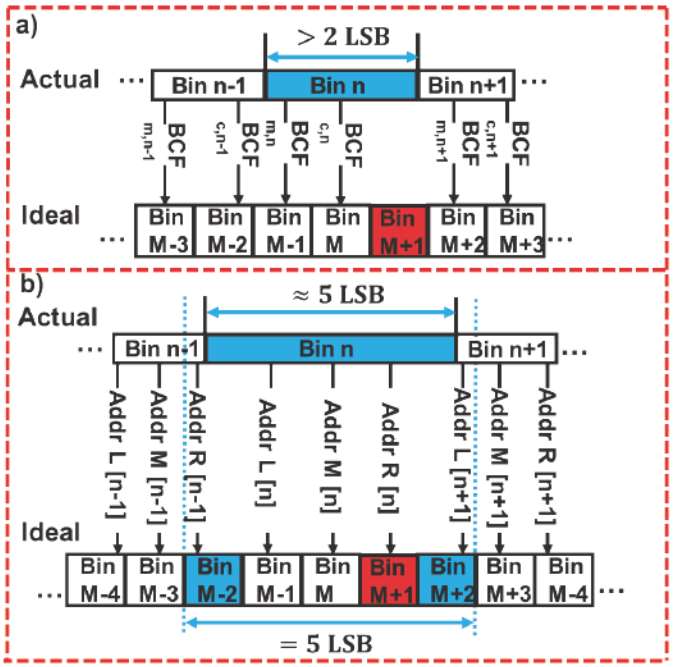

Fig. 2. Examples of bin compensation in a) the mixed calibration method [35] and b) the proposed weighted histogram calibration method.

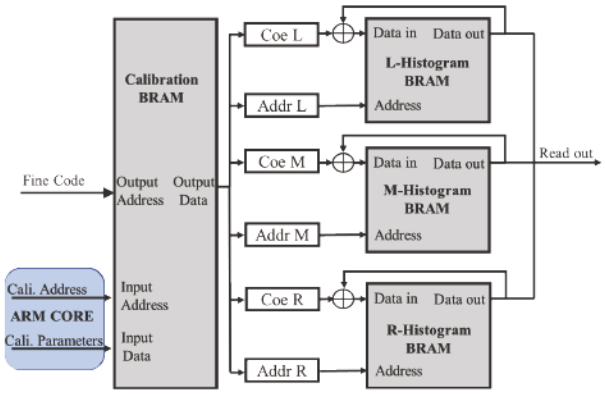

Fig. 3. Hardware implementation of weighted histogram calibration.

In Case B, Bin [k] is remapped to two ideal bins (see Fig. 4b). Therefore, *Coe L and Coe M* can be defined as:

$$Coe\ L[k] = \frac{Width[k,n-1]}{W[k]}, \tag{6}$$

$$Coe\ M[k] = \frac{Width[k,n]}{W[k]}, \tag{7}$$

In Case C, all width factors are valid and can be calculated as:

$$Coe\ L[k] = \frac{Width[k,n-1]}{W[k]}, \tag{8}$$

$$Coe\ M[k] = \frac{Width[k,n]}{W[k]}, \tag{9}$$

$$Coe\ R\ [k] = \frac{Width[k,n+1]}{W[k]}. \tag{10}$$

Compared with the mixed calibration method in [35], which needs two-round code density tests, the proposed weighted histogram calibration method can calculate both address factors and width factors in a single round (see the difference between Fig. 6a and Fig. 6b, highlighted in yellow), which is more suitable for automatic calibration.

D. Automatic Calibration

The proposed AC function is based on Zynq SoC architectures. The workflow of the proposed function is shown in Fig. 6c and can be divided into two parts: the initial and the measurement stages. After powering up the board, the ARM core in PS calculates calibration factors and loads them to BRAMs in PL in the initial stage. In the measurement stage, indexed by raw data, the calibrated results will be delivered from the calibration module and stored in the histogramming module. Through this procedure, real-time and automatic calibration can be achieved with the ARM core and BRAM modules.

The system is free from manual or offline calibrations with the proposed automatic calibration function, suitable for broader commercial multichannel FPGA-TDC applications.

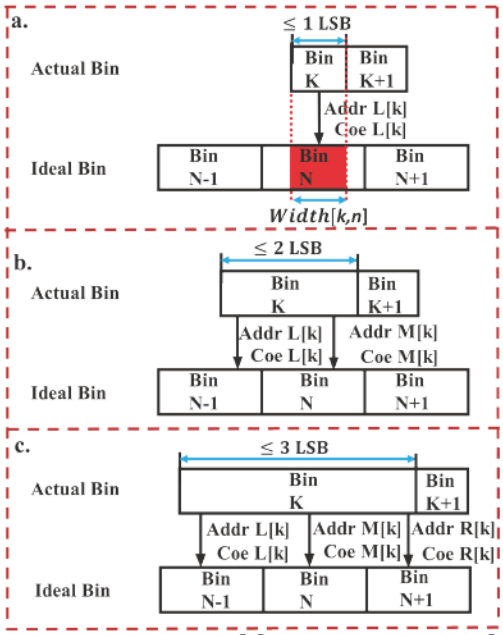

Fig. 4. Bin compensation when a) $W[k] \leq 1$ LSB, b) 1 LSB < $W[k] \leq 2$ LSB, and c) 2 LSB < $W[k] \leq 3$ LSB.

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Set T_act[k] = ∑_{n=1}^{k} W[n];
Set T_ideal[k] = ∑_{n=1}^{k} Q
if ((T_ideal[k-1]<=T_act [k])&&(T_act[k]<T_ideal[k]))
      /***** W[k] ≤ 1 LSB *****/
      if(T_act [k-1]>=T_ideal[k-1])
            Addr_L[k]=k;
      /***** 1 LSB < W[k] ≤ 2 LSB *****/
      else if((T_act [k-1]>=T_ideal[k-2])&&(T_act [k-1]<T_ideal[k-1]))
            Addr_L[k]=k-1;
            Addr_M[k]=k;
      /***** 2 LSB < W[k] ≤ 3 LSB *****/
      else if((T_act [k-1]>=T_ideal[k-3])&&(T_act [k-1]<T_ideal[k-2]))
            Addr_L[k]=k-2;
            Addr_M[k]=k-1;
            Addr_R[k]=k;
.....
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Fig. 5. The pseudo-codes for address factor calculations.

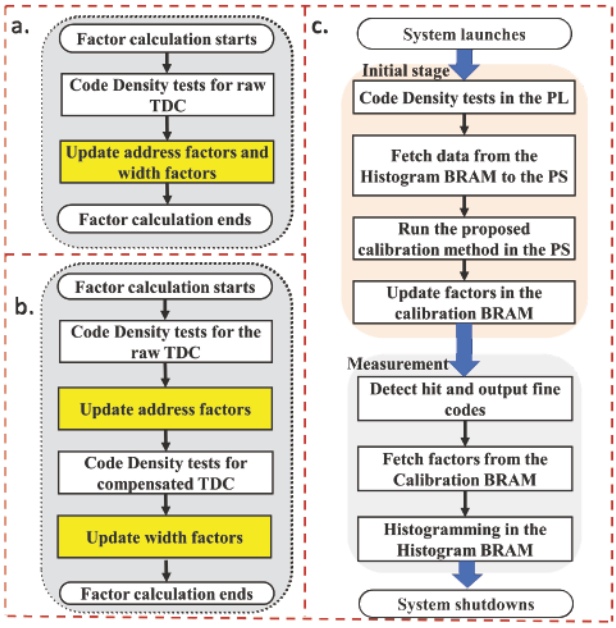

Fig. 6. Flow diagrams of (a) the proposed weighted histogram calibration method, (b) the mixed calibration method in [35]. (c) the workflow of AC TDCs.

III. Experimental Results

We conducted experiments to evaluate the AC-WU TDC. Two asynchronous clocks from independent low-jitter crystal oscillators (Fox-767) were used as the system clock and the random input for code density tests. The temperature and the operation voltage were maintained in the experiment.

A. Linearity and Bin Width Distribution

The TDC's linearity is mainly evaluated by DNL, INL and their standard deviations (σ_{DNL} and σ_{INL}). Besides, the equivalent bin-width ω_{eq} and its standard deviation σ_{eq} were also proposed to evaluate TDC's linearity [51]. They are defined as:

$$\sigma_{eq}^2 = \sum_{i=1}^{N} \left(\frac{W[i]^2}{12} \times \frac{W[i]}{W_{total}} \right), \tag{11}$$

where

$$W_{total} = \sum_{i=1}^{N} W[i], \tag{12}$$

and

$$\omega_{eq} = \sigma_{eq}\sqrt{12} = \sqrt{\sum_{i=1}^{n} \left(\frac{W[i]^3}{W_{total}} \right)}. \tag{13}$$

The AC-WU TDC's DNL and INL are improved significantly compared with the uncalibrated TDC. The experimental results are summarized and shown in Table II and Fig. 7. After the calibration, DNL_{pk-pk} and INL_{pk-pk} are improved by 13-fold (from 3.91 LSB to 0.30 LSB) and 18-fold (from 12.05 LSB to 0.67 LSB), respectively. σ_{DNL} is enhanced by 21-fold (from 0.86 LSB to 0.04 LSB), and σ_{INL} is enhanced by 21-fold (from 2.79 LSB to 0.13 LSB). Besides, ω_{eq} and σ_{eq} are improved from 19.76 ps to 9.85 ps and from 5.70 ps to 2.84 ps, respectively. Meanwhile, the AC-WU TDC's bin-width distribution is shown in Fig. 8a. The calibrated TDC shows a much more concentrated bin-width distribution than the uncalibrated TDC, as shown in Fig. 8b.

B. Time Interval Tests

The standard deviation of repeated measurements can evaluate the proposed TDC's RMS resolution. The built-in programmable delay modules, IDELAYE2 and IDELAYCTRL, can generate a controllable delay between the sampling clock and the hit signal [52]. Benefiting from the delayed signal generated inside the FPGA device, external measurement errors and jitters are minimized. As shown in Fig. 9a, we conducted 30 measurements covering one sampling clock, and each measurement captures 100 000 samples. The standard deviations of each measurement were calculated, and the average value (13.86 ps) is the TDC's RMS resolution. Meanwhile, the measured histogram of a 980 ps time interval is shown in Fig. 9b, achieving 14.16 ps RMS resolution.

TABLE II
LINEARITY COMPARISON BETWEEN THE UNCALIBRATED TDC AND CALIBRATED TDC

	Tuned & Sub-WU	AC-WU
LSB (ps)	9.83	
DNL (LSB)	[-0.93,2.98]	**[-0.14,0.16]**
DNL_{pk-pk}(LSB)	3.91	**0.30**
σ_{DNL} (LSB)	0.86	**0.04**
INL (LSB)	[-6.52,5.53]	**[-0.25,0.42]**
INL_{pk-pk} (LSB)	12.05	**0.67**
σ_{INL} (LSB)	2.79	**0.13**
ω_{eq} (ps)	19.76	**9.85**
σ_{eq} (ps)	5.70	**2.84**

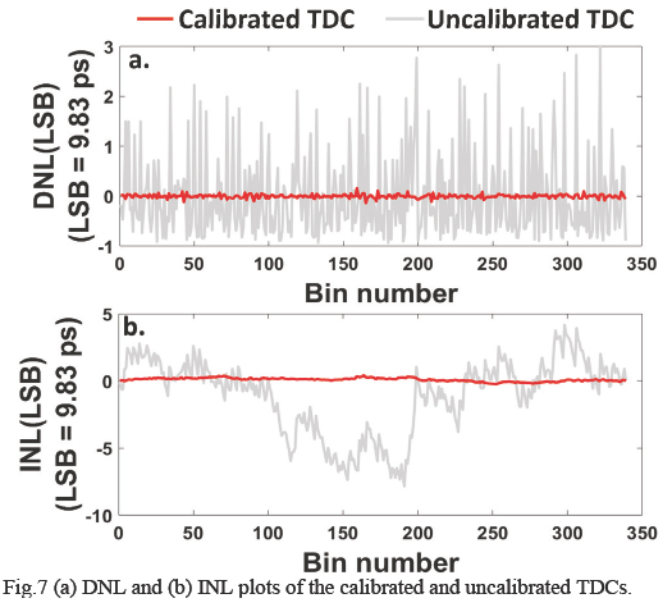

Fig.7 (a) DNL and (b) INL plots of the calibrated and uncalibrated TDCs.

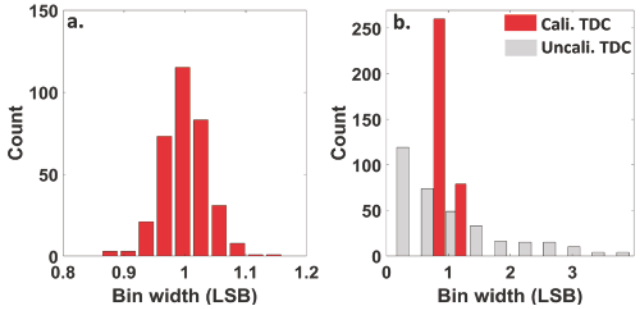

Fig. 8. Distribution of (a) calibrated bin-widths and (b) uncalibrated bin-widths. LSB = 9.83 ps.

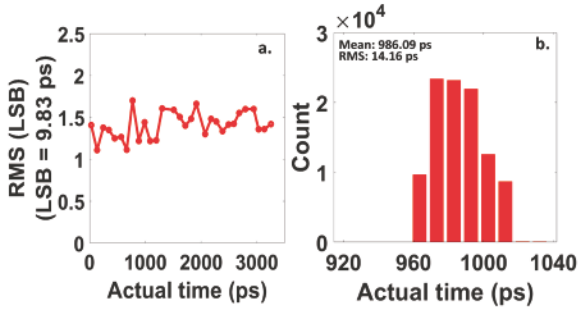

Fig. 9 (a) Time interval measurement results and (b) Time interval histogram at the time interval about 980 ps.

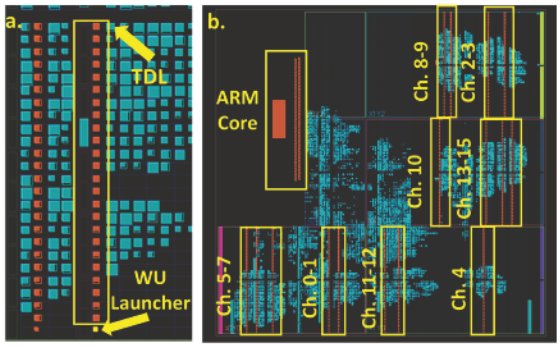

Fig. 10. Implementation layouts of (a) a single channel and (b) 16 channels.

Table III
Logic Resources Utilization

	CARRY4	LUTs	DFFs	BRAM
Available	13300	53200	106400	140
Single-channel	**50** (0.38%)	**764** (1.44%)	**1095** (1.02%)	**2** (1.42%)
16-channel	**800** (6.02%)	**9681** (18.19%)	**15141** (14.23%)	**32** (22.85%)
AXI Bus	**0**	**797** (1.49%)	**1278** (1.20%)	**0**

C. *Multichannel Implementation and Logic Resources Consumption*

We have implemented and tested a 16-channel AC-WU TDC in Zynq-7000 SoCs. To avoid significant clock skews, each TDL (containing 50 CARRY4s) is placed within a clock region. Every WU launcher is constrained near the corresponding TDL's first CARRY4 to minimize jitters introduced by routing resources (see Fig. 10a). To show the efficiency of the proposed weighted histogram calibration method, 16 channels are distributed in the tested chip randomly (see Fig. 10b).

Table III summarizes the resource consumption for the 16-channel design. Each channel costs 764 LUTs, 1095 DFFs, and 2 BRAMs. The usage report shows the proposed TDC architecture has great potential in multichannel applications. Moreover, the AXI bus is for communications between PL and PS with the cost of 1278 DFFs and 797 LUTs.

Code density tests were conducted for all channels. The linearity performances for 16 channels are concluded in Table IV, showing that the proposed 16-channel TDC has good uniformity.

IV. Comparison and Discussions

Table V compares our proposed calibration method with other published calibration methods. Table VI summarizes recently published FPGA-TDCs and the proposed TDC.

Although calibration methods like bin-by-bin calibration [33], bin-width calibration [53], and mixed calibration [35] methods can improve linearity and precision, these methods require manual calibration, which is unsuitable for commercial products. The gain and error calibration [54] can correct data automatically, using signal processing methods (efficient but complex). However, this method [54] requires two signal interpolators and consumes more resources per channel than our solution (see Table VI).

Unlike ultra-high resolution (< 5 ps) TDCs [41], [47], [54]–[57], the AC-WU TDC aims to achieve a high resolution and linearity simultaneously in low-cost SoC devices. Compared with previously reported TDCs with similar resolutions, the proposed TDCs are easy to implement in modern SoC devices and have better linearity. Compared with the PLL delay matrix TDC proposed in [58], our TDC has similar linearity performances. However, the PLL delay matrix TDC requires 6-fold more LUTs than our TDC with the AXI bus. Meanwhile, easy implementation is essential for broader applications. In this aspect, our design shows advantages compared with the two-stage delay line loop shrinking TDC [59] and the bidirectional RO Vernier TDC [60] because modern FPGAs do not have dedicated logic resources to construct loop architectures.

The proposed work allows researchers to produce repeatable measurements using established ARM-based ZYNQ devices easily. The proposed approach can also be implemented with open-source softcore processors for low-cost commercial developments. However, compared with the proposed TDC, the resources consumption of a softcore processor in FPGAs is close to or even higher than a single-channel design. They cost at least thousands of LUTs and DFFs [61], [62]. The Rocket Chip Generator [63], a dedicated open-source core, and its variation *S-RISC-V* [64] consume more than 30K LUTs and 15K DFFs. Resource optimization in softcore processors is complex and requires expertise in implementing control buses and data buses and developing arithmetic logical units (ALUs).

Generally, benefiting from automatic calibration with ARM-core processors, our design does not require manual calibration like the direct histogram TDC [53] and the mixed calibration TDC [35]. This advantage widens the AC-WU TDC's applications.

Table IV
Summary of Linearity Performances of 16-Channel TDCs (Units: LSB)

Channel	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	Ave.
DNL_{pk-pk}	0.21	0.34	0.33	0.28	0.30	0.29	0.56	0.69	0.25	0.41	0.25	0.26	0.52	0.27	0.48	0.60	0.38
σ_{DNL}	0.03	0.05	0.05	0.04	0.04	0.04	0.10	0.07	0.04	0.06	0.03	0.04	0.07	0.03	0.06	0.07	0.05
INL_{pk-pk}	0.52	0.55	0.51	0.52	0.67	0.45	0.90	0.86	0.51	0.45	0.57	0.37	0.87	0.62	0.89	0.87	0.63
σ_{INL}	0.10	0.11	0.10	0.12	0.13	0.08	0.17	0.18	0.09	0.08	0.11	0.08	0.19	0.14	0.23	0.26	0.14

V. CONCLUSION

We developed a multichannel auto-calibration architecture and a weighted histogram method for the first time. Besides, we combined the WU method, the tuned-TDL method and the sub-TDL method to implement high linearity, high resolution and multichannel TDCs in a low-cost ARM-based SoC device. The advantages are as follows.

1) Sometimes calibration methods require off-line or manual calibration (channel-by-channel or chip-by-chip). The proposed automatic calibration architecture resolves this problem by using ARM processors inside ARM-based SoC devices. The proposed TDC is more suitable for commercial products.
2) Traditional histogram-based calibration methods [35] need two steps to conduct address remapping and width calibration. We performed these two steps simultaneously for the proposed weighted histogram calibration method by analyzing relative positions between ideal and actual bins. Besides, the proposed method can ease ultra-wide bin problems caused by bins whose width is less than 5 LSB with only an extra BRAM module, compared with the mixed calibration method [35], which can only deal with 2 LSB ultra-wide bins.

Combining the WU method, the tuned-TDL method and the sub-TDL method, a novel TDC was proposed and evaluated. The bin size (LSB) achieves 9.83 ps, and DNL_{pk-pk} and INL_{pk-pk} are enhanced to 0.38 LSB and 0.63 LSB, respectively, in a low-cost Zynq-7000 ARM-based SoC. A 16-channel TDC system was also implemented and tested. The tests results show good uniformity between channels.

Table V
Comparison of published calibration methods

Ref.-Year	Methods	Multiple steps	Auto/manual Calibration
[33]-10	Bin-by-bin calibration	Single-step	Manual
[53]-17	Bin-width calibration	Single-step	Manual
[35]-19	Mixed calibration	Two-step	Manual
[54]-21	Gain & error calibration	Single-step	Auto
This work	Weighted histogram calibration with an AC function	Single-step	Auto

Table VI
Comparison of Recently Published FPGA-TDCs

Ref-Year	Methods	Device Process (nm)	LSB (ps)	ω_{eq} (ps)	RMS Resol. (ps)	DNL (LSB)	INL (LSB)	LUT	DFF	BRAM	AXI Bus
[34]-16	Tuned-TDL	28	10.6	N/S [1]	8.13	[-1.00, 1.45]	[-1.23, 4.30]	577	1641	0	-
		40	10.1	N/S [1]	9.82	[-1.00, 1.18]	[-3.03, 2.46]	577	1641	0	-
		45	16.7	N/S [1]	12.75	[-1.00, 1.22]	[-0.70, 2.56]	261	787	0	-
[56]-16	Dual-sampling, Bin Realignment, Bin Decimation	20	3.29	N/S [1]	2.97	[-1.00, 3.95] [2]	[-1.50, 1.95] [2]	664	1652	0	-
[55]-17	Multichain Ave.	28	1.15	N/S [1]	3.50	[-0.98, 3.50]	[-5.90, 3.10]	15255 [3]	N/S [1]	43 [3]	-
[53]-17	Tuned-TDL, Direct Histogram Bin-width Cali.	28	10.50	10.55	4.42	[-0.04, 0.04]	[-0.09, 0.04]	N/S [1]	N/S [1]	0	-
[59]-18	Two-Stage Delay Line Loop Shrinking	130	8.50	N/S [1]	42.40	[-0.22, 0.36]	[-0.62, 0.91]	N/S [1]	N/S [1]	0	-
[35]-19	Tuned-TDL, Sub-TDL, Mixed Calibration	28	10.54	10.55	14.59	[-0.05, 0.08]	[-0.09, 0.11]	1145	1916	1.5	-
		20	5.02	5.03	7.80	[-0.12, 0.11]	[-0.18, 0.46]	703	1195	1.5	-
[60]-20	Bidirectional RO Vernier	65	24.50	N/S [1]	28.00	[-0.20, 0.25]	[0.03, 0.82]	172	986	0	-
[58]-20	PLL Delay Matrix with DDR	40	15.60	N/S [1]	15.60	[-0.18, 0.18] [4]	[-0.16, 0.14] [4]	9886 [5]	N/S [1]	0	-
[47]-20	$PSDL_{10}$	28	1.11	1.71	<5.30	[-0.98, 3.73]	[-17.47, 38.56]	200	2000	0	-
	$10\times TCL_{chopped}$	28	1.01	1.39	<4.50	[-0.98, 2.73]	[-17.83, 5.06]	2000	2000	0	-
[54]-21	Slide Scale, Gain & Error cal., Moving Ave.	28	4.88	N/S [1]	2.90~8.03	[-0.10, 0.15]	[-0.23, 0.28]	2962	4157	0	-
[57]-21	Large Scale Parallel Routing	40	5.50	N/S [1]	N/S [1]	[-0.84, 1.67]	[-3.48, 3.33]	414	1090	0	-
		28	1.29	N/S [1]	N/S [1]	[-1.20, 1.40]	[-3.28, 3.78]	1002	3900	0	-
		20	3.95	N/S [1]	N/S [1]	[-2.75, 3.00]	[-5.75, 6.00]	334	1100	0	-
[41]-21	Sub-TDL, DS, WU-A, Binning	20	2.48	2.95	3.63	[-0.93, 1.68]	[-1.78, 2.67]	2460	3463	7.5	-
This Work	**WU-A, Tuned-TDL, Sub-TDL, Auto Cal.**	**28**	**9.83**	**9.85**	**13.86** [6]	**[-0.14, 0.16], 0.38** [7]	**[-0.25, 0.42], 0.63** [7]	**764**	**1095**	**2**	**1278 DFFs 797 LUTs**

[1] N/S= not specified; [2] Approximate values from figures presented in literature; [3] Calculated values from data presented in literature; [4] Rounding values from data presented in literature; [5] Combinational ALUTs in Altera FPGA; [6] The RMS resolution is measured internally. [7] Averaged peak-peak DNL or INL results of the Multichannel TDCs.

Previously published FPGA-TDCs were implemented in ARM-free FPGAs instead of ARM-based SoCs. The proposed architecture shows that ARM-based solutions can offer online automatic calibration over traditional FPGA devices, promising broader applications in LiDAR, PET-CT or Raman spectroscopy.

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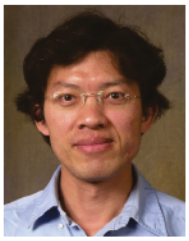

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