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Modeling and analyzing parasitic parameters in high frequency converters

Mohamad Saleh Sanjari Nia

Department: Electrical and Computer Engineering

MODELING AND ANALYZING PARASITIC PARAMETERS IN HIGH FREQUENCY CONVERTERS

by

MOHAMAD SALEH SANJARI NIA

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Approved by:

Dr. Pourya Shamsi, Advisor
Dr. Mehdi Ferdowsi
Dr. Jonathan W. Kimball
Dr. Rui Bo
Dr. Ali Rownaghi

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ABSTRACT

This research focuses on electromagnetic interference (EMI) / electromagnetic compatibility (EMC) design and analysis in power electronics systems. To limit the EMI under the standards, different methods and strategies are investigated. Parasitic parameters of high frequency (HF) transformer are analyzed using a novel analytical method, finite element method (FEM), and experimental measurements for different structures and windings arrangements. Also, the magnetic field, electric field, electric displacement, and electric potential distribution are simulated and analyzed. Moreover, a high voltage system is considered and analyzed to improve the EMC. The EMI propagation paths are analyzed. The EMI noise level of the system is obtained and compared to the IEC61800-3 standard. To improve the EMC, the parasitic parameters of the transformer, as the main path of EMI circulation, are analyzed and optimized to block the propagation. Furthermore, the geometry structure of the HF transformer is optimized to lower the parasitics in the system. Three pareto-optimal techniques are investigated for the optimization. The models and results are verified by 3D-FEM and experimental results for several given scenarios. Furthermore, the EMC modeling and conducted EMI analysis are developed for a system including an AC-DC-DC power supply (rectifier and dual active bridge (DAB) converter). Moreover, the common mode (CM) EMI noise propagation through the system is discussed and the noise sources and effect of components on the noise are analyzed. Additionally, the CM impedance of different parts of the system and the noise levels are discussed. Finally, EMI attenuation techniques were applied to the system.

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TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

PAPER I Page

PAPER II

LIST OF TABLES

1. INTRODUCTION

Performance, efficiency, power density, and commercialization of power electronics converters are highly dependent on the EMI noise level in the systems. Based on the national and international standards and regulations, the EMI noise in the power electronics systems should meet certain level of limitations to pass the standard procedure and perform properly in the electric systems.

The traditional way of EMI mitigation in power electronics converters is using EMI filters between the supply and the converter. However, using the EMI filters not only reduce the efficiency and power density, but also can add stability complexity to the control units of the converters. As the efficiency and power density of the power electronics are attracting more attention from the industry and academia, finding new and optimized solutions for meeting the standard regulations and EMI mitigation in the systems are necessary. Moreover, the market demand of the power electronics is increasing rapidly due to transitioning to the green technologies and electric transportation. It is anticipated that by 2030 the electric transportation will be less expensive than the fossil fuel transportation and the number of sold vehicles will reach up to 30 percent of the whole vehicles in the world [1]. From the electric system point of view, this rapid increase adds more complexity to the systems. Therefore, the power electronics converters can affect the other systems and/or affected by the other systems and interrupt the performance.

Advent of wide band gap switch technologies has led to more challenges in the EMI noise level of the systems. Silicon carbide (SiC) and gallium nitride (GaN) switches are becoming more common in power electronics converters. In spite of higher price compared

to silicon MOSFET and IGBT switches, these types of switches show a promising future [2]. The power density in the converters using wide band gaps enhance significantly. Moreover, the switching loss and the overall efficiency of the system improve significantly as well. Power density and higher efficiency is specifically important in power electronics converters of the electric vehicles. As an example, in the on-board chargers (OBC) of the electric vehicles, the power factor correction stage and the isolated DC-DC converter are expected to show efficiency of 99 and 98 percent, respectively [3].

From the EMI point of view, the wide bang gap switches that are very fast compared to the silicon MOSFETs or IGBTs, add more challenges to the system. The rise time and fall time of these switches can be 10 times faster than silicon switches and the dv/dt can reach anywhere between 30-100 kV/μs [4]. Hence, the EMI noise modeling, analyzing, and mitigation techniques in the high frequency power converters are inevitable.

In this research, modeling and analyzing the parasitic parameters of the components of the power electronics systems is considered as the first step in analyzing and mitigating the EMI noise level. Among the components, high frequency transformers (HFTs) and inductors create the main paths for EMI noise flowing and show design complexity, which should be taken into account. Optimizing and improving the performance of the HFTs, not only increase the system efficiency, but also lead to lower EMI noise in the system.

In this research, parasitic parameters of HFTs are modeled and analyzed by analytical modeling, FEM technique, and experimental results. Moreover, an optimal design method for HFTs is proposed for limiting the parasitic parameters and adjusting leakage inductance and parasitic capacitances. The proposed methods of calculating and modeling the parasitic parameters of the HFTs and inductors, not only are applicable for

EMC purposes, but also applicable to design resonant converters. Furthermore, mentioned models are used for EMC modeling of the power conversion systems and by using these models, the EMI noise level was analyzed and attenuated. Additionally, different methods of noise reduction techniques such as using EMI filters, balancing the noise sources, and hybrid methods are analyzed and compared and the optimal method was proposed for limiting the EMI noise under the IEC61800-3 standards.

This dissertation consists of three transaction/journal papers. In the first paper, HF transformer parasitic parameters, such as leakage inductances and parasitic capacitances, are analyzed using a novel analytical method, finite element method, and experimental measurements for different structures and windings arrangements. Also, the magnetic field, electric field, electric displacement field, and electric potential distribution within the transformers are simulated and analyzed. Four different high frequency transformers with E and U cores with different windings are designed and analyzed. Investigation outcomes help to classify structures according to the trade-off between leakage inductances and series parasitic capacitance. This information can later be used for the optimal selection and design of transformers as a function of their operating frequency for any power rating and voltage level. Moreover, 3D FEM and experimental results validate the proposed methodology to be used for designing HF transformers in high voltage/power applications. In this part, different structures of transformers with different winding arrangements are designed, analyzed, simulated, and experimentally validated. The structures are designed and selected based on the feasibility and popularity of manufacturing in industrial applications for high power. Flux density, magnetic field, and electric fields distribution are obtained. The leakage inductance and parasitic capacitances, which resulted from a

novel analytical method, FEM, and experimental are investigated and compared to each other.

In the second paper, an electric system is analyzed and the EMI propagation routes are investigated. In addition, the EMI noise level of the system is shown. For improving the EMC and reducing the EMI noise level under IEC61800-3 limits, transformer parasitic parameters are modeled to be optimized and block the EMI circulation. Transformer parasitics provide the main path for CM EMI circulation. Novel analytical and FEM methods are proposed for both leakage inductance and parasitic capacitance. Additionally, different pareto-optimal techniques are implemented into the defined cost function for achieving the best combination of parasitic parameters. FEM analysis and experimental results are used to verify the model. The winding arrangement and structure for FEM and experimental verifications are chosen due to the previous research in the first paper, which proved that this structure is the best, both in terms of leakage inductance and parasitic capacitance for some applications. At the end, it is shown that, after optimization, the CM EMI noise level of the system is decreased significantly and placed in a good agreement with IEC61800-3 standard.

In the third paper, conducted CM EMI noise modeling of an electric system including an AC-DC-DC power supply is developed. The EMI equivalent circuit of the system is explained and the effect of each component and each noise source is investigated. Moreover, the noise flowing into the isolation stage of the AC-DC-DC system that provides the path for noise circulating is analyzed. The CM noise voltage level and impedance of the system are investigated and calculated. Furthermore, the effect of different parasitic parameters values on the CM noise voltage is studied. Additionally, an optimized EMI

filter is designed and studied and the effect of that filter on the power supply CM noise voltage level is analyzed. As well, EMI noise reduction techniques are explained and used for this system and by applying those methods the EMI level is reduced significantly to meet IEC61800-3 [22] limits. Contributions of this paper are analyzing EMI noise and developing new reduction techniques by considering the power supply. In more detail, a novel method of EMI analysis and CM noise attenuation techniques are proposed by considering the noise propagation of the feeding power converter. Moreover, optimized EMI filters for the system are designed and developed by considering both magnetic and parasitic behavior, which lead to filter minimization or filter-free systems.

PAPER

I. INVESTIGATION OF VARIOUS TRANSFORMER TOPOLOGIES FOR HF ISOLATION APPLICATIONS

ABSTRACT

High frequency (HF) transformers are an essential part of many power electronics devices. The performance and behavior of HF transformers, can greatly affect the efficiency and performance of all systems, particularly, from a parasitic parameters point of view. In this paper, HF transformer parasitic parameters, such as leakage inductances and parasitic capacitances, are analyzed using a novel analytical method, finite element method (FEM), and experimental measurements for different structures and windings arrangements. Also, the magnetic field, electric field, electric displacement field, and electric potential distribution within the transformers are simulated and analyzed. Four different high frequency transformers with E and U cores with different windings are designed and analyzed. Investigation outcomes help to classify structures according to the trade-off between leakage inductances and series parasitic capacitance. This information can later be used for the optimal selection and design of transformers as a function of their operating frequency for any power rating and voltage level. Moreover, 3D FEM and experimental results validate the proposed methodology to be used for designing HF transformers in high voltage/power applications.

NOMENCLATURE

Symbol	Description
A, B, C	Block set dimensions [m].
$\hat{A}$	Cross-sectional area [m^2].
B	Magnetic flux density [T].
B_m	Amplitude of the flux density peak [T].
C_p	Intra-winding capacitance of primary [F].
C_s	Intra-winding capacitance of secondary [F].
$C_{p_i s_j}$	Capacitance between any arbitrary two layers of primary and secondary [F].
C_{ps}	Total inter-winding capacitance [F].
C_{ps1}, C_{ps2}, C_{ps3}, C_{ps4}	Inter-winding capacitances between primary and secondary [F].
D	Core depth [m].
D_{dsp}	Electric displacement field [C/m^2].
$\widehat{D}$	Duty cycle.
$E_{ins_{primary}}$	Energy stored in the primary insulations [J].
$E_{ins_{secondary}}$	Energy stored in the secondary insulations [J].
$E_{primary}$	Energy stored in the primary conductors [J].
$E_{secondary}$	Energy stored in the secondary conductors [J].
f	Frequency [Hz].

H	Magnetic field strength [A/m].
h	Window height [m].
$I_{primary}$	Primary current [A].
$I_{secondary}$	Secondary current [A].
$L_{leakage}$	Leakage inductance [H].
L_m	Magnetizing inductance [H].
ℓ	Length path on the core [m].
m_1	Number of conductor layers on primary.
m_2	Number of conductor layers on secondary.
MLT_{pri}	Mean length turn of primary [m].
MLT_{sec}	Mean length turn of secondary [m].
N	Primary number of turns.
n_1	Number of conductors per layer on primary.
n_2	Number of conductors per layer on secondary.
$P_{core\ loss}$	Core loss density [W/m^3].
$t_{cond_{pri}}$	Thickness of primary conductors [m].
$t_{cond_{sec}}$	Thickness of secondary conductors [m].
t_b	Thickness of bobbin and spacer [m].
$t_{ins_{pri}}$	Thickness of insulation between primary conductors [m].
$t_{ins_{sec}}$	Thickness of insulation between secondary conductors [m].
V_{p_i}	Voltage of ith layer of primary [V].
V_{s_i}	Voltage of ith layer of secondary [V].

V_p	Primary voltage [V].
V_s	Secondary voltage [V].
w	Window width [m].
α, β, k	Constant values of magnetic core.
$\mathcal{R}$	Magnetic reluctance [A/Wb].
γ	Primary to secondary turn ratio.
ε	Absolute permittivity [F/m].
μ	Absolute permeability [H/m].

1. INTRODUCTION

Parasitics play an important role in the design and performance of electronics and electrical devices. In transformers, the leakage inductance and parasitic capacitances have a significant impact on performance and efficiency. Leakage inductance changes field distribution, contributes to skin-effect losses, and because of its non-magnetizing stored energy, voltage spikes would occur [1]-[3]. In high frequency transformers used in the power electronics applications, these effects can lead to problems such as electromagnetic interferences (EMI), circulating reactive power, the shifts that may occur in soft switching region in phase shift modulated DC-DC converters, and efficiency reduction [4]-[6]. Moreover, in applications using soft switching techniques, it is tempting to use the leakage inductance of the transformer instead of the actual inductor in the resonant tank circuit; since it reduces size of the elements, which is important in applications like electric vehicle fast charging [7]-[10]. However, care should be taken as this approach can lead to higher

power losses. Furthermore, in some power electronics applications for filtering, tuning, and/or eliminating series inductors, the specific leakage inductance value may be used.

Leakage inductance values depend on the transformer structure and winding arrangements [11]. Therefore, in the designing process, a comprehensive vision of different structures and winding arrangements is required as they can lead to a range of values for leakage inductance. In [12], leakage inductance was evaluated for different transformer structures by analytical expressions and validated by FEM for an HF planar transformer in a DC-DC converter. In [13], a detailed model of winding arrangement dimensions depicted the calculation of leakage inductance by energy technique. In both [12] and [13], besides the limitations of winding arrangements, the magnetic field distribution was assumed linear in both magnetic and insulation parts, which makes the accuracy insufficient. Moreover, in [14] and [15], frequency dependent methods proposed to calculate the leakage inductance, however [16] shows that the deviation of the methods proposed by [14] and [15] from FEM and experimental results can reach up to 30%. Additionally, in [16] and [17], more elaborate analytical techniques are proposed, by taking HF effects into account for EE core transformers but the validation accuracy is still unclear. The methods of [16] and [17] validated by 2D FEM and low number of turns experimental results--maximum number of turns used in [14] and [15] is 6 and 20 respectively--which make them uncertain for some winding arrangements with a high number of turns such as high power and high/medium voltage converters [18]-[21]. Also, the methods proposed in [16] and [17] are only suitable for a specific EE core structure and winding arrangement.

Table 1. Several magnetic materials for HF transformer cores.

Material Type	Composition	Relative Permeability	Saturation Flux (T)	Density (g/cm^3)
Iron Powder	Fe	4-100	0.5-1.4	3.3-7.2
High Flux	Fe, Ni	14-160	1.5	8
MPP	Fe, Ni	14-550	0.7	8.5
Kool Mu (Sendust)	Fe, Si, Al	26-125	1	6.15
MnZn Ferrite	Fe, Zn, Mn	750-15000	0.3-0.5	4.8
NiZn Ferrite	Fe, Zn, Ni	15-1500	0.3-0.5	4.8

The other significant parameter in transformers is parasitic capacitance, which create path for common mode (CM) noise. In some cases, parasitic capacitances can interrupt resonant modes; because of high dv/dt in switches, high frequency currents can flow into the circuit and create EMI problems, which can lead to unwanted electrostatic coupling and efficiency reduction, especially in SiC and GaN switches with short rise and fall times [22]-[24]. In [25], the parasitic capacitance of a high voltage transformer was analyzed and validated by experimental results and in [26] a new technique was introduced to calculate and reduce the parasitic capacitance of HF transformers. However, in the design process of isolated DC-DC converters with fast switches and lower EMI, considering the parasitic capacitance behavior along with leakage inductance and different winding arrangements is an important issue that is not covered in the previous researches.

In this paper, different structures of transformers with different winding arrangements are designed, analyzed, simulated, and experimentally validated. The structures are designed and selected based on the feasibility and popularity of manufacturing in industrial applications for high power. Flux density, magnetic field, and electric fields distribution are obtained. The leakage inductance and parasitic capacitances,

which resulted from a novel analytical method, FEM, and experimental are investigated and compared to each other. These structures are going to be incorporated in a high-voltage extreme fast charging converter with H-bridge cells that use HF isolation stages. The contribution of this paper is to develop an accurate and novel methodology for selecting an HF isolation transformer considering both the leakage inductance and series parasitic capacitance. The proposed methodology, which validated by FEM and experimental results, not only help the industries to optimize the HF transformer topologies and decrease/adjust the parasitic parameters, also provide a comprehensive analysis for parasitic behavior of the transformers. Moreover, the proposed methodology can be applied to any structure, power rating, voltage level, and frequency, especially high power and high voltage applications.

2. DESIGN OBJECTIVES

In the design process of HF transformers, the major steps are designing magnetic inductance, leakage inductance, and insulation. To design magnetizing inductance the magnetic core should be chosen first. The transformer is designed at 1kW power rating with primary and secondary voltage of 200V operating at the frequency of 3 kHz.

When choosing the magnetic core there are different options at high frequency. Three major factors that determine the type of magnetic material are cost, size, and performance. These three factors are dependent on core loss, temperature stability, permeability, etc. In HF transformers, a higher saturation flux point can result in smaller

passive components, and lower core loss leads to higher efficiencies. Table 1 shows different magnetic material.

In this design, Kool Mu is used for magnetic core. Kool Mu demonstrates a saturation point of 1T and a permeability of 26. By the modified Steinmetz equation presented in [27], the loss density of the core is determined:

$$P_{core\ loss} = \frac{2^{\beta+1}\bar{D}}{(\bar{D})^{\alpha}} \cdot \frac{1}{(2\pi)^{\alpha-1}\int_0^{2\pi}|\cos\theta|^{\alpha}.2^{\beta-\alpha}.d\theta} . K . f^{\alpha} . {B_m}^{\beta} \quad (1)$$

Constant values for Kool Mu are shown in Table 2. Power loss density in the frequency of 3 kHz with the flux density of 0.9T at duty cycle of 0.5 is 733.44 mW/cm^3.

By fixing the maximum flux at 0.9T and considering the B-H curve of Kool Mu, the number of turns on the primary and the secondary can be found by equations (2) and (3). The calculations are obtained from quasi-sinusoidal forms.

$$L_m = \frac{N^2}{\mathcal{R}} \quad (2)$$

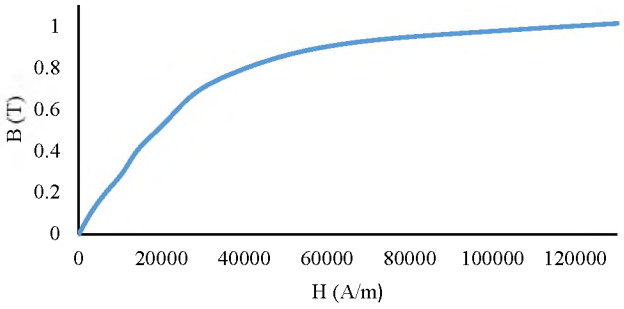


Figure 1. B-H curve of the Kool Mu.

Table 2. Constant values of the Kool Mu.

$K(mW/cm^3)$	94.674
α	1.998
β	1.402

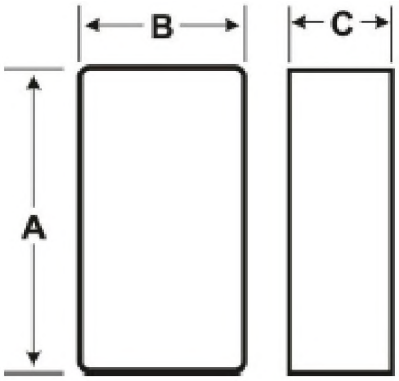
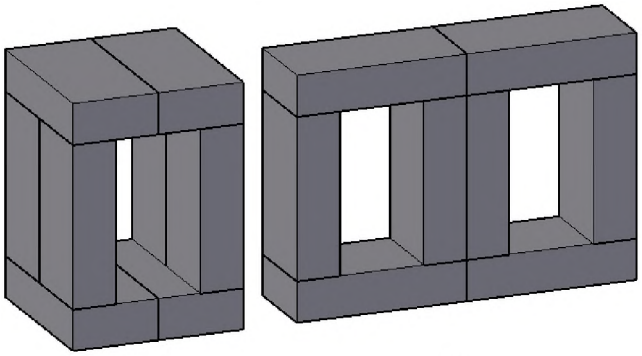


Figure 2. A block set of the Kool Mu.



(a) (b)

Figure 3. Structures of the proposed transformers. Both shapes are composed of 8 blocks. a) UU core. b) EE core.

Table 3. Dimensions of a block set.

A	60(mm)
B	30(mm)
C	15(mm)

$$N.I_{primary} = \sum H.\ell \tag{3}$$

$$\mathcal{R} = \frac{\ell}{\mu \tilde{A}} \tag{4}$$

In Figure 1, the B-H curve of Kool Mu is shown. Topologies of the transformer are considered EE and UU shapes. The geometry determines the average length path and remarkably affects both leakage inductance and parasitic capacitance. Figure 2 and Figure 3 depict a block set dimensions and two types of geometries used for simulation and experimental results, respectively. Also, Table 3 shows the dimensions of Figure 2. In this design, 8 Kool Mu blocks are used to satisfy the window area and the desired inductance.

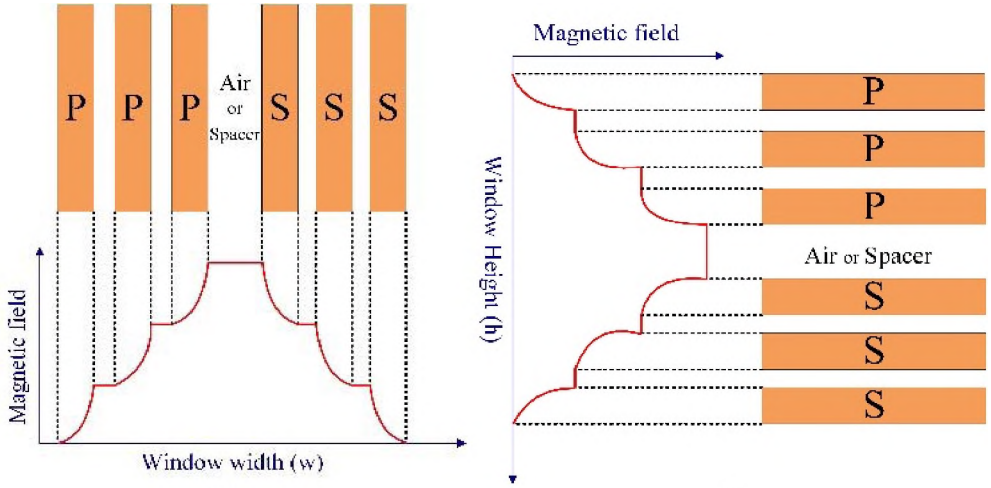


Figure 4. Magnetic field strength distribution on the windings, air and spacer. a) Magnetic field strength distribution on the layers along with *w*. b) Magnetic field strength distribution on the layers along with *h*.

In the B-H curve, the corresponding point of B=0.9T for the magnetic field strength is almost H=1000(A/m). To adjust the primary current to at least 4 times greater than the magnetizing current, the number of turns is considered 400 turns for both the primary and the secondary. Also, AWG#19 is used for the transformers' windings.

2.1. LEAKAGE INDUCTANCE

Imperfect magnetic coupling between the windings of a transformer results in leakage inductance. Not all magnetic flux passes through the core; instead, a portion closes in air, insulation, or windings. This leakage magnetic field or inductance in an HF transformer significantly affects the performance of the power electronics device and as the frequency increases the leakage inductance values change because of the skin effect. Figure 4 shows the magnetic field strength distribution on the windings and the space between conductors. The classic analytical models of leakage inductance suppose that the magnetic field distribution inside the conductors is linear. While, the frequency dependent models consider the nonlinearity of the magnetic field distribution. As the frequency increases the nonlinearity intensifies and the overall area under the magnetic field curve decreases.

While the secondary is short circuited, magneto motive force (MMF) distribution in the space, especially in the window area, represents the behavior of leakage inductance. Additionally, leakage inductance is proportional to the energy stored in the space, and with (6) and (7), the magnetic energy in the space is related to magnetic field strength (H).

$$MMF = \oint H.d\ell \tag{5}$$

$$E_{magnetic\ energy} = \frac{1}{2}\iiint H.Bdv \tag{6}$$

$$B = \mu H \tag{7}$$

$$E_{total\ stored\ energy} = \frac{1}{2}.L_{leakage}.I_{primary}^{2} \tag{8}$$

Changing the windings arrangements is an efficient way to alter and set the leakage inductance. By changing the winding arrangements, the magnetic coupling between windings changes and different winding arrangements could lead to build a range for

leakage inductance. In this paper, the results show a range of leakage inductance values that represent each arrangement capability of producing leakage inductance.

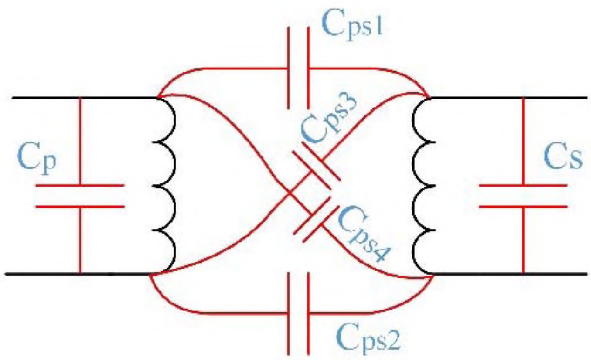


Figure 5. Inter-winding and intra-winding parasitic capacitances.

2.2. PARASITIC CAPACITANCE

Figure 5 shows the model of inter-winding and intra-winding parasitic capacitances. The inter-winding capacitances are the main path of CM noise in the converters using isolated transformers. Also, the intra-winding capacitance governs the self-resonance of the transformer. The coupling capacitances result in circulating high frequency currents. This is intensified in high power devices with SiC MOSFET switches in which dV/dt can reach to 30-100 kV/μs [28]. To avoid these high frequency currents, which cause problems in control parts, lead to EMI problems, and cause interruptions in resonant modes, the value of the capacitances should be calculated. Also, parasitic capacitance varies as winding arrangements and the core structure change.

Parasitic capacitance can be found by calculating the total energy stored in the electric field:

$$E_{electric\ energy} = \frac{1}{2}\iiint D_{dsp}.Edv \tag{9}$$

$$D_{dsp} = \varepsilon E \tag{10}$$

$$E_{total\ stored\ energy} = \frac{1}{2}C.V^2 \tag{11}$$

In some cases, the parasitic capacitances lead to an unwanted resonant mode as well as current spikes, which cause an interruption in soft switching. In [28], by using different cores and some insulation methods, the capacitance between the primary and the secondary decreased to 0.5pF. In this paper, different winding arrangements and cores are investigated for finding electric field distribution and calculating the parasitic capacitance of the transformers with different arrangements.

2.2.1. Transformer Models. UU cores demonstrate simplicity in winding arrangements and a high window utilization factor. In some applications the high density of the electric field can be reduced by using CC cores with round corners. Furthermore, EE cores are widely used in power electronics applications. If airgaps are needed, EE cores allow for gapping of the center leg, which decreases the EMI and causes fringing problems [29]. As the windings in these cores are not completely covered by magnetic material, there is more EMI issues with this type of cores compared to pot and PQ cores, which makes them unsuitable for very high frequency applications.

In Figure 6, transformer models with winding arrangements that are analyzed in this paper are depicted. In Figure 6(a), the primary and secondary are wound on different legs, while in Figure 6(b), both the primary and the secondary are wound on the middle leg, and in Figure 6(c) the primary and the secondary are wound on the middle leg on each other and this configuration increases the magnetic coupling between the primary and the secondary. In Figure 6(d), both windings are on the same middle leg, but the secondary is

divided into two identical 200-turn windings. In all figures, bobbins with spacers that have a thickness of 2mm are observable.

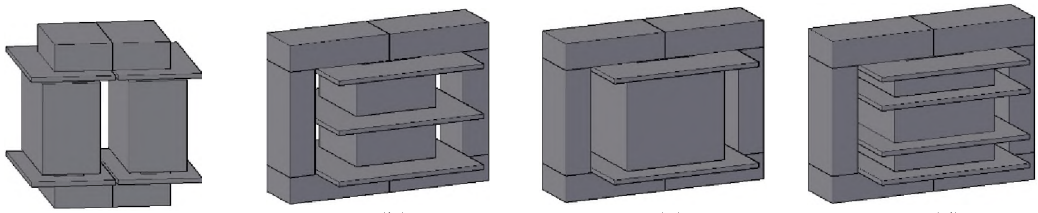


Figure 6. Different transformer models and winding arrangements. a) UU core with the primary and the secondary wound on separated legs. b) EE core with the primary and the secondary wound on the middle leg. c) EE core with the primary and the secondary wound on each other. d) EE core with the primary on the middle and half of the secondary on top and half on bottom.

3. PARASITIC PARAMETERS ANALYSIS

To find leakage inductance for each structure, the leakage energy stored in different parts of the transformer such as insulation, spacer and conductor parts should be calculated. For this aim, by using Maxwell equations and finding the magnetic field strength in different parts of the transformer, the leakage inductance for each structure is formulated. Also, in order to find the parasitic capacitance, by using stored energy technique and equations (9)-(11) the parasitic capacitance can be formulated. Note that, in a nonconductive core the parasitic capacitance is the inter-winding capacitance between primary and secondary, but in a conductive core in addition to the inter-winding, the capacitances between windings and the core can play a role. FEM simulation show that in the structures modeled in this paper, the majority of the parasitic capacitance forms between the primary and secondary. Also, this capacitance that is the leading cause of the

CM noise, is 10 times higher than the sum of other capacitances (if the core is also conductive). Hence, other capacitances are not analytically modeled in this paper. However, the methodology for finding the inter-winding capacitances used in this paper can still be used if anyone is interested in formulating the remaining capacitances as well. In the following, the leakage inductance and parasitic capacitance for the transformer structures are presented. Types a, b, c, and d are the same as Figure 6.

3.1. PARASITIC PARAMETERS FOR TYPE a

To find the leakage inductance, by using (6) the energy stored in the insulation parts of the primary and secondary and the conductors of the primary and secondary is calculated.

$$E_{ins_{primary}} = \frac{1}{2}\mu(h)\left(MLT_{pri}\right)\sum_{i=1}^{m_1-1}\left(\int_0^{t_{ins_{pri}}}\left(\frac{in_1 I_{primary}}{h}\right)^2 dx\right) \tag{12}$$

$$E_{ins_{secondary}} = \frac{1}{2}\mu(h)(MLT_{sec})\sum_{i=1}^{m_2-1}\left(\int_0^{t_{ins_{sec}}}\left(\frac{in_2 I_{secondary}}{h}\right)^2 dx\right) \tag{13}$$

To find $E_{primary}$ and $E_{secondary}$, the magnetic field in the primary and secondary conductors should be found. H_1 and H_2 are the magnetic field in the primary and secondary conductors, respectively.

$$H_1 = H_{11}e^{\frac{1+j}{\delta}x} + H_{21}e^{-\frac{1+j}{\delta}x} \tag{14}$$

$$H_2 = H_{12}e^{\frac{1+j}{\delta}x} + H_{22}e^{-\frac{1+j}{\delta}x} \tag{15}$$

Also, δ is the skin depth:

$$\delta = \frac{\sqrt{2}}{\sqrt{2\pi f\mu\sigma}} \tag{16}$$

H_{c1} and H_{c2} that resulted from the boundary conditions, are defined:

$$H_{c1} = \frac{n_1 I_{primary}}{h} \tag{17}$$

$$H_{c2} = \frac{n_2 I_{secondary}}{h} \tag{18}$$

By applying the boundary conditions the coefficient of H_1 and H_2 are obtained:

$$H_{11} = \frac{(m_1-1)H_{c1} - e^{(-\frac{1+j}{\delta}t_{cond_{pri}})} m_1 H_{c1}}{e^{(\frac{1+j}{\delta}t_{cond_{pri}})} - e^{(-\frac{1+j}{\delta}t_{cond_{pri}})}} \tag{19}$$

$$H_{21} = \frac{(m_1-1)H_{c1} - e^{(\frac{1+j}{\delta}t_{cond_{pri}})} m_1 H_{c1}}{e^{(-\frac{1+j}{\delta}t_{cond_{pri}})} - e^{(\frac{1+j}{\delta}t_{cond_{pri}})}} \tag{20}$$

$$H_{12} = \frac{(m_2-1)H_{c2} - e^{(-\frac{1+j}{\delta}t_{cond_{sec}})} m_2 H_{c2}}{e^{(\frac{1+j}{\delta}t_{cond_{sec}})} - e^{(-\frac{1+j}{\delta}t_{cond_{sec}})}} \tag{21}$$

$$H_{22} = \frac{(m_2-1)H_{c2} - e^{(\frac{1+j}{\delta}t_{cond_{sec}})} m_2 H_{c2}}{e^{(-\frac{1+j}{\delta}t_{cond_{sec}})} - e^{(\frac{1+j}{\delta}t_{cond_{sec}})}} \tag{22}$$

Therefore, $E_{primary}$ and $E_{secondary}$ can be shown in the following equations:

$$E_{primary} = \frac{1}{2}\mu(h)\left(MLT_{pri}\right)\sum_{i=1}^{m_1}\left(\int_0^{t_{cond_{pri}}}\left(H_{11}e^{\frac{1+j}{\delta}x} + H_{21}e^{-\frac{1+j}{\delta}x}\right)^2 dx\right) \tag{23}$$

$$E_{secondary} = \frac{1}{2}\mu(h)(MLT_{sec})\sum_{i=1}^{m_2}\left(\int_0^{t_{cond_{sec}}}\left(H_{12}e^{\frac{1+j}{\delta}x} + H_{22}e^{-\frac{1+j}{\delta}x}\right)^2 dx\right) \tag{24}$$

Moreover, the stored energy between the primary and secondary windings at the window area can be calculated by the following equation:

$$E_{p-s} = \frac{1}{2}\mu(h)\left(MLT_{p-s}\right)\int_0^{t_{p-s}}\left(\frac{n_1 m_1 I_{primary}}{h}\right)^2 dx \tag{25}$$

Then, by using (8) the leakage inductance can be calculated. By using (9)-(11), the parasitic capacitance between the primary and secondary for type a can be calculated.

$$E_{total\ stored\ energy} = \frac{1}{2}\sum_{i=1}^{m_1}\sum_{j=1}^{m_2} C_{p_i s_j}(V_{p_i} - V_{s_i})^2 = \frac{1}{2}C_{ps4}V_p^2 + \frac{1}{2}C_{ps3}V_s^2 + \frac{1}{2}C_{ps1}(V_p - V_s)^2 = \frac{1}{2}\left(C_{ps4} + \frac{C_{ps3}}{\gamma^2} + \frac{C_{ps1}(\gamma-1)^2}{\gamma^2}\right)V_p^2 = \frac{1}{2}\left(C_{ps}\right)V_p^2 \tag{26}$$

$$V_{p_i} - V_{s_i} = \frac{V_p}{m_1} + \frac{V_s}{m_2} \tag{27}$$

$$C_{p_i s_j} = \frac{\varepsilon.D.min\{n_1 t_{cond_{pri}}, n_2 t_{cond_{sec}}\}}{w - 2t_b - it_{cond_{pri}} - jt_{cond_{sec}} + t_{ins_{pri}} + t_{ins_{sec}}} \tag{28}$$

Therefore, C_{ps} can be obtained:

$$C_{ps} = \sum_{i=1}^{m_1} \sum_{j=1}^{m_2} C_{p_i s_j} \left(\frac{1}{m_1^2} + \frac{1}{\gamma^2 m_1^2} + \frac{2}{\gamma m_1 m_2}\right) \tag{29}$$

3.2. PARASITIC PARAMETERS FOR TYPE b

To find the leakage inductance for this structure, the same steps as type a, should be followed.

$$E_{ins_{primary}} = \frac{1}{2}\mu(w)\left(MLT_{pri}\right) \sum_{i=1}^{n_1 - 1} \left(\int_0^{t_{ins_{pri}}} \left(\frac{i m_1 I_{primary}}{w}\right)^2 dx \right) \tag{30}$$

$$E_{ins_{secondary}} = \frac{1}{2}\mu(w)(MLT_{sec}) \sum_{i=1}^{n_2 - 1} \left(\int_0^{t_{ins_{sec}}} \left(\frac{i m_2 I_{secondary}}{w}\right)^2 dx \right) \tag{31}$$

$$H_{c1} = \frac{m_1 I_{primary}}{w} \tag{32}$$

$$H_{c2} = \frac{m_2 I_{secondary}}{w} \tag{33}$$

$$H_{11} = \frac{(n_1 - 1)H_{c1} - e^{\left(-\frac{1+j}{\delta} t_{cond_{pri}}\right)} n_1 H_{c1}}{e^{\left(\frac{1+j}{\delta} t_{cond_{pri}}\right)} - e^{\left(-\frac{1+j}{\delta} t_{cond_{pri}}\right)}} \tag{34}$$

$$H_{21} = \frac{(n_1 - 1)H_{c1} - e^{\left(\frac{1+j}{\delta} t_{cond_{pri}}\right)} n_1 H_{c1}}{e^{\left(-\frac{1+j}{\delta} t_{cond_{pri}}\right)} - e^{\left(\frac{1+j}{\delta} t_{cond_{pri}}\right)}} \tag{35}$$

$$H_{12} = \frac{(n_2 - 1)H_{c2} - e^{\left(-\frac{1+j}{\delta} t_{cond_{sec}}\right)} n_2 H_{c2}}{e^{\left(\frac{1+j}{\delta} t_{cond_{sec}}\right)} - e^{\left(-\frac{1+j}{\delta} t_{cond_{sec}}\right)}} \tag{36}$$

$$H_{22} = \frac{(n_2 - 1)H_{c2} - e^{\left(\frac{1+j}{\delta} t_{cond_{sec}}\right)} n_2 H_{c2}}{e^{\left(-\frac{1+j}{\delta} t_{cond_{sec}}\right)} - e^{\left(\frac{1+j}{\delta} t_{cond_{sec}}\right)}} \tag{37}$$

Therefore,

$$E_{primary} = \frac{1}{2}\mu(w)\left(MLT_{pri}\right)\sum_{i=1}^{n_1}\left(\int_0^{t_{cond_{pri}}}\left(H_{11}e^{\frac{1+j}{\delta}x} + H_{21}e^{-\frac{1+j}{\delta}x}\right)^2 dx\right) \quad (38)$$

$$E_{secondary} = \frac{1}{2}\mu(w)(MLT_{sec})\sum_{i=1}^{n_2}\left(\int_0^{t_{cond_{sec}}}\left(H_{12}e^{\frac{1+j}{\delta}x} + H_{22}e^{-\frac{1+j}{\delta}x}\right)^2 dx\right) \quad (39)$$

Also, the stored energy between the primary and secondary windings can be calculated by the following equation:

$$E_{p-s} = \frac{1}{2}\mu(w)\left(MLT_{p-s}\right)\int_0^{t_{p-s}}\left(\frac{n_1 m_1 I_{primary}}{w}\right)^2 dx \quad (40)$$

Then, by using (8) the leakage inductance can be calculated.

Also, the parasitic capacitance between the primary and secondary for type b can be calculated by the followings:

$$E_{total\ stored\ energy} = \frac{1}{2}\sum_{i=1}^{n_1}\sum_{j=1}^{n_2} C_{p_i s_j}(V_{p_i} - V_{s_i})^2 = \frac{1}{2}C_{ps4}V_p^2 + \frac{1}{2}C_{ps3}V_s^2 + \frac{1}{2}C_{ps1}(V_p -$$

$$V_s)^2 = \frac{1}{2}\left(C_{ps4} + \frac{C_{ps3}}{\gamma^2} + \frac{C_{ps1}(\gamma-1)^2}{\gamma^2}\right)V_p^2 = \frac{1}{2}\left(C_{ps}\right)V_p^2 \quad (41)$$

$$V_{p_i} - V_{s_i} = \frac{V_p}{n_1} + \frac{V_s}{n_2} \quad (42)$$

$$C_{p_i s_j} = \frac{\varepsilon.\pi.\left[(C+t_b+min\{m_1 t_{cond_{pri}}, m_2 t_{cond_{sec}}\})^2 - (C+t_b)^2\right]}{t_b + (n_1 - i)t_{cond_{pri}} + t_{ins_{pri}} + (j-1)t_{cond_{sec}} + t_{ins_{sec}}} \quad (43)$$

$$C_{ps} = \sum_{i=1}^{n_1}\sum_{j=1}^{n_2} C_{p_i s_j}\left(\frac{1}{n_1^2} + \frac{1}{\gamma^2 n_1^2} + \frac{2}{\gamma n_1 n_2}\right) \quad (44)$$

3.3. PARASITIC PARAMETERS FOR TYPE c

For this structure, $E_{ins_{primary}}$, $E_{ins_{secondary}}$, $E_{primary}$, and $E_{secondary}$ are the same as type a. The only difference here is the absence of E_{p-s}, because in this winding arrangement there is no major spacer between the primary and secondary. Moreover,

equations (26), (27), and (29) are valid for finding the inter-winding capacitance for this type but $C_{p_i s_j}$ that is directly related to the structure and winding arrangement is different:

$$C_{p_i s_j} = \frac{2\varepsilon.\pi.min\{n_1 t_{cond_{pri}}, n_2 t_{cond_{sec}}\}}{\ell n\left(\frac{c+t_b+m_1 t_{cond_{pri}}+(j-1)t_{cond_{sec}}+t_{ins_{sec}}}{c+t_b+it_{cond_{pri}}-t_{ins_{pri}}}\right)} \quad (45)$$

3.4. PARASTIC PARAMETERS FOR TYPE d

$E_{ins_{primary}}$ for this structure is the same as equation (30). But $E_{ins_{secondary}}$ is not the same as type b.

$$E_{ins_{secondary}} = \mu(w)(MLT_{sec}) \sum_{i=1}^{\left\lceil \frac{n_2}{2} \right\rceil - 1} \left(\int_0^{t_{ins_{sec}}} \left(\frac{i m_2 I_{secondary}}{w} \right)^2 dx \right) \quad (46)$$

Also, H_{c1}, H_{c2}, H_{11}, and H_{21} are the same as (32)-(35).

$$H_{12} = \frac{2\left(\left\lceil \frac{n_2}{2} \right\rceil - 1\right) H_{c2} - e^{\left(-\frac{1+j}{\delta} t_{cond_{sec}}\right)} n_2 H_{c2}}{e^{\left(\frac{1+j}{\delta} t_{cond_{sec}}\right)} - e^{\left(-\frac{1+j}{\delta} t_{cond_{sec}}\right)}} \quad (47)$$

$$H_{22} = \frac{2\left(\left\lceil \frac{n_2}{2} \right\rceil - 1\right) H_{c2} - e^{\left(\frac{1+j}{\delta} t_{cond_{sec}}\right)} n_2 H_{c2}}{e^{\left(-\frac{1+j}{\delta} t_{cond_{sec}}\right)} - e^{\left(\frac{1+j}{\delta} t_{cond_{sec}}\right)}} \quad (48)$$

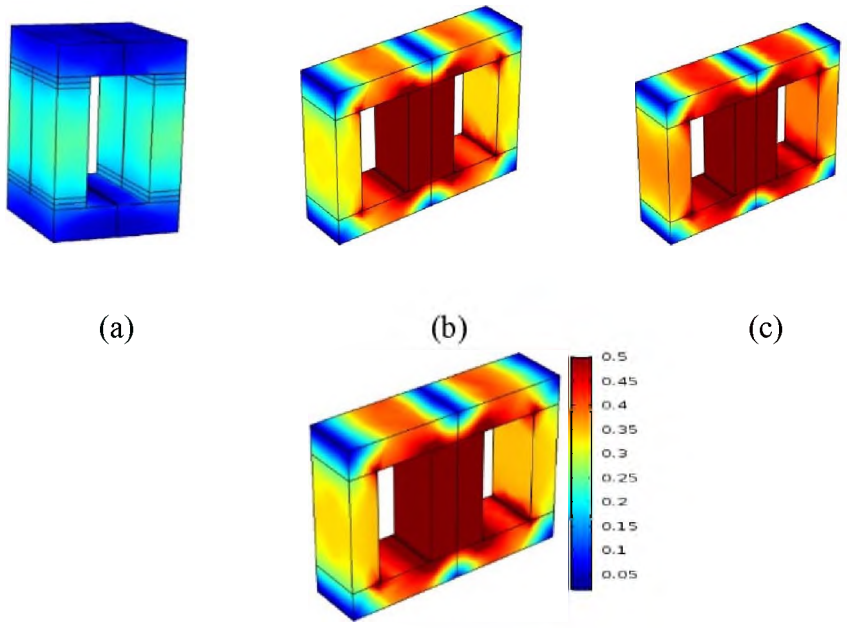
Therefore, $E_{primary}$ is the same as equation (38).

$$E_{secondary} = \mu(w)(MLT_{sec}) \sum_{i=1}^{\left\lceil \frac{n_2}{2} \right\rceil} \left(\int_0^{t_{cond_{sec}}} \left(H_{12} e^{\frac{1+j}{\delta} x} + H_{22} e^{-\frac{1+j}{\delta} x} \right)^2 dx \right) \quad (49)$$

Moreover, the stored energy between the primary and secondary windings is:

$$E_{p-s} = \mu(w)\left(MLT_{p-s}\right) \int_0^{t_{p-s}} \left(\frac{n_1 m_1 I_{primary}}{w}\right)^2 dx \quad (50)$$

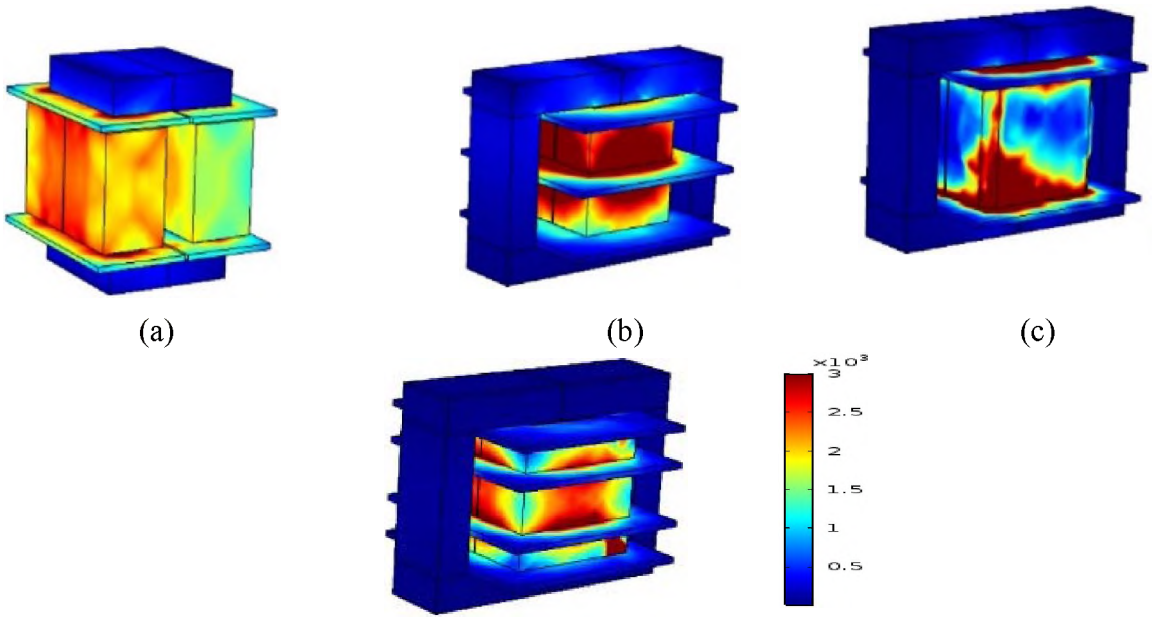
Then, by using (8) the leakage inductance can be calculated. Also, the inter-winding parasitic capacitance for type d can be calculated by the followings:



(a) (b) (c)

(d)

Figure 7. Magnetic flux density distribution (T). Cases a, b, c, and d are based on the cases shown in Figure 6.



(a) (b) (c)

(d)

Figure 8. Magnetic field strength distribution (A/m). Cases a, b, c, and d are based on the cases shown in Figure 6.

$$E_{total\ stored\ energy} = \frac{1}{2}\sum_{i=1}^{n_1}\sum_{j=1}^{\left\lceil\frac{n_2}{2}\right\rceil} C_{p_i s_j}(V_{p_i} - V_{s_i})^2 = \frac{1}{2}C_{ps4}V_p^2 + \frac{1}{2}C_{ps3}V_s^2 + \frac{1}{2}C_{ps1}(V_p - V_s)^2 = \frac{1}{2}\left(C_{ps4} + \frac{C_{ps3}}{\gamma^2} + \frac{C_{ps1}(\gamma-1)^2}{\gamma^2}\right)V_p^2 = \frac{1}{2}(C_{ps})V_p^2 \quad (51)$$

$$C_{p_i s_j} = \frac{2\varepsilon.\pi.\left[(C+t_b+min\{m_1 t_{cond_{pri}}, m_2 t_{cond_{sec}}\})^2-(C+t_b)^2\right]}{t_b+(j-1)t_{cond_{pri}}+t_{ins_{pri}}+\left(\left\lceil\frac{n_2}{2}\right\rceil-i\right)t_{cond_{sec}}+t_{ins_{sec}}} \quad (52)$$

Equation (42) is valid for this structure. Therefore, the inter-winding capacitance can be calculated by the following equation:

$$C_{ps} = \sum_{i=1}^{n_1}\sum_{j=1}^{\left\lceil\frac{n_2}{2}\right\rceil} C_{p_i s_j}\left(\frac{1}{n_1^2} + \frac{1}{\gamma^2 n_1^2} + \frac{2}{\gamma n_1\left\lceil\frac{n_2}{2}\right\rceil}\right) \quad (53)$$

4. FINITE ELEMENT ANALYSIS

4.1. MAGNETIC FIELD DISTRIBUTION IN TRANSFORMER MODELS

The magnetic flux density distribution of the transformers on the cores, during the full load operation are displayed in Figure 7. It is clear that at some points the cores are saturated but the average flux density in all four cores is at the linear part of the Kool Mu B-H curve of Figure 1.

As mentioned in section 2, to find the leakage inductance in the transformers, leakage energy in the space, especially in the window area, needs to be calculated. Therefore, by applying the short circuit test on the secondary and applying the nominal current on the primary, the leakage energy and subsequently leakage inductance can be obtained. Figure 8 shows the magnetic field strength in the transformers during the short

circuit test. As the magnetic field increases in the space and specifically in the window area, the magnetic leakage energy intensifies.

Transformer structures and winding arrangements are responsible for different magnetic field strength and leakage energy. By observing the magnetic energy on different parts of the transformers, the magnetic field on the primary windings are higher than other parts and this results in increase of H_{11} and H_{21} in the analytical modeling of section 2. It is clear in Figure 8 that different winding arrangements for a certain transformer could result in various field distributions. Consequently, based on the special parameters of a power electronics device, a designer may choose a specific arrangement. Total magnetic field during the short circuit in case (a), shown in Figure 8, is higher than other arrangements in other cases. Thus, it is expected that the leakage energy and leakage inductance will become higher. Table 4 presents the leakage inductance and the magnetizing inductance obtained from analytical models and the simulations. Cases a, b, c, and d are the same as the cases shown in Figure 6.

Table 4 shows different winding arrangements and transformer structures with the same electric and magnetic parameters; a wide range of leakage inductance is observable. However, note that due to the same winding turns, magnetic block permeability, and cross-sectional area of the geometries, the magnetizing inductance in all cases is almost the same. As is clear in Table 4, the leakage inductance values resulted from the analytical method and FEM are in a good agreement.

Agreement between analytical method and FEM pave the way of using the mentioned methology for all arrangements and configurations. However, for verification, the experimental resulst should be taken into account, as well.

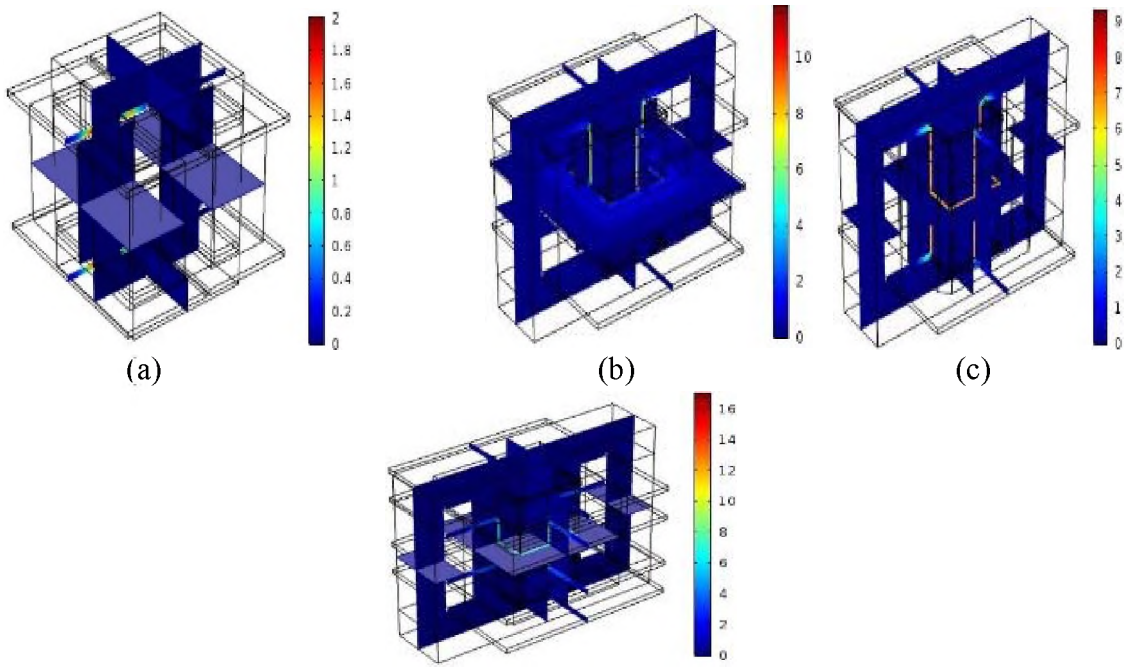


Figure 9. Electric field (kV/mm) distribution in the transformers. Cases a, b, c, and d are based on the cases shown in Figure 6.

Table 4. Magnetizing inductance and leakage inductances of the transformers.

Transformer Type	Magnetizing Inductance(mH)	Leakage Inductance(mH) (Analytical)	Leakage Inductance(mH) (FEM)
a	34.119	23.16	21.872
b	31.992	14.47	13.360
c	33.273	0.887	1.073
d	32.246	7.351	8.038

4.2. ELECTRIC FIELD DISTRIBUTION IN TRANSFORMER MODELS

As is shown in equations (9)-(11), to find the parasitic capacitance in the transformers, the electric field and total stored energy must be calculated. Capacitance between the different parts of each transformer is dependent on the transformer structure, winding arrangements, and dielectric constant of the materials. Therefore, insulation coordination should be designed for the transformers before calculation and measuring the capacitance.

High frequency isolated transformers provide insulation safety for the system. Hence, the insulation design between the primary and the secondary and the primary and the core should be based on the input voltage level. The input voltage level in this study is assumed to be 6 times of the primary, thus it is 1200V. Because this transformer is designed to later be used in a multilevel converter with 6 modules. Note that that the insulation design for the secondary and the core is based on the 200V. Based on the IEEE Std. C57.12.01 dry-type transformer standard [30], the crest value of the lightning impulse test for the aforementioned input voltage level is 10kV, and all the insulation materials used in the transformers need to be designed according to this voltage, which is the maximum insulation requirement.

The insulation material used as bare conductor insulator is silicon varnish with dielectric constant and a dielectric strength of 3.1 and 120kV/mm, respectively. Also, the bobbin material is ABS plastic, with a dielectric constant and dielectric strength of 2.2 and 25kV/mm.

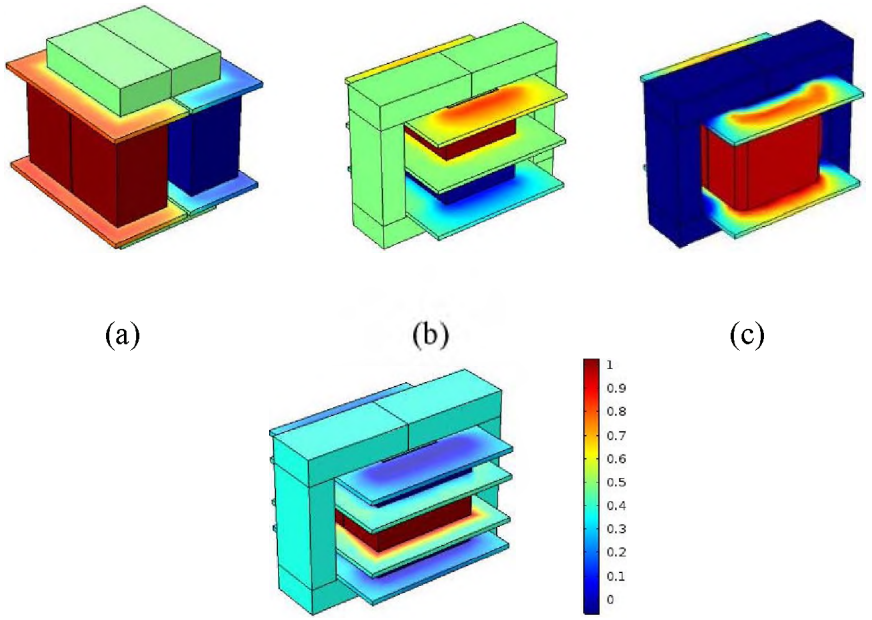
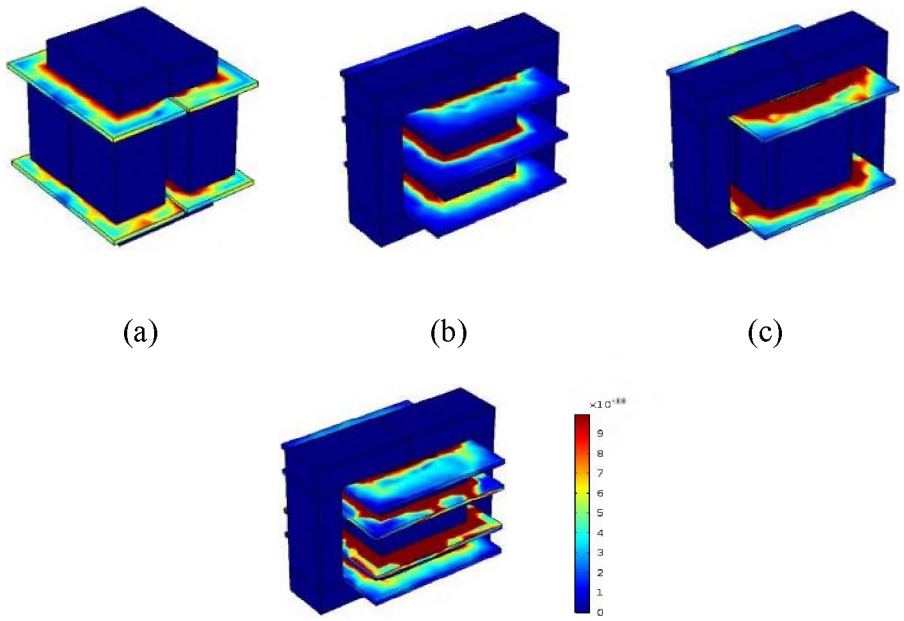


Figure 10. Electric potential (V) distribution in the transformers. Cases a, b, c, and d are based on the cases shown in Figure 6.

The electric field distribution is presented in Figure 9 for the four transformer structures during the presence of all materials with the highest insulation test voltage of 10kV. This figure displays a slice of the cores for better visibility. Based on the IEEE Std. C57.12.01 [30] the maximum electric field for all the structures should be lower than the electric field strength of the materials. Figure 9 shows that the IEEE standard conditions are provided. To find parasitic capacitance, electric potential distribution in the space should be calculated, and then the electric field strength and electric displacement field will be found. Then, by calculating the electric energy stored in the field, the capacitance is calculated. Figure 10 shows the voltage distribution in the space for each transformer structure. The distribution is achieved by applying 1V to a winding and 0V to the other winding of each structure.



(a) (b) (c)

(d)

Figure 11. Electric displacement field (C/m^2) distribution in the transformers. Cases a, b, c, and d are based on the cases shown in Figure 6.

Table 5. Parasitic capacitances of the transformers.

Transformer Type	Parasitic Capacitance (pF) (Analytical)	Parasitic Capacitance (pF) (FEM)
a	29.34	31.05
b	41.86	38.69
c	1426.97	1473.18
D	65.82	62.32

Electric displacement field distribution in the transformers is displayed in Figure 11. Figure 11 clearly shows that in magnetic parts and air domains, the electric

displacement field is very small, but in domains such as bobbins, which have a higher relative permittivity, the electric displacement field increases and leads to creating charge in those areas.

Each process needed to calculate the parasitic capacitance with numeric method is conducted in the FEM software package. Table 5 presents the parasitic capacitance between the primary and the secondary of each transformer structure with the analytical models of section 2 and with FEM simulations. Cases a, b, c, and d are the same as cases shown in Figure 6. Table 5 clearly shows that different winding arrangements of a transformer lead to a wide range of parasitic capacitance. As was expected, in cases with a smaller distance between windings, such as case c, the electric energy and parasitic capacitance is higher than the other transformers with winding arrangements. Also, the parasitic capacitance values resulted from the analytical method and FEM are in a good agreement.

5. EXPERIMENTAL MEASUREMENTS

In this section, the experimental results of the leakage inductance and the parasitic capacitances are presented. The experimental results were achieved for Figure 6(a) which has the lowest capacitance and is suitable for specific applications, Figure6 (c) which is a popular and common structure in industry, and Figure6 (b) and (d) which are the best structures in terms of both leakage inductance and parasitic capacitance. The experimental measurements were achieved by using HP Hewlett Packard 4284A and IET DE-6000 LCR meters. The transformer prototypes were made by the materials and the insulation strategy

mentioned in the previous sections. Figure 12 shows the transformers prototypes and the measurement devices.

Figure 12. Measurement devices and transformer prototypes.

Table 6. Experimental results of leakage inductance and parasitic capacitance.

Transformer Type	Leakage Inductance (mH)	Parasitic Capacitance (pF)
a	20.537	27.12
b	12.37	34.63
c	0.984	1384.1
d	7.267	55.47

Table 6 shows the experimental results values. Cases a, b, c, and d are the same as cases shown in Figure 6. Comparing the experimental and FEM results shows a good agreement between the outcomes. As is clear in Tables 4, 5, and 6, in all of the cases, the difference between the analytical method, 3D FEM, and experimental results is relatively low, which proves the validity of the mathematical model and simulation strategy for obtaining the magnetizing and the leakage inductance and the parasitic capacitance.

To show the superiority of the proposed method in this paper over the other frequency-dependent methods introduced in the introduction, the leakage inductance of type c is calculated with the methods of [14]-[17]. Table 7 shows the leakage inductance values for the transformer type c obtained from different methods and the deviation of the values from experimental result of this paper for type c.

Table 7. Leakage inductances calculated with the methods of [14]-[17].

Method Used from	Leakage Inductance (mH)	Deviation from Experimental (%)
This paper	0.887	9.8
[14]	1.43	45.3
[15]	2.06	109.3
[16]	1.37	39.2
[17]	1.28	30.1

6. CONCLUSION

Parasitic parameters in high frequency transformers can change the performance of power electronics devices, enormously. In this paper, the novel and accurate methodology based on analytical method, FEM, and experimental developed for finding the parasitic parameters of an HF transformer. The results show that for one transformer with the same electric and magnetic parameters, there can be a range of different values for parasitic parameters. Compromising between parasitic values by selecting winding arrangement and transformer structure can relate to other design factors, such as the facility of insulating, specific application, transformer magnetic core selection and designing strategies, etc. The proposed methodology in this paper shows that the transformer designing process, selected insulating materials, insulation strategy, and winding arrangements cause a wide range of parasitic behavior, which should be taken into account for an optimal design to minimize CM noise and reduce EMI in the systems. Based on the methodology and the results, depending on the specific application, in the optimal designing process there should be a trade-off between the parasitic parameters. As an example, low leakage inductance can cause problems for some multilevel converters using phase shift modulation or resonant converters, while a certain value of parasitic capacitance can be integrated in the resonant tank for ZVS/ZVC achievement.

REFERENCES

[1] S. Mohsenzade, M. Aghaei, and S. Kaboli, "Leakage Inductance Calculation of the Transformers with Disordered Windings," *IEEE Transactions on Plasma Science*, vol. 47, no. 4, pp. 1799–1807, 2019.

[2] F. Pan, L. Jin, P. Pan, and Z. Xu, "Design Procedure of the Leakage Inductance for a Pulse Transformer Considering Winding Structures," *IEEE Transactions on Plasma Science*, vol. 45, no. 9, pp. 2504–2510, 2017.

[3] A. Baktash and A. Vahedi, "Calculation of Parasitic Elements in Toroidal Core Transformers," *IEEE Transactions on Plasma Science*, vol. 42, no. 6, pp. 1690–1696, 2014.

[4] J.-E. Baek, J.-H. Rhee, and K.-C. Ko, "Hybrid Analog and Digital Control of a High Current Converter Based on an EDLC Bank for Rapidly Decreasing Input Voltage," *IEEE Transactions on Plasma Science*, vol. 47, no. 1, pp. 542–548, 2019.

[5] M. U. Hassan, M. Humayun, P. Fu, Z. Song, and L. Hua, "Fuzzy Controller Using Circulating Mode for ITER Poloidal Field AC/DC Converter System," *IEEE Transactions on Plasma Science*, vol. 47, no. 6, pp. 2890–2895, 2019.

[6] X. Chen, L. Huang, P. Fu, G. Gao, S. He, and Z. Wang, "The Design on Pulse Distributor and its Online Status Diagnosis for ITER PF ac/dc Converter," *IEEE Transactions on Plasma Science*, vol. 46, no. 6, pp. 2262–2266, 2018.

[7] A. Zabihinejad and P. Viarouge, "Optimal Design of High-Power Modular Multilevel Active Front-End Converter Using an Innovative Analytical Model," *IEEE Transactions on Plasma Science*, vol. 46, no. 10, pp. 3417–3426, 2018.

[8] Y. Shi, R. Li, Y. Xue, and H. Li, "Optimized Operation of Current-Fed Dual Active Bridge DC–DC Converter for PV Applications," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 11, pp. 6986–6995, 2015.

[9] J.-W. Yang and H.-L. Do, "Soft-Switching Dual-Flyback DC–DC Converter With Improved Efficiency and Reduced Output Ripple Current," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 5, pp. 3587–3594, 2017.

[10] J.-M. Choi, B.-J. Byen, Y.-J. Lee, D.-H. Han, H.-S. Kho, and G.-H. Choe, "Design of Leakage Inductance in Resonant DC-DC Converter for Electric Vehicle Charger," *IEEE Transactions on Magnetics*, vol. 48, no. 11, pp. 4417–4420, 2012.

[11] Y. Du, S. Baek, S. Bhattacharya, and A. Q. Huang, "High-voltage high-frequency transformer design for a 7.2kV to 120V/240V 20kVA solid state transformer," *IECON 2010 - 36th Annual Conference on IEEE Industrial Electronics Society*, 2010.

[12] J. Ferrell, J.-S. Lai, T. Nergaard, X. Huang, L. Zhu, and R. Davis, "The role of parasitic inductance in high-power planar transformer design and converter integration," *Nineteenth Annual IEEE Applied Power Electronics Conference and Exposition, 2004. APEC 04.*

[13] A. Jahromi, J. Faiz, and H. Mohseni, "Calculation of distribution transformer leakage reactance using energy technique," *J. Faculty Eng.*, vol. 38, no. 3, pp. 395–403, Sep. 2004.

[14] P. Dowell, "Effects of eddy currents in transformer windings," *Proceedings of the Institution of Electrical Engineers*, vol. 113, no. 8, p. 1387, 1966.

[15] W. Hurley and D. Wilcox, "Calculation of leakage inductance in transformer windings," *IEEE Transactions on Power Electronics*, vol. 9, no. 1, pp. 121–126, 1994.

[16] M. A. Bahmani and T. Thiringer, "Accurate Evaluation of Leakage Inductance in High-Frequency Transformers Using an Improved Frequency-Dependent Expression," *IEEE Transactions on Power Electronics*, vol. 30, no. 10, pp. 5738–5745, 2015.

[17] Z. Ouyang, J. Zhang, and W. G. Hurley, "Calculation of Leakage Inductance for High-Frequency Transformers," *IEEE Transactions on Power Electronics*, vol. 30, no. 10, pp. 5769–5775, 2015.

[18] M. Mogorovic and D. Dujic, "100 kW, 10 kHz Medium-Frequency Transformer Design Optimization and Experimental Verification," *IEEE Transactions on Power Electronics*, vol. 34, no. 2, pp. 1696–1708, 2019.

[19] M. Mogorovic and D. Dujic, "Sensitivity Analysis of Medium-Frequency Transformer Designs for Solid-State Transformers," *IEEE Transactions on Power Electronics*, vol. 34, no. 9, pp. 8356–8367, 2019.

[20] T. Hatakeyama, N. Kurita, and M. Kimura, "Prototyping of 500 kVA Medium Frequency Transformer for Offshore Direct-Current Collection Grid," *2018 International Power Electronics Conference (IPEC-Niigata 2018 -ECCE Asia)*, 2018.

[21] F. Hoffmann, L. Camurca, and M. Liserre, "Modular EV Fast Charging Station Architectures based on Multiphase-Medium-Frequency Transformer," *IECON 2018 - 44th Annual Conference of the IEEE Industrial Electronics Society*, 2018.

[22] A. Ghazanfari, C. Perreault, and K. Zaghib, "EV/HEV Industry Trends of Wide-bandgap Power Semiconductor Devices for Power Electronics Converters," *2019 IEEE 28th International Symposium on Industrial Electronics (ISIE)*, 2019.

[23] V. Sangwan, C. M. Tan, D. Kapoor, and H.-C. Chiu, "Electromagnetic Induced Failure in GaN-HEMT High Frequency Power Amplifier," *IEEE Transactions on Industrial Electronics*, pp. 1–1, 2019.

[24] F. M. Shah, H. M. Xiao, R. Li, M. Awais, G. Zhou, and G. T. Bitew, "Comparative performance evaluation of temperature dependent characteristics and power converter using GaN, SiC and Si power devices," *2018 IEEE 12th International Conference on Compatibility, Power Electronics and Power Engineering*, 2018.

[25] L. Dalessandro, F. D. S. Cavalcante, and J. W. Kolar, "Self-Capacitance of High-Voltage Transformers," *IEEE Transactions on Power Electronics*, vol. 22, no. 5, pp. 2081–2092, 2007.

[26] D. Fu, P. Kong, F. C. Lee, and S. Wang, "Novel techniques to suppress the common mode EMI noise caused by transformer parasitic capacitances in DC-DC converters," *2010 IEEE Energy Conversion Congress and Exposition*, 2010.

[27] M. A. Bahmani, T. Thiringer, and M. Kharezy, "Optimization and experimental validation of medium-frequency high power transformers in solid-state transformer applications," *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2016.

[28] K. Mainali, S. Madhusoodhanan, A. Tripathi, K. Vechalapu, A. De, and S. Bhattacharya, "Design and evaluation of isolated gate driver power supply for medium voltage converter applications," *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2016.

[29] M. K. Kazimierczuk, *High-frequency magnetic components*. Chichester: John Wiley & Sons, 2014.

[30] *IEEE Standard for General Requirements for Dry-Type Distribution and Power Transformers*, IEEE Standard C57.12.01-2015 (Revision of IEEE Standard C57.12.01-2005), 2015.

II. EMC IMPROVEMENT FOR HIGH VOLTAGE PULSE TRANSFORMERS BY PARETO-OPTIMAL DESIGN OF GEOMETRY STRUCTURE BASED ON PARASITIC ANALYSIS AND EMI PROPAGATION

ABSTRACT

High voltage pulse transformers have an essential role in pulsed power systems and power conversion applications. Improving the electromagnetic behavior of such devices leads to better efficiency and low-level electromagnetic interference (EMI) noise propagation in systems. In this paper, a high voltage pulsed power system is considered and analyzed to improve the electromagnetic compatibility (EMC). The new generation of pulsed power systems that use SiC and GaN fast switches in capacitor charger power electronic circuit, face far more EMI challenges. Moreover, in this paper, the EMI propagation paths in the pulsed power system are realized and analyzed. The EMI noise level of the system is obtained and compared to the IEC61800-3 standard. To improve the EMC, the parasitic parameters of the transformer, as the main path of EMI circulation, are optimized to block the EMI propagation in the pulsed power system. For this aim, the parasitics are modeled and calculated with a novel and accurate energy distribution model. Then, by defining a cost function the geometry structure of the transformer is optimized to lower the parasitics in the system. Three pareto-optimal techniques are investigated for the cost function optimization. The models and results are verified by 3D-finite element method (FEM) and experimental results for several given scenarios. FEM and experimental verifications of this model, make the model suitable for any desirable design

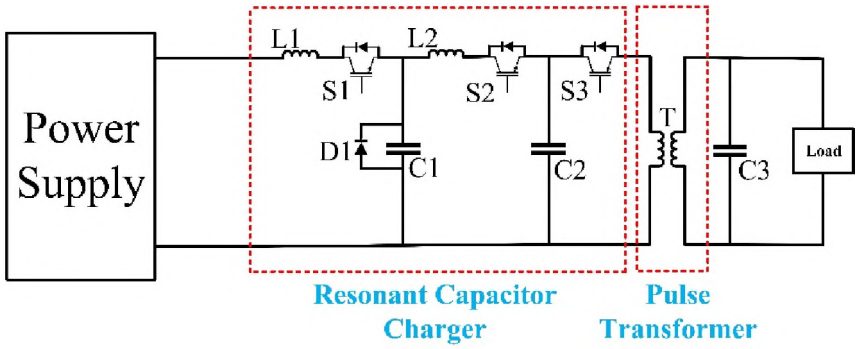
in any pulsed power systems. Finally, the EMI noise level of the system after optimization is shown and compared to the IEC61800-3 standard.

1. INTRODUCTION

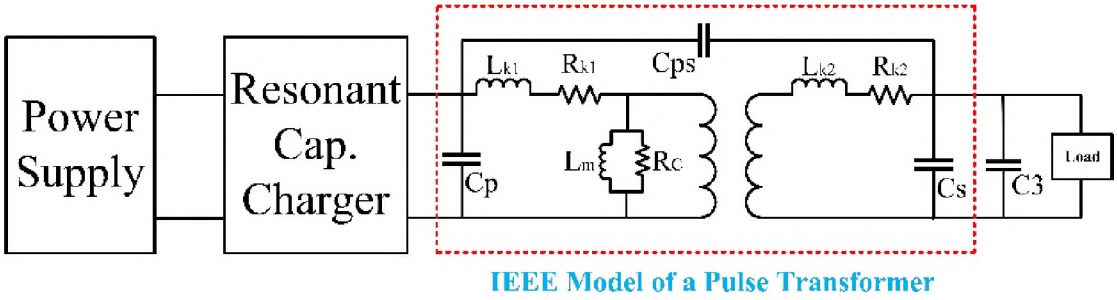
The performance and efficiency of pulsed power generators and power conversion systems are highly dependent on the parasitic parameters and noise level of the whole system. In power conversion systems that include HV transformers and magnetic parts, leakage inductance and parasitic capacitance values affect the losses, noise, and control of the system [1] due to creating EMI propagation paths in the system. Calculating and/or adjusting the values for the parasitic parameters not only increases the efficiency and helps to reduce the size of passive components, but also can lead to more robust control strategies [2]. Leakage inductance results from an imperfect magnetic coupling between the primary and secondary of a transformer. Due to eddy currents and proximity effect, as the frequency increases, the concentration of current on the skin of the conductor increases. This phenomenon, called skin effect, leads to a lower leakage inductance. Hence, calculating the exact values of leakage inductance in pulsed power applications and high frequency (HF) systems such as resonant capacitor chargers should be different from calculating the values in 50/60 Hz systems [3], [4]. In [5], by using leakage inductance for zero voltage switching (ZVS) and zero current switching (ZCS), the total volume of the system decreased up to 15%. Also, by adjusting the resonant frequency to 1.25 times of the switching frequency, 30% loss saving was observed when compared to the hard switching. These power electronics converters are very useful in charging the capacitances of the pulse

generators. On the other hand, higher values of leakage inductance lead to reactive power circulation in the system and efficiency reduction [6], [7]. Thus, creating a robust magnetic coupling between the primary and the secondary by devising a suitable winding arrangement and structure for the transformer is crucial. Additionally, in applications with phase shift modulations, such as the HF isolation stage of multi-level converters, there is a minimum leakage inductance needed for the proper operation of the phase-shift modulation strategy to achieve ZVS [8]-[11]. All the aforementioned reasons and applications emphasize the necessity of an accurate calculation method for leakage inductance in pulse transformers and high frequency transformers (HFTs), and HF systems that used in pulsed power applications.

Parasitic capacitances in the system exist due to the electric field distribution among different parts of the transformer. The nonlinearity of the electric field distribution makes the capacitance modeling more difficult [12], [13]. Calculating the parasitic capacitance in the magnetic parts of the system can allow for the integration of parasitic capacitance into the ZVS and ZCS tanks, or to minimize the parasitic capacitance, thus reducing common mode (CM) EMI noise and losses [14]-[17]. In new switches such as SiC and GaN, which demonstrate a short rising and falling time, the dV/dt can reach anywhere between 30-100 kV/μs [18]. This large amount of dV/dt can cause the injection of HF currents through the series parasitic capacitances of pulse transformers/HFTs and lead to EMI [19] and change the output pulse waveform due to resonance with inductor parts. Parasitic capacitance values are directly related to the transformer winding arrangements and core structure. Changing the arrangements and structure lead to an optimized value for the capacitances.



(a)



(b)

Figure 1. Pulsed power system.

In [20] and [21], the leakage inductance for an EE core transformer is calculated by using Maxwell equations without taking the frequency into account. Simplifying the Maxwell equations and neglecting the frequency dependent leakage inductance lead to simple equations. Also, in [22], by using Biot Savart law and calculating the magnetic field, in some parts of an EE core a more accurate expression for leakage inductance is presented. Moreover, a more accurate modeling of winding arrangements is presented in [23]. All the methods used in [20]-[23] present simplified equations and frequency independent expressions, which make them inaccurate for many HF and pulsed applications.

In [24], a frequency-dependent method that uses time variant Maxwell equations is introduced to provide an expression for leakage inductance, but the proposed method and

expression are suitable for toroidal cores, not EE cores. Moreover, in both [25] and [26] a frequency dependent method that solves time variant Maxwell equations is used to calculate leakage inductance for an EE core in any frequency. However, in both [25] and [26], due to using 2D FEM and low turn prototypes, the accuracy and validation for high power applications with a large number of turns per winding are not totally clear. Also, in [25] and [26], Maxwell equations are solved only for an arrangement in which both windings are wound on each other.

Two effective methods, namely measurements and FEM, are used to find the exact amounts of parasitic capacitance. However, for optimizing the parasitic values, obtaining an analytical method for finding capacitance is necessary. In [27]-[33], different methods of finding analytical expressions are investigated for parasitic capacitance in transformers used in power converters. Also, in [27] the orthogonal, orthocyclic, and plate winding arrangements of an HFT are considered. Moreover, in [28], a semi-analytical method using FEM is proposed with disordered winding arrangements. Because of the winding and insulation complexity in high voltage transformers, finding the capacitance by analytical methods is more difficult. In [29] and [30], the capacitance of high voltage transformers with different complex windings are investigated.

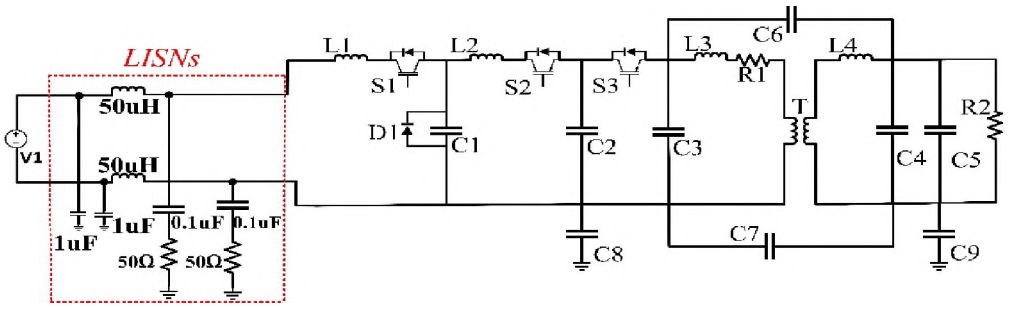


Figure 2. LTspice Simulation model.

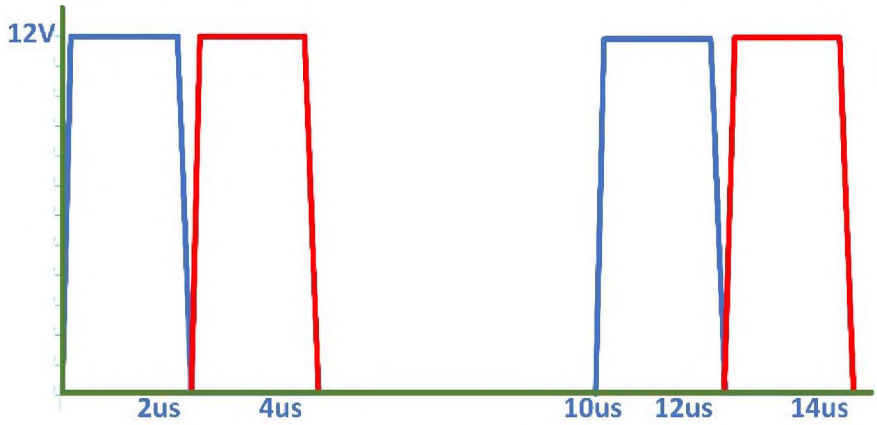


Figure 3. Gate signals of S1 (blue) and S2 (red) for switches gate drivers.

In this paper, a pulsed power system is analyzed and the EMI propagation routes are investigated. In addition, the EMI noise level of the system is shown. For improving the EMC and reducing the EMI noise level under IEC61800-3 limits, transformer parasitic parameters are modeled to be optimized and block the EMI circulation. Transformer parasitics provide the main path for CM EMI circulation. Novel analytical and FEM methods are proposed for both leakage inductance and parasitic capacitance. Additionally, different pareto-optimal techniques are implemented into the defined cost function for achieving the best combination of parasitic parameters. FEM analysis and experimental results are used to verify the model. The winding arrangement and structure for FEM and experimental verifications are chosen due to the previous research in this field [34], which proved that this structure is the best, both in terms of leakage inductance and parasitic capacitance for some applications. At the end, it is shown that, after optimization, the CM EMI noise level of the system is decreased significantly and placed in a good agreement with IEC61800-3 standard.

2. PULSED POWER SYSTEM AND EMI NOISE LEVEL

Figure 1(a) shows a pulse generation system that derived from [35]. This system implemented in [35] with SiC power electronics switches for a high voltage pulse level of 20kV. Figure 1(b) shows the standard model of a pulse transformer in the pulsed power system of Figure 1(a). The EMI noise in this system propagates through interwinding and intra-winding parasitic capacitances. Also, leakage inductances not only affect the EMI propagations paths, but also affect the output pulse voltage by resonance with the capacitors.

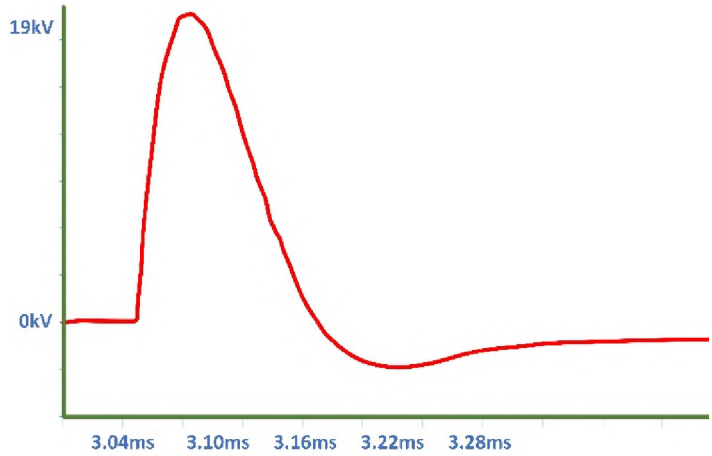


Figure 4. Generated pulse.

To show how the parasitics affect the EMC, Figure 1(a) system is simulated in LTspice and the CM EMI noise level of the system is obtained here. Figure 2 shows simulations schematic developed in this paper. As is clear in Fig 2, two-line impedance stabilization networks (LISNs) are also simulated and shown for receiving the EMI noise.

Figure 3 shows the gate signals of S1 and S2 of Figure1(a) that shows how the switches drive for charring C1 and C2 capacitors. Figure 4. shows the pulse signal created by the HV pulse transformer. Moreover, Figure 5 shows the EMI noise level of the simulated pulsed power system. As is clear in this figure, at the frequency of 330kHz and above, the noise level is higher than 73dB(uV), which is not in agreement with IEC61800-3 standard. Therefore, EMC improvement is necessary and optimizing the parasitics and the structure of HV transformer and winding configurations is the key for lowering the EMI under the limits of IEC61800-3 standard. Furthermore, Figure 6 shows the EMI propagation paths in the pulsed power system.

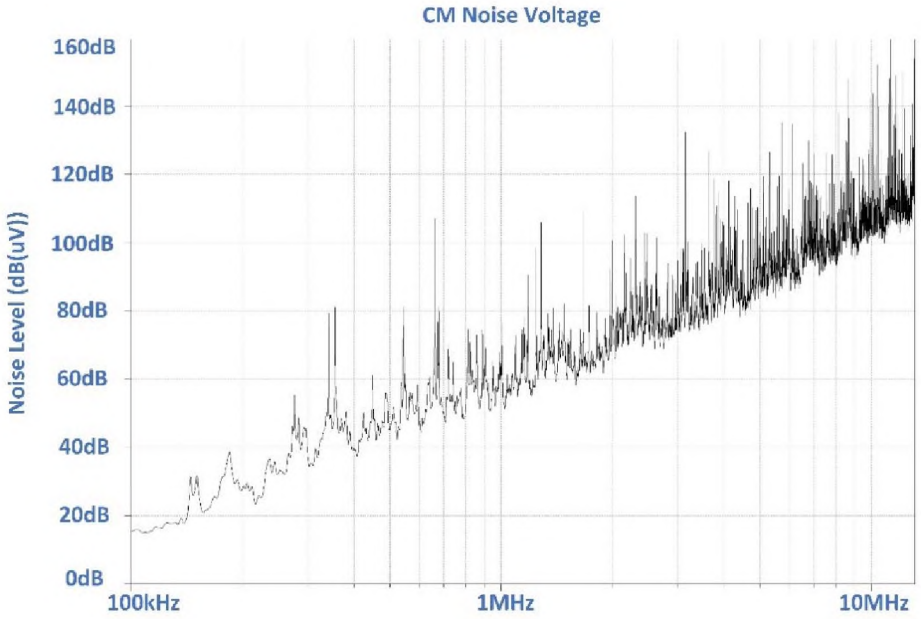


Figure 5. EMI noise level of the pulsed power system.

Figure 6 shows that the EMI noise propagates through the parasitics of the elements such as inductors, switches, and transformer and close itself by the parasitic capacitances

between the circuit and the ground. This paper focuses on attenuating the CM EMI noise by optimizing the transformer elements, which play significant roles in EMI propagations. At the end it will be shown that, the transformer optimization could lower the EMI noise under the IEC61800-3 limits and effectively block the EMI circulating in the system. Optimizing the parasitics in other elements, putting EMI filter in the system, or using passive components for EMI noise attenuating are also effective; however, are not the interest of this paper.

3. LEAKAGE INDUCTANCE CALCULATIONS

By short circuiting the secondary, the energy remaining in the space--mainly in the window areas--is equal to the leakage energy, and the leakage inductance can be calculated. Thus, calculating the leakage energy on different parts of the transformer is the main solution for finding the leakage inductance. However, the energy distribution can be different in various models. This paper introduces a novel and accurate energy distribution model for finding the leakage values.

Figure 7 shows the 2D conductor arrangements options of the transformer at the right window. The left window has a symmetrical arrangement. The number of conductors per layer for the primary and secondary is n_1 and n_2, respectively. Also, the number of layers for the primary and secondary is m_1 and m_2, respectively.

To find the total leakage magnetic energy, it is necessary to calculate the leakage energy on the insulations, the bobbin spacer, and the conductors. The magnetic field on the insulations and the spacer is constant. However, the magnetic field inside the conductors

changes linearly with respect to the conductor radius and nonlinearly in presence of skin effect.

Before discussing the distributed magnetic energy on different parts of the transformer, following coefficients are defined:

$$K_p = \frac{1}{2}\int_0^{MLT_{pri}} \int_0^{w} \mu . d\ell . dr \tag{1}$$

$$K_s = \frac{1}{2}\int_0^{MLT_{sec}} \int_0^{w} \mu . d\ell . dr \tag{2}$$

$$K_{spacer} = \frac{1}{2}\int_0^{MLT_{spc}} \int_0^{w} \mu . d\ell . dr \tag{3}$$

where MLT_{pri},MLT_{sec},MLT_{spc}, and μ are mean length turn of primary, mean length turn of secondary, mean length turn of the spacer between primary and secondary, and absolute permeability, respectively.

Magnetic energy on the insulation parts is discussed in [34]. However, for a better accuracy the following energy distribution in the insulation parts of the conductors of the primary and secondary is described as follows. The following model is more accurate than the model described in [34].

$$E_{ins_{primary}} = K_p \sum_{j=1}^{m_1-1} \sum_{i=1}^{n_1-1} \int_0^{t_{ins_{pri}}} \left(\frac{ijI_{primary}}{2\pi t_{ins_{pri}}}\right)^2 dx \tag{4}$$

$$E_{ins_{secondary}} = K_s \sum_{j=1}^{m_2-1} \sum_{i=1}^{n_2-1} \int_0^{t_{ins_{sec}}} \left(\frac{ijI_{secondary}}{2\pi t_{ins_{sec}}}\right)^2 dx \tag{5}$$

Moreover, magnetic energy on the spacer that is between the windings is described as follows. The following model is more accurate than the model described in [34].

$$E_{spacer} = K_{spacer} \sum_{j=1}^{m_1} \sum_{i=1}^{n_1} \int_0^{t_{spc}} \left(\frac{ijI_{primary}}{2\pi w}\right)^2 dx \tag{6}$$

In (4), (5), and (6) $t_{ins_{pri}}$,$t_{ins_{sec}}$, and t_{spc} are insulation thickness between primary

conductors, insulation thickness between secondary conductors, and insulation thickness of the spacer, respectively.

To find the magnetic energy inside the conductors, by using the Maxwell equations and the procedure described in [34], the following equation should be solved:

$$\frac{\partial^2 H}{\partial x^2} = j(2\pi f)\mu\sigma H \tag{7}$$

where H, σ, and f are magnetic field strength, electric conductivity, and frequency respectively. Also, the skin depth is necessary to be defined here:

$$\delta = \frac{\sqrt{2}}{\sqrt{2\pi f \mu\sigma}} \tag{8}$$

As is clear in this equation, by increasing the frequency, the skin depth, which shows the penetration of current inside a conductor, decreases. In other words, the skin effect intensifies.

Magnetic energy on the primary winding parts is discussed in [34]. However, for a better accuracy the following energy distribution is described as follows. The following model is more accurate than the model described in [34]. Therefore, the magnetic energy on the primary windings can be calculated:

$$E_{primary} = n_1 K_p \left[\frac{H_{11}^2}{2\left(\frac{1+j}{\delta}\right)} \left(e^{2\left(\frac{1+j}{\delta}\right) t_{cond_{pri}}} - 1 \right) - \frac{H_{21}^2}{2\left(\frac{1+j}{\delta}\right)} \left(e^{-2\left(\frac{1+j}{\delta}\right) t_{cond_{pri}}} - 1 \right) + 2H_{11}H_{21}(t_{cond_{pri}}) \right] \tag{9}$$

By following the same steps as the primary, the magnetic energy for the secondary is calculated. The following model is more accurate than the model described in [34]:

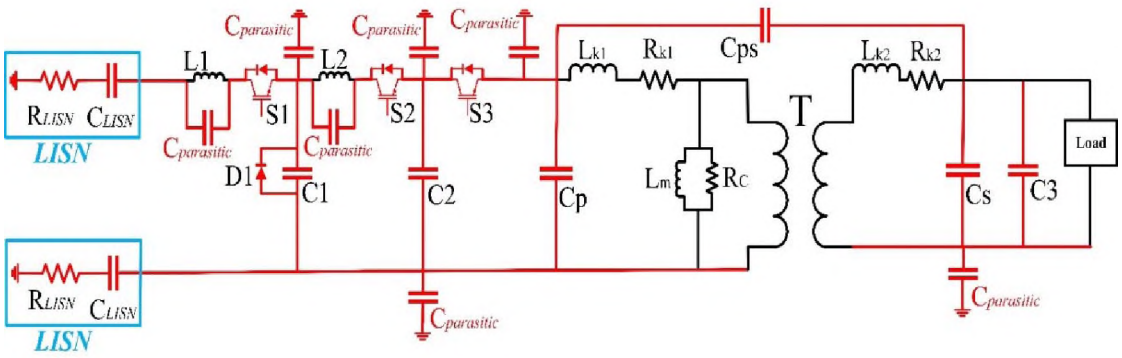
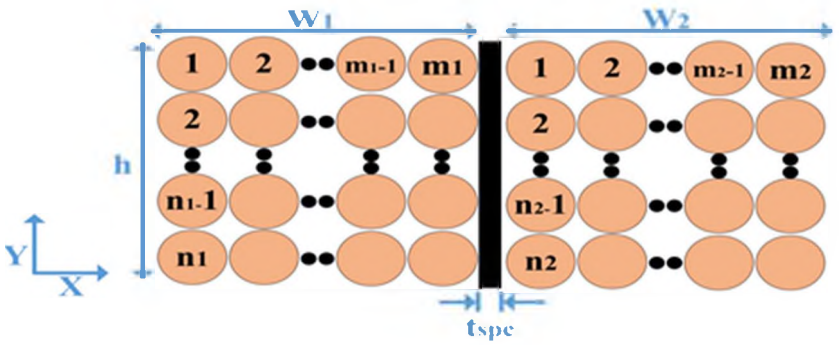
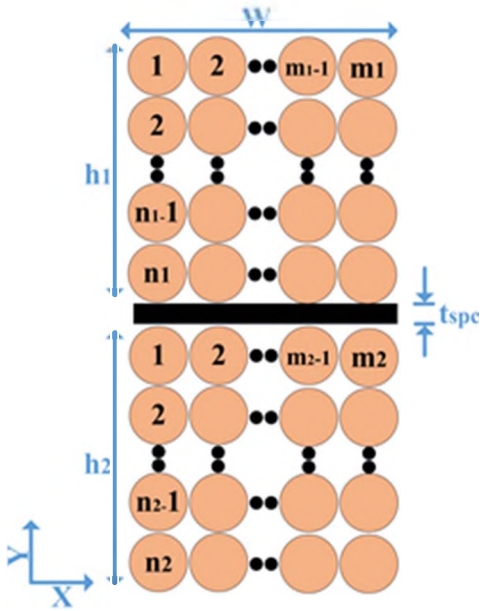


Figure 6. EMI propagation paths in the pulsed power system (red routes).



(a)



(b)

Figure 7. Conductor arrangements in right window. a) arrangement a. b) arrangement b.

$$E_{secondary} = n_2 K_s \left[\frac{H_{12}^2}{2\left(\frac{1+j}{\delta}\right)} \left(e^{2\left(\frac{1+j}{\delta}\right) t_{cond_{sec}}} - 1 \right) - \frac{H_{22}^2}{2\left(\frac{1+j}{\delta}\right)} \left(e^{-2\left(\frac{1+j}{\delta}\right) t_{cond_{sec}}} - 1 \right) + 2H_{12}H_{22}(t_{cond_{sec}}) \right] \quad (10)$$

Detailed procedure of finding H_{11}, H_{21}, H_{12}, and H_{22} coefficients is discussed in [34]. $t_{cond_{pri}}$ and $t_{cond_{sec}}$ are the primary and the secondary conductor thicknesses, respectively.

As a result, the leakage inductance is achieved by the following equation and using the energy method:

$$L_{leakage\ inductance} = \frac{2(E_{ins_{primary}} + E_{ins_{secondary}} + E_{spacer} + E_{primary} + E_{secondary})}{I_{primary}^2} \quad (11)$$

4. CAPACITANCE CALCULATIONS

There are several parasitic capacitance values in a transformer structure. The number of parasitic values depend on the conductivity of the core. If the core is conductive, there are more parasitic values, which are placed between the core and the windings. In this section, scenarios of both conductive and nonconductive cores are investigated to calculate the parasitic capacitances. Figure 8 illustrates some of the parasitic capacitances in the right window of the transformer; the left window has a symmetric distribution. The rest of the parasitic capacitances are represented in Figure 9 (inter-winding and intra-winding capacitances). If the core is conductive, the parasitic values of both Figure 8 and Figure 9 should be considered, but for a nonconductive core, only the parasitic values of Figure 9 should be taken into account.

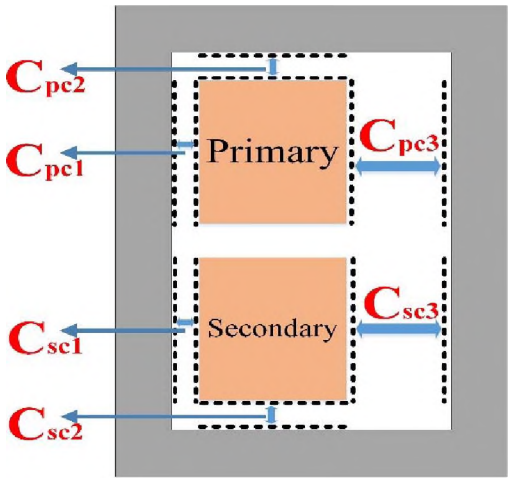


Figure 8. Parasitic capacitances between windings and a conductive core.

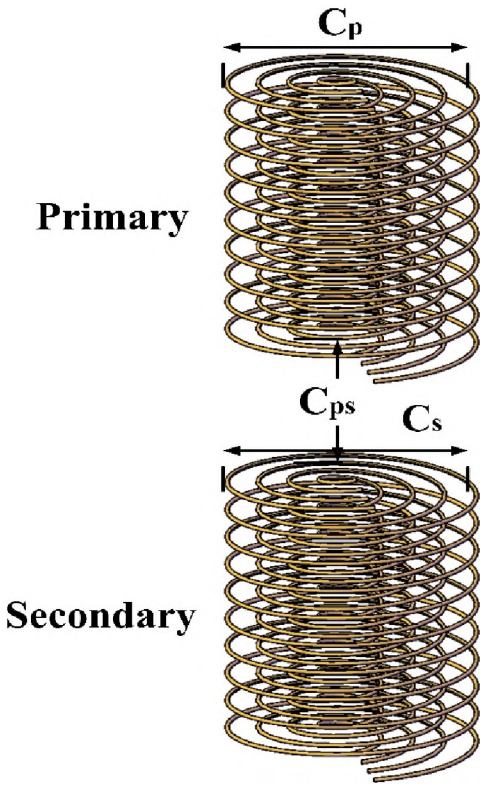


Figure 9. Inter-winding (Cps) and intra-winding (Cp and Cs) capacitances.

To find the parasitic capacitances, the energy method is used. The following equations describe the parasitic capacitances of Figure 8 and Figure 9:

$$E_{total\ stored\ energy} = \frac{1}{2}\sum_{i=1}^{m_1} C_{pc1i}\left(V_{p_{mi}} - V_c\right)^2 = \frac{1}{2}C_{pc1}(V_p - V_c)^2 \quad (12)$$

$$V_{p_{mi}} = \frac{V_p}{m_1} \quad (13)$$

$$C_{pc1i} = \frac{\varepsilon D_{core} n_1 t_{cond_{pri}}}{t_B + t_{ins_{pri}} + (i-1)t_{cond_{pri}}} \quad (14)$$

$$C_{pc1} = \frac{\sum_{i=1}^{m_1} C_{pc1i}\left(V_{p_{mi}} - V_c\right)^2}{(V_p - V_c)^2} \quad (15)$$

$$V_{p_{ni}} = \frac{V_p}{n_1} \quad (16)$$

$$C_{pc2i} = \frac{\varepsilon D_{core} m_1 t_{cond_{pri}}}{t_B + t_{ins_{pri}} + (i-1)t_{cond_{pri}}} \quad (17)$$

$$C_{pc2} = \frac{\sum_{i=1}^{n_1} C_{pc2i}\left(V_{p_{ni}} - V_c\right)^2}{(V_p - V_c)^2} \quad (18)$$

$$C_{pc3i} = \frac{\varepsilon D_{core} n_1 t_{cond_{pri}}}{w - t_B - i t_{cond_{pri}} + t_{ins_{pri}}} \quad (19)$$

$$C_{pc3} = \frac{\sum_{i=1}^{m_1} C_{pc3i}\left(V_{p_{mi}} - V_c\right)^2}{(V_p - V_c)^2} \quad (20)$$

$$V_{s_{mi}} = \frac{V_s}{m_2} \quad (21)$$

$$C_{sc1i} = \frac{\varepsilon D_{core} n_2 t_{cond_{sec}}}{t_B + t_{ins_{sec}} + (i-1)t_{cond_{sec}}} \quad (22)$$

$$C_{sc1} = \frac{\sum_{i=1}^{m_2} C_{sc1i}\left(V_{s_{mi}} - V_c\right)^2}{(V_s - V_c)^2} \quad (23)$$

$$V_{s_{ni}} = \frac{V_s}{n_2} \quad (24)$$

$$C_{sc2i} = \frac{\varepsilon D_{core} m_2 t_{cond_{sec}}}{t_B + t_{ins_{sec}} + (n_2 - i)t_{cond_{sec}}} \quad (25)$$

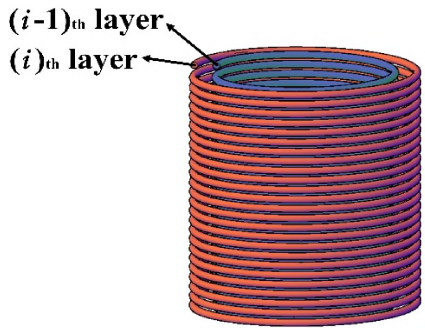
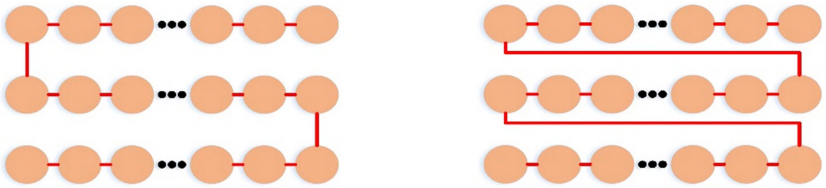


Figure 10. Two successive layers.



(a) (b)

Figure 11. Conductor winding arrangement. a) Winding arrangement type I. b) Winding arrangement type II.

$$C_{sc2} = \frac{\sum_{i=1}^{n_2} C_{sc2i}\left(V_{s_{ni}} - V_c\right)^2}{(V_s - V_c)^2} \tag{26}$$

$$C_{sc3i} = \frac{\varepsilon D_{core} n_2 t_{cond_{sec}}}{w - t_B - i t_{cond_{sec}} + t_{ins_{sec}}} \tag{27}$$

$$C_{sc3} = \frac{\sum_{i=1}^{m_2} C_{sc3i}\left(V_{s_{mi}} - V_c\right)^2}{(V_s - V_c)^2} \tag{28}$$

To find the interwinding capacitance (C_{ps}), the detailed procedure is explained in [34]. By following the method described in [34], C_{ps} can be found:

$$C_{psij} = \frac{\varepsilon\pi\left[\left(\frac{D_{core}}{2} + t_B + m_1 t_{cond_{pri}}\right)^2 - \left(\frac{D_{core}}{2} + t_B\right)^2\right]}{(n_1 - i) t_{cond_{pri}} + (j-1) t_{cond_{sec}} + t_{ins_{pri}} + t_{ins_{sec}} + t_B} \tag{29}$$

$$C_{ps} = \sum_{i=1}^{n_1} \sum_{j=1}^{n_2} C_{p_i s_j} \left(\frac{1}{n_1^2} + \frac{1}{N^2 n_1^2} + \frac{2}{N n_1 n_2}\right) \tag{30}$$

where D_{core}, t_B, N, V_p, V_s, and V_c are core depth, thickness of bobbin, turn ratio, primary voltage, secondary voltage, and core voltage, respectively. Note that, t_B and t_{spc} are equal, here. V_c can be calculated by the numeric methods such as FEM.

To find C_p and C_s, using the parallel plate method is not accurate enough. In order to find these parameters, it is important to note that due to the small voltage increase per turn, the stored energy between adjacent conductors in a given layer is negligible, and the main stored energy is between two adjacent layers. Therefore, by considering the layers to be cylindrical shapes and the winding conductors to be orthogonal shapes, as shown in Figure 10, the capacitance and the stored energy between any arbitrary two layers can be calculated. Using the energy technique, the capacitance between each two successive layers of the primary is:

$$C_{p,layer,i} = \frac{2\varepsilon\pi n_1 t_{cond_{pri}}}{\ell n\left(\frac{\frac{D_{core}}{2}+t_B+i.t_{cond_{pri}}}{\frac{D_{core}}{2}+t_B}\right)}, \quad 2 \le i \le m_1 \tag{31}$$

Hence, the energy between the i_{th} and $i-1_{th}$ layers will be:

$$E_{layer(i,i-1)} = \frac{1}{2} C_{p,layer,i} V_{p,i,i-1}^2 \tag{32}$$

$$V_{p,i,i-1} = V_{p,i} - V_{p,i-1} \tag{33}$$

The voltage between each two successive layers ($V_{p,i,i-1}$) depends on the winding arrangement direction. In many applications, the winding arrangement direction of type I, which is shown in Figure 11(a), is desirable. However, in some high voltage/power applications, in order to reduce the tension between the layers and to decrease the insulation requirement, type II, which is shown in Figure 11(b), is preferable to type I.

$$V_{p,i,i-1} = \begin{cases} \frac{2V_{primary}}{m_1}, & widing\ arrangement\ type\ I \\ \frac{V_{primary}}{m_1}, & widing\ arrangement\ type\ II \end{cases} \quad (34)$$

Equation (35) represents the energy equation in the primary:

$$\frac{1}{2}C_p V_p^2 = \frac{1}{2}\sum_{i=2}^{m_1} C_{p,layer,i}\, V_{p,i,i-1}^2 \quad (35)$$

Therefore, the primary winding capacitance, C_p, is:

$$C_p = \begin{cases} \sum_{i=2}^{m_1} \frac{4C_{p,layer,i}}{m_1^2}, & widing\ arrangement\ type\ I \\ \sum_{i=2}^{m_1} \frac{C_{p,layer,i}}{m_1^2}, & widing\ arrangement\ type\ II \end{cases} \quad (36)$$

Note that in cases with one-layer winding ($m_1 = 1$), if the core is conductive, then there is a parasitic capacitance between the winding and the core, which can be defined as:

$$C_{p,m1=1} \approx 4C_{pc1} \quad (37)$$

Equation (37) assumes that the core depth (D_{core}) is equal to the middle leg width (MLW). By following the steps taken for finding C_p, the capacitance of secondary winding, C_s, can be calculated by (38)-(40):

$$C_{s,layer,i} = \frac{2\varepsilon\pi n_2 t_{cond_{sec}}}{\ell n\left(\frac{\frac{D_{core}}{2}+t_B+i.t_{cond_{sec}}}{\frac{D_{core}}{2}+t_B}\right)},\ 2 \le i \le m_2 \quad (38)$$

$$V_{s,i,i-1} = \begin{cases} \frac{2V_{secondary}}{m_2}, & widing\ arrangement\ type\ I \\ \frac{V_{secondary}}{m_2}, & widing\ arrangement\ type\ II \end{cases} \quad (39)$$

$$C_s = \begin{cases} \sum_{i=2}^{m_2} \frac{4C_{s,layer,i}}{m_2^2}, & widing\ arrangement\ type\ I \\ \sum_{i=2}^{m_2} \frac{C_{s,layer,i}}{m_2^2}, & widing\ arrangement\ type\ II \end{cases} \quad (40)$$

with the same assumption as the primary winding, the one-layer winding capacitance between the secondary and the conductive core is:

$$C_{s,m2=1} \approx 4C_{sc1} \quad (41)$$

by finding all the parasitic parameters of a transformer, the following expressions, which are the total parasitic capacitances, can be defined as:

$$C_{parasitic} = 2\left[\frac{(C_{pc1}+C_{pc2}+C_{pc3})(C_{sc1}+C_{sc2}+C_{sc3})}{C_{pc1}+C_{pc2}+C_{pc3}+C_{sc1}+C_{sc2}+C_{sc3}}\right] + C_{ps} \quad (42)$$

$$C_T = C_{parasitic} + C_p + C_s \quad (43)$$

5. TRANSFORMER STRUCTURE OPTIMIZATION

By using the parasitic parameter equations, the optimal transformer structure dimensions can be found. The optimal dimensions minimize both the leakage inductance and the parasitic capacitance of a transformer. With this in mind, the cost function of (44) is defined as:

$$f_c = \alpha\frac{L_{leakage}}{L_{base}} + (1-\alpha)\frac{C_T}{C_{base}}, \quad 0 \le \alpha \le 1 \quad (44)$$

where $L_{leakage}$ and C_T are given in mH and pF, respectively. L_{base} and C_{base} are 1mH and 1pF, respectively. Equations (45), (46) describe other parts of the transformer structure that were mentioned in the analytical models discussed in sections 3 and 4:

$$D_{core} = MLW = 10t_B = 30\ mm \quad (45)$$

$$t_{ins_{pri}} = t_{ins_{sec}} = 0.15t_{cond_{pri}} \quad (46)$$

Pareto-optimal technique can be performed under a variety of constraints including but not limited to:

I) a fixed number of turns as the window area changes

II) a fixed window area while the number of turns is constant

III) a fixed utilization factor (i.e. the number of turns is a linear function of the window area).

These constraints are studied in this section. The selection of the constraint depends on the topology and application of the power converter. By assuming the conditions of equations (45), (46) the f_c-w- α and f_c-w- h graphs for conductive and nonconductive cores can be shown when the window area or/and number of turns are fixed. Figure 12 shows the f_c-w- α graphs for the number of turns of 400 and 450 with the window area of 1800mm^2.

Furthermore, by changing w and h, the cost function changes. Figure 13 shows the f_c-w- h graphs for conductive and nonconductive cores when the number of turns and α are constant. Figure 13 is obtained by considering the number of turns 400 and 450 and α equals to 0.5. Moreover, Figure 14 shows the cost function variations for conductive and nonconductive cores when w, h and the number of turns change and α equals to 0.5. In Figure 13, as the width and height of the window area increase, the number of turns increase by the filling utilization factor, which is defined by equation (47):

$$FUF = \frac{w_i h_i}{w_{i-1} h_{i-1}} \tag{47}$$

Figures 12-14 show that for a fixed number of turns, which is a fixed magnetizing inductance and/or a fixed window area, changing the parameters can lead to an optimal design for the transformer structure. Also, for a fixed filling utilization factor of the window area, which leads to the different number of turns and magnetizing inductance, by changing the parameters, the optimal values can be found. Each of the two aforementioned strategies can be used for designing optimal HFTs/pulse transformers with lower parasitic parameters.

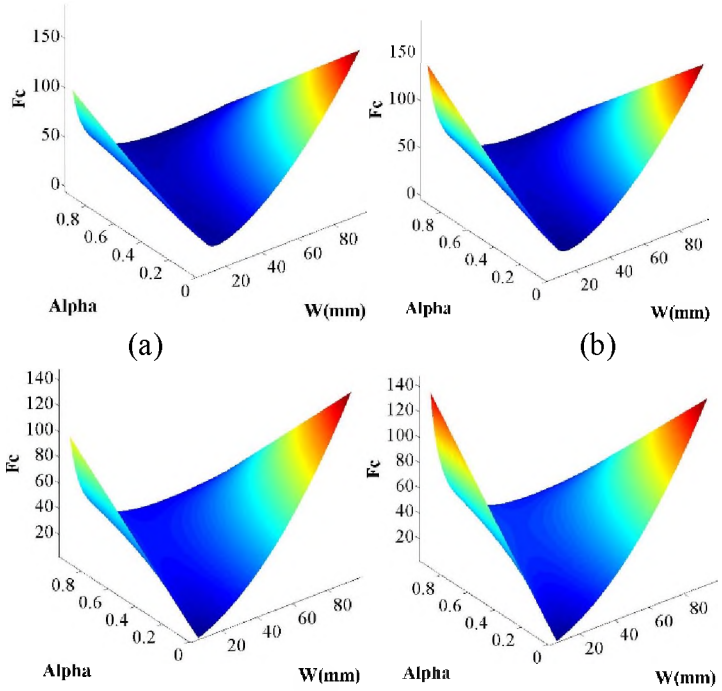


Figure 12. f_c-w- α graphs. a) Conductive core, N=400. b) Conductive core, N=450. c) Nonconductive core, N=400. d) Nonconductive core, N=450.

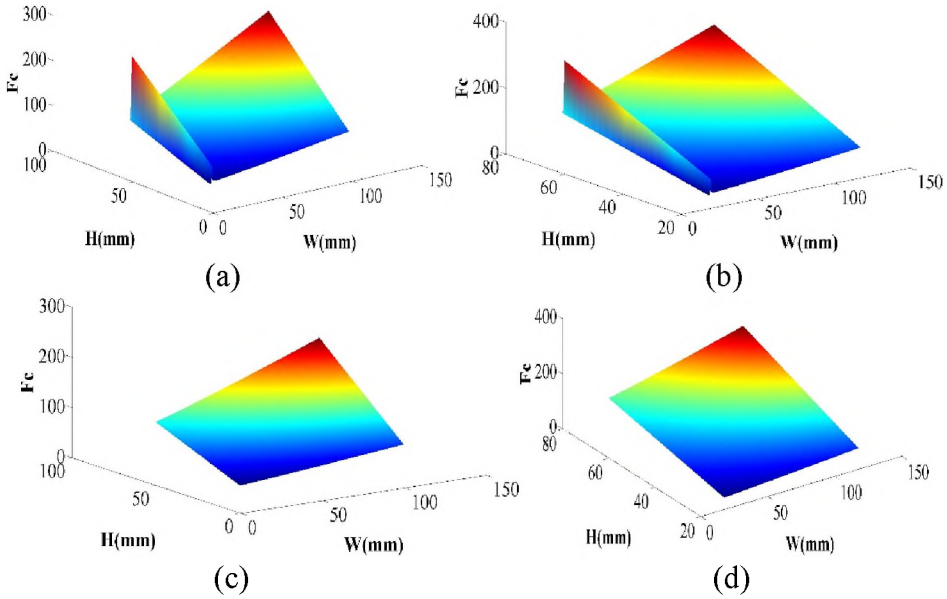
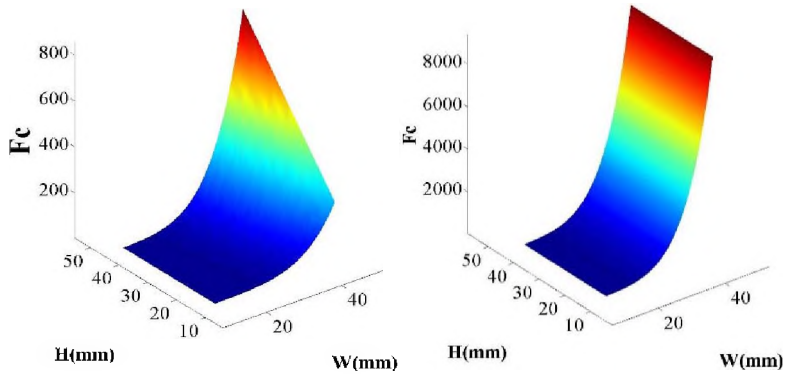


Figure 13. f_c-w- h graphs. a) Conductive core, N=400. b) Conductive core, N=450. c) Nonconductive core, N=400. d) Nonconductive core, N=450.

The optimization based on the three mentioned strategies is performed to design winding arrangement, geometry structure, and number of turns so that the defined cost function minimized. For the first optimization strategy, first the alpha parameter should be set based on the system/converter that this HF transformer is going to work on. Then based on the number of turns and window area the optimized measurements can be found.

For the second optimization method, the number of turns should be designed and fixed first, then the window area needs to be designed as well. Moreover, for the fixed window area, there are many combinations of width and height (W x H = const.). The optimization here should perform so that the width and height of the structure geometry can be set optimally. Therefore, the cost function variations based on the mentioned parameters is the goal of this optimization strategy.

The third strategy focuses on optimizing the number of turns and the window area with each other. In this optimization technique, the number of turns, window width, and window height should be designed interactively. Therefore, this optimization strategy, focuses on considering both window area and number of turns at the same time by considering the cost function.



(a) (b)

Figure 14. f_c-w-h graphs. a) Conductive core. b) Nonconductive core.

Figure 15 shows the flowchart diagram of the optimization method that is used in this paper. This flowchart is based on parasitic analysis, defined cost function, pareto-optimal design, FEM/experimental results, EMI noise level, and IEC61800-3 standard.

In the CM EMI reduction, the most important impedance is the HF transformer interwinding capacitances. Because these parasitic provide the circulating path for the noise. In the matter of differential mode noise reduction, leakage inductance reduction is quite effective. Because it leads to lowering the noise current circulating in the loops and reduce the spikes in the current and voltage waveforms. In the optimization process, with the fixed number of turns (N), the magnetizing inductance does not change and only parasitic capacitances and leakage inductances were modified. In other words, the proposed optimization method does not affect other operating parameters and only focus on the EMI reduction in the system. A depth analysis regarding the mentioned points is discussed in [36]. As discussed in [36], the EMI mitigation process with respect to the optimization of the HF transformers not only depends on the impedance analysis but also is independent from operating parameters.

6. ANALYSIS OF PARASITIC PARAMETERS

In sections 3 and 4, leakage inductance and parasitic capacitance are formulated for the transformer structure. The obtained analytical expressions can be applied to any high voltage level, high power rating, frequency, and core volume. Additionally, in section V, the optimal design graphs for the transformer structure are obtained. In this section, to validate the analytical models of the parasitic parameters the transformer structure and

winding arrangement is investigated. To remove the effect of impedance transferring from secondary to primary, the turn ratio is set to 1. Moreover, in this section, FEM and experimental results are obtained and compared with the analytical models.

6.1. ANALYTICAL VERIFICATION I

By solving equations (11) and (42) and by increasing the width of the window area (w), the leakage inductance variation and the parasitic capacitance variation for both the conductive and nonconductive cores are shown in Figure 16. Since the number of turns for both the primary and secondary is assumed to be fixed, as the w increases, the height of the window area (h1 and h2) decreases, so that the area of each window (w ×(h1+h2)) is constant. In other words, by increasing w, the layers (m1 and m2) increase, and the number of conductors per layer (n1 and n2) decrease. The number of turns is 400 and equations (45), (46) are still valid. The results of Figure 16 are based on the analytical model expressions shown in sections 3 and 4. In order to validate these results, 3D-FEM simulations are used. Figure 17 shows the front view of the magnetic field strength distribution during the short circuit test, and Figures 18 and 19 show the front view of the electric displacement field distribution. The window area parameters are shown in Table 1.

Table 2 show the parasitic parameter results from FEM simulations. In the analysis, the insulation material that used as bare conductor insulator is silicon varnish with dielectric constant and a dielectric strength of 3.1 and 120kV/mm, respectively. Also, the bobbin material is ABS plastic, with a dielectric constant and dielectric strength of 2.2 and 25kV/mm. The copper conductivity is considered 5.8x107. The core considered both

conductive and non-conductive in the analysis based on the Ferrite-MnZn and Ferrite-NiZn. By comparing the results of Table 2 and Figures 17-19, it is clear that as the magnetic and electric fields intensify the parasitic values increase. Also, Table 2 and Figure 16 show that the analytical expressions and FEM results are in a good agreement.

Table 1. Window area parameters of the transformer structures used for FEM.

Transformer Types	h_1+h_2 (Window Height (mm))	w (Window Width (mm))
Type I	180	10
Type II	90	20
Type III	60	30
Type IV	30	60
Type V	10	180

Table 2. Leakage inductance and parasitic capacitance. The results are for the transformer structures shown in Figures 17-19 that resulted from FEM simulations.

Transformer Type	Leakage Inductance (mH)	Conductive Core Parasitic Capacitance (pF)	Nonconductive Core Parasitic Capacitance (pF)
Type I	62.33	54.74	6.87
Type II	24.61	48.53	13.67
Type III	15.84	33.61	15.46
Type IV	10.34	56.87	34.31
Type V	1.76	158.63	147.15

6.2. ANALYTICAL VERIFICATION II AND EXPERIMENTAL RESULTS

In the previous section, *Analytical Verification I*, the parasitic parameter variations obtained for a fixed number of turns and a constant window area. In this section, the leakage inductance and the parasitic capacitance of the transformer structures, which have different

numbers of turns, window width, and window height, are calculated by equations (11) and (42). Also, the results are compared to the FEM simulation and the experimental results. Based on the optimization results, these structures and dimensions show an approximated optimized behavior in case of parasitic parameters and that is the reason of choosing these structures.

Table 3. Window area parameters of the transformer structures shown in Figure 20.

Transformer Types	h_1+h_2 (Window Height (mm))	w (Window Width (mm))	Number of Turns (N)
Type a	60	30	400
Type b-1	45	45	400
Type b-2	45	45	450
Type c	30	60	400

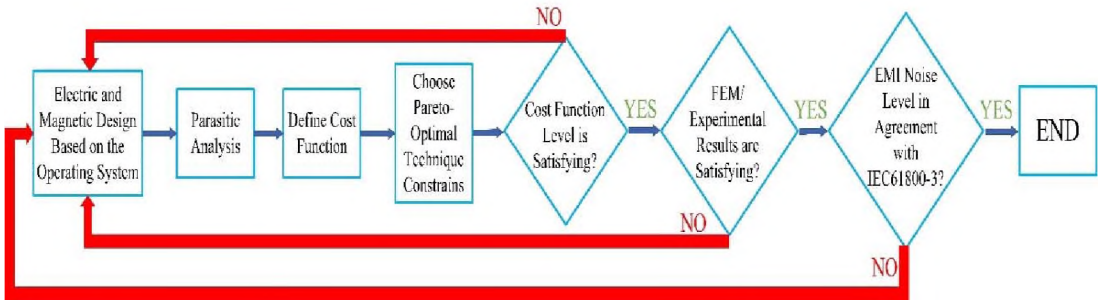


Figure 15. Optimization flowchart diagram.

Table 3 shows the window area width and height for each structure. Types a, b, and c in Table 3 are the same as Figure 20. Note that equations (45), (46) are still valid. Figure 21 shows the magnetic field strength distribution during the short circuit test in the

transformer structures. Also, Figure 22 shows the electric displacement field distribution in the transformer structures. The experimental results for the transformer structures are shown in Figure 23. The experimental measurements were achieved by using the HP Hewllet Packard 4284A and IET DE-6000 LCR meters. Figure 24 shows the leakage inductance and the parasitic capacitance values that resulted from using different methods for the transformer structures shown in Figure 20.

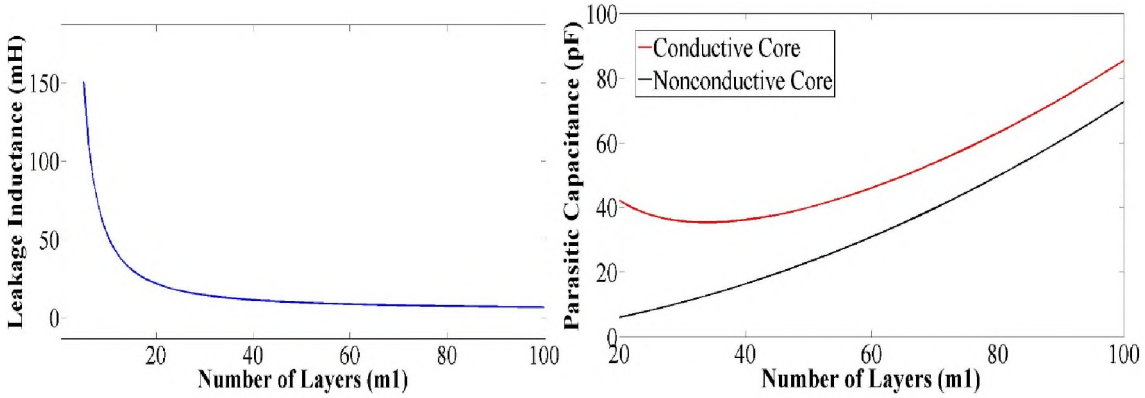


Figure 16. Leakage inductance and parasitic capacitance variation.

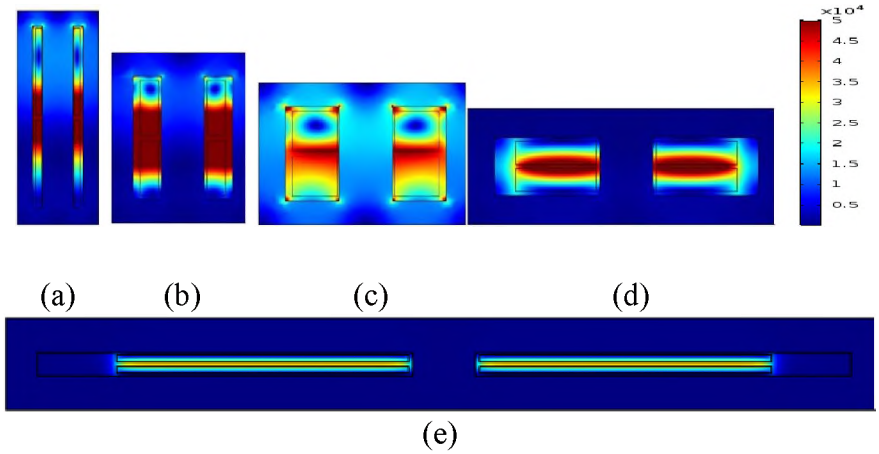


Figure 17. Front view of the magnetic field strength distribution (A/m). a) Type I. b) Type II. c) Type III. d) Type IV. e) Type V.

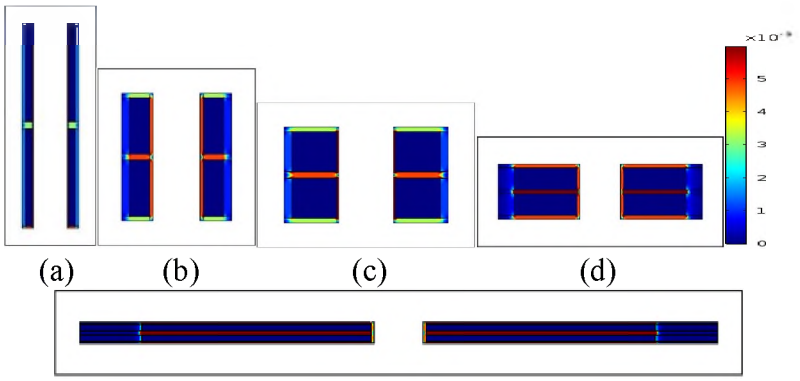


Figure 18. Front view of the electric displacement field (C/m^2) distribution. a) Type I. b) Type II. c) Type III. d) Type IV. e) Type V.

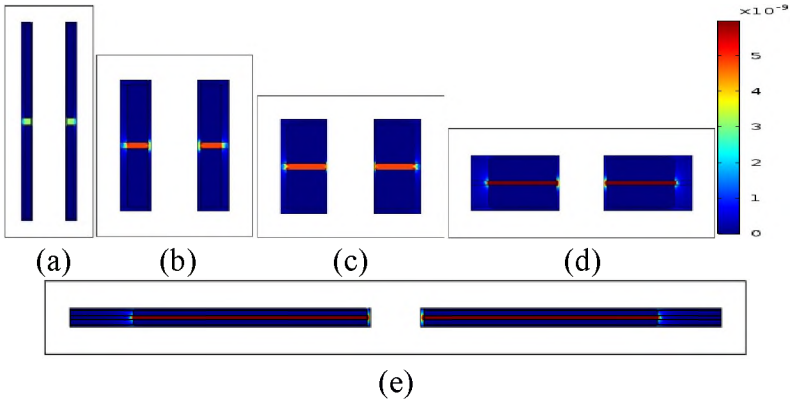


Figure 19. Front view of the electric displacement field (C/m^2) distribution. a) Type I. b) Type II. c) Type III. d) Type IV. e) Type V.

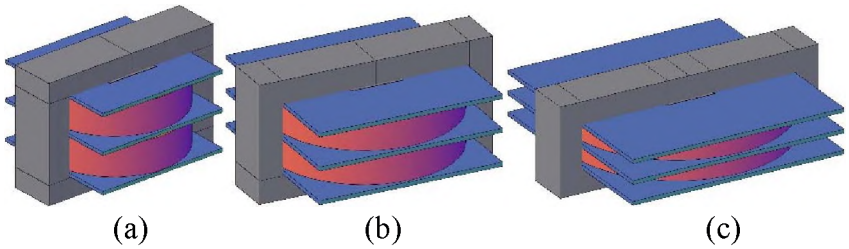
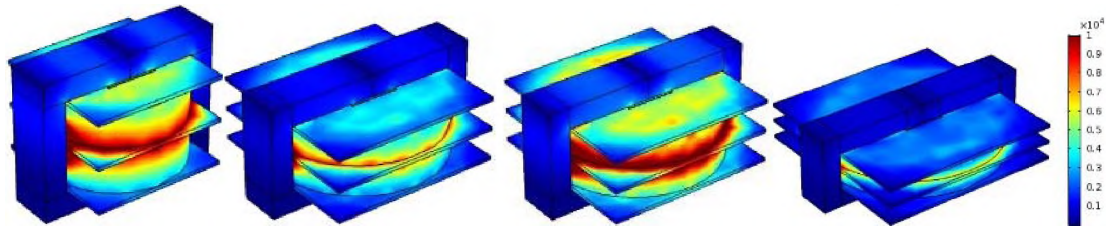
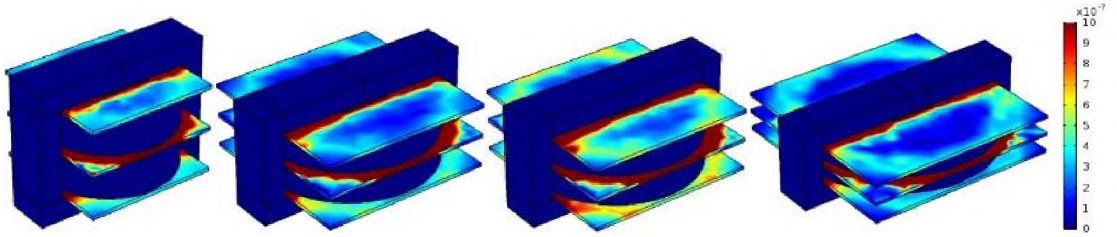


Figure 20. Transformer structures and the winding arrangements.



(a) (b1) (b2) (c)

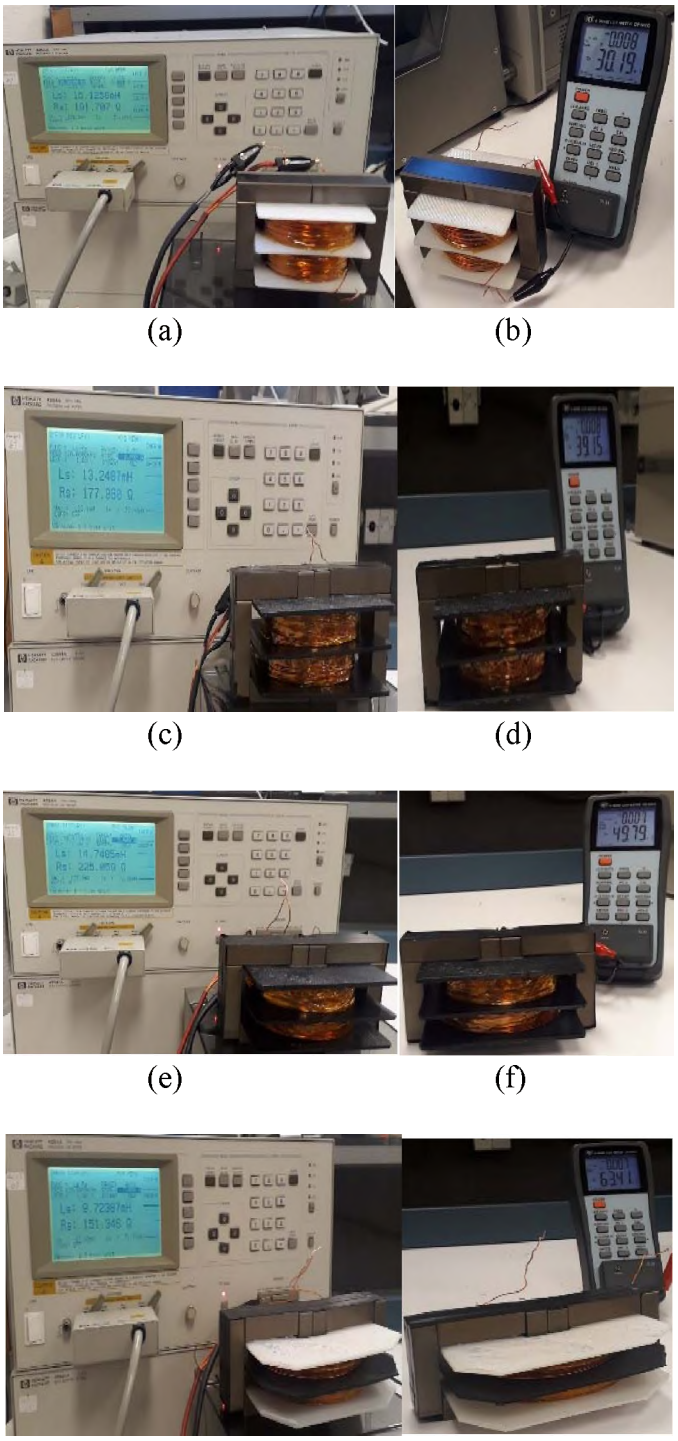
Figure 21. Magnetic field strength distribution (A/m). a) Type a. b1) Type b-1. b2) Type b-2. c) Type c.



(a) (b1) (b2) (c)

Figure 22. Electric displacement field distribution (C/m^2). a) Type a. b1) Type b-1. b2) Type b-2. c) Type c.

As is shown in Figure 24, there is an appropriate agreement among the results of all three methods. The maximum deviations from the experimental results are in agreement with the error analysis preformed in [34]. Therefore, the experimental results and the FEM results verify the analytical models. In the analytical models shown in section 3 for the leakage inductance, the frequency plays an important role. As the frequency increases, the leakage inductance is expected to decrease, due to the skin effect. Figure 25 shows the frequency response of the leakage inductance for the structures shown in Figure 20. As is shown in Figure 25, increasing the frequency decreases the skin depth in equation (8), intensifies the skin effect, and results in changing of the leakage inductance.



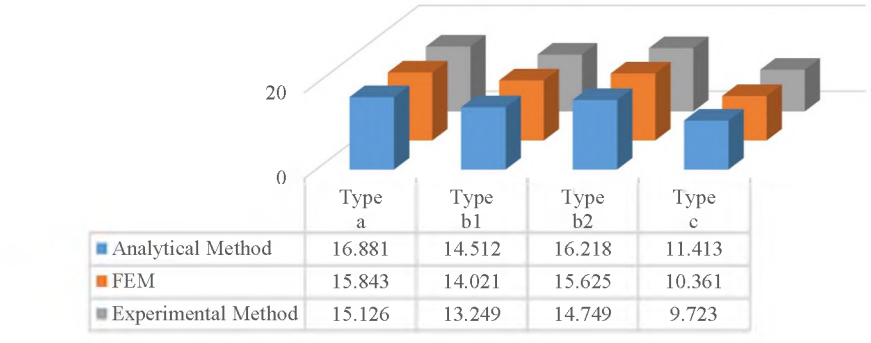
(a) (b)

(c) (d)

(e) (f)

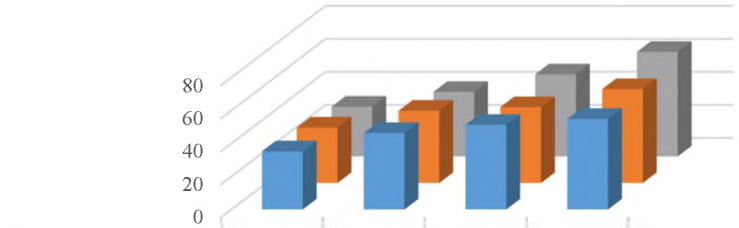
(g) (h)

Figure 23. Experimental results. a) Leakage inductance of type a. b) Parasitic capacitance of type a. c) Leakage inductance of type b1. d) Parasitic capacitance of type b1. e) Leakage inductance of type b2. f) Parasitic capacitance of type b2. g) Leakage inductance of type c. h) Parasitic capacitance of type c.



	Type a	Type b1	Type b2	Type c
Analytical Method	16.881	14.512	16.218	11.413
FEM	15.843	14.021	15.625	10.361
Experimental Method	15.126	13.249	14.749	9.723

(a)



	Type a	Type b1	Type b2	Type c
Analytical Method	35.27	46.32	51.27	54.88
FEM	33.61	43.78	45.96	56.87
Experimental Method	30.19	39.15	49.79	63.41

(b)

Figure 24. Leakage inductance and parasitic capacitance of the transformers. a) Leakage inductance (mH). b) Parasitic capacitance (pF).

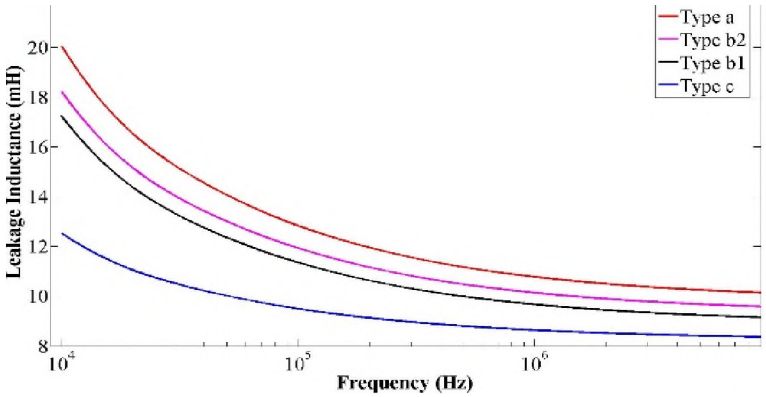
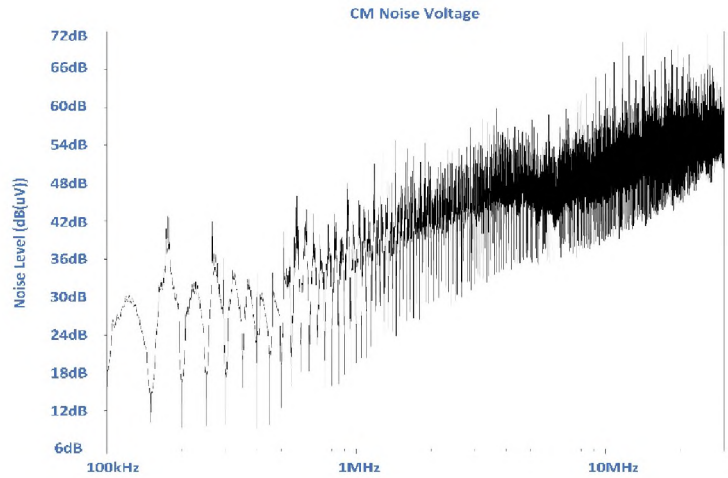
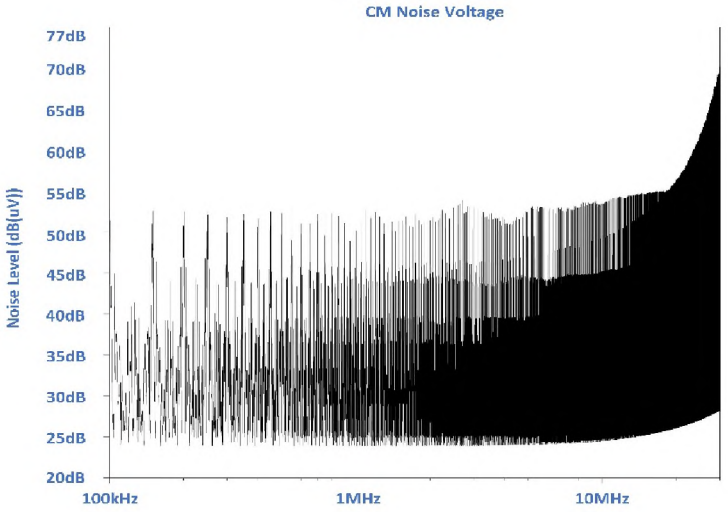


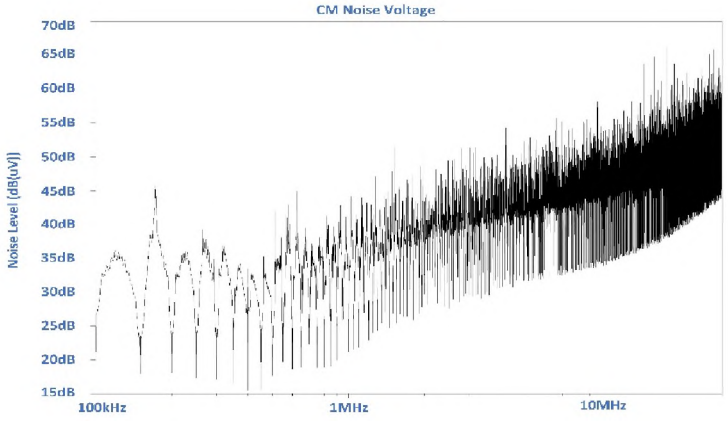
Figure 25. Frequency response of the leakage inductance.



(a)



(b)



(c)

Figure 26. EMI noise level after using pareto-optimal techniques. a) pareto-optimal technique I. b) pareto-optimal technique II. c) pareto-optimal technique III.

6.3. EMI NOISE LEVEL AFTER IMPLEMENTING PARETO-OPTIMAL TECHNIQUES

The pareto-optimal techniques and constrains that described in section 5 are implemented to the high voltage pulse transformer of the system that is shown in Figure 1. As mentioned before, in order for lowering the EMI noise level under the standard limits, the EMI propagation should be blocked from circulating through the transformer parasitics. Before the optimizations, the EMI noise level (that is shown in Figure 5) is far greater than the IEC61800-3 limits. Figure 26 shows the EMI noise level of the system after implementing the pareto-optimal methods. Three pareto-optimal techniques described in section 5 are investigated here for noise attenuating. Figure 26(a) is the EMI noise level after optimizing with pareto-optimal technique I, Figure 26(b) is the EMI noise level after optimizing with pareto-optimal technique II, and Figure 26(c) is the EMI noise level after optimizing with pareto-optimal technique III. All of the pareto-optimal techniques could lower the EMI noise under the IEC61800-3 limits. The IEC61800-3 limits are 79dB(uV) and 73dB(uV) for the frequency band of 150kHz – 500kHz and 500kHz – 30MHz, respectively. All the techniques here are effective for the aim of EMI noise attenuating. However, using which pareto-optimal techniques depend on the design strategy and costs of the project.

7. CONCLUSION

In order for increasing the efficiency and improving the performance of power conversion systems, it is very important to comply with EMC regulations and standards.

Especially, the new generation of power converters, due to the advent of new fast switches such as SiC and GaN. In this paper, the transformer geometry that shows an important effect on the EMI propagation is optimized and the results could be used in the HF transformer optimization for reducing the EMI in the AC-DC / DC-DC / DC-AC converters. This paper, analyzed a power application that designed to perform with SiC switches. The results not only present accurate parasitic parameters modeling but also present how the HF transformer can be optimized for EMI purposes and also shows the EMI variations based on the models and optimization. The EMI noise level of the system was obtained and compared to the IEC61800-3 standard. The optimized geometry structures were designed to show low-level parasitics. For this aim, pareto-optimal techniques implemented into the cost function that defined based on the transformer parasitics. The optimization could reduce the EMI propagation and reduce the EMI noise under the IEC61800-3 standard limitations. As concluded in this paper, optimizing the parasitics of the HF transformer is very effective in EMI mitigation and can remove the necessity of using filters and other passive elements. In conclusion, the parasitic values in power electronics system can be adjusted/limited by optimizing geometry structure of the HF transformer. Therefore, the parasitics cannot flow from a winding to the other windings. As shown in this paper, HF magnetic components optimization can reduce the EMI noise level under the standard limits and in some cases this optimization technique can lead to remove/minimize the EMI filters.

REFERENCES

[1] T. Qian, Q. Wei, Z. Yu, W. Tang and Q. Wu, "Multi-parametric sensitivity analysis of improved transformer thermal models considering nonlinear effect of oil time constant," *CSEE Journal of Power and Energy Systems, 2020.*

[2] J. Li, X. Zuo, Y. Zhao, X. Lv and J. Wang, "Operation, analysis and experiments of DC transformers based on modular multilevel converters for HVDC applications," *CSEE Journal of Power and Energy Systems*, vol. 5, no. 1, pp. 87-99, March 2019.

[3] C. Pan and H. Su, "Research on excitation current and vibration characteristics of DC biased transformer," *CSEE Journal of Power and Energy Systems, 2019.*

[4] Y. Liu, G. Li, L. Guan and Z. Li, "The single-active-part structure of the UHVDC converter transformer with the UHVAC power grid," *CSEE Journal of Power and Energy Systems*, vol. 3, no. 3, pp. 243-252, Sept. 2017.

[5] J.-M. Choi, B.-J. Byen, Y.-J. Lee, D.-H. Han, H.-S. Kho, and G.-H. Choe, "Design of Leakage Inductance in Resonant DC-DC Converter for Electric Vehicle Charger," *IEEE Transactions on Magnetics*, vol. 48, no. 11, pp. 4417–4420, 2012.

[6] A. Pokryvailo and H. Dave, "Coupled Magnetic Field-Circuit Analysis of Inductive Power Transfer in High-Potential Transformers," in *IEEE Transactions on Plasma Science*, 2019.

[7] Y. Xu, L. Chen, W. Guo, C. Shangguan, J. Zuo and K. He, "Optimal Design of Medium-Frequency Fe-Based Amorphous Transformer Based on Genetic Algorithm," in *IEEE Transactions on Plasma Science*, vol. 46, no. 10, pp. 3240-3248, Oct. 2018.

[8] H. Shi, H. Wen and Y. Hu, "Deadband Effect and Accurate ZVS Boundaries of GaN-Based Dual Active Bridge Converters with Multiple-Phase-Shift Control," *IEEE Transactions on Power Electronics*, 2020.

[9] Y. Liu *et al.*, "A Simple Phase-Shift Modulation Using Parabolic Carrier for Dual Active Bridge DC-DC Converter," *IEEE Transactions on Power Electronics*, 2020.

[10] T. Guillod, D. Rothmund and J. W. Kolar, "Active Magnetizing Current Splitting ZVS Modulation of a 7 kV/400 V DC Transformer," *IEEE Transactions on Power Electronics*, vol. 35, no. 2, pp. 1293-1305, 2020.

[11] B. Zhang, S. Xie, X. Wang and J. Xu, "Modulation Method and Control Strategy for Full-Bridge-Based Swiss Rectifier to Achieve ZVS Operation and Suppress Low-Order Harmonics of Injected Current," *IEEE Transactions on Power Electronics*, vol. 35, no. 6, pp. 6512-6522, 2020.

[12] M. Li, Z. Ouyang and M. A. E. Andersen, "High-Frequency LLC Resonant Converter With Magnetic Shunt Integrated Planar Transformer," *IEEE Transactions on Power Electronics*, vol. 34, no. 3, pp. 2405-2415, 2019.

[13] H. F. Ahmed and H. Cha, "A New Class of Single-Phase High-Frequency Isolated Z-Source AC–AC Converters With Reduced Passive Components," *IEEE Transactions on Power Electronics*, vol. 33, no. 2, pp. 1410-1419, 2018.

[14] W. Water and J. Lu, "Shielding Analysis of High-Frequency Coaxial Transformers Used for Electric Vehicle On-Board Charging Systems," *IEEE Transactions on Magnetics*, vol. 49, no. 7, pp. 4005-4008, July 2013.

[15] B. Chen, P. Wang, Y. Wang, S. Zhang, L. Yang, and R. Ji, "A Bidirectional CDT-LC Resonant DC-DC Converter with a Wide Voltage Range," *IEEE Transactions on Industrial Electronics*, pp. 1–1, 2019.

[16] M. Nazmunnahar, S. Simizu, P. R. Ohodnicki, S. Bhattacharya, and M. E. Mchenry, "Finite-Element Analysis Modeling of High-Frequency Single-Phase Transformers Enabled by Metal Amorphous Nanocomposites and Calculation of Leakage Inductance for Different Winding Topologies," *IEEE Transactions on Magnetics*, vol. 55, no. 7, pp. 1–11, 2019.

[17] M. Jabbari and M. Mokhtari, "High-Frequency Resonant ZVS Boost Converter with Grounded Switches and Continuous Input Current," *IEEE Transactions on Industrial Electronics*, pp. 1–1, 2019.

[18] A. Kumar, A. Ravichandran, S. Singh, S. Shah, and S. Bhattacharya, "An intelligent medium voltage gate driver with enhanced short circuit protection scheme for 10kV 4H-SiC MOSFETs," *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2017.

[19] Y.-S. Hwang, J.-J. Chen, J. Yang, and Y. Ku, "A Low-EMI Continuous-Time Delta-Sigma-Modulation Buck Converter with Transient Response Eruption Techniques," *IEEE Transactions on Industrial Electronics*, pp. 1–1, 2019.

[20] A. Jahromi, J. Faiz, and H. Mohseni, "Calculation of distribution transformer leakage reactance using energy technique," *J. Faculty Eng.*, vol. 38, no. 3, pp. 395–403, Sep. 2004.

[21] V. V. Kantor, "Methods of calculating leakage inductance of transformer windings," *Russian Electrical Engineering*, vol. 80, no. 4, pp. 224–228, 2009.

[22] S. R. Thondapu, M. B. Borage, Y. D. Wanmode, and P. Shrivastava, "Improved Expression for Estimation of Leakage Inductance in E Core Transformer Using Energy Method," *Advances in Power Electronics*, vol. 2012, pp. 1–6, 2012.

[23] Z. Ouyang, O. C. Thomsen, and M. A. E. Andersen, "The analysis and comparison of leakage inductance in different winding arrangements for planar transformer," *2009 International Conference on Power Electronics and Drive Systems (PEDS)*, 2009.

[24] W. Hurley and D. Wilcox, "Calculation of leakage inductance in transformer windings," *IEEE Transactions on Power Electronics*, vol. 9, no. 1, pp. 121–126, 1994.

[25] M. A. Bahmani and T. Thiringer, "Accurate Evaluation of Leakage Inductance in High-Frequency Transformers Using an Improved Frequency-Dependent Expression," *IEEE Transactions on Power Electronics*, vol. 30, no. 10, pp. 5738–5745, 2015.

[26] Z. Ouyang, J. Zhang, and W. G. Hurley, "Calculation of Leakage Inductance for High-Frequency Transformers," *IEEE Transactions on Power Electronics*, vol. 30, no. 10, pp. 5769–5775, 2015.

[27] J. Biela and J. Kolar, "Using transformer parasitics for resonant converters - a review of the calculation of the stray capacitance of transformers," *Fourtieth IAS Annual Meeting. Conference Record of the 2005 Industry Applications Conference, 2005.*

[28] S. Mohsenzade, M. Aghaei, and S. Kaboli, "Leakage Inductance Calculation of the Transformers With Disordered Windings," *IEEE Transactions on Plasma Science*, vol. 47, no. 4, pp. 1799–1807, 2019.

[29] N. B. Chagas and T. B. Marchesan, "Analytical Calculation of Static Capacitance for High-Frequency Inductors and Transformers," *IEEE Transactions on Power Electronics*, vol. 34, no. 2, pp. 1672–1682, 2019.

[30] L. Dalessandro, F. D. S. Cavalcante, and J. W. Kolar, "Self-Capacitance of High-Voltage Transformers," *IEEE Transactions on Power Electronics*, vol. 22, no. 5, pp. 2081–2092, 2007.

[31] M. Pahlevaninezhad, D. Hamza, and P. K. Jain, "An Improved Layout Strategy for Common-Mode EMI Suppression Applicable to High-Frequency Planar Transformers in High-Power DC/DC Converters Used for Electric Vehicles," *IEEE Transactions on Power Electronics*, vol. 29, no. 3, pp. 1211–1228, 2014.

[32] J. A. Collins, "An Accurate Method for Modelling Transformer Winding Capacitances", Indus. Electronics Conference, 1990, pp. 1094 – 1099.

[33] M. Xinkui; Chen Wie, "More precise model for parasitic capacitances in high-frequency transformer", 33rd Power Electronics Specialists Conference PESC'02, Vol. 2, June 23-27, June 2002, pp. 1054 – 1057.

[34] M. S. Sanjari Nia, P. Shamsi and M. Ferdowsi, "Investigation of Various Transformer Topologies for HF Isolation Applications," IEEE Transactions on Plasma Science, vol. 48, no. 2, pp. 512-521, Feb. 2020.

[35] J. Kołek and M. Hołub, "Practical Design of a High-Voltage Pulsed Power Supply Implementing SiC Technology for Atmospheric Pressure Plasma Reactors," *Applied Sciences*, vol. 9, no. 7, p. 1451, 2019.

[36] M. S. Sanjari Nia, P. Shamsi and M. Ferdowsi, "EMC Modeling and Conducted EMI Analysis for a Pulsed Power Generator System Including an AC–DC–DC Power Supply," IEEE Transactions on Plasma Science, vol. 48, no. 12, pp. 4250-4261, Dec. 2020.

III. EMC MODELING AND CONDUCTED EMI ANALYSIS FOR A PULSED POWER GENERATOR SYSTEM INCLUDING AND AC-DC-DC POWER SUPPLY

ABSTRACT

High voltage (HV) pulsed power generators are very important in plasma generation in corona discharge reactors. With the advent of new fast switches technologies such as silicon carbide (SiC) and gallium nitride (GaN), electromagnetic interference (EMI) noise in such systems is very challenging. In this paper, electromagnetic compatibility (EMC) modeling and conducted EMI analysis for a pulse generator including an AC-DC-DC power supply are developed. Moreover, the common mode (CM) EMI noise propagation through the system is discussed and the noise sources and effect of each component on the noise flowing are analyzed. The AC-DC-DC power supply role is also investigated and since there is an isolation stage in the system the effect of high frequency (HF) transformers that provide a flowing path for noise is also studied. Additionally, the CM impedance of different parts of the system as well as the noise voltage are discussed by regarding different values for parasitic parameters of the system. As the system noise level could not meet IEC61800-3 standard, EMI attenuation techniques were applied to the system. By using balance technique and adding filtering inductor as a decoupling inductance, the EMI noise is reduced. Furthermore, an EMI filter optimized and designed for the power supply system that could reduce the EMI noise level. However, by using some EMI reduction techniques that are explained in the paper, the size of the required EMI filter is reduced. In this paper, EMC modeling, conducted EMI analysis, and EMI

reduction techniques led to higher performance and efficiency and lower size of EMI filter that reduced the overall size of the system.

1. INTRODUCTION

The efficiency and performance of power electronic converters are highly under influence of the flowing EMI noise in the system. Removing and/or reducing EMI noise in the systems not only enhances the overall performance and power density but also leads to less expensive, smaller, and more reliable converters [1]-[3]. Modeling and analyzing EMI noise in converters and applying noise attenuating methods can lead to removing or minifying the EMI filters [4], [5]. In some converters, the EMI filters include 30% of the size and mass of the converters. On the other hand, due to the complexity of the electronic systems and new devices, the EMC standards are stricter on the new coming power electronic converters such as the converters used in pulse generators, electric vehicles, and extremely fast charging systems.

Power electronic switches are the main source of EMI noise in the systems, also the parasitic capacitances between drain and heat-sink of the switches provide a flowing path for the CM noise [6]-[8]. Moreover, in many converters due to the safety and technical requirements, HF transformers are an essential part of the systems [9], [10]. In the HF transformers the parasitic capacitance between the windings (inter-winding capacitance) is the main path of CM circulation in the power electronic systems [11]. Analyzing the EMI sources and impedances is the main key in studying noise models and EMI reduction techniques of the systems.

AC-DC-DC power supply are among the most popular and practical power conversion systems. There are several switches in AC-DC-DC systems due to two-stage power conversion and in many cases, there are HF transformers as well. Fig .1 shows the AC-DC-DC converter and pulse generator that is used in this paper. The pulse generator includes resonant capacitor charger and pulse shaping unit. The pulse generator used in this paper is based on the scheme explained in [12]. In this converter the rectifier that is placed after the line impedance stabilization network (LISN), provides relatively low impedance for CM EMI sources. Also, dual active bridge (DAB) DC-DC converter including an HF transformer alter the DC voltage level in the system and due to the HF transformer, a low impedance path for the noise circulation is observable. In this converter there are 16 main CM noise sources that lead to CM noise circulation in the system due to the impedance of the switches and magnetic parts of the converter. The output of the AC-DC-DC system is connected to the HV pulsed power supply that is used in non-thermal plasma reactors. By advent of new SiC and GaN switches, which show high dv/dt and di/dt, analyzing EMC is necessary in pulse generators to guarantee the robust generation of plasma in corona discharge reactors [12].

In [13], the EMI analysis for converters are studied and modeled. However, lack of accuracy and ignoring parasitic effects and impedances are the main problems. In [14], EMI models and noise reduction techniques are discussed as well, but the proposed methods and attenuation techniques cannot apply for an AC-DC-DC power converter. On the other hand, some proposed methods such as [15] are only acceptable for a certain range of frequencies. In [16], by using balance technique, noise is reduced and this method removed the necessity of the EMI filters. In [17], the balance technique is discussed for

inverters and converters. In [18], the EMI analyzed in a series rectifier and inverter to drive a three-phase motor. The proposed methodology in that paper is effective for a suitable range of frequencies. However, the discussed converter did not include an isolation stage and HF transformer in the analysis. Furthermore, in [19], parasitic capacitance analysis is studied for the magnetic parts of an LLC converter. In that paper, CM noise impedances are analyzed and the CM noise voltage is reduced. Regarding parasitic impedance analysis in HF transformers, reference [20] investigated a detailed model for analyzing and measuring of those parameters. However, the mentioned models and techniques were not considered in an AC-DC-DC converter with rectifier and DAB. In [21], a boost DC-DC converter is studied and the CM noise model is investigated. In that paper the equivalent circuit of each part of the converter, is extracted for HF /VHF and by using superposition theorem, different EMI sources are analyzed. By considering the methods and models used in the aforementioned references it can be concluded that, analyzing EMI models for each converter and system require different methods and novel analysis.

In this paper, conducted CM EMI noise modeling of a pulse generator including an AC-DC-DC power supply is developed. The EMI equivalent circuit of the system is explained and the effect of each component and each noise source is investigated. Moreover, the noise flowing into the isolation stage of the AC-DC-DC system that provides the path for noise circulating is analyzed. The CM noise voltage level and impedance of the system are investigated and calculated. Furthermore, the effect of different parasitic parameters values on the CM noise voltage is studied. Additionally, an optimized EMI

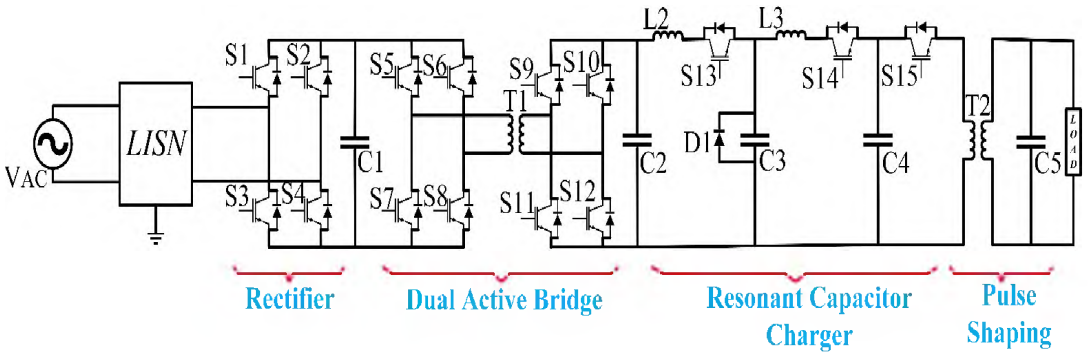


Figure 1. Pulse generator system including the AC-DC-DC power converter.

filter is designed and studied and the effect of that filter on the power supply CM noise voltage level is analyzed. As well, EMI noise reduction techniques are explained and used for this system and by applying those methods the EMI level is reduced significantly to meet IEC61800-3 [22] limits. Contributions of this paper are analyzing EMI noise and developing new reduction techniques for a pulse generator system by considering the power supply. In more detail, a novel method of EMI analysis and CM noise attenuation techniques for the pulsed power systems are proposed by considering the noise propagation of the feeding power converter. The EMI sources are considered based on the SiC switches noise behavior. Moreover, optimized EMI filters for pulsed power applications are designed and developed by considering both magnetic and parasitic behavior, which lead to filter minimization or filter-free systems.

2. EMI NOISE MODELING

EMI noise consists of CM and differential mode (DM) noise. CM noise is far greater than DM noise in this system. Based on the analysis, the CM EMI noise is at least

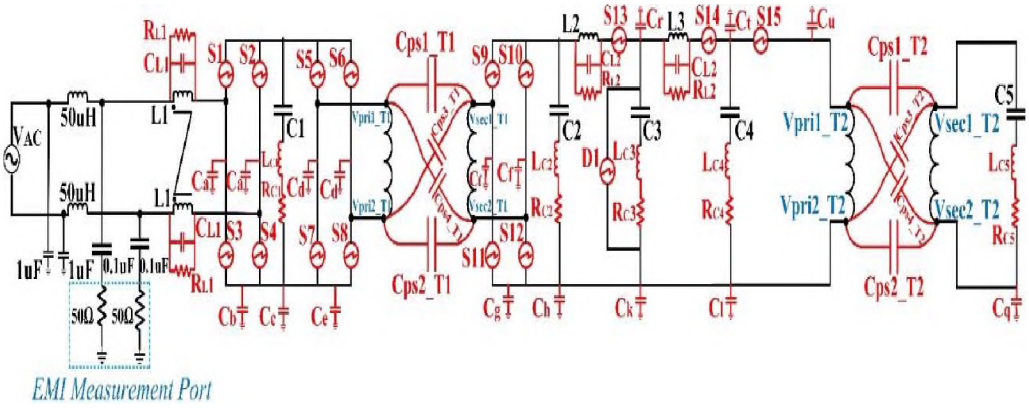


Figure 2. CM conducted EMI model of the whole system.

ten times greater than DM noise. Hence, the CM noise is the main problem regarding EMC issues. In order to find the CM EMI noise in the system depicted in Figure 1, the EMC model for noise analyzing is illustrated in Figure 2. Two LISNs as low-pass filters and known impedances are placed after the AC system for noise measurement purposes and filtering the AC source harmonics injecting into the system. The approximate equivalent impedance of two LISNs is considered 25Ω. In order for reducing the EMI noise in the system, a fully coupled inductor is placed before the rectifier. As shown in the model, the switches are considered as noise sources, the inductors and capacitors are modeled for HF and VHF with parasitic components, and the heat-sink to ground parasitic capacitances of the switches provide CM noise path. Based on the source substitution theorem [23], switches S1, S2, S5, S6, S9, S10, S13, S14, and S15 are considered as current sources and switches S3, S4, S7, S8, S11, S12, and D1 are considered as voltage sources. These current/voltage sources are the same as drain to source current/voltage waveforms of the corresponded switches and anode to cathode voltage waveform for D1 diode.

In the EMC model of Figure 2, based on the superposition theorem in the circuit theory, the CM noise does not flow in the loop made by upper switches. Thus, those

switches are open-circuited. Among the capacitors C1, C2, C4, and C5 are considered relatively large, thus these capacitors can be modeled as short-circuited in the CM noise model at high frequencies and the series inductors and resistors of these capacitors can be ignored. Also, the effect of the anti-parallel diodes of the switches are negligible in the CM noise propagation.

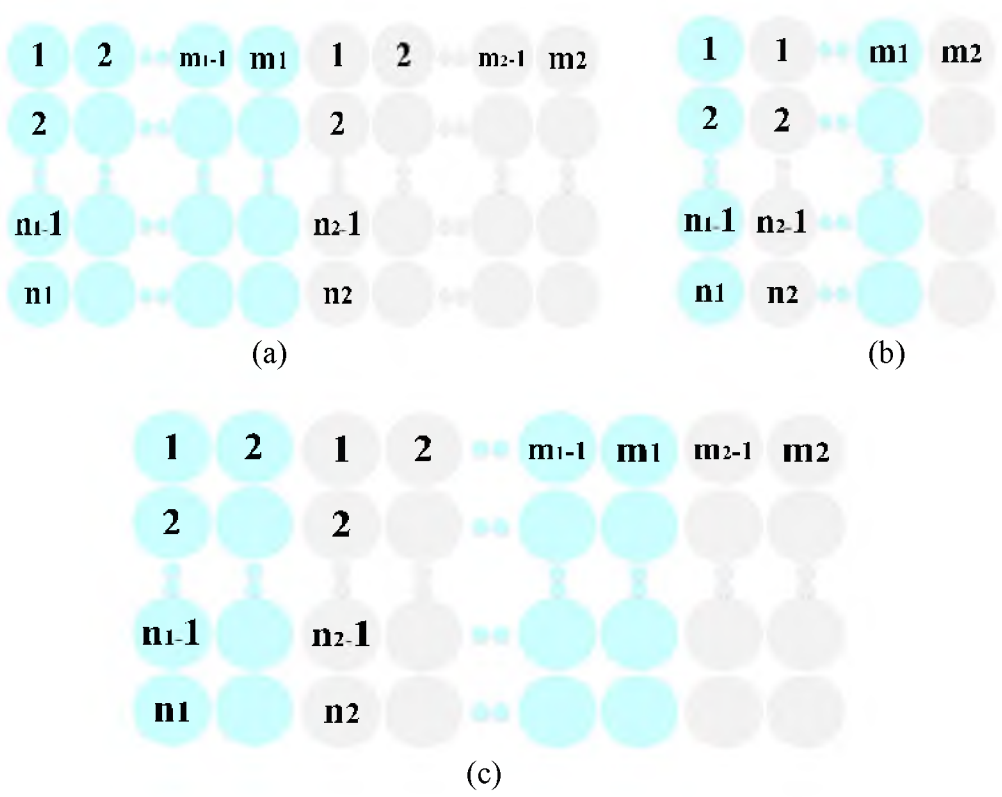


Figure 3. Winding arrangement of the HF transformer at the right window. a) primary and secondary wound on each other. b) Interleaved configuration with P-S-P-S arrangement. c) Interleaved configuration with P-P-S-S arrangement.

The other important impedance in the CM noise modeling, which provides the main path for the EMI noise is the transformer inter-winding capacitance. As shown previously in [24], due to the skin effect, the leakage inductance value in high frequencies is negligible.

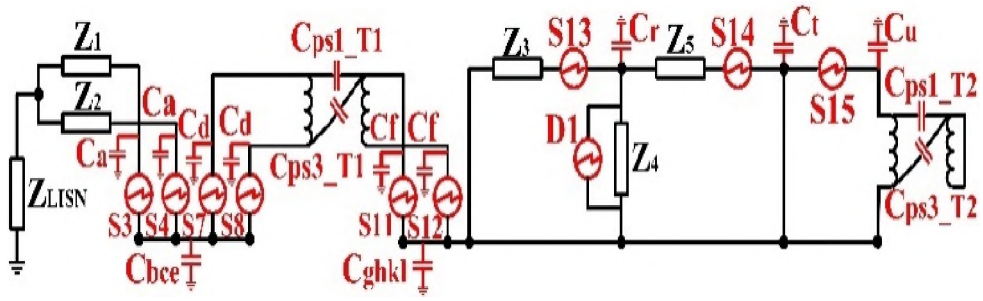


Figure 4. Reduced circuit of the CM conducted EMI model.

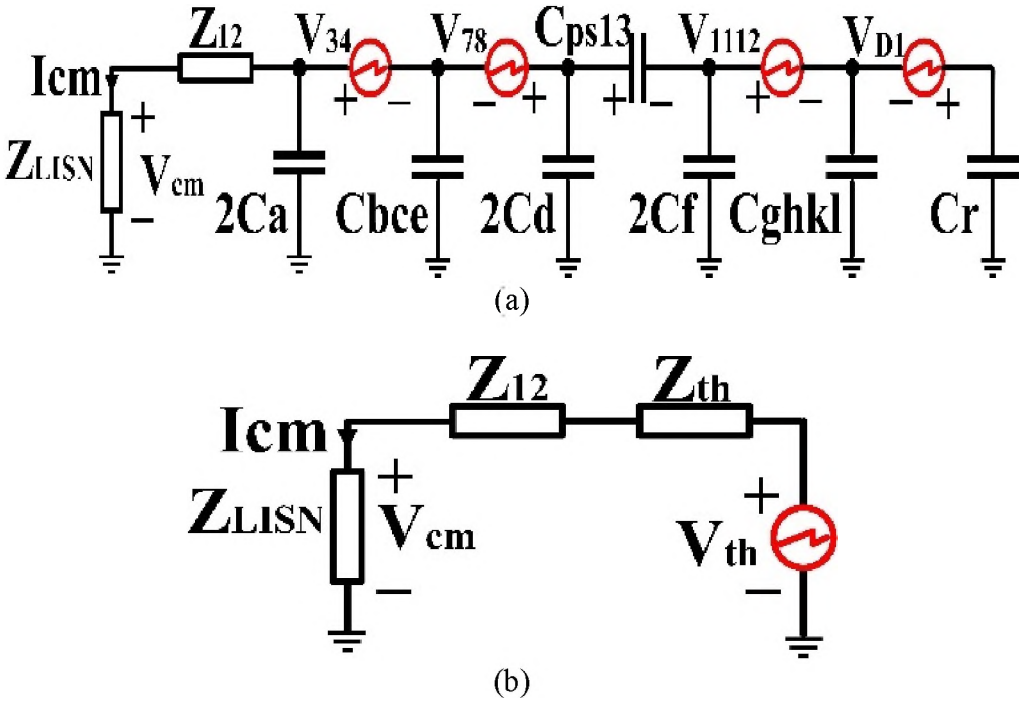


Figure 5. Equivalent circuit and thevenin model. a) Equivalent circuit of the CM conducted EMI model. b) Thevenin equivalent model of the system.

Moreover, the four-capacitor model of the transformer can be reduced to a 2-capacitor model without compromising the accuracy of CM noise flowing [10]. Following equations describe the CM current flowing through the parasitic capacitors of the HF transformer:

$$i_{cm-T1} = C_{ps1_{T1}} \frac{d}{dt}\left(V_{pri1_{T1}} - V_{sec1_{T1}}\right) + C_{ps3_{T1}} \frac{d}{dt}\left(V_{pri2_{T1}} - V_{sec1_{T1}}\right) \quad (1)$$

$$i_{cm-T2} = C_{ps1_{T2}} \frac{d}{dt}\left(V_{pri1_{T2}} - V_{sec1_{T2}}\right) + C_{ps3_{T2}} \frac{d}{dt}\left(V_{pri2_{T2}} - V_{sec1_{T2}}\right) \quad (2)$$

Also, $C_{ps1_{T1}}$, $C_{ps3_{T1}}$, $C_{ps1_{T2}}$, and $C_{ps3_{T2}}$ values depend on the transformer structure and winding arrangements. By using the following expression and the method used in [10], [20], the parasitic capacitances should satisfy the following energy equation:

$$\frac{1}{2}C_{ps1}(V_{pri1\_T1or2} - V_{\text{sec1}\_T1or2})^2 + \frac{1}{2}C_{ps3}(V_{pri2\_T1or2} - V_{\text{sec1}\_T1or2})^2 =$$

$$\frac{1}{2}\sum_{i=1}^{m_1}\sum_{j=1}^{m_2} C_{p_i s_j}(V_{p_i} - V_{\hat{s}_j})^2 \quad (3)$$

$$V_{p_i} - V_{\hat{s}_j} = \frac{V_{pri1\_T1or2} - V_{pri2\_T1or2}}{m_1} + \frac{V_{\text{sec1}\_T1or2} - V_{\text{sec2}\_T1or2}}{m_2} \quad (4)$$

V_{p_i} and $V_{\hat{s}_j}$ are the voltage of the primary and secondary conductors, respectively and $C_{p_i s_j}$ is the capacitance between primary and secondary conductors. m_1 and m_2 are number of layers in primary and secondary, respectively. Rest of the variables are shown in Figure 2. Consequently, the CM current can be expressed approximately by the following equation:

$$i_{cm-T1orT2} = \sum_{i=1}^{m_1}\sum_{j=1}^{m_2} C_{p_i s_j} \frac{d}{dt}(V_{p_i} - V_{\hat{s}_j}) \quad (5)$$

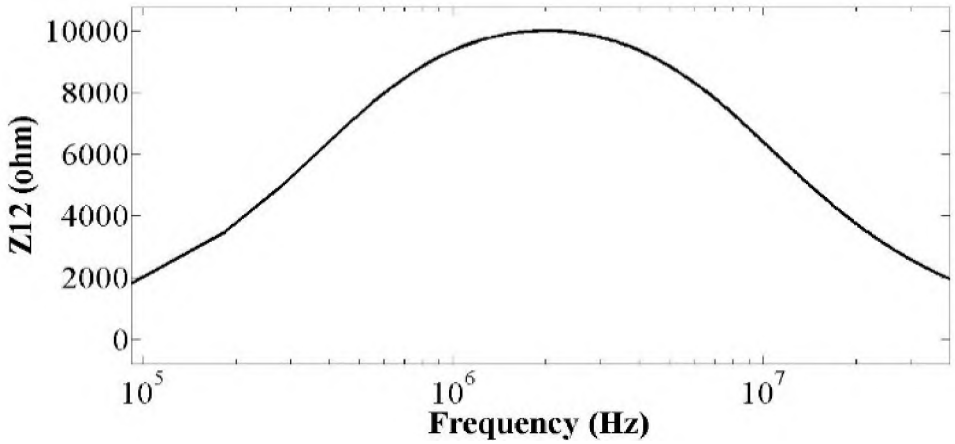


Figure 6. Magnitude of the Z_{12} impedance.

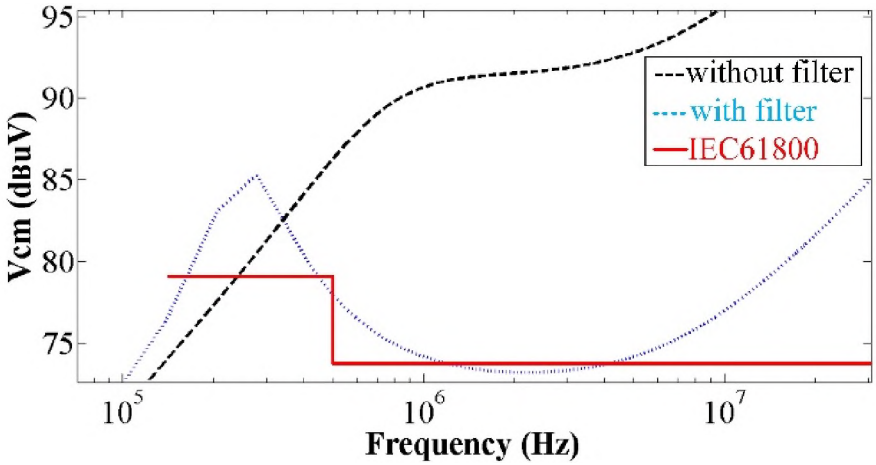


Figure 7. CM noise voltage of the system.

$C_{p_i s_j}$ depends on the winding arrangement and the transformer structure. In Figure 3, three winding arrangements are depicted. In these winding arrangements the primary and secondary are wound on each other on the middle leg of an EE core. Figure 3(a) is the regular winding arrangement with P-P-P-S-S-S configuration, Figure 3(b) is the interleaved winding arrangement with P-S-P-S-P-S configuration, and Figure 3(c) is the interleaved winding arrangement with P-P-S-S-P-P-S-S configuration. These three arrangements are analyzed here since these configurations are more practical and popular in HF isolation applications. The interleaved configurations are used to lower the leakage inductance of the transformer but the parasitic capacitance of the interleaved configurations is higher than regular arrangements. For the rest of this paper, Figure 3(a) is considered for analysis.

$C_{p_i s_j}$ for Figure 3(a):

$$C_{p_i s_j} = \frac{2\varepsilon \cdot \pi \cdot min\{n_1 t_{cond_{pri}} \,\&\, n_2 t_{cond_{sec}}\}}{\ell n\left(\frac{\frac{\hat{D}}{2} + m_1 t_{cond_{pri}} + (j-1) t_{cond_{sec}} + t_{ins_{sec}}}{\frac{\hat{D}}{2} + i t_{cond_{pri}} - t_{ins_{pri}}}\right)} \tag{6}$$

Table 1. System parameters.

Parameter	Parameter description	Parameter value
P_{system}	System power	1500 VA
V_{AC}	RMS voltage of the AC source	110 V
Vr_output	Rectifier output voltage	140 V
DAB DC-DC Converter	DAB voltage	140 V- 400 V
Vmax	Pulse generator maximum output voltage	20 kV
f_r	Rectifier frequency	500 Hz
f_{DAB}	DAB frequency	1400 Hz
f_{pg}	Pulse generator frequency	1800Hz
L_1	L_1 inductance	20mH
L_2	L_2 inductance	22uH
L_3	L_3 inductance	22uH
C_1	C_1 capacitance	1200uF
C_2	C_2 capacitance	1500uF
C_3	C_3 capacitance	15nF
C_4	C_4 capacitance	2uF
C_5	C_5 capacitance	1uF

$C_{p_i s_j}$ for Figure 3(b):

$$C_{p_i s_j} = \frac{2\varepsilon \cdot \pi \cdot min\{n_1 t_{cond_{pri}} \,\&\, n_2 t_{cond_{sec}}\}}{\ell n\left(\frac{\frac{\hat{D}}{2} + j t_{cond_{pri}} + j t_{cond_{sec}} + t_{ins_{sec}}}{\frac{\hat{D}}{2} + i t_{cond_{pri}} + (i-1) t_{cond_{sec}} - t_{ins_{pri}}}\right)} \tag{7}$$

$C_{p_i s_j}$ for Figure 3(c):

$$C_{p_i s_j} = \frac{2\varepsilon \cdot \pi \cdot min\{n_1 t_{cond_{pri}} \,\&\, n_2 t_{cond_{sec}}\}}{\ell n\left(\frac{\frac{\widehat{D}}{2} + (j-1{\cdot}5) t_{cond_{pri}} + j t_{cond_{sec}} + t_{ins_{sec}}}{\frac{\widehat{D}}{2} + i t_{cond_{pri}} + (i-1{\cdot}5) t_{cond_{sec}} - t_{ins_{pri}}}\right)} \tag{8}$$

n_1, n_2, $t_{cond_{pri}}$, $t_{cond_{sec}}$, $t_{ins_{pri}}$, $t_{ins_{sec}}$, and $\widehat{D}$ are number of conductors per layer for primary, number of conductors per layer for secondary, primary conductors' thickness, secondary conductors thickness, insulation thickness between primary conductors, insulation thickness between secondary conductors, EE core middle leg depth, respectively. Consequently, by using the above equations for $C_{p_i s_j}$, the CM current flowing through the transformer can be calculated by the aforementioned equations.

By considering the mentioned points, the EMC model can be reduced to Figure 4. Furthermore, by using superposition theorem and considering this fact that the CM noise cannot flow in the loops and must pass through the LISN, the EMC model can be simplified to the equivalent circuit of Figure 5(a). Therefore, only voltage sources of V_{S3}, V_{S4}, V_{S7}, V_{S8}, V_{S11}, V_{S12}, and V_{D1} are important in the CM noise model. The other noise sources influence the DM noise model. V_{34}, V_{78}, and V_{1112} are the equivalent noise voltage source and the average value of (V_{S3}, V_{S4}), (V_{S7}, V_{S8}), and (V_{S11}, V_{S12}), respectively. Likewise, C_{ps13}, C_{bce}, and C_{ghkl} are the parallel capacitances of (C_{ps1}, C_{ps3}), (C_b, C_c, C_e), and (C_g, C_h, C_k, C_l). Additionally, by using Thevenin theorem, the reduced circuit of Figure 5(a) can represent in Figure 5(b). Inductor line of the system and CM filter is combined into Z_{12}. The coupled inductor of the CM EMI filter is assumed to be fully coupled ($\hat{k}$=1). Also, Z_a,

Z_{bce}, Z_d, Z_f, Z_{ghkl}, Z_r, and Z_{ps13} are the corresponded impedance of the C_a, C_{bce}, C_d, C_f, C_{ghkl}, C_r, and C_{ps13} capacitors. C_T, Z_{th}, V_{th}, Vcm, and Z_{12} are shown in the following equations:

$$C_A = C_r + C_{ghkl} + 2C_f \tag{9}$$

$$C_B = \frac{C_A \cdot C_{ps13}}{C_A + C_{ps13}} \tag{10}$$

$$C_T = C_B + 2C_d + C_{bce} + 2C_a \tag{11}$$

$$Z_{th} = \frac{1}{j \cdot \omega \cdot C_T} \tag{12}$$

$$V_{th} = \frac{2Z_a}{2Z_a + [(Z_r || Z_{ghkl} || (2Z_f)) + Z_{ps13}] || (2Z_d) || Z_{cbe}} V_{34} -$$

$$\frac{(2Z_a) || Z_{cbe}}{(2Z_a) || Z_{cbe} + [(Z_r || Z_{ghkl} || (2Z_f)) + Z_{ps13}] || (2Z_d)} V_{78} +$$

$$\frac{[((2Z_a) || Z_{cbe} || (2Z_d)) + Z_{ps13}] || (2Z_f)}{[((2Z_a) || Z_{cbe} || (2Z_d)) + Z_{ps13}] || (2Z_f) + Z_r || Z_{ghkl}} V_{1112} -$$

$$\frac{[((2Z_a) || Z_{cbe} || (2Z_d)) + Z_{ps13}] || (2Z_f) || Z_{ghkl}}{[((2Z_a) || Z_{cbe} || (2Z_d)) + Z_{ps13}] || (2Z_f) || Z_{ghkl} + Z_r} V_{D1} \tag{13}$$

$$V_{cm} = \frac{Z_{LISN}}{Z_{LISN} + Z_{12} + Z_{th}} V_{th} \tag{14}$$

$$Z_{12} = \left[j \cdot \omega \cdot \left(1 + \hat{k}\right) \cdot \frac{L_1}{2} \right] \left| \left| \frac{1}{j \cdot \omega \cdot 2C_{L1}} \right| \right| \left(\frac{R_{L1}}{2} \right) =$$

$$\frac{j\omega R_{L1}\left(1+\hat{k}\right)L_1}{2R_{L1} - 2\omega^2 R_{L1}\left(1+\hat{k}\right)L_1 C_{L1} + j2\omega\left(1+\hat{k}\right)L_1} \tag{15}$$

Additionally, to consider the influence of skin effect, equation (16), model the frequency effect in the inductors by using Kelvin functions based on the Bessel functions.

$$L(\omega) = L_{initial} \cdot \frac{4\sqrt{2}\delta}{D} \left[\frac{ber\left(\frac{\sqrt{2}D}{2\delta}\right) \cdot bei'\left(\frac{\sqrt{2}D}{2\delta}\right) - bei\left(\frac{\sqrt{2}D}{2\delta}\right) \cdot ber'\left(\frac{\sqrt{2}D}{2\delta}\right)}{[ber'\left(\frac{\sqrt{2}D}{2\delta}\right)]^2 + [bei'\left(\frac{\sqrt{2}D}{2\delta}\right)]^2} \right] \tag{16}$$

In the above equation, D is conductor diameter and δ is the skin depth that is defined in the following equation:

$$\delta = \sqrt{\frac{2}{\omega \cdot \sigma \cdot \mu}} \tag{17}$$

Equations (16) and (17) are based on the analytical modeling of HF isolation applications that discussed in [25] and [20], respectively. In equation (16), ber, ber', bei, and bei' are Bessel functions. Modeling the skin effect led to accurate results and exact inductance values in HF that is important in EMI modeling and noise attenuation.

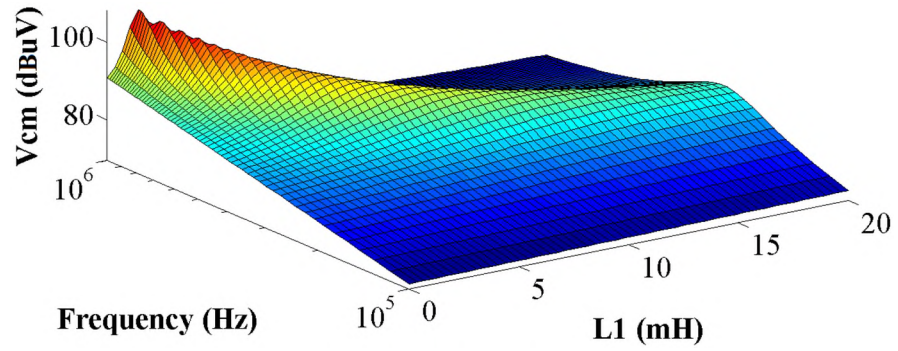
3. IMPEDANCE AND CM VOLTAGE ANALYSIS

In this section, impedances and CM noise voltage of different parts of the system is analyzed. Additionally, the effect of various capacitances and different inductance values of the EMI filter on the CM noise voltage is analyzed. Table 1 shows the system parameters, which are used in the analysis. As is clear in the previous section equations, the system CM noise voltage depends on the Z_{12}, Z_{th}, and V_{th} and these parameters are under influence of the parasitic values of the system. Hence, changing and controlling the parasitic values is a key method in CM noise voltage attenuation, especially at HF frequency bands.

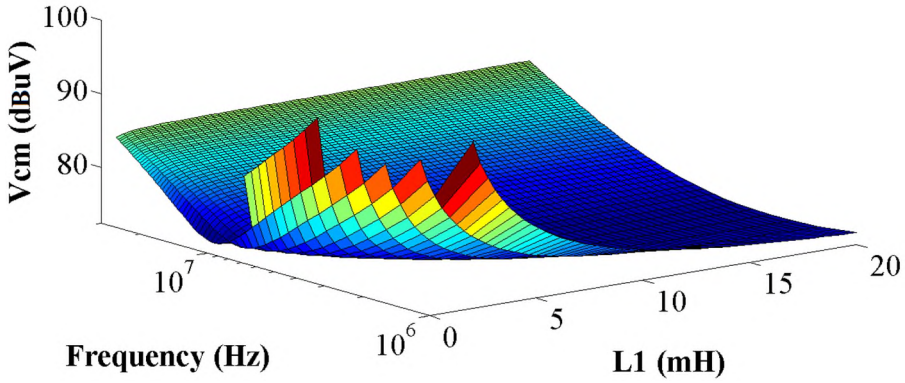
3.1. CM NOISE VOLTAGE ANALYSIS IN THE SYSTEM

CM noise voltage and impedance of the system including AC-DC-DC power supply and pulse generator is shown and analyzed here. Figure 6 shows Z_{12} impedance, which is the combination of the CM EMI filter and line inductor impedances that is shown in Figure 2. Since L_{12} (corresponded inductance of Z_{12}) is in order of mH and C_T is in order

of pF/nF, in the EMI range of 150 kHz-30 MHz, Z_{12} impedance is much higher than Z_{th}. Thus, by considering equation (14), Z_{12} is the main impedance that controls the CM noise voltage. Z_{12} impedance increases up to 1.5MHz. After 1.5MHz, Z_{12} impedance decreases due to the parasitic capacitance and the skin effect of the inductor. Changing Z_{12} impedance by using different inductance values and different inductors lead to lower CM noise voltage. Also, changing the CM filter location from AC side to DC side can alter the CM voltage.



(a)



(b)

Figure 8. CM noise voltage of the system with variable L_1. a) Frequency band of 150kHz – 1MHz. b) Frequency band of 1MHz – 30MHz.

Figure 7 shows the CM noise voltage of the system without Z_{12} EMI filter, the CM noise voltage of the system with filter, and IEC61800-3 standard limits. The IEC61800-3 limits for this category are 79dBuV and 73dBuV for the frequency band of 150kHz – 500kHz and 500kHz – 30MHz, respectively. Comparing these curves shows the importance of the CM inductor in the system. Additionally, it is clear in Figure 7 that in the system without the filter, the CM voltage is above the standard limit at the large frequency band of 260kHz – 30MHz. In the system including the filter, the CM noise voltage does not meet the standard requirements at frequency 170kHz – 450kHz, 500kHz - 1.2MHz, and above 4.4MHz. In spite of the effectiveness of the CM filter, it cannot completely satisfy the standard requirement and this means that other methods should be taken or/and the filter should be optimized.

Because of Z_{12} dominance over the Thevenin impedance, the inductor of the EMI filter can change the CM noise voltage in a wide range. However, the skin effect, parasitic capacitance, and parasitic resistance of the filter prevent the linear relation of the inductance value and the CM noise voltage over the frequency band of 150kHz – 30MHz. By varying the inductance value of the EMI filter, the CM noise voltage is calculated over the EMI frequency range and depicted in Figure 8. For a better visibility, Figure 8(a) shows the variation in the frequency band of 150kHz – 1MHz and Figure 8(b) shows the frequency band of 1MHz – 30MHz. As is clear in Figure 8(a), as the inductance increases the CM noise voltage peak reduces but occurs at a lower frequency. Moreover, in Figure 8(b) it is clear that lower inductance leads to high CM noise voltage and significant divergence from the IEC standard limit. However, Figure 8(b) shows that at the frequencies higher than 10MHz, the effectiveness of the inductor is decreased significantly. The other

important impedance that controls and affects the CM noise voltage is Z_{th}. As is clear in (14), Z_{th} is a major player in the CM noise voltage. The effect of Z_{th} is not as much as Z_{12}.

However, this impedance has a significant role along with Z_{12} for CM EMI attenuation. As shown in the equations of section 2, Z_{th} is directly related to C_T. selecting different switches and components for the system as well as adding capacitance to some specific parts of the system can change C_T that led to different Z_{th}. In order to illustrate the effect of C_T on the CM noise voltage, Figure 9 shows the 3-D variation of the CM noise voltage over frequency and parasitic capacitance. Figure 9 is showing the CM noise voltage of the system including the EMI filter. For better visibility Figure 9 is depicted in four parts.

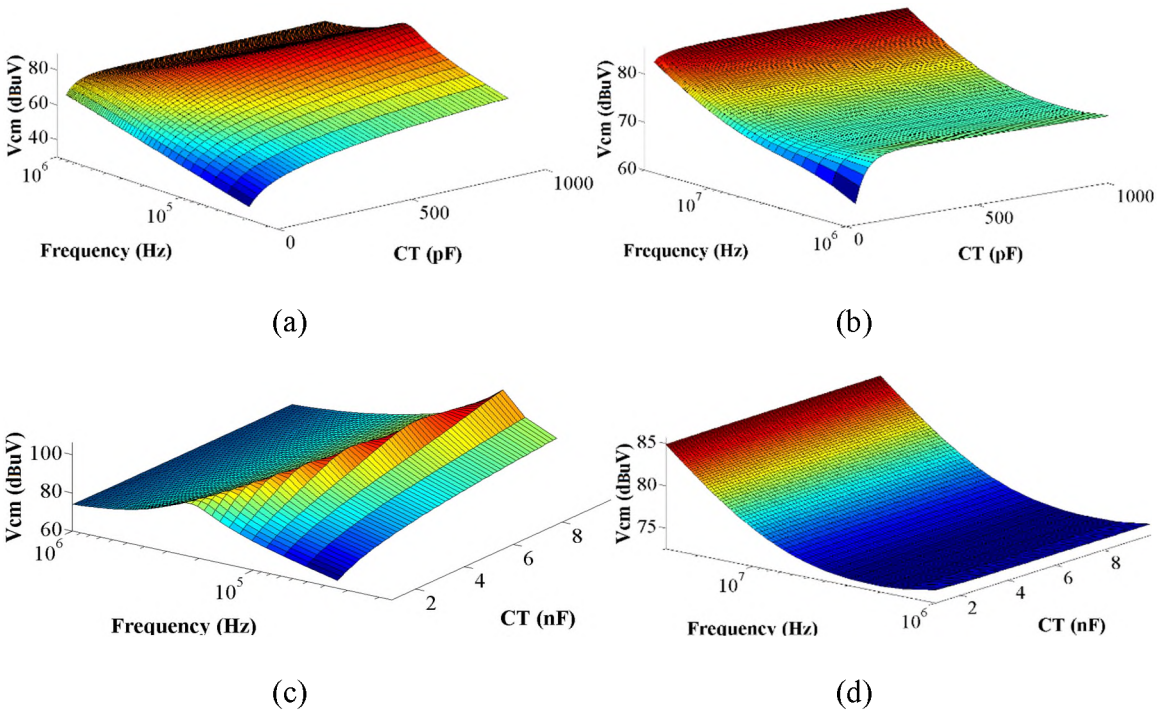


Figure 9. CM noise voltage of the system with variable C_T. a) Frequency band of under 1MHz and C_T of 0-1000pF. b) Frequency band of 1MHz – 30MHz and C_T of 0-1000pF. c) Frequency band of under 1MHz and C_T of 0-8nF. d) Frequency band of 1MHz – 30MHz and C_T of 0-8nF.

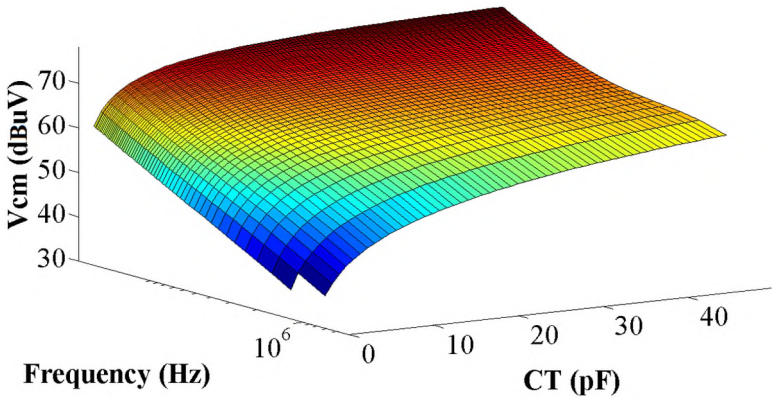


Figure 10. CM noise voltage of the system. The Frequency band is 150kHz – 30MHz and C_T of under 50pF.

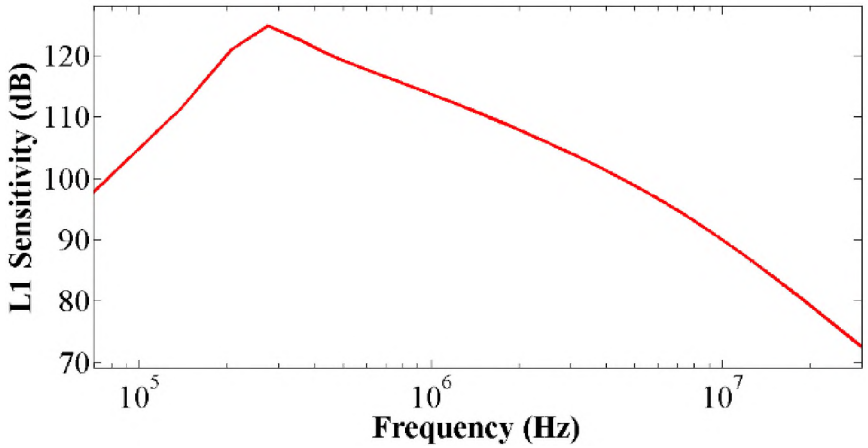


Figure 11. Sensitivity of the CM noise voltage to L_1 in the whole system.

Figure 9(a) and (b) show the CM noise voltage variation for parasitic capacitance between zero and 1000 pF and Figure 9(c) and (d) show that variation for 1nF – 10nF. Also, Figure 9(a) and (c) show the CM noise variation for frequency band of 0 – 1MHz and Figure 9(b) and (d) show that variation for 1MHz – 30MHz. As is clear in Figure 7 and Figure 9, at lower values of C_T, the difference between the CM noise voltage and IEC61800-3 is the lowest. For the frequency band of 1MHz – 30MHz, the CM noise

voltage does not change significantly for the parasitic capacitances that are higher than 100pF. Figure 10 shows the CM noise voltage over the frequency band of 150kHz –30MHz with C_T of under 50pF. As is clear in this figure, the CM noise voltage is under the limits of IEC61800-3.

Since, in most of the power electronic systems, C_T is expected to be higher than a few hundreds of Pico Farad, the noise attenuation strategy should focus on reducing C_T and/or designing an effective EMI filter. A trade-off is expected between the filter volume and adding new components to the system. Furthermore, in order for analyzing the sensitivity of the system to L_1, the following equation is defined:

$$S_{L1}^{Vcm} = \frac{dVcm}{dL_1} \cdot \frac{L_1}{Vcm} \tag{18}$$

This equation shows the sensitivity of the CM noise voltage to L_1 in the EMI frequency band. Figure 11 shows the sensitivity function. As is clear in this function, the CM noise voltage sensitivity at 250kHz is the highest and after this frequency the sensitivity decreases. This variation shows that at higher frequency bands the role of parasitic parameters in the CM noise voltage intensifies. Therefore, in EMI filter designing or other attenuation methods, the strategy should be based on decreasing the parasitic parameters influence after 250 kHz and/or placing EMI attenuation passive components by regarding the mentioned frequency.

3.2. CM NOISE VOLTAGE ANALYSIS IN AC-DC-DC POWER SUPPLY

In this part, the CM noise is analyzed for the AC-DC-DC power supply including the AC source, rectifier, and DAB DC-DC converter. This system is a popular system in

power conversion and its analysis can lead to performance improvement and efficiency enhancing.

Figure 12 shows the CM noise voltage in the AC-DC-DC power supply with different C_{TS}s. As shown in the last part, for limiting the CM noise voltage under the IEC61800-3 standard, C_T should be decreased and optimized along with the CM EMI filter. By assuming that C_T is optimized to lower the CM noise voltage, Figure 12 shows the variation of the CM noise voltage with the regular EMI filter and line inductor (Z_{12}) and C_T with Pico Farad order values. With a C_T of 1000 pF, the CM noise voltage is higher than the standard at the frequency bands of 150kHz – 400kHz, 500kHz – 600kHz, and higher than 8MHz. For C_T of 100pF and 50pF, the CM noise voltage decreased and improved. However, these capacitance values do not meet the IEC61800-3 at some frequency bands. For C_T of 10pF, the CM noise voltage meets the standard better than other capacitances, however for the frequency band of 17MHz -30MHz other attenuation methods should be considered as well.

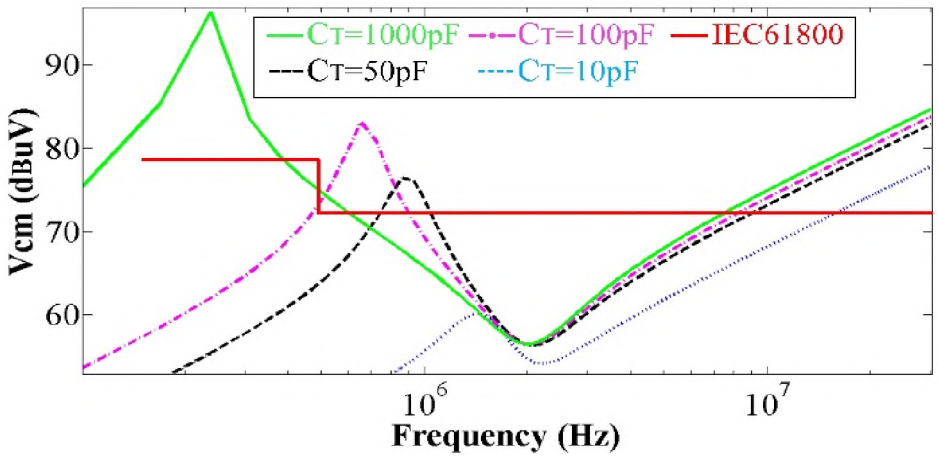


Figure 12. CM noise voltage of the AC-DC-DC power supply with different C_{TS}.

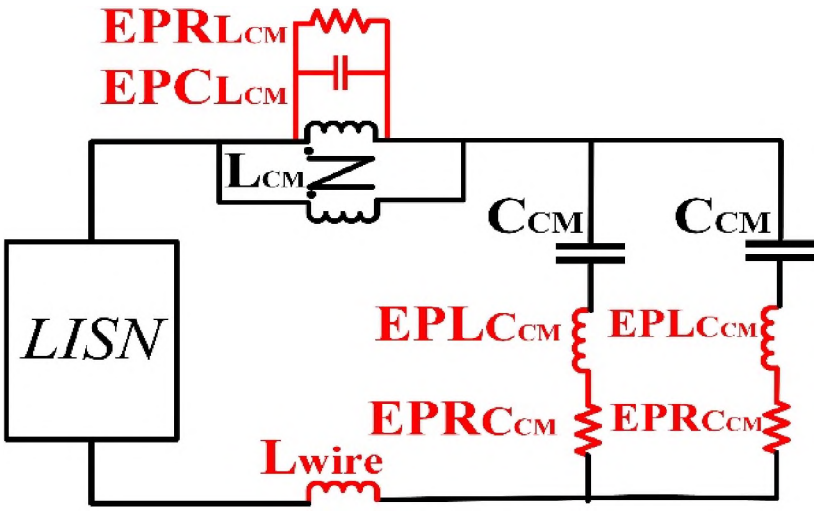


Figure 13. EMI filter circuit with parasitic parameters.

3.3. OPTIMAL EMI FILTER DESIGN FOR AC-DC-DC POWER SUPPLY

In order for effective designing of the EMI filter, Figure 13 shows the CM EMI filter with the components and parasitics. To find the inductance, capacitance, and parasitic values of the filter, equation (19) is defined. This equation is the difference of the CM noise voltage of the AC-DC-DC system and IEC61800-3 standard.

$$F = Vcm - Vcm_{IEC} = \begin{cases} Vcm - 79\ dbuV & 150\ kHz < f < 500\ kHz \\ Vcm - 73\ dbuV & 500\ kHz < f < 30\ MHz \end{cases} \quad (19)$$

Moreover, f_{cm1} and f_{cm2}, which are the cut-off frequencies are defined by the following equations:

$$f_{cm1} = 150kHz - \frac{F(150kHz)}{\frac{dF}{df}(@f{=}150kHz)} = \frac{|Vcm(@f{=}150kHz){-}79|}{\frac{d}{df}|Vcm{-}79|(@f{=}150kHz)} \quad (20)$$

$$f_{cm2} = 30MHz - \frac{F(30MHz)}{\frac{dF}{df}(@f{=}30MHz)} = \frac{|Vcm(@f{=}30MHz){-}73|}{\frac{d}{df}|Vcm{-}73|(@f{=}30MHz)} \quad (21)$$

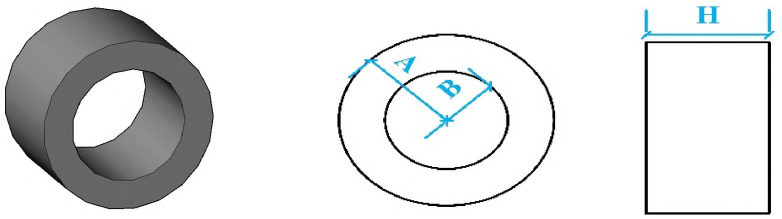
Additionally, by following the procedure explained in [5] and [26], L_{cm} and the parasitics of the filter shown in Figure 13 can be found by the following equations:

$$L_{cm} = \frac{1}{8 \cdot \pi^2 \cdot f_{cm1}^2 \cdot C_{CM}} \tag{22}$$

$$\max\{L_{wire}\} = \frac{1}{8 \cdot \pi^2 \cdot f_{cm2} \cdot f_{cm1} \cdot C_{CM}} - \frac{EPL_{C_{CM}}}{2} \tag{23}$$

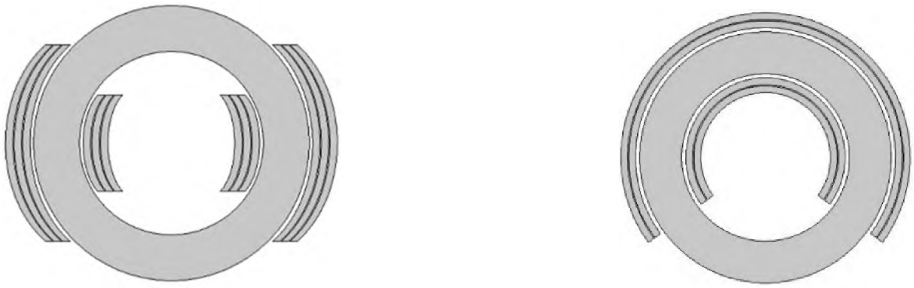
$$\max\{EPC_{L_{CM}}\} = \frac{1}{(4 \cdot \pi^2 \cdot f_{cm2}^2) \cdot (L_{wire} + \frac{EPL_{C_{CM}}}{2})} \tag{24}$$

The filter is designed based on the toroidal core in four different structures and winding configurations. Figure 14 shows the toroidal core and the side view and front view of the inductor and Figure 15 shows two winding arrangements used for the inductor. By assuming a MnZn ferrite core with a permeability of 1000, maximum flux density of 0.4T, 30 turns per winding, and by using AWG#11 for the conductors of the windings, the filter parameters are shown in Table 2. Type I and Type II are the same as winding arrangements of Figure 14(a) and Type III and Type IV are the same as winding arrangements of Figure 14(b). Table 2 shows the difference of the parameters for different winding arrangement and configuration of the same filter. For showing the temperature stability of the filter, by using FEM, Figure 16 depicts the temperature distribution and the temperature rise of all four types of the filters at steady state conditions. As is shown in Figure 16, the maximum temperature in the filters will be 390 K^o that is a 97 K^o temperature rise from the room temperature, which is under the limits of the IEC62477-1 [27] standard.



(a) (b) (c)

Figure 14. Torioidal core views. a) Toroidal core. b). Front view of the toroidal core c) Side view of the toroidal core that shows the depth of the core.



(a) (b)

Figure 15. Winding arrangements of the inductor. a) Toroidal core with 3 layers for each winding. b) Toroidal core with 1 layer for each winding.

Table 2. Filter parameters.

Parameter	Type I	Type II	Type III	Type IV
A(mm)	72	94	72	94
B(mm)	28	14	28	14
H(mm)	80	50	80	50
L_{CM}(mH)	12.5	12.5	12.5	12.5
C_{CM}(nF)	7.5	7.5	7.5	7.5
EPR_{LCM}(kΩ)	9	9	14	14
EPC_{LCM}(pF)	64	56	25	18
Lwire(uH)	7.5	7.5	4.3	4.3
EPL_{CCM}(nH)	7	7	7	7
EPR_{CCM}(mΩ)	180	180	180	180

By using the designed filter and assuming the Z_{12} is as the line inductor of the system, the CM noise voltage for different C_{TS} are shown in Figure 17. As is shown in

Figure 17 the CM noise voltage is controlled under the standard limits for all four possible C_T of the system. However, the CM filter does not show significant progress compared to the conventional EMI filters regarding performance, volume, and power loss. Hence, limiting the CM noise with the conventional filter is not still the optimal solution. Using balance technique, decoupled inductors, and hybrid techniques with small and optimal CM filters can be the effective alternatives.

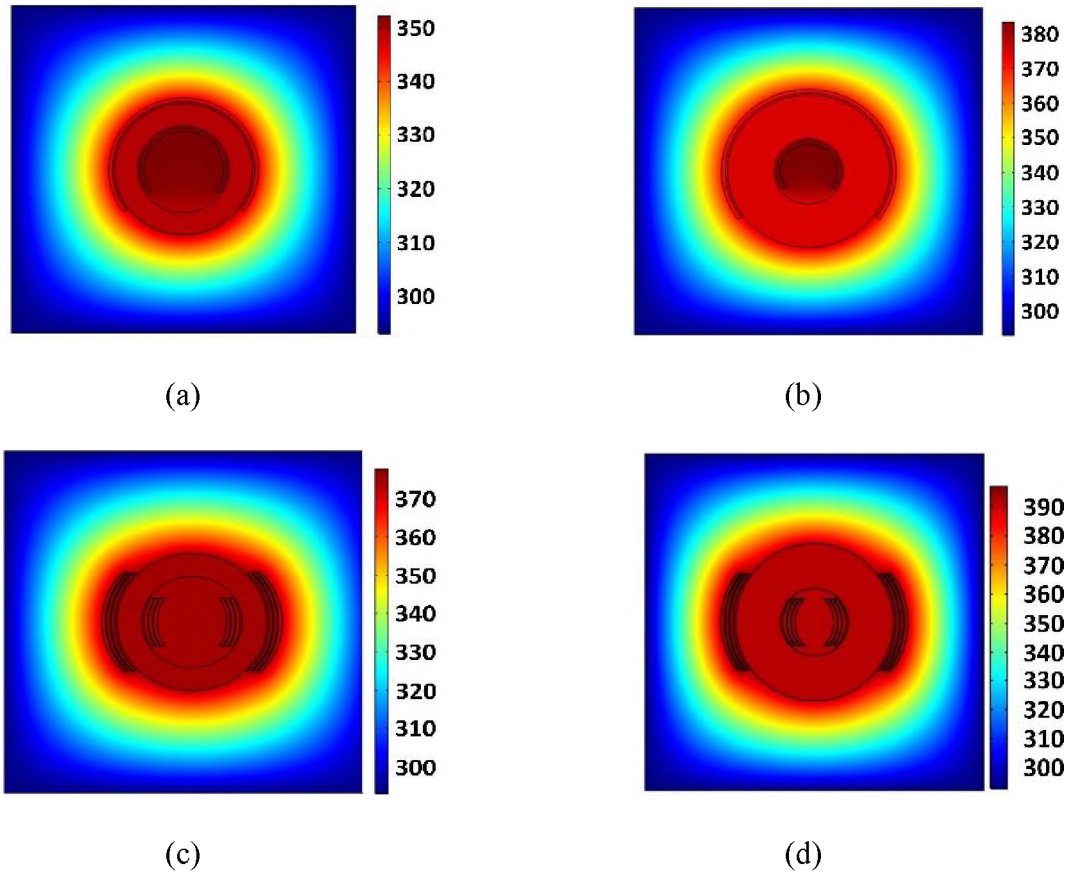


Figure 16. Temperature distribution of the inductor of the EMI filter. a) Type I. b) Type II. c) Type III. d) Type IV.

Moreover, by using equation (18), the CM noise voltage sensitivity to L_1 in the AC-DC-DC power supply is shown in Figure 18. The sensitivity after 2MHz starts to decrease. This frequency is almost 8 times of the corresponding frequency for the whole system.

4. CM NOISE ATTENUATION TECHNIQUES

In this section the EMI noise reduction methods are used and analyzed to attenuate the CM noise of the system along with optimizing and minifying the EMI filter. The balance technique that is based on the Wheatstone bridge and superposition theorem is the first method that is analyzed here. Furthermore, by using an added inductor for the pulse generator that is placed in the grounding path, the CM noise impedance increases and leads to lower EMI. The effect of the added inductor on the CM noise voltage is analyzed. This inductance also creates a safety impedance in the grounding route during the short circuit faults.

4.1. BALANCE TECHNIQUE FOR NOISE SOURCES

By short circuiting all voltage sources except V_{34}, the equivalent circuit of Figure 5(a) can be reduced to Figure 19. $\hat{Z}_1$ is defined in the following equation:

$$\hat{Z}_1 = \left[\left(Zr||Zghkl||(2Zf)\right) + Zps13\right]||(2Zd) \tag{25}$$

Based on the Wheatstone bridge, equation (26) should be satisfied to minimize the effect of the noise source. This requires to parallel an additional capacitor with C_{bce}, which is explained in the balance technique of V_{78}. The other technique that can be used here is to

add $\hat{Z}_{11}$to the system, as shown in Figure 20. The new balance equation is defined in equation (27).

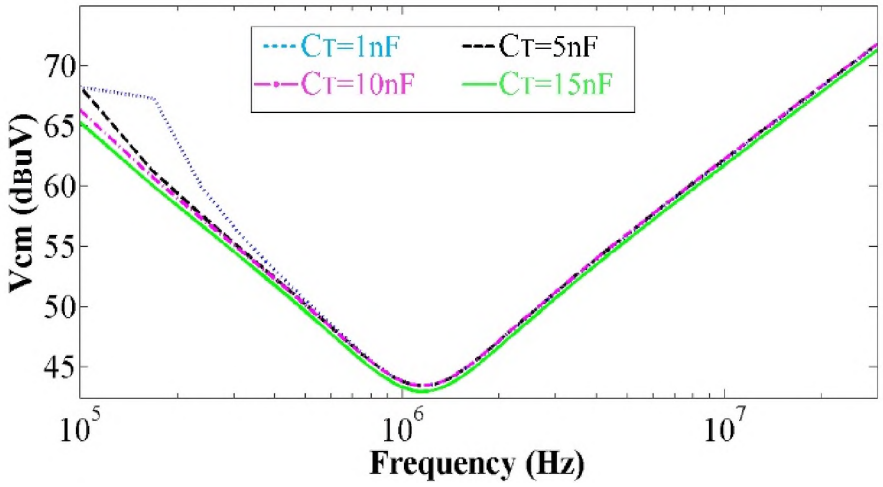


Figure 17. CM noise voltage of the AC-DC-DC power supply. The optimized designed EMI filter with various C_Ts were applied.

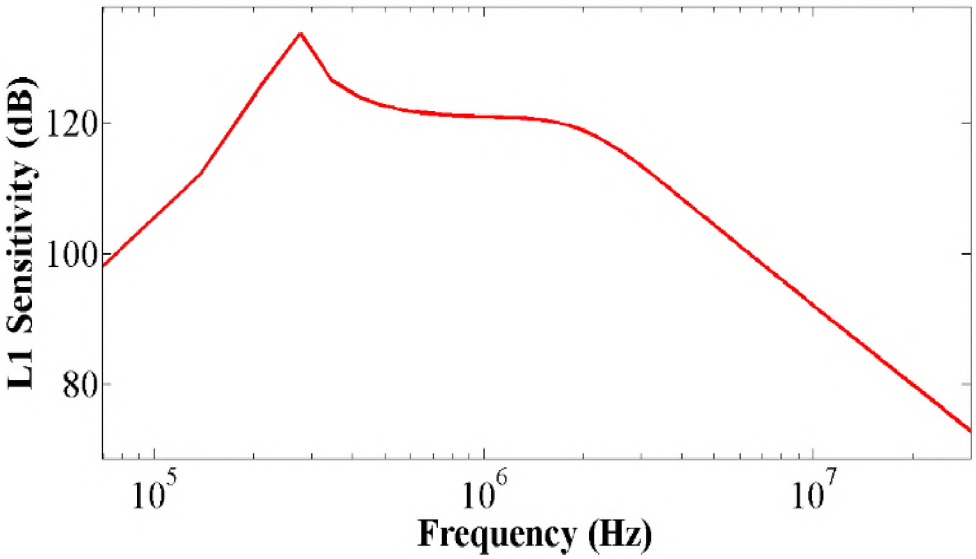


Figure 18. Sensitivity of the CM noise voltage to L_1 in the power supply.

$$\frac{Cbce}{2Ca} = \frac{Z_{LISN}+Z12}{\hat{Z}_1} \tag{26}$$

$$\frac{Cbce}{2Ca} = \frac{Z12}{\hat{Z}_{11}} \tag{27}$$

By assuming $\hat{Z}_{11}$ to be 20nF, the CM noise voltage at low frequencies and middle frequencies attenuates.

By using the balance technique for the noise source of V_{78}, the reduced equivalent circuit can be depicted in Figure 21. $\hat{Z}_2$ and $\hat{Z}_3$ are defined in the following equations:

$$\hat{Z}_2 = [Z_{LISN} + Z12]||(2Za) \tag{28}$$

$$\hat{Z}_3 = \left[\left(Zr||Zghkl||(2Zf)\right) + Zps13\right] \tag{29}$$

The balance equation of V_{78} noise voltage is defined in the following equation:

$$\frac{Cbce}{2Cd} = \frac{\hat{Z}_3}{\hat{Z}_2} \tag{30}$$

In order for closing the right side and the left side of the equation (30) together, C_{a1} = 5nF is added to the ground path of the rectifier. This capacitor is paralleled to C_{bce} capacitor and increases the ground path capacitance of the rectifier and low voltage side of DAB. The effect of this added capacitor in middle frequencies is higher than low and high frequency bands.

Moreover, the balance technique is used for V_{1112} and the equivalent circuit is shown in Figure 22. $\hat{Z}_4$ and the balance equation are defined in the following equations:

$$\hat{Z}_4 = [(Z_{LISN} + Z12)||(2Za)||Zbce||(2Zd)] + Zps13 \tag{31}$$

To reduce the noise effect of V_{1112}, C_{a2}=8nF is added to the ground path that is paralleled to C_{ghkl}. This added capacitor is effective at low frequency bands and can decrease the amplitude of the CM noise voltage at some low frequency peaks.

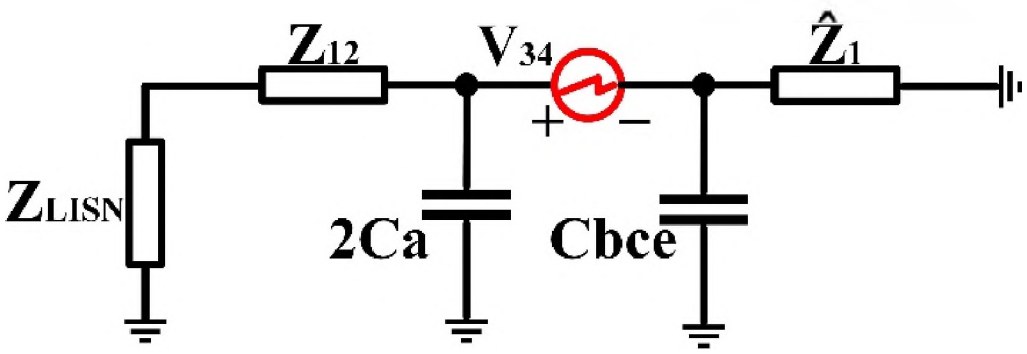


Figure 19. Balance technique equivalent circuit for V_{34}.

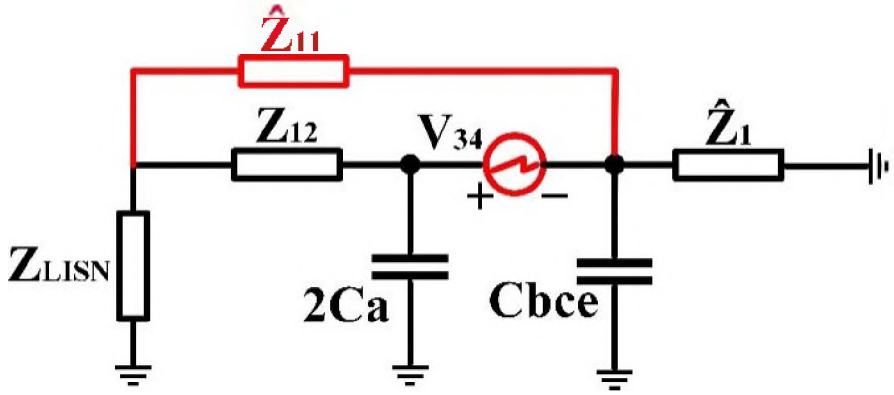


Figure 20. Balance technique equivalent circuit for V_{34} with added component.

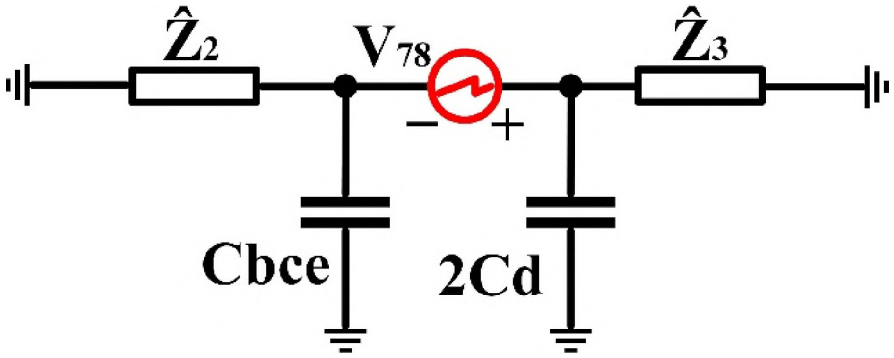


Figure 21. Balance technique equivalent circuit for V_{78}.

The other noise source that should be analyzed here is V_{D1}. For balancing the noise source, $\hat{Z}_{55}$ is added to the ground path of the pulse generator, paralleled with Cr. The equivalent circuit is illustrated in Figure 23. $\hat{Z}_5$ and the balance equation are shown here:

$$\hat{Z}_5 = [((Z_{LISN} + Z12)||(2Za)||Zbce||(2Zd)) + Zps13]||(2Zf) \quad (32)$$

$$\frac{Cr}{Cghkl} = \frac{\hat{Z}_5}{\hat{Z}_{55}} \quad (33)$$

By considering the balance equation, $\hat{Z}_5$ is considered 10nF. This added capacitor reduces the CM noise voltage in most of the frequency bands, even high frequencies. This added capacitor increases the impedance of the CM noise regardless of the frequency band.

4.2. ADDING FILTERING INDUCTOR FOR PULSE GENERATOR

Instead of grounding the pulse generator directly, an additional inductor is added in the grounding path. This inductor not only provides a safe path for passing the possible fault currents, but also increases the CM noise impedance in the EMI analysis. Figure 24 shows the added inductor configuration. Based on the IEC62477-1 safety standard, a 75µH inductor is used here for the pulse generator grounding.

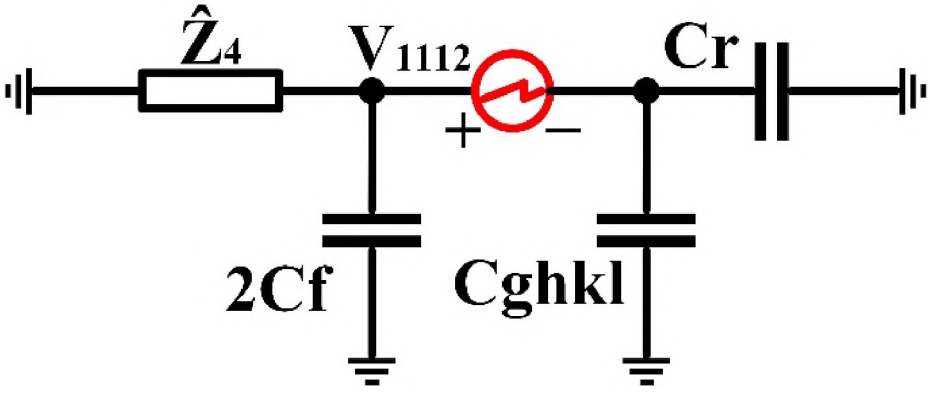


Figure 22. Balance technique equivalent circuit for V_{1112}.

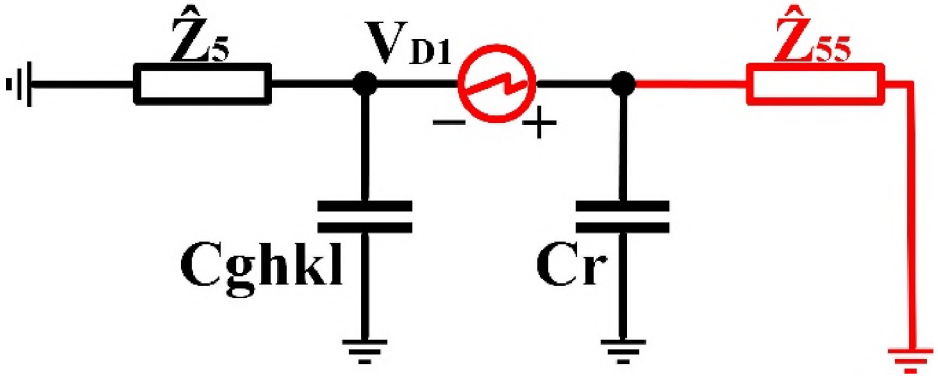


Figure 23. Balance technique equivalent circuit for V_{D1} with added component.

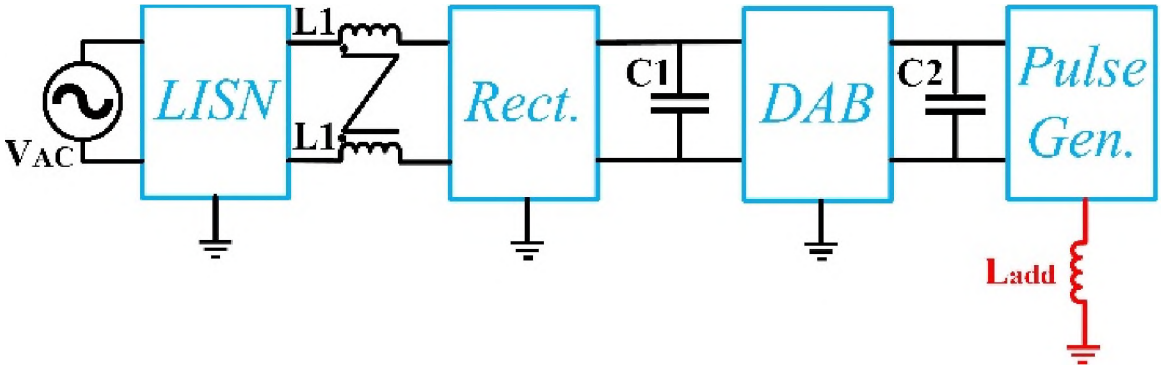


Figure 24. Filtering inductor added to the pulse generator.

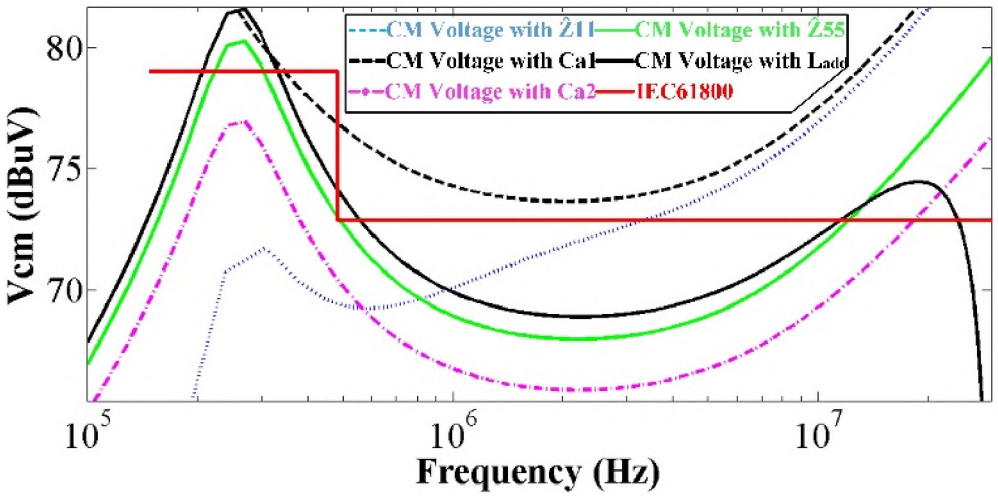


Figure 25. CM noise voltage of the system with added components.

4.3. CM NOISE WITH ADDED COMPONENTS AND FINAL SCHEME

In the last two parts, by using the balance technique and filtering inductor, the CM noise voltage is balanced and reduced. Figure 25 shows the CM noise voltage variation over frequency by regarding the balance components and the filtering inductor. In Figure 25, the CM noise voltage for each added component is shown with only the corresponding component and the line inductor and the filter combination of Z_{12}.

As is clear in Figure 25, each of the added capacitors or the inductor, cannot completely reduce the CM noise voltage under the standard limits. However, each added component is able to attenuate the CM EMI for some frequency bands or reduce the amplitude of the CM noise voltage for several decibels.

Figure 26 shows the CM noise voltage of the whole system by considering all balance components and the added inductor. As is shown in this figure, the CM noise

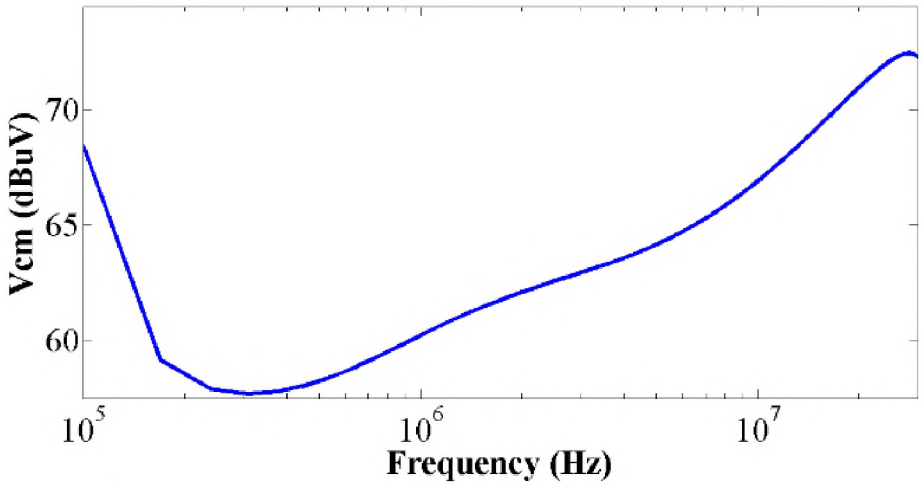


Figure 26. CM noise voltage of the system with all added components.

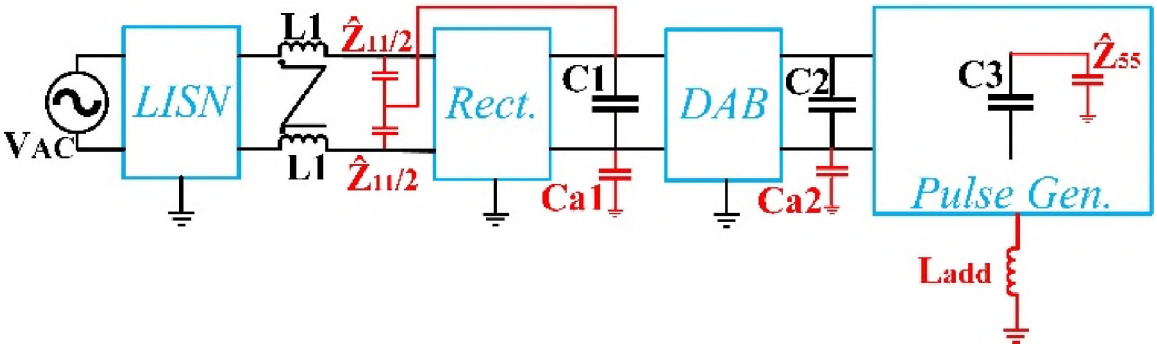


Figure 27. Added components to the system for EMI reduction.

voltage is well below the IEC61800-3. Figure 26 shows the effectiveness of the proposed methods for noise attenuating. Moreover, Figure 27 illustrates the final scheme of the proposed system that keeps the EMI noise under the standard limits and this figure shows the added components. This configuration is comparable with the designed filter that explained in section 3.

To satisfy the IEC61800-3 standard and keeping the system immune from the EMI noise, both proposed scheme of Figure 27 and the designed filter can be used. However, using the proposed method of Figure 27 instead of the designed filter can increase the system efficiency and lower the system volume. The system volume depends on the magnetic design and can vary in each system. In the system explained in this paper by using the proposed scheme of Figure 27, the magnetic components of the EMI noise attenuation can decrease up to 60% compared to the regular filter that is described in section 3.

At the end it is important to compare the results with the experimental measurements for validation. Table 3 shows the maximum deviation (dB) from the

experimental measurements of the references that have similar arrangements and noise behavior for the converters of this paper, which compensated with Wheatstone bridge technique (WBT) and EMI filter.

In comparing the noise level results of this paper with experimental measurements of the references, the number of noise sources and EMI propagation paths in the corresponded converters were considered. This comparison method is based on equivalent circuit of the EMI noise circulation and number of noise sources. As shown in Table 3, there is a good agreement between the EMI noise results of this paper and the experimental measurements of the references. The maximum deviation is less than 10% of the standard limit.

Table 3. Maximum deviation from experimental measurements of the references (dB).

	References	Rectifier Converter	DAB Converter	Whole System
Systems Compensated with WBT and EMI Filter	[10]	N/A	<5	N/A
	[14]	<3	N/A	N/A
	[17]	N/A	<4	N/A
	[18]	<5	N/A	<3
	[28]	<6	N/A	N/A
	[29]	<3	N/A	<5
	[30]	N/A	N/A	<5

5. CONCLUSION

In this paper, EMC modeling of a pulse generator including an AC-DC-DC power supply is explained and analyzed. Additionally, conducted CM EMI analysis of the system is investigated by considering EMI filter effect, the parasitic parameters of the components, and the CM noise flowing in the circuits. The system components showed different weights in the EMI analysis and some of the noise sources did not show a significant role in the CM noise flowing, since the CM noise produced by those did not flow through the LISN. Based on the impedances and noise analysis of the EMI equivalent circuit, the system without EMI filter optimization and without adding additional components could not meet the IEC61800-3. To meet the standard requirements, some EMI reduction techniques were used for the system. The results show that each technique cannot lower the EMI noise under the IEC standard by itself. However, applying all the techniques together into the system and using required values for the added components in the suitable place in the circuit is very effective in meeting the standard limits. The results showed that it is possible to reduce the CM noise voltage to the desirable level by using an optimized EMI filter alone. However, adding new components based on the EMI reduction techniques will lead to a way smaller EMI filter, which reduces the overall size of the system and increases the efficiency and performance. At the end, it is important to note that each system and power converter require specific EMI reduction techniques and EMI filter optimization, and compromising between the filter size and added components is necessary for the better performance and higher efficiency.

REFERENCES

[1] M. Ma, T. Wei, Z. Xu, Z. Xu, H. Li and W. Qunjing, "Electromagnetic Interference Analysis of Permanent Magnet Linear Synchronous Launchers," in *IEEE Transactions on Plasma Science*, vol. 48, no. 5, pp. 1309-1315, May 2020.

[2] L. Gharib and A. Keshtkar, "Electromagnetic Interference of Railgun and Its Effect on Surrounding Electronics," in *IEEE Transactions on Plasma Science*, vol. 47, no. 8, pp. 4196-4202, Aug. 2019.

[3] W. Xu, H. Xu, F. Liu, H. Hu and J. Feng, "Electromagnetic Compatibility in Electron Cyclotron Resonance Heating System," in *IEEE Transactions on Plasma Science*, vol. 47, no. 5, pp. 1887-1894, May 2019.

[4] L. Gharib, A. Keshtkar and A. Ghorbani, "Electromagnetic Compatibility and Current Pulse of Railgun," in *IEEE Transactions on Plasma Science*, vol. 45, no. 7, pp. 1453-1458, July 2017.

[5] Y. Maillet, R. Lai, S. Wang, F. Wang, R. Burgos and D. Boroyevich, "High-Density EMI Filter Design for DC-Fed Motor Drives," in *IEEE Transactions on Power Electronics*, vol. 25, no. 5, pp. 1163-1172, May 2010.

[6] A. Videt, M. Messaoudi, N. Idir, H. Boulharts, and H. Vang, "PWM strategy for the cancellation of common-mode voltage generated by threephase back-to-back inverters," *IEEE Transactions on Power Electronics*, vol. 32, no. 4, pp. 2675–2686, Apr. 2017.

[7] L. Yang, S. Wang, H. Zhao, and Y. Zhi, "Prediction and analysis of EMI spectrum based on the operating principle of EMC spectrum analyzers," *IEEE Transactions on Power Electronics*, vol. 35, no. 1, pp. 263–275, Jan. 2020.

[8] Y. Bai, X. Yang, D. Zhang, X. Li, W. Chen, and W. Hu, "Conducted EMI mitigation schemes in isolated switching-mode power supply without the need of a Y-capacitor," *IEEE Transactions on Power Electronics*, vol. 32, no. 4, pp. 2687–2703, Apr. 2017.

[9] S. Mohsenzade, M. Aghaei, and S. Kaboli, "Leakage inductance calculation of the transformers with disordered windings," *IEEE Transactions on Plasma Science*, vol. 47, no. 4, pp. 1799–1807, Apr. 2019.

[10] H. Zhang, S. Wang, Y. Li, Q. Wang and D. Fu, "Two-Capacitor Transformer Winding Capacitance Models for Common-Mode EMI Noise Analysis in Isolated DC–DC Converters," in *IEEE Transactions on Power Electronics*, vol. 32, no. 11, pp. 8458-8469, Nov. 2017.

[11] M. S. Sanjari Nia, M. Altimania, P. Shamsi and M. Ferdowsi, "Electric Field and Parasitic Capacitance Analysis for HF Transformers with Coaxial Winding Arrangements," *2020 IEEE Kansas Power and Energy Conference (KPEC)*, Manhattan, KS, USA, 2020, pp. 1-5.

[12] J. Kołek and M. Hołub, "Practical Design of a High-Voltage Pulsed Power Supply Implementing SiC Technology for Atmospheric Pressure Plasma Reactors," *Applied Sciences*, vol. 9, no. 7, p. 1451, 2019.

[13] P. Kong, S. Wang, F. C. Lee and Z. Wang, "Reducing Common-Mode Noise in Two-Switch Forward Converter," in *IEEE Transactions on Power Electronics*, vol. 26, no. 5, pp. 1522-1533, May 2011.

[14] R. Goswami and S. Wang, "Investigation and Modeling of Combined Feedforward and Feedback Control Schemes to Improve the Performance of Differential Mode Active EMI Filters in AC–DC Power Converters," in *IEEE Transactions on Industrial Electronics*, vol. 66, no. 8, pp. 6538-6548, Aug. 2019.

[15] Y. Li, H. Zhang, S. Wang, H. Sheng, C. P. Chng and S. Lakshmikanthan, "Investigating Switching Transformers for Common Mode EMI Reduction to Remove Common Mode EMI Filters and Y-Capacitors in Flyback Converters," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 6, no. 4, pp. 2287-2301, Dec. 2018.

[16] S. Wang and F. C. Lee, "Common-Mode Noise Reduction for Power Factor Correction Circuit with Parasitic Capacitance Cancellation," in *IEEE Transactions on Electromagnetic Compatibility*, vol. 49, no. 3, pp. 537-542, Aug. 2007.

[17] Y. Li, S. Wang, H. Sheng and S. Lakshmikanthan, "Investigate and Reduce Capacitive Couplings in a Flyback Adapter with a DC-Bus Filter to Reduce EMI," in *IEEE Transactions on Power Electronics*, vol. 35, no. 7, pp. 6963-6973, July 2020.

[18] L. Yang, H. Zhao, S. Wang and Y. Zhi, "Common-Mode EMI Noise Analysis and Reduction for AC–DC–AC Systems with Paralleled Power Modules," in *IEEE Transactions on Power Electronics*, vol. 35, no. 7, pp. 6989-7000, July 2020.

[19] D. Fu, S. Wang, P. Kong, F. C. Lee and D. Huang, "Novel Techniques to Suppress the Common-Mode EMI Noise Caused by Transformer Parasitic Capacitances in DC–DC Converters," in *IEEE Transactions on Industrial Electronics*, vol. 60, no. 11, pp. 4968-4977, Nov. 2013.

[20] M. S. Sanjari Nia, P. Shamsi and M. Ferdowsi, "Investigation of Various Transformer Topologies for HF Isolation Applications," in *IEEE Transactions on Plasma Science*, vol. 48, no. 2, pp. 512-521, Feb. 2020.

[21] S. Wang, P. Kong and F. C. Lee, "Common Mode Noise Reduction for Boost Converters Using General Balance Technique," in *IEEE Transactions on Power Electronics*, vol. 22, no. 4, pp. 1410-1416, July 2007.

[22] *Adjustable Speed Electrical Power Drive Systems-Part 3: EMC Requirements and Specific Test Methods,* IEC61800-3, 2012.

[23] Y. Chu and S. Wang, "A Generalized Common-Mode Current Cancelation Approach for Power Converters," in *IEEE Transactions on Industrial Electronics*, vol. 62, no. 7, pp. 4130-4140, July 2015.

[24] M. S. Sanjari Nia, M. Altimania, P. Shamsi and M. Ferdowsi, "Magnetic Field Analysis for HF Transformers with Coaxial Winding Arrangements," *2020 IEEE Kansas Power and Energy Conference (KPEC),* Manhattan, KS, USA, 2020, pp. 1-5.

[25] O. Gatous and J. Pissolato, "Frequency-dependent skin-effect formulation for resistance and internal inductance of a solid cylindrical conductor," *IEE Proceedings – Microwaves, Antennas and Propagation*, vol. 151, no. 3, p. 212, 2004.

[26] J. L. Kotny, T. Duquesne and N. Idir, "EMI Filter design using high frequency models of the passive components," *2011 IEEE 15th Workshop on Signal Propagation on Interconnects (SPI)*, Naples, 2011, pp. 143-146.

[27] *Safety requirements for power electronic converter systems and equipment - Part 1: General,* IEC62477-1, 2012.

[28] R. Goswami, S. Wang, E. Solodovnik and K. J. Karimi, "Differential Mode Active EMI Filter Design for a Boost Power Factor Correction AC/DC Converter," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 1, pp. 576-590, 2019.

[29] L. Yang, H. Zhao, S. Wang, Y. Zhi, B. Zhu and J. Min, "Develop common-mode EMI noise models for AC-DC-AC traction systems," *IECON 2017 – 43rd Annual Conference of the IEEE Industrial Electronics Society*, Beijing, 2017.

[30] H. Zhang, L. Yang, S. Wang and J. Puukko, "Common-Mode EMI Noise Modeling and Reduction with Balance Technique for Three-Level Neutral Point Clamped Topology," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 9, pp. 7563-7573, 2017.

SECTION

2. CONCLUSIONS

This dissertation focused on the EMI noise modeling, analysis, and mitigation in the power electronics systems. The EMI noise was analyzed and mitigated through analyzing and optimizing the components such as HF transformers, inductors, and capacitors; moreover, using the mitigation techniques and filtering. The results show that optimizing the components and accurate analysis were very effective in EMI noise attenuation. Furthermore, using other attenuation techniques separately and/or along with the mentioned optimization were significant in limiting the EMI noise level under the standard boundaries.

In the first paper, the novel and accurate methodology based on analytical method, FEM, and experimental developed for finding the parasitic parameters of an HF transformer. The results show that for one transformer with the same electric and magnetic parameters, there can be a range of different values for parasitic parameters. Compromising between parasitic values by selecting winding arrangement and transformer structure can relate to other design factors, such as the facility of insulating, specific application, transformer magnetic core selection and designing strategies, etc. The proposed methodology in this paper shows that the transformer designing process, selected insulating materials, insulation strategy, and winding arrangements cause a wide range of parasitic behavior, which should be taken into account for an optimal design to minimize CM noise and reduce EMI in the systems.

In the second paper, the results not only present accurate parasitic parameters modeling but also present how the HF transformer can be optimized for EMI purposes and also shows the EMI variations based on the models and optimization. The EMI noise level of the system was obtained and compared to the IEC61800-3 standard. The optimized geometry structures were designed to show low-level parasitics. For this aim, pareto-optimal techniques implemented into the cost function that defined based on the transformer parasitics. The optimization could reduce the EMI propagation and reduce the EMI noise under the IEC61800-3 standard limitations.

In the third paper, to meet the standard requirements, some EMI reduction techniques were used for the system. The results show that each technique cannot lower the EMI noise under the IEC standard by itself. However, applying all the techniques together into the system and using required values for the added components in the suitable place in the circuit is very effective in meeting the standard limits. The results showed that it is possible to reduce the CM noise voltage to the desirable level by using an optimized EMI filter alone. However, adding new components based on the EMI reduction techniques will lead to a way smaller EMI filter, which reduces the overall size of the system and increases the efficiency and performance.

REFERENCES

[1] Y. Xiang, Y. Wang, S. Xia and F. Teng, "Charging Load Pattern Extraction for Residential Electric Vehicles: A Training-free Non-intrusive Method," in *IEEE Transactions on Industrial Informatics*, 2021.

[2] J. Chen, X. Du, Q. Luo, X. Zhang, P. Sun and L. Zhou, "A Review of Switching Oscillations of Wide Bandgap Semiconductor Devices," in *IEEE Transactions on Power Electronics*, vol. 35, no. 12, pp. 13182-13199, Dec. 2020.

[3] Y. Xuan, X. Yang, W. Chen, T. Liu and X. Hao, "A Novel Three-Level CLLC Resonant DC–DC Converter for Bidirectional EV Charger in DC Microgrids," in *IEEE Transactions on Industrial Electronics*, vol. 68, no. 3, pp. 2334-2344, March 2021.

[4] A. Kumar, A. Ravichandran, S. Singh, S. Shah, and S. Bhattacharya, "An intelligent medium voltage gate driver with enhanced short circuit protection scheme for 10kV 4H-SiC MOSFETs," 2017 IEEE Energy Conversion Congress and Exposition (ECCE), 2017.

VITA

Mohamad Saleh Sanjari Nia received his B.Sc. degree in Electrical Engineering from the University of Tehran, Tehran, Iran, in 2015 and his M.Sc. degree in Electrical Engineering from Iran University of Science and Technology, Tehran, Iran in 2018. From 2018 to 2021, he worked as Graduate Research Assistant with the subject of "*Modeling and Analyzing Parasitic Parameters in High Frequency Converters*" focused on EMI/EMC analysis and design in power electronics, at Missouri University of Science and Technology. His research interests included power electronics, EMI/EMC, electric vehicles, high voltage, and control systems. In May 2021, he received his Ph.D. degree in Electrical Engineering from Missouri University of Science and Technology, Rolla, MO.