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A PHYSICS-BASED PI PRE-LAYOUT TOOL FOR PCB PDN DESIGN

by

SHUANG LIANG

A THESIS

Presented to the Graduate Faculty of the

MISSOURI UNIVERSITY OF SCIENCE AND TECHNOLOGY

In Partial Fulfillment of the Requirements for the Degree

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

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ABSTRACT

With increasingly stringent requirements for lower voltage supply, and higher density in PCB PDN design, now integrity (PI) is an increasingly important aspect that must be considered. A pre-layout tool based on the Cavity Model and Boundary Element Method is built to automatically achieve a specified target impedance for a multi-layered Printed Circuit Board (PCB) Power Distribution Network (PDN) design with a minimal number of decoupling capacitors.

The pre-work about the post-layout design and analysis is proposed and the guidelines for creating a decoupling capacitors network with better performance has been built. With limit inputs, physical limitations for the minimal impedance that can be achieved in PDN system are calculated first to determine if a design is physically realizable and provide feedback to the user. The decoupling capacitor location will be determined by physics. Then a special decoupling capacitor selection algorithm through poles and zeros is utilized to determine which decoupling capacitor from a library should be added. Finally, the target impedance could be achieved using the minimum number of decoupling capacitors. Genetic algorithm is utilized to verify the performance and time cost of the new designed algorithm and several industry designs are used to verify the calculation result. The process is quite time-saving and convenient, and allows the user to do design discovery quickly, and determine the limiting factors under different conditions.

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1. INTRODUCTION

As we enter the era of large-scale integrated circuit (IC) systems, Moore's Law – the number of transistors in a dense IC doubles about every two years – places greater demands on system design. To achieve higher speed and density, lower power consumption and higher transient currents, engineers need to consider about how to design a system – level power distribution network (PDN) that meet engineering requirements with better performance and greater stability under a variety of constraints. This difficulty comes from two sources: on the one hand, the modeling methods used to solve the problems are loss of use with the accelerated complexity of the printed circuit board (PCB); on the other hand, in the conditions of Moore's law, the time leaving for scholars to solve the model is gradually compressed, that is, researchers are required to use less time to handle more complicated issues.

There are many considerations and constraints for PCB design, however, power integrity (PI) is a major bottleneck faced by system today [1]. As data rates increase, with higher power consumption of ICs and ASICS, and lower signal voltages, there is often more focus on the signal integrity (SI) design in a high-speed electronic system. However, because of the advancement of semiconductors and packaging technology, the maximum tolerable power voltage ripple on the PCBs has also significantly reduced [2]. As a result, the reduction of the voltage noise margin makes it harder to meet the power transmission requirements under new demands, which poses challenges for the design and power integrity analysis of power distribution networks (PDNs) in contemporary electronic systems.

In general, the function of PDN is to establish a current path to deliver power to a PCB device. A typical PCB PDN, which is illustrated in Figure 1.1, mainly includes the power and the decoupling capacitor network, voltage regulator modules (VRM), and several network cabling. For convenience, decoupling capacitor or decoupling capacitors would be referred as “decap or decaps” in this thesis. At the center point there is a packaged IC part. IC is mounted on the mainboard with a power supply through a socket, where the voltage is transformed from the source to IC through VRM.

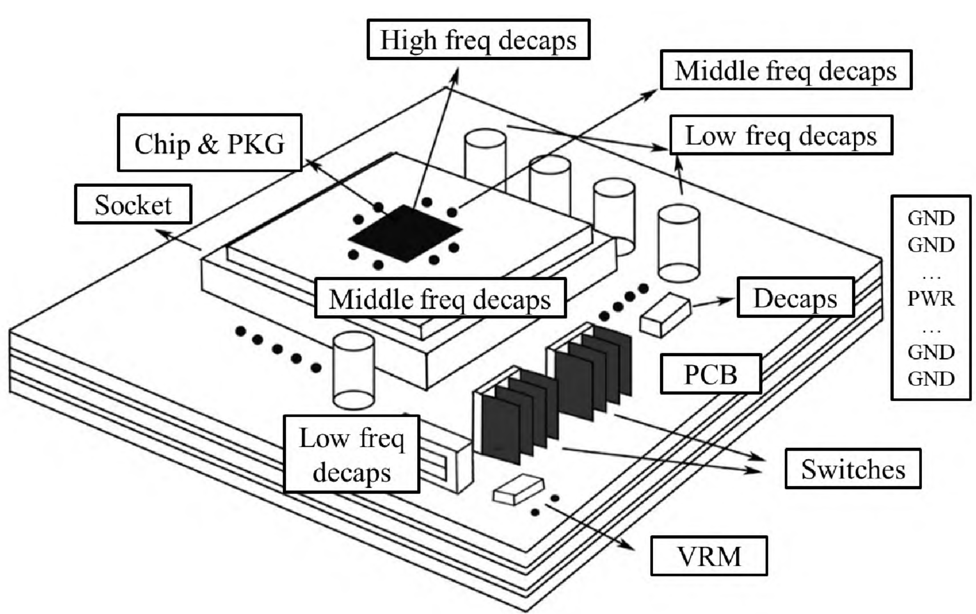


Figure 1.1 A typical PCB PDN system.

Because of the parasitic parameters in the PDN system, voltage ripple would be generated from the transient current caused by the switching circuit in the ICs, and there would be PI problems from the voltage drop at the power supplies, which would have a bad impact on the performance and usage of the PDN. The voltage drop at the IC port can

not only slow down the electron transfer rate on the transistor, but also prevent the transistor from switching states. Meanwhile, the increased voltage at the IC port can cause reliability issues and even lead to the damage of the PCB. Therefore, the impedance from the VRM to the IC section, which is usually defined as PDN impedance (Figure 1.2), should meet the requirements of the target impedance so that the DC current fluctuations would not affect the working states of all transistors. At the same time, electromagnetic interference (EMI) problems and signal integrity (SI) problems of a PDN system could also be caused by various aspects [3]-[9], such as, the noise from the IC switching current, the coupling from the voltage ripple through different DC supplies and nearby signals, the radiation from the discontinuities on the boards and so on [10].

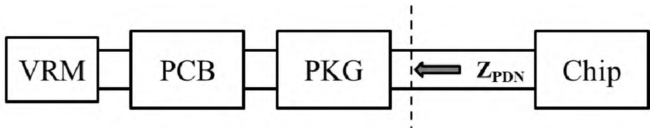


Figure 1.2 The system PDN diagram and PDN impedance definition.

In the process of modern technology development, multilayer PCBs (more than 20 – 30 layers), also with multiple power layers and power nets, have gradually replaced single-layer boards as the mainstream in the industry. Fundamentally speaking, in order to solve PDN problem, it is necessary to implement a better system design with minimized PDN impedance as seen looking from the IC because of the complex systems. There are many methods generated to analysis PI problem, to be specific, including the resonant Cavity Model, Partial Element Equivalent Circuit (PEEC), Boundary Element Method

(BEM), and so on. Also, several commercial tools could be used to simulate the performance of a designed PDN, such as CST, Matlab, PowerSI and so on.

This thesis will start from the power supply integrity problem, and then propose a system understanding about the post-layout PCB PDN design from the theoretical basis to the establishment of a reasonable pre-layout PCB PDN tool with the application of real products. The main idea is that if engineers can have a better analysis and prediction of various performance of the PDN system at the early stage of design, users can find and solve the hidden power integrity problems as much as possible to minimize the possibility of product development failure and improve circuit reliability, which can not only reduce the cost, but also shorten the development time and provide a better reference for the subsequent design solutions.

2. PHYSICS BASED PCB PDN MODELING METHOD

The PDN impedance should be carefully designed and minimized to achieve the required performance. For multilayer boards, designers have the flexibility to control the location of power layer in the board, the placement of decaps, and the number, distance, and arrangement pattern of decaps and each of these design options can affect the performance of the input impedance [11]-[16]. To meet the requirements, the PDN impedance (referred as Z_{PDN}) must be designed smaller than the target impedance, which is set to achieve voltage ripple specifications.

Then the verification of the PDN design can be another issue. Usually it can be done through simulation, but the results cannot be simply linked to the real PDN design, one reason is that the simulation time is so long that, as the circuit complexity is increasing, the simulation of multi-layer circuit boards need to consume several days, so it is necessary to find a more concise way to calculate Z_{PDN}; the second reason is that there is still a certain gap between the simulation structure and the real case, and then users are required to spend more time on the real measurements.

Meanwhile, various methods have been developed over the years to perform the calculations, for example, for modeling the power/ground plane, there are the Partial Element Equivalent Circuit (PEEC) method [17]-[19], the Finite-Different Time-Domain (FDTD) method [20]-[21], the Method of Moments (MOM) method [22], the Plane Resonant Cavity Model method [23]-[24], the Transmission-Line Matrix (TLM) method, the Finite Element Method (FEM) [25], the Boundary Element (BEM) method [26] and so on. The system PDN could be divided into three parts, as PCB PDN, package (PKG) PDN

and chip PDN and different part need to use different method to build the circuit model. PCB PDN is the main part of a PDN system, which is used to deliver power from the source through VRM to the ICs. This thesis would focus more on the PCB PDN part and Cavity Model, PEEC/Parallel Plate PEEC (PPP) and BEM are used in the PCB PDN equivalent circuit model extraction based on the different geometry details of different components in PCB PDN.

2.1. PDN IMPEDANCE CURVE WITH EQUIVALENT CIRCUIT MODEL

First, the target impedance (referred as Z_{target}) should be defined carefully based on the IC switching current and the maximum allowable voltage drop to clarify the design requirements. A very straightforward and intuitive definition is given in [11] as:

$$Z_{target} = \frac{Power\ Supply\ Voltage \times Voltage\ allowed\ ripple(\%)}{Current} \tag{1}$$

however, the voltage ripple and switching current would change with time and in this equation, the target impedance is a constant frequency domain concept. Actually, in high frequency range, PDN inductance would increase with the frequency and the constant resistance target impedance in the high frequency range, after about 100 MHz, could result in an over design [11]. Here a simple resolution is that after mid frequency range, such as 100 MHz, the constant resistance could be replaced by an inductance and there would have a 20dB/decade increase in the target impedance curve as shown in Figure 2.1.

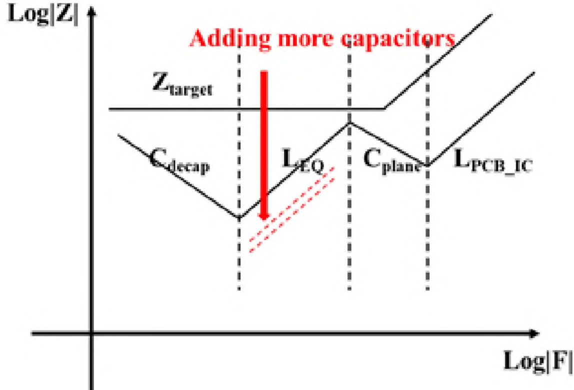


Figure 2.1 The target impedance definition and the impedance curve of a typical PCB PDN.

Based on the previously mentioned constrains about the PCB PDN design, solving PDN impedance equals to ensure the Z_{PDN} is lower that the Z_{target}, in other words, designers are suggested to first have a quick and convenience approach to calculate PDN impedance, then to layout the system which is complied with the industry specifications. And the inductance calculation part is the most essential aspect of PDN analysis. Analytical calculations for specific PCBs require area partitioning. The inductance associated with the current path between the IC to the decaps placed on the PCB is divided into smaller blocks, including L_{PCB_EQ}, L_{PCB_IC}, L_{PCB_Decap}, L_{PCB_Plane} and L_{above}, that can be modeled separately, and the requirement is that there is little or no coupling between different blocks.

Figure 2.2 shows how a PCB can be divided so that the dominant part of the impedance in different frequency ranges can be clearly identified, and the researchers can use this as a basis for improving the inductance of a particular piece. Different methods are used to calculate different components of the PCB PDN. The inductance contribution of current between IC and power layer is defined as L_{PCB_IC} and can be calculated by cavity model, the inductance contribution of current between decaps and power layers is defined

as L_{PCB_Decap} and also calculated by cavity model. Inductance of power plane, L_{PCB_Plane}, could be calculated by PEEC/PPP and the inductance between top or bottom layer and the decaps, which is defined as L_{above} could be obtained by PEEC.

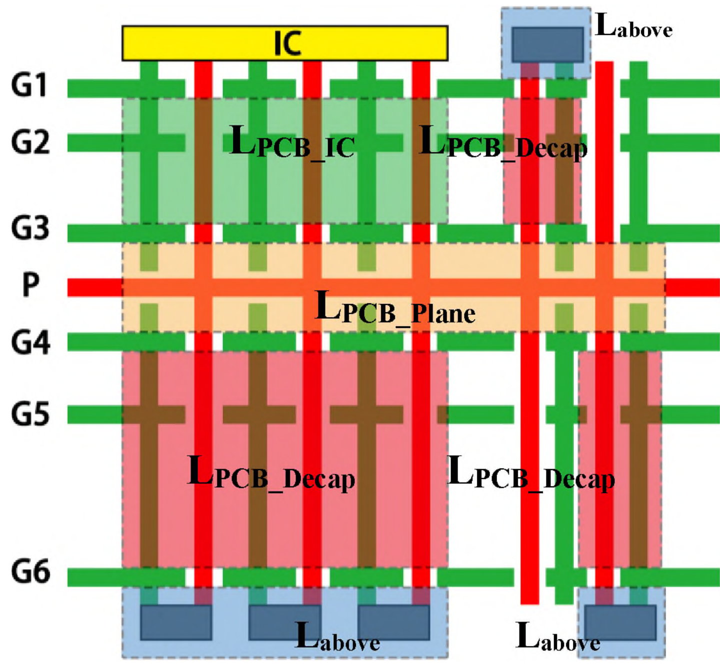


Figure 2.2 The side view of a typical PCB PDN with decaps placed on the surface.

From low frequency range to high frequency range, the PDN impedance has a generic trend between different designs, as shown in Figure 2.1. If the VRM, PKG and Chip model are ignored first, at low frequency, the dominant structure is the decap capacitance and the impedance decreases as the frequency increases. At that stage, the current goes from IC to the decaps through the power area fill in the PDN system, then goes back from the decaps to the power return plane (ground plane). The equivalent inductance (L_{PCB_EQ}) in the mid frequency can be calculated as,

$$L_{PCB_EQ} = L_{PCB_IC} + L_{PCB_Decap} + L_{PCB_Plane} + L_{above} \quad (2)$$

in the mid and high frequency, instead of going to the decaps, the current would directly come back from the power area fill through the capacitance between the power area fill (power plane) and its nearby ground plane, calculated based on the plane area and distance as:

$$C_{plane} = \frac{\varepsilon A}{d} \quad (3)$$

and the impedance would decrease with the frequency again. After that in the high frequency range, the dominate component is the inductance from the current contribution of the IC to the power plane, which is the minimum inductance of a typical PCB PDN. In the even higher frequency range, the cavity resonance leads to the end of the PDN modeling process.

Then the PI problem can be approached by handling each part of the inductance, such as, improving the IC pin map to decrease L_{PCB_IC}, adding more decaps or changing the power layer location in the stackup to have smaller L_{PCB_Decap}, arranging decaps placement around the IC to minimize L_{PCB_Plane}, and utilizing better package and layout for the decap interconnect to achieve a lower L_{above}. In real case, VRM model would have influence on the PCB PDN in low frequency range and Chip and PKG model would have effect on the PCB PDN at mid and high frequency.

2.2. INDUCTANCE EXTRACTION METHOD

According to the different geometries in the system, different methods are used in this thesis to generate inductance matrix from the design. The Cavity Model method is used for the cases with regular and large enough power and ground layers, while BEM is used for the cases with irregular power and ground layers with voids. The tool used for L_{above} calculation is based on PPP and the details are described in [27]-[30].

2.2.1. Cavity Model Method Used for Regular Plane Shape Case. The widely used cavity model method is utilized here to generate the inductance contribution for the current flowing through a parallel plane pair structure [31]-[32]. In most cases, the board vertical size is relatively smaller than its horizontal size so that it could be treated as electrically small and invariant in the analysis. Figure 2.3 shows a typical geometry of a two-layer case with a single via. Assume there is a current flowing throw the power via and there is also a current return via in the cavity. According to the cavity model method, it could be modeled by electromagnetic field theory and with the usage of Maxwell's equations, the Green's function and the boundary condition, the inductance between the two vias can be calculated as [11]:

$$L_{ij}(\omega) = \frac{\mu d}{ab} \sum_{m=0}^{\infty} \sum_{n=0}^{\infty} \frac{(2-\delta_m)(2-\delta_n)}{k_{mn}^2 - k^2} f(x_i, y_i, x_j, y_j) \,|_{(m,n)\neq(0,0)} \quad (4)$$

where:

$$f(x_i, y_i, x_j, y_j) = cos\left(\frac{m\pi x_i}{a}\right) sin\,c\left(\frac{m\pi W_{xi}}{2a}\right) cos\left(\frac{n\pi y_i}{b}\right) sin\,c\left(\frac{n\pi W_{yi}}{2b}\right)$$

$$\cos\left(\frac{m\pi x_j}{a}\right) sin\,c\left(\frac{m\pi W_{xj}}{2a}\right) cos\left(\frac{n\pi y_j}{b}\right) sin\,c\left(\frac{n\pi W_{yj}}{2b}\right),$$

$$k_x = \frac{m\pi}{a},\ k_y = \frac{n\pi}{b},\ k_{mn}^2 = \left(\frac{m\pi}{a}\right)^2 + \left(\frac{n\pi}{b}\right)^2,\ k^2 = \omega^2\mu\varepsilon,$$

$$\delta_m = \begin{cases}1, m = 0\\ 0, m \neq 0\end{cases},\ \delta_n = \begin{cases}1, n = 0\\ 0, n \neq 0\end{cases},$$

and a and b are the dimensions of plane along the x and y directions; (x_i, y_i, x_j, y_j) is the location of ith and j[th] port; W_{xi} and W_{yi} are the dimensions of ith port along x and y directions; m and n are the mode numbers; μ is the permeability of the dielectric layer and ε is the permittivity of the dielectric layer.

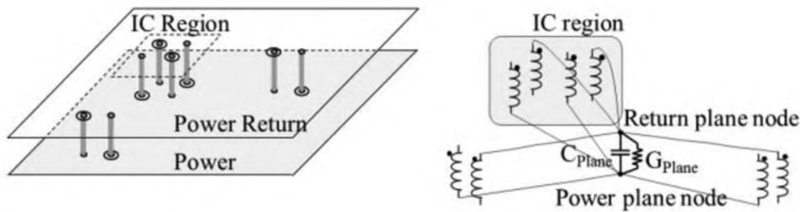


Figure 2.3 A rectangular power cavity with a power plane and return plane, with the lumped circuit model, including the parallel plate capacitance, loss, and inductors [33].

The advantage for Cavity Model is that the self and mutual inductance are already including in the calculation, and it can be easily extended from two planes structure to multiple layers PCB. However, it has the weak point that the Cavity Model method can only be applied when the two planes are large enough compared with the whole structure without voids in the layers.

2.2.2. Boundary Element Method Used for Arbitrary Plane Case. The disadvantage of cavity model is that it cannot handle the case which the plane shape is irregular. And to solve that problem, another method named PEEC is suggested to extract

the inductance value. However, PEEC would cost a lot of time to do the calculation with complex system, and then a method called BEM is implemented to generate inductance value of parallel-plane structures in [34]-[35]. The Boundary Element method is a very effective and time saving approach for calculating the quasi-static port inductance in irregular shaped power/ground plane structure, which is based on the Green's function.

A typical case is designed to compare the different between BEM and Cavity Model method. The stack-up and IC pin map are placed in Figure 2.4 and the inductance performance in the 1GHz, named as L_{PCB_IC} in Section 2.1 is calculated to do the verification. To ensure the case is suitable for the cavity model, all the power layers and power-return layers are set as rectangular, and the sizes are large enough for placing all the vias. The comparison of the Z_{PDN} with 18 low frequency decaps of 470 uF, which are placed at the top layer, is plotted in Figure 2.5.

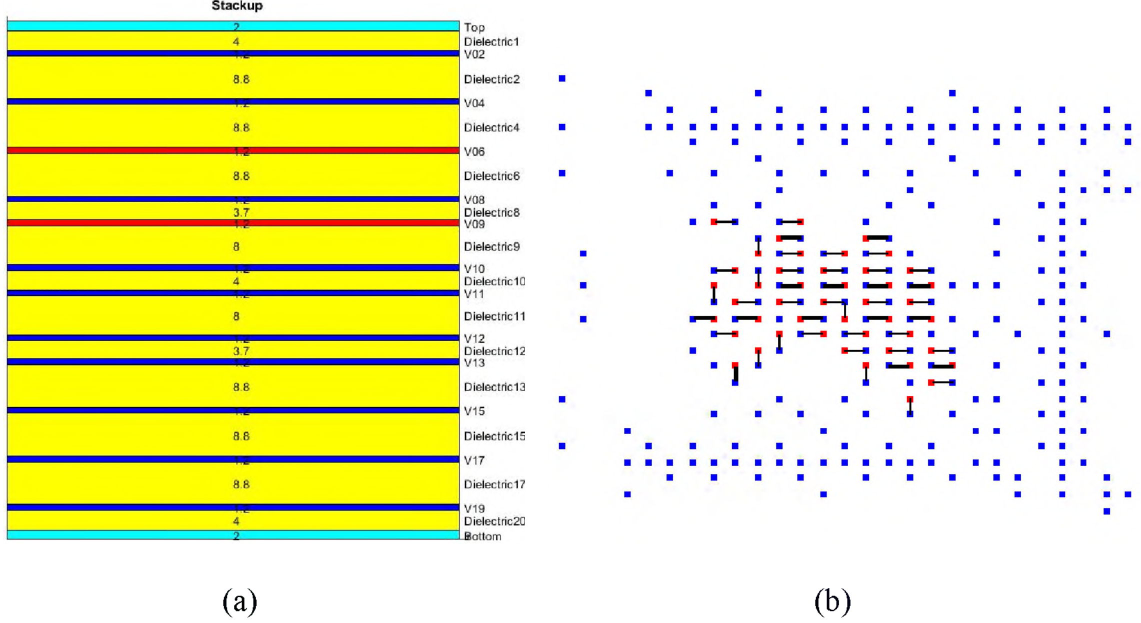


Figure 2.4 Geometry. (a) The stack-up (side view) of the designed case. (b) The IC pin map of the designed case. Blue dots are ground vias and red dots are power vias.

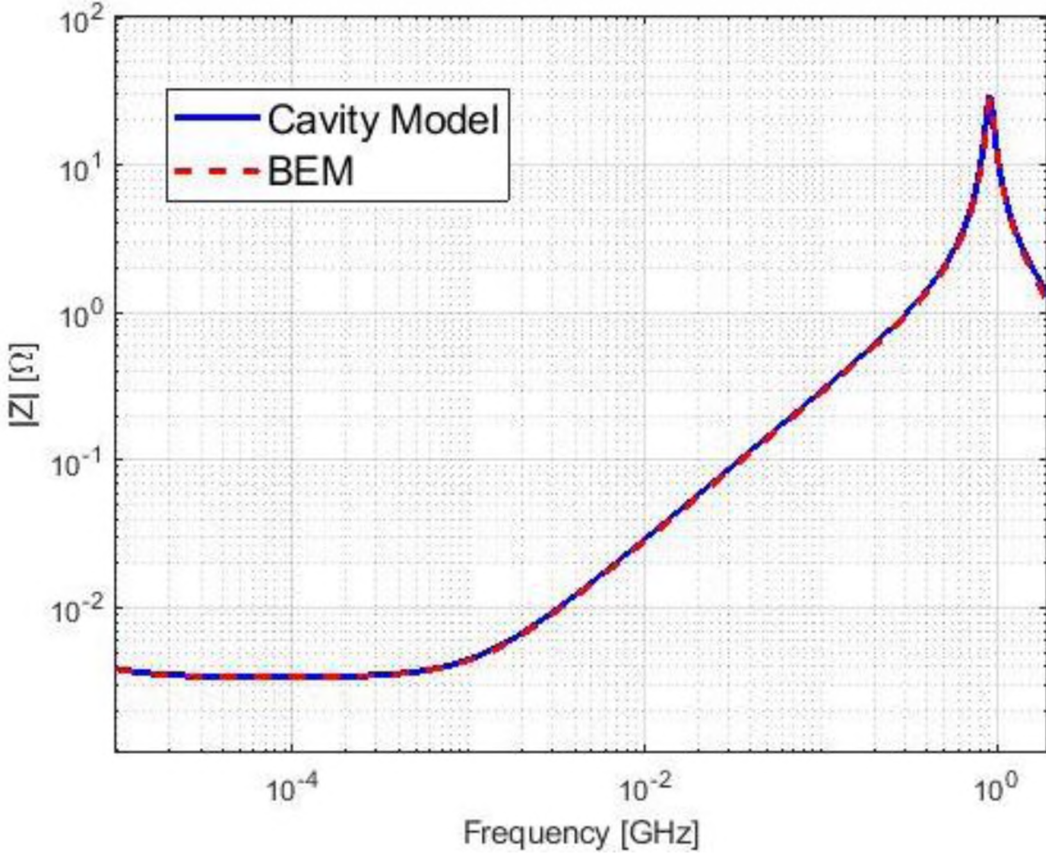


Figure 2.5 Comparison of results from Cavity Model and BEM.

At higher frequency, the L_{PCB_IC} generated from BEM is 7.60 pH and the inductance calculated from Cavity Model is 7.09 pH. The difference is less than 7%, which means that these two methods agree well with each other.

2.2.3. L_{above} Calculation Based on PEEC/PPP. The inductance of a PCB PDN is not only coming from the system itself, but also the decap itself. Capacitor's vendors would provide ESL, ESR and Capacitance value for each decaps, which is usually measured in a certain environment and the ESL value cannot be used directly in PDN analyses since the inductance would be different in different layouts or under different conditions. The L_{above} includes the inductance from the vias, pads and traces in the decap structure when it is

mounted on the PCB surface as Figure 2.6 [29]. It is a decap layout named as 'Doublet' with two decaps and four vias are used to connect these decaps to the surface of PCB. And the inductance could be generated with PEEC.

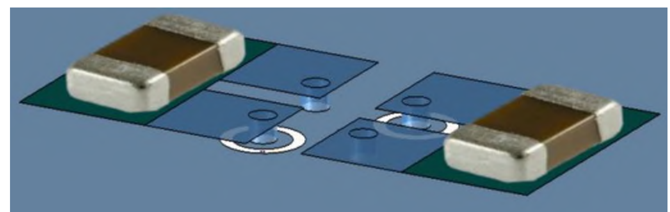


Figure 2.6 A typical decap layout structure.

2.3. EQUIVALENT CIRCUIT WITH A SINGLE POWER LAYER CASE

After obtaining the inductance matrix for every via segment with multiple layers and multiple via connections from the Cavity Model or BEM, a simplified inductance matrix can be generated based on [14]. Also, the inductance matrix could be divided into different segments and then extended to multiple cavities. After simplified, a 4x4 matrix with self and mutual inductance from the current contribution in IC and around IC power and ground vias is constructed as:

$$|L\ big\ matrix| = \begin{vmatrix} L_{IC_Power} & \cdots & & \cdots \\ \cdots & L_{AroundIC_Power} & & \\ & & L_{IC_Ground} & \cdots \\ & \cdots & \cdots & L_{AroundIC_Ground} \end{vmatrix} \quad (5)$$

here L_{IC_Power} and L_{IC_Ground} is the inductance coming from IC power pins and ground vias; $L_{AroundIC_Power}$ and $L_{AroundIC_Ground}$ is the inductance coming from power vias and ground vias

for the decaps placed around IC. As a result, the inductance for each portion in Figure 2.2 can be calculated separately and used in the PDN impedance calculation.

After that, an impedance equivalent circuit model for a multilayer PCB with a single power net area fill can be developed, which is shown in Figure 2.7, based on the individual inductance portions and plane capacitance calculation. Here the decap network includes local decaps and low frequency decaps, which are the large decaps placed relatively far away from IC part to reduce the impedance in low frequency range. Also, there are some bulk decaps placed near the VRM model, even further than the low frequency decaps, which is ignored in this thesis. The plane capacitance is generated from a parallel plane capacitance calculation equation (3) and plane inductance must be simulated with Hspice because of the coupling between power-ground cavities, or a self-written Matlab circuit solver is used in this thesis and the boards with multiple power layers could also be modeled. The values from VRM, PKG and chip model would be provided by designers.

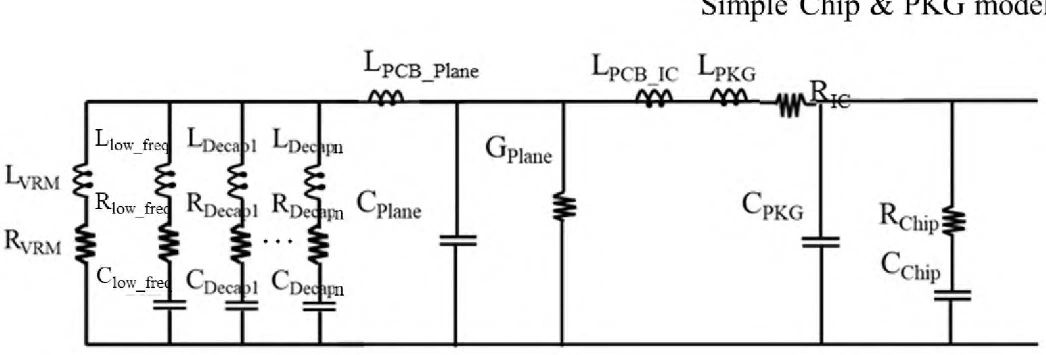


Figure 2.7 Equivalent circuit model.

Finally, the remaining part in the equivalent circuit model is the loss, including R_{IC}, $G_{_Plane}$ and part of $R_{_Decap}$ since except for the decap loss, there would also be ESR value for different decaps. The loss of a PDN could be divided into two parts, as via loss and plane loss. The via loss calculation is simple and straightforward. The current would only flow through the surface of vias when the frequency increases, as shown in Figure 2.8, then the via loss can be generated as:

$$skindepth = \sqrt{\frac{2}{\omega\mu\sigma}}, A = \pi r_{via}^2 - \pi(r_{via} - skindepth)^2 \cong skindepth * 2\pi r_{via} \quad (6)$$

$$Via\ loss = \frac{h}{\sigma A}, \sigma = 5.8 \times 10^7 \quad (7)$$

and based on boundary conditions and cavity model, the input impedance could be generated by Green's function as:

$$Z_{in} = \sum_{m=0}^{\infty} \sum_{n=0}^{\infty} \frac{j\omega\mu d\varepsilon_m^2\varepsilon_n^2}{2ab(k_{xm}^2 + k_{yn}^2 - k^2)} (\cos k_{xm}^2 T)^2 (\frac{\sin k_{xm}^2 W/2}{k_{xm} W/2})^2 \quad (8)$$

if the material is not lossless, which means that $k = k' - jk''$, then the equation can be rewritten as:

$$Z_{in} = \sum_{m=0}^{\infty} \sum_{n=0}^{\infty} \frac{1}{j\omega C_{mn} - j(\frac{1}{\omega L_{mn}}) + G_{mn}} + \frac{1}{j\omega C_{00} + G_{00}} \quad (9)$$

$$G_{00} = C_{00} \times (\tan\delta + skindepth/d) \quad (10)$$

then the first term of (10) is used as plane loss.

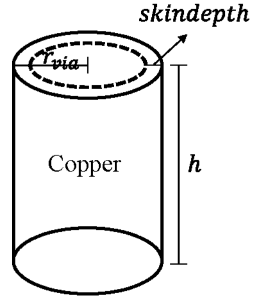


Figure 2.8 Via structure.

Several cases are used to validate this method. Here shows one of the test cases. Figure 2.9 is the stackup and board top view and Figure 2.10 shows the comparison result of Matlab calculation and CST simulation. The inductance difference is less than 5% and the peak of the resonance is greatly reduced when adding loss in the system.

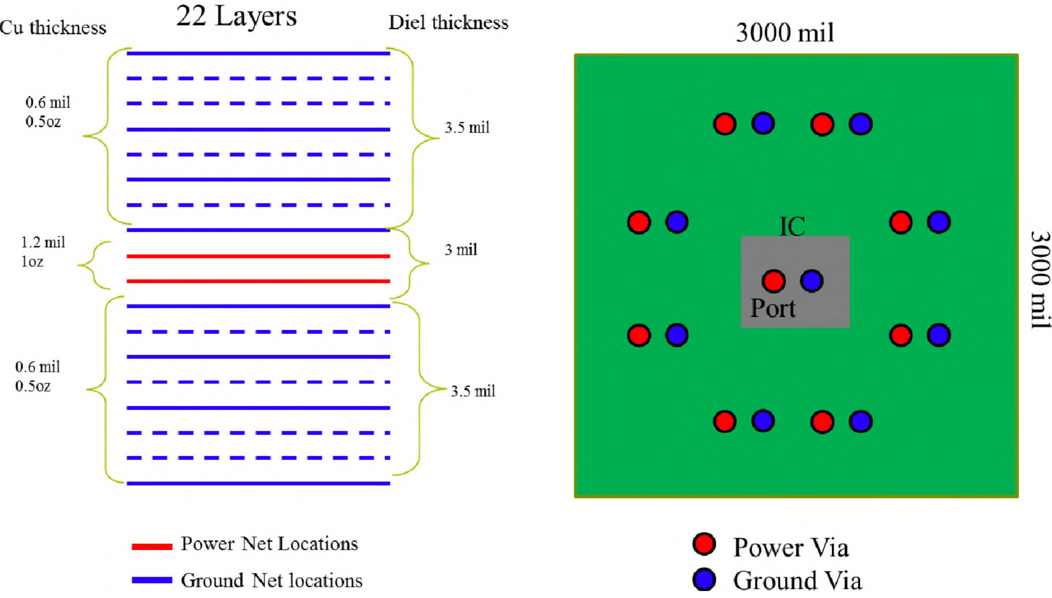


Figure 2.9 The geometry details of the test board.

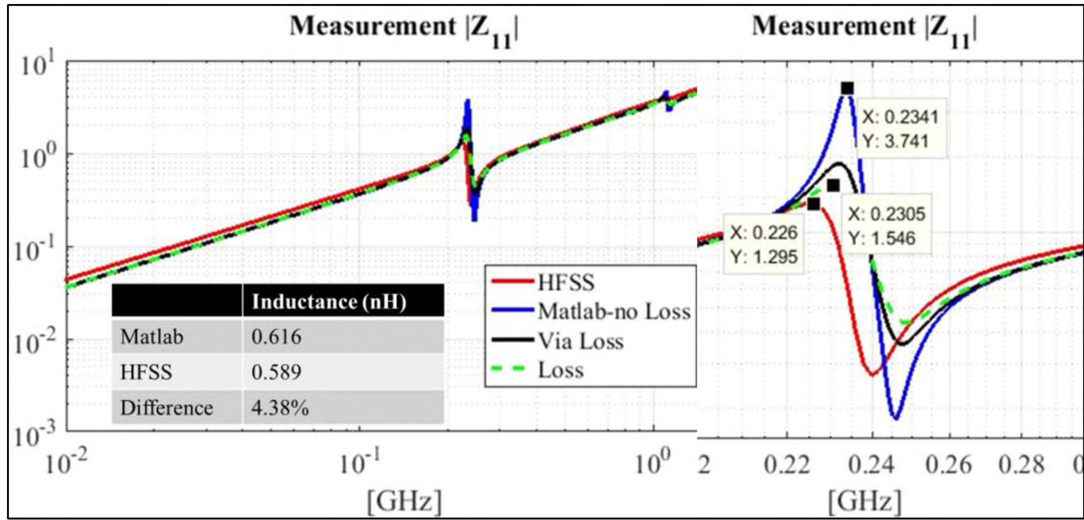


Figure 2.10 Comparison between HFSS simulation and Matlab calculation.

With the circuit model and all existing values from the equation calculation, the PDN impedance can be calculated in different cases.

3. POST-LAYOUT PCB PDN DESIGN

As mentioned before, there are two major challenges faced by the SI and PI designers when developing a PCB PDN, including how to analyze the performance of PCB PDN, which is defined as the post-layout design and how to improve the PDN network, which is defined as the pre-layout design. The physics-based post-layout PCB PDN design is an essential approach to solve the first problem, which would be the prerequisites for handling the second issue with a pre-layout design.

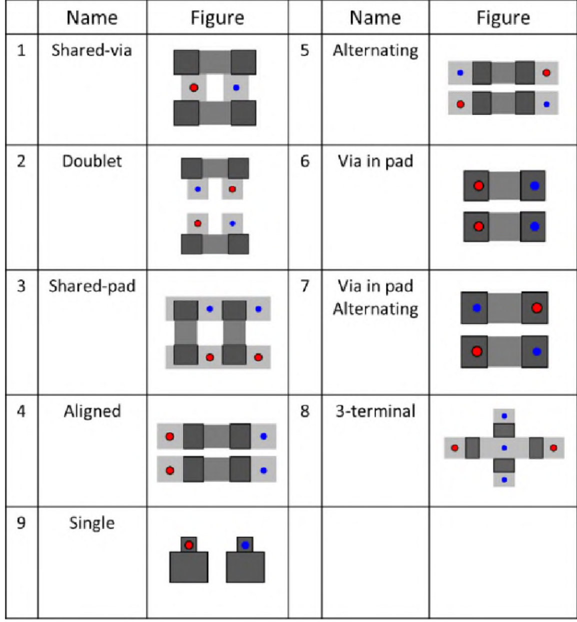
Also, it is necessary to think about what should be added in design considerations. Most important parts here are IC pin map, layout of the board, stack-up and decap network. Usually, the first three items are not decided by PI engineers, so this thesis mostly considers decaps, to be specific, the number, location, size, and layout of decaps and so on. Another pre-work for the pre-layout design in the post-layout part is to explore the influence of decap network to the inductance as L_{above} [12], L_{PCB_Decap} [36] and L_{PCB_Plane} [37]. Based on the equivalent circuit mentioned in Figure 2.6 and the methods mentioned in Section 2.2, the PDN impedance could be calculated and the comparison between the Matlab calculation and CST simulation is proposed in this section.

3.1. EQUIVALENT DECOUPLING CAPACITOR INDUCTANCE LIBRARY

Based on the equivalent circuit model theory, the mid frequency equivalent inductance (L_{PCB_EQ}) is decided by L_{PCB_Decap}, L_{PCB_IC}, L_{PCB_Plane} and L_{above}. The calculation for L_{PCB_Decap} based on Cavity Model method for different decap layouts has been validated with measurement and a library for L_{PCB_Decap} values under different conditions has been

built in this section. The calculation process and the results could be provided as guidelines in the following pre-layout design.

3.1.1. Different Layouts When Calculating L_{PCB_Decap}. Decap inductance is the inductance from the current contribution through the decaps to the power-return plane which is the most nearby from the power plane. There are several factors can put influence on the decap inductance, including different geometries of decap layouts (The layouts are shown in Figure 3.1, and the first four cases are used in this thesis to process the study) and different number of decap pairs (1, 2, 4, 8, 16, 32, the placement of different decap pairs is shown in Figure 3.2). When adding decaps in the design, the simplest idea is that the decap inductance would be divided by the decap number. In fact, there are mutual inductance in between the power and ground vias in one single decap pair model and the inductance would tend to converge after adding lots of decaps.



	Name	Figure		Name	Figure
1	Shared-via		5	Alternating	
2	Doublet		6	Via in pad	
3	Shared-pad		7	Via in pad Alternating	
4	Aligned		8	3-terminal	
9	Single				

Figure 3.1 9 different decap layouts.

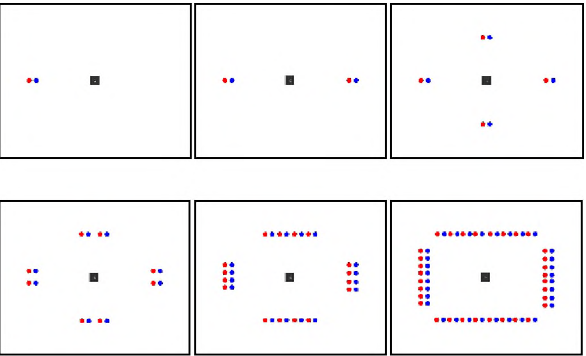


Figure 3.2 The decap placement when adding different number of decap pairs with power vias (red dots) and ground vias (blue dots) locations.

As a mostly commonly used decap placement pattern, the Shared via pattern (Figure 3.3 (a)) consists of two decaps and two vias which are connected by traces. However, according to the methods for L_{PCB_Decap} calculation, the inductance of Shared-via case is much larger than other cases under the same condition, since the equivalent inductance cannot be reduced by mutual inductance.

When designing a PCB PDN, most engineers choose to add more decaps to get a smaller PDN impedance. However, due to the larger coupling inductance between adjacent decaps and vias, the actual impedance will be much larger than the ideal value. Therefore, some scholars have proposed a method of placing vias alternately, such as the structure of Doublet (Figure 3.3 (b)), to reduce the total impedance and also some practical experiments have shown that alternating of power and ground vias do effectively reduce inductance.

Other generally used layouts are Aligned and Alternating. In Aligned case (Figure 3.3 (c)), decaps are placed directly, which will lead to a larger current path, thereby increasing the inductance. To improve this layout, Alternating is shown Figure 3.3 (d). This

case is a modification of the Aligned case. The decap pairs are placed alternatively then the inductance of decaps is greatly reduced from the previous larger value.

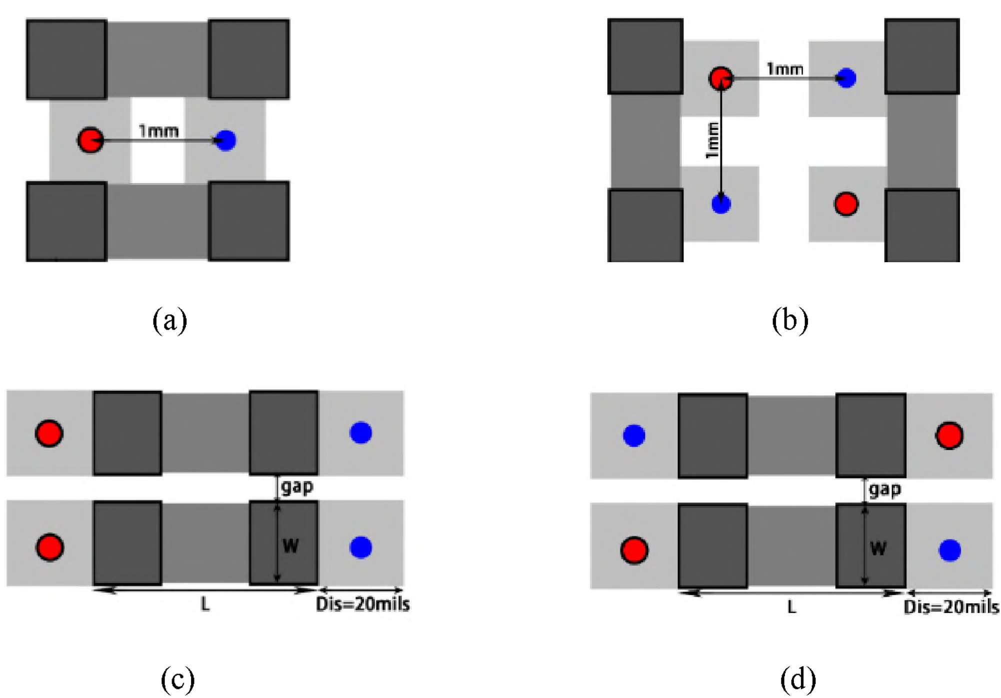


Figure 3.3 Decap geometry. (a) Shared-via layout. (b) Doublet layout. (c) Aligned layout. W=50 mils, L=100 mils. (d) Alternating layout. Gap=11 mils, W=50 mils, L=100 mils.

3.1.2. Measurement and Validation for L_{PCB_Decap} Calculation. Since a certain difference between the ideal simulation environment and the actual situation would always exist, the measurement is required to verify the result of the Matlab calculation. Based on the real inductance value, the inductance is so small that if they are directly measured, the error would be very large. As a result, to make the error as small as possible, when designing the test board, the distance between first layer and second layer is relatively larger (40 mils) than others (8 mils) so that the inductance of decap part will be obvious.

The details of the test cases are shown in Figure 3.4 and a picture of the real PCB is placed in Figure 3.5. The per-unit-length inductance of decap part can be calculated as:

$$L_{PCB_Decap_PUL} = (L_{Fixture\ \#1} - L_{Fixture\ \#2})/D_{TOP_GND} \quad (11)$$

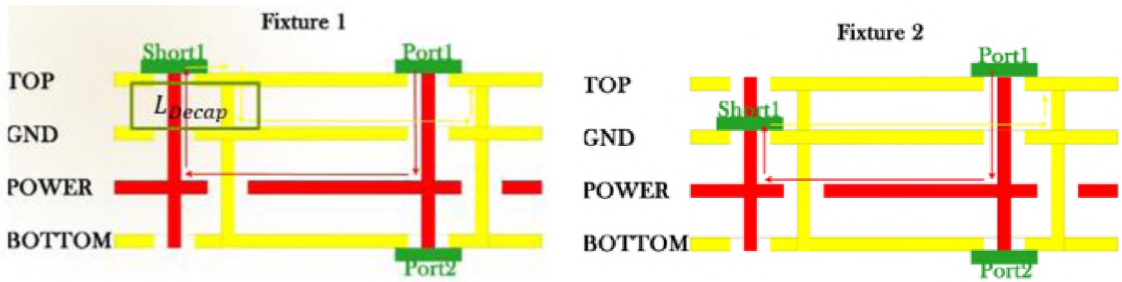


Figure 3.4 The stack-up of the test vehicle cases.

Figure 3.5 Test PCB.

The structures of these two test cases are similar. The first, second, and fourth layers are ground layer, and the third layer is power layer. The inductance of decaps are marked

in Fixture 1. And two-port measurement is used as [38] proposed. In Fixture 1, a short geometry is added between the top layer and the power via, then the current flows from IC port, through the power vias and go into the decap section to the power-return net and finally back to the port; in Fixture 2, the short geometry is placed between the second power-return layer and the power via, so the current will return from the 'GND' layer instead of flowing through the decap at the top layer. Then the two inductances of two cases can be measured and the objective inductance can be obtained by subtracting these two inductances. The inductance results for per unit length of different layouts are listed in Table 3.1. The results of all are similar and the error is small.

Table 3.1 The comparison of the Matlab, CST and measurement [36].

	Number	Matlab (pH)	CST (pH)	Test (pH)
Shared-via	1	17.8	17.6	17.1
	2	8.9	8.6	8.2
Doublet	1	7.2	7.0	7.0
	2	3.6	3.6	3.2
Alinged	1	18.7	18.3	18.4
	2	9.3	8.7	9.2
Alternating	1	10.6	10.8	10.6
	2	5.3	4.9	4.6

The conclusion summarized from the results is that when adding decaps in the design, the Doublet layout can lead to the smallest decap inductance due to the negative mutual inductance caused by the different directions of the current flowing in the power and ground vias when connecting the decaps to the PCB. And other layouts can also be used if the Doublet layout is not available in the design.

3.2. PHYSICS BASED EQUIVALENT CIRCUIT MODEL VALIDATION

To make sure the post-layout calculation process is accurate and correct, a comparison for a typical PCB PDN product is used in this thesis, and the calculation result from the self-written PI tool is compared with commercial tool to validate the PDN impedance generated from the equivalent circuit model and all the values in it. The equivalent circuit model can only handle cases with only one power layer.

3.2.1. The Geometry Details for A Typical Production in PCB PDN Design. The top view of the production with a general PCB PDN geometry is represented in Figure 3.6. It is a high-speed board with 20 layers and Layer 'V11' and Layer 'V12' are designed as power layers. The center of the board is designed as the IC pins and 60 decaps, including 20 decaps of 1uF, 20 decaps of 0.1uF and 20 decaps of 0.01uF, are placed at the bottom layer under the IC part. Approximately 800mils away from the IC part, there are 7 decaps of 0.1uF placed at the top layer. And totally 28 low frequency decaps, with 4 decaps of 470uF and 24 decaps of 100uF, among those 12 decaps are placed at the top layer and 12 decaps are placed at the bottom layer, are used remotely from the center of the board to restrict the impedance in the low frequency range, with values provided in Table 3.2.

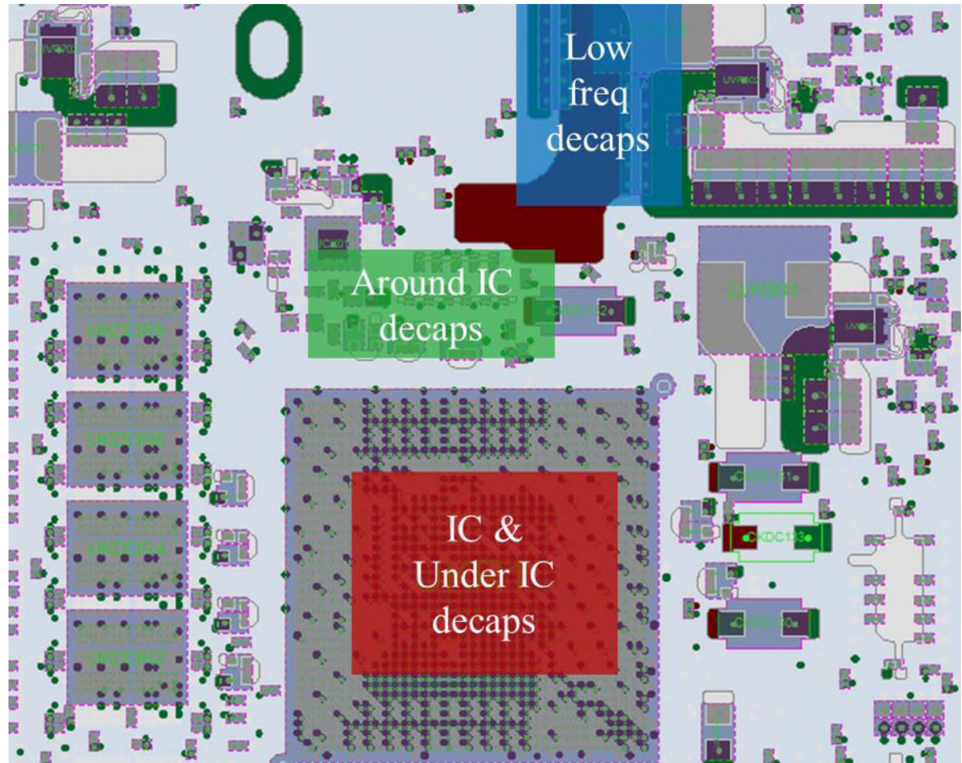


Figure 3.6 The geometry and top view of a 20-layer board showing the IC and decap locations.

Table 3.2 Low frequency decaps used in the design.

Name	ESL (H)	ESR (Ohm)	C (F)	Number	Layer
C1	1e-9	0.03	4.7e-4	4	Top
C2_1	1e-9	0.03	1e-4	12	Top
C2_2	1e-9	0.03	1e-4	12	Bottom

To simplify the calculation process, and also the equivalent circuit model can only handle the simple case with only one power layer, one power layer is deleted, and the power layer location is placed in Layer ‘V11’. Then based on cavity model theory, all the parallel

plane cavities built by two ground layers can be assembled and the inductance is proportional with the combined cavity height. The side view of the example is placed in Figure 3.7 and the height in each cavity is marked in the same figure.

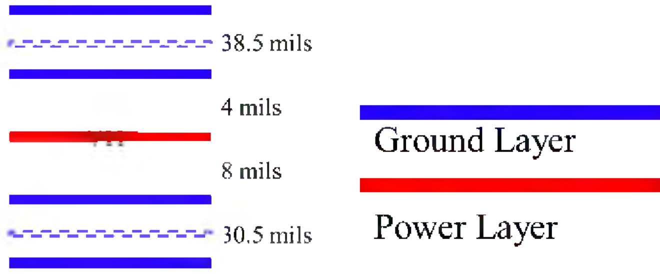


Figure 3.7 The represented side view of the PCB PDN with a simplified conceptual model.

3.2.2. Impedance Equivalent Circuit Model and the Comparison with Commercial Tool. The PI tool places decaps under the IC from the left side to the right side with given IC pin map and would place a ring of four separate decaps around the IC in one step. So here, as shown in Figure 3.8 (a), 8 decaps are placed around the IC to make an approximate for the production case. The equivalent circuit model and part of the circuit RLC values are labeled in Figure 3.8 (b) and Table 3.3. Here L_{PCB_IC} is dominated for the inductance behavior in high frequency range when plane capacitance is represented as short circuit and the current is only flowing from IC power vias to the power plane and then back through IC ground vias. With all the values in the circuit model calculated, the PDN impedance can be generated and compared with the commercial tool simulation result, which is plotted in Figure 3.9.

The discrepancies in the results come from different placement of the decaps in the two cases. It is a post-layout design, however, there are around 123 IC pins in the IC part, and it is a hard work to input the real decap location with the decap values. In these two cases, the decap locations for under the IC decaps and around the IC decaps are not the same. Also, there is one more decap placed around the IC part in the post-layout design due to the defects of the tool so the results in the mid frequency range are not very accuracy.

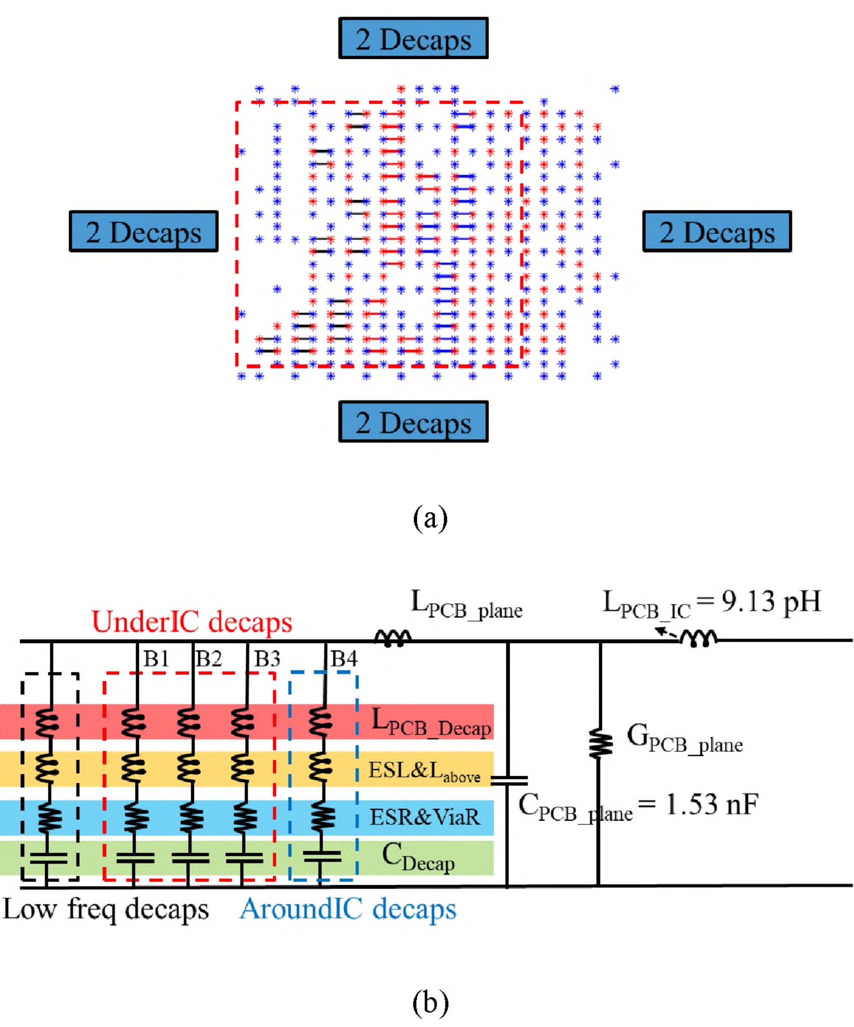


Figure 3.8 Test case. (a) The bottom view with 60 decaps placed under IC and 8 decaps placed around IC. (b) Equivalent circuit model with values for L_{PCB_IC} and C_{PCB_plane}.

Table 3.3 RLC values in the equivalent circuit.

Branch #	1	2	3	4
Decap #	20	20	20	20
Decap location	Under IC	Under IC	Under IC	Around IC
L_{above} (pH)	9.92	9.92	9.92	9.75
L_{PCB_Decap} (pH)	52.3	33.6	31.7	54.98
ESL (pH)	50	50	50	125
ESR (mOhm)	0.5	0.5	0.5	1.25
C (uF)	20	2	0.2	0.8

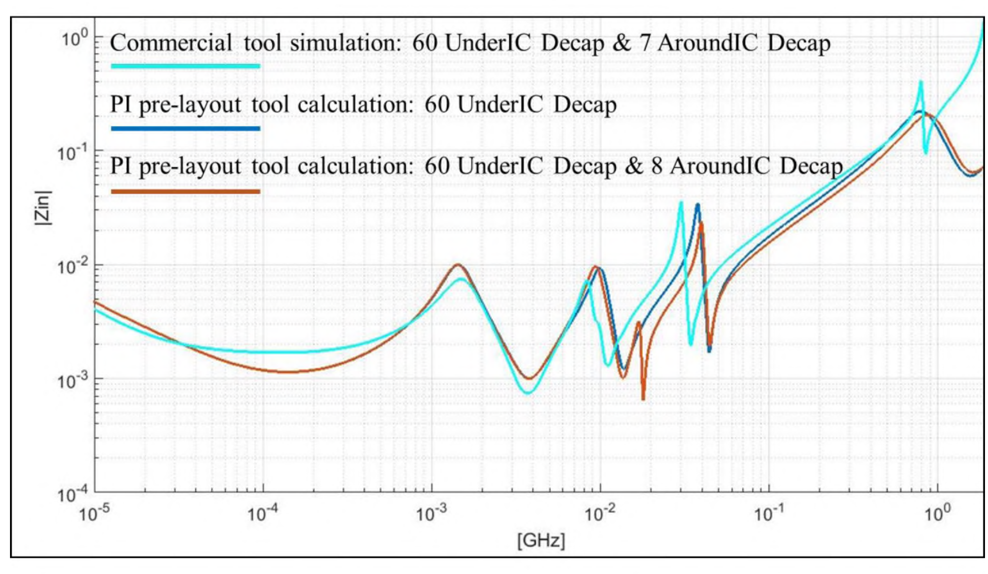


Figure 3.9 Comparison between the simulation and calculation.

Overall, the PDN impedance given from the post-layout calculation matches adequately with the commercial tool simulation result. The capacitance behavior in the low

frequency range and the inductance behavior in the high frequency range are almost the same. The poles and zeros and the peak locations are similar.

Moreover, from Figure 3.9, a brief rule about the decap network effect on the Z_{PDN} could be generated. The impedance in the low frequency range is affected by the inductance and capacitance contribution from low frequency decaps, which would be decided before placing local decaps at the first step by users. The inductance in the high frequency range is L_{PCB_IC}, which would be mostly defined by the IC pin map and the height from the top layer to the power layer. The impedance in the mid frequency range, is mostly determined by the placement and values of decaps under and around the IC and the stack-up. Besides, the three poles and zeros are coming from the three different decaps of 1uF, 0.1uF and 0.01uF, which leads to an estimation that a well-arranged series of decaps can contribute to reduce the PDN impedance with minimum number of decaps.

3.3. MATLAB BASED SELF-WRITTEN CIRCUIT SOLVER

When generating L_{PCB_EQ}, the inductance related to the current flowing through the power layer and nearby ground layers, referred as plane inductance (L_{PCB_Plane}), plays an essential and irreplaceable role in the total inductance. Because of the coupling of different cavities near the power layer, the plane inductance would be more difficult to calculated and estimated as other Ground-Ground cavities which do not include power layers. In Section 3.2, a physics based equivalent circuit model is implemented to handle the cases with only one power layer. The reason is that the circuit is only designed for the simple situation with a single power layer. Another disadvantage comes from the time of calculating plane inductance. The plane inductance is not proportional with the cavity

height so that the value needs to be simulated by Hspice or other methods as PEEC or PPP, which are time-consuming.

The node voltage method is utilized in this post-layout design to generate Z parameters with the inductance big matrix built from Section 2.2 and the plane capacitance calculated from (3) using matrix formulations [39] so that it can handle cases with more than one power layer. The main idea is from the relationship of voltage and current as:

$$(\mathrm{A} \times Y_b \times A^T) \times Y_n = I_n \quad (12)$$

here the A matrix is the relationship of all the current directions and nodes in the system; V_n is the node voltage, and I_n is the node current (the direction is the current entering the node); Y_b is the inverse of the Z matrix building with as:

$$[V_b] = [Z_b][I_b] = \begin{bmatrix} Z_{Cavity\#1} & 0 & 0 \\ 0 & \dots & 0 \\ 0 & 0 & Z_{Cavity\#n} \end{bmatrix}, [Y_b] = \begin{bmatrix} Z_{Cavity\#1}^{-1} & 0 & 0 \\ 0 & \dots & 0 \\ 0 & 0 & Z_{Cavity\#n}^{-1} \end{bmatrix} \quad (13)$$

after generating the Z parameter from (12), the Z matrix after placing a single decap at port ‘p’ can be calculated based on [40] as:

$$Z'_{aa} = Z_{aa} - Z_{ap}(Z_{pp} + Z_{dd})^{-1} Z_{pa} \quad (14)$$

here the Z matrix before placing the decap has a+1 ports and the decap is placed at port ‘p’ and Z_{dd} is the Z parameter for the decap. Z_{dd} equals to:

$$Z_{dd} = j\omega(ESL + L_{above}) + \frac{1}{j\omega C} + (ESR + R_via) \quad (15)$$

here ESL and ESR are the input value for each kind of decaps in the library provided by the vendors; The added loss (R_Via) caused by placing one via is calculated by (7) and since it is a frequency dependent item, the used frequency in the circuit model is 10 MHz to estimate the loss at a certain situation since the Z_{PDN} in the mid frequency range is the major consideration. Then all the decaps could be placed one by one at different nodes in the system.

Hspice can also be used to get the Z parameter of a typical PCB PDN, it is a time-consuming process so that it is not a best approach to handle circuit, however, it can be utilized to do the verification with the node voltage method. A comparison between the Hspice simulation and Matlab circuit solver is made. The stack-up and top view about the IC and around IC decap vias placement are shown in Figure 3.10, and the results calculated from Hspice and Matlab are plotted in Figure 3.11. To be specific, there are 50 IC pins and 8 around IC pins and in this case, 25 decaps of 0.01 uF and 25 decaps of 0.1 uF are placed under IC, 8 decaps of 0.1 uF are placed at the top layer and 8 decaps of 1 uF are placed at the bottom layer around IC

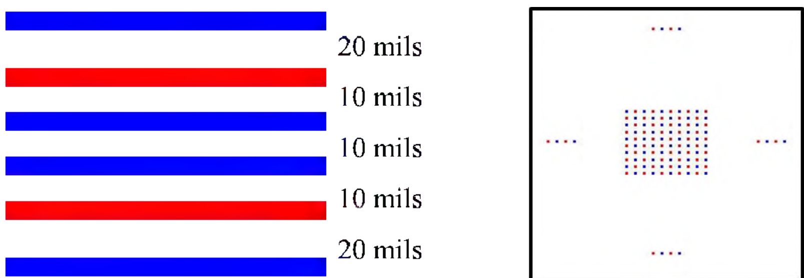


Figure 3.10 Stack-up and top view of the test vehicle.

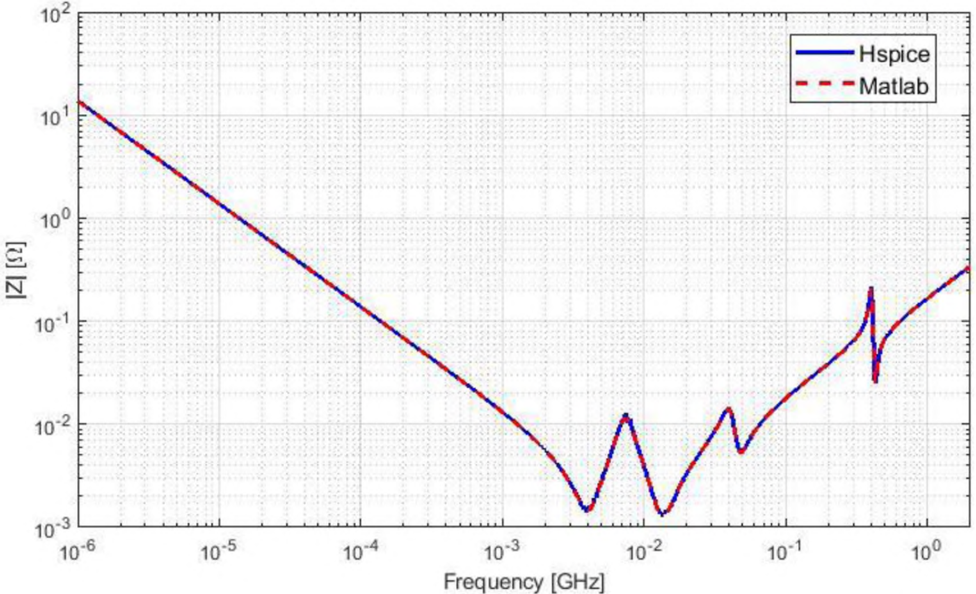


Figure 3.11 Results comparison.

The Matlab calculation result and Hspice simulation result are nearly the same. And the same case in Section 3.2 is used here for the result verification, which is shown in Figure 3.12 (a). In the comparison, the only difference is the loss estimation in the low frequency range and high frequency range. The difference comes from two parts. The first is the inaccurate low-freq decap locations, which is plotted in Figure 3.12 (b) and can lead to the inaccuracy of inductance and loss calculation. The second reason is from frequency dependent loss calculation. The loss is calculated at 10 MHz so that in low frequency range, the calculated loss would be larger than the real loss, which leads to a larger zero than the simulation result. The resonance frequency for each poles and zeros are nearly the same and the inductance are similar for Matlab calculation and PowerSI simulation.

To reach the objective of handling the cases with two power layers, Layer 'V11' and 'V12' is used as power layers for the testing. The geometry is the same with the PCB

PDN in Section 3.2 and the only change is the number of power layers. The results comparison is shown in Figure 3.12 (c) and the stackup detail is shown in Figure 3.12 (d).

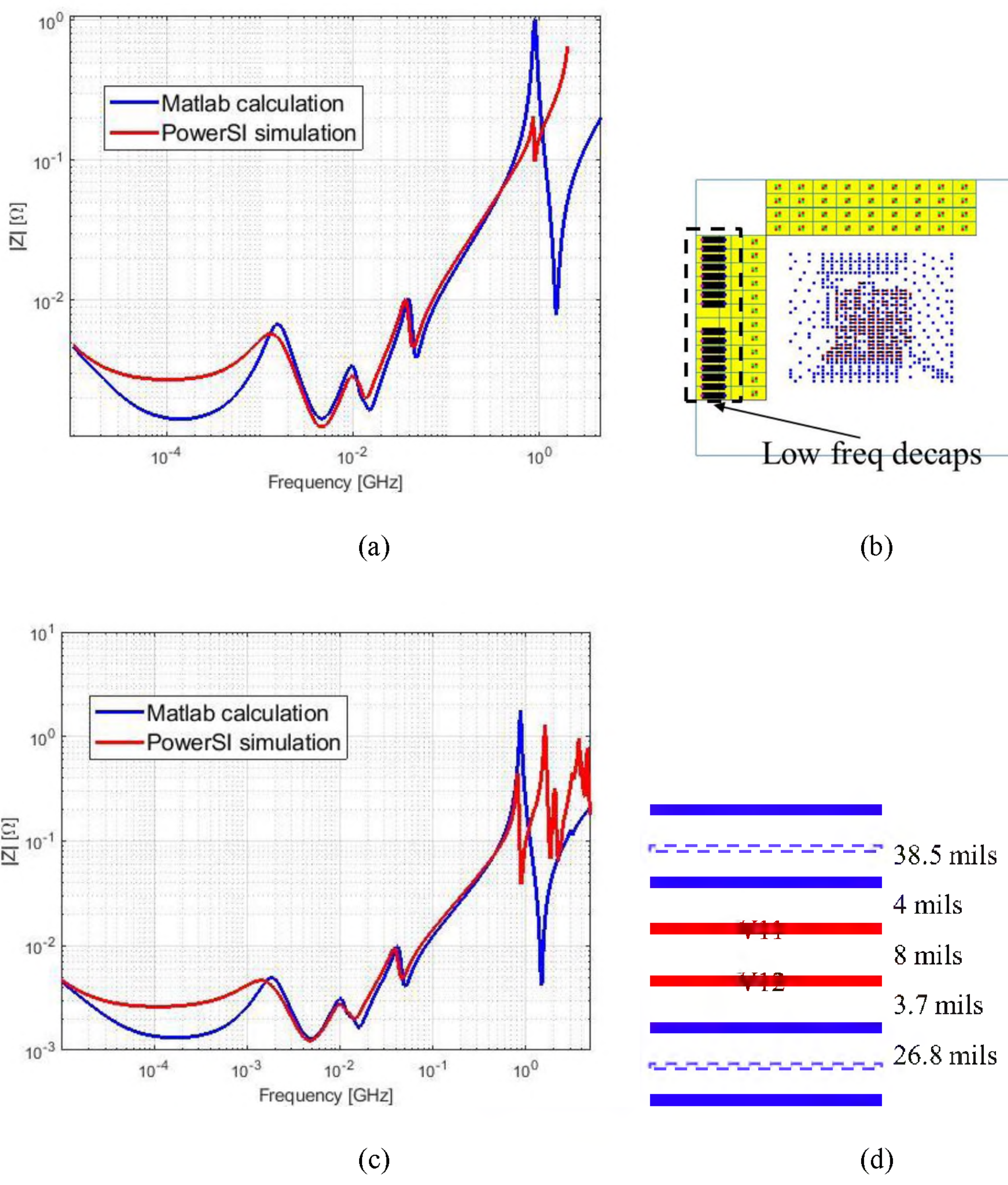


Figure 3.12 Solutions. (a) Comparison between PowerSI and Matlab calculation for one power layer case. (b) Designed decap locations. (c) Stackup with two power layers. (d) Comparison between PowerSI simulation and Matlab calculation for two-power case.

According to Figure 3.12 (c), in the low frequency, the capacitance and inductance behavior show similar trend except for the deep in the first zeros, which is not very important since the peaks in the estimation are more essential than the deeps. And the reason is the same with the calculation result from one-power layer case. As the frequency enters the mid frequency range, the poles and zeros caused by the three different decaps are similar between the two approaches. Then in the high frequency, the peak for the plane capacitance in the Matlab calculation is the same with the first peak of the simulation result. Since the power area fills in the two power layers are different in the real case, and there are also irregular ground layer shapes in the same layer with the power layer shape, there are multiple resonances in the simulation results, which may be caused by other power-ground cavities, which are not included in the calculation process.

In this section, the PDN impedance of a typical production PCB design is calculated with based on cavity model, BEM, equivalent circuit model method and node voltage method. A simulation result from a commercial tool, PowerSI, is provided to validate the accuracy of the impedance equivalent circuit model achieved by node voltage method and network reduction of the physics-based model obtained from a first principles formulation. The results agree with each other before high frequency as 1 GHz.

4. A PI PRE-LAYOUT PCB PDN TOOL

A pre-layout tool based on the cavity model and parallel plate PEEC is built to automatically achieve a specified target impedance for a multi-layered PCB PDN design with a minimal number of decoupling capacitors. Only limited input geometry details are required for the tool. Physical limitations for the minimal target impedance that can be achieved are calculated first to determine if a design is physically realizable and provides feedback to the user. Most importantly, since choosing decoupling capacitors is a primary issue in PDN design, a special selection algorithm based on zeros and poles is utilized to determine which decoupling capacitors from a library should be added. The decoupling capacitor location will be determined by physics. Finally, the target impedance could be achieved using the minimum number of decoupling capacitors. The calculations are accurate and fast. Several industry design cases are used to verify the calculation result. The process is quite time-saving and convenient, and allows the user to do design discovery quickly, and determine the limiting factors under different conditions.

4.1. DESIGN CONSIDERATIONS

Because of the increasingly requirement for the lower voltage supply and higher density in PCB PDN design, how to solve power integrity issue plays a more important role among industry teams. The performance of the board must be able to pass the checking procedure after completing the PCB, or designers are required to modify the design again and again to make sure the target is satisfied. Many general principles and commercial tools are utilized to help PCB PDN designers saving time in the repetitive work, for

instance, how to generate a better stack-up, how to save cost while placing enough decoupling capacitors, how to make a best placement of IC pins and so on. The most essential part in the PCB PDN design is the approach of placing as less as possible decoupling capacitors to achieve industry requirement. In this pre-layout tool, the influence from the decoupling capacitors types and stack-up is mostly considered. The variety of decoupling capacitors contribute to the objective of reaching the target with minimum number of decoupling capacitors.

The design considerations in the PCB PDN area are including multiply cases, such as IC pin map, stack-up, and decap network and even the padstack. All in all, the most important part is the decap type and placement, and here this thesis only talks about local decaps except for low frequency decaps and how the PDN impedance would be influenced by the decap network is discussed in this section. The geometry, the stack-up, IC pin map, decap library and so on are the same from the production in Section 3, which is used in this part to continue the design analysis.

4.1.1. Stackup. Based on the physics, L_{PCB_Decap} is promotional to the distance between decaps to the power layer or $L_{PCB_Decap_PUL}$, which would be a great and major part in L_{PCB_EQ} because of the thinner PWR-GND cavity with smaller L_{PCB_Plane} in general multiple-layered PCB PDN design. If the power layer is placed closer to the decap location, the needed decap number to achieve target impedance would be reduced.

Assume Layer 'V06', which is closer to the decaps placed on the top layer is used as power layer and assume another power layer is Layer 'V09', then the comparison results for only under IC decaps and both under and around IC decaps are plotted in Figure 4.1 (a) & (c) and the stackup details are plotted in Figure 4.1 (b) & (d). The frequency range of

interested is from 100 kHz to 200 MHz and the resistance in the initial point of the defined target impedance is 32 mOhm.

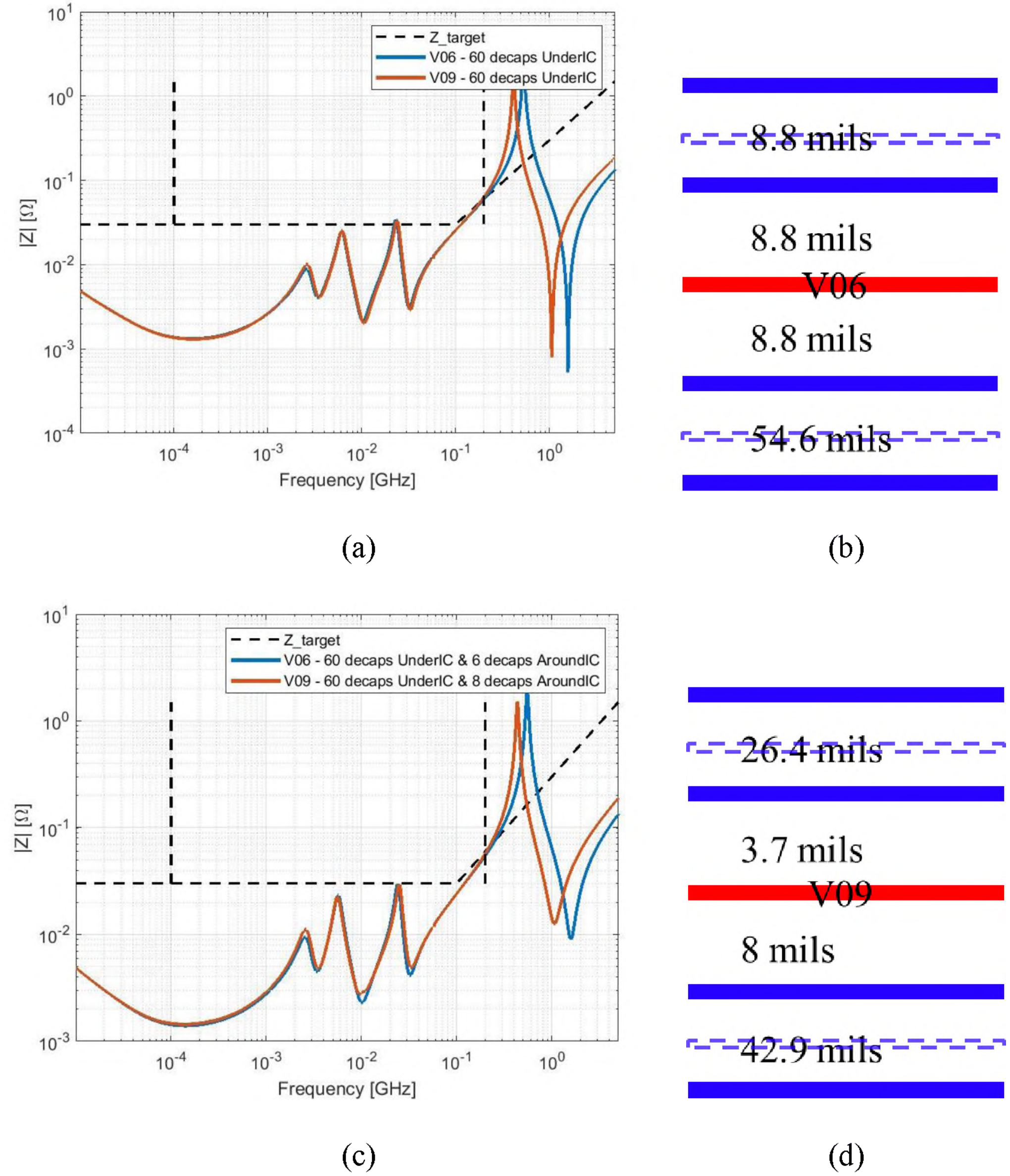


Figure 4.1 Results. (a) Comparison result with 60 decaps placed under IC. (b) The represented side view by a simplified conceptual model when power layer is 'V06'. (c) Comparison results with 60 decaps placed under IC and 8 or 6 decaps placed around IC when Layer 'V06' or Layer 'V09' is designed as the only power layer. (d) The represented side view by a simplified conceptual model when power layer is 'V09'.

First decaps are typically placed under the IC because no additional vias are required, and hence, the routing of signals is not restricted with this choice. In this case, with 60 decaps a maximum under the IC, the target impedance cannot quite be reached. Then more decaps are placed around the IC on the top layer. The conclusion is that if power layer location is changed as close to the decap network as possible, the inductance would be nearly similar if only a maximum number of decaps is decided and it cannot reach the target impedance. Meanwhile, if more decaps are allowed in the design, the inductance would be reduced and the amount for placed decaps could be smaller to save cost in the same design.

4.1.2. Decap type. One strategy for choosing decap values proposes using the largest decap value in a given package size. Another strategy is to use a series of values, e.g., three or four decaps per decade of frequency. Using a poles and zeros algorithm allows the target impedance to be met with a well-designed series of different decaps. The available decap ESL, ESR and C values in the library of the design are listed in Table 4.1. The maximum number of both under and around IC decaps are set as 60, which means that it would be marked as failed in the design process if the target impedance cannot be achieved with 60 decaps placed under the IC plus 60 decaps placed around IC. And the tool would only place decaps around IC after completing the placement of 60 decaps under IC however without reaching the target impedance. A complex RL-RL target impedance with a resistance of 3.5 mOhm at 1 MHz and a resistance of 35 mOhm at 100 MHz is used; and the frequency of interest is from 100 kHz to 300MHz. 'V11' is used here as power layer.

Table 4.1 Decap library.

Under IC Decaps				
Name	ESL (pH)	ESR (Ohm)	C (F)	Size
DecapU1	0.4	3.0e-01	1.0e-09	0402
DecapU2		2.5e-01	2.2e-09	
DecapU3		9.0e-02	4.7e-09	
DecapU4		6.0e-02	1.0e-08	
DecapU5		4.3e-02	2.2e-08	
DecapU6		3.8e-02	4.7e-08	
DecapU7		2.8e-02	1.0e-07	
DecapU8		2.0e-02	2.2e-07	
DecapU9		1.6e-02	4.7e-07	
DecapU10		1.2e-02	1.0e-06	
Around IC decaps				
DecapA1	0.4	1.6e-02	4.7e-07	0402
DecapA2		1.2e-02	1.0e-06	
DecapA3		9.0e-03	2.2e-06	
DecapA4		7.0e-03	4.7e-06	
DecapA5		5.0e-03	1.0e-05	

The impedance curve under a different condition is shown in Figure 4.2, and the summary of decap type and number are listed in Table 4.2. Among all four cases, the target impedance is achieved, and the objective cannot be reached only by under IC decaps. As a result, except for the 60 decaps placed under IC, several around decaps are mounted to meet the target in the mid frequency range. In Figure 4.2, U8 and A5 are used in (a); U1, U4, U8 and A5 are used in (b); U1~U8 and A5 are used in (c); U1~U8 and A1~A5 are used in (d).

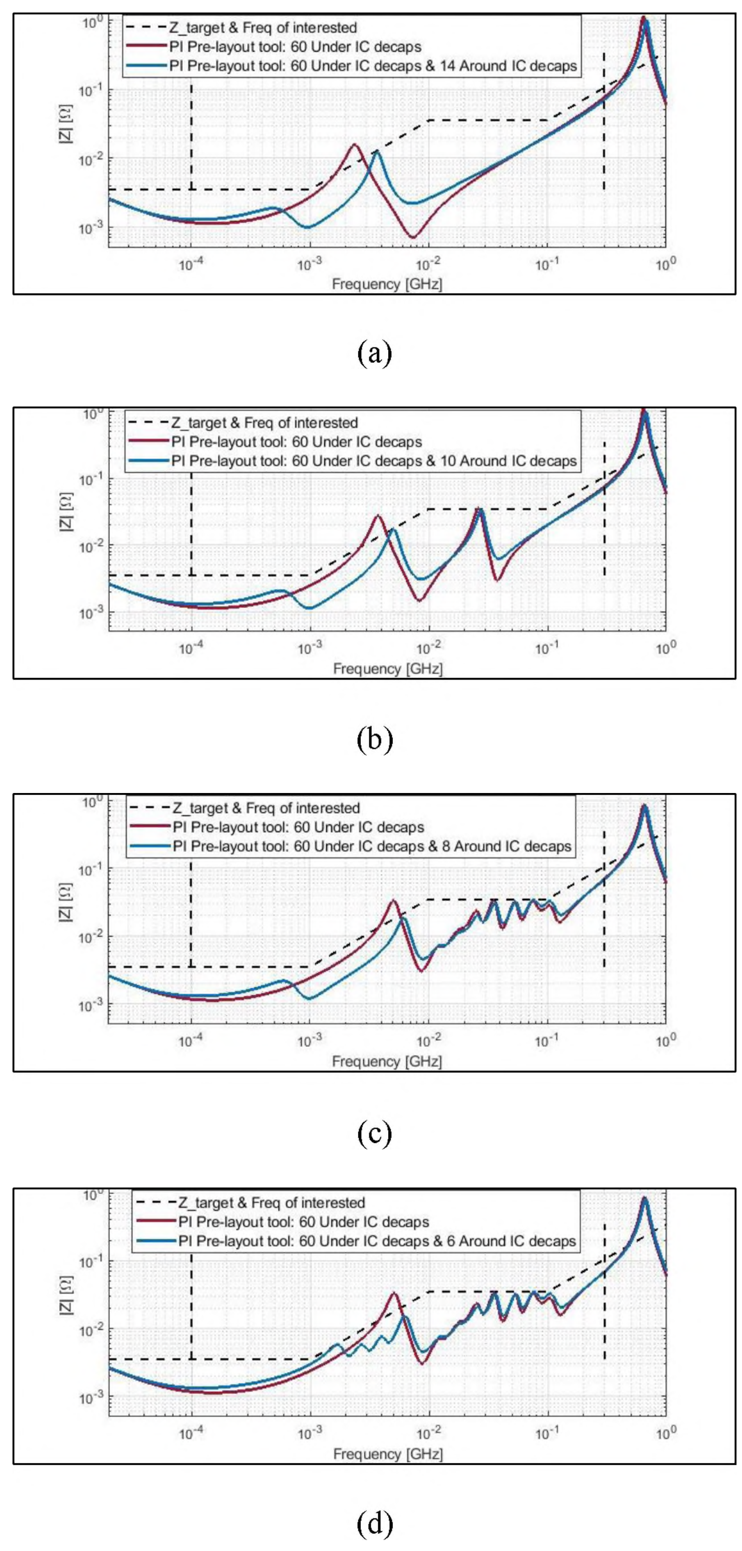


Figure 4.2 Target impedance and PDN impedance result with different designed decap networks.

Table 4.2 Used decap type number and used decap number in the design.

Number of different decap values from the library used				
	Type Number			
Under IC	1	3	8	8
Around IC	1	1	1	5
Used decap number in the design				
Under IC	60	60	60	60
Around IC	14	10	8	6
Achieve target or not?	Yes	Yes	Yes	Yes

Figure 4.2 (a) shows the result with a single decap value from under the IC decap library and a single decap value from around IC decap library. In the picture, there is only one pole in the under IC result and one pole in the around IC result, which is typical for the two different decap types. And in this case, except for 60 under IC decaps, 14 around IC decaps are used to achieve target impedance. Figure 4.2 (b) shows the result with 3 decap values from under IC decap library and a single decap value from around IC decap library. Also, in the result, there are multiple poles and zeros, which is consistent with multiple decap types. Figure 4.2 (c) shows the result with 8 decap values from under IC decap library, and a single decap value from around IC decap library. There are also multiple poles and zeros around 50MHz, corresponding to the multiple capacitor values. Figure 4.2 (d) shows the result with 8 decap values from under the IC decap library and 5 decap values from around the IC decap library. There are more poles and zeros around both 3 MHz and

50 MHz, corresponding to the increase in the number of different decap values. As seen in the progress in Figure 4.2, suitably expanding the number of decap values available for use, and properly calculating the placement of zeros, can lead to a smaller number of overall decaps used.

The conclusion generated from Section 4.1 is that placing the power layer near decaps reduces the decap inductance and number of decaps necessary. Meanwhile, using a series of decaps of different values and an appropriate zero placing algorithm, instead of a single decap value can reduce the number of decaps needed in the design.

4.2. DECOUPLING CAPACITOR OPTIMIZATION ALGORITHM

The main idea to achieve target impedance with minimum amount of decaps is to use a series of decaps which are useful to lower the PDN impedance. For the decaps network, the location, layout, and type are considered separately to simplify the problem. Firstly, an optimization for the decap location placement for under IC and Around IC is established, including how to mount decaps on the existing IC vias, how to choose layers on the PCB to place decaps and how to place decaps around IC to achieve smaller L_{PCB_Plane}. Secondly, there are different decap layouts with four of them are analyzed in Section 3.1. The layout should be carefully decided to obtain lower L_{PCB_Decap} and L_{above} [41]-[42]. Finally, the decap types are essential to the inductance at mid frequency and a poles and zeros algorithm is proposed to use in the design and compared with the genetic algorithm.

4.2.1. Decap Location and Layout Optimization. On the one hand, the first step for decap network design is placing decaps under the IC since there are designed IC vias to connect decaps to the PCB and large space under IC region in most cases. The main

approach in this part is to choose decaps as ‘Doublet’ part based on the conclusion in Section 3.1 and [36]. Then based on the various input and options in the design, the workflow for using under IC vias to place decaps is plotted in Figure 4.3. After using all the possible ‘Doublet’ pattern, the tool would choose the power vias with most ground vias nearby to achieve the lower inductance.

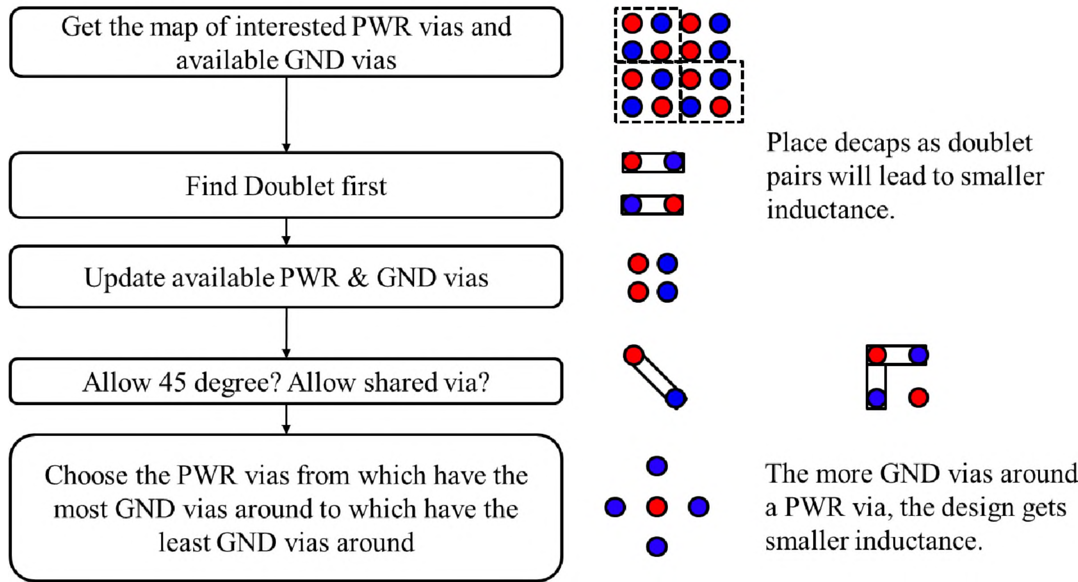


Figure 4.3 Under IC decap placement with IC power and ground vias.

On the other hand, for around IC decaps, it is suggested to place decaps as a ring around the IC region as Figure 4.4 (a). Another aspect for around IC decaps is the layer which should be used to mount decaps. There are two possible locations to place decaps, as top layer and bottom layer. A simple way to decide which one is better to use is to compare the distance between the top layer and closest ground layer and the bottom layer with the closest ground layer. Based on the conclusion made from Section 3.1, the smaller distance leads to the lower inductance of L_{PCB_Decap}.

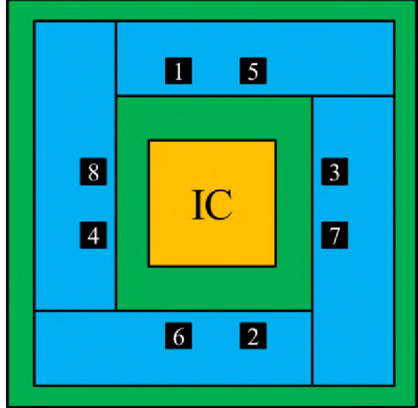


Figure 4.4 Top view about the suggested around IC decap placement and the order.

To optimize L_{PCB_Decap} and L_{above}, the inductance from the decap to the most nearby power layer could be generated by Cavity Model method and the inductance from the decap to the top or bottom layer should be calculated based on PEEC. There are 9 different decap layouts in the most designs as described in Figure 3.1. The estimate equivalent inductance for a single decap pair can be generated, and a layout could be easily decided by the inductance value.

4.2.2. Decap Type Optimization. Several algorithms are used based on different methods to choose decap types from a library, such as, physic understand is applied to decap network design in [43]-[45] to save time while improve the performance, while genetic algorithm is utilized in [46]-[47] to achieve the target, and there are also some other methods which are demonstrated in [48]-[50] to handle this issue.

A decoupling capacitor optimization algorithm based on poles and zeros is applied in this PI pre-layout tool in PCB PDN design. There are given possible decoupling capacitor locations including the X and Y dimensions for power and ground vias in the tool. A library with series of decoupling capacitors is provided and the ESL, ESR and C

values are listed in the input spreadsheet. Then in the algorithm, the frequency intersection of target impedance, plotted as f1, and PDN impedance, plotted as f2, are marked, and shown in Figure 4.5, and the needed decoupling capacitor type is calculated with RLC frequency equation from the library.

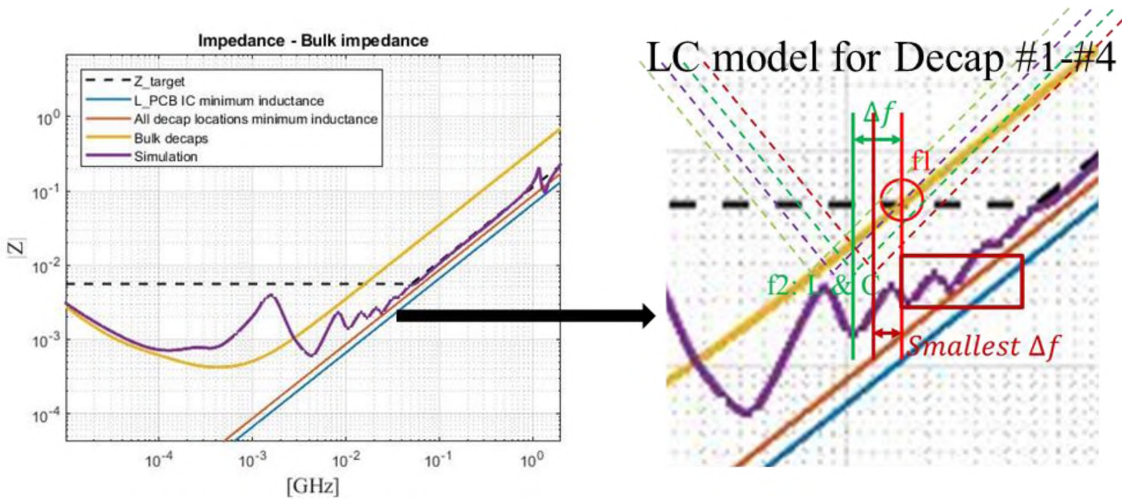


Figure 4.5 One example for the poles and zeros algorithm.

Another approach in the poles and zeros algorithm is that after adding decaps, the updated f1 would be compared with the original f1. If the intersection frequency point is turned left by adding one decap, the tool would use a larger value decap instead of the calculated one to ensure the peak would not be too high to touch the target impedance curve. And for the time-saving requirement, this judgement would only be made for one loop.

The whole process is quite time-saving and convenient, and it helps the pre-layout tool with a better performance. A comparison for both time and performance for the

designed decap network between the poles and zeros algorithm and GA are made in the later section with real productions.

4.3. DESIGN WORKFLOW FOR THE PRE-LAYOUT TOOL

The algorithm is based on local optimization to minimize L_{PCB_EQ} by minimizing inductance contribution from each part, as L_{PCB_IC}, L_{PCB_Decap}, L_{PCB_Plane} and L_{above}. For each component, L_{PCB_IC} is decided by the IC pin map design and broad stack-up., while L_{PCB_Decap} and L_{above} are determined by decap network design, such as decap location, type layout and so on. The last one as L_{PCB_Plane} is influenced by the power-ground cavities and the decap network. As a result, an effect way to minimize L_{PCB_EQ} is to design a suitable decap network, which is considered in the pre-layout tool.

The design workflow is demonstrated in Figure 4.6. A special designed input spreadsheet is used for the basic geometry details such as the stack-up, IC pin map and decap library. Then the fundamental inductance limits are calculated to determine if user design can meet the target impedance in the limitation check step. After that, the decap network is designed to decrease the PDN impedance. Usually, designers would prefer to place the decaps under IC since there are existing IC vias to connect decaps to the PCB and the space for around IC decaps is limited. So, the tool would first plane to place under IC decaps if it is allowed by the users. Then if around IC decaps are allowed and needed, the decaps would continue to place these decaps around IC region to reach the target impedance. After placing every single decap pair, the PDN impedance would be calculated by the circuit solver and compared with the target impedance to make sure the minimum decap number is used.

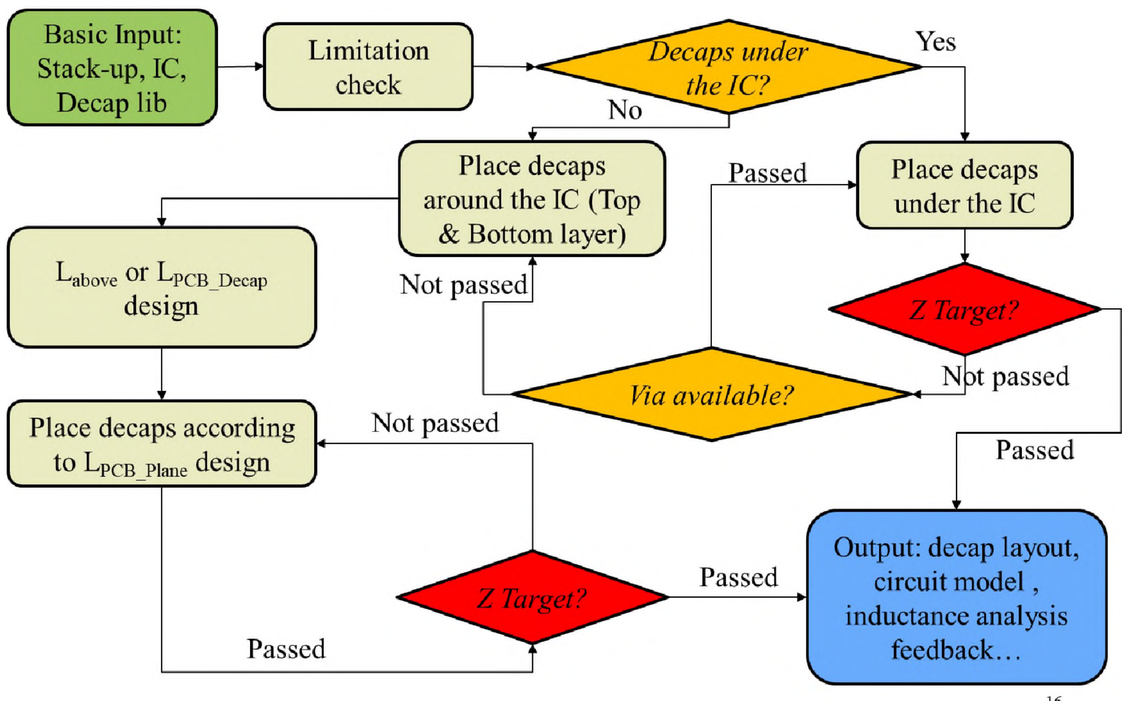
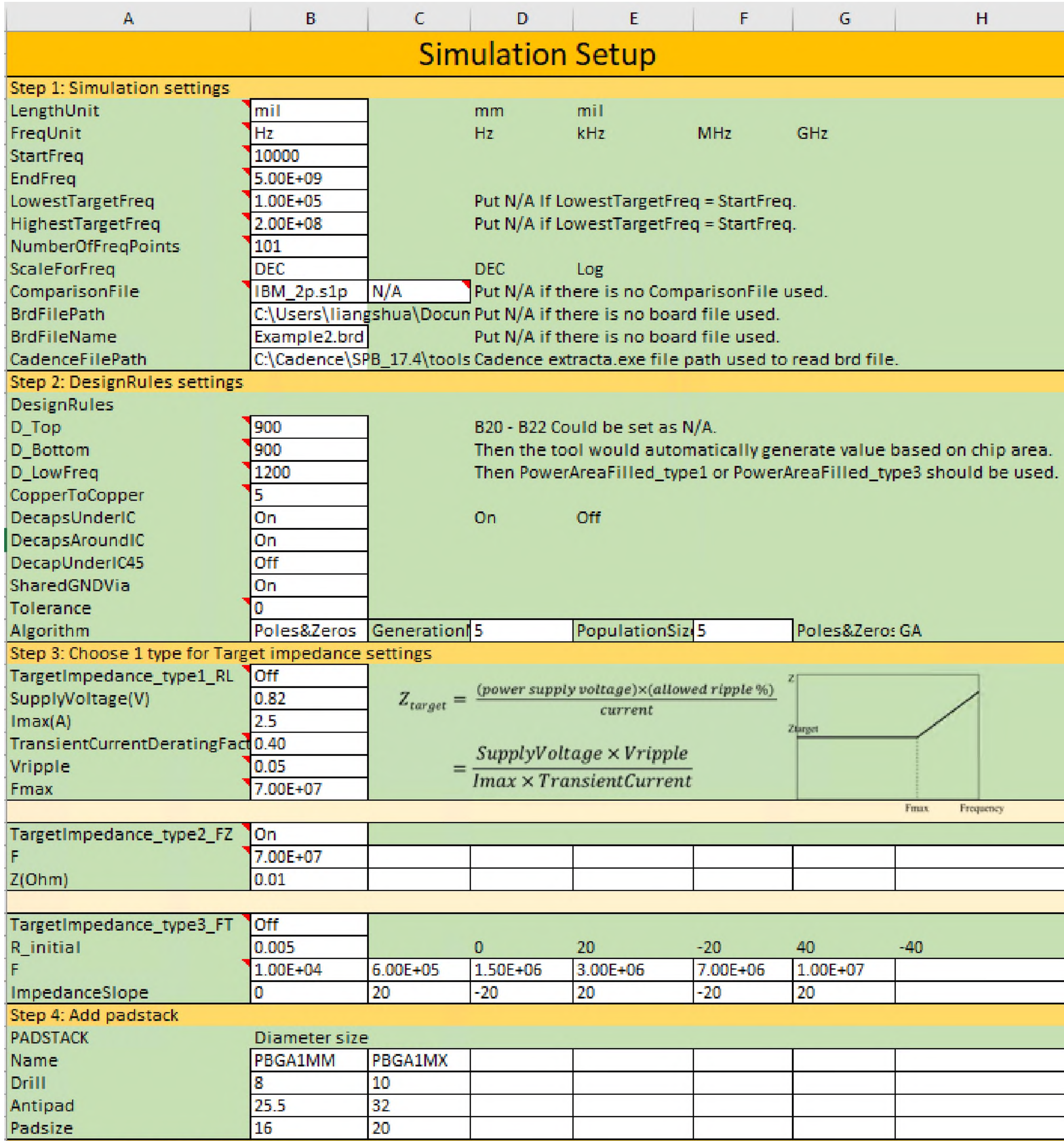


Figure 4.6 Design workflow for the pre-layout tool.

Then the details for the workflow would be explained step by step in the following section, including a special designed input spreadsheet, limitation checks, previous mentioned decap network design and the output report details and feedback from the design process.

4.3.1. Special Designed Input Spreadsheet. First, a excel format input spreadsheet is designed as the input file for the users, including four important segments, as Simulation, IC, Stackup and Decap, which are displayed in Figure 4.7 to Figure 4.10 as an example. There are comments added in the green area and rollover tips with the red rectangle. Then the users are required to fill in the white blank part. Others would be locked to avoid unwanted changes. It is created as simple as possible with rollover tips and comments to save users' time.



A	B	C	D	E	F	G	H
Simulation Setup							
Step 1: Simulation settings							
LengthUnit	mil		mm	mil			
FreqUnit	Hz		Hz	kHz	MHz	GHz	
StartFreq	10000						
EndFreq	5.00E+09						
LowestTargetFreq	1.00E+05		Put N/A If LowestTargetFreq = StartFreq.				
HighestTargetFreq	2.00E+08		Put N/A if LowestTargetFreq = StartFreq.				
NumberOfFreqPoints	101						
ScaleForFreq	DEC		DEC	Log			
ComparisonFile	IBM_2p.s1p	N/A	Put N/A if there is no ComparisonFile used.				
BrdFilePath	C:\Users\liangshua\Docun		Put N/A if there is no board file used.				
BrdFileName	Example2.brd		Put N/A if there is no board file used.				
CadenceFilePath	C:\Cadence\SPB_17.4\tools		Cadence extracta.exe file path used to read brd file.				
Step 2: DesignRules settings							
DesignRules							
D_Top	900		B20 - B22 Could be set as N/A.				
D_Bottom	900		Then the tool would automatically generate value based on chip area.				
D_LowFreq	1200		Then PowerAreaFilled_type1 or PowerAreaFilled_type3 should be used.				
CopperToCopper	5						
DecapsUnderIC	On		On	Off			
DecapsAroundIC	On						
DecapUnderIC45	Off						
SharedGNDVia	On						
Tolerance	0						
Algorithm	Poles&Zeros	GenerationN	5	PopulationSiz	5	Poles&Zeros GA	
Step 3: Choose 1 type for Target impedance settings							
TargetImpedance_type1_RL	Off						
SupplyVoltage(V)	0.82						
Imax(A)	2.5						
TransientCurrentDeratingFact	0.40						
Vripple	0.05						
Fmax	7.00E+07						
TargetImpedance_type2_FZ	On						
F	7.00E+07						
Z(Ohm)	0.01						
TargetImpedance_type3_FT	Off						
R_initial	0.005		0	20	-20	40	-40
F	1.00E+04	6.00E+05	1.50E+06	3.00E+06	7.00E+06	1.00E+07	
ImpedanceSlope	0	20	-20	20	-20	20	
Step 4: Add padstack							
PADSTACK	Diameter size						
Name	PBGA1MM	PBGA1MX					
Drill	8	10					
Antipad	25.5	32					
Padsize	16	20					

$$Z_{target} = \frac{(power\ supply\ voltage)\times(allowed\ ripple\ \%)}{current} = \frac{SupplyVoltage \times Vripple}{Imax \times TransientCurrent}$$

Figure 4.7 Simulation setup.

In the ‘Simulation’ part step 1, ‘LengthUnit’ and ‘FreqUnit’ are the length and frequency unit in the whole design; ‘StartFreq’ and ‘EndFreq’ are the frequency range which would be modeled in the calculation process, while ‘LowestTargetFreq’ and ‘HighestTargetFreq’ are the frequency range of interest in which the PDN performance

would be compared with the target impedance; 'NumberOfFreqPoints' and 'ScaleForFreq' define the frequency points used in each decade; 'ComparisonFile' is the possible file name input in case users plan to make a comparison between the too result and the existing snp file; 'BrdFilePath' and 'BrdFileName' are used to input the board file if the users wish to input geometry details from an existing design.

IC Pin Map							
Step 1: Fill B4 - B6							
PowerNetName	+0.9VB						
GndNetName	GND						
Padstack_Brdfile	On	Only can be on when IC type 1 in step 2 is used					
Padstack	PBGA1MM						
Step 2: Choose 1 type for IC pin map input							
IC_PIN_MAP_type1	On						
BrdFile	Would be the same in the Simulation setting part.						
ICName	UKR1						
IC_PIN_MAP_type2	Off		On	Off			
PinFilePath	C:\Users\liangshua\Documents\project\project5_Prelayout\Matlab\20200925_Pre						
PinFileName	u1_sw_pin.txt						
IC_PIN_MAP_type3	Off	pitch	39				
Row	8						
Column	8						
Type	Alternating	Alternating	Grid	Hex	Hex3	Row	
DeletedX	1	4					
DeletedY	1	4					
IC_PIN_MAP_type4	Off	pitch	39	X	7	Y	6
GND	PWR	GND	PWR	GND	PWR		
PWR	GND	PWR	GND	PWR	GND		
GND	PWR	GND	PWR	GND	PWR	N/A	
PWR	GND	PWR	GND	PWR	GND		
GND	PWR	GND	PWR	GND	PWR		
PWR	GND	PWR	GND	PWR	GND		

Figure 4.8 IC pin map.

Stackup					
BoardSizeX	4000				
BoardSizeY	4000				
Step 1: Choose 1 type for stackup input					
STACKUP_type1	On		On	Off	
LossTangent	N/A		B5 - B7 could be set as N/A.		
DielectricConstant	N/A		Then the tool would use the		
Conductivity (e7)	N/A		value in the .brd file.		
BrdFile	Would be the same in the Simulation setting part.				
STACKUP_type2	Off		Signal	Dielectric	Plane
UserDefinedName	Type	Thickness	Conductivity (e7)	DielectricConstant	LossTangent
D	Dielectric	0	N/A	4	0.03
TOP	Plane	2	5.96	N/A	N/A
D	Dielectric	4	N/A	4	0.03
L02	Plane	1.2	5.96	N/A	N/A
D	Dielectric	3.6	N/A	4	0.03
L03	Plane	1.2	5.96	N/A	N/A
D	Dielectric	4	N/A	4	0.03
L04	Plane	1.2	5.96	N/A	N/A
D	Dielectric	3.6	N/A	4	0.03
L05	Plane	1.2	5.96	N/A	N/A
D	Dielectric	4	N/A	4	0.03
L06	Plane	1.2	5.96	N/A	N/A
D	Dielectric	3.6	N/A	4	0.03
L07	Plane	1.2	5.96	N/A	N/A
D	Dielectric	4	N/A	4	0.03
BOTTOM	Plane	2	5.96	N/A	N/A
D	Dielectric	0	N/A	4	0.03
Step 2: Choose power layer(s)					
SinglePowerLayerSetting	Off		On: Handle as single power case		
SinglePowerLayerType	UserDefined		Middle	UserDefined	Sweep All
SinglePowerLayerName(s)	V11				
MutiplePowerLayerSetting	On		On: Handle as mutiple power case		
MutiplePowerLayerName(s)	V11	V12			
Step 3: Layer shape for power area fill					
Outer Boundary			All power layers are set with the same outer boundary.		
PowerAreaFilled_type1	Off				
Chip	Generating from the used brd file in step 2				
AreaFactorMutiplied	3				
PowerAreaFilled_type2	Off				
ChipSizeX	1000		Outer	Inner	
ChipSizeY	1200				
AreaFactorMutiplied	3				
PowerAreaFilled_type3	On				
X	-1500	1500	1500	-1500	
Y	-1500	-1500	1500	1500	

Figure 4.9 Stackup.

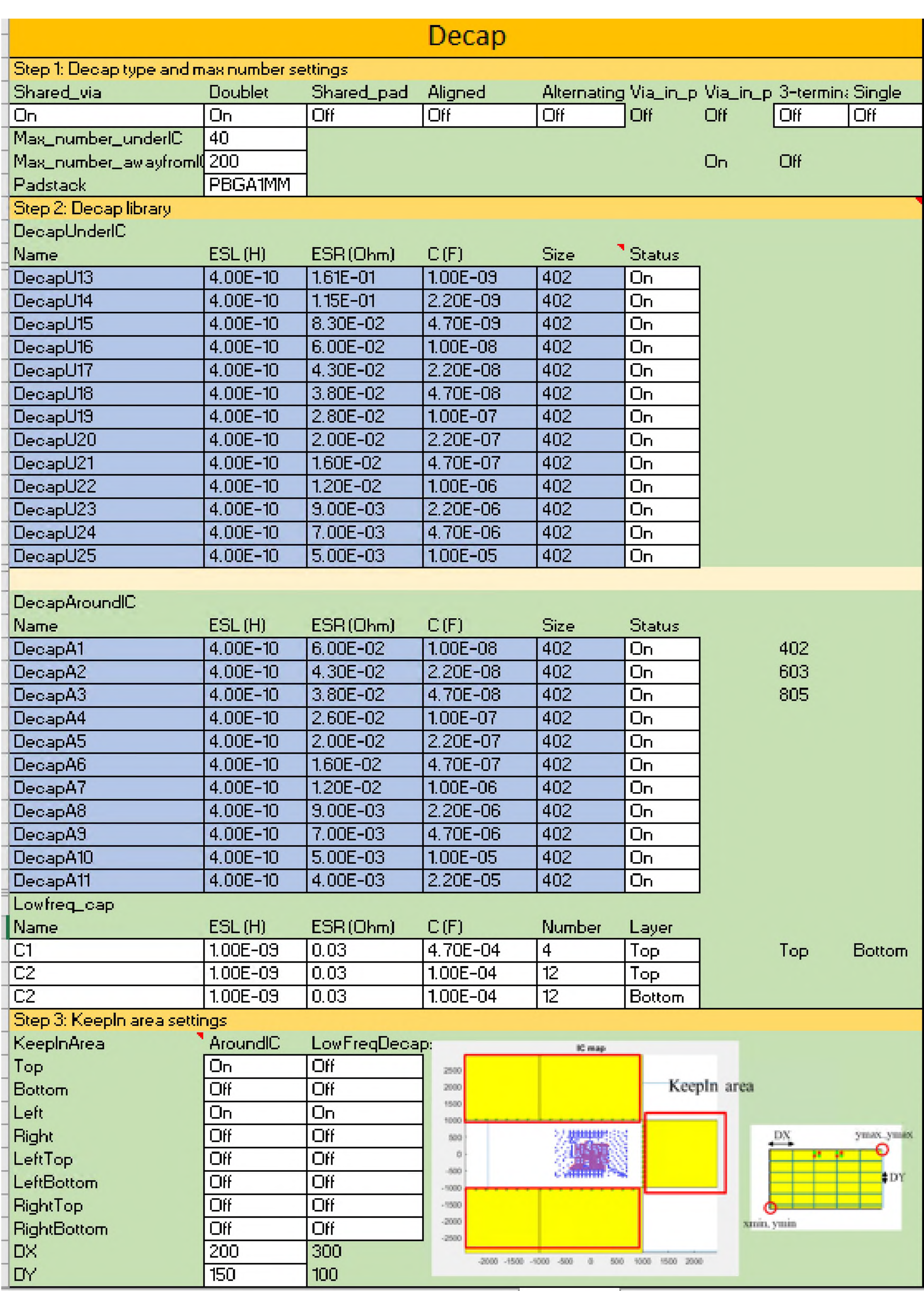
For step 2, 'D_Top', 'D_Bottom' and 'D_LowFreq' are explained in Figure 4.11 (a); 'CopperToCopper' is the minimum distance between two copper edge; 'DecapsUnderIC' and 'DecapsAroundIC' are the chooses of placing decaps under IC or around IC, which could be turned on or turned off; 'DecapUnderIC45' is a way to place decaps as 45 degree; 'SharedGNDVia' means that whether users allow shared ground vias

or not; ‘Tolerance’ is a term created to make the target easier or harder to achieve; ‘Algorithm’ is an option for the user to choose one decap placement algorithm, including ‘poles and zeros algorithm’, which is faster, and ‘genetic algorithm’, which maybe better in the decap number reduce than the first one but more time-consuming.

For the target impedance input in step 3, there are 3 kinds of definition in the design, including simple RL target impedance, freq-impedance definition and RLC target definition, which are shown in Figure 4.11 (b). And the padstack definition is in step 4, which has name, drill, antipad and pad size, which is plotted in Figure 4.11 (c). And the tool can only handle through- hole via case

Four different kinds of IC input are used in this tool. First, the power and ground net name should be the first input. The type 1 and type are utilizing the board file to input IC pin map from existing design; type 3 and type 4 require user to define the IC pin map. Figure 4.11 (d) are the different IC placement types [51] in type 3.

In the stackup part, first, the ‘BoardSizeX’ and ‘BoardSizeY’ are the max X and Y size to create a rectangular board, which is also the ground layer size. The stackup is either read from the board or created by the users. There two kinds of power layer setting, one is for the cases with power net area fill on single layer only and the layer on which the power net can be located can be swept over several or all layers for design discovery to develop a suitable solution; another is for the cases that power net area fills of the same net can be located on multiple layers. The footprint of the power net could be arbitrary, and the footprint is the same for the power net area fills on all layers on which it is located. For the outer boundary input, type 1 and type 2 are from the chip size and an area multiplied factor, while type 3 is from the dimensions by user’s input.



Decap

Step 1: Decap type and max number settings

Shared_via	Doublet	Shared_pad	Aligned	Alternating	Via_in_p	Via_in_p	3-termin:	Single
On	On	Off	Off	Off	Off	Off	Off	Off
Max_number_underIC	40							
Max_number_awayfromI(	200					On	Off	
Padstack	PBGA1MM							

Step 2: Decap library

DecapUnderIC

Name	ESL (H)	ESR (Ohm)	C (F)	Size	Status
DecapU13	4.00E-10	1.61E-01	1.00E-09	402	On
DecapU14	4.00E-10	1.15E-01	2.20E-09	402	On
DecapU15	4.00E-10	8.30E-02	4.70E-09	402	On
DecapU16	4.00E-10	6.00E-02	1.00E-08	402	On
DecapU17	4.00E-10	4.30E-02	2.20E-08	402	On
DecapU18	4.00E-10	3.80E-02	4.70E-08	402	On
DecapU19	4.00E-10	2.80E-02	1.00E-07	402	On
DecapU20	4.00E-10	2.00E-02	2.20E-07	402	On
DecapU21	4.00E-10	1.60E-02	4.70E-07	402	On
DecapU22	4.00E-10	1.20E-02	1.00E-06	402	On
DecapU23	4.00E-10	9.00E-03	2.20E-06	402	On
DecapU24	4.00E-10	7.00E-03	4.70E-06	402	On
DecapU25	4.00E-10	5.00E-03	1.00E-05	402	On

DecapAroundIC

Name	ESL (H)	ESR (Ohm)	C (F)	Size	Status	
DecapA1	4.00E-10	6.00E-02	1.00E-08	402	On	402
DecapA2	4.00E-10	4.30E-02	2.20E-08	402	On	603
DecapA3	4.00E-10	3.80E-02	4.70E-08	402	On	805
DecapA4	4.00E-10	2.60E-02	1.00E-07	402	On	
DecapA5	4.00E-10	2.00E-02	2.20E-07	402	On	
DecapA6	4.00E-10	1.60E-02	4.70E-07	402	On	
DecapA7	4.00E-10	1.20E-02	1.00E-06	402	On	
DecapA8	4.00E-10	9.00E-03	2.20E-06	402	On	
DecapA9	4.00E-10	7.00E-03	4.70E-06	402	On	
DecapA10	4.00E-10	5.00E-03	1.00E-05	402	On	
DecapA11	4.00E-10	4.00E-03	2.20E-05	402	On	

Lowfreq_cap

Name	ESL (H)	ESR (Ohm)	C (F)	Number	Layer		
C1	1.00E-09	0.03	4.70E-04	4	Top	Top	Bottom
C2	1.00E-09	0.03	1.00E-04	12	Top		
C2	1.00E-09	0.03	1.00E-04	12	Bottom		

Step 3: KeepIn area settings

KeepInArea	AroundIC	LowFreqDecap
Top	On	Off
Bottom	Off	Off
Left	On	On
Right	Off	Off
LeftTop	Off	Off
LeftBottom	Off	Off
RightTop	Off	Off
RightBottom	Off	Off
DX	200	300
DY	150	100

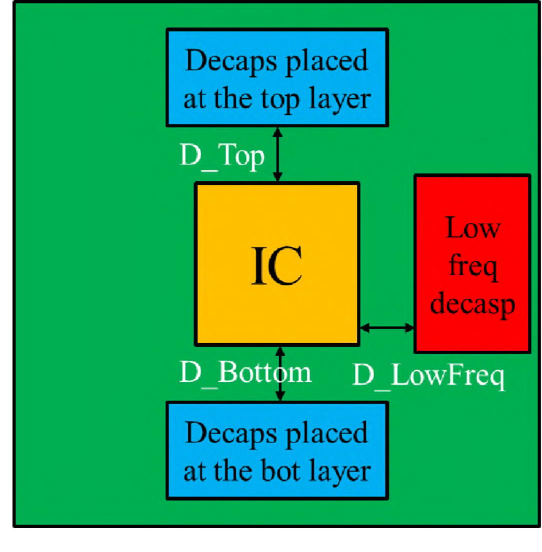
Figure 4.10 Decap.

The decap library is the last part for the input. There are 9 different decap layouts in the design (Figure 3.1) which could be used, and 'Via in Pad' and 'Via in Pad Alternating' are marked as off since the cost are high in these two designs.

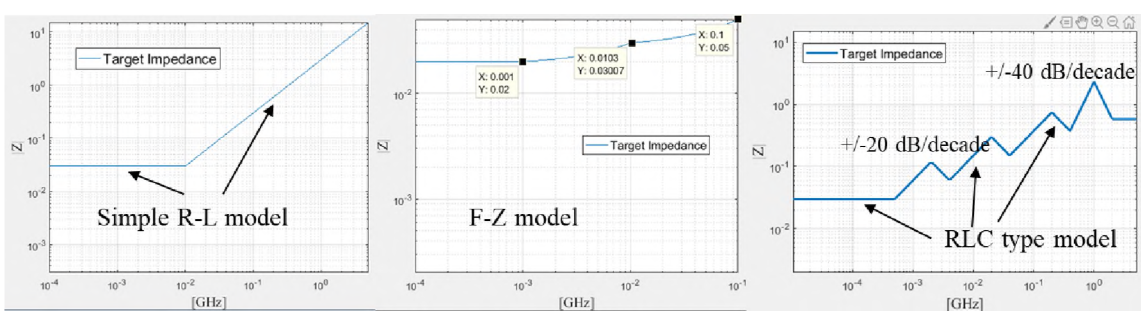
For under IC decaps, only the 'single' type would be used in the design since the existing power and ground vias are placed as single type. The decaps would be placed a little bit farther from the vias in the real production, leading to a special structure called 'Dog-bone', which the inductance is very small and would be ignored in this design. The widely used package sizes for under IC decaps are 0402 and 0201, which is decided by the minimum distance between the power vias and ground vias, referred as 'Pitch size'. Usually, 0402 package size would be used when the pitch size is 1 mm and 0201 package size would be used when the pitch size is 0.8 mm. The pitch would be input in the IC part or generated from the board file.

Only one decap layout and package size from step 1 would be used to achieve the minimum inductance for around IC decaps, the allowable package size is decided by users from 0805, 0603 and 0402 since 0201 package size is too small for around IC decaps. The ESL, ESR and C values in each decap type are collected from decap vendors. Then the possible inductance caused by different decap package size and type would be estimated in advance and the one decap size and layout with the smallest decap inductance would be used in the design. The keep in area for around IC decaps should be input in this part with the allowable space in the PCB and the dimensions for creating the grid.

The number and location for the low-freq decaps are also required for this version of the tool since there are no low-freq decaps optimization option. The keep in area definition which can place decaps is placed in step 3 with details put in the sheet.



(a)



(b)

Antipad

Pad

Drill

Alternating

Row

Hex

Grid

Hex3

(c) (d)

Figure 4.11 Input details. (a) Distance between decaps and IC part definition. (b) Three kinds of target impedance. (c) Size for the padstack. (d) Different types for IC pin placement.

4.3.2. Limitation Check. A limitation check is proposed before the design to give a brief estimation about the design possibilities. If the target cannot be met according to the input geometry, users can find other approaches such as improving the stackup or IC map to develop the design instead of wasting time on the decap network.

There are two steps for the limitation check. According to the equivalent circuit model, in high frequency range, plane capacitance shows short circuit as Figure 4.12 (a), then IC is the dominant inductance part and the minimum inductance in the design, which is referred as minimal L_{PCB_EQ}. By adding decaps, the inductance in mid frequency range could be reduced and if we add as many decaps as we can both under IC and around IC at the top and bottom layer and treat all decaps as short circuit as Figure 4.12 (b), as a result, there would be a best inductance we could achieve in this design process, which is referred as physical limitation of L_{PCB_EQ}. Figure 4.13 plots these two kinds of limitations and compare the inductance got from limitation check with target, the tool would tell the possibility for the design.

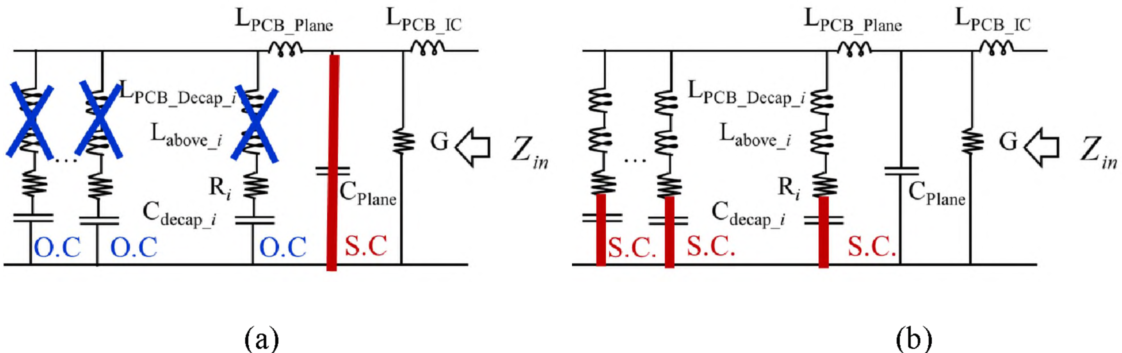


Figure 4.12 Equivalent circuit. (a) Equivalent circuit in high frequency range. (b) Equivalent circuit in mid frequency range when adding as many decaps as possible.

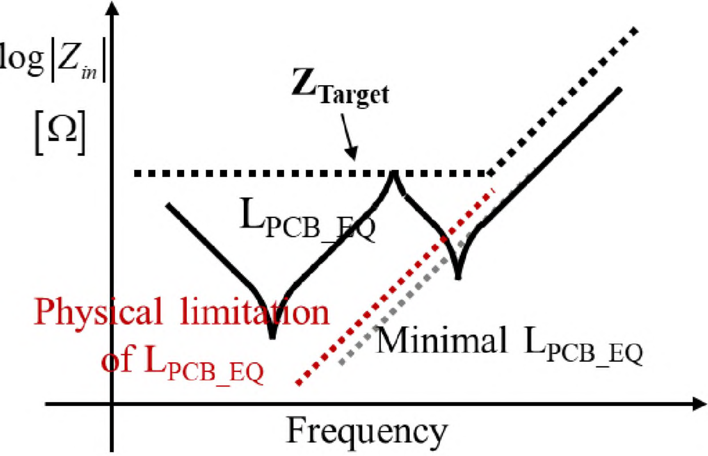


Figure 4.13 Two kinds of limitations.

4.3.3. Output Report with Feedback for Users. The output is including two parts: the decap solution and the impedance curve. First, there are geometry details for the stackup, padstack and board top view in the design. Then for each power layer settings, the impedance curve is exported and there are also a excel sheet contains the decap information such as ESL, ESR and C values, the x and y dimensions for vias and the decap layer location. Also, a picture and a list for the decap colors for different types are drawn based on the decap solution.

Following would lead to the stop of the tool, including:

- File cannot read due to format error, please make sure the file is compatible.
- Not enough room for low frequency decaps.
- Limitation checks failed.
- Z_{PDN} (Bare board only with low-freq decaps or/and VRM model) is larger than Z_{target} in the low frequency range, means need more low-freq decaps.
- Design completed only using under IC decaps.

- Design failed only using under IC decaps, and around IC decaps is not allowed.
- Design completed using both under IC and around IC decaps, or only around IC decaps if underIC decap is not allowable.
- Design failed using both underIC and around IC decaps, or only around IC decaps if underIC decap is not allowable.

More details for the output are plotted in the Section 4.4 with the tool solutions for real productions.

4.4. EXAMPLES FROM TYPICAL PRODUCTION

To make a conclusion for the designed pre-layout tool, first, after reading the input from the spreadsheet, the stackup and IC pin map are generated and the vias for the possible around IC decaps are also built together to calculate the inductance big matrix through Cavity Model method and BEM. Then based on [52]-[55], the inductance matrix is reduced and Z parameter for the bare board only with low frequency decaps is got from the node voltage theory. Then the decap network are designed based on the poles and zeros algorithm and the decap is added in the Z_{PCB_PDN} with matrix calculation. Finally, the output and feedback are provided for the users.

The tool is applied in different real cases and several simulations for the existing designs are given based on the method in [56]-[58]. The performance of the tool is tested with GA.

4.4.1. Design Case #1 with One Power Layer. When applying the pre-layout tool to the first case, the target impedance would be achieved by only placing decaps under IC

at the bottom layer. In this section a real production from industry is used to show the convenience of the tool.

All the geometry details are input in the spreadsheet, including the stackup, IC pin map, decap distance between the IC center and so on. Then 29 larger decaps are placed at the board to lower the impedance at low frequency according to the real design. The geometry details are plotted in Figure 4.14. In order to reduce the decap amount, the type of the decaps in the library are extended and the values are listed in Table 4.3.

Table 4.3 Pre-added decap library.

Name	ESL (H)	ESR (Ohm)	C (F)	Size
Under IC decaps				
DecapU1	4.00E-10	8.30E-02	4.70E-09	0402
DecapU2	4.70E-10	7.80E-02	1.00E-08	0402
DecapU3	4.50E-10	4.40E-02	2.20E-08	0402
DecapU4	4.00E-10	4.00E-02	4.70E-08	0402
DecapU5	8.60E-10	2.85E-02	1.00E-07	0402
DecapU6	4.40E-10	2.00E-02	2.20E-07	0402
DecapU7	4.00E-10	1.59E-02	4.70E-07	0402
DecapU8	7.00E-10	1.09E-02	1.00E-06	0402
DecapU9	3.71E-10	1.00E-02	2.20E-06	0402
DecapU10	3.00E-10	9.00E-03	4.70E-06	0402
DecapU11	4.00E-10	5.00E-03	1.00E-05	0402

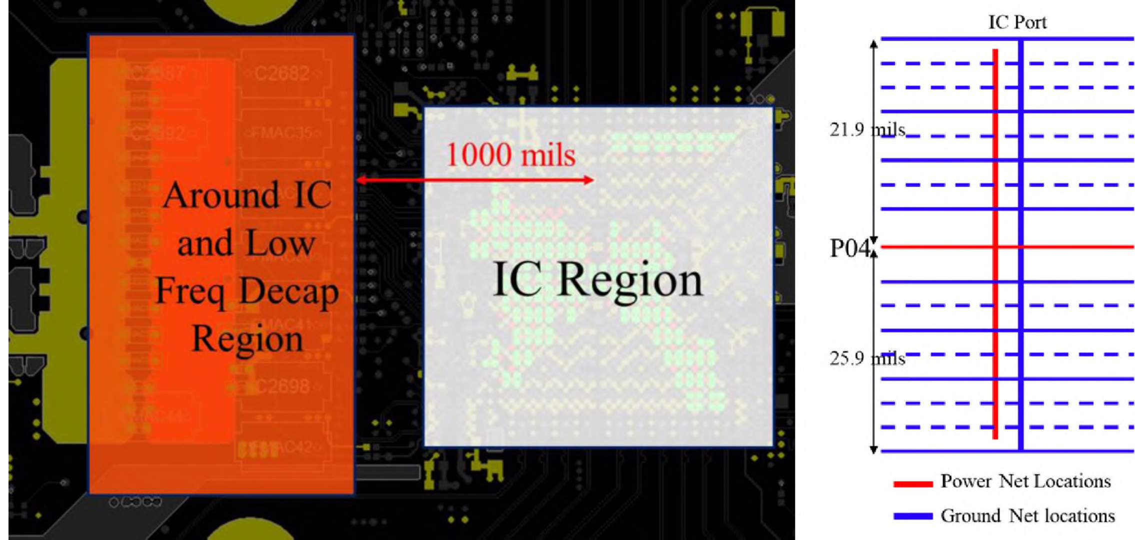
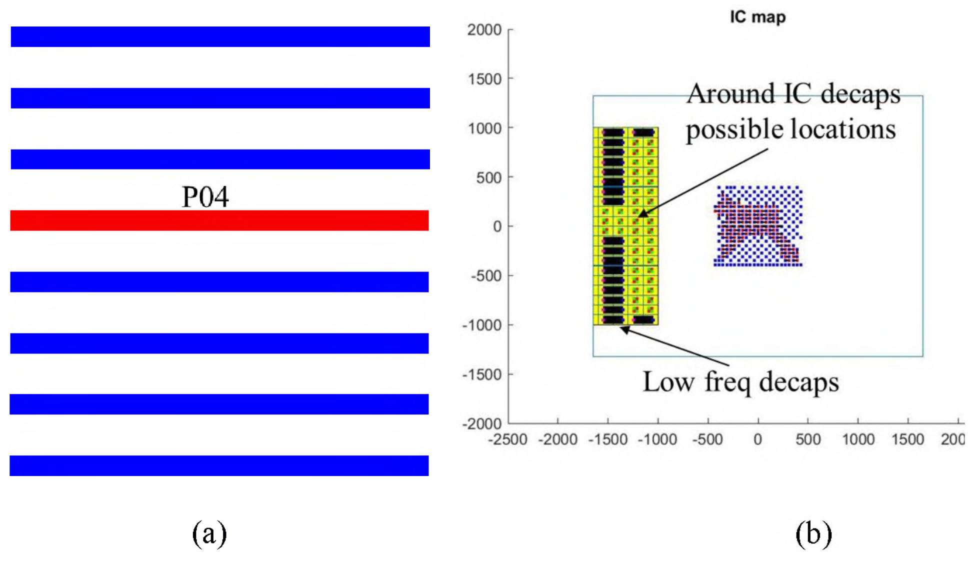


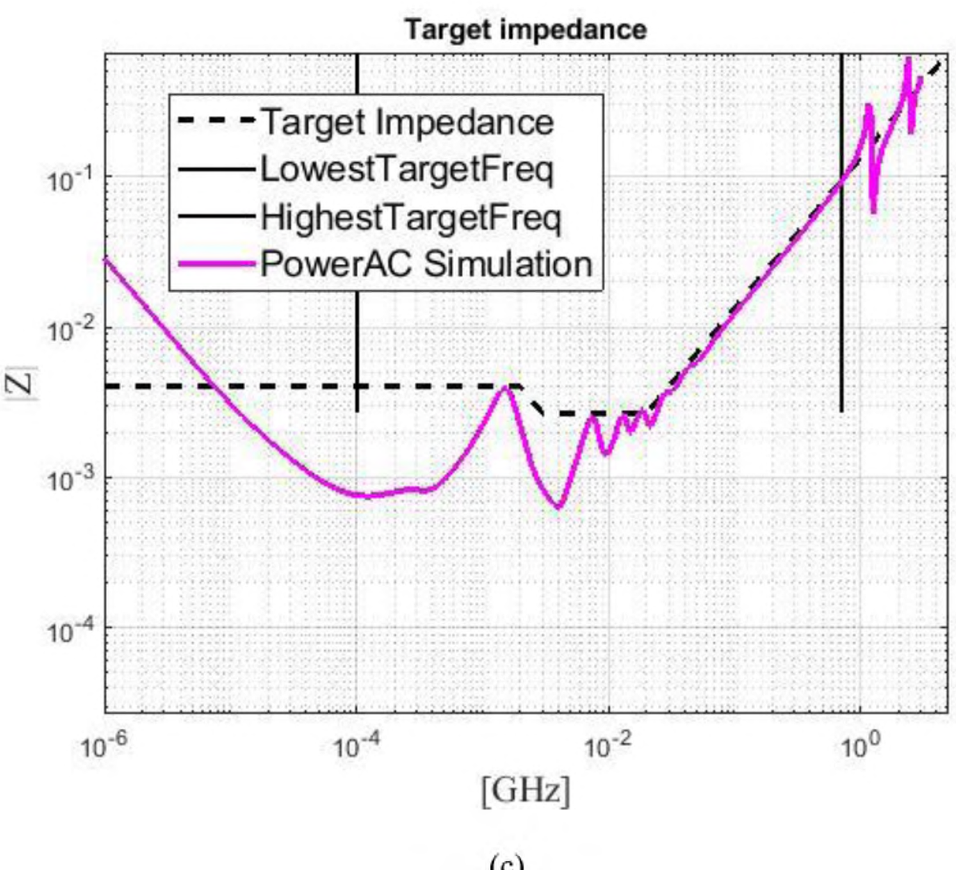
Figure 4.14 Board bottom layer view and the stackup for the design.

The designer also provides a solution and PowerSI simulation result. Based on the power AC simulation, a special target impedance is generated to achieve a better performance with the solution. First a resistance about 4 mOhm is used for the inductance comparison in the low frequency range. And then a capacitance and a resistance again is used in the middle frequency range to make sure the designed target is close to the simulation result. Finally, an inductance with 20/db per decade increase is created to model the circuit behavior at high frequency.

The stackup, low frequency decaps location and possible around IC decaps location are shown in Figure 4.15, while the interest range of the frequency is from 100 kHz to 800 MHz. The decap solution made from the pre-layout tool is shown in Figure 4.16 (a) with a comparison with the industry solution. And the decap location is shown in Figure 4.16 (b), while different color refers to different decap type, and the decap number difference is listed in Table 4.4.



(a) (b)



(c)

Figure 4.15 Test case. (a) Stackup details generated by pre-layout tool. (b) Decap location details generated by pre-layout tool. (c) PowerSI simulation result and special designed target impedance.

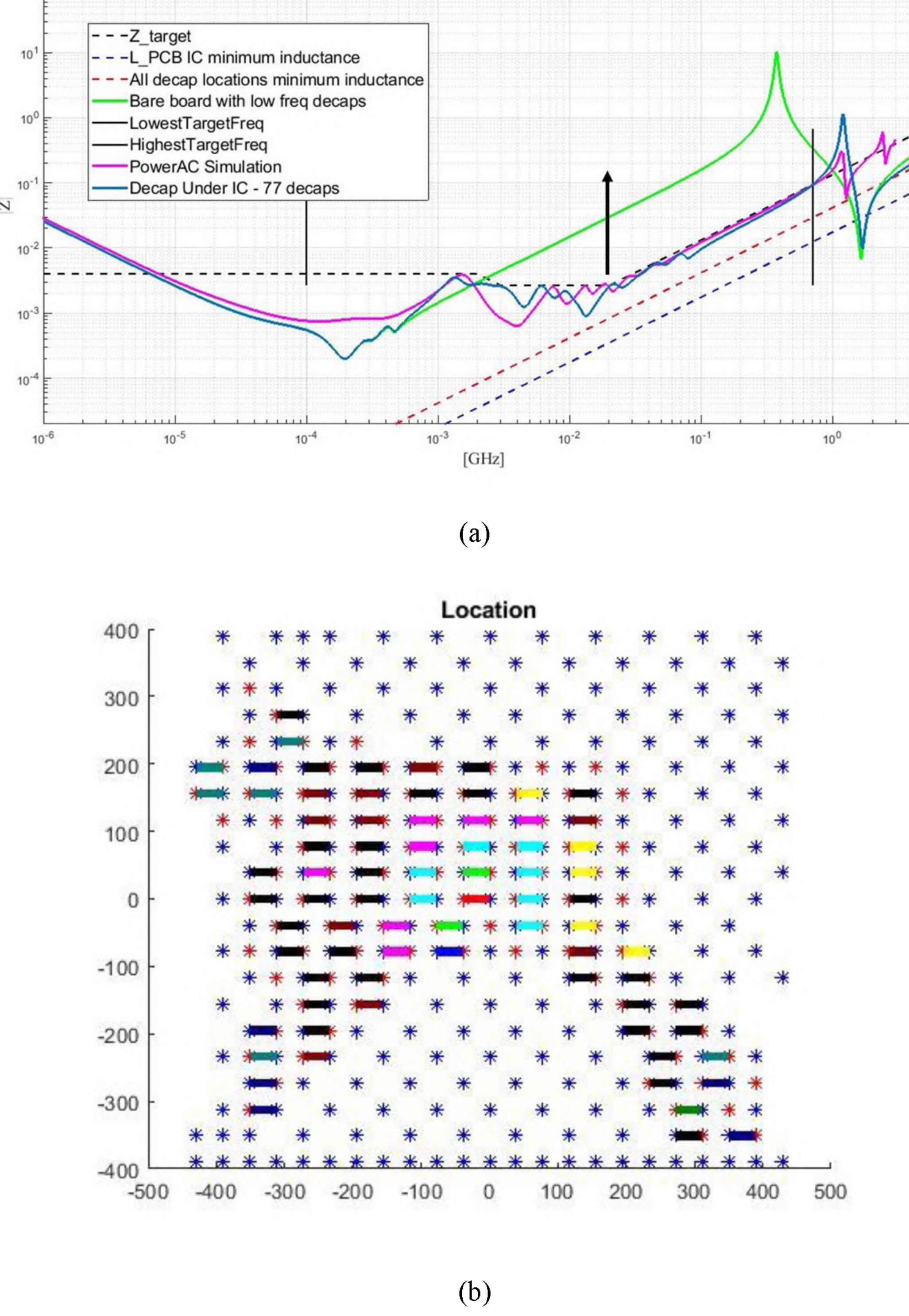


Figure 4.16 Solution. (a) Impedance curve and the impedance comparison between industry solution and pre-layout solution. (b) Decap location for the pre-layout solution.

Table 4.4 Decap solutions comparison from real design and pre-layout tool.

Cap Value (uF)	Size	Location	Industry Solution	Pre-layout Solution
0.0047	0402	UnderIC	0	6
0.01	0402	UnderIC	10	6
0.022	0402	UnderIC	12	1
0.047	0402	UnderIC	18	10
0.1	0402	UnderIC	12	31
0.22	0402	UnderIC	20	5
0.47	0402	UnderIC	0	7
1	0402	UnderIC	23	7
2.2	0402	UnderIC	16	1
4.7	0402	UnderIC	0	2
10	0402	UnderIC	0	1
22	0603	Bot layer around IC	3	3
47	0805	Bot layer around IC	4	4
100	1209	Bot layer around IC	12	12
470	7374	Top layer around IC	10	10
Total			111+29=140	77+29=106

There is a greatly reduced in the decap number while using pre-layout solution since the decap library is extended. There are only 7 different under IC decap types in the original design, while 11 types in the new pre-layout solution. Around IC decaps are not used in both real design and pre-layout solution, since the target impedance could be met using available IC vias to place decaps under IC.

4.4.2. Design Case #2 with One Power Layer and Multiple Power Layer Settings. When applying the pre-layout tool to the next case, the target impedance would

also be achieved by only placing decaps under IC at the bottom layer. The difference is that in this case there are only one power layer, but the designer plans to check the solution difference when placing power layer on different layers in the stackup.

In this case, the geometry is input by a different option in the sheet instead of simply adding the path and name of the existing board file. The board file is also not provided as part of input in this case, but an txt format file is used as the input for the power and ground vias of the IC pin map. The stackup, board top view and IC pin map are plotted in Figure 4.17 and Figure 4.18, and it is a one power layer case, but the users plan to have a look at both when the 6th layer is the power layer and when the 9th layer is the power layer. At this requirement, the tool would run the design twice for each power layer setting and give a comparison when placing one power layer on different layers. There is a simple VRM model, a series of 1 mOhm resistance and 0.2 nH inductance, added in the real production. However, the first version of the tool cannot handle cases with VRMC models so that it utilizes low-freq decaps (18 decaps with 470 uF, 2.3 nH and 49 mOhm, placing on the top layer) to reduce the impedance at low frequency.

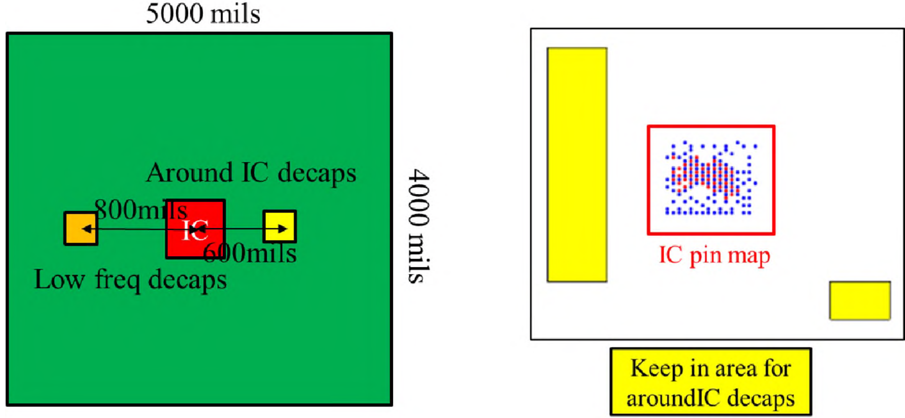


Figure 4.17 Board top view and IC pin map with power and ground vias.

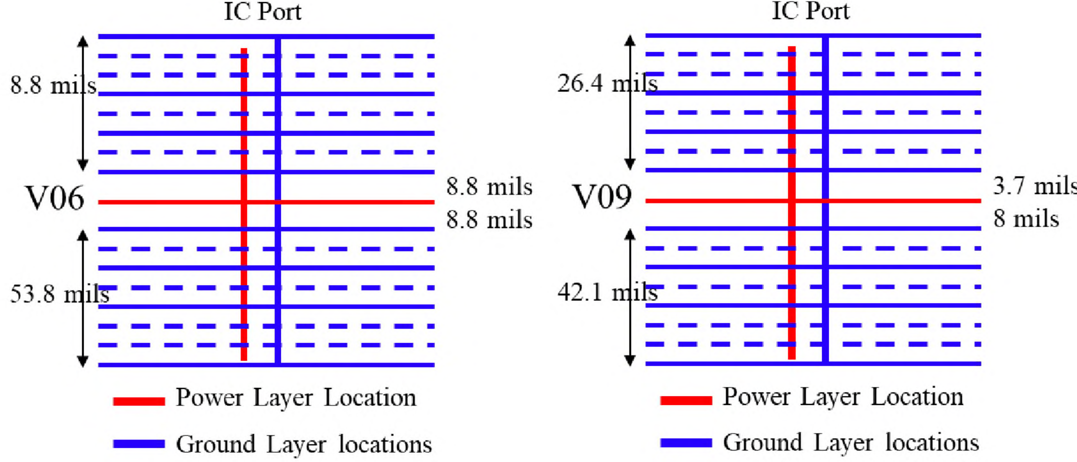


Figure 4.18 Stackup for different power layer settings.

There are totally 44 available IC pins to place decaps under IC and all possible around IC decaps are placed on the top layer since the top layer is closer to the power layer, which is near the middle of the stackup, under both conditions than the distance between bottom layer to the power layer. The used decap library is listed in Table 4.5, similar with the library input in the case in Section 3.2. Two different solutions from the pre-layout tool are given in Figure 4.19 (a) and (b), and a comparison between these two power layer settings is plotted in Figure 4.19 (c). The interest frequency range is from 100 kHz to 20 MHz. When the 6th layer is the power layer, only 43 under IC decaps are needed, while 44 under IC decaps and 2 around IC decaps are needed when 9th layer is set as power layer. The most essential conclusion draw from the solutions is that placing power layer near the decap network is a useful way to reduce the decap number while reaching the target, which is the same with the guideline generated from Section 4.1.1.

Table 4.5 Pre-added decap library.

Name	ESL (H)	ESR (Ohm)	C (F)	Size
Under IC decaps				
DecapU1	4.00E-10	3.80E-02	4.70E-08	0402
DecapU2	4.00E-10	2.80E-02	1.00E-07	0402
DecapU3	4.00E-10	2.40E-02	1.50E-07	0402
DecapU4	4.00E-10	2.00E-02	2.20E-07	0402
DecapU5	4.00E-10	1.60E-02	4.70E-07	0402
DecapU6	4.00E-10	1.20E-02	1.00E-06	0402
DecapU7	4.00E-10	9.00E-03	2.20E-06	0402
DecapU8	4.00E-10	7.00E-03	4.70E-06	0402
DecapU9	4.00E-10	5.00E-03	1.00E-05	0402
Around IC decaps				
DecapA1	3.70E-10	1.90E-01	1.00E-05	0805
DecapA2	3.70E-10	1.47E-01	2.20E-05	0805
DecapA3	3.70E-10	1.40E-01	4.70E-05	0805

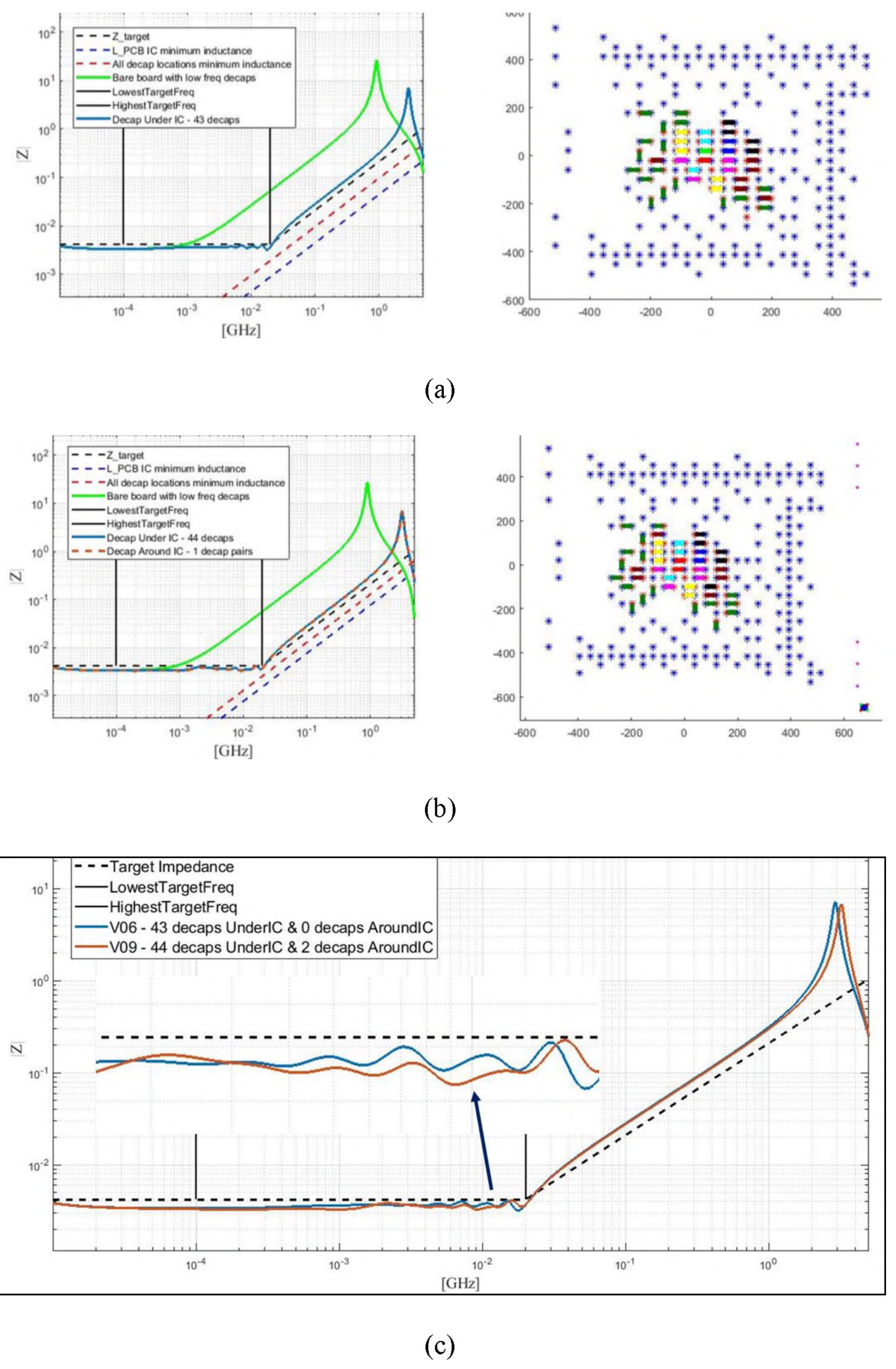


Figure 4.19 Solutions. (a) Impedance curve and decap location when 6th layer is set as power layer. (b) Impedance curve and decap location when 9th layer is set as power layer. (c) Comparison for two different power layer settings.

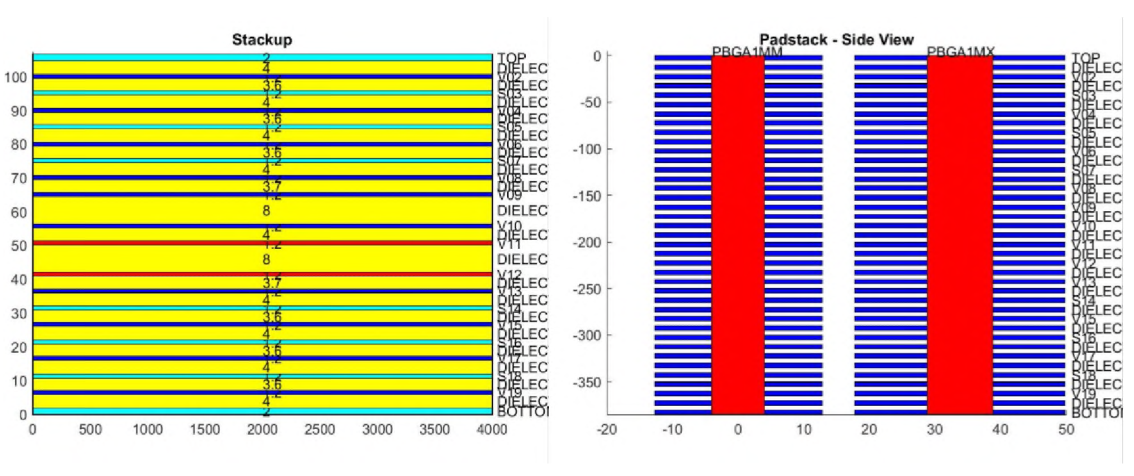
Then a decoupling solution with ‘V09’ power layer setting and 44 maxima under IC decaps made from an industry designer is compared from the pre-layout tool solution (Figure 4.19 (b)), which is listed is Table 4.6.

Table 4.6 Decap solutions comparison from real design and pre-layout tool.

Cap Value (uF)	Size	Location	Real Design Solution	Pre-layout Solution
0.047	0402	UnderIC	0	17
0.1	0402	UnderIC	12	5
0.15	0402	UnderIC	10	6
0.22	0402	UnderIC	9	5
0.47	0402	UnderIC	8	4
1	0402	UnderIC	3	3
2.2	0402	UnderIC	1	2
4.7	0402	UnderIC	1	0
10	0402	UnderIC	0	2
10	0805	AroundIC	8	2
22	0805	AroundIC	4	0
47	0805	AroundIC	0	0
Total			44+12 = 56	44+2 = 46

The pre-layout solution uses 10 less decaps than the real design. The difference is that the pre-layout tool use two more decap types in the library. Also, decap location and type optimization algorithms play an important role in reducing the decap quantity [59].

4.4.3. Design Case #3 with Two Power Layers. The geometry details for the last design are the same with Figure 3.6 and Figure 3.12 (d). All other information is demonstrated in Figure 4.7 to Figure 4.10 and the only difference is that the ESL values for all the decaps in the under IC decap library is set as 0.3 nH. The output for the geometry information is plotted in Figure 4.20.



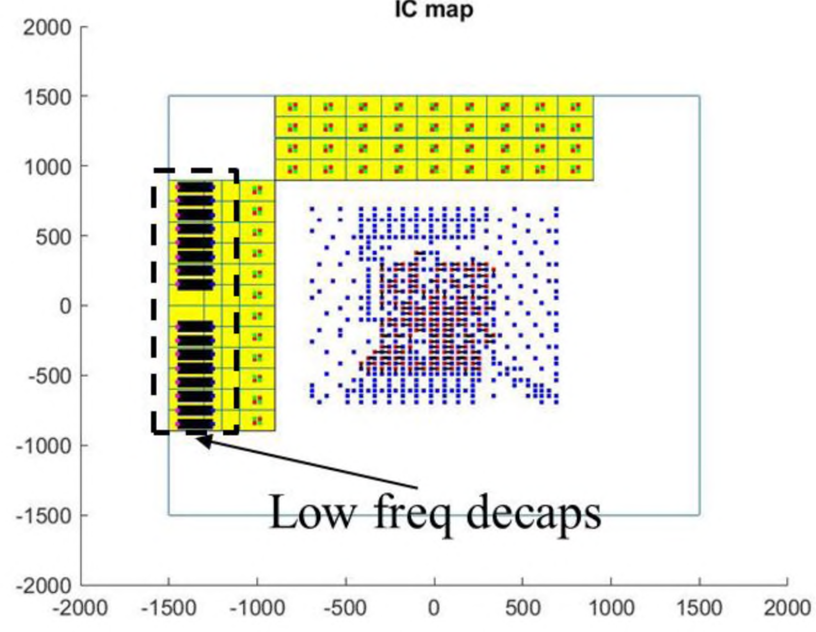


Figure 4.20 Geometry details.

The comparison between the simulation for the design with 67 decaps, the pre-layout calculation with the same design with 67 decaps, the poles and zeros algorithm solution with 53 decaps and the GA solution with 50 decaps is placed in Figure 4.21.

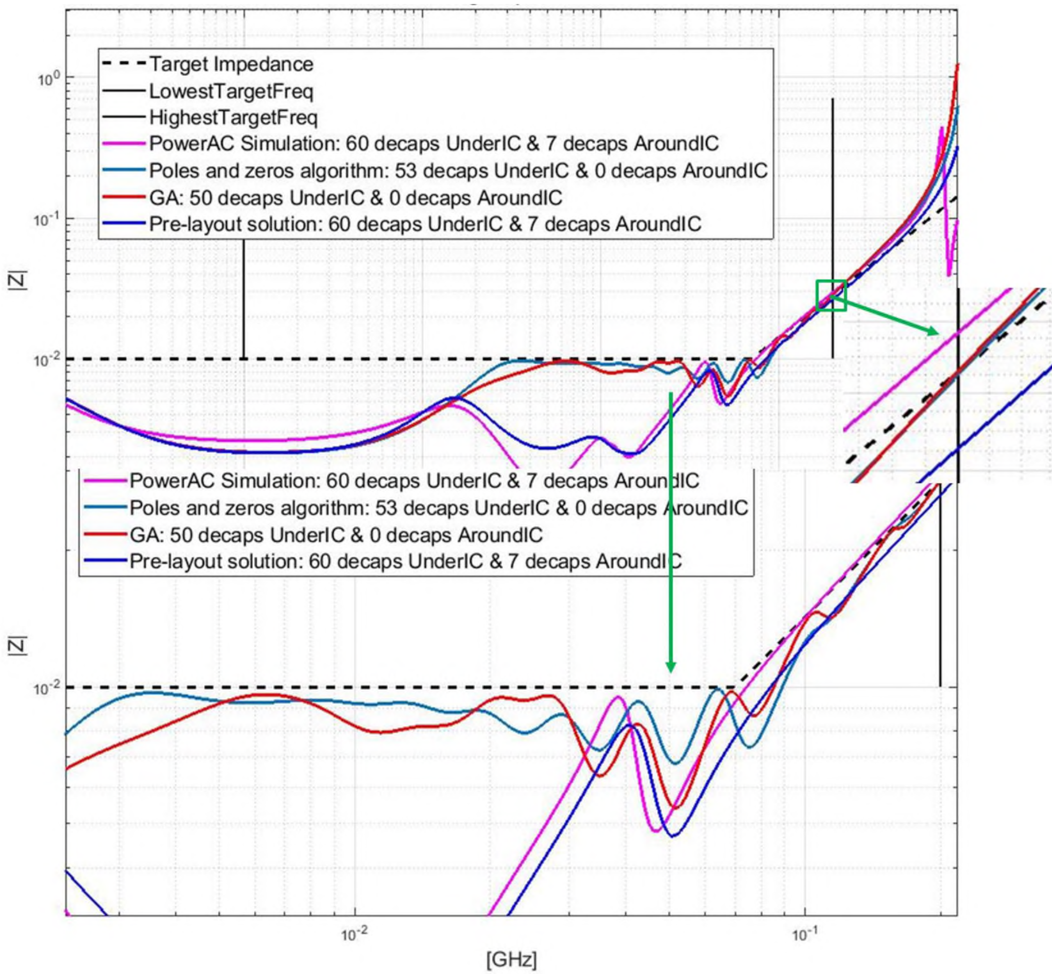


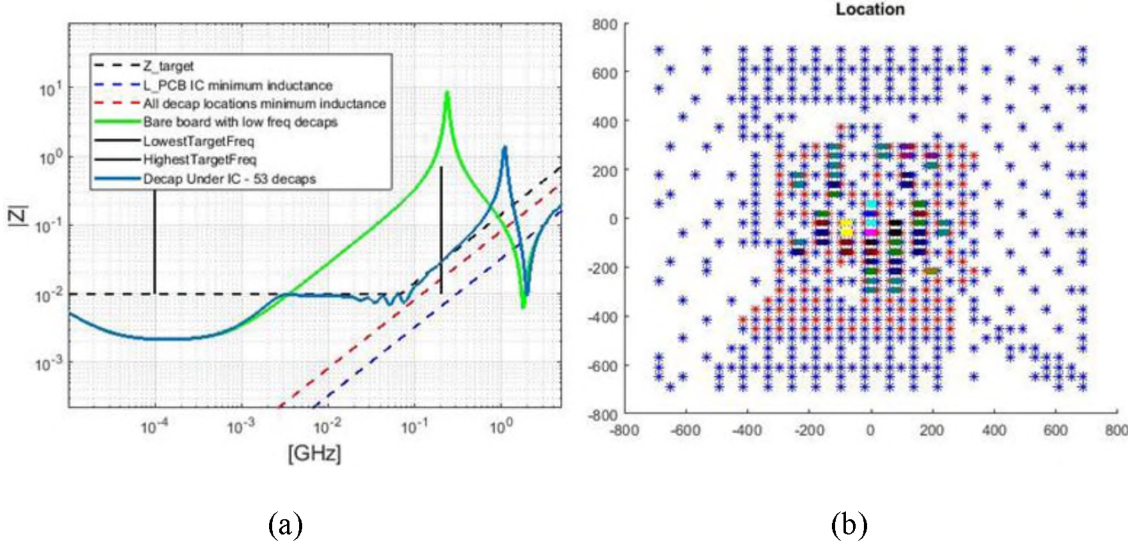
Figure 4.21 Impedance curve.

Then the details for the zeros and poles algorithm solution with results from the limitation checks are in Figure 4.22 (a) and the decap location and type information is drawn in Figure 4.22 (b). The output for the decap details are listed in Table 4.7. The

maximum number for under IC decaps is set as 60 and both solutions from the poles and zeros algorithm and GA are reaching the target with only under IC decaps.

Table 4.7 Decap details for solutions from poles & zeros algorithm and GA.

Type	C	Num – GA	Num – P&Z	Num – Real design	PlaceOrder – GA	PlaceOrder – P&Z
1	1 nF	1	1	20	49	53
2	2.2 nF	4	3		40,41,45,47	50,51,52
3	4.7 nF	9	16		29-34,37,39,42,	33-49
4	10 nF	15	12	20	20-25,27,28,35, 36,38, 43,46,48,50	20-32,38
5	22 nF	8	7		13-19,26	14,16-19,22,28
6	47 nF	3	5		10,11,12	10-13,15
7	100 nF	3	3	20	7-9	7-9
8	220 nF	3	2		5,6,44	5,6
9	470 nF	1	1		4	4
10	1 uF	0	2		0	2,3
11	2.2 uF	2	1		2,3	1
12	4.7 uF	1	0		1	0



(a) (b)

Figure 4.22 Pre-layout solution. (a) Impedance curve for pre-layout solution. (b) Decap type and location for pre-layout solution.

Based on Figure 4.21, following conclusion could be made:

- The pre-layout calculation result agrees with the simulation before 1 GHz.
- Both poles and zeros algorithm and GA are better than the original design which uses 60 under IC decaps and 7 around IC decaps.
- The poles and zeros algorithm use 3 more decaps than GA, while it only needs 3 minutes for the decap solution and GA needs around 11 minutes.
- The solutions from the poles and zeros algorithm and GA are similar. The results from these two algorithms are close to the target impedance, which means that the primary estimation about how to minimize the decap number based on poles and zeros is reasonable.

Both algorithms would be added in the tool so that the tool would contain two options during the design. In the future version, the voltage ripple calculation also will be added in the tool [60] – [61].

5. CONCLUSION

A pre-layout tool based on physics is built in PCB PDN design to achieve industry specifications with minimum number of decaps. During the calculation process, all current segments inductance contribution in all layers are modeled and the self-inductances for every segments and mutual inductance between segments are extracted using the cavity model and BEM. The calculation process of one of the inductance segments, L_{PCB_Decap}, is validated by two-port measurement. After that, circuit reduction can be done to produce an impedance equivalent circuit model in which the model values can be calculated. The impedance equivalent circuit model can be directly related to the geometry and current paths.

The Z parameter for the bare board can be calculated by node voltage method and the decaps can be placed at the ports in the Z matrix through KCL and KVL equation. Fundamental inductance limits are calculated to determine if the design can meet the target impedance after placing as much decaps as possible at first to save the time. Then a special designed poles and zeros algorithm are defined to optimize the decap network. The solution is compared with genetic algorithm and it's a faster algorithm with wonderful performance.

The tool can also be applied for multi-layer PCB with arbitrary number of layers. The power area fill shape can be irregular, and it can handle cases with multiple power layers. A well-designed input spreadsheet is created with more than one meaning for the target impedance, IC pin map, stackup and power area fills to save users' time.

In the future, more functions are suggested to add in the tool for improvement. The ground layer should be defined as arbitrary shape so that it has the ability to handle more

complex case. More elaborate VRMC, PKG and Chip model can be used by RLC values or s parameter to model real situation and reduce the impedance in low and high frequency range. Also, the L_{above} calculation is needed to develop by equation estimation to save lots of time and decap ESL value is required to be generated by PEEC to increase inductance calculation accuracy. There are also some other discussions about low freq decaps optimization, multiple objective optimization such as decap cost and other functions such as voltage ripple estimation.

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