Summer 2021

Contributions to the performance of thin film capacitors for high reliability applications

Daniel Krueger

Department: Materials Science and Engineering

CONTRIBUTIONS TO THE PERFORMANCE OF THIN FILM CAPACITORS FOR HIGH RELIABILITY APPLICATIONS

by

DANIEL SCOTT KRUEGER

A DISSERTATION

Presented to the Graduate Faculty of the

MISSOURI UNIVERSITY OF SCIENCE AND TECHNOLOGY

In Partial Fulfillment of the Requirements for the Degree

DOCTOR OF PHILOSOPHY

in

CERAMIC ENGINEERING

2021

Approved by:

Wayne Huebner, Advisor
Robert W. Schwartz, Co-Advisor
Richard K. Brow
William G. Fahrenholtz
James Drewniak
J. Ambrose Wolf

PUBLICATION DISSERTATION OPTION

This dissertation consists of the following three articles, formatted in the style used by the Missouri University of Science and Technology:

Paper I, found on pages 16-31, has been published in the *Journal of Microelectronic and Electronic Packaging* ***2016****, vol. 13, No. 3, pp. 95-101.*

Paper II, found on pages 32-52, has been submitted to the *International Journal of Ceramic Science and Technology.*

Paper III, found on pages 53-71, has been submitted to *IEEE Transactions on Dielectrics and Electrical Insulation.*

ABSTRACT

Capacitors are critical devices in microelectronic assemblies that must be incorporated into electronic systems through a variety of ways such as integrated or discrete devices. This work has developed new thin film capacitors deposited directly onto multichip module or printed circuit board surfaces to benefit from closer integration that enhances system performance for use in high reliability applications. The capacitors serve as filters or provide tuning and energy storage functions. Unexpected performance was observed during development that included low adhesion of the films to the substrates, higher effective dielectric constants than reported in literature, and low yields. Three publications resulted from this work with Paper I presenting a study of thin films on low temperature cofired ceramic (LTCC) and their reliability for multiple functions. The thin film and LTCC system are modeled with results suggesting a mechanism of enhancing thin film adhesion to the LTCC through a combination film composition and surface modification. Paper II presents measurements of dielectric properties of thin film capacitors on LTCC. Multiple mechanisms are detailed that contribute to the measured dielectric constant values of the capacitors. One case is modeled to determine the extent of dielectric constant enhancement from fringe fields related to capacitor dimensions. Paper III describes the behavior of thin film capacitors with varying electrode compositions and configurations. Trends are observed that suggest energy band overlap and electrode work functions are influential in dielectric properties and yield of the capacitors. A preferred electrode composition and configuration is suggested based on the capacitor performance.

ACKNOWLEDGMENTS

I would like to thank my parents, Warren and Betty Jane Krueger, who instilled in me a deep faith in God, the belief that you can do anything you set your mind to, and to never give up. My thanks go to my children, Ritter, Reagan, and Luke, who have been my motivation throughout my PhD. My love and thanks to my wife, Dr. Mary Cristina Ruales Ortega, who has provided constant support, encouragement, love, and understanding while I pursued what others have said wasn't possible.

Thank you is completely inadequate to express my gratitude to my advisor, Dr. Wayne Huebner, who has been an example, mentor, and friend without whom, none of this program or pursuit would have been possible. I would also like to thank Dr. Robert W. Schwartz, who has also been a constant source of advising, mentoring, and guidance. My thanks go to my committee that includes Dr. Ambrose Wolf, Dr. William G. Fahrenholtz, Dr. Richard K. Brow, and Dr. James Drewniak for their thoughtful feedback and patience.

My sincere thanks also go to Dr. John Jungk, Dr. Dennis Eichorst, and Dr. Dave Wieliczka who served as mentors and advisors at Honeywell FM&T along with my coworkers and the many other engineers and scientists that have provided support during this research. Additionally, many thanks go to James Claypool, Aaron Reed, Lauren Nuckels, Cassandra Hurley, Ben Lawrence, Bailey Ricketts, and Matt Webster for their work in support of this research. This work was funded by the Department of Energy's Kansas City National Security Campus, operated by Honeywell Federal Manufacturing & Technologies, LLC under contract number DE-NA0002839.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

SECTION Page

PAPER II

PAPER III

LIST OF TABLES

SECTION

1. INTRODUCTION

1.1. RESEARCH OBJECTIVE

The purpose of this research is to characterize thin film dielectrics and conductors important to capacitors and other devices on a variety of LTCC and glass substrates as an alternative technology to discrete capacitor devices for use within MCMs. Specifically, the processing, structure, properties, and performance (PSPP) interrelations of the thin films for capacitors and other functionality on these substrates has been explored and documented in peer reviewed journal articles. Gaining an understanding of these relationships is important for using these materials and devices at high frequencies and fields and ensuring they demonstrate high reliability and performance. In particular, the material interactions between electrodes and dielectrics within metal-insulator-metal (MIM) capacitors, surfaces the devices are fabricated on, and the relationship between the materials and adhesion to the substrates requires more complete understanding.

The first article has been completed and published and this describes how surface energies of thin film metals and LTCC substrate materials can be used to determine the preferred combinations for enhanced film adhesion. The article titled "Thermodynamic Analysis of Physical Vapor Deposited Thin Films on Low Temperature Cofired Ceramic" was published in 2016 in the peer reviewed Journal of Microelectronics and Electronic Packaging.

The second article has been completed and submitted for review, and it describes the multiple mechanisms that contribute to dielectric constant enhancement. One such mechanism is the contribution of fringe field capacitance to the observed capacitance and the relationship of the fringe field capacitance to capacitor geometry, including electrode edge tapering. The extent of the contribution to increased capacitance, and therefore effective dielectric constant enhancement due to fringe fields, is modeled and reported. This article was submitted to the International Journal of Ceramic Science and Technology on January 26, 2021.

The third article focused on effects of various materials on the performance of thin film capacitors. This paper reported on the experiments exploring Ag, Al, Au, Cu, and Pt electrodes in multiple combinations with Al_2O_3 as the dielectric. Non-Ohmic, non-linear conduction was observed in capacitors with certain electrode materials and this behavior was studied in-depth along with the effect of dielectric thickness and substrate material. This article was submitted to IEEE Transactions on Dielectrics and Electrical Insulation on March 24, 2021.

1.2. BACKGROUND

The reliability and performance of thin film capacitors are ultimately influenced by the relationships between their materials, processing, and use cases. In this research, thin film capacitors on LTCC involved multiple material sets including evaluations of Ag, Al, Au, Cu, and Pt electrodes, Al_2O_3 dielectric films as well as Ti and Cr adhesion layers and oxide variants of these metals within circuit traces. The performance of these materials was evaluated relative to various configurations of capacitors and MCMs.

1.2.1. Capacitors and Dielectrics. Capacitors are found within almost every modern electronic system. Metal oxide (ceramic) dielectrics are suitable materials for capacitors due to advantageous dielectric properties including a variable and high dielectric constant (from three up to thousands or tens of thousands), low dielectric loss (< 0.01), and high dielectric strength (typically $\geq 10^5$ V/cm) [1]. Recognizing these properties all vary with frequency, electric field, and temperature, designers often develop new materials optimized for specific applications.

Ceramic dielectrics can behave linearly or non-linearly with respect to frequency, electric field, and temperature depending on their structure and chemical composition. This work characterized dielectric thin film materials that behaved both linearly and non-linearly. In some cases, materials that were expected to behave linearly based on their composition and crystal structure behaved non-linearly. This work explores the behavior of these materials for a wide range of DC and RF (MHz+) applications where different dielectric classes are suitable, to better understand the relationships between the processing, structure, properties, and performance of the capacitors.

In their simplest form, fundamentally, capacitors can be described as a dielectric between two parallel plate electrodes, i.e. a metal-insulator-metal (MIM) configuration. The capacitors can be combined in a series or parallel configuration to increase or decrease the overall capacitance of the device. The relationship that determines the performance of a capacitor is shown in Eq. 1

$$C = \frac{\epsilon_0 \epsilon_r A}{d} \qquad (1)$$

where C is capacitance, ϵ_0 is the permittivity of free space (8.85 x 10^{-12} F/m), ϵ_r is the relative permittivity or effective dielectric constant of the material, A is the active area of the dielectric between the electrodes, and d is the thickness of the dielectric.

Using the basic relationships in Eq. 1, researchers and manufacturers have worked to maximize capacitance while minimizing the form factor by developing ever higher dielectric constant materials while simultaneously making the dielectric thinner. The present research desires to also take advantage of that fundamental relationship through the alternate fabrication method of thin film deposition that enables integration of the capacitor directly onto or into the substrate, PWB, or MCM. This is driven from the desire to reduce form factor, increase integration, tailor properties and performance, and protect from supply chain volatility.

Thin film deposition enables a sub-micron dielectric thickness and tailorable form factor devices. Thin films can be deposited directly onto the ceramic or glass substrate, increasing integration and eliminating solder joints, thereby eliminating a potential and common failure mode related to solder. The thin film devices can also be positioned so that parasitics, such as inductance, are reduced in the overall circuit, further increasing device performance [2]. Lastly, the thin film devices can be manufactured in-house, lowering the exposure to supply chain volatility for passive devices as has been experienced multiple times over the past three decades [3-8]. A contributing factor to the desire to develop devices in-house to avoid supply chain volatility is that in recent years, demand for MLCCs has increased dramatically, driven in part by the increased use of electronics within the automotive market, as can be seen in Figure 1.1.

Additional considerations include temperature and frequency stability for selection of a dielectric for RF applications [9]. Dielectric constant is impacted dramatically by frequency, atomic structure, and composition. Amorphous thin films are expected to have much lower dielectric constants in general due to the absence of dipolar polarization.

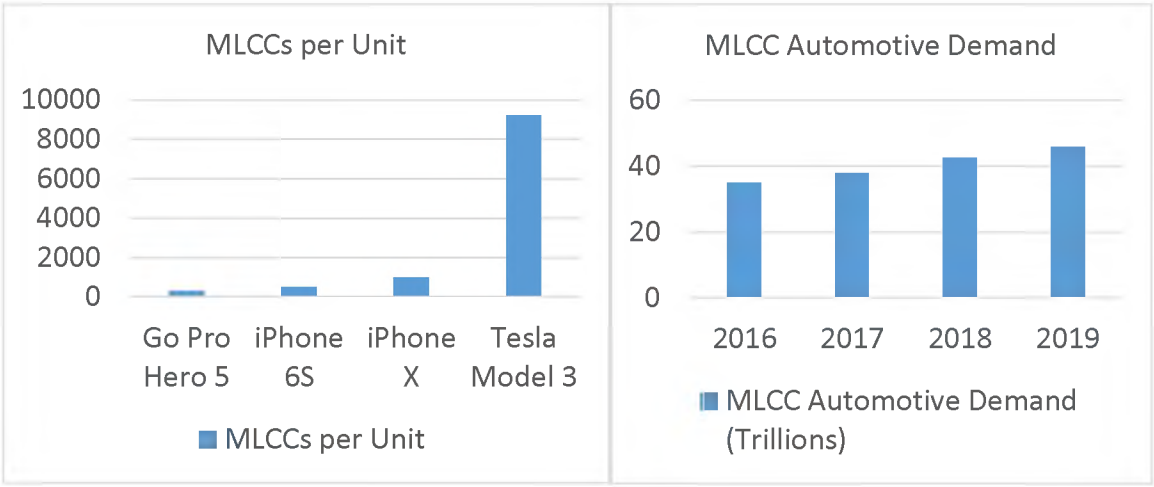

Figure 1.1: Relative quantity of MLCCs by application (left) [10] and demand within the automotive market (right). [11]

1.2.2. Thin Films and LTCC. Thin films on ceramic and glass substrates have offered compelling solutions for many electronic interconnect and packaging challenges for decades [12]. On the other hand, thin films have their own challenges that have limited broader application [13]. This research explores the state-of-the art for thin films on ceramic and glass substrates for interconnects and capacitors, addresses adhesion studies, and the processing, structure, properties, and performance of thin film capacitors with the potential to address prior challenges. Three areas of focus are film adhesion,

surface roughness and coatings, and electrode effects on device performance and reliability. Low temperature cofired ceramic (LTCC) has been a useful substrate material for more than 30 years in the microelectronics industry. LTCC have high reliability, high performance, and can be used for specialty applications and for multichip module (MCM) substrates [14, 15]. More recently, new glass substrate formulations have emerged for similar applications when used with thin films for multilayer interconnects [16]. The studies in this work evaluate thin films primarily on LTCC, but also describe some examples of capacitors on glass.

LTCC was designed to be compatible with thick film printing methods to pattern internal and external metallizations for circuit patterns. [17] In addition to metallizations, LTCC materials include resistor, dielectric, and ferrite thick film inks that can be used to create integrated passive devices such as resitors, capacitors, and inductors as shown in Figure 1.2 (left). [18-21] In order to overcome challenges of thick film dimensional limitations for LTCC, Wolf, et al. developed a thin film metallization system capable of finer lines and spaces (Figure 1.2, right) and compatible with LTCC. [22] Goals of developing a thin film metallization system for LTCC included maintaining the ability to have solderable surfaces as well as improving wire bonding since LTCC MCMs use chip-and-wire where ICs are directly bonded to the LTCC surface and wire bonded to the circuit pattern to complete the interconnections of the IC to the MCM. This is in contrast to packaged ICs that are encapsulated in an epoxy, ceramic, or metal package and require additional surface area in the MCM as compared with chip-and-wire.

Thin films on LTCC are not as mature as thick films and the LTCC was not originally engineered with this in mind. One of the challenges that the separate

development of LTCC and thin films on LTCC created is related to the dimensional predictability of the sintered LTCC. LTCC begins as unfired, flexible layers that are intended to be patterned primarily prior to firing. The firing process results in the LTCC densifying and reducing in X, Y, and Z-dimensions with a final size that is dependent on the metallization loading. [23] Since thin films are applied to the LTCC surface after firing and each MCM varies by 400 µm or more across a 12 cm x 12 cm substrate, alignment of the this films to the underlying LTCC features is one of the more substantial challenges. In the present research adhesion of the thin films on the as-fired surfaces and the performance of thin film capacitors are the major considerations.

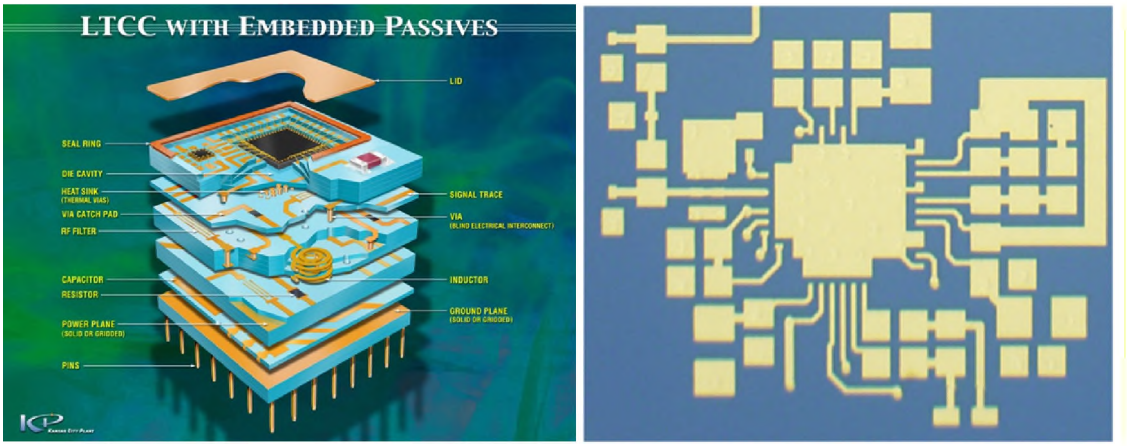

Figure 1.2: (left) Exploded view of an MCM-C with surface mount and embedded passive components. (right) Thin film pattern definition on LTCC. ©Copyright Honeywell Federal Manufacturing & Technologies LLC, 2019

1.2.3. Adhesion Studies and Issues. Adhesion of the thin films on the as-fired LTCC surface was determined to be one of the issues that required increased understanding in order to predict the long-term reliability of the LTCC MCMs. While there is a fundamental understanding of glass adhesion to metal surfaces [24], there has

been less focus on understanding adhesion of thin metal films on the ceramic-filled glass LTCC substrate surfaces. Specifically, an understanding of the mechanisms that underpin adhesion of thin films on LTCC was needed in order to develop improved reliability of this technology.

Thin films on ceramic and glass substrates is an existing technology that provides a starting point for understanding thin film adhesion on LTCC. Early work by Benjamin et al. noted that thin film adhesion had largely been neglected up to that point and that there were conflicting theories on the mechanism of adhesion. They proposed that oxygen atoms acted as a bridge between the deposited metal film and the glass substrate [25]. Their study revealed different levels of adhesion for metal films deposited on the glass, with adhesion being highest for oxygen-active metals such as Ti, Cr, Fe, and Ni.

The present research used physics-based computer modeling to calculate the total energy of the thin film metal on LTCC through a simplified representation of the LTCC. This modeling was based on the true work of adhesion (W_A) that was proposed by Volinsky, et al. and represented by the following equation:

$$W_A = \gamma_f + \gamma_s - \gamma_{fs} \qquad (2)$$

where γ_f, γ_s, and γ_{fs} are the specific surface energies of the film, substrate, and interface, respectively. [26] The total energy of the system can be represented by the following equation:

$$\Delta E = E_{total} - (E_f + E_s) \qquad (3)$$

where E_f and E_s are the potential energies of the film and substrate, respectively. This allowed the total system to be modeled and values for film and substrate energies calculated as representative of the adhesion of the system.

1.2.4. Metallization Behavior and Issues. The effect of various electrode materials on the performance of thin film capacitors has also been investigated. Many thin film MIM capacitor systems have been characterized in multiple configurations, materials systems, and on a variety of substrates. Thin film capacitors can exhibit non-linear conduction behavior with respect to fields and frequencies. The impact of the band energies of the electrode and dielectric materials has been noted as contributing to capacitor conductivity and performance. [27, 28] In these studies, Schottky emission has been proposed as the mechanism for conduction, as described in Eq. 4

$$J = AT^2 exp\left[\frac{\frac{1}{2}E^{\frac{1}{2}} - \emptyset}{kT}\right] \qquad (4)$$

where, J is current density, A is the Richardson constant, E is the applied electric field, $\emptyset$ is the barrier potential, k is the Boltzmann constant, and T is temperature.

Other possible conduction mechanisms include space charge limited current (Eq. 5) and Fowler-Nordheim tunneling (Eq. 6), with both of these mechanisms being temperature independent.

$$J = \frac{9}{8} K \epsilon_0 \mu \frac{V^2}{t^3} \qquad (5)$$

$$J = \frac{A}{\emptyset} E^2 exp\left[\frac{-B\emptyset^{\frac{3}{2}}}{E}\right] \qquad (6)$$

Here K is the dielectric constant, ϵ_0 the permittivity of free space, μ is the mobility, V is the voltage, t the dielectric thickness, and B is a constant. The dependence of current density on field allows for the determination of the physical mechanism contributing to conduction. In the present study, the various electrode metallization/dielectric

combinations were evaluated to determine the primary mechanisms contributing to conduction and capacitor performance.

One scenario related to this non-linear conduction behavior is described in Figure 1.3. In this diagram, the work function of the dielectric is greater than that of the metal, resulting in electron transfer and the formation of an accumulation layer in the dielectric. This is an ohmic contact. If an accumulation layer forms in a typical capacitor dielectric where the dielectric has a thickness on the order of many microns, the accumulation layer is so small relative to the insulator that it is not noticed. This may not be the case for thin film dielectrics where the overall thickness is on the order of 1 micron or less. In some cases, the accumulation layers could be large enough relative to the dielectric thickness that they actually overlap, leading to failure of the capacitor.

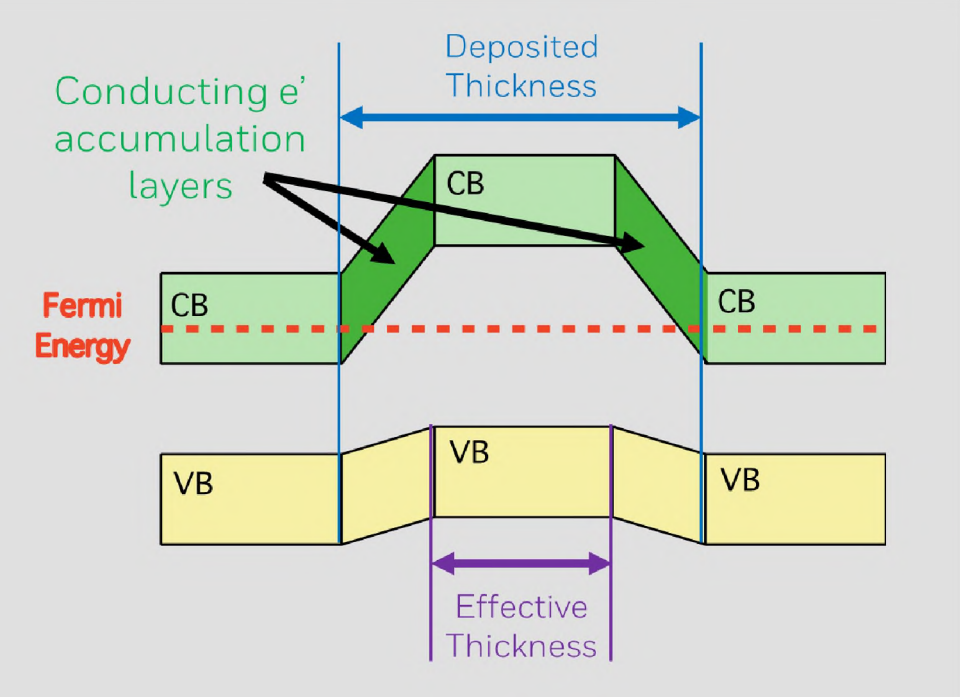

Figure 1.3: Band bending due to Fermi level equilibration

1.2.5. Fringe Field Effects. The third area of interest is the interaction of the size of devices with fringe fields created at electrode edges and the impact of dielectric properties on those fringe fields. MIM capacitors are expected to behave according to Eq. 1, however device geometries may result in a capacitance greater than that predicted by this equation. Subramanian, et al. observed empirically that an edge correction calculation described by Eq. 7 can account for the capacitance contribution at the edge, C_e (units of pF), which scales in proportion to the ratio of the capacitor perimeter, P, and thickness, t. [29] This applies to circular, parallel plate capacitors with areas in the range of devices considered in this research (~300 μm diameter for the smallest devices studied Subramanian, et al.).

$$C_e = [0.019 \ln(P/t) - 0.043]P \qquad (7)$$

The increase in observed capacitance over the expected capacitance results in a larger dielectric constant than expected from Eq. 1. The calculated dielectric constant in this research scaled inversely with the capacitor area, which agrees with the empirically derived Eq. 7, however the similarities end there. The present research found larger increases in measured dielectric constants than were calculated from this empirical relationship as the device size decreased.

Advanced electromagnetic modeling tools are available now that can be used to understand the expected contribution of fringe fields on devices as the edge dimensions decrease, and that take into account additional geometric factors such as tapering of electrodes that can further increase capacitance.

1.2.6. Other Process, Material, and Design Considerations. Additional process, material, and design factors that contribute to the reliability of MCMs. The

substrate surface roughness, material interactions related to solder joints, and electromagnetic isolation between components within an MCM are all important to long term reliability. The following sections review these additional factors and introduce some of the work that was carried out, but not included within this dissertation, as well as related works to the overall topic of MCM and thin film reliability during the dissertation research period or prior to this research effort.

1.2.6.1. Substrate surface conditions. Another area of interest is the interaction of the substrate or surface condition/roughness on capacitor performance and yield. It has been noted that the surface roughness of LTCC is generally much greater than the thickness of the films used in thin film MIM capacitors and thus can be a limiting factor in the application of thin films on LTCC. [30, 31] To overcome this limitation, multiple approaches have been evaluated to reduce LTCC surface roughness. Mechanical polishing, dip coating a sol gel material, and thick film printing a glass encapsulant are some of the approaches documented for smoothing the surface of LTCC to make it more suitable for thin film devices that are sensitive to surface roughness. [32, 33]

Size, weight, and power (SWaP) considerations drive designers in their selection of substrate technology for multichip modules. Low Temperature Cofired Ceramic (LTCC) has size and performance benefits, particularly for RF applications where there are specific LTCC systems with tailored properties. The DuPont 9K7 is one such system [34]. Previous work within this research group documented low yields in PVD thin film capacitors on DuPont 951 and DuPont 9K7 substrates. Yields ranged from 0% up to 96% depending on the combination of substrate, dielectric, and electrode materials. From those previous studies, the 9K7 devices had lower overall yields than devices on 951.

This was attributed in part to a different surface finish and an approach was developed to mitigate the effect of surface finish by applying a surface coating to the 9K7 in order to develop an LTCC substrate with a lower surface roughness than the as fired substrate material. As a result, higher capacitor yields were obtained on these substrates.

1.2.6.2. Thermomechanical design improvements enabled by thin films. LTCC is a versatile packaging technolog, and this versatility is in part related to its thermomechanical properties such as having a coefficient of thermal expansion (CTE) similar to that of silicon, used for the integrated circuits (ICs). The relatively close CTE between LTCC and ICs result in low residual stress and low thermally induced stress during thermal cycling of MCMs throughout their lifecycle. Every constituent of LTCC systems has been co-developed to minimize CTE mismatches while optimizing the processing parameters and electrical performance. Still, processing, materials, and designs are limited by the presence of discontinuities when a high level of electromagnetic isolation (EMI) is required.

Combination of three-dimensional structures with thin film metallizations have been created that alleviate the thermomechanical stress at the interfaces between large EMI components in MCMs. The first structure was developed to overcome process and material limitations of the LTCC system to create a highly isolating Faraday shield in RF MCMs. The original concept utilized full tape thickness features (FTTFs) [35-37] in the top one or two layers of the LTCC that were filled with via fill conductor. The via fill conductor is a composite of an Au alloy and ceramic filler that sinters at a rate similar enough to the ceramic layers to minimize the formation of residual stresses when the via fill diameters are on the order of the thickness of a single layer of LTCC.

A modification to the FTTFs has been proposed and implemented that created an open channel in a laminated, unfired LTCC stack. This approach was previously not disclosed in the literature. The open channel was coated with the multi-layer, multi-function thin film composition, as described in Paper I, after the LTCC was cofired. Multiphysics modeling of the thermomechanical stress was performed to study the stress reduction in the solder joint of the LTCC substrate-to-metal seal frame and lid, compared to those that develop in a traditional surface mount configuration on a FTTF Faraday slot. This work was presented and published in the Proceedings of the 2011 International Symposium on Microelectronics prior to the author's acceptance into the PhD program at Missouri S&T. [38] The models confirmed a reduction of residual stress in the solder joint that correlated with observed improvement in solder joint reliability.

A further enhancement to the MCM/LTCC system was later proposed which consisted of replacing the metal seal frame and lid with an LTCC single piece, integrated seal frame and lid component with thin film coating for EMI shielding and solder functionality. The concept was reduced to practice with a prototype single piece, LTCC seal frame and lid. This LTCC component was integrated into the model architecture developed for the study presented and modeled to evaluate if further stress reduction could be realized in the solder joint and system with this concept. [38] The study was published in the *Journal of Ceramic Science and Technology*, **2015**, Vol. 6, No. 4, pp. 261-266 after being accepted into the PhD program at Missouri S&T. [39]. Furthermore, the novel concept of a monolithic LTCC seal frame and lid component was patented in 2016. [40]

The combination of thin films and novel LTCC structures has been impactful to the microelectronics assembly and packaging industry with research continuing by others as well as many of these innovations being implemented into use.

PAPER

I. THERMODYNAMIC ANALYSIS OF PHYSICAL VAPOR DEPOSITED INORGANIC THIN FILMS ON LOW TEMPERATURE COFIRED CERAMIC

Carol Putman, Rachel Cramm Horn, J. Ambrose Wolf, and Daniel Krueger*
DOE's National Security Campus, 14520 Botts Road, Kansas City,
Missouri 64147

*Corresponding author; email: dkrueger@kcp.com

ABSTRACT

Low temperature cofired ceramic (LTCC) has been established as an excellent packaging technology for high-reliability, high-density microelectronics. The functionality and robustness of rework have been increased through the incorporation of a physical vapor deposition (PVD) thin film Ti/Cu/Pt/Au metallization. PVD metallization is suitable for radio frequency (RF) applications as well as digital systems. Adhesion of the Ti "adhesion layer" to the LTCC as-fired surface is not well understood. Although previous work has established extrinsic parameters for delamination mechanisms of thin films on LTCC substrates, there is incomplete information regarding the intrinsic (i.e., thermodynamic) parameters in the literature. This article analyzes the thermodynamic favorability of adhesion between Ti, Cr, and their oxide coatings on LTCC (assumed as amorphous silica glass and Al_2O_3). Computational molecular calculations are used to determine interface energy as an indication of molecular stability between pair of materials at specific temperature. The end result will expand the understanding of thin

film adhesion to LTCC surfaces and assist in increasing the long-term reliability of the interface bonding on RF microelectronic layers.

1. INTRODUCTION

Low temperature cofired ceramic (LTCC) technology is a substrate technology of choice for multichip modules (MCMs) exposed to high-temperature and extreme environments and requiring high reliability. MCMs consist of a substrate (LTCC in this study) with insulator and conductor layers that provide interconnects to integrated circuits and passive surface mount components such as capacitors, resistors, and inductors (Figure 1, left). Ceramic multichip modules (MCM-Cs; Figure 1, left) have been utilized in high-speed, high-reliability, and high density microelectronics for more than 30 y [1]. LTCC permits the use of high-conductivity internal metallization for improved high-speed digital and high-frequency circuit performance. Wolf et al. have developed a thin film metallization system compatible with LTCC, which extends the high-frequency performance and robustness of MCM-Cs [2]. The thin film metallization increases the solder reworkability and also the wire bonding strengths of the LTCC compared to the traditional thick film metallizations.

The use of thin film metallization also presents certain challenges to fabrication and characterization of LTCC reliability. Thin films are deposited using physical vapor deposition (PVD) onto the fired LTCC to create the outer surface circuit definition as shown in the right of Figure 1. The outer surface circuit is defined by a glass photomask with fixed pattern dimensions. The LTCC final dimensions can vary due to the shrinkage

that occurs during the cofiring process. These two conditions of fixed thin film circuit dimensions and varying LTCC final size make alignment between the target features on the LTCC and the circuit features of the thin film challenging. Another challenge resulting from the use of thin films is the characterization of adhesion strength to the LTCC for understanding long-term reliability and quality control standards.

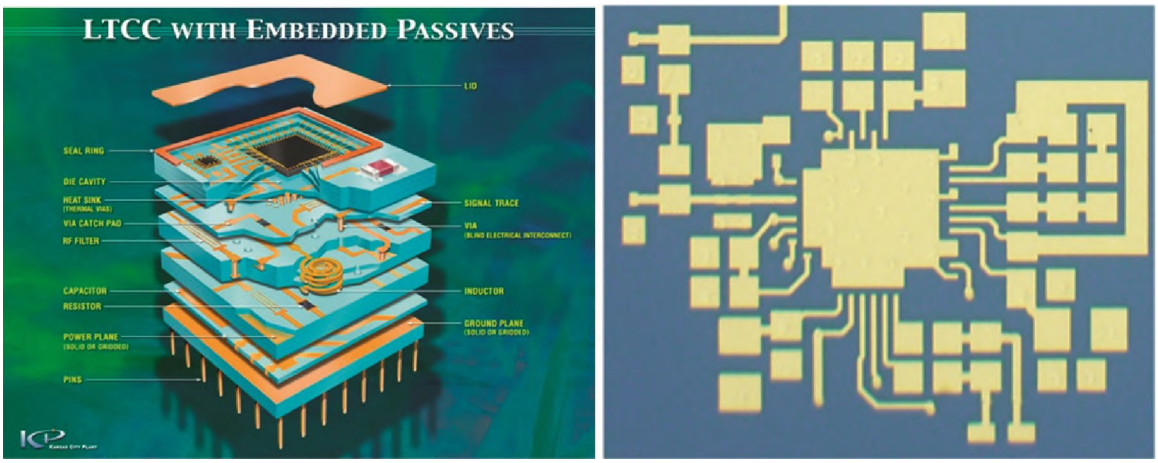

Figure 1: (Left) Exploded view of an MCM-C with surface mount and embedded passive components. (Right) Thin film pattern definition on LTCC.

The use of thin films on ceramic and glass substrates has been prolific for decades; however, the understanding of the adhesion mechanisms and characteristics has not been advanced significantly since early work explored this topic. Benjamin et al. noted at the time of their publication that this topic had largely been neglected as well and that there were conflicting theories on the mechanism of adhesion. They proposed that oxygen atoms acted as a bridge between the deposited metal film and the glass substrate [3]. Their study revealed different levels of adhesion for different metals deposited on the glass, with adhesion being the highest for oxygen-active metals such as Ti, Cr, Fe, and Ni.

Other researchers have studied the interfacial toughness measurements of such systems related to microelectronics and reported their results acknowledging the role of thermodynamics in adhesion, but without exploring the thermodynamic models [4]. In their work, the true work of adhesion (W_A) is proposed to be represented by the following equation:

$$W_A = \gamma_f + \gamma_s - \gamma_{fs} \qquad (1)$$

where γ_f, γ_s, and γ_{fs} are the specific surface energies of the film, substrate, and interface, respectively. The total energy of the system can be represented by the following equation:

$$\Delta E = E_{Total} - \left(E_f + E_s\right) \qquad (2)$$

where E_f and E_s are the potential energies of the film and substrate, respectively.

The primary goal of this work is to understand the favorability or lack thereof, for adhesion of thin film Ti, Ti_2O_3, or TiO_2 and Cr or Cr_2O_3 on LTCC through the use of quantum mechanics (QM) and molecular dynamics (MD) by analyzing the interfacial energies of these systems.

2. MODELING AND CALCULATIONS

Development of MCM-Cs at Honeywell has resulted in a thin film on LTCC system as reported previously by Wolf et al., which serves as the base system in this study [5]. The LTCC substrate material is a Ca, Mg, K, Na, Pb-containing alumino-borosilicate glass with Al_2O_3 particles. The thin film metal is a multifunction, multilayer system deposited by electron-beam-evaporative PVD. The multilayer thin film consists of

a Ti “adhesion” layer, Cu layer for radio frequency performance, Pt layer for solder connection and leach protection, and Au cover layer for wire bonding (Figure 2). The complexity of this material system and metal film configuration has necessitated the simplification of modeling and calculations in the context of this study. The LTCC interface models have been built as SiO_2 and Al_2O_3 substrates in conjunction with different metal or metal oxide coatings stacked on the top, thus, Ti, TiO_2, Ti_2O_3, Cr, and Cr_2O_3. In this study, metal oxides are compared to the pure elements to determine thermodynamic energy stabilities, with the purpose of driving processing conditions to the most favorable adhesion case. A schematic representing the thermodynamic system of LTCC during PVD is shown in Figure 3 that includes a 2 phase substrate consisting of amorphous silica and Al_2O_3, thin film metallization, and metal atoms in a vacuum.

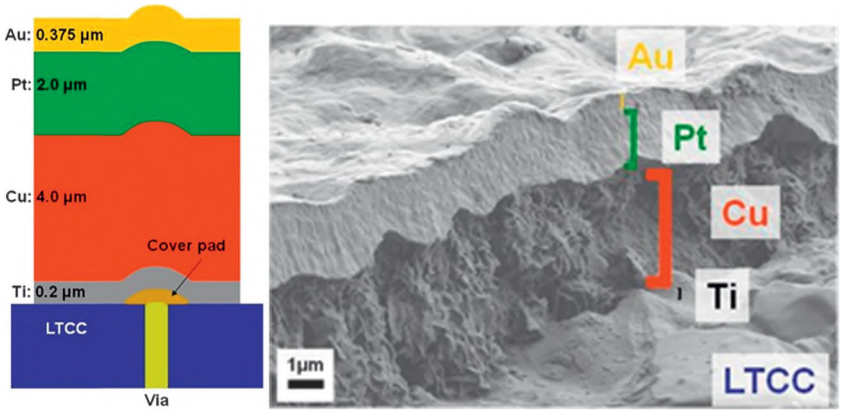

Figure 2: (Left) Schematic cross section of thin film layers covering a thick film cover pad on a typical LTCC substrate. (Right) Ion-beam milled edge of multifunction, multilayer thin film on LTCC imaged in scanning electron microscope.

Two different molecular computational methods were explored in this work: an MD approach and a QM approach.

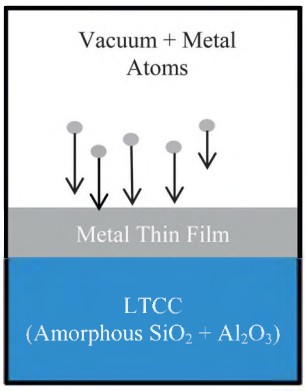

Figure 3: Thermodynamic representation of LTCC/thin film system.

2.1. MD APPROACH

Despite the reduced computational expense of the MD approach, the difficulty of finding accurate force fields for pure metals restricted this methodology to only the case of Ti_2O_3 as the thin film layer on LTCC substrates, considering temperature effects. The total energy was calculated for cells of crystalline silica (quartz) and titanium oxide III (Ti_2O_3), as well as alumina (Al_2O_3) and titanium oxide III (Ti_2O_3) at temperatures 300, 600, and 900 K. Schematic representations of the MD models are shown in Figure 4 as well as the converging energy curves for each case in Figure 5. Interface energy is measured in megajoules/mole and refers to the converging energy as the structure approaches a more stable configuration. Therefore, when comparing energies between cases, the lowest energy value indicates the more favorable thermodynamic combination of substrate and thin film layer, which would be expected to have better reliability in terms of interface adhesion.

From the MD approach, it can be seen from Figure 5 that alumina will have a favored stability with titanium oxide III (Ti_2O_3). Temperature proved to have minor impact on these results. The interaction between this specific combinations of materials is

later confirmed through the QM approach when considering titanium and the different forms of titanium oxides (II and III) on both substrates.

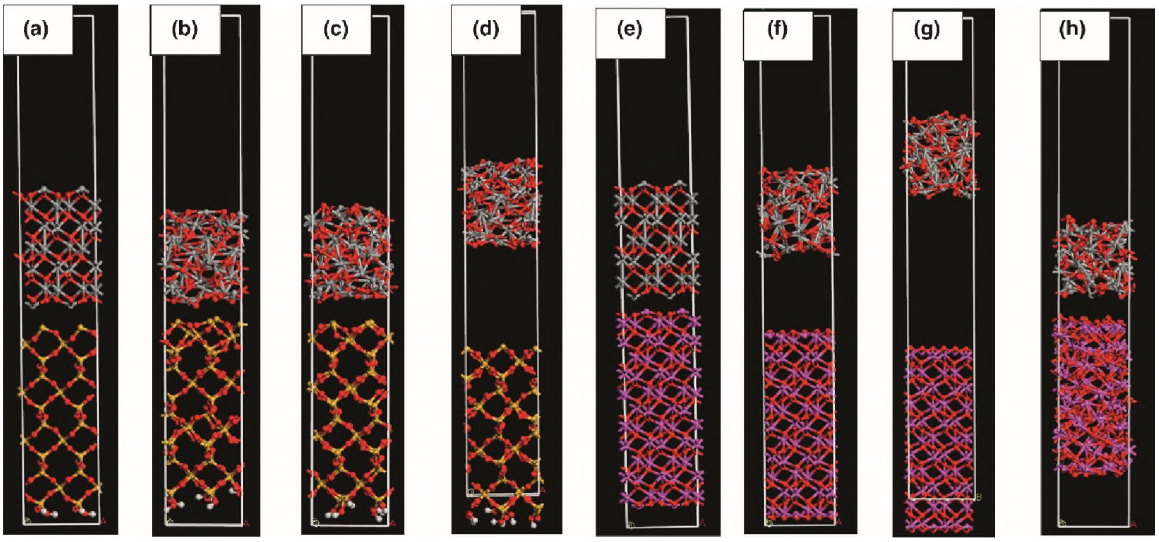

Figure 4: MD geometry optimization of crystalline models as function of temperature: original structure, 300, 600, and 900 K, for (a-d) silica/Ti_2O_3 and (e-h) alumina/Ti_2O_3 systems.

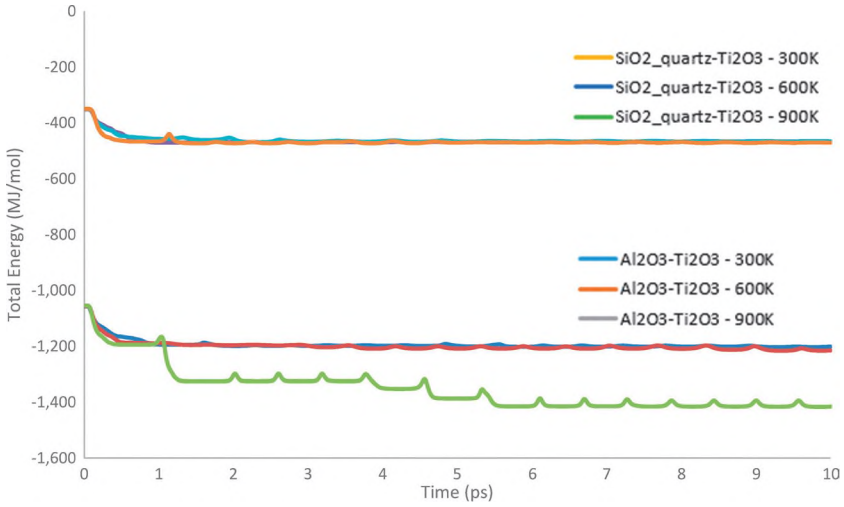

Figure 5: Converging energy over time for the interaction between a Ti_2O_3 thin film on silica and alumina substrates as function of temperature using the MD approach.

2.2. QM APPROACH

Because of the limitations of MD when simulating metals, a second approach utilized QM, despite its increased computational expense. Thus, on average, each case of QM took 96 h to converge versus 2 h using MD on 16 processor cores.

QM proved the most thorough and reliable approach to quantify differences between Cr and Ti and their oxides on both substrates, amorphous SiO_2 and Al_2O_3. Ti and Cr were suggested as candidates to improve adhesion, but concerns about processing conditions led to an evaluation of the effect of their oxides at the interface. For this approach, 10 cases were built and optimized using QM to determine total energy as an indicator of stability of the interface between amorphous silica (SiO_2) and alumina (Al_2O_3) substrates with thin films of titanium (Ti), chromium (Cr), and their oxides (TiO_2, Ti_2O_3, and Cr_2O_3) as shown in Figure 6.

Table 1 shows the most favorable combination at the top (lowest energy, more thermodynamically stable) and the least favorable combination at the bottom (highest energy). All energy calculations were done using CASTEP, a QM method in Materials Studio 8.0 (BIOVIA, San Diego, CA) that employs density functional theory (DFT) with a plane-wave basis set [6]. This allowed for exploration of the properties of crystals and surfaces in solid state materials.

The following steps were taken to model and simulate the interface interaction:

1. Construction of the crystal structure of the thin film material.
2. Determination of lattice parameters for minimum interface area.
3. Construction of the crystal structure of the alumina substrate, or building amorphous silica to the same interfacial cell size.

4. Stacking layers for surface-to-surface interaction.

5. Running geometry optimization using CASTEP (QM method).

6. Normalization of energy by interface area.

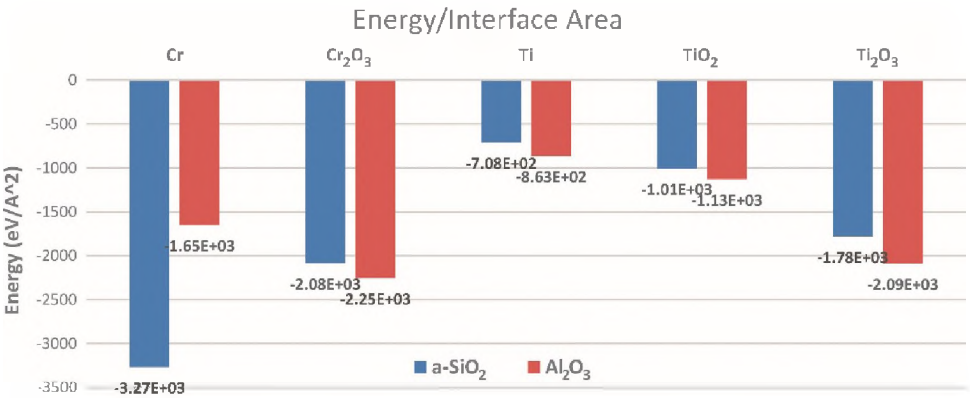

Figure 6: Converging energy for interfaces of silica substrate and alumina substrate with titanium, chromium, and their oxides using QM approach.

Table 1: Interface Energy for LTCC Main Components and Interconnect Thin Film Layers

LTCC Interface	Energy/Interface Area (eV/A^2)
SiO_2-Cr	-3.27×10^3
Al_2O_3-Cr_2O_3	-2.25×10^3
Al_2O_3-Ti_2O_3	-2.09×10^3
SiO_2-Cr_2O_3	-2.08×10^3
SiO_2-Ti_2O_3	-1.78×10^3
Al_2O_3-Cr	-1.65×10^3
Al_2O_3-TiO_2	-1.13×10^3
SiO_2-TiO_2	-1.01×10^3
Al_2O_3-Ti	-8.63×10^2
SiO_2-Ti	-7.08×10^2

Most Favorable Combination

Thermodynamically Least Favorable Combination

Unit cell type, lattice parameters, and cell size were particular to each interface case, thus normalization of energy was required as a final step to compare cases. Figures

7 and 8 show the molecular models built for amorphous silica and alumina in combination with titanium, chromium, and their possible oxides.

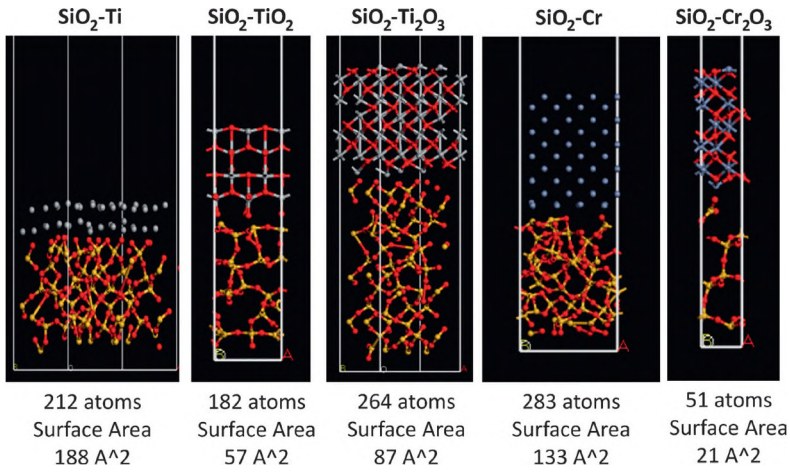

Figure 7: Molecular models for QM to calculate interface energy for amorphous silica substrate and various thin film coatings.

The data suggest that the crystal structure plays a role in the time required for the model to reach a converged minimum level of energy. Compatibility of crystal structures, as between hexagonal-close-packed (HCP) Al_2O_3 and HCP titanium, took less time to converge during the geometry optimization. On the other hand, all cases with amorphous silica took longer to converge. The time required to reach convergence during geometric optimization could also be an indication of compatibility between layers, suggesting that layers between components with similar crystalline structures will have better reliability and less probability for defect formation since atoms can settle into natural positions. Figure 9 shows the crystal systems of each coating and substrate used to build the molecular models.

To agree with the type of silica in the LTCC, amorphous silica was built in a consistent manner for all cases via the following steps (Figure 10).

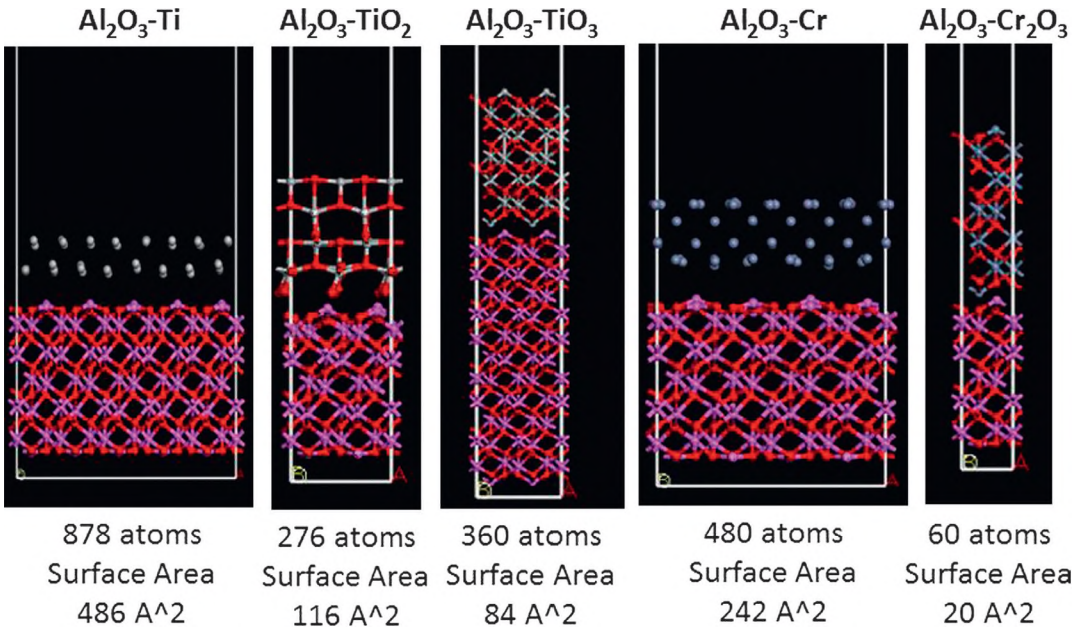

Figure 8: Molecular models for QM to calculate interface energy for alumina substrate and various thin film coatings.

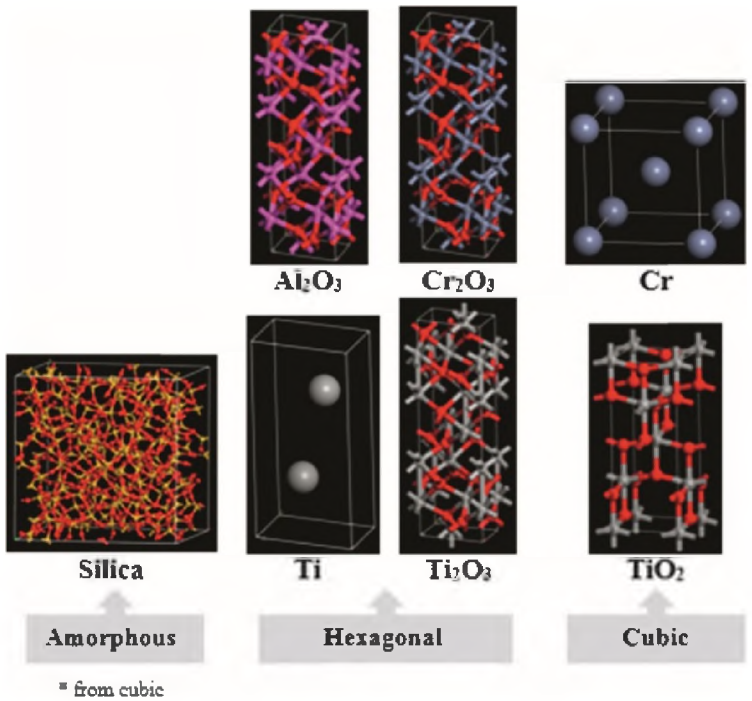

Figure 9: Crystal systems of substrates and coatings used to build QM models. Silica was built to match the crystal system of each individual coating.

1. Create a supercell of the coating material with the desired interfacial area.

2. Create an empty periodic cell with lattice parameters match those of the coating layer along the interface.

3. Create single-atom models of Si and O (or a single-molecule model of SiO2).

4. Use the Amorphous Cell module in Materials Studio to pack the Si and O atoms (or the SiO_2 molecules) into

5. Run geometry optimizations with density-functional-based tight binding method to speed up conversion to final structure, starting with the most coarse tolerances, and then rerunning with tighter tolerances.

6. Run geometry optimizations with DMoL3, a DFT method, to converge to a more accurate amorphous structure, starting with coarse tolerances, and then rerunning with tighter tolerances.

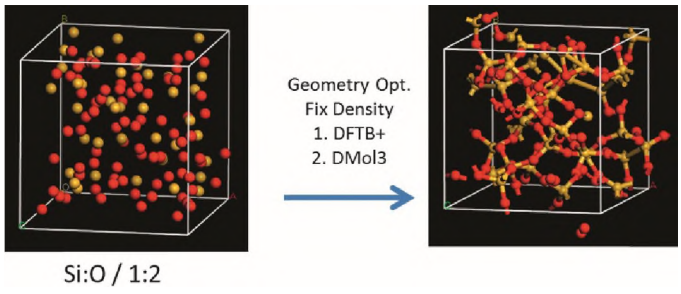

Figure 10: Building amorphous silica.

Once the interface layers were built, CASTEP was utilized for the thermodynamic calculations of total energy for each substrate/coating pair as shown in Figures 7 and 8.

Table 1 shows the final (equilibrated) energies for 10 systems: SiO_2-Ti, SiO_2-TiO_2, SiO_2-Ti_2O_3, SiO_2-Cr, SiO_2-Cr_2O_3, Al_2O_3-Ti, Al_2O_3-TiO_2, Al_2O_3-Ti_2O_3, Al_2O_3-Cr, and Al_2O_3-Cr_2O_3. For all cases, SiO_2 was built as an amorphous solid to better represent the actual LTCC substrate material. Table 2 shows some of the computational parameters used to reach equilibration energy as shown in Figures 11 and 12, where silica and alumina converged to low energy levels with Cr or its oxide rather than with Ti or its oxides. The chromium oxide (Cr_2O_3) coating was found to be the most favorable thin film considering that both substrates (SiO_2, Al_2O_3) are in almost equal composition on the LTCC.

Table 2: QM Parameters for Geometry Optimization

Functional integration method	Generalized gradient approximation/PW91
Convergence tolerances	Energy 0.001 eV/cell Maximum force 100 eV/Å Maximum stress 100 GPa Displacement 100 Å
Energy cutoff	260 eV
points	Coarse

3. CONCLUSIONS

After all runs using the QM approach and based on results shown in Table I and Figure 6, it can be observed that a potential increase in interfacial strength could be achieved when selecting chromium over titanium on silica substrates. This study also demonstrated that if oxidation of a chromium or titanium layer occurs, the formation of those oxides (Cr_2O_3, Ti_2O_3) will increase the stability of the layer in combination with either substrate by ~40%. The oxidation process is something that could possibly be

addressed and controlled by processing parameters during the thin film depositions. For both substrates, the combination with pure Ti leads to the least favorable thermodynamic interaction. Also, for both substrates, titanium and its oxides were always less favorable than Cr and its oxides. Chromium was also shown to exhibit double the stability on a silica substrate as on alumina.

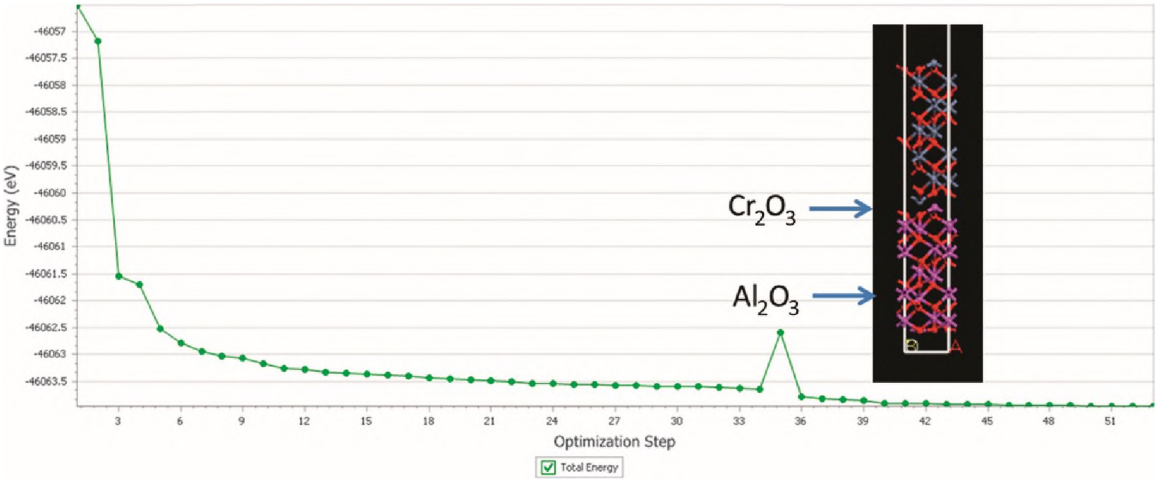

Figure 11: Converging energy for alumina and chromium oxide.

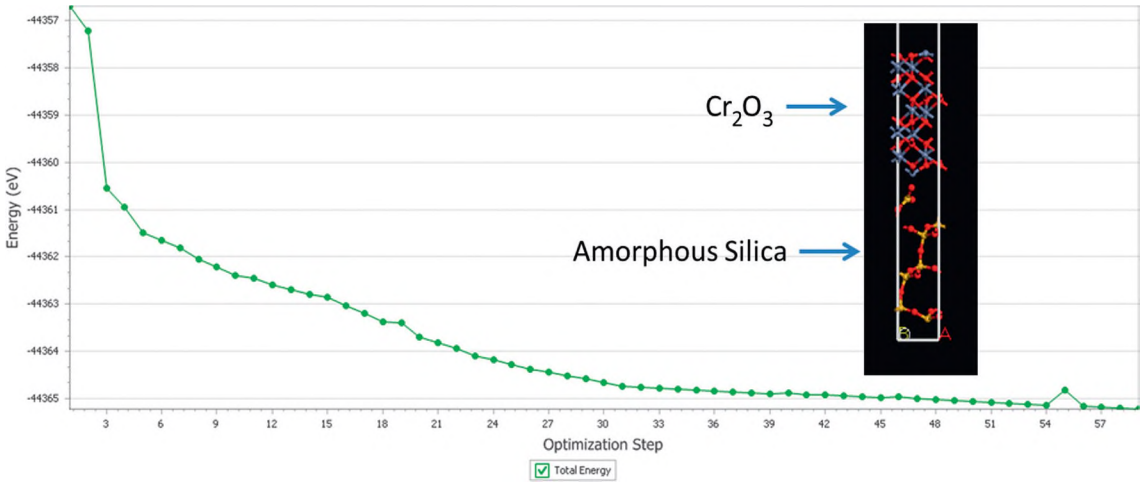

Figure 12: Converging energy for amorphous silica and chromium oxide.

Thus, a higher concentration of silica over alumina in LTCC will be desirable if coating with pure chromium. Preliminary experimental testing has shown results consistent with what is described in this theoretical work, confirming that computational molecular modeling is a valid tool to drive processing decisions and understand materials' performance.

Advanced software with QM and MD algorithms has progressed to the point of predicting thermodynamic properties of some material systems. Using simplified assumptions of the materials of interest, a greater understanding of the thermodynamic mechanism of adhesion was achieved. QM proved to be the best approach to simulate models representing simplified components in the interface interaction of LTCC and thin film layers. Crystalline and amorphous structures, of both pure metals and their oxides, were considered during this work. Chromium on amorphous silica was shown to be the most promising scenario to drive experimentation efforts to improve adhesion strength on LTCC and interconnect layers.

Future work should involve the modeling and simulation of diffusion of elements as a function of temperature and the effect of contaminants at the interface on interface adhesion.

ACKNOWLEDGMENTS

The submitted manuscript has been authored by a contractor of the U.S. Government under contract no. DE-NA-0002839. Accordingly, the U.S. Government

retains a nonexclusive, royalty free license to publish or reproduce the published form of this contribution or allow others to do so for U.S. Government purposes.

REFERENCES

[1] R.G. Pond and W.A. Vitriol, "Custom packaging in a thick-film house using low-temperature cofired multilayer ceramic (LTCC) technology," Proceedings of the 1984 ISHM International Symposium of Microelectronics, pp. 268-271, Dallas, TX, 17-19 September 1984.

[2] J.A. Wolf and K.A. Peterson, "Thin film on LTCC for connectivity and conductivity," Journal of Microelectronics and Electronic Packaging, Vol. 8, No. 2, pp. 43-48, 2011.

[3] P. Benjamin and C. Weaver, "The adhesion of evaporated metal films on glass," Proceedings of the Royal Society of London, Series A, Mathematical and Physical Sciences, Vol. 261, No. 1307, pp. 516-531, 1961.

[4] A.A. Volinsky, N.R. Moody, and W.W. Gerbrich, "Interfacial toughness measurements for thin films on substrates," Acta Materialia, Vol. 50, pp. 441-466, 2002.

[5] J.A. Wolf, K.A. Peterson, P.T. Vianco, M.H. Johnson, and S. Goldammer, "Robustness and versatility of thin films on low temperature cofired ceramic (LTCC)," Proceedings of the 44th IMAPS International Symposium on Microelectronics, pp. 559-565, Long Beach, CA, October 9-13, 2011.

[6] Materials Studio 8.0 Online Help, BIOVIA, San Diego, CA.

II. CONTRIBUTIONS TO DIELECTRIC CONSTANT ENHANCEMENT IN THIN FILM METAL INSULATOR METAL CAPACITORS

Daniel S. Krueger*[1], Zach Legenzoff[1], Ambrose Wolf[1], James Claypool[2], Robert W. Schwartz[2], Wayne Huebner[2]

[1]The Department of Energy's Kansas City National Security Campus, managed by Honeywell – Kansas City, MO

[2]Missouri University of Science and Technology – Rolla, MO

*Corresponding author; email: dkrueger@kcnsc.doe.gov

ABSTRACT

Thin film metal-insulator-metal capacitors were fabricated with varying dielectric and electrode thicknesses and areas. Measurement of the dielectric properties of the capacitors consistently yielded higher than predicted dielectric constants, which prompted the exploration of factors that could enhance the capacitance. Modeling of the fringing capacitance and field enhancement due to the capacitor geometry both yield capacitance gains, albeit insufficient to fully explain the observed behavior. Other contributions to increased device capacitance and apparent dielectric constant are explored as well. Studies of additional dielectric constant enhancement mechanisms beyond those discussed in this paper are in progress.

Keywords — Thin Film Capacitor, Fringe Field Capacitance, Dielectric Enhancement

1. INTRODUCTION

Thin film capacitors fabricated on low temperature cofired ceramic (LTCC) substrates are of interest for reducing the number of solder joints and discrete components for high density multichip modules (MCMs) and incorporation into glass interposers. [1] [2] In this work, thin film metal-insulator-metal capacitors have been developed with varying electrode and dielectric compositions for frequencies up to 15 MHz. The capacitors also have varying thickness and area in order to achieve specified capacitance values between 10 pF and 10 nF. Dielectric materials were selected for their stable and predictable dielectric constant and high breakdown strengths that allow operation of thin devices at fields approaching 1 x 10^6 V/cm.

While the overall research included a larger set of materials, the dielectric utilized in this study is Al_2O_3. Polycrystalline Al_2O_3 is a linear dielectric with a dielectric constant of ~9.8. Combined with its electrical resistivity $>10^{12}$ Ω cm, Al_2O_3 is desirable for capacitor applications that are exposed to elevated temperatures and voltage. In thin film form, capacitance values of interest can be achieved with dielectric constants ≤ 10, making these materials suitable choices for this development effort.

However, nearly all experimental samples exhibited higher than predicted, or enhanced, capacitance values. Potential contributions to the enhanced capacitance include fringe effect capacitance, polarizability changes due to the amorphous structure of the materials, and accumulation or depletion layers in the dielectric layers, resulting in effective thinner dielectric layers. These contributions have been studied individually and previously have been thought to be a minor contribution and therefore of little use to

consider for devices of the size and capacitance studies here. However, as the operational frequencies of capacitors have increased to 50-100 GHz and beyond, these contributions can minimize insertion losses and therefore their usefulness has increased. [2] Understanding the contributions to the apparent enhancement of dielectric constant may facilitate more accurate predictive models of such devices in new higher frequency applications.

For a dielectric under bias, the electric field lines extend beyond the geometry of the electrodes through the surrounding medium, be that air or an encapsulant. The relative magnitude of this contribution will depend upon the dielectric constant, K, of the dielectric and the surrounding medium, the geometry of the electrode edge, and the overall size of the capacitor, i.e., smaller capacitors exhibit a larger fringe effect. In this work the fringe field capacitance was calculated using 3D electromagnetic analysis software by applying physics-based calculations. Others have studied and developed empirically derived calculations to apply to capacitors based on an edge effect that approximates the enhancement due to the fringe field. [4]

Thin film dielectrics are typically amorphous, and as such, can certainly exhibit dielectric constants significantly different from crystalline systems. Intuitively the lower density of an amorphous system would lead to a lower K, yet that makes the assumption that the ionic polarizability is constant. The open structure of an amorphous system could lead to higher ionic displacements under field application. Polarizability contributions are also evaluated in this work. The dielectric polarizability, consisting of both ionic and electronic polarizabilities, has long been estimated for crystalline materials using the Clausius-Mossotti equation. There has also been prior work that has studied the

effect of crystalline versus amorphous structures on the dielectric polarizability of compositionally identical dielectrics. This work suggests that structure may impact polarizability. [5]

Another potential contributor to dielectric constant enhancement is the formation of semiconducting accumulation, depletion, or inversion layers within the dielectric immediately adjacent to the electrode. In the world of semiconductors, it is well known that these layers form due to differences in the work function. Accumulation or inversion layers would reduce the effective dielectric thickness, leading to an increased capacitance, and a higher apparent dielectric constant. Accumulation or depletion layer formation in these devices is the focus of future work and will not be included in the analysis here. Discussion of TiO_2 and $SrTiO_3$ capacitor devices will also be presented in later papers.

2. CAPACITOR FABRICATION AND CHARACTERIZATION

A series of capacitors was fabricated and studied using various dielectric, electrode, and substrate compositions and dimensions. These capacitors were characterized and then compared with the contributions to dielectric constant enhancement from fringe and edge effects, as well as polarizability enhancement due to crystalline versus amorphous phase differences.

Each substrate consisted of 48 capacitors of varying top and bottom electrode dimensions. The dielectric thickness was varied between substrates and there was thickness variation within substrates due to process effects. The electrode and dielectric

layer deposition was performed under an Ar backfill. Physical masks were used to define the sample geometries, which led to some shadowing at the edges. Nominal physical mask dimensions and experimentally measured device geometries were the basis for the model geometry used in the calculations later. Vacuum was broken between layers in order to change masks and no reactive back sputtering was used between layers. The lack of reactive back sputtering may have led to oxide layer formation on some electrodes prior to dielectric deposition. Layers consisted of a bottom metal electrode of 500nm thickness, Al_2O_3 dielectric of 1000nm thickness, and a top metal electrode of 500nm thickness. Metal electrode layers were deposited from 99.99% pure metal targets at 300 W using a DC magnetron power supply. The Al_2O_3 dielectric was deposited from a 99.9% pure ceramic target at 200 W using an RF power supply. All materials were deposited with a Denton (Moorestown, NJ) Discovery 18 sputter deposition system using an atmosphere of 99.999% pure Ar at a working pressure of 5- 8 mtorr. No substrate heating was used during deposition.

Device configuration of fabricated samples consisted of Al electrodes and Al_2O_3 dielectric as deposited on DuPont 951. Electrode widths were fabricated with nominal physical mask dimensions of 150, 375, 530, and 750 μm, such that there were an array of capacitors of active areas of approximately 0.0225 to 0.5625 mm^2. The panel layout is shown in Figure 1 and consists of 12 rows and 4 columns of capacitors. The 4 columns are subgrouped by top electrode width. The rows have varying top electrode widths and every 4^{th} row repeats the bottom electrode width. There are 16 different electrode configurations in this layout and 10 different capacitor areas represented due to the

repeating nature of the layout. Every total capacitor area was represented by either 3 or 6 devices.

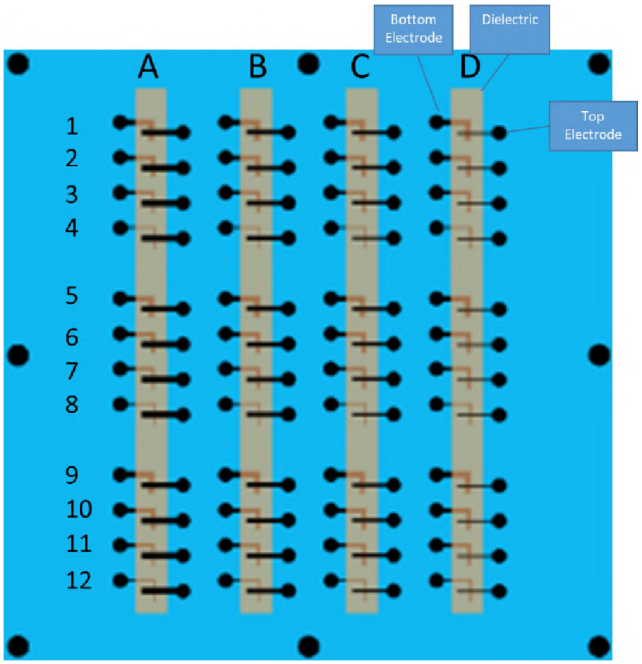

Figure 1: Schematic layout of thin film capacitors on LTCC substrate.

Actual electrode dimensions varied from nominal mask dimensions because the use of physical masks led to shadowing, which imparted different electrode dimensions and were accounted for in later calculations of effective dielectric constant of measured devices. Dimensional measurements, both lateral and thickness, were performed on a KLA Tencor (Milpitas, CA) P-17 profilometer system. The edges were not probed for conductivity to determine the edge since this was beyond the capability of the measurement setup used in this work. It was assumed the electrode was conductive up to the edge.

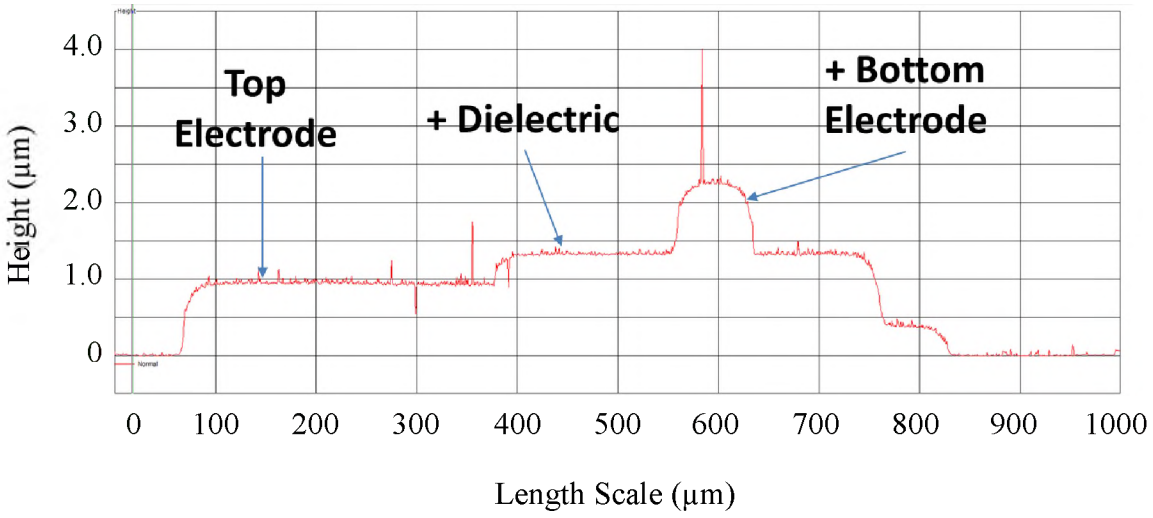

Figure 2: Typical KLA Tencor P-17 thickness profile.

Dielectric characterization was performed in a Faraday cage using a Hewlett Packard (Santa Clara, CA) 4194A Impedance Analyzer at 1 KHz, 10 KHz, and 100 KHz at room temperature.

3. FRINGE FIELD EFFECTS AND FRINGE FIELD CAPACITANCE

Additional capacitance is generated at the edge of electrodes due to the extension of the electric field beyond the physical electrode edge. This enhancement increases as a percentage of the total capacitance as the ratio of the capacitor perimeter to the area increases. In semiconductors and circuit design, fringe capacitance can lead to parasitic and undesirable performance, however in discrete devices it can be used to engineer enhanced performance. [2, 6] Accurately understanding and characterizing the extent of fringe capacitance has been studied through empirical and basic experiments. [7, 8] Little work has been published that utilizes modern physics based modeling tools to

evaluate factors that contribute to, and can therefore be used, to predict and engineer the extent of fringe capacitance within specific devices.

Other researchers have developed edge correction models to empirically account for the fringe capacitance contribution. [4] Their model has been expressed as shown in Eq. 1, where the edge capacitance contribution, C_e, is a function of the capacitor perimeter, P, and the dielectric thickness, t.

$$C_e = [0.019 \ln(P/t) - 0.043]P \qquad (1)$$

In this study, models were developed that approximate the physical structure of the as-fabricated devices to account for observed tapering of the electrode and dielectric layers. Tapering of the layers is a result of use of a physical "shadow" mask and physical vapor deposition for the fabrication of the devices on low temperature cofired ceramic (LTCC) and glass substrates. The LTCC substrates were DuPont 951® and the glass substrates.

Models were developed for the ideal condition for the capacitor devices using CST Microwave Studio (3DS Dassault Systemes) using the electrostatic solver in which the capacitor dimensions for the models utilized the defined physical mask dimensions. Perfect electrical conductors (PEC) are used for the top and bottom electrodes. The dielectric material is placed between the two electrodes. The simulation model is shown in Figure 3 and simulations were carried out where the capacitor was placed on a LTCC substrate with a dielectric constant of 7.8.

Tapers were added to the edges of all dielectric and electrode layers, however, only the taper of the electrodes impacted the model calculations since the dielectric taper was outside of the active device area. The dielectric followed the contour of the bottom

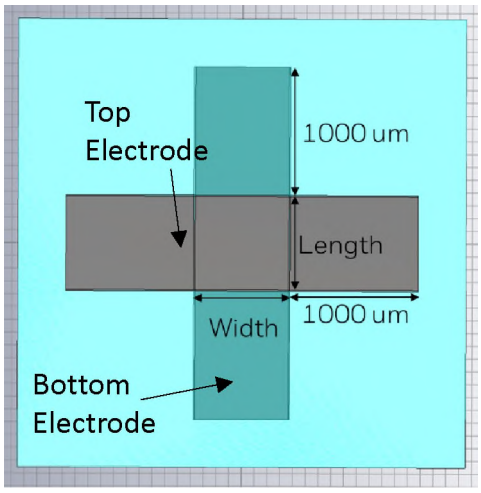

Figure 3: Model diagram 1 (note: the aqua color is the dielectric layer).

electrode taper as show in Figure 4. The tapered devices have the same overall area as the non-tapered. The taper starts 10, 100, 200, or 300 μm from the edge of the nominal dimensions. Tapering is added to the edge of electrodes as illustrated in Figure 4 and Figure 5, and the dielectric layer follows the contour of the electrode layer below it. Where the taper length is greater than ½ the nominal width of the electrode, that taper length was not applied to that electrode geometry.

Each of the taper geometry angles were calculated using Eq. 2 and is shown in Table 1. The model is completely parameterized to allow for a parameter sweep that changes the dielectric thickness, electrode thickness, capacitor width, and capacitor length. Two sets of simulations were performed: one with fringing fields and one without fringing fields. To eliminate fringing fields, magnetic boundary conditions, which force the tangential magnetic field to zero, are placed on the sides of the capacitor. For the simulation with fringing fields, open boundary conditions were used.

$$Angle\ (degrees) = \left(sin^{-1}\frac{t_{electrode}}{taper_{length}}\right) \times \left(\frac{360}{2\pi}\right) \qquad (2)$$

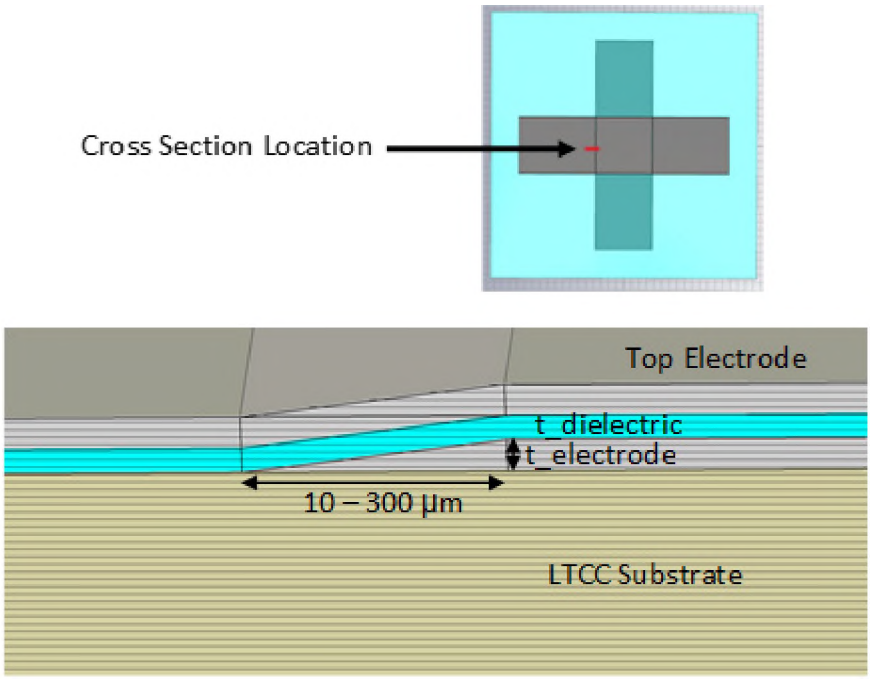

Figure 4: Model Cross Section 1.

A tetrahedral mesh was used for the simulations. The mesh density of the model was increased around the electrode edges as the magnitude of the electric field varies rapidly with position near the edges. A coarse mesh is used in the center of the capacitor where there is no electric field variation. The mesh of the simulation model is shown in Figure 6 as a top view representation of Figure 3 looking through the electrode at the meshing of the dielectric layer. The left-hand Figure 6 provides the entire top view of the model and mesh while the right-hand is an enlarged view showing the mesh detail at the edges.

An electric potential is defined on the top electrode while no potential is defined on the bottom electrode. An effective dielectric constant is then calculated by solving for

the permittivity using the parallel-plate capacitor formula and the capacitance result from simulation.

Table 1: Taper Geometry Combinations.

Electrode Thickness (µm)	Taper Length (µm)	Taper Angle (°)
1.3	10	7.47
1.3	100	0.74
1.3	200	0.37
1.3	300	0.25
0.5	10	2.87
0.5	100	0.29
0.5	200	0.14
0.5	300	0.10
0.3	10	1.72
0.3	100	0.17
0.3	200	0.09
0.3	300	0.06

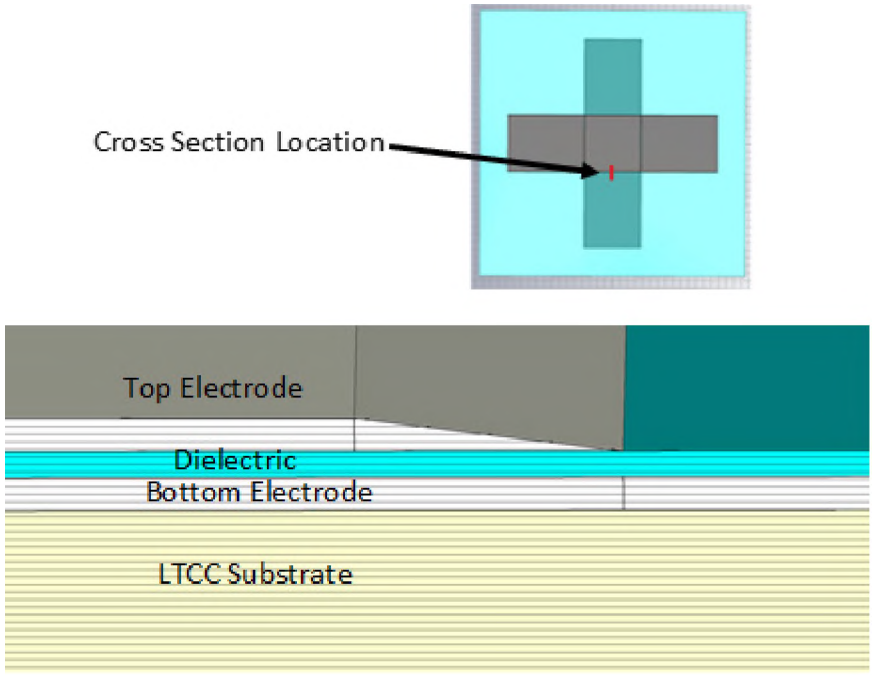

Figure 5: Model Cross Section 2.

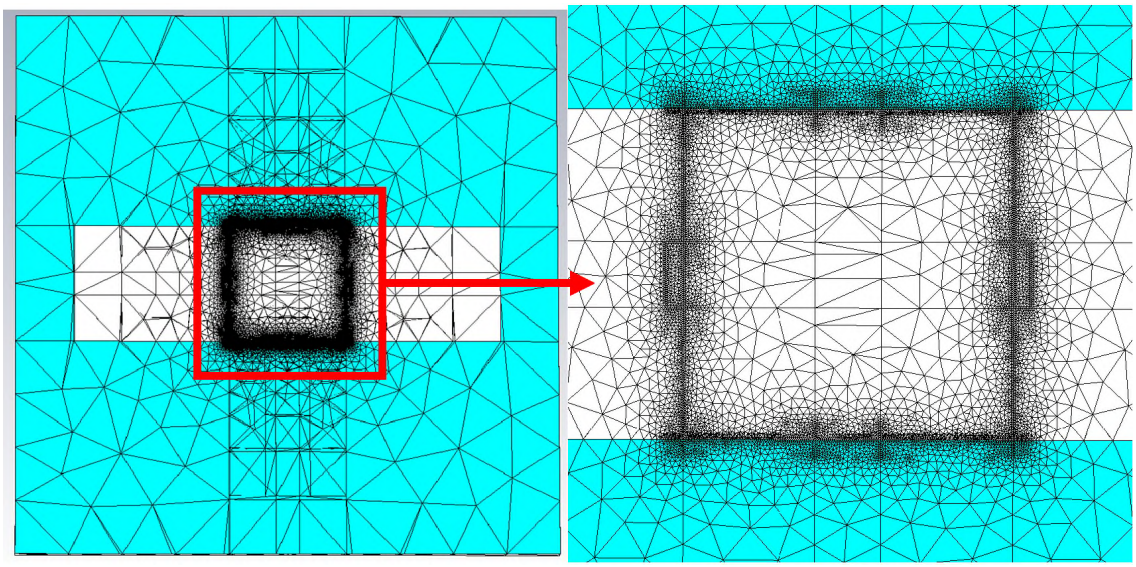

Figure 6: Tetrahedral mesh of capacitor simulation model.

In these simulations, the behavior for Al_2O_3 is modeled, but SiO_2, a lower dielectric constant material (K = 3.3) is also modeled. The second material was selected for study because of a possible decrease in the dielectric constant of Al_2O_3, due to decreased polarizability contributions. Modeling both materials also presents a more complete study of the possible magnitude of fringe field contributions to effective dielectric constant, enabling consideration of device architectures for high frequency use as noted earlier.

4. POLARIZABILITY CONTRIBUTIONS

While fringing field contributions to capacitance, and thus to the calculated dielectric constant, may represent one enhancement factor to the calculated permittivity, differences in ionic and electronic polarizability in the amorphous versus crystalline state

of the films may represent an additional contribution. The ionic polarizability contribution to dielectric constant is expected to decrease with increasing lattice spacing simply due to the lower density of charged species in the material. For the dielectric layers of the present study, increased interatomic spacing would be expected due to their amorphous state as compared with crystalline state. Thus, lower dielectric constants would be predicted. Interesting, however, Shannon, et al. [5] observed that the greater molar volume of glasses and amorphous phases compared to crystalline compounds of the identical compositions led to an abnormal positive deviation of dielectric constant and postulated that it was related to the "rattling" of loosely bound cations and disordered oxygen anions. This may also be the case in this study.

Polarizability contributions of atoms to the dielectric constant may be estimated using the Clausius-Mossotti equation (Eq. 3):

$$\frac{K_e - 1}{K_e + 2} = \frac{1}{3_{\epsilon_0}} \sum_i n_i \alpha_i \qquad (3)$$

where K_e is the effective dielectric constant of the material of interest, ϵ_0 is the permittivity of free space constant (8.85 x 10^{-12} F/m), n_i is the number of i atoms, and α_i is the polarizability of i atoms. The sum of the electronic polarizabilities, N_e, ionic polarizabilities, N_i, and dipolar polarizabilities, N_d can be summed in the Clausius-Mossotti Eq. 3 in a static electric field and represented with the following equations:

$$\frac{K_e - 1}{K_e + 2} = \frac{1}{3_{\epsilon_0}} N_e \alpha_e + N_i \alpha_i + N_d \alpha_d \qquad (4)$$

$$\frac{K_e - 1}{K_e + 2} = \frac{4\pi}{3} N_i \alpha_i \qquad (5)$$

In order to solve for the predicted K_e when the dielectric constant of the material is unknown as in the case of amorphous Al_2O_3, Eq. 5 can be transformed to the following equation:

$$K_e = \frac{\frac{8\pi}{3} N_i \alpha_i + 1}{1 - \frac{4\pi}{3} N_i \alpha_i} \qquad (6)$$

Possible effects of material structure/density on dielectric constant are analyzed below and compared with the results reported by Shannon and coworkers [5], to evaluate contributions to apparent dielectric constant.

5. RESULTS AND DISCUSSION

5.1. EXPERIMENTAL MEASUREMENTS

Samples were fabricated and measured across 1 kHz to 100 kHz for capacitance and dielectric loss. The capacitors were fabricated on DuPont 951 LTCC. As seen in Figure 7, the capacitance increased with increasing area, as expected, although the calculated dielectric constant for these samples increased with decreasing area, from a value of approximately 12 to a value of 23 for the smallest devices.

5.2. MODEL CALCULATIONS

CST Studio Suite solves for the electric field (E) and the electric flux density (D) through the structure. Various post-processing steps can be performed, which include the generation of cross sections of the 3D fields and evaluation of the field strength along the length of the path or electrode in this case. Figure 8 shows the electric field enhancement

at the edge of the electrode. To obtain the effect of the electric field enhancement at the edge of an electrode, the electric field strength was evaluated on a curve across the width of the capacitor.

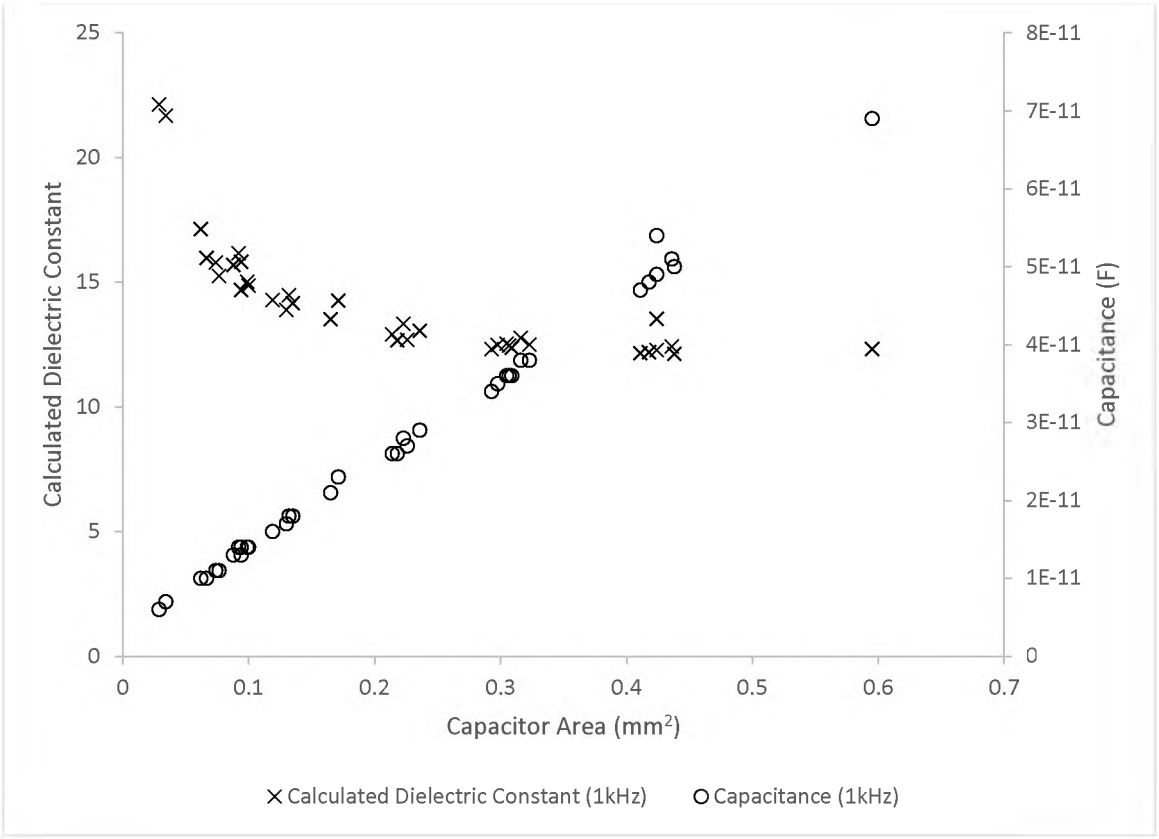

Figure 7: Al-Al_2O_3-Al Capacitors on LTCC substrate active dielectric area vs relative permittivity and capacitance.

Multiple parameters were evaluated within the fringe field model for varying electrode thickness, dielectric thickness, and capacitor length and width for the case with and without fringing. The model predicts a strong dependence of the dielectric enhancement due to the fringe field related to capacitor size. There is an increasing enhancement due to the fringe field on the dielectric as the size of the capacitor

decreases, as seen in Figure 9. The field enhanced dielectric constant would increase greater than 9% in this material. While this paper has focused on Al_2O_3 as the dielectric, other dielectrics were modeled including SiO_2. For comparison, SiO_2 with an assumed dielectric constant of 3.3, the fringe field contributed to an increase in effective dielectric constant by up to 16%.

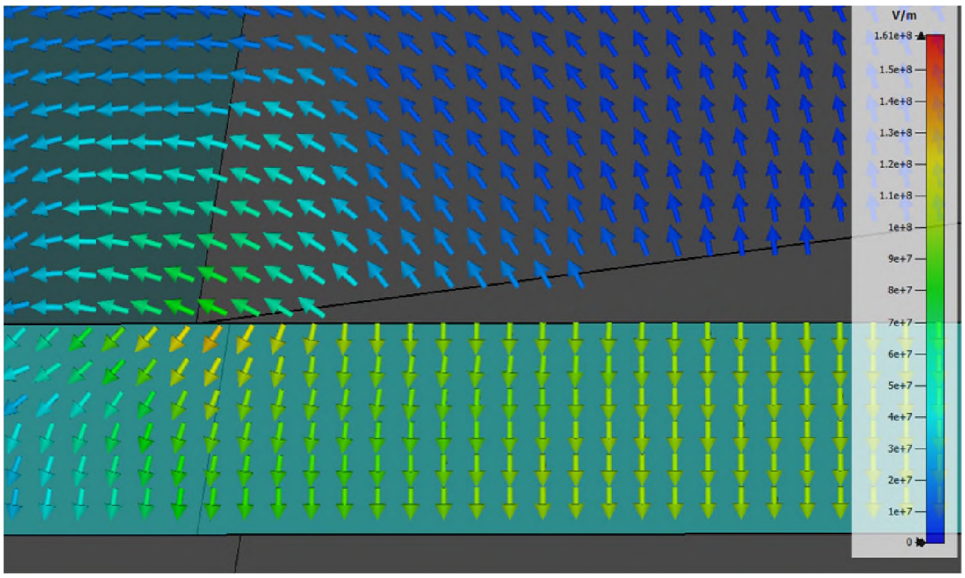

Figure 8: 2D cross section of electric field at electrode edge.

The model results were also evaluated as a function of the dielectric thickness. The dielectric thickness had a strong relationship with the enhancement in the dielectric constant: thicker dielectric devices, e.g., devices of lower capacitance, had a stronger enhancement response compared to thinner dielectric devices. (Figure 10)

Crystalline Al_2O_3 with ideal lattice parameters has a predicted dielectric constant of 10 using the Clausius-Mossotti relationship. There would be no dipolar contributions to dielectric constant with Al_2O_3 due to the nature of the material. Hexagonal crystalline

Al_2O_3 has a calculated theoretical density of approximately 3.99 g/cm^3. In contrast, the density of amorphous Al_2O_3 thin films has been reported to be 2.9 – 3.3 g/cm^3, which suggests a free volume of 19 – 37% greater compared to the crystalline state. [9, 10]

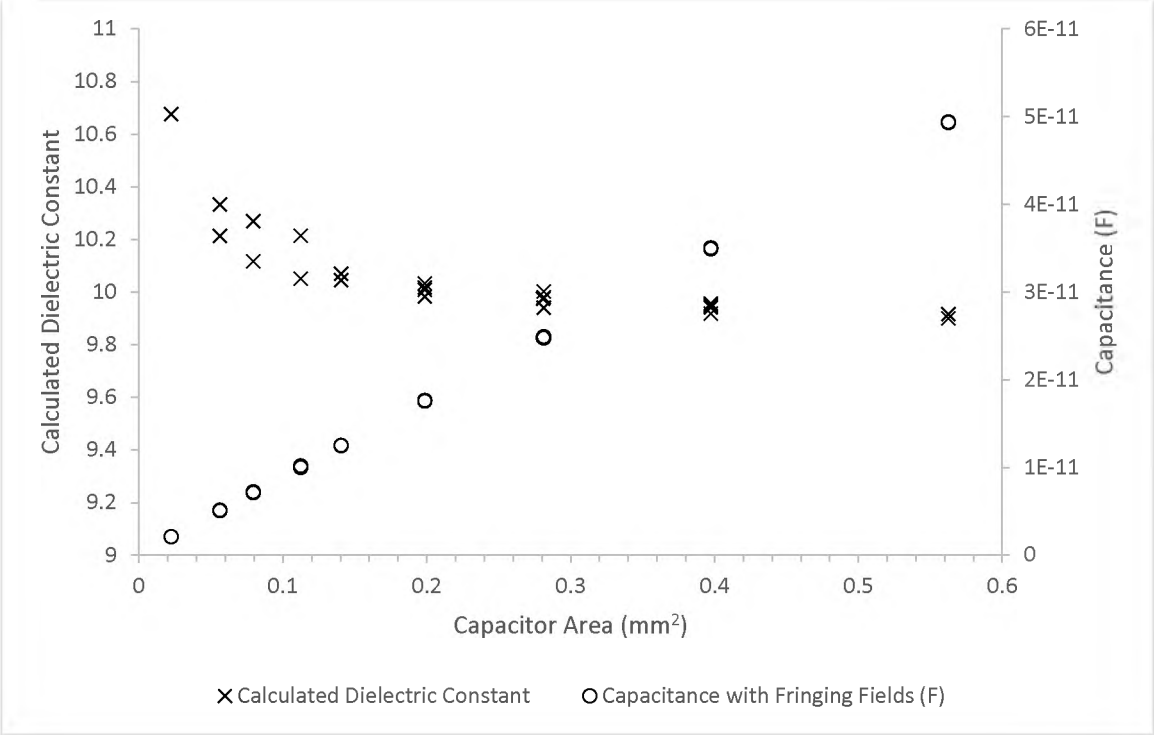

Figure 9: Model results of Al-Al_2O_3-Al Capacitors active dielectric area vs relative permittivity and capacitance.

The Clausius-Mossotti relationship from Eq. 6 was used to calculate the permittivity for hexagonal Al_2O_3 assuming standard and expanded interatomic spacing parameters in Table 2. The associated dielectric constant of amorphous Al_2O_3 based on interatomic spacing of this magnitude is 6.1 to 4.6, respectively. The model contribution of dielectric constant enhancement increases with decreasing dielectric constant, so that a material with a lower dielectric constant will experience a greater increase in capacitance

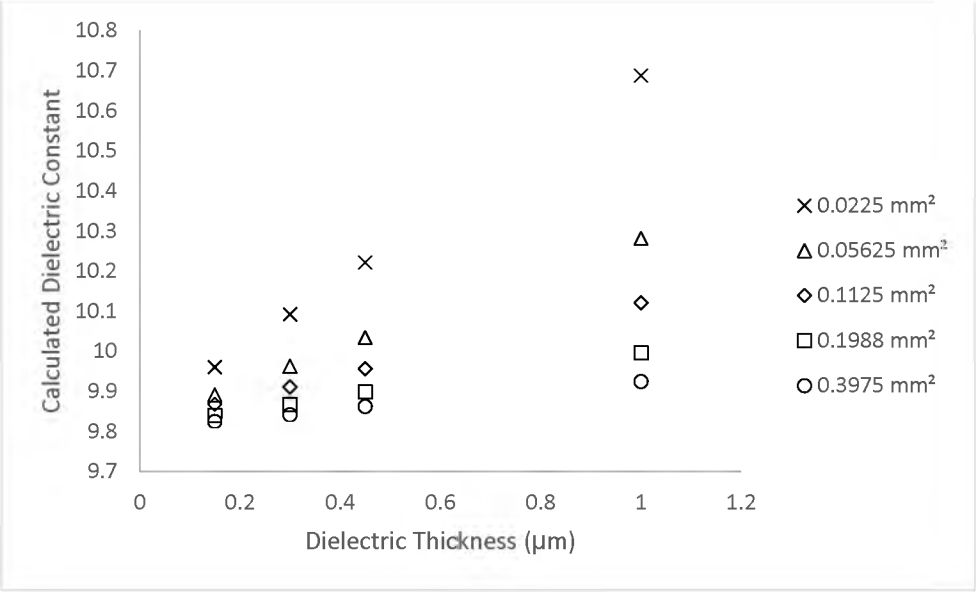

Figure 10: Model Results of Effective Dielectric Constant vs. Dielectric Thickness of Al-Al_2O_3-Al capacitors with various areas (averages of model results displayed).

Table 2: Clausius-Mossotti based dielectric constant calculations for hexagonal Al_2O_3 having expanded lattice parameters.

Interatomic Spacing Increase	a (Å)	c (Å)	Calculated Dielectric Constant	Calculated Volume (Å^3)	Calculated Vol % Increase	Calculated Density (g/cm^3)
0%	4.76	12.99	10.00	255.02	0.0%	3.98
1%	4.81	13.12	9.03	262.74	3.0%	3.87
2%	4.86	13.25	8.23	270.63	6.1%	3.76
3%	4.90	13.38	7.56	278.66	9.3%	3.65
4%	4.95	13.51	7.00	286.86	12.5%	3.54
5%	5.00	13.64	6.52	295.21	15.8%	3.44
6%	5.05	13.77	6.10	303.73	19.1%	3.35
7%	5.09	13.90	5.74	312.41	22.5%	3.25
8%	5.14	14.03	5.41	321.25	26.0%	3.16
9%	5.19	14.16	5.13	330.25	29.5%	3.08
10%	5.24	14.29	4.87	339.43	33.1%	2.99
11%	5.28	14.42	4.64	348.77	36.8%	2.91
12%	5.33	14.55	4.44	358.28	40.5%	2.84

due to fringe fields than a higher dielectric constant material. In the case of Al_2O_3 with dielectric constant of 9.8 in the model, the fringe field contributed to increasing the capacitance and effective dielectric constant by up to 10%. The thin films in this study were Al_2O_3 in a known amorphous state [11] and would likely have a density of as low as 2.9 g/cm^3, therefore a dielectric constant of as low as 4.6 from these calculations.

6. CONCLUSIONS

Thin film Al-Al_2O_3-Al capacitors on LTCC were fabricated and characterized to have higher than predicted capacitance. The capacitance was nearly double the predicted value in some cases in the characterized capacitors. Fringe field and Clausius-Mossotti polarizability contributions to capacitance were modeled for this system as potential sources of increased capacitance through dielectric enhancement. Fringe field enhancement to dielectric constant was successfully modeled using CST Microwave Studio's electrostatic solver and demonstrated up to a 9% increase in the dielectric constant due to fringe enhancements when a tapered electrode was present. While the fringe field model does not account for the entire dielectric enhancement observed experimentally, it does indicate a trend of increasing dielectric enhancement as the capacitor size decreases as observed experimentally.

The polarizability model indicated that interatomic spacing increase expected from an amorphous state as compared to a crystalline state would be expected to decrease the dielectric constant and is therefore unlikely to have contributed to any enhancement

of the dielectric in this samples. Other contributions to the observed dielectric enhancement of these films are more significant than a fringe field effect.

Another likely contribution to the dielectric enhancement of the thin film dielectrics in this study is due to a reduced effective dielectric thickness arising from accumulation layers in the dielectric adjacent to the electrodes. Electron beam induced current (EBIC) is being used to characterize the cross section of these samples for evidence of accumulation layers and their respective reduction of the effective dielectric thickness if present.

ACKNOWLEDGMENTS

The submitted manuscript has been authored by a contractor of the U.S. Government under contract no. DE-NA-0002839. Accordingly, the U.S. Government retains a nonexclusive, royalty-free license to publish or reproduce the published form of this contribution or allow others to do so for U.S. Government purposes.

REFERENCES

[1] Shannon, R.D., Dickinson, J.E., Rossman, G.R.: Dielectric Constants of Crystalline and Amorphous Spodumene, Anorthite and Diopside and the Oxide Additivity Rule, *Physics and Chemistry of Minerals*, **19**, 148-156, (1992)

[2] Trinh, H.V., Devoe, A.: High Voltage Fringe-Effect Capacitor. U.S. Patent 9,786,437, (2017)

[3] Subramanian, M.A., Shannon, R.D., Chai, B.H.T, Abraham, M.M., Wintersgill, M.C.: Dielectric Constants of BeO, MgO, and CaO Using the Two-Terminal Method, *Physics and Chemistry of Minerals*, **16**, 741-746, (1989)

[4] Pillai, K.P.P.: Fringing fields in finite parallel-plate capacitors. In: Proceedings of Institution of Electrical Engineers. London, England, 1970.

[5] R. D. Shannon, J. E. Dickinson and G. R. Rossman, "Dielectric Constants of Crystalline and Amorphous Spodumene, Anorthite and Diopsie and the Oxide Additivity Rule," Physics and Chemsitry of Minerals, vol. 19, pp. 148-156, 1992.

[6] Tane, M., Nakano, S., Nakamura, R., Ogi, H., Ishimaru, M., Kimizuka, H., Nakajima, H.: Nanovoid formation by change in amorphous structure through the annealing of amorphous Al_2O_3 thin films, *Acta Materialia*, **59**, 4631-4640, (2011)

[7] Etinger-Geller, Y., Katsman, A., Pokroy, B.: Density of Nanometrically Thin Amorphous Films Varies by Thickness, *Chemistry of Materials*, **29**, 4912-4919, (2017)

[8] Chen, P., Liu, J., Zhang, H., Chu, B.: Increase of Capacitance of Thick Dielectrics by Fringe Effect, *IEEE Transactions on Dielectrics and Electrical Insulation*, **26**, 1716-1719, (2019)

[9] Murray, J., Huebner, W., O'Keefe, M.J., Wilder, K., Eatinger, R., Kuhn, W., Krueger, D.S., Wolf, J.A.: Sputter deposition of thin film capacitors on LTCC substrates for RF bypass and filtering applications. In: Proceedings of the 44th International Symposium on Microelectronics. Long Beach, CA, 2011.

[10] Wolf, A., Peterson, K., O'Keefe, M., Huebner, W., Kuhn, B.: Fully Integrated Applications of Thin Films on Low Temperature Cofired Ceramic (LTCC). In: Proceedings of the IMAPS/ACerS 8th International CICMT Conference and Exhibition. Erfurt, Germany, 2012.

[11] Kim, C., Senior, D.E., Shorey, A., Kim, H.J., Thomas, W., Yoon, Y.K.: Through-Glass Interposer Integrated High Quality RF Components. In: Proceedings of Electronic Components & Technology Conference, Orlando, FL, 2014.

III. EFFECT OF ELECTRODE COMPOSITION ON PERFORMANCE OF SPUTTER DEPOSITED MIM CAPACITORS ON LTCC SUBSTRATES

Daniel S. Krueger[1*], J. Ambrose Wolf[1], Matthew O'Keefe[2], James B. Claypool[3], Robert W. Schwartz[3], Wayne Huebner[3]

[1]The Department of Energy's Kansas City National Security Campus, managed by Honeywell – Kansas City, MO

[2]Kansas State University – Manhattan, KS

[3]Missouri University of Science and Technology – Rolla, MO

*Corresponding author; email: dkrueger@kcnsc.doe.gov

ABSTRACT

This work systematically studies the effect that electrode composition and configuration imparts on dielectric behavior. Thin film capacitors of a Metal-Insulator-Metal (MIM) parallel plate configuration on DuPont 951 LTCC were fabricated with amorphous Al_2O_3 dielectric and aluminum, copper, or gold electrodes. The electrode configuration was varied between both cathode and anode being composed of the same metal and each being composed of different metals. Thicknesses of the dielectric and electrodes were held constant in this set of experiments. The active area of the MIM capacitors and applied voltage were varied. It was observed that the electrode composition and the configuration of the electrodes strongly influenced the capacitance, dielectric loss, and yield, which is postulated to be strongly influenced by the work function of the electrode materials in relation to that of the dielectric.

Keywords: thin film capacitor, low temperature cofired ceramic (LTCC), electrode, work function

1. INTRODUCTION

Low temperature co-fired ceramic (LTCC) substrates provide performance benefits over other packaging technologies for RF and high frequency applications [1, 2, 3]. As such, LTCC substrates are used to create Multi-Chip Modules (MCM) for mounting and interconnecting semiconductor integrated circuits. These support structures are kiln-fired in one or multiple steps, producing a monolithic carrier for the surface mounted chips [4]. Traces, vias, and passive devices are fabricated from metal pastes, utilizing the full three dimensions of the substrate.

Currently, discrete capacitors are typically surface mounted on LTCC substrates [5]. Utilizing thin film capacitors fabricated directly on the LTCC rather than surface mounted devices offers packaging miniaturization and integration advantages for RF and high reliability applications. In addition, this approach eliminates process steps and weaker links, such as solder connections, under aging and extreme environment situations. Solder joints in particular are known to effect multilayer ceramic capacitors (MLCCs) and system reliability when using MLCCs. [6, 7] However, LTCC substrates have much greater surface roughness than traditional thin film substrates or silicon wafers, making it imperative that the thin film deposition technique produce highly conformal films. Sputtering is a commonly used technique for physical vapor deposition and is usable with a wide variety of substrates and deposition materials. It yields

conformal films with good thickness uniformity, purity, and adhesion. Previous work (Murray et al.) [8] observed non-linear and anisotropic I-V behavior in thin film capacitors on LTCC. While other researchers have observed work function and surface roughness effect on I-V behavior of thin film capacitors [9, 10], the yield, effective permittivity, and dielectric loss have not been reported.

The configuration for the capacitors in this study was a metal-insulator-metal (MIM) design. The thin film capacitors were fabricated via DC magnetron sputtering on DuPont 951 LTCC substrates using Al_2O_3 as the dielectric and three types of metal electrode configurations: 1) a single metal type was used for both electrodes; 2) a bi-layer metallic (bimetallic) electrode consisting of a thin coating of Al between Cu and the dielectric; and 3) a two metal electrode system with Al as one electrode and Cu as the other electrode. The electrodes and dielectric deposition were defined using physical masks. Area of the capacitors varied between 0.0225 mm^2 and 0.5625 mm^2 and were measured optically to verify resulting dimensions.

Previous work has shown a strong effect of sputter conditions [11-14], metal-dielectric interfaces [15-17], space charge effect [18], and surface roughness [19] on capacitor performance. Metals used in the single material electrode case were Ag, Al, Au, Cu, and Pt to evaluate the effect of the material interplay at the interface between the electrode and the dielectric on capacitor performance. In the second case of a bi-layer metallic electrode, the dependence of the capacitor performance on the thickness of a thin Al layer deposited between the bulk Cu electrode and the dielectric was studied. The third case contrasts the top and bottom positions of the dissimilar Al and Cu electrode materials.

An extensive current-voltage, capacitance, and dissipation characterization and understanding of the electrode interaction with the dielectric is presented below. Energy band theory and models were qualitatively used to assess their influence on the results of this work. Quantitative modeling was beyond the scope of this study; existing software treats dielectrics as perfect insulators, with no internal band bending. Yes the influence of work function of the electrodes related to the dielectric have been shown by other researchers to have a strong influence on capacitor performance. [9, 10] Results show a marked improvement in device performance when aluminum is in direct contact with the dielectric on LTCC substrates.

2. EXPERIMENTAL

Capacitors were sputter deposited through physical masks in three separate layers onto 11x11 cm LTCC substrates (Figure 1). Layers consisted of a bottom metal electrode of 500 nm thickness, Al_2O_3 dielectric of 760 to 1010 nm thickness, and a top metal electrode of 500 nm thickness. The composition of the electrodes consisted of pure metals or stacked combinations of Ag, Al, Au, Cu, and Pt.

Metal electrode layers were deposited from 99.99% pure metal targets at 300 W using a DC magnetron power supply. The Al_2O_3 dielectric was deposited from a 99.9% pure ceramic target at 200 W using an RF power supply. All materials were deposited with a Denton Discovery 18 sputter deposition system using an atmosphere of 99.999% pure Ar at a working pressure of 5 – 8 mtorr. No substrate heating was used during deposition.

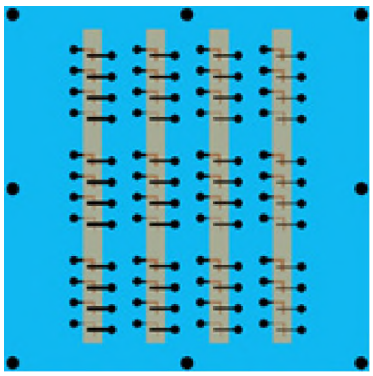

Figure 1. Schematic of relative alignment of the three physical masks. Gray vertical bars represent the dielectric and the black features represent the metal electrodes.

The physical masks were fabricated at Towne Technologies, Inc. (Somerville, NJ) using a bilayer Cu/Ni composition. Widths of the bottom and top electrodes on the masks were approximately 0.150, 0.380, 0.530, and 0.750 mm. The 90° orientation of the electrodes allowed for better tolerance to possible mask misalignment, ensuring greater yield based on purely geometrical conditions. The array of 4 columns and 12 rows results in 48 devices with 10 different areas nominally ranging from 0.0225 mm^2 to 0.5625 mm^2. Due to "bowing" of the mask during deposition, capacitor areas were generally increased from the nominal. This effect was minimized by the use of magnets to hold the masks in position. Nevertheless, all capacitors were measured optically to determine the actual capacitor areas as shown in (Figure 2).

Initial screening of devices was done with a digital multi-meter. The specification for a "good" capacitor was a resistance of > 2 MΩ. For a 0.150 x 0.150 mm^2 capacitor with a dielectric thickness of 1 μm this corresponds to a resistivity = 4.5 x 10^6 Ω·cm Results were calculated as percent yield out of 48 possible devices. Capacitance and tan δ were measured from 1 kHz to 10 MHz with an HP 4194A impedance analyzer. Results

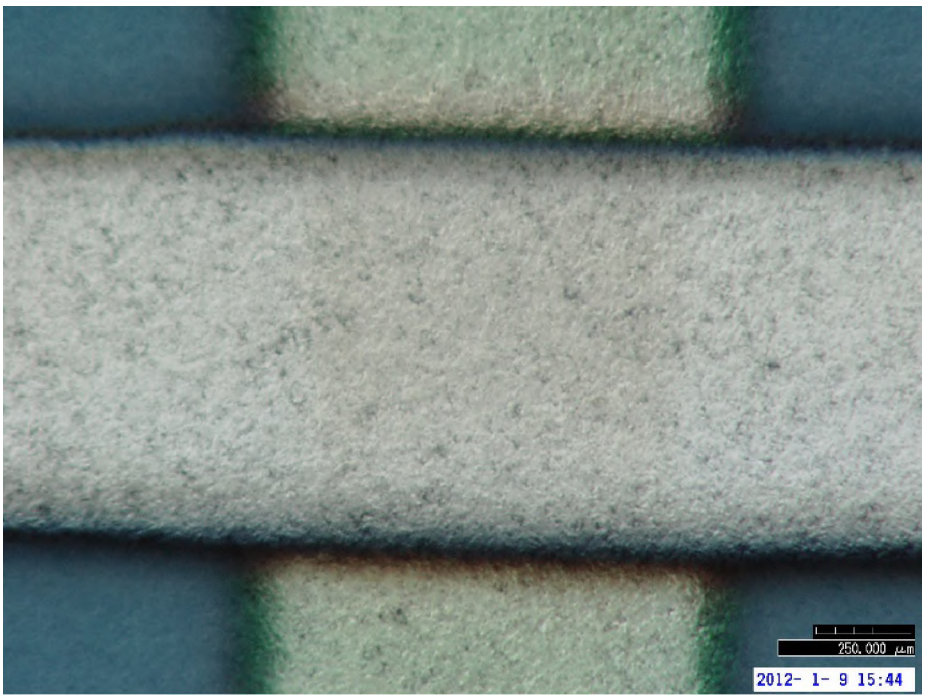

Figure 2. Picture of thin film capacitor created by overlapping two traces at a 90° angle, making actual effective capacitor area more apparent.

were plotted as relative permittivity vs. area and tan δ vs. area. Current-voltage characteristics were measured with an HP 4140B pA meter from $+V_{max}$ to $-V_{max}$ in an alternating sequence with a 5 minute charging time at each voltage, e.g., $0.05V_{max}$, $-0.05V_{max}$, $0.1V_{max}$, $-0.1V_{max}$, etc. At V_{max} = 5 V, this corresponds to electric field strengths of ±50 kV/cm for a 1000 nm thick dielectric. The alternating approach was used to evaluate asymmetry of the I-V behavior, and to ensure data was obtained in both bias directions in the even breakdown occurred. Results are reported as current density, J (A/cm^2), vs. electric field strength, E (V/cm).

The basis for comparison of the electrode systems was: A. device yield; B. capacitance, relative permittivity, and tan δ vs. area; C. J-E characteristic; and D. electrical breakdown.

3. RESULTS AND DISCUSSION

Table 1 summarizes the nine different combinations of electrodes and dielectrics utilized in this study. Schematic representations of each electrode configuration are shown` in Figure 3. All single metal samples are represented in Figure 3 (top) and have the same electrode metal composition for the bottom and the top electrode. All bimetallic samples consist of two metals composing each electrode, as shown in Figure 3 (middle) with the exception of one sample set that was coated with a thin Cu layer to improve solderability. The two metal electrode samples are shown in Figure 3 (bottom) and have a single metal layer as the bottom electrode and a different composition single metal layer as the top electrode.

Table 1: Summary of electrode configurations for capacitors evaluated in this study

Electrode Configuration	Metal A	Metal B
Single Metal	Al	N/A
Single Metal	Ag	N/A
Single Metal	Au	N/A
Single Metal	Cu	N/A
Single Metal	Pt	N/A
Bimetallic	Cu	Al
Bimetallic	Al	Cu
Two Metal	Al	Cu
Two Metal	Cu	Al

3.1. SINGLE METAL ELECTRODES

Testing began using Ag, Al, Au, Cu, and Pt as electrode systems for purposes of good electrical contact. For purposes of solderability Cu, Au, and Pt were preferred materials. However, good yields were only obtained by using Al electrodes (Table 2).

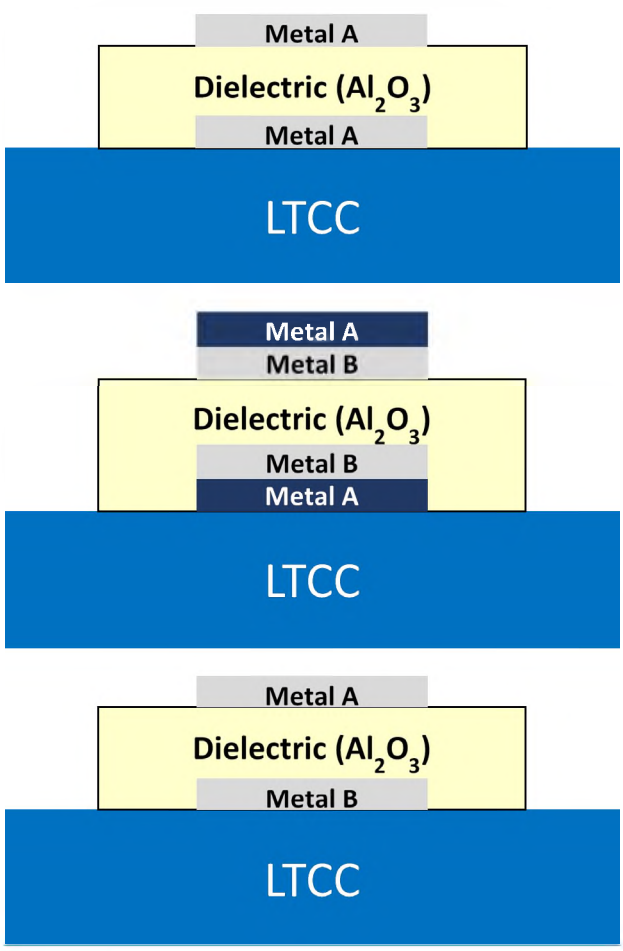

Figure 3: Cross sectional diagram of single metal (top), bimetallic (middle), and two metal (bottom) electrode capacitors.

Table 2: Single metal electrode systems.

Electrode Configuration (bottom-dielectric-top)	**Yield (% with R>2MΩ)**	**Mean tan δ (100 kHz)**
500nm Ag-1000nm Al_2O_3-500nm Ag	0%	n/a
500nm Al-1000nm Al_2O_3-500nm Al	85%	0.047
500nm Au-1000nm Al_2O_3-500nm Au	69%	0.15
500nm Cu-1000nm Al_2O_3-500nm Cu	37%	0.08
500nm Pt-1000nm Al_2O_3-500nm Pt	0%	n/a

Ag and Pt in particular yielded no working devices, while Au devices generally performed poorly in AC impedance analysis. For this reason, all subsequent testing focused on Al, Cu, and various combinations of these two materials.

Figure 4 shows relative permittivity and dissipation for electrodes that yielded functional capacitors: Al, Au, and Cu electrodes. Relative permittivity is consistent across the frequency range 1 kHz – 10 MHz for all electrode materials. Dissipation is decreasing for the pure Al sample over the frequency range 1 kHz – 1 MHz, while it is somewhat erratic for the pure Cu sample. The dissipation values for the Au electrode capacitors were generally higher than for the other electrode materials.

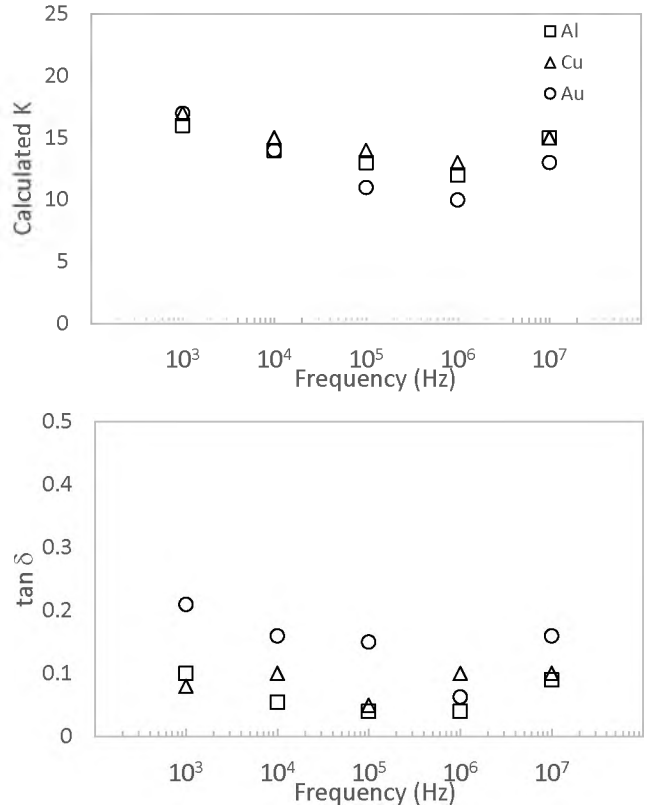

Figure 4: Average relative permittivity (top) and dissipation (bottom) for Al-Al_2O_3-Al, Au-Al_2O_3-Au, and Cu-Al_2O_3-Cu.

Current density measurements for the single metal Al samples appear to be space charge limited (Figure 5). The current density of single metal Al samples equates to resistivity values in the range of 1 – 100 TΩ cm and may be considered excellent insulators in this range. The single metal Cu samples exhibit breakdown at field strengths of 10-20 $kVcm^{-1}$ (Figure 5).

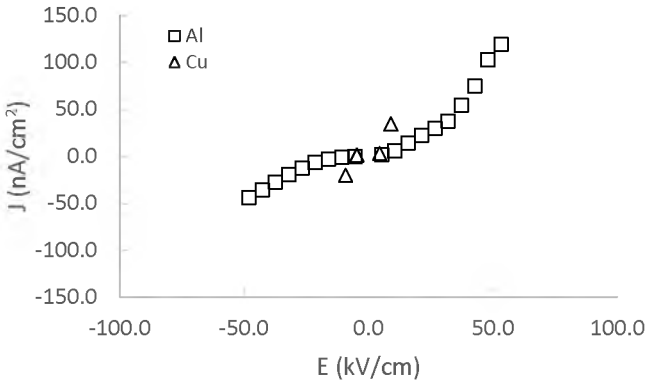

Figure 5: Representative current density vs. electric field behavior for Al and Cu single metal electrode systems.

3.2. BIMETALLIC ELECTRODES

Maintaining a Cu contact is desirable for solderability purposes, however in the single metal electrode system the Cu exhibited breakdown at unacceptable field strengths and a higher current density than Al at lower fields. Because of the poor performance of the Cu electrode samples we conjectured that a thin layer of Al at the interface in direct contact with the dielectric as seen in Figure 3 (middle) could mitigate the effect of Cu on device yield and performance.

Initially 50 nm of Al was interposed between the Al_2O_3 dielectric and the Cu electrode material. The total electrode thickness was maintained at 500 nm with

systematic increases of Al thickness of 10, 20, 50, and 80 nm and observed the effect on yield. As show in (Table 5) yield generally increased with Al thickness until a thickness of 80 nm was reached, the maximum Al thickness tested for bimetallic electrodes.

Table 3: Bimetallic electrode systems

Electrode Configuration (bottom-dielectric-top)	**Yield (% with R>2MΩ)**	**Mean tan-δ (100 kHz)**
420nm Cu-80nm Al-1000nm Al_2O_3-80nm Al-420nm Cu	75%	0.13
450nm Cu-50nm Al-1000nm Al_2O_3-50nm Al-450nm Cu	49%	0.035
480nm Cu-20nm Al-1000nm Al_2O_3-20nm Al-480nm Cu	65%	0.20
490nm Cu-10nm Al-1000nm Al_2O_3-10nm Al-480nm Cu	56%	0.10
450nm Al-50nm Cu-1000nm Al_2O_3-450nm Al-50nm Cu (Solderable surface)	35%	0.16

Since the use of a thin layer of Al was successful in mitigating the detrimental effect of Cu electrodes, whether or not a thin layer of Cu on thick Al electrodes would provide a solderable surface without adversely affecting device yield and performance was investigated. Device yield was comparable to pure Cu electrode systems (Table 2), but dissipation was relatively high compared to both pure Cu electrodes and typical bimetallic electrodes. Relative permittivity was similar to typical pure Al or pure Cu systems (Figure 6).

3.3. TWO METAL ELECTRODES

These studies illustrate that the common condition of good performing electrode systems was having at least one electrode with Al directly in contact with the dielectric.

Additionally, energy band simulations supported the idea that top electrode composition plays a strong role in device performance. In all cases the Fermi level of the top electrode is pinned to the Fermi level of the dielectric, however when Al is the top electrode there is band bending in the dielectric vs. no band bending when Cu is the top electrode. Also, the energy level of the bottom electrode is dependent on the composition of the top electrode.

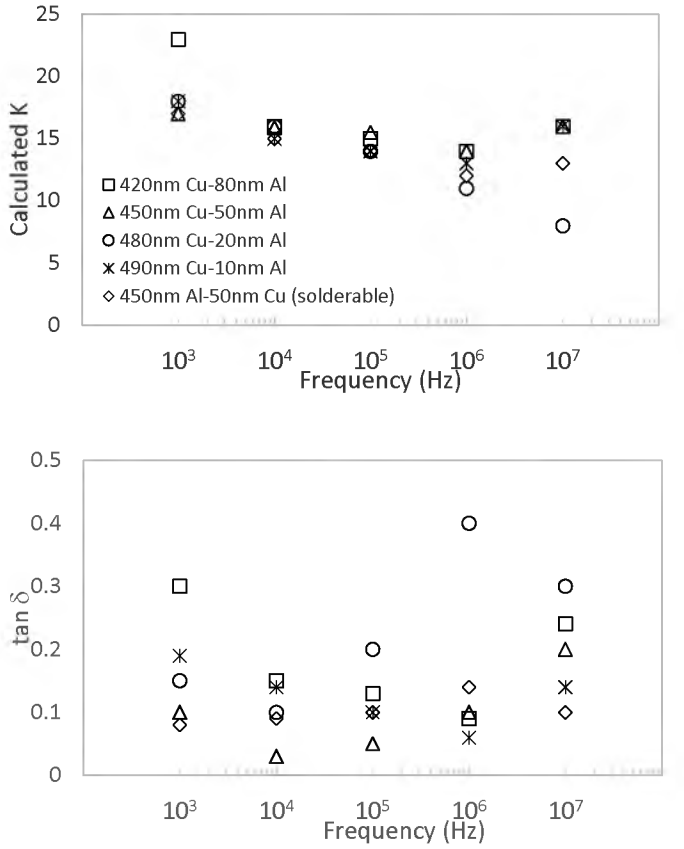

Figure 6: Average relative permittivity (top) and dissipation (bottom) for bimetallic electrode configurations.

Because of these results, samples were produced where the top and bottom electrodes were composed of two different metals: either Cu on bottom and Al on top

(Cu-Al); or Al on bottom and Cu on top (Al-Cu). Figure 7 shows the impedance analysis for these samples. Relative permittivity is essentially the same for all two metal electrode configurations studied (Al-Cu and Cu-Al). However, dissipation and yield are strongly dependent on the electrode configuration. In terms of yield and dissipation the Cu-Al configuration is best, having an average yield of 93% (Table 4) and dissipation less than 0.02 at frequencies from 100 kHz – 1 MHz.

Current density measurements also show a difference between the Cu-Al and Al-Cu configurations. The Al-Cu configuration has a resistivity of 1 GΩcm – 100 TΩcm and may be beginning to breakdown at field strengths > $\left|40\right|$ $kVcm^{-1}$ (Figure 8).

Hwei et al. have suggested that electrically induced diffusion of Cu ions were responsible for breakdown of MIM capacitors with an Al bottom electrode and Cu top electrode. [20]

Table 4: Two metal electrode systems

Electrode Configuration (bottom-dielectric-top)	**Yield (% with R>2MΩ)**	**Mean tan-δ (100 kHz)**
500nm Al-1000nm Al_2O_3-500nm Cu	65%	0.07
500nm Cu-1000nm Al_2O_3-500nm Al	93%	0.015

The basic question to address is why noble metals such as Pt and Au did not work for fabricating these MIM capacitors. Certainly within the early days of multilayer ceramic capacitors, Pt, Pt/Au, Pt/Pd/Au and other refractory noble metal systems were commonly used as the electrode of choice for high reliability capacitors. This was driven by the need for the electrode to be cofired within the dielectric. When a metal comes into

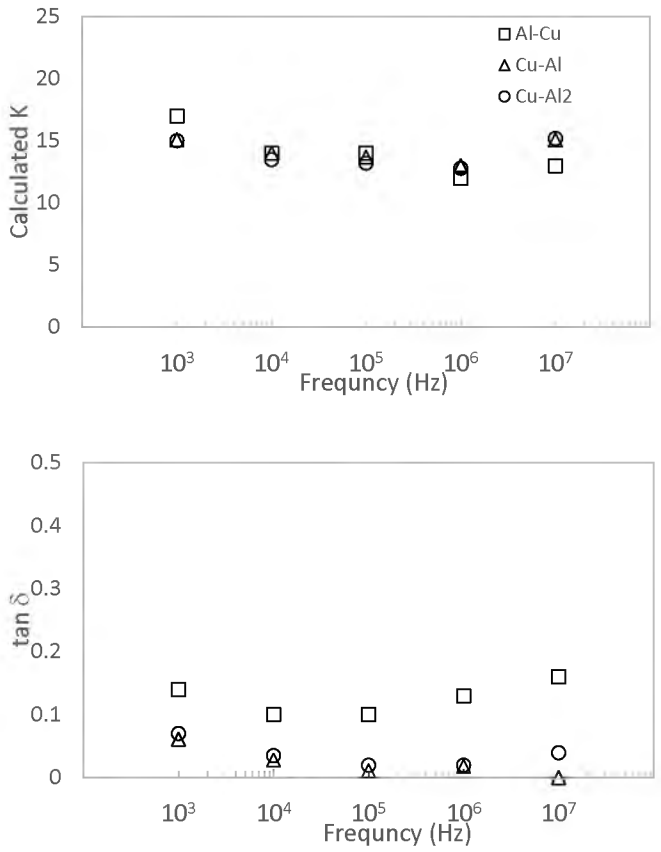

Figure 7: Average relative permittivity (top) and dissipation (bottom) for two metal electrode configurations. Note that two sets of Cu-Al samples with the same characteristics were studied (denoted as Cu-Al and Cu-Al2).

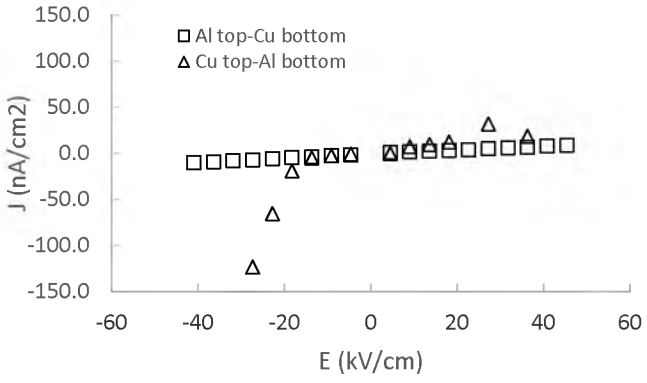

Figure 8: Representative current density vs. electric field behavior for Al-Cu and Cu-Al two metal electrode systems.

contact with a semiconductor or dielectric, differences in the work functions cause electron transfer as the Fermi levels equilibrate. For semiconductors, this is a well understood phenomenon that controls whether ohmic or non-ohmic, rectifying contacts form. Within the semiconductor accumulation, depletion or inversion layers will form depending upon the relative work functions, and electron/hole concentrations. This also affects the depth, w, that band bending occurs in the semiconductor, and can be modeled using Poisson's equation (Eq. 1):

$$w = \left[\frac{2\varepsilon}{q}\left(\frac{N_A+N_D}{N_A N_D}\right)\Delta\phi\right]^{1/2} \qquad (1)$$

where N_A and N_D are the hole and electron concentrations, $\Delta\phi$ is the difference in work functions, ε is the permittivity and q the charge on an electron.

This depth increases with the permittivity of the semiconductor, smaller carrier concentrations and the $\Delta\phi$. When creating a capacitor, whether or not the metal forms an ohmic or non-ohmic contact is typically irrelevant since the device by choice needs to be an insulator; that is, unless the thickness of the resultant band bending that occurs is on the same order as the dielectric thickness.

Table 5 contains the work functions of the metals used in this work, and that of Al_2O_3. In all instances, the work functions of the metal are greater than that of the Al_2O_3, meaning that all will form non-ohmic contacts. For an insulating dielectric such as Al_2O_3, this would result in the formation of p-type accumulation layers within the dielectric. The metals that did not work in this study, Pt and Au, have the greatest work function difference compared to Al_2O_3. The metals that worked better, Al and Cu, have work functions closer to Al_2O_3. These results suggest that the band bending occurring in

the Al_2O_3 for the high work function metals is overlapping enough to effectively decrease the overall resistivity and rendering the devices useless as a capacitor.

Table 5: Work Functions of Metals [21] and Al_2O_3 Dielectric [22].

Metal	Work Function (eV)
Al	4.06 – 4.41
Au	5.1 – 5.47
Cu	4.48 – 4.94
Pt	5.65 – 5.7
Al_2O_3	3.90

Modeling efforts are challenging since carrier concentrations for Al_2O_3 are unknown. If the intrinsic reaction is assumed to control conduction, then $N_A = N_D$, and the actual carrier concentration will be negligible at room temperature since the band gap of Al_2O_3 is ≈ 7 eV. Using $N_A = 10^4/m^3$, $\varepsilon_r = 10$, and $\Delta\phi = 1$ eV, as an example, the penetration depth calculates to be 133 nm, a number that is appreciable compared to the dielectric thickness of 1000 nm. Band bending of this magnitude might, therefore, decrease the effective thickness of the dielectric, contributing to higher observed effective dielectric constants. We plan to further investigate this contribution to capacitor performance.

4. CONCLUSIONS

The results of this investigation show that the material composition of the electrodes plays a critical role in capacitor performance. In particular, an aluminum layer in the top electrode in direct contact with the Al_2O_3 dielectric provides significant

improvements in yield, dissipation, and dielectric strength compared to copper only electrodes, while Cu contributes improved solderability characteristics. The exact nature of the electrode-dielectric interaction is unknown, but appears to be related to band shifting in the dielectric; a focus of current work. Future investigations will also widen the range of electrode materials and processing to determine this relationship.

ACKNOWLEDGMENT

The submitted manuscript has been authored by a contractor of the U.S. Government under contract no. DE-NA-0002839. Accordingly, the U.S. Government retains a nonexclusive, royalty-free license to publish or reproduce the published form of this contribution or allow others to do so for U.S. Government purposes.

REFERENCES

[1] K. Kuang, F. Kim, and S. S. Cahill, *RF and Microwave Microelectronics Packaging*, Springer Science+Business Media, 2010.

[2] J. A. Wolf, *et al*, "Fully Integrated Application of Thin Films on Low Temperature Cofired Ceramic (LTCC)," *IMAPS/ACerS Int. CICMT Conf.*, 2012, vol. 8, pp. 339-340.

[3] T. Schless, "The Relevance of Low Temperature Co-fired Ceramic Module Packaging in the 5G Market," *IMAPS Int. Symp. Microelec.*, 2017, vol. 50, pp. 773-778.

[4] C. Q. Scranton and J. C. Lawson, "LTCC Technology: Where We Are Ane Where We're Going-II," *MTT-S Symposium on Technologies for Wireless Applications*, 1999, pp. 193-200.

[5] K. A. Peterson, *et al*, "Novel Microsystem Applications with New Techniques in Low-Temperature Co-Fired Ceramics," Int. J. Appl. Ceramic Technol., vol. 2, no. 5, pp. 345-363, 2005.

[6] C.-M. Huang, *et al*, "Life cycle trends of electronic materials, processes and components," *Microelectron.. Reliab.*, vol. 99, pp. 262-275, 2019.

[7] J.-H. Chae, I.-H. Park, and H.-J. Youn, "Thermo-Mechanical Stresses and Mechanical Reliability of Multilayer Ceramic Capacitors (MLCC)," *J. Am. Ceram. Soc.*, vol. 90, no. 7, pp. 2151-2158, 2007.

[8] J. Murray, *et al*, "Sputter deposition of thin film MIM capacitors on LTCC substrates for RF bypass and filtering applications," *IMAPS Int. Symp. Microelec.*, 2011, vol. 44, pp. 747-751

[9] T. Kim, *et al*, "Effect of Microstructure and Crystalline Orientation of Pt Single- or Pt/Ru Bilayer-Electrodes on the Work Function and Leakage Current of $SrTiO_3$ Capacitors," Jpn. J. Appl. Phys., vol.. 47, no. 8, pp. 6374-6379, 2008.

[10] J. H. Han, *et* al, "Improvement in the leakage current characteristic of metal-insulator-metal capacitor by adopting RuO_2 film as bottom electrode," Appl. Phys. Lett., vol. 99, no. 2, 2011.

[11] Y. Zhang, *et al*, "Optical and Electrical Properties of Magnetron Sputtering Deposited Cu-Al-O Thin Films," Int. J. Antennas Propag, vol. 2012.

[12] K. Koski, J. Holsa, and P. Juliet, "Properties of aluminum oxide thin films deposited by reactive magnetron sputtering," Thin Solid Films, vol. 339, pp. 240-248, 1999.

[13] S. Prasanna, *et al*, "Dielectric properties of DC reactive magnetron sputtered Al_2O_3 thin films," Thin Solid Films, vol. 520, no. 7, pp. 2689-2694, 2012

[14] M. Voight and M. Sokolowski, "Electrical properties of thin rf sputtered aluminum oxide films," Mater. Sci. Eng. B Solid State Mater. Adv. Technol., vol. 109, pp. 99-103, 2004.

[15] M. Peressi, N. Binggeli, and A. Baldereschi, "Band engineering at interfaces: theory and numerical experiments," J. Phys. D. Appl. Phys., vol. 31, pp. 1273-1299, 1998.

[16] Y.-C. Yeo, T.-J. King, and C. Hu, "Metal-dielectric band alignment and its implications for metal gate complementary metal-oxide-semiconductor technology," J. Appl. Phys., vol. 92, no. 12, pp. 7266-7271, 2002.

[17] C.-H. Lu, *et al*, "Characteristics and Mechanism of Tunable Work Function Gate Electrodes Using A Bilayer Metal Structure on SiO_2 and HfO_2," IEEE Electron Device Lett, vol. 26, no. 7, pp. 445-447, 2005.

[18] G. Blaise and W. J. Sarjeant, "Space Charge in Dielectrics: Energy Storage and Transfer Dynamics from Atomistic to Macroscopic Scale," IEEE Trans. Dielectr. Electr. Insul., vol. 5, no. 5, pp. 779-808, 1998.

[19] Y. P. Zhao, G. C. Wang, and T. M. Lu, "Surface-roughness effect on capacitance and leakage current of an insulating film," Phys. Rev. B, vol. 60, no. 12, pp. 9157-9164, 1999.

[20] C. Hwei Ng, *et al*, "MIM Capacitor Integration for Mixed-Signal/RF Applications," IEEE Trans. Elec. Dev., vol. 52, no. 7, pp. 1399-1409, 2005.

[21] Elemental Work Functions from CRC, 75th Edition

[22] W. Song and M. Yoshitake, "A work function study of ultrathin alumina formation on Cu-9% Al (111) surface," *Surf. Interface Anal.*, vol. 38, pp. 793-796, 2006

SECTION

2. CONCLUSIONS AND RECOMMENDATIONS

2.1. CONCLUSIONS

Automotive, mobile, medical, 5G, and other high reliability industries continue to drive demand for high density microelectronic packaging and components such as capacitors. The high reliability requirements of these industries in particular make LTCC an attractive choice for performing in demanding environments. Current LTCC and MCM technology can benefit from further integration of passive components and technologies like the use of thin films to overcome limitations. [41-43] Thin film integration with LTCC and MCM technology has been previously studied and this research expands upon some of that work. Specifically, this research addresses the interaction of the substrate properties with thin film performance for circuit and capacitor functions.

Paper I evaluates limitations with adhesion of thin films on the LTCC substrates. A simplified model of the LTCC substrate is developed that uses Al_2O_3 and amorphous SiO_2 as surrogate constituents to represent the complex composition. A quantum mechanics model is applied to the simplified LTCC model with Ti and Cu metallizations and their oxides to understand thermodynamic interface energetics associated with each combination. The model and calculations indicate lower interfacial energies associated with Ti on Al_2O_3 as compared with amorphous SiO_2. These model results were empirically confirmed with peel tests on treated and untreated substrates where the

treated substrate resulted in increased exposure of Al_2O_3 grains at the surface and superior adhesion of the Ti metallization.

Paper II describes various mechanisms which can contribute to dielectric constant enhancement. In this research, higher than expected capacitance was observed in thin film, amorphous Al_2O_3 MIM capacitors on LTCC. The measured capacitance and device dimensions were used to calculate effective dielectric constants for the devices that were higher than the reported dielectric constant for Al_2O_3. Dielectric constant enhancements were inversely proportional to device size. Fringe field capacitance was modeled in this study using advanced computing capabilities to determine the contribution of fringe field due to electrode size and geometry on increased capacitance and therefore dielectric constant enhancement. The model indicated increases in calculated dielectric constant of up to 9% for the smallest devices in the study, however this enhancement was significantly lower than observed in actual samples. This difference between fringe field capacitance contributions and measured capacitance indicates additional contributions to dielectric constant enhancement are present that are not accounted for by the model.

Paper III reports on thin film, amorphous Al_2O_3 capacitors on LTCC with various thin film metal electrode compositions and configurations. Ag, Al, Au, Cu, and Pt were used as electrode materials individually and in some cases in combination. This study observed that electrode composition plays an important role in capacitor performance and yield. Al exhibited the most consistent dielectric strength, dissipation, and yield. In combination with Cu as one electrode, Al as the top electrode also performed similarly to when Al was the top and bottom electrode material. Consideration of the capacitor yield data for the different electrode materials, e.g., work function effects, together with a

rudimentary calculation of band bending depth seem to suggest that accumulation regions in the dielectric may be related to both observed yield behavior and dielectric constant enhancements.

2.2. RECOMMENDATIONS

The current research presented a partial understanding of the overall objectives need to develop thin film capacitors for high reliability applications, however additional work is recommended. Methods to quantify effective dielectric thickness, characterization of capacitor temperature dependence, additional energy band modeling, and the development of an empirical model of dielectric constant enhancement are some of the future work that will benefit the development of these devices.

2.2.1. Quantification of Effective Dielectric Thickness. The results of this research have evaluated the inferred effective dielectric thickness of Al_2O_3 thin film MIM capacitors on LTCC and prior work has quantified the as-deposited physical thickness of the Al_2O_3 and electrode films. Methods to quantify the actual effective dielectric thickness will aid in confirming the mechanism(s) of the increased effective dielectric constant. One method to quantify the effective dielectric thickness is electron beam induced current (EBIC). Some experimentation was conducted with the EBIC technique to image and measure thickness indirectly through picoammeter results with initial imaging showing some promise, however, further investigation is needed to optimize the SEM and EBIC configuration such that ambient EMI is minimized.

2.2.2. Temperature Dependence Characterization. Temperature dependent I-V/J-E measurements would further confirm non-linear conduction mechanisms in the

dielectric layer of the capacitors. Samples from this research have been consumed though and are no longer available for this characterization. New samples are required as well as a suitable test setup that includes a programmable temperature chamber, pico-ammeter, LCR bridge, and sample fixture. This setup was created and used to characterize a set of $SrTiO_3$ capacitors and has been shown to be capable of the necessary measurements.

2.2.3. Energy Band Modeling. Confirmation of work function and energy band contributions to electrode composition effects on dielectric performance and yield has yet to be completed with models capable of representing the as-fabricated devices within this study. Several modeling software suites and custom developed programs have been researched. Based on this research, the COMSOL Semiconductor module may be capable of this complex modeling where other programs have had insufficient capabilities and/or errors that prevent accurate modeling of the electrode composition effect on dielectric behavior.

2.2.4. Dielectric Enhancement Model. The fringe field enhancement model results in Paper II indicated a trend in enhancement of dielectric constant that related to capacitor size, while not accounting for the entire magnitude of enhancement. The energy band calculations presented in Paper III indicate a relationship with electrode metallization and configuration creating semiconducting regions in the dielectric that may also enhance the dielectric constant through reduction in the effective thickness of the dielectric. An empirical model should be developed that includes the dielectric enhancement contributions from these multiple sources and could be utilized by practioners to more predictively design thin film capacitors for MCMs.

BIBLIOGRAPHY

[1] Hench, L. L. and West, J. K, Principles of Electronic Ceramics, Wiley-Interscience, New York, pp. 185 – 191, (1990)

[2] Kuhn, W. B., Wolf, J. A., "Thin Film Capacitor Application in RF/Microwave Circuits, Proc. 50th International Symposium on Microelectronics, Raleigh, NC, USA, October 2017, 56 – 60 (2017)

[3] Liotta, B., "Capacitor crunch: MLCC tags rising", EE Times, www.eetimes.com/document.asp?doc_id=1120963#, (1999)

[4] Jorgensen, B., "How the Supply Chain Developed an IP&E Shortage", EPS News, https://epsnews.com/2018/09/19/supply-chain-ipe-shortage/, (2018)

[5] Margraf, R., "MLCC shortage leads to modular-focused shift in 2019, according to industry expert", The BurnIn, https://www.theburnin.com/industry/mlcc-shortage-leads-new-direction-2019/ (2018)

[6] Wolfe, D. "The global shortage of capacitors impacts all consumer electronics", Quartz, https://qz.com/1575735/a-mlcc-shortage-is-stifling-electronics-hardware-auto-makers/, (2019)

[7] "Capacity Expansion in the Global MLCC Industry: 2018 – 2019 Forecasts", http://www.paumanokgroup.com/homepage/capacity-expansion-in-the-global-mlcc-industry-2018-2019-forecasts-isbn-1-893211-08-8-updated-april-may-2018.html, Paumanok Publications, (2019)

[8] "The global MLCC shortage: What are your options?", Avnet Abacus, https://www.avnet.com/wps/portal/abacus/solutions/technologies/passive/capacitors/the-global-mlcc-shortage/, (2019)

[9] Rentsch, S., Müller, J., Hein, M., "Tunability, Frequency, and Temperature Behavior of Cofired LTCC-Integrated Barium-Strontium-Titanate Shunt Capacitors up to 8 GHz", *Journal of Microelectronics and Electronic Packaging*, 10 (2013) 23 – 29

[10] Wolfe, D., "The global shortage of capacitors impacts all consumer electronics", The Quartz, https://qz.com/1575735/a-mlcc-shortage-is-stifling-electronics-hardware-auto-makers/, (2019)

[11] Han, D., "Material Shortage & Price Trend", Silecta, https://lyticafasttrack.files.wordpress.com/2018/07/silecta-material-shortage-price-trend-report.pdf, (2018)

[12] Schwartz, B., "Review of Multilayer Ceramics for Microelectronic Packaging", *Journal of Physical and Chemistry of Solids*, 45 (1984) 1051-1068

[13] Putman, C., Cramm Horn, R., Wolf, A., and Krueger, D., "Thermodynamic Analysis of Physical Vapor Deposited (PVD) Inorganic Thin Films on Low Temperature Cofired Ceramic (LTCC)", *Journal of Microelectronics and Electronic Packaging*, 13 (2016) 95-101

[14] Peterson, K. A., Krueger, D. S., Sandoval, C. E., "Selected Applications and Processing for Low Temperature Cofired Ceramic", Proc. 43rd International Symposium on Microelectronics, Raleigh, NC, USA, October 2010, 248-253

[15] Golonka, L. J., "New Application of LTCC Technology", Proc. 28th Int. Spring Seminar on Electronics Technology, Austria, May 2005, 148-152

[16] Lu, R., Shorey, A., "Glass Solutions for Packaging and IoT", Proc. 50th Int. Symp. On Microelectronics, Raleigh, NC, USA, October 2017, 473-476

[17] Mohanran, A., Messing, G. L., and Green, D. J., "Densification and Sintering Viscosity of Low-Temperature Co-fired Ceramics", *Journal of the American Ceramic Society*, 88 [10] (2005) 2681-2689

[18] Pond et al., "Custom Packaging in a Thick-Film House Using Low-Temperature Cofired Multilayer Ceramic (LTCC) Technology", ISHM Proceedings 1984

[19] Krueger, D. S., et al., "Effect of Dielectric Selection on Sintering Behavior of LTCC", Proc. 43rd International Symposium on Microelectronics, Raleigh, NC, USA, October 2010, 261-267

[20] Trivedi, H. C., et al., "High-Q Embedded LTCC Inductors for high performance RF MCMs", Proc. 2020 IEEE International Conference on Electronics, Computing and Communication Technologies (CONECCT), Bangalore, India, July 2020,

[21] Xia, L., Xu, R., and Yan, B., "LTCC-Based Highly Integrated Millimeter-Wave Receiver Front-End Module", *Int. J. Infrared Milli Waves*, 27 (2006) 975-983

[22] Wolf, J.A., Peterson, K. A., "Thin Film on LTCC for Connectivity and Conductivity," *Journal of Microelectronics and Electronic Packaging*, 8 [2] (2011) 43-48

[23] Girardi, M. A., Peterson, K. A., and Vianco, P. T., "LTCC Thick Film Process Characterization", Proc. 12th International CICMT Conference and Exhibition, Denver, CO, USA 142-150 (2016)

[24] Tomsia, A. P., and Pask, J. A., "Chemical reactions and adherence at glass/metal interfaces: an analysis", *Dental Materials*, 2 [1] (1986) 10-16

[25] Benjamin, P., Weaver, C., "The Adhesion of Evaporated Metal Films on Glass," Proceedings of the Royal Society of London. Series A, Mathematical and Physical Sciences, 261 (1307) 516-531, (1961)

[26] Volinsky, A. A., Moody, N. R., Gerbrich, W. W., "Interfacial Toughness Measurements for Thin Films on Substrates," *Acta Materialia*, 50 (2002) 441-466

[27] Juan, P. C. Chou, H. C., Lee, J. Y. M., "The Effect of Electrode Material on the Electrical Conduction of Metal-Pb($Zr_{0.53}Ti_{0.47}$)O_3-Metal Thin Film Capacitors", *Microelectronics Reliability*, 45 (2005) 1003-1006

[28] Horiuchi, N., Hoshina, T., Takeda, H., Tsurumi, T., "The Influence of Metal/Perovskite-Type Oxide Interfaces on Tunability of Thin Film Capacitors", *Journal of the Ceramic Society of Japan*, 118 (2010) 664-668

[29] Subramanian, M.A., Shannon, R. D., Chai, B. H. T, Abraham, M. M., Wintersgill, M. C., "Dielectric Constants of BeO, MgO, and CaO Using the Two-Terminal Method", *Physics and Chemistry of Minerals*, 16, (1989) 741-746

[30] Imanaka, Y., Multilayered Low Temperature Cofired Ceramics (LTCC) Technology, Springer, US (2005)

[31] Rohde, S. L., ASM Handbook, Volume 5: Surface Engineering; Sputter Deposition, ASM, US, pp. 573-581, (1994)

[32] Goj, B. Brokmann, U., Bartsch, H., Rädlein,, E., Müller, J., "Thin-Film Capable Ceramics for Humidity and Temperature Sensing Applications", 58th Ilmenau Scientific Colloquium, Ilmenau, Germany, September 2014

[33] Mi, X., Takhashi, T., Ueda, S., "Integrated Passives on LTCC for Achieving Chip-Sized-Modules", Proc. of the 38th European Microwave Conference", Amsterdam, The Netherlands, October 2008

[34] Souders, K. E., Nair, K. M., McCombs, M. F., Parisi, J. M., Nair, D. M., "DuPont Green Tape 9K7 Low Temperature Co-fired Ceramic (LTCC) Low Loss Dielectric System for High Frequency Applications", *Advances in Electroceramic Materials II*, 221 (2010) 213-229

[35] Knudson, R., Barner, G., Smith, F., Zawicki, L., Peterson, K., "Full Tape Thickness Features for New Capabilities in LTCC", Proceedings of the 41st International Symposium on Microelectronics, Providence, RI USA 341-348 (2008)

[36] Peterson, K. A., Knudson, R. T., Smith, F. R., Barner, G., "Full tape thickness feature conductors for EMI structures," U.S. Patent 8,747,591 (2014)

[37] J. A. Wolf, K. A. Peterson, P. T. Vianco, M. H. Johnson, S. Goldammer, "Robustness and Versatility of Thin Films on Low Temperature Cofired Ceramic," Proc. 44th International Symposium on Microelectronics, Long Beach, CA USA 559-565 (2011)

[38] Krueger, D., Peterson, K., and Euler, L., "Electromagnetic Isolation Solutions in Low Temperature Cofired Ceramic (LTCC)", Proc. of the 44th International Symposium on Microelectronics, Long Beach, CA USA 760-767 (2011)

[39] Krueger, D., Porter, J., and Peterson, K., "Stress and Strain Modeling of Low Temperature Cofired Ceramic (LTCC) Seal Frame and Lid", *Journal of Ceramic Science and Technology*, 6 [4] (2015) 261-266

[40] Krueger, D. S., et al., "Monolithic LTCC seal frame and lid," U.S. Patent 9,374,923 (2016)

[41] Kuang, K., Kim, F., Cahill, S. S., RF and Microwave Microelectronics, Springer Science+Business Media, 2010

[42] Wolf, J. A., Peterson, K. A., O'Keefe, M. J., Huebner, W., Kuhn, B., "Fully Integrated Application of Thin Films on Low Temperature Cofired Ceramic (LTCC)," Proceedings of the 8th International CICMT Conference and Exhibition, Erfurt, Germany 339-340 (2012)

[43] Schless, T., "The Relevance of Low Temperature Co-fired Ceramic Module Packaging in the 5G Market," Proceedings of the 50th International Symposium on Microelectronics, Raleigh, NC USA 773-778 (2017)

VITA

Daniel Scott Krueger was born in Kansas City, Missouri and was raised in Grandview, Missouri until his family moved to Leawood, Kansas where he completed his secondary education at Blue Valley North High School. He completed his Bachelor of Science degree in Ceramic Engineering at the University of Missouri – Rolla (now Missouri S&T) in 1994 where he also worked as an undergraduate research assistant for Dr. Wayne Huebner, conducting research related to piezoelectric and dielectric ceramics. After completing his undergraduate degree, he gained industrial experience with Philips Display Components Company as a Glass Engineer and later as a Senior Process Engineer responsible for numerous glass and ceramic components and processes in the CRT production facility. After his initial experience with Philips, Dan made a career change and began work at AlliedSignal Federal Manufacturing & Technologies (later changed to Honeywell Federal Manufacturing & Technologies under the same ownership) where he was responsible for high voltage ceramic capacitor development, multichip module development and production, and numerous other R&D and production responsibilities. While employed at Honeywell, he completed a Master of Science in Mechanical and Aerospace Engineering with Materials Science minor at the University of Missouri – Columbia in 2003. His master's degree research was on the Characterization of Y_2O_3-doped $SrTiO_3$ Capacitors. Dan worked in the role of the Electrical Products Center of Excellence since 2012 and was named an Engineer Fellow at Honeywell in 2015. He received his Doctor of Philosophy in Ceramic Engineering from Missouri University of Science and Technology in July 2021.