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EMI characterization for power supplies and machine learning based modeling in EMC/SI

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EMI CHARACTERIZATION FOR POWER SUPPLIES AND MACHINE LEARNING BASED MODELING IN EMC/SI

by

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ABSTRACT

Signal integrity (SI) and electromagnetic interference (EMI) are essential for consumer electronics and high-speed server applications. It is necessary to do EMI and SI modeling at the design stage. In this research, several modeling approaches for EMI and SI problems are proposed. By using measurement-based modeling method, the mechanism of conducted emissions (CE) on ac to dc power supplies in an LED TV is analyzed. A system-level transient simulation model is built to predict the conducted emission (CE). To characterize the equivalent dipole moment sources in RFI and EMI problems, a dipole source reconstruction method based on machine learning techniques is proposed. The picture of the electromagnetic field is fed to the convolutional neural network, and the CNN performs a multi-label classification to determine all types of dominant dipole moments. The CNN also generates a class activation map, which indicates the locations of each type of present dipole moment. By using the integer programming method, a PCB stack-up design method is proposed. In high-speed PCB designs, a design with 30 layers or more is not uncommon and there are many logical design constraints that need to be considered. The constraints are converted to mathematical inequalities using the integer programming technique. Then an integer program solver is called to get all possible combinations. The number of possible combinations gets large as the number of layers increases, and the proposed method is much more efficient than brute-force searching. After a nominal design is picked, a searching algorithm based on integer programming is further used to find corner cases by considering the manufacturing variations.

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1. INTRODUCTION

SI/EMI problems are more and more important in electrical systems as the speed getting higher and design density getting larger. Three SI/EMI modeling problems are discussed in this research.

In Section 2, the conducted emissions (CE) on ac to dc power supplies in an LED TV is analyzed and modeled. Power factor correction and resonant converters are widely used in ac to dc power supplies. The switching noise of power converters is the main noise source for conducted EMI. The parasitic capacitors between the board layout and chassis form a current path for common mode noise. The differential mode noise is naturally caused by the normal operation of the converters. Mode conversion can happen when one diode is forward biased while other three are reversed biased, and this mode conversion is the dominant mechanism of DM EMI at high frequencies for this LED TV. The current paths of both DM and CM EMI noise are analyzed and modeled in full-wave simulations. The switching noise of converters are modeled using circuit models. A system-level transient simulation model is built to predict the conducted emission (CE). The predicted DM and CM CE show good agreement with measurements.

In Section 3, a dipole source reconstruction based on machine learning techniques is proposed. In the study of RFI and EMI problems, equivalent dipole moments are widely used to reconstruct the noise source. The coupled voltage or coupled power can be calculated from the reconstructed dipole sources. A machine learning based dipole source reconstruction method using convolutional neural networks (CNN). The picture of the electromagnetic field is fed to the convolutional neural network, and the CNN performs a

multi-label classification to determine all types of dominant dipole moments. The CNN also generates a class activation map, which indicates the locations of each type of present dipole moment. With the types and locations of the dipoles known, the magnitude and phase of each dipole can be obtained from LSQ or other optimization methods. With a pre-trained convolutional neural network model, the proposed method is validated with simulated and measured field patterns.

In Section 4, an integer programming application for PCB stack-up design is discussed. In high-speed PCB designs, a design with 30 layers or more is not uncommon and there are many logical design constraints that need to be considered. A method based on integer programming is proposed to convert logical constraints to pure mathematical inequalities. Then an integer program solver is called to get all possible combinations. The number of possible combinations gets large as the number of layers increases, and the proposed method is much more efficient than brute-force searching. After a nominal design is picked, another searching algorithm based on integer programming is proposed to find corner cases by considering the manufacturing variations. First the searching range is narrowed down by adding constraints in the integer program, then 2D cross-section simulations are launched in parallel to find the corner cases. The accuracy and efficiency of proposed method are validated with practical PCB designs.

2. ANALYSIS AND MODELING OF CONDUCTED EMISSION FROM AN LED TV POWER SUPPLY

AC-DC power supplies are widely used in consumer power electronic devices. Power factor correction (PFC) and dc-dc converters are two important parts in ac-dc power supplies to achieve high efficiency. The PFC shapes the input current of power supplies to makes it in phase with the input voltage and minimize its line-frequency harmonics, thus achieving a high power factor (PF) [1], [2]. In this case, the power loss is minimized and the interference with other devices being powered from the same source is also minimized.

PFC boost converters can work in three conditions: continuous conduction mode (CCM), critical conduction mode (CRM) and discontinuous conduction mode (DCM). In lower power applications like power adaptors and televisions (TV), CRM PFC boost converters are popular because they are inexpensive, efficient, and relatively simple to use. The output of the PFC is further converted to the desired voltage level by a dc-dc converter in the second stage. Resonant converters have less switching loss and high power density characteristics than pulse-width modulation converters [3], [4]. Hence, resonant converters are widely used as dc-dc converters in commercial products.

Electromagnetic Compatibility (EMC) standards such as EN55032 are defined to limit the electromagnetic interference (EMI) noise levels coming out from real products. EMI filters are usually placed inside power supplies to meet the EMC standards [5]-[9]. A lot of research and investigations have also been done in this area [10]-[16]. Knowing the EMI characteristics and being able to model the EMI noise from power supply converters can help reduce the time and cost required for a product design.

The overall system diagram of the power supply is shown in Figure 2.1. The power supply uses a two-wire power cord. The power supply consists of two stages: a CRM boost PFC converter and an LLC resonant converter. The operating frequency range of the boost PFC converter is from 190 to 250 kHz, and the operating frequency of the LLC resonant converter is 78 kHz. The output of the LLC resonant converter is referenced to a large metal chassis with a size of 48 in by 28 in in the TV.

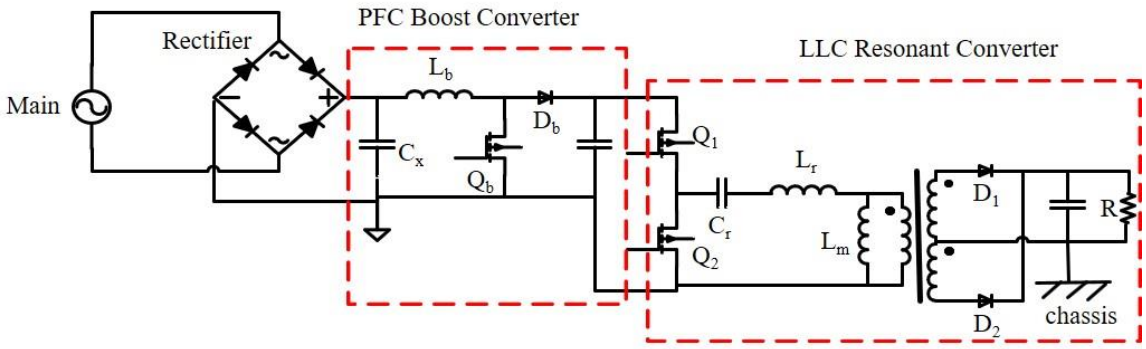

Figure 2.1. System diagram of the power supply for the LED TV.

The conducted EMI from the power supply on an LED TV is measured by an oscilloscope and analyzed by the joint Time-Frequency analysis using the short-time Fourier transform (STFT) up to 30 MHz. Dominant noise sources and coupling mechanisms are identified and analyzed. A transient circuit model is built to model the entire system and the noise current paths. The conducted EMI noise up to 30 MHz is predicted from the transient simulation.

2.1. MEASUREMENT OF THE CONDUCTED EMI NOISE

The measurement setup is shown in Figure 2.2. The distance between the TV and the vertical earth ground plane is 40 cm. The height of the wooden table is 80 cm. The power supply board is mounted on the TV metal chassis which is floating from the earth ground. The power supply board is a two-layer printed circuit board (PCB) where the top layer is for components and the bottom layer is for routing. The distance between the board and the metal chassis is 6 mm. Two measurement ports for the line and neutral of the line impedance stabilization network (LISN) are connected to two channels of an oscilloscope.

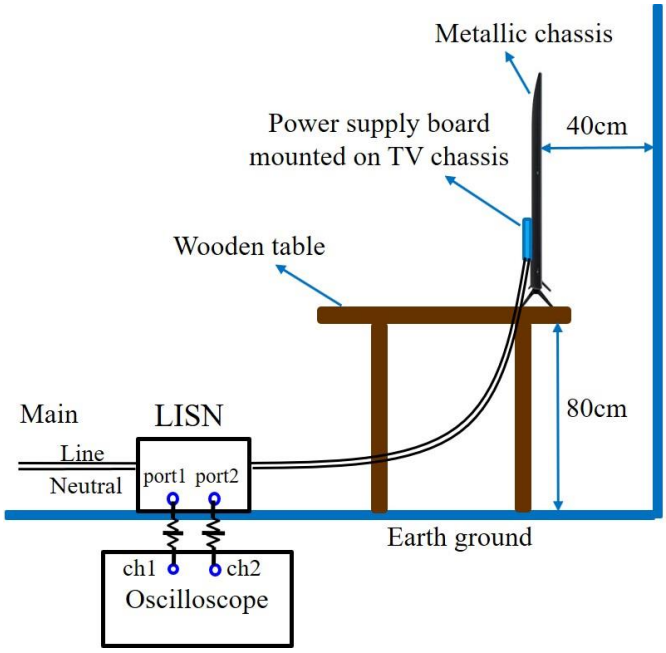

Figure 2.2. Measurement setup of the conducted EMI noise.

The time domain waveforms of the two channels are recorded with an adequate time length. The DM and CM voltages V_{dm} and V_{cm} are calculated as:

$$V_{dm} = \frac{V_1 - V_2}{2} \tag{1}$$

$$V_{cm} = \frac{V_1 + V_2}{2} \tag{2}$$

where V_1 and V_2 are the measured voltages from the two measurement ports of the LISN.

An EMI receiver model is developed to convert time domain noise waveforms to CE spectrums including the characteristics of the Gaussian window filter and detector of an EMI receiver [17]. Based on CISPR16 standard, the 6 dB bandwidth of the filter, which is also called as the resolution bandwidth (RBW), is allowed to be in between 8 kHz and 10 kHz [18]. Time domain waveforms are first converted to time-varying spectrums by the STFT. Then, detector models are used to evaluate the peak, average or quasi-peak values of time-varying spectrums. The structure of the EMI receiver model is shown in Figure 2.3. [19].

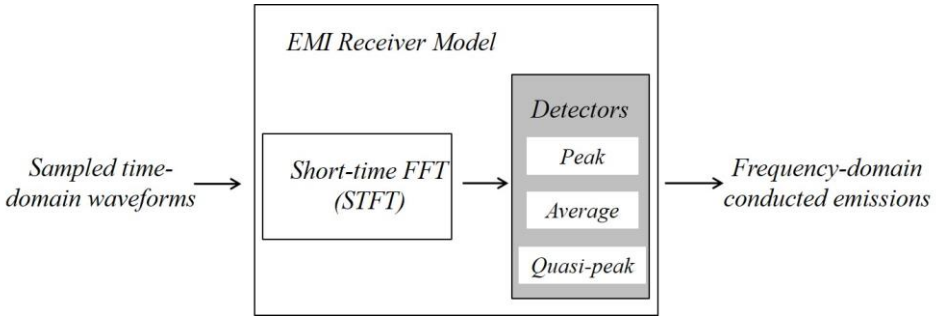

Figure 2.3. The diagram of the EMI receiver model.

The characteristic of the Gaussian filter is shown in Figure 2.4.

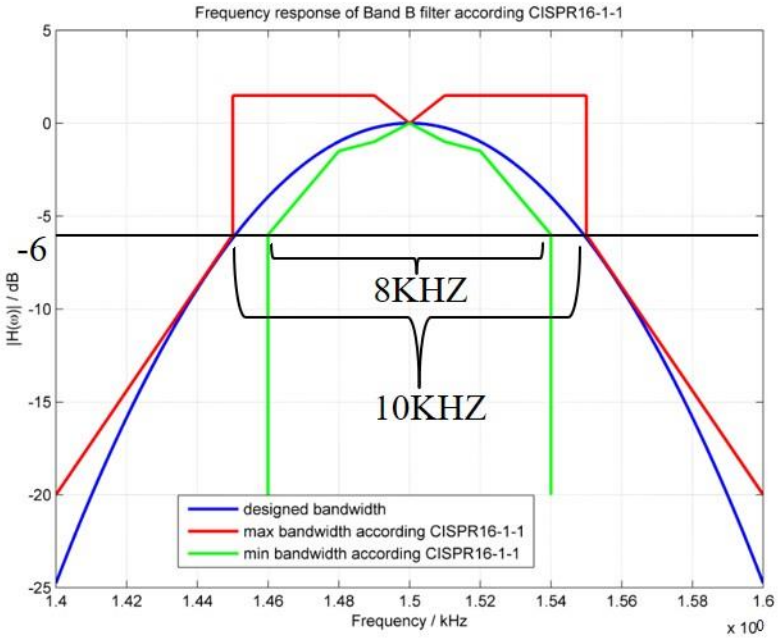

Figure 2.4. The Gaussian filter in the EMI receiver model.

2.2. ANALYSIS OF EMI CHARACTERISTICS

2.2.1. Analysis of CM EMI Noise. The time-varying spectrums of the measured CM EMI noises are shown in Figure 2.5 and Figure 2.6. Figure 2.5 shows the time-varying spectrum below 1 MHz, Figure 2.6 shows the time-varying spectrum from 1 MHz to 3 MHz and the peak values of the time-varying spectrum up to 30 MHz is presented in Figure 2.7.

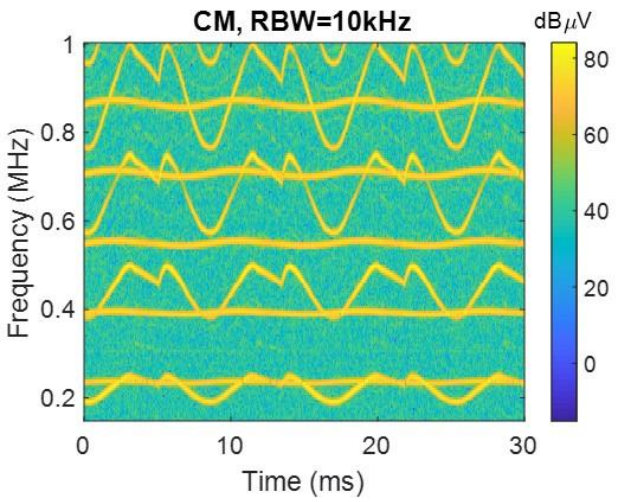

Figure 2.5. Measured CM conducted EMI spectrogram from 150 kHz to 1 MHz.

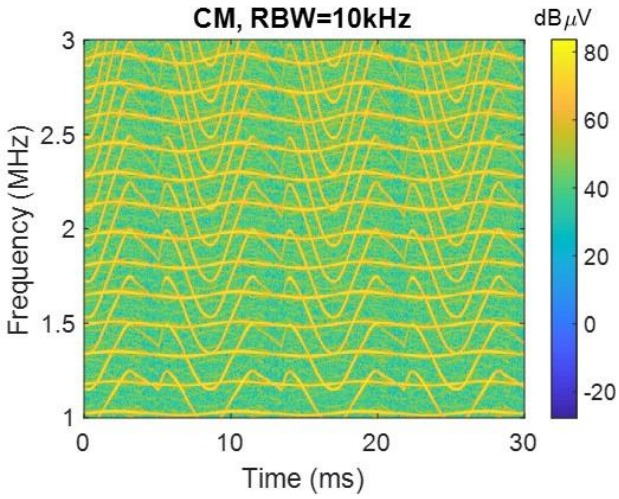

Figure 2.6. Measured CM conducted EMI spectrogram from 1 MHz to 3 MHz.

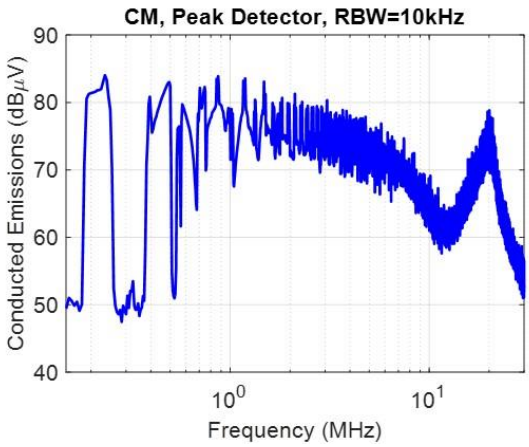

Figure 2.7. CM EMI noise in peak detector.

From the time-varying spectrums, it can be seen that there are mainly two groups of frequency components. The first group is changing periodically in time domain, which corresponds to the switching frequency of the boost PFC converter and its harmonics. The second group is almost constant and does not vary a lot with respect to time, which corresponds to the switching frequency of the LLC resonant converter and its harmonics. Therefore, both the boost PFC converter and the LLC resonant converter are the noise sources of CM conducted emission.

Current paths for CM EMI noise are shown in Figure 2.8. The CM EMI noise is caused by the parasitic capacitances between the PCB traces and the metallic chassis of the TV and the parasitic capacitance between the metallic chassis of the TV and the earth ground plane of the test setup. The important parasitic capacitances between the PCB traces and the metallic chassis of the TV include the parasitic capacitance between the drain node of the switching MOSFET of the boost PFC converter and the metallic chassis of the TV; the parasitic capacitance between the drain node of the low-side switching MOSFET,

which is also the source node of the high-side switching MOSFET, of the LLC resonant converter and the metallic chassis of the TV; the parasitic capacitance between the primary and secondary sides of the transformer of the LLC resonant converter; and the parasitic capacitance between the metallic chassis of the TV and the earth ground plane of the test setup.

The current path consisting of metallic chassis of the TV, vertical earth ground wall, horizontal earth ground, LISN and the power cable forms a large loop. There is a large inductance associated with this loop. This inductance and the total capacitance in the loop form a serial LC resonance. From the CM EMI results using peak detector, a serial resonance is observed at 20 MHz.

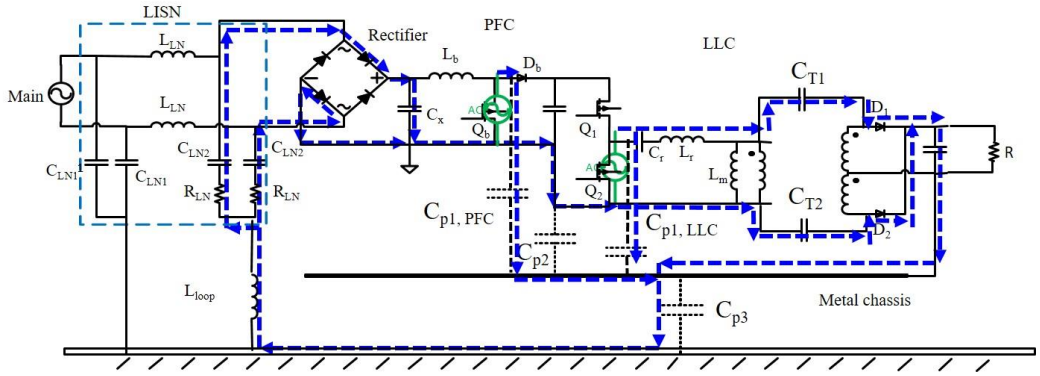

Figure 2.8. Major paths of the CM EMI noise current.

2.2.2. Analysis of DM EMI Noise. The time-varying spectrums of the measured DM EMI noises are shown below. Figure 2.9 shows the time-varying spectrum below 1 MHz, Figure 2.10 shows the time-varying spectrum from 1 MHz to 3 MHz, and the peak

values of the time-varying spectrum up to 30 MHz is presented in Figure 2.11. For fundamental switching frequency range of the PFC, the DM noise level is much larger than the CM noise level and the PFC noise is dominant. For the frequency range above 1 MHz, the DM noise level is lower than the CM noise.

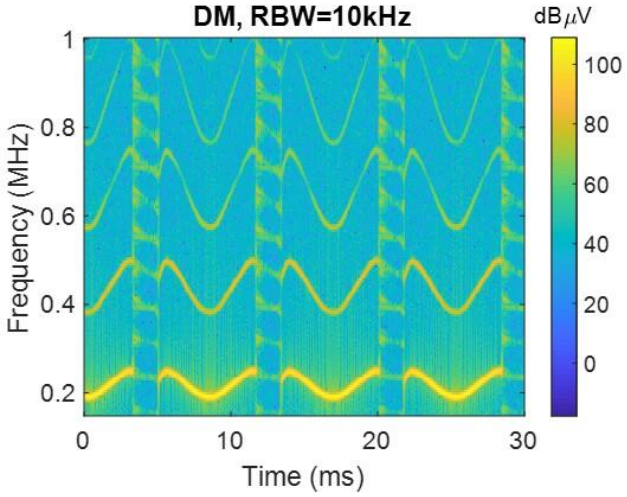

Figure 2.9. Measured DM conducted EMI spectrogram from 150 kHz to 1 MHz.

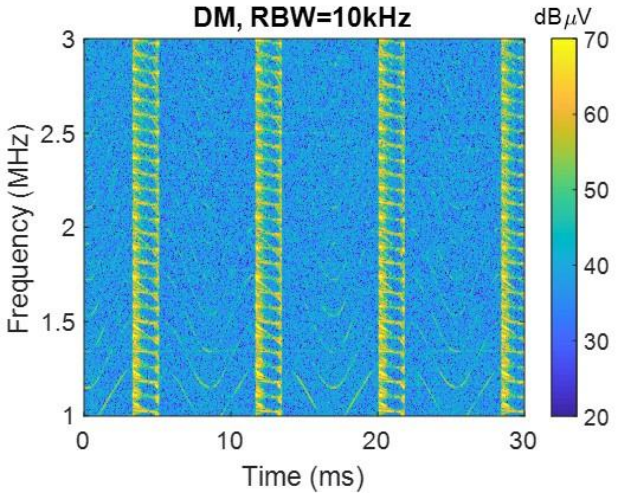

Figure 2.10. Measured DM conducted EMI spectrogram from 1 MHz to 3 MHz.

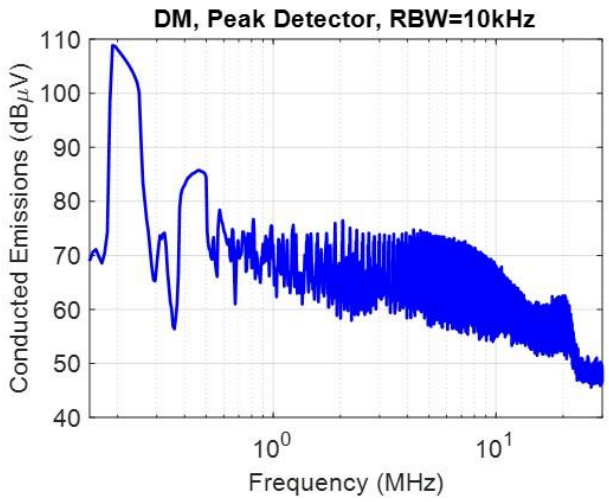

Figure 2.11. DM EMI noise in peak detector.

The DM EMI spectrum characteristics vary with time and are related to the status of the rectifier. The line voltage is 120 V, 60 Hz ac voltage. The absolute input voltage and output voltage of the rectifier are plotted in Figure 2.12.

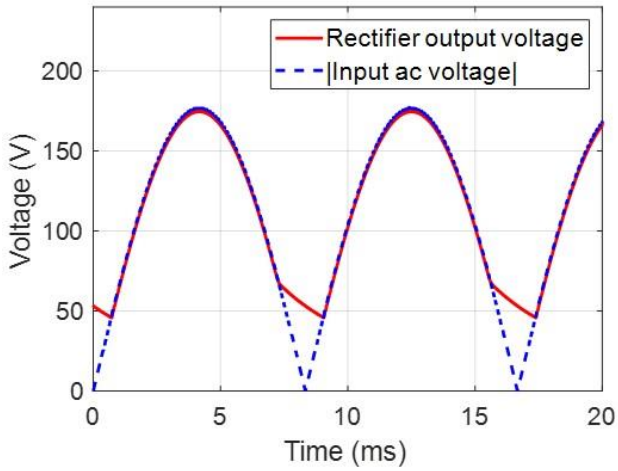

Figure 2.12. Time domain waveforms of the rectifier output voltage and input voltage.

Below 500 kHz, DM EMI is strong when the rectifier is on and the main noise source is PFC. However, DM EMI above 500 kHz gets large when the rectifier is off, which means at most 1 diode in the rectifier is on. When the rectifier is on, DM EMI noise is mainly caused by the differential current loop during normal switching actions as shown in Figure 2.13. Since the LLC switching noise will be greatly attenuated by the boost inductor and the output capacitor of the PFC boost converter, PFC is the dominant noise source. During the time interval that absolute line voltage is smaller than the voltage at PFC input, at most one diode in the rectifier is on. When there is one diode on in the rectifier, the current can also flow through the parasitic capacitor between board layout and TV chassis and then through this one forward biased diode as shown in Figure 2.14. Since the boost inductor node and signal ground node are not symmetric to earth ground, voltages across two diodes in the bridge rectifier are different. Two diodes are turned from forward biased to reversed biased at different times. In this situation, mode conversion happens, and DM CE noises at the LISN can be observed.

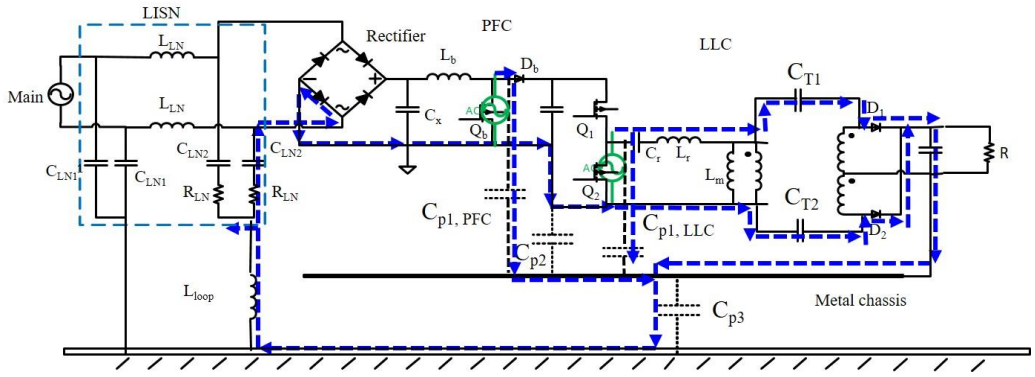

Figure 2.13. DM EMI current paths when only one diode is on.

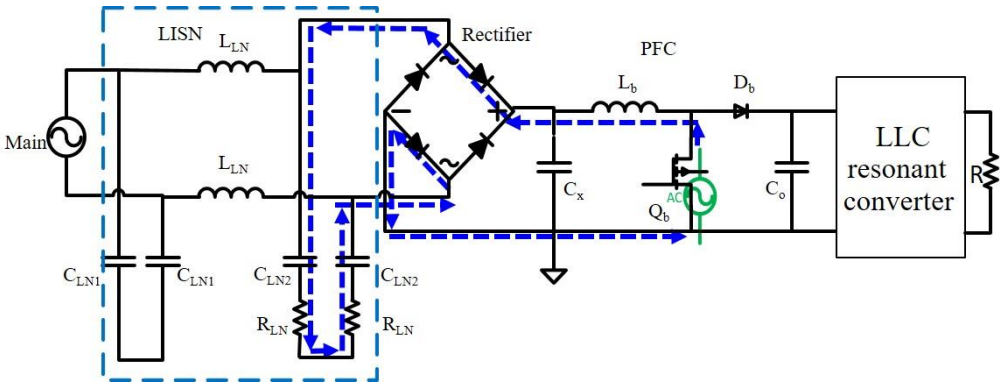

Figure 2.14. DM EMI current paths when two diodes are on.

The summary of the EMI mechanism is shown in Table 2.1:

Table 2.1. EMI mechanism summary.

	Mechanisms
Differential mode CE	1. From the normal working condition of PFC. 2. Mode-conversion when the rectifier is off.
Common mode CE	1. The parasitic capacitances between the board layout and TV chassis. 2. The parasitic capacitance between the primary and secondary side of the transformer. 3. The loop inductance and total capacitance can form an LC resonance.

2.3. EMI MODELING

A transient model is built to predict conducted EMI for this DUT.

2.3.1. Parasitic Parameters Extraction. The parasitic parameters play an important role in EMI noise of the DUT. The parasitic capacitors between PCB layout and metal chassis are extracted using Ansys Q3D as shown in Figure 2.15 [19]. The simulated results are as follows: $C_{p1,\,PFC}$ = 4 pF, $C_{p1,\,LLC}$ = 1 pF, C_{p2} = 36 pF.

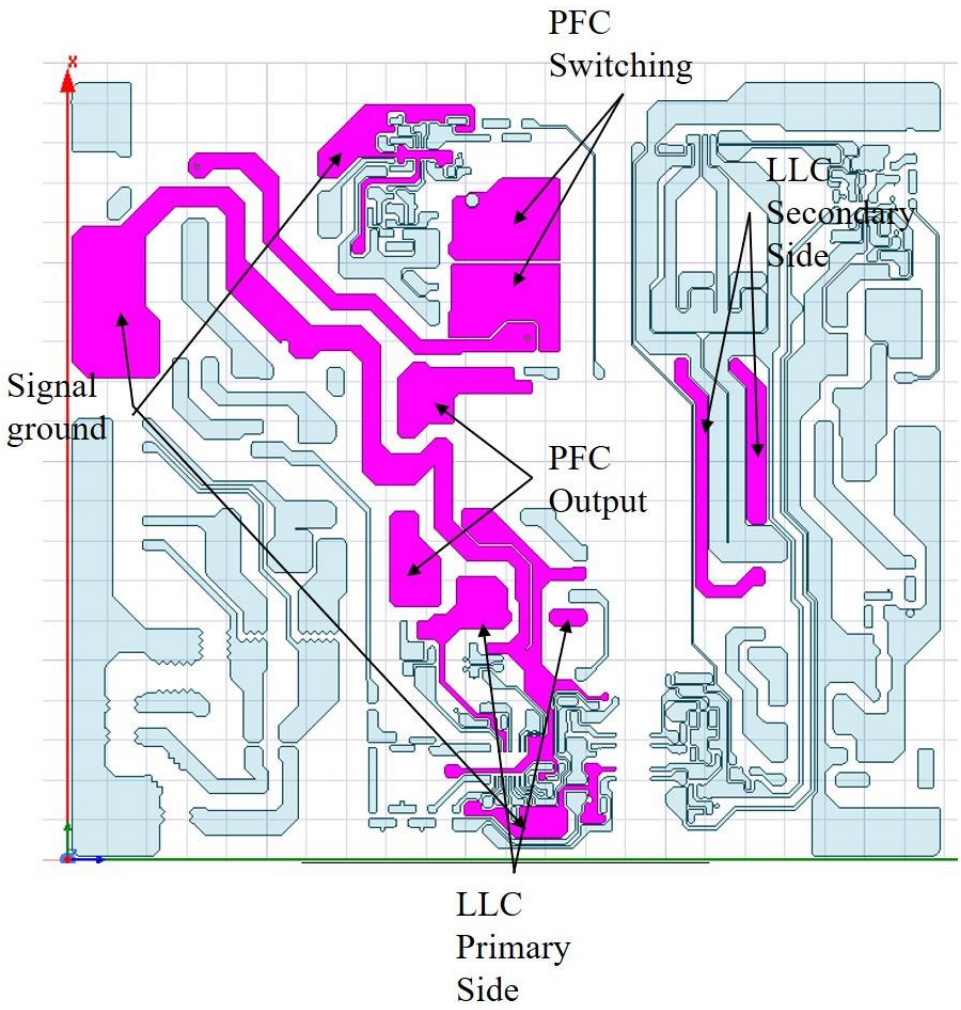

Figure 2.15. Q3D simulation model for parasitic capacitance extraction.

The loop inductance and the parasitic capacitor between TV chassis and vertical ground are simulated using Ansys HFSS [20]. The simulation model for loop impedance is shown in Figure 2.16. The simulated result is shown in Figure 2.17. At low frequencies, the impedance is dominated by the capacitance between the metallic chassis and the vertical ground wall. There is a resonance at 13 MHz, and this resonance is associated with the chassis to ground wall capacitance and the loop inductance. From simulated Z_{11} result, C_{p3} is 70 pF and L_{loop} is 2.1 µH.

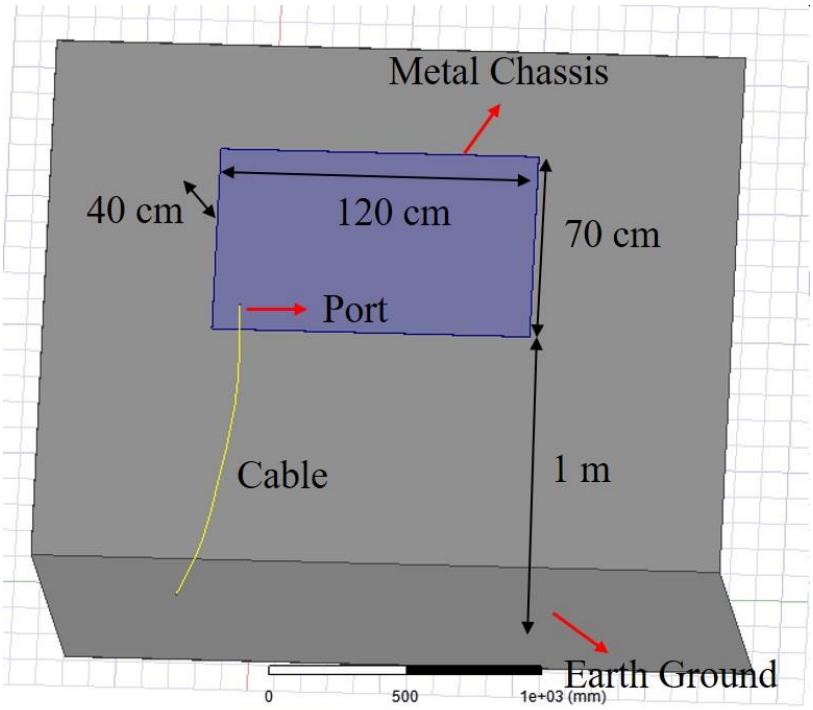

Figure 2.16. HFSS simulation model for C_{p2} and loop inductance extraction.

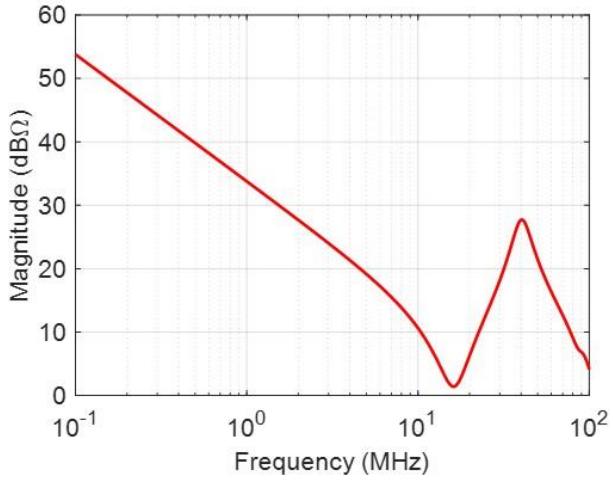

Figure 2.17. Simulated impedance result.

2.3.2. EMI Prediction by Transient Simulation. A system-level transient simulation model is built to predict the conducted emissions of the power supply. The LISN model, PFC model, LLC model and parasitic components on the current path are included in the transient simulation. In the LISN model, L_{LN} = 50 µH, C_{LN1} = 1µF, C_{LN2} = 0.1 µF, R_{LN} = 50 Ω. For PFC, L_b = 238 µH, C_x = 0.82 µF and C_o = 82µF.

In PFC boost converter, the switching is controlled so that the average inductor current follows the input voltage of the PFC, which is usually the voltage after the rectifier. The inductor current increases when the switch is turned on and decrease when the switch is turned off. For a CRM PFC, the switch is turned from off to on when the inductor current reaches zero. Since the output voltage of the PFC boost converter is almost a constant while the input voltage after the rectifier is changing in half line period, the duty cycle is varying in half line period. For a CRM PFC with a constant on-time, the off-time of the switch is varying, thus making the switching frequency vary in half line period. The PFC is

switching at the maximum frequency when the input voltage reaches the minimum value and switching at the minimum frequency when the input voltage is at its maximum level. An accurate switching frequency is very important in a CRM PFC model as the switching noise is the main noise source of the conducted EMI.

To accurately model the time domain switching waveform, the control circuit of a CRM PFC is built as shown in Figure 2.18. When the power switch turns on, the inductor current ramps up until the comparator signal reaches the threshold. At this point the comparator output state changes and the power switch is turned off. Then the inductor current starts to ramp down until it reaches zero. The zero current detection (ZCD) circuit measures the voltage across the inductor. When the inductor current reaches zero, the voltage will also be zero and be detected by ZCD circuit. The switch is turned on again at this point.

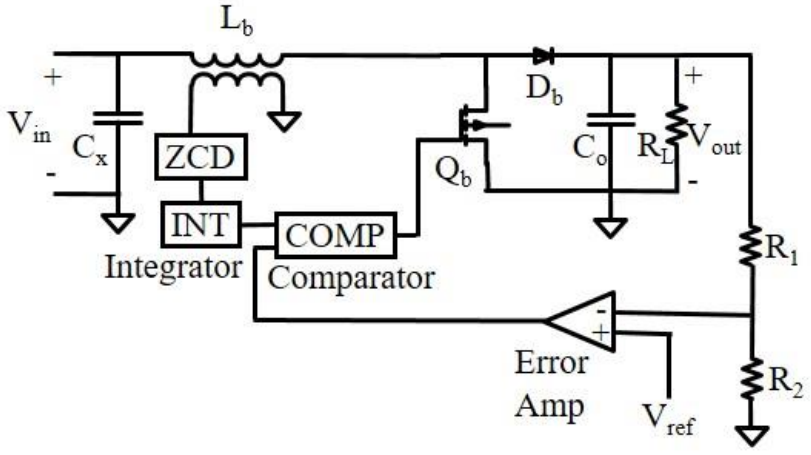

Figure 2.18. Control circuit of a CRM PFC.

The complete transient simulation model for PFC is shown in Figure 2.19. The switching frequency of the CRM PFC is controlled by a voltage-mode control scheme. The control circuit is built to accurately model the time domain switching waveform [21].

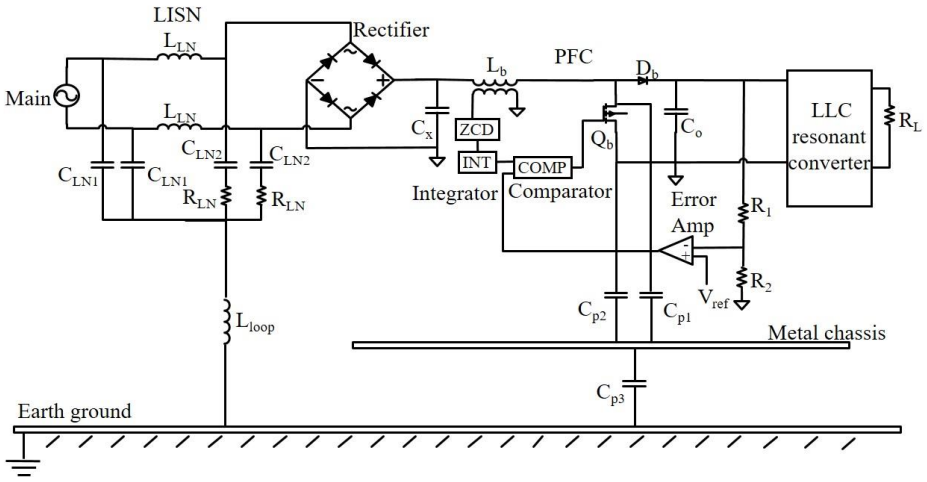

Figure 2.19. Transient simulation model for CRM PFC boost converter.

To validate the PFC is working as expected, the simulated inductor current, PFC input voltage and control signal waveforms are shown in Figure 2.20 and Figure 2.21. It can be seen that the inductor current is in phase with PFC input voltage and the envelope of the inductor current has the same shape as the input voltage, thus achieving a high power factor. The duty cycle and switching frequency of the PFC are changing during half line period. The on-time is controlled to be 2.2 μs. So the PFC is working in CRM with a constant on-time.

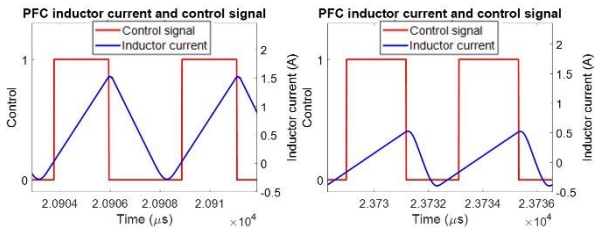

Figure 2.20. The inductor current waveform and control signal.

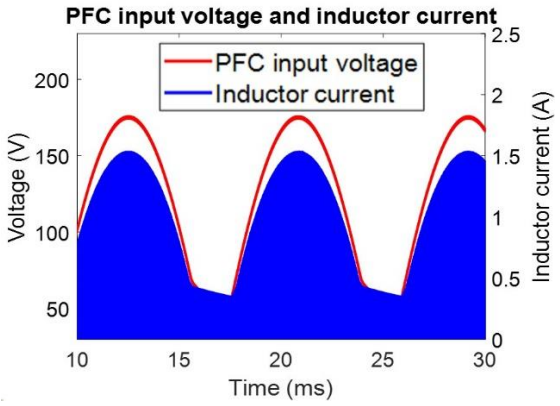

Figure 2.21. PFC input voltage and inductor current.

The PFC switching waveform is also measured using high-voltage differential probe MicSig DP10013. Simulated switching spectrum matches well with measured switching spectrum as shown in Figure 2.22.

In LLC resonant converter, C_r = 27 nF, L_m = 605 μH. The switching frequency of LLC resonant converter is 78.5 kHz. The transformer parasitics are modeled by a two-capacitor model [23]. Two capacitors, C_{T1} and C_{T2} are 3.5 pF and 2.5 pF, respectively. The transient simulation model for LLC is shown in Figure 2.23.

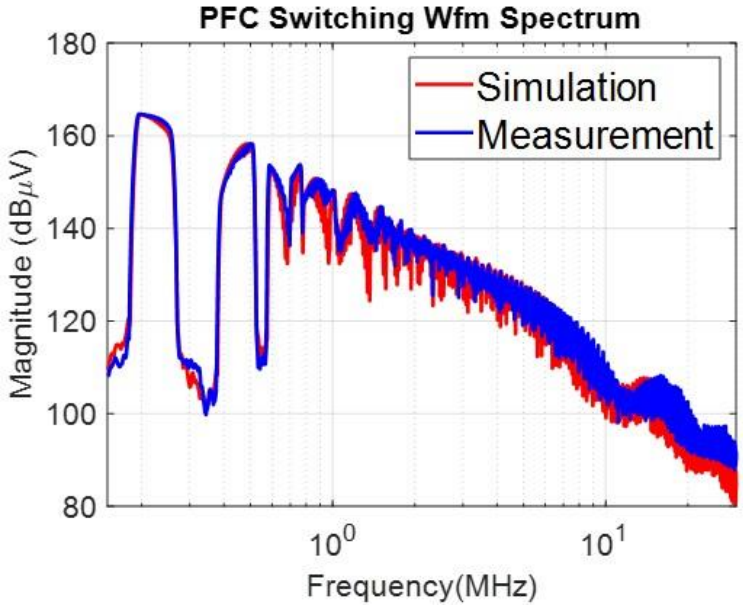

Figure 2.22. PFC switching signal spectrum.

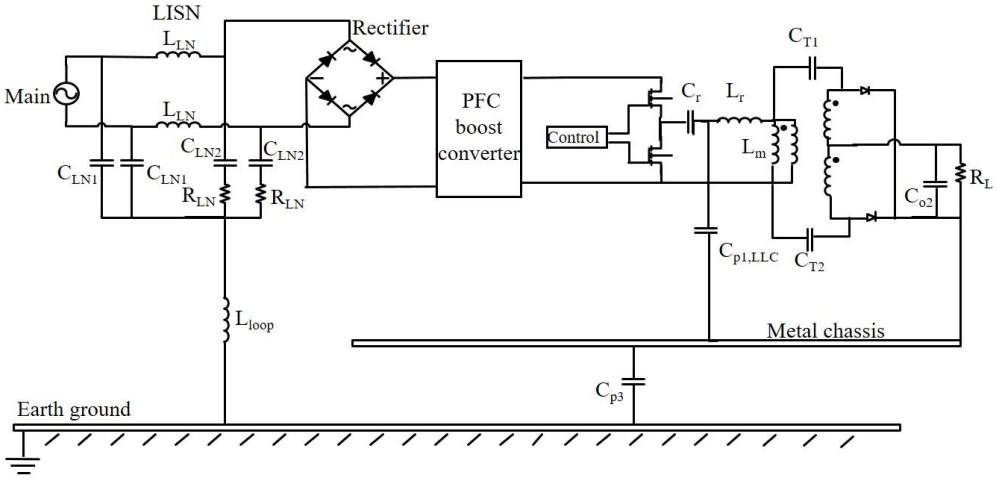

Figure 2.23. Transient simulation model for LLC resonant converter.

The comparison of switching noise spectrum between simulation and measurement is shown in Figure 2.24. Then these two parts of the power supply are combined as the

complete transient simulation model for CE prediction. The voltage waveforms across two LISN resistors are simulated. The simulated noise waveforms are converted to frequency domain conducted emissions by the developed EMI receiver model. Simulated CM EMI noise spectrum agrees well with measurement results to 30 MHz and the resonance at 20 MHz is captured by the simulation model as shown in Figure 2.25 and Figure 2.26. Figure 2.27 and Figure 2.28 shows the DM EMI noise spectrum comparison between simulation and measurement results. Good correlation is achieved up in DM conducted emissions to 15 MHz. The DM CE is attenuated by the PFC boost inductor and its level is getting lower above 15 MHz.

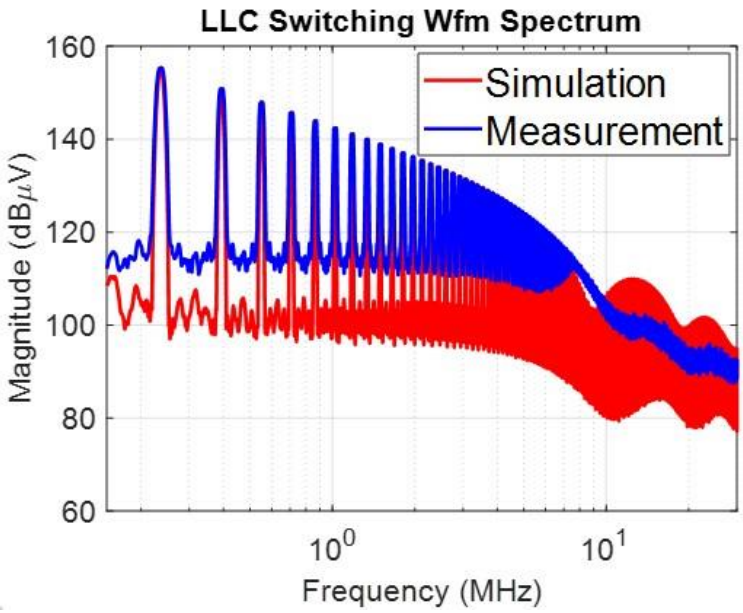

Figure 2.24. LLC switching signal spectrum.

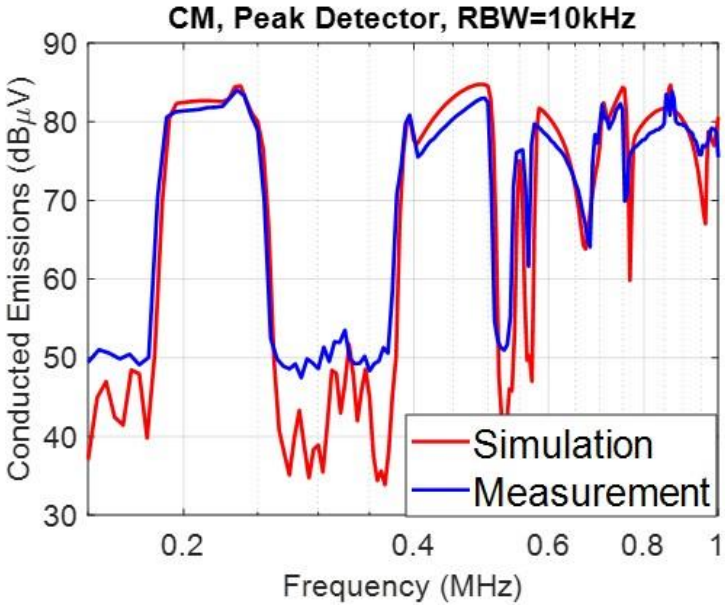

Figure 2.25. CM EMI spectrum comparison below 1 MHz.

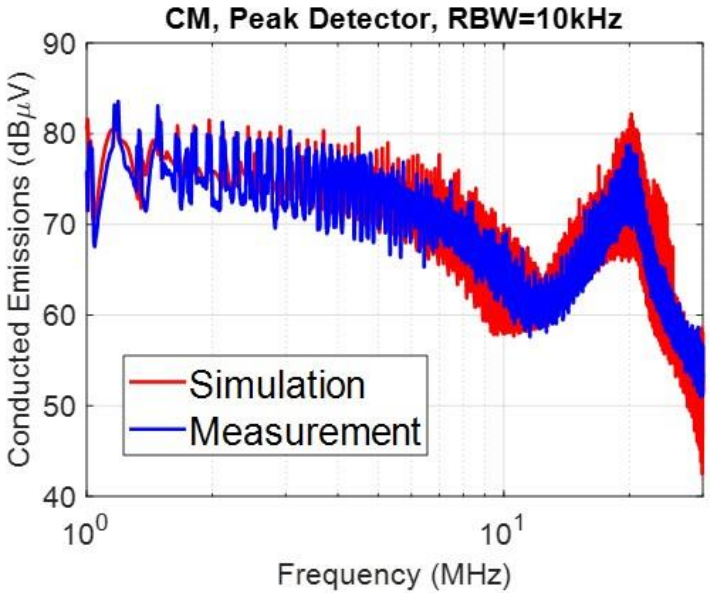

Figure 2.26. CM EMI spectrum comparison above 1 MHz.

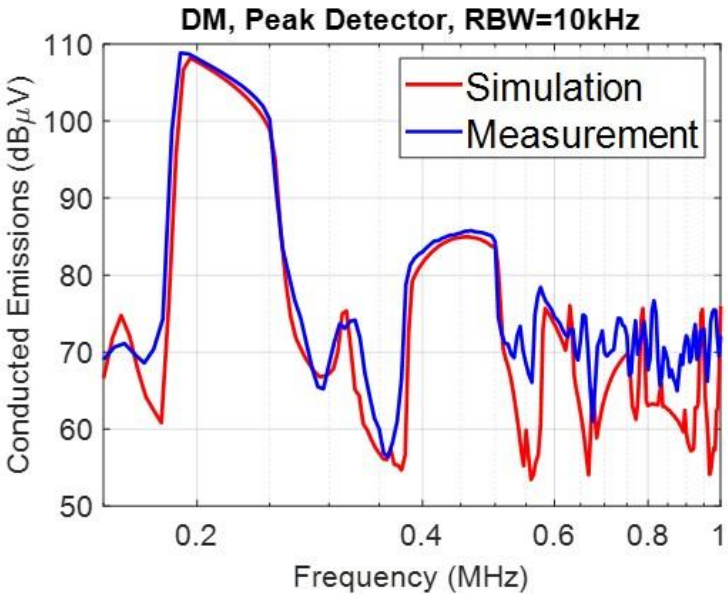

Figure 2.27. DM EMI spectrum comparison below 1 MHz.

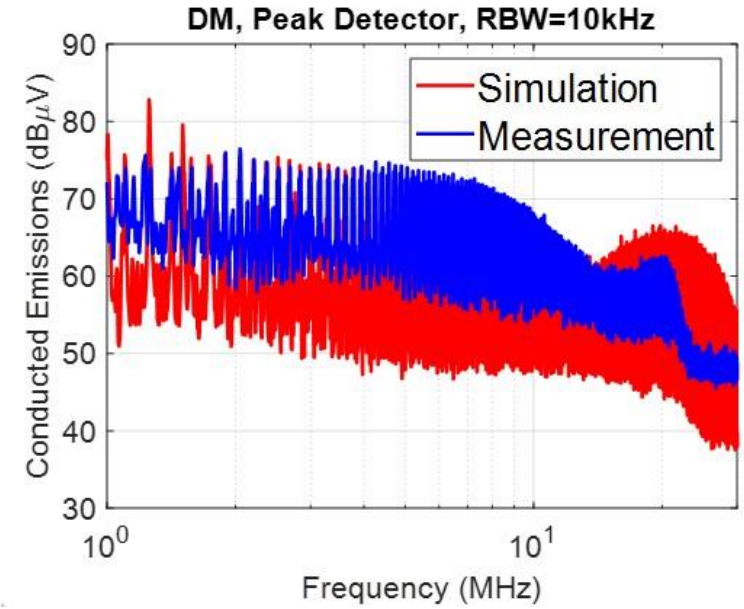

Figure 2.28. DM EMI spectrum comparison above 1MHz.

2.3.3. The Effect of the Ground Filter. A ground filter is usually placed between the signal ground and the metal chassis to reduce conducted emissions. A typical design of the ground filter consists of a ferrite and a capacitor. The comparisons of CM and DM conducted emissions are shown in Figure 2.29, Figure 2.30, Figure 2.31 and Figure 2.32, respectively. The transient simulation model results agree well with measurement results. The ground filter reduces the CM EMI noise and shifts the resonance frequency. It can also be seen DM conducted emissions don't change with the ground filter at low frequencies. But at higher frequencies, the ground filter also reduces DM conducted emissions, which further proves that mode conversion is the dominant mechanism for DM EMI noise above 700 kHz.

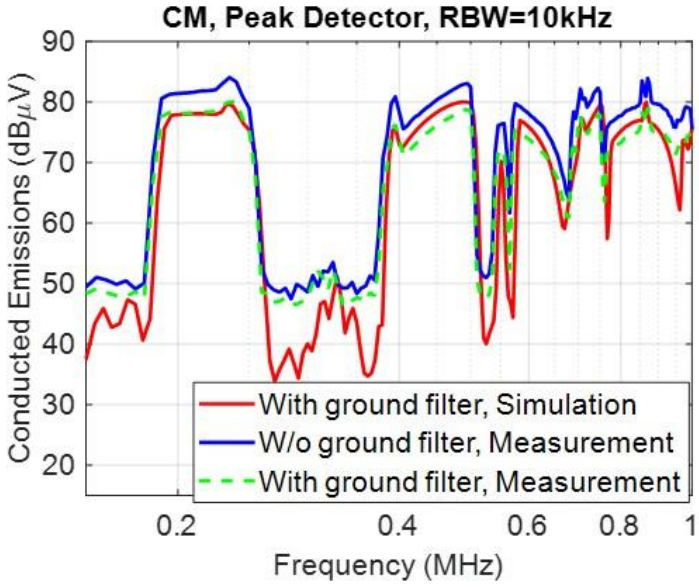

Figure 2.29. CM EMI spectrum comparison below 1 MHz, with filter.

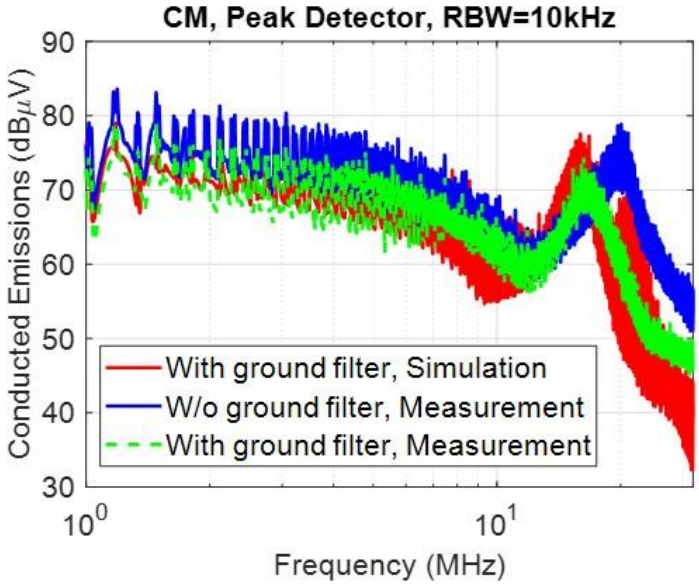

Figure 2.30. CM EMI spectrum comparison above 1 MHz, with filter.

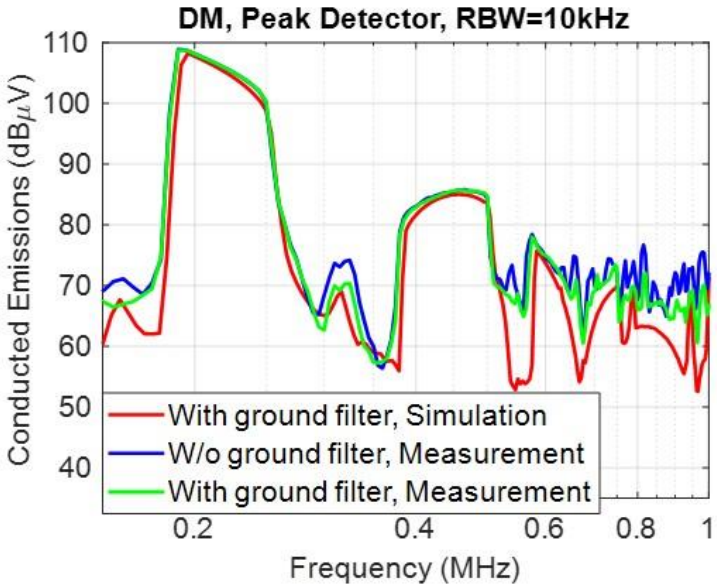

Figure 2.31. DM EMI spectrum comparison below 1 MHz, with filter.

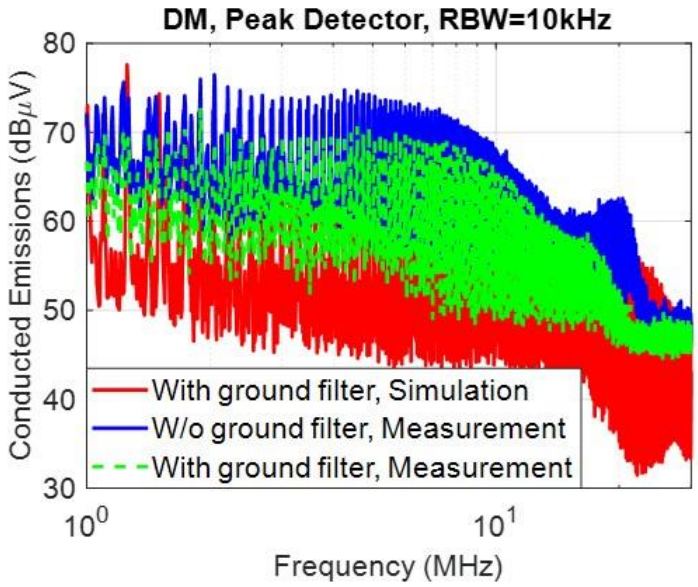

Figure 2.32. DM EMI spectrum comparison above 1 MHz, with filter.

3. DIPOLE SOURCE RECONSTRUCTION BY CONVOLUTIONAL NEURAL NETWORKS

As the data rate in electronic devices gets higher, radio frequency interference (RFI) problems are becoming more significant. In the study of RFI problems, equivalent dipole moments are widely used to reconstruct the noise source [24], [25]. The coupled voltage or coupled power can be calculated from the reconstructed dipole sources. Designers can also improve the design to mitigate the coupling based on the equivalent source models.

Since dipole sources reconstruction can help the analysis and design significantly, various methods have been developed to extract dipole moments. With a uniform array of electric and magnetic dipole moments predefined, the least square (LSQ) method can be used to solve the magnitude and phase of each dipole moment [26]. However, this method is sensitive to measurement noise and the solution may be non-physical when the size of the dipole array gets large. Optimization methods such as Genetic algorithm are also common solutions to this problem [27], [28]. But the convergence and computation time of optimization methods usually depend on the initial value. A machine learning method based on support vector machine (SVM) have been used to classify the dominant dipole type from the image of the near-field pattern [29]. The location of the dipole is further determined from auto-correlation calculation after the type is identified. This method shows the capability of pattern recognition techniques in field pattern classification and dipole source reconstruction.

A machine learning based dipole source reconstruction method using convolutional neural networks (CNN) is proposed. CNNs are widely used to process 2-D grid data such as images. CNNs have also been used to solve electromagnetic problems [30]. The picture

of the electromagnetic field is fed to the convolutional neural network, and the CNN performs a multi-label classification to determine all types of dominant dipole moments. The CNN also generates a class activation map, which indicates the locations of each type of present dipole moment [9]. With the types and locations of the dipoles known, the magnitude and phase of each dipole can be obtained from LSQ or other optimization methods.

3.1. MACHINE LEARNING BASED DIPOLE RECONSTRUCTION

Dipole moments are the most basic radiation sources. An infinitely small electrical current segment forms an electrical dipole (P dipole). An infinitely small current loop forms a magnetic dipole (M dipole). There are six types of basic dipole moments based on the orientations as shown in Figure 3.1. The near field of each basic dipole moment can be calculated from analytical formulas. Each basic dipole moment also has its unique near field patterns. The feature of the pattern can be used to classify the type of the dipole moment by machine learning algorithms.

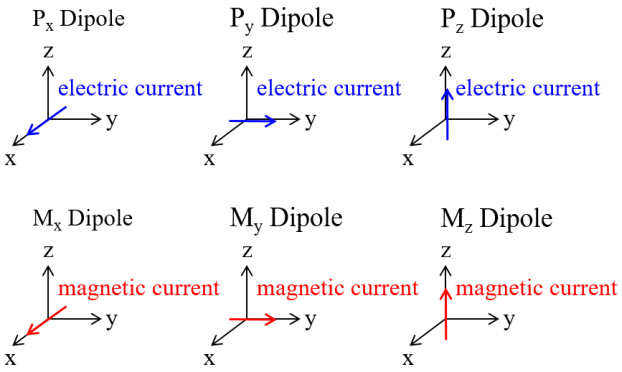

Figure 3.1. Six types of basic dipole moments.

3.1.1. Convolutional Neural Network for Multi-Label Classification. In machine learning and computer vision, the convolutional neural network is a typical neural network used for image classification analysis [31]. In this work, a set of field pattern pictures generated from analytical formulas is given as the training dataset. Each picture is labeled with the categories of the present dipoles. If a type of dipole moment exists in the field pattern, this category is labeled with 1, otherwise it is labeled with 0. As a result, the label for each picture is a 1 by 6 array and each element in the array is either 1 or 0. In convolutional neural networks, there are usually a few convolutional layers with rectified linear unit (ReLu) function as the activation function and pooling layers. In multi-class classification, softmax function is usually used as the activation function at the last stage as shown in Figure 3.2. In this case, only 1 type of dipole can be recognized.

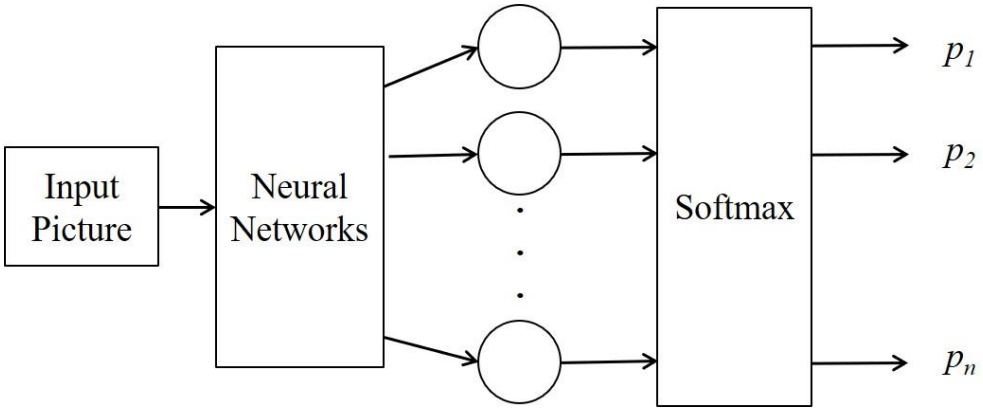

Figure 3.2. Multi-class classification.

Since it's possible that multiple types of dipole moments are present, different types of dipole moments are not exclusive and a multi-label classification task is desired. Therefore, the activation function of the last layer is the sigmoid function instead of the softmax function, which is widely used as the activation function in multi-class classification tasks as shown in Figure 3.3. The sigmoid function is shown as follows:

$$sigmoid(x) = \frac{1}{1+e^{-x}} \tag{3}$$

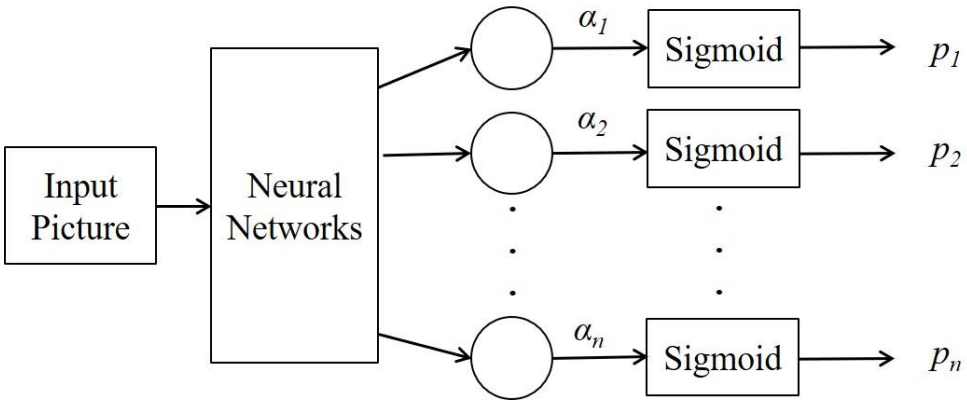

Figure 3.3. Multi-label classification.

The output of the sigmoid function can be interpreted as the probability of the input belonging to this category. The loss function is the cross entropy between the output logits and the corresponding labels as shown in (4),

$$\begin{aligned} cross\_entropy = &-z \times \log(sigmoid(\alpha)) \\ &-(1-z) \times \log(1-sigmoid(\alpha)) \end{aligned} \tag{4}$$

where z is the label vector of the picture and α is the output of the neural network before the sigmoid activation function. With the sigmoid cross entropy as the loss function, the convolutional neural network is supposed to recognize all the present types of dipoles in the given field pattern.

3.1.2. Class Activation Map. To get the location of each type of dipole, the class activation mapping (CAM) technique is used. In image processing, a class activation map for a particular category indicates the discriminative image regions used by the CNN to identify that category [32], [33]. CAM can be generated using global averaging pooling after the last convolutional layer. Figure 3.4 shows the structure of the CNN for generating CAM. Global averaging pooling outputs the spatial average of the feature map at the last convolutional layer. Then a fully-connected layer is used as the last layer to produce the final output.

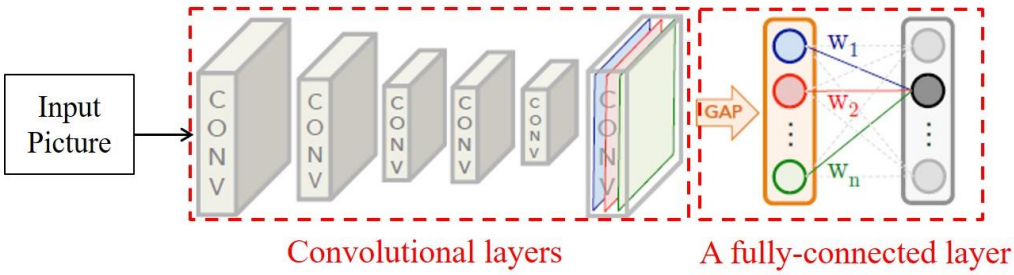

Figure 3.4. Location feature extraction in CNN.

For a given image, let $f_k(x, y)$ represent the output of unit k in the last convolutional layer at location (x, y). Then equation (5) shows the result of global average pooling.

$$F^k = \sum_{x,y} f_k(x, y) \tag{5}$$

The final score of a given class c, S_c, is calculated in (6).

$$S_c = \sum_k \omega_k^c F_k \tag{6}$$

where ω_k^c is the weight corresponding to class c for unit k in the last fully-connected layer. By plugging equation (5) into (6), the final score can be expressed in (7).

$$\begin{aligned} S_c &= \sum_k \omega_k^c \sum_{x,y} f_k(x, y) \\ &= \sum_{x,y} \sum_k \omega_k^c f_k(x, y) \end{aligned} \tag{7}$$

Then the class activation map for class c, denoted as M_c, is defined in (8).

$$M_c(x, y) = \sum_k \omega_k^c f_k(x, y) \tag{8}$$

Since the total score is the spatial summation of the class activation map, the class activation map directly indicates the importance of the image region leading to a certain class. The image region with larger values in the class activation map tends to be more relevant to this class. In this work, if a certain type of dipole moment is recognized by the neural network, the class activation map is calculated to identify the location of this dipole moment.

3.1.3. Dipole Extraction Algorithm by CNN. The structure of the CNN is shown in Figure 3.5. The batch size is 256 in this structure. After the input layer, there are two 2D convolutional layers connecting in series to increase the network complexity and function-fitting ability. Then a linear layer is used to reduce the dimension of the data. Finally a fully-connected layer with sigmoid activation function is used to generate the classification outputs. The last fully connected layer is also used to compute the class activation map.

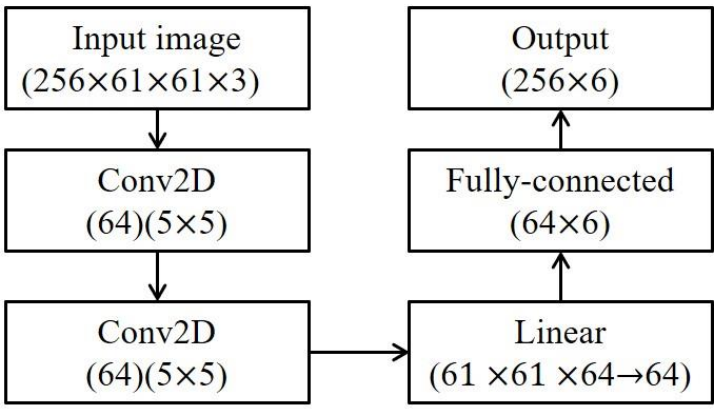

Figure 3.5. The structure of the CNN layer.

3000 field patterns generated from analytical formulas and their corresponding labels are used as training data. A learning rate of 0.01 with Adam Optimizer is used in training. The loss on test data is shown in Figure 3.6. The loss converges after 40 epochs.

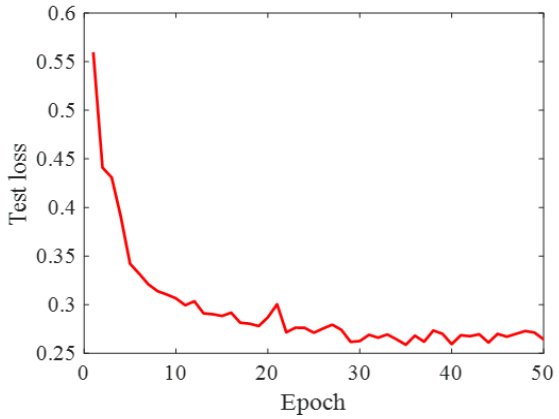

Figure 3.6. Testing loss graph of the neural network.

The workflow of the proposed dipole source reconstruction is shown in Figure 3.7. First the unknown field pattern is fed to the trained convolutional neural network to determine the types of dipole moments in this pattern. For each type of the dipole moment, the corresponding class activation map is calculated to determine its location.

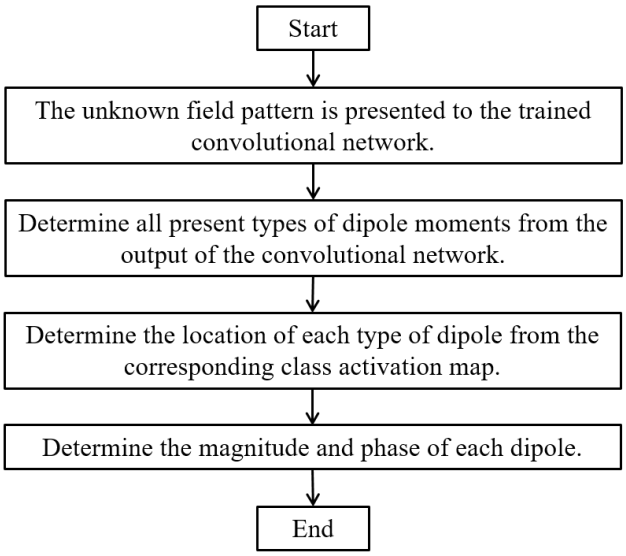

Figure 3.7. Workflow of the proposed algorithm.

3.2. VALIDATIONS

3.2.1. Synthesized Examples. The field pattern of the first example is shown in Figure 3.8. This pattern is from a simple M_x dipole and used to illustrate the function of class activation map. The neural network classifies the field pattern to M_x dipole category. Then the class activation map for this category is calculated and the result is shown in Figure 3.9.

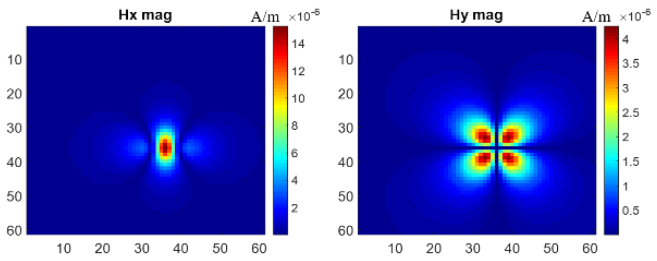

Figure 3.8. Field patterns of the input image in example 1.

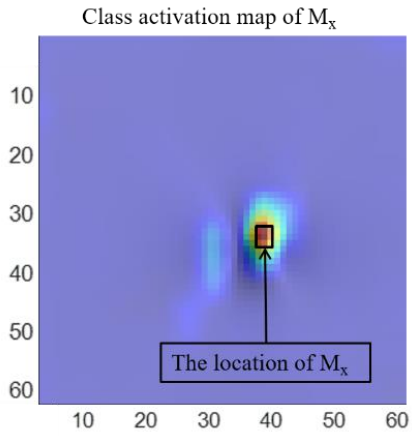

Figure 3.9. Class activation map of the M_x dipole type.

In the class activation map, the hot region represents the location that is most relevant to this category, thus indicating the location of the dipole moment. It can be seen that the region with largest color value in Figure 3.9 corresponds to the location of the dipole in the field pattern shown in Figure 3.8. Though the location information are not provided and only image-level labels are used in the training, this algorithm has the ability to locate the feature of a certain category.

The H_x and H_y field patterns of the second example are shown in Figure 3.10. The field pattern picture is sent to the pre-trained convolutional neural network. Two types of dipoles, M_x and M_z, are identified by the network. Similarly, the class activation maps for these two categories are calculated and the results are shown in Figure 3.11.

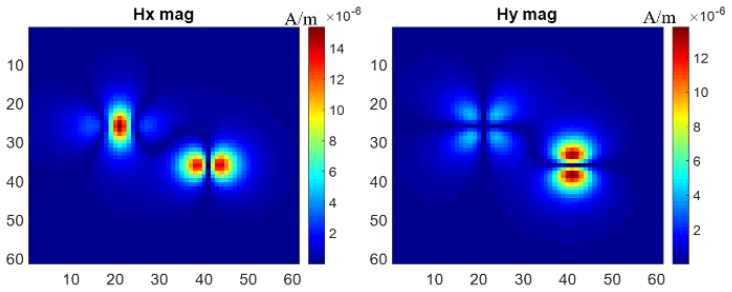

Figure 3.10. Field patterns of the input image in example 2.

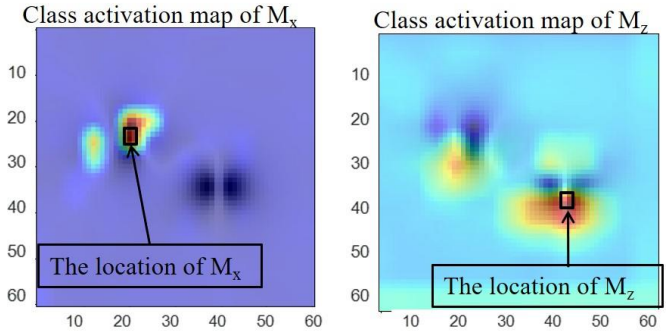

Figure 3.11. The class activation map of M_x and M_z.

In the class activation map for M_x dipole, it is clear that there is only one red region and the location of the largest value in this map is the location of the M_x dipole. The

location of the M_z dipole is also where the largest value locates in the M_z dipole map. The map for M_z dipole is noisier than the map for M_x in this example. Possible reasons can be the imbalance of the training data or hyper-parameters not being well-tuned. With the types and the locations of the dipoles known, their magnitudes and phases can be determined by least square or optimization methods. The H fields from the M_x dipole moment and the M_z dipole moment at the detected locations are shown in Figure 3.12.

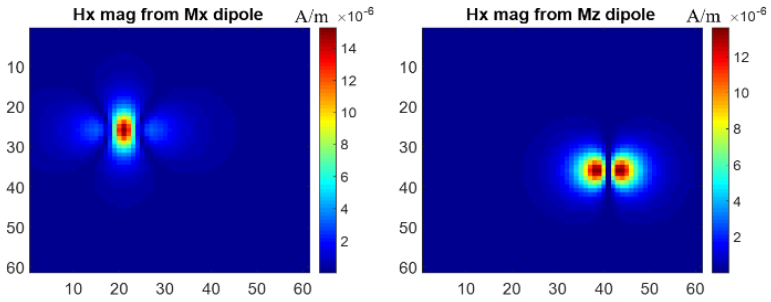

Figure 3.12. H_x patterns from the extracted dipoles.

Since two dipoles are located far away from each other, the field pattern in Figure 3.10 is relatively easier to recognize. A more complex example is tested on the proposed algorithm. The field pattern is shown in Figure 3.13. In this example, the probability for M_x and M_y categories is more than 99% and 20% for M_z from the neural network output. For other categories, the probability is less than 1%. If 50% is used as the threshold, M_x and M_y are two types of dipole moments identified by the algorithm.

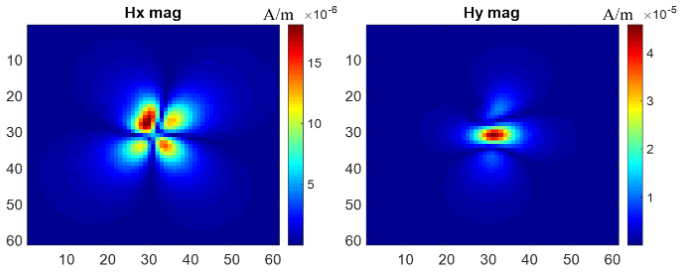

Figure 3.13. Field patterns of the input image in example 3.

Their corresponding class activation maps are shown in Figure 3.14. It can be observed that the M_x and M_y dipoles are pretty close to each other. Similarly, the magnitudes and phases of the dipoles can be further determined.

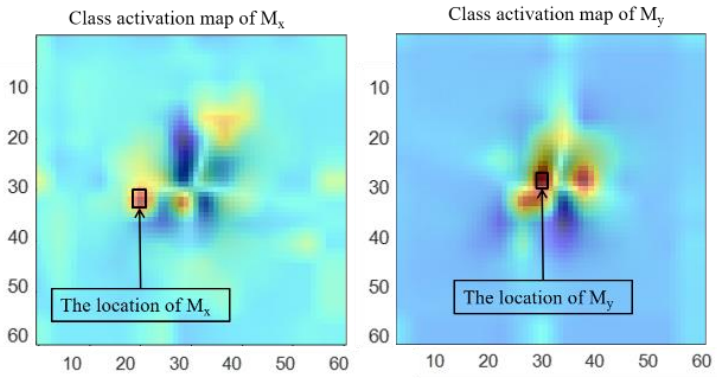

Figure 3.14. The class activation map of M_x and M_z.

The H fields from the M_x dipole moment and the M_y dipole moment at the detected locations are shown in Figure 3.15. The reconstructed field is compared to the original field

as shown in Figure 3.16. It can be seen that the reconstructed field pattern is very close to the input pattern.

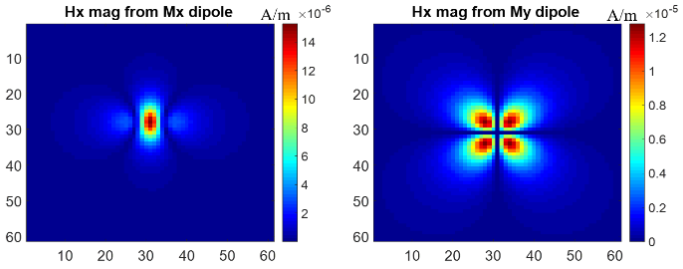

Figure 3.15. H_x patterns from the extracted dipoles.

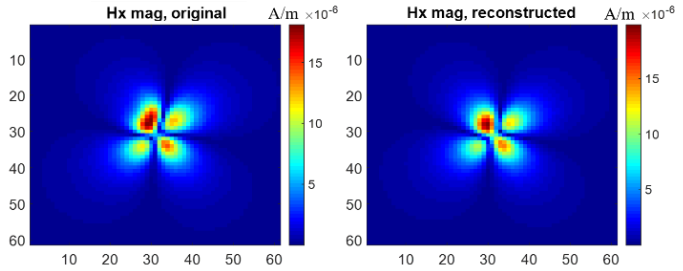

Figure 3.16. Reconstructed field pattern.

3.2.2. Practical Example. The proposed method is also tested on a more practical example from measurement. The measurement setup is shown in Figure 3.17. The measured H-field pattern is shown in Figure 3.18 and Figure 3.19.

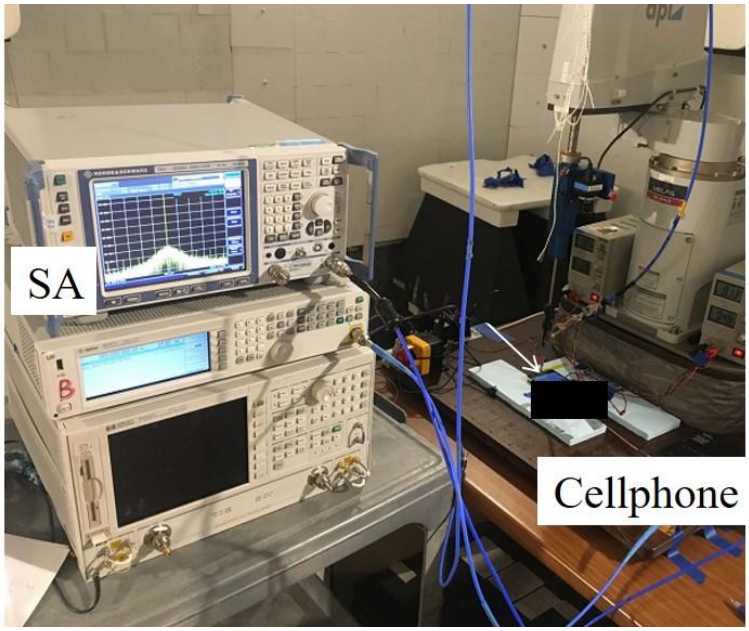

Figure 3.17. Setup of the field measurement.

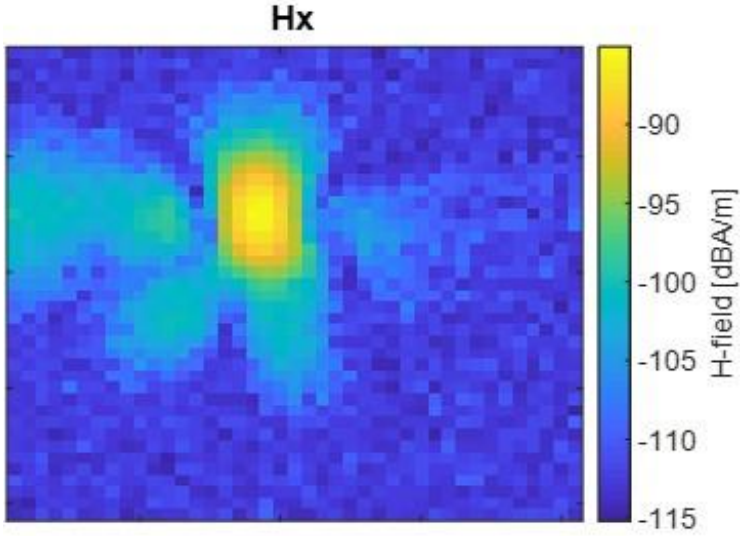

Figure 3.18. Measured H_x.

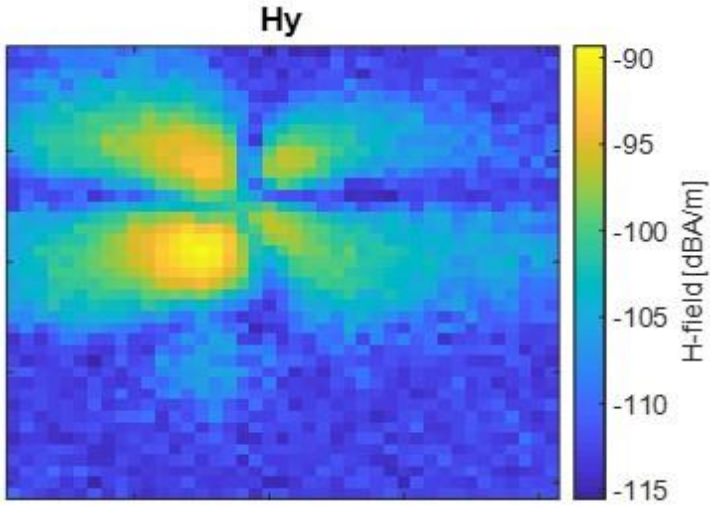

Figure 3.19. Measured H_y.

In this case, M_x and M_y are two types of dipole moments identified by the algorithm. Their corresponding class activation maps are shown in Figure 3.20 and Figure 3.21. The reconstructed field is compared to the original field as shown in Figure 3.22. It can be seen that the reconstructed field pattern is very close to the input pattern.

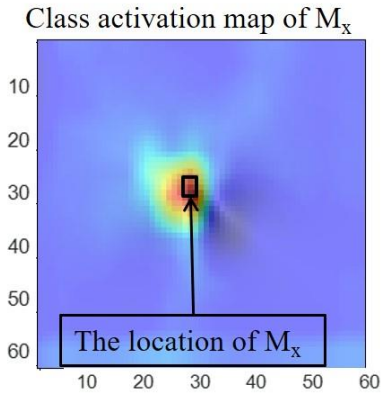

Figure 3.20. The class activation map of H_x.

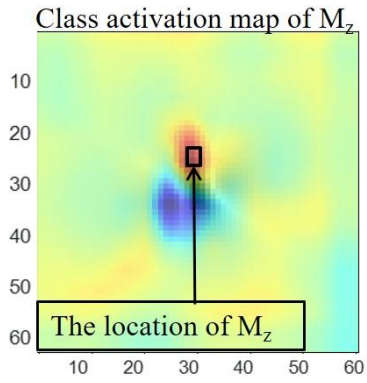

Figure 3.21. The class activation map of H_y.

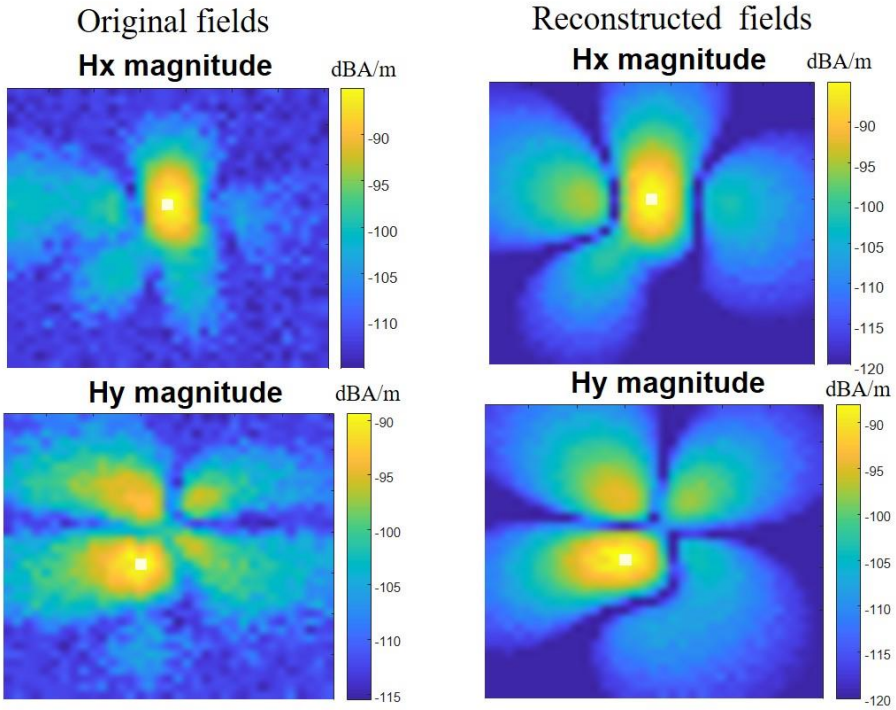

Figure 3.22. Reconstructed field pattern.

The main advantage of the proposed algorithm is that it can determine the dipole moment types and their corresponding locations in a short time with a well-trained neural network. Then the calculation of the magnitude and phase of each dipole with the location and type known is much easier than directly performing an optimization algorithm to extract dipole sources. The main drawback of this method is its generalization capability, like other machine learning based algorithms, is affected by the quality of training data and the values of hyper-parameters. Data augmentations and hyper-parameters tunings are needed to further improve the algorithm.

4. THE APPLICATION OF INTEGER PROGRAMMING TECHNIQUE FOR PCB STACK-UP DESIGN

In high speed system design, optimizing printed circuit board (PCB) stack-up plays an important role in design stage. Since PCB stack-up definition is one of the first things to be locked during the design phase, a less than optimum PCB stack-up can result in the selection of expensive laminate materials [34]-[37]. The cost of a system can be significantly reduced with an optimum stack-up design. An example of a PCB stack-up design is shown in Figure 4.1.

Z Type					Single Ended		Differential		
Target Z (ohms)					50		85		
Layer	Layer Name	Nominal Cu Wt	Dk Assumption	Nominal Thickness	Line-W / Z		Line-W / Space /Z		
	soldermask		3.2	0.5					
1	TOP	1.5 oz		1.9	7.8	49.3	8.9	9.7	84.09
Prepeg	PP		3.4	4					
2	GND	1 oz		1.3					
Core	Core		3.4	4					
3	INNER1	1 oz		1.3	4.6	49.3	6.1	10	84.03
Prepeg	PP		3.4	6					
4	GND	1 oz		1.3					
Core	Core		3.4	4					
5	INNER2	1 oz		1.3	6	49.36	7.4	10	84.26
Prepeg	PP		3.4	12					
6	INNER3	1 oz		1.3	6	49.36	7.4	10	84.26
Core	Core		3.4	4					
7	GND	1 oz		1.3					
Prepeg	PP		3.4	6					
8	INNER4	1 oz		1.3	4.6	49.3	6.1	10	84.03
Core	Core		3.4	4					
9	GND	1 oz		1.3					
Prepeg	PP		3.4	4					
10	BOTTOM	1.5 oz		1.9	7.8	49.3	8.9	9.7	84.09
	soldermask			0.5					
	Total Height			63.2					

Figure 4.1. An example of PCB stack-up.

In PCB stack-up design and optimization, signal integrity engineers are usually informed with the desired board thickness, the desired number of layers and the desired number of routing layers. In general, the ground/signal assignment and an initial value of the dielectric thickness for each layer need to be determined first, then the cross-section of each routing layer must be well tuned to achieve good electrical performances. Transmission line electrical properties such as characteristic impedance, insertion loss and crosstalk are usually considered at this step [38]-[43].

The stack-up arrangement is easy for a simple 6-layer or 8-layer board. However, in high performance workstations or servers, the high-speed PCB already goes to 20 layers or more, and this number may grow larger and larger in the future. The number of possible combinations becomes large, and there may be multiple optimum solutions that satisfy the requirements at this initial step. In different applications, the objective and the design rule may also be different. For example, whether setting microstrip lines or striplines as the primary objective will result in different designs. In general, this step is a problem to find all feasible combinations that satisfy the desired constraints. One way to generate a good stack-up arrangement is referring to a previous design and making some modifications. This approach is usually efficient in real designs, though some better choices may be ignored easily. Another approach is brute-force searching, but brute-force searching will be slow when the number of layers goes beyond 20. A scalable, flexible, and efficient approach for stack-up arrangement can help the entire design significantly.

After the stack-up arrangement is determined, the cross-section of each routing layer needs to be optimized. The objective of this step is usually optimizing the electrical properties of the transmission lines and can be modeled as a black-box optimization. Black-

box optimization methods like genetic algorithm (GA) and Bayesian optimization (BO) have been applied to similar optimization tasks [44]-[47]. In [44] and [45], advanced Bayesian optimization algorithms are developed to reduce the number of function evaluations. In [47], GA is used for optimizing high speed channels. In [46], Bayesian optimization is also applied to transmission line cross-section optimizations. In practical PCB stack-up designs, there are many constraints to the variables in the cross-section of transmission lines. For example, there are only a few possible choices for core thickness and dielectric materials. An optimization algorithm for discrete variables is more suitable for cross-section optimization in real designs. After optimizing the transmission lines in one layer, it is also necessary to check whether the entire design still satisfies all the design rules and constraints.

A new stack-up design optimization approach based on mixed integer programming technique is proposed. First, the stack-up arrangement problem is solved by integer programming solver. Integer programming is a mathematical optimization technique that has been used in many practical applications [48], [49]. Current integer programming solvers have included advanced heuristic searching algorithms and become very powerful. A scalable, flexible and efficient approach is developed by converting the stack-up arrangement problem to an integer linear programming problem. Next the cross-section of each routing layer is tuned by a black-box optimization algorithm, Harmonica, based on polynomial sparse recovery [50], [51]. In this algorithm, each variable is encoded by binary encoding to represent the possible values. The original optimization problem is converted to optimizing several recovered sparse polynomials. Finally these two algorithms are connected by an iterative approach to complete the PCB stack-up design.

4.1. INTEGER PROGRAMMING FOR STACK-UP DESIGN

4.1.1. Introduction of Integer Programming. An integer programming problem is a mathematical optimization or feasibility program in which some or all of the variables are restricted to be integers [49]. In many cases the term refers to integer linear programming (ILP), in which the objective function and the constraints are linear. An integer linear program in canonical form is expressed in (9):

$$\begin{aligned} &\text{maximize} && \mathbf{c}^T\mathbf{x} \\ &\text{subject to} && \mathbf{D}\mathbf{x} \le \mathbf{b}, \\ & && \mathbf{x} \ge 0, \\ &\text{and} && \mathbf{x} \in Z^n \end{aligned} \tag{9}$$

where **c**, **b** are vectors, **D** is a matrix and **x** is the unknown integer vector. As shown above, the mathematical model of an ILP consists of an objective and constraints. Integer programming solvers usually only take the equalities or inequalities as the constraints and optimize for a certain objective.

The following optimization problem is a simple example:

$$\begin{aligned} &\text{maximize} && x_1 + x_2 + x_3 + x_4 \\ &\text{If} && x_1 + 2x_2 \le 10, \\ &\text{then} && x_3 - 2x_4 \ge 2, \\ &\text{and} && 0 \le x_i \le 10, x_i \in Z, i = 1,2,3,4 \end{aligned} \tag{10}$$

The constraint in this example is a logical “if-then” constraint and can be transformed to an integer program by the equations below:

$$x_1 + 2x_2 \ge 11 - My_1, \tag{11}$$

$$x_3 - 2x_4 \ge 2 - M(1 - y_1), y_1 \in \{0,1\} \tag{12}$$

where y_1 is a new binary variable and M is a big number.

The explanation of the above equations is as follows. When the binary variable y_1 is 0, (11) is contradict to the "if" condition in (10). In this case, there is no other constraint to input variables and (12) becomes a trivial constraint when M is a large number like 100. When the binary variable y_1 is 1, (11) becomes a trivial constraint which includes the case that "if" condition in (10) is satisfied. Then (12) becomes the "then" logic in (10). The original "if-then" logic is also equivalent to either "$x_1 + 2x_2 \geq 11$" or "$x_3 - 2x_4 \geq 2$" or both. The additional binary variable in the equations interpret whether the "if" condition is satisfied. When no constraint needs to be satisfied, the large number M makes sure other equations are naturally true. By above transformations, any logical constraints can be transformed to an integer program consisting of mathematical equalities or inequalities only. Then an integer program solver can solve the problem very fast.

4.1.2. Stack-up Constraints Transformation by Integer Programming. As the stack-up arrangement is done before the cross-section optimization, the complex electromagnetic solvers are not involved yet. The linear equalities and inequalities are enough to cover the constraints. The electrical properties such as characteristic impedance or crosstalk are not determined at this step, however, based on our knowledge of transmission line physics, some general rules can still be developed to determine initial dielectric thickness values and ground/signal assignments.

Let's consider a PCB design with L layers, N routing layers, N_1 outer routing layers and total thickness T. The conductor type for jth layer is denoted as x_j, and x_j is a binary variable where 0 represents ground and 1 represents signal. The range of dielectric thickness is assumed to be between 3 mil and 20 mil and 0.5 mil granularity is considered. Therefore, the dielectric thickness can be converted to integers by multiplying a factor of

2. The dielectric thickness for *j*th layer is denoted as y_j, where y_j is an integer between 6 and 40 representing twice the real thickness value.

To build a mathematical model that can be solved by ILP solvers for this problem, all constraints need to be programmed as either equalities or inequalities. First of all, the number of routing layers and the total thickness requirements must be satisfied. The corresponding equalities and inequalities are shown in (13) to (15).

$$\sum_{j=1}^{L} x_j = N \quad , \tag{13}$$

$$x_1 + x_L = N_1 \ , \tag{14}$$

$$T' - \Delta T \le \frac{1}{2}\sum_{j=1}^{L-1} y_j \le T' + \Delta T \quad , \tag{15}$$

where N is the desired routing layer number, N_1 is the desired outer layer number, T' is the desired total thickness and ΔT is the tolerance defined by user. Since the conductor thickness is usually fixed, T' is also equal to the total board thickness T minus the total conductor thickness. Three consecutive signal layers are usually not allowed in high-speed PCB design, therefore one more inequality can be added as shown in (16). In this paper, only balanced and symmetric designs are considered for now and this rule can be written as two equalities in (17) and (18).

$$x_j + x_{j+1} + x_{j+2} \le 2, j = 1, 2, \ldots, L-2 \quad , \tag{16}$$

$$x_j = x_{L+1-j}, j = 1, 2, \ldots, L \ , \tag{17}$$

$$y_j = y_{L-j}, j = 1, 2, \ldots, L-1 \ , \tag{18}$$

There will be too many solutions if the above constraints are included. More rules need to be defined to further select the solutions. As mentioned before, even though the

electromagnetic solver is not involved, some general design rules can still be defined for transmission lines based on our knowledge. The transmission lines in PCB usually include mircrostrip lines, striplines and dual-striplines. The structure of a stripline is shown in Figure 4.2. For a stripline, since the surface roughness is more at the prepreg side of the trace, the primary reference plane is usually preferred to be the ground next to the core. Therefore, the prepreg needs to be thicker than the core especially when the core is thin. As the insertion loss tends to be larger when the dielectric thickness gets smaller, the difference between prepreg and core thickness should not be too large. For example, a 3 mil core with 10 mil stripline design and a 5 mil core with 8 mil prepreg stripline design have the same total thickness, but the latter design is considered to be better for loss consideration.

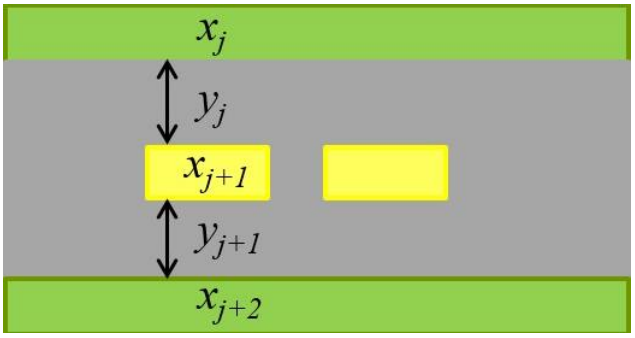

Figure 4.2. The structure of a differential stripline.

The following constraints for striplines are considered: if the core thickness is less than 7 mil, then the prepreg needs to be at least 1.5 mil thicker; if the core thickness is

greater than 7 mil, then prepreg needs to be thicker than core. The difference between prepreg and core thickness is not greater than 4 mil. This constraint is a logical "if-then-else-then" condition, however, the ILP solvers only accept equalities or inequalities as constraints. So the "big M" mathematical programming method is used to convert this logical condition to equalities and inequalities by introducing some additional variables. The derived inequalities are shown in (19) to (29):

$$A_j = x_j + 2x_{j+1} + 4x_{j+2} \ , \tag{19}$$

$$2 - M(1 - \mathrm{u}_j) \le \mathrm{A}_j \ , \tag{20}$$

$$1 + Mu_j \ge A_j \ , \tag{21}$$

$$2 + M(1 - v_j) \ge \mathrm{A}_j \ , \tag{22}$$

$$3 - Mv_j \le \mathrm{A}_j \ , \tag{23}$$

$$0 \le u_j + v_j - 2t_j \le 1 \ , \tag{24}$$

$$13 + M(1 - p_j) \ge y_{j+1} \ , \tag{25}$$

$$14 - Mp_j \le y_{j+1} \ , \tag{26}$$

$$y_j - y_{j+1} \ge 3 - M(1 - p_j) - M(1 - t_j) \ , \tag{27}$$

$$y_j - y_{j+1} \ge 0 - Mp_j - M(1 - t_j) \ , \tag{28}$$

$$\begin{matrix} y_j - y_{j+1} \le 8 + M(1 - t_j) \\ j = 1, 2, \ldots, L - 2 \end{matrix} \ , \tag{29}$$

where y_j and y_{j+1} represents twice the prepreg and core thickness respectively, u_j, v_j, t_j, p_j are new binary variables which can only be 0 or 1, M is a large constant and is set to 100 in this example.

The explanation of the above equations is as follows. First A_j is a binary encoding of three variables that represent three consecutive conductor assignments, the stack-up forms a ground-signal-ground stripline structure only when A_j is equal to 2, which is also equivalent to A_j is both greater or equal to 2 and less than or equal to 2. Then (20) to (23) ensure that this is true only when both u_j and v_j are 1. When either u_j or v_j is zero, the stack-up at jth layer is not a stripline so the constraints don't apply. In this condition, the inequalities in (27) to (29) are automatically satisfied as M is a large number that exceeds the range of y_i and $y_{j+1.}$ And this is equivalent to no constraints are applied. Equation (24) means t_j is equal to the logical and of u_j and v_j, so whether t_j is 1 determines the current structure is a stripline or not. When p is equal to one, (25) and (27) are equivalent to the constraint when core is thinner than 7 mil. Equation (26) and (28) will become two trivial constraints in this condition due to the large M. Similarly when p is zero, (26) and (28) are equivalent to the "else-then" part while (25) and (27) become two trivial constraints. In summary, the additional binary variables interpret whether some conditions are satisfied and the large constant ensures that other constraints are always satisfied automatically. Finally, the original logical constraints are converted to multiple inequalities that fit to integer programming formulations. Since the range of unknown variables are known, it is very easy to determine a large number to serve as M.

There may be some dual-striplines in the design as well due to the number of layers limitation. Figure 4.3 shows the structure of a dual-stripline. For a dual-stripline, two signal to ground distances are usually required to be the same. The separation between two signals needs to be large so the broadside coupling is reduced. For example, the signal to signal

separation is constrained to be greater or equal to 4 times the dielectric thickness between signal and ground.

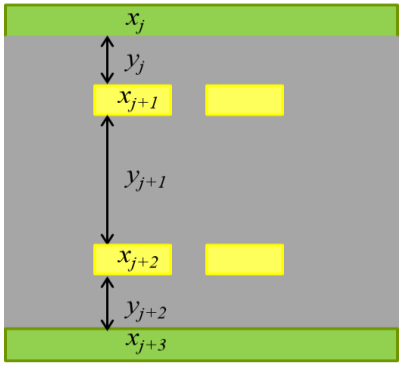

Figure 4.3. The structure of a dual stripline.

The corresponding equalities and inequalities are shown in (30) to (38):

$$B_j = x_j + 2x_{j+1} + 4x_{j+2} + 8x_{j+3} \ , \tag{30}$$

$$6 - M(1-k_j) \le B_j \ , \tag{31}$$

$$5 + Mk_j \ge B_j \ , \tag{32}$$

$$6 + M(1-l_j) \ge B_j \ , \tag{33}$$

$$7 - Ml_j \le B_j \ , \tag{34}$$

$$0 \le k_j + l_j - 2q_j \le 1 \ , \tag{35}$$

$$y_{j+2} - y_j \le 0 + M(1-q_j) \ , \tag{36}$$

$$y_{j+2} - y_j \ge 0 - M(1-q_j) \ , \tag{37}$$

$$\begin{matrix} y_{j+1} - 4y_j \geq 0 - 4M(1-q_j) \\ j = 1, 2, \ldots, L-3 \end{matrix}, \tag{38}$$

where y_j and y_{j+2} are twice the dielectric thickness between signal and ground, y_{j+1} is twice the separation between signals, k_j, l_j, q_j are new binary variables that can only be 0 or 1, M is the same large constant defined previously.

Similarly, B_j is a binary encoding of four consecutive layers, the current structure is a dual-stripline only when B_j is equal to 6. Then by (31) to (35), this condition is further converted to binary variable q_j equal to 1. Equation (36) to (38) are the desired constraints for dual-stripline designs when q_j is equal to 1 and they become trivial constraints when q_j is zero due to the large constant M.

Depending on the specific applications, other constraints may also apply. As long as the constraints can be written in simple linear equations, they can be converted to inequalities using a similar method no matter how complex in logical they are. With all constraints being converted to inequalities, the integer programming solver will be called to solve the problem.

4.2. SOLVING BY INTEGER PROGRAMMING SOLVER

Characteristic impedance and insertion loss are two main electrical properties that are considered in transmission line designs. The characteristic impedance is determined by per-unit-length (PUL) RLGC parameters [52]-[58]. Total loss consists of conductor loss and dielectric loss. They are determined by PUL RLGC parameters and dielectric material properties. Characteristic impedance and insertion loss will affect the eye diagram in the system [59]-[61]. Since the transmission line is usually designed for a desired characteristic impedance, a larger dielectric height leads to a larger trace width to achieve the desired

impedance. The PUL R term gets smaller when trace width increases. Therefore, the objective of the integer program can be set as maximizing the summation of all core layer heights if minimizing insertion loss is the primary target.

Design density is another factor that is usually considered in practical designs. Smaller trace width and spacing lead to a higher design density. If high design density is the priority, the objective of the integer program can be set as minimizing the summation of all core layer heights.

The objective of this integer program can also be left empty when there is no primary target. In this case, the integer program becomes a feasibility problem and all combinations that satisfy the constraints are solutions.

Integer programming solvers give one solution in one run. To obtain multiple solutions or all feasible solutions, the solver can be called iteratively, and in each iteration a new constraint that the next solution must be different from the solution in last iteration is added. The flow diagram of solving the stack-up arrangement problem is shown in Figure 4.4. For the additional constraint that the next solution must be different from the solution in previous iteration, it also needs to be converted to inequalities to be fed to integer programming solvers. Suppose a1, …, aL represents the solution for x1, …, xL in the last iteration, then the additional constraint can be written as (39):

$$\sum_{j=1}^{L} a_j x_j \leq N - 1 \tag{39}$$

where N is still the number of routing layers. Since a_j is already known in last iteration, it is just a constant that can be either 0 or 1. This inequality can be interpreted as the signal layers assignment is different from the last iteration.

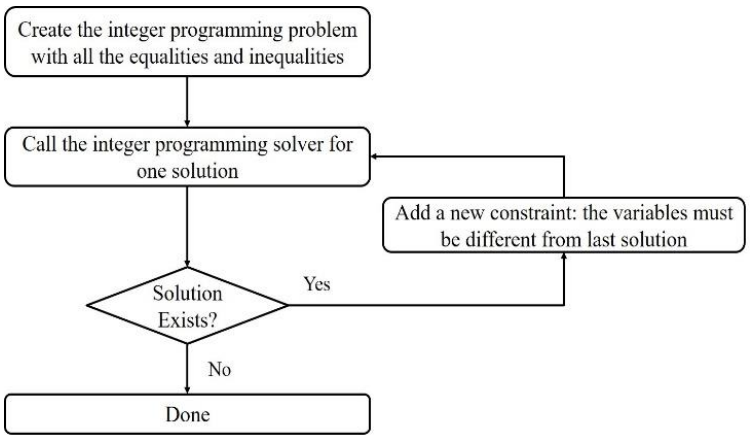

Figure 4.4. The flow chart for solving integer programming problems.

4.3. STACK-UP DESIGN VALIDATIONS

The proposed algorithm is tested on a 30-layer PCB design. In this example, 16 inner routing layers and 2 outer routing layers are required, and the desired total board thickness is 180 mil. The stripline designs need to satisfy the constraints mentioned in the previous section. For dual striplines, the design rule is that the signal to signal separation is greater or equal to 4 times the distance between signal and reference plane to reduce the broadside coupling. The ranges for core and prepreg thickness are 3 – 10 mil and 3 – 20 mil, respectively. The Coin-or is used as the integer programming solver [62].

For a 30-layer case, the number of possible signal/ground assignments without any constraint is 4 million and 35 solutions among the 4 million combinations satisfy the specific requirements in this case and the basic PCB stack-up design rules mentioned in previous section. The integer programming method can find all 35 solutions in 10 seconds shown in Figure 4.5. Assuming other constraints for this 30-layer example are the same as the previous example, a similar procedure is performed to tune the cross-section of

transmission lines and make sure the desired constraints are satisfied at the same time. The completed stack-up design of this 30-layer case is shown in Figure 4.6.

	1	TOP	TOP	TOP	TOP	TOP	TOP	TOP	TOP	TOP	TOP	TOP	TOP	TOP	TOP
Prepreg		PP	PP	PP	PP	PP	PP	PP	PP	PP	PP	PP	PP	PP	PP
	2	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
Core		Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core
	3	INNER1	INNER1	INNER1	INNER1	INNER1	GND	INNER1	INNER1	INNER1	INNER1	INNER1	INNER1	INNER1	GND
Prepreg		PP	PP	PP	PP	PP	PP	PP	PP	PP	PP	PP	PP	PP	PP
	4	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	INNER1
Core		Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core
	5	INNER2	INNER2	INNER2	INNER2	INNER2	INNER1	INNER2	INNER2	INNER2	INNER2	INNER2	INNER2	INNER2	INNER2
Prepreg		PP	PP	PP	PP	PP	PP	PP	PP	PP	PP	PP	PP	PP	PP
	6	INNER3	INNER3	GND	GND	GND	INNER2	INNER3	INNER3	INNER3	INNER3	GND	GND	INNER3	GND
Core		Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core
	7	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	INNER3	INNER3	GND	GND
Prepreg		PP	PP	PP	PP	PP	PP	PP	PP	PP	PP	PP	PP	PP	PP
	8	INNER4	INNER4	INNER3	INNER3	INNER3	INNER3	INNER4	INNER4	GND	GND	INNER4	INNER4	GND	INNER3
Core		Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core
	9	INNER5	INNER5	INNER4	INNER4	INNER4	INNER4	INNER5	INNER5	INNER4	INNER4	GND	GND	INNER4	INNER4
Prepreg		PP	PP	PP	PP	PP	PP	PP	PP	PP	PP	PP	PP	PP	PP
	10	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
Core		Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core
	11	INNER6	GND	INNER5	GND	INNER5	INNER5	GND	GND	INNER5	INNER5	GND	INNER5	GND	INNER5
Prepreg		PP	PP	PP	PP	PP	PP	PP	PP	PP	PP	PP	PP	PP	PP
	12	GND	INNER6	INNER6	INNER5	INNER6	GND	GND	INNER6	GND	INNER6	INNER5	INNER6	INNER5	GND
Core		Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core
	13	GND	GND	GND	INNER6	GND	INNER6	INNER6	GND	INNER6	GND	INNER6	GND	INNER6	INNER6
Prepreg		PP	PP	PP	PP	PP	PP	PP	PP	PP	PP	PP	PP	PP	PP
	14	GND	GND	GND	GND	INNER7	GND	GND	INNER7	INNER7	GND	GND	GND	GND	GND
Core		Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core
	15	INNER7	INNER7	INNER7	INNER7	GND	INNER7	INNER7	GND	GND	INNER7	INNER7	INNER7	INNER7	INNER7
Prepreg		PP	PP	PP	PP	PP	PP	PP	PP	PP	PP	PP	PP	PP	PP
	16	INNER8	INNER8	INNER8	INNER8	GND	INNER8	INNER8	GND	GND	INNER8	INNER8	INNER8	INNER8	INNER8
Core		Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core
	17	GND	GND	GND	GND	INNER8	GND	GND	INNER8	INNER8	GND	GND	GND	GND	GND
Prepreg		PP	PP	PP	PP	PP	PP	PP	PP	PP	PP	PP	PP	PP	PP
	18	GND	GND	GND	INNER9	GND	INNER9	INNER9	GND	INNER9	GND	INNER9	GND	INNER9	INNER9
Core		Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core
	19	GND	INNER9	INNER9	INNER10	INNER9	GND	GND	INNER9	GND	INNER9	INNER10	INNER9	INNER10	GND
Prepreg		PP	PP	PP	PP	PP	PP	PP	PP	PP	PP	PP	PP	PP	PP
	20	INNER9	GND	INNER10	GND	INNER10	INNER10	GND	GND	INNER10	INNER10	GND	INNER10	GND	INNER10
Core		Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core
	21	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
Prepreg		PP	PP	PP	PP	PP	PP	PP	PP	PP	PP	PP	PP	PP	PP
	22	INNER10	INNER10	INNER11	INNER11	INNER11	INNER11	INNER10	INNER10	INNER11	INNER11	GND	GND	INNER11	INNER11
Core		Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core
	23	INNER11	INNER11	INNER12	INNER12	INNER12	INNER12	INNER11	INNER11	GND	GND	INNER11	INNER11	GND	INNER12
Prepreg		PP	PP	PP	PP	PP	PP	PP	PP	PP	PP	PP	PP	PP	PP
	24	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	INNER12	INNER12	GND	GND
Core		Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core
	25	INNER12	INNER12	GND	GND	GND	INNER13	INNER12	INNER12	INNER12	INNER12	GND	GND	INNER12	GND
Prepreg		PP	PP	PP	PP	PP	PP	PP	PP	PP	PP	PP	PP	PP	PP
	26	INNER13	INNER13	INNER13	INNER13	INNER13	INNER14	INNER13	INNER13	INNER13	INNER13	INNER13	INNER13	INNER13	INNER13
Core		Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core
	27	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	INNER14
Prepreg		PP	PP	PP	PP	PP	PP	PP	PP	PP	PP	PP	PP	PP	PP
	28	INNER14	INNER14	INNER14	INNER14	INNER14	GND	INNER14	INNER14	INNER14	INNER14	INNER14	INNER14	INNER14	GND
Core		Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core
	29	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
Prepreg		PP	PP	PP	PP	PP	PP	PP	PP	PP	PP	PP	PP	PP	PP
	30	BOTTOM	BOTTOM	BOTTOM	BOTTOM	BOTTOM	BOTTOM	BOTTOM	BOTTOM	BOTTOM	BOTTOM	BOTTOM	BOTTOM	BOTTOM	BOTTOM

Figure 4.5. The stack-up arrangement results.

Casenumber		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	Solderm	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5
1	TOP	1.9	1.9	1.9	1.9	1.9	1.9	1.9	1.9	1.9	1.9	1.9	1.9	1.9	1.9	1.9
Prepreg	PP	3	3	3.5	3	3	3.5	4	3	3	3.5	3.5	3	3	4	4.5
2	GND	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3
Core	Core	3	3	3	3.5	4	3.5	3	3.5	3	3	3.5	3	4	3	3.5
3	GND	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3
Prepreg	PP	6	5.5	6	6	6	6	6	5.5	6	5.5	5.5	5.5	5.5	5.5	5
4	INNER1	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3
Core	Core	3	3.5	3	3	3	3	3	3.5	3	3.5	3.5	3.5	3.5	3.5	3.5
5	GND	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3
Prepreg	PP	6	5.5	6	6	6	6	6	5.5	6	5.5	5.5	5.5	5.5	5.5	5
6	INNER2	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3
Core	Core	3	3.5	3	3	3	3	3	3.5	3	3.5	3.5	3.5	3.5	3.5	3.5
7	GND	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3
Prepreg	PP	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3
8	INNER3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3
Core	Core	12	12	12	12	12	12	12	12	13	12	12	13	12	12	12
9	INNER4	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3
Prepreg	PP	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3
10	GND	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3
Core	Core	3	3.5	3	3	3	3	3	3.5	3	3.5	3.5	3.5	3.5	3.5	3.5
11	INNER5	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3
Prepreg	PP	6	5.5	6	6	6	6	6	5.5	6	5.5	5.5	5.5	5.5	5.5	5
12	GND	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3
Core	Core	3	3.5	3	3	3	3	3	3.5	3	3.5	3.5	3.5	3.5	3.5	3.5
13	INNER6	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3
Prepreg	PP	6	5.5	6	6	6	6	6	5.5	6	5.5	5.5	5.5	5.5	5.5	5
14	GND	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3
Core	Core	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3
15	INNER7	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3
Prepreg	PP	12	12	12	12	12	12	12	12	13	12	12	13	12	12	12
16	INNER8	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3
Core	Core	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3
17	GND	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3
Prepreg	PP	6	5.5	6	6	6	6	6	5.5	6	5.5	5.5	5.5	5.5	5.5	5
18	INNER9	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3
Core	Core	3	3.5	3	3	3	3	3	3.5	3	3.5	3.5	3.5	3.5	3.5	3.5
19	GND	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3
Prepreg	PP	6	5.5	6	6	6	6	6	5.5	6	5.5	5.5	5.5	5.5	5.5	5
20	INNER1	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3
Core	Core	3	3.5	3	3	3	3	3	3.5	3	3.5	3.5	3.5	3.5	3.5	3.5
21	GND	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3
Prepreg	PP	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3
22	INNER1	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3
Core	Core	12	12	12	12	12	12	12	12	13	12	12	13	12	12	12
23	INNER1:	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3
Prepreg	PP	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3
24	GND	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3
Core	Core	3	3.5	3	3	3	3	3	3.5	3	3.5	3.5	3.5	3.5	3.5	3.5
25	INNER1:	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3
Prepreg	PP	6	5.5	6	6	6	6	6	5.5	6	5.5	5.5	5.5	5.5	5.5	5
26	GND	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3
Core	Core	3	3.5	3	3	3	3	3	3.5	3	3.5	3.5	3.5	3.5	3.5	3.5
27	INNER1	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3
Prepreg	PP	6	5.5	6	6	6	6	6	5.5	6	5.5	5.5	5.5	5.5	5.5	5
28	GND	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3
Core	Core	3	3	3	3.5	4	3.5	3	3.5	3	3	3.5	3	4	3	3.5
29	GND	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3
Prepreg	PP	3	3	3.5	3	3	3.5	4	3	3	3.5	3.5	3	3	4	4.5
30	BOTTOI	1.9	1.9	1.9	1.9	1.9	1.9	1.9	1.9	1.9	1.9	1.9	1.9	1.9	1.9	1.9
	Solderm	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5
	Total He	179	179	180	180	181	181	181	180	181	180	181	181	181	181	179

Figure 4.6. The stack-up design result.

The main advantage of using integer programming method for layer arrangement step is its scalability and efficiency. Figure 4.7 shows the time spent by integer programming solver .vs the number of layers. It can be seen that the consumed time is still small even when the number of layers reach 40. If this process is done by logical searching, it will take much longer to find all possible solutions. Since the integer programming approach converts constraints to inequalities, it is also flexible with constraints changed or additional constraints. The main limitation is current integer programming solvers can only handle linear or quadratic inequalities. The solvers can't deal with complex non-linear inequalities such as an electromagnetic problem. Hence, the integer programming approach can only be used for layer arrangement.

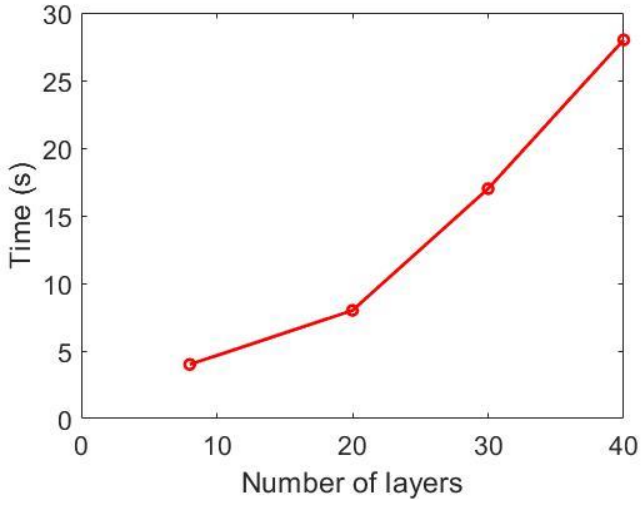

Figure 4.7. The time this method takes.

4.4. CORNER CASES SEARCHING BY INTEGER PROGRAMMING

When a stack-up arrangement is selected, the transmission line at each signal layer is designed to meet the required characteristic impedance. The trace width and spacing can be tuned by optimization methods such as Genetic algorithm or Bayesian optimization [46], [47]. At the pre-layout design stage, it is necessary to take the manufacturing variations into consideration and find the corner cases. In real applications, the manufacturing variation can affect the overall performance and de-embedding accuracy in characterizations and verifications [63], [64]. When all parameters including cross-section geometry and material properties are at designed values, the characteristic impedance and insertion loss of this nominal case are the nominal impedance and nominal loss. With the variation range of each parameter given, there are 6 corner cases that need to be considered: high impedance and high loss; high impedance and low loss; nominal impedance and high loss; nominal impedance and low loss; low impedance and high loss; low impedance and low loss. Since PCB house will usually do impedance control, high impedance case means the case with a characteristic impedance about 10% higher than the nominal value assuming 10% impedance control is done. Therefore, high impedance and high loss corner case means the case with highest loss and its impedance is constrained to be 10% higher than the nominal value. In other words, this problem is to find combinations with constraints while maximizing or minimizing another quantity, which is also in the scope of integer programming applications. The proposed method is to find multiple possible solutions by solving an integer program first, then do a brute-force searching on these possible cases by 2D cross-section simulations. The flow of the proposed algorithm is shown in Figure 4.8.

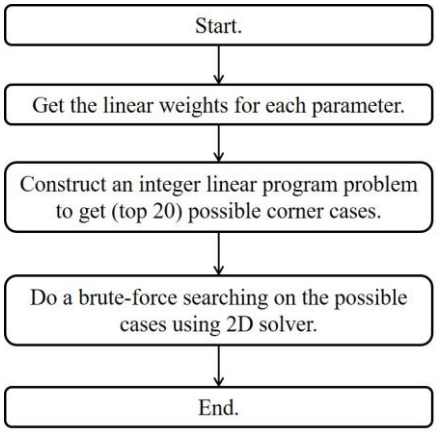

Figure 4.8. The flow chart for corner case searching.

4.4.1. Integer Program Construction. Since differential stripline is the most common transmission line in high speed PCB, the stripline model shown in Figure 4.9 is used for illustration. This model includes the core layer, resin layer and prepreg layer to model the stripline accurately. There are 13 variables in this model including all geometry and material parameters, denoted as $\alpha_1, \alpha_2, \ldots, \alpha_{13}$. Each variable is first encoded as integers based on its low bound, high bound and step size. The nominal value of each variable is encoded as 0. Since all variables will only vary in a small range, the relationship between inputs and outputs can be approximated as a linear function. The weights for one variable are calculated from 2D simulations by setting this variable to its high bound or low bound value, while other variables are at the nominal value as shown in (40) – (41).

$$w_{i,z} = (Z(\alpha)|_{\alpha_i=\alpha_{i,high}} - Z(\alpha)|_{\alpha_i=\alpha_{i,low}}) / N_i \ , \tag{40}$$

$$w_{i,loss} = (L(\alpha)|_{\alpha_i=\alpha_{i,high}} - L(\alpha)|_{\alpha_i=\alpha_{i,low}}) / N_i \ , \tag{41}$$

where Z and L are the characteristic impedance and per-unit-length loss function calculated from 2D simulations, N_i is the number of levels for each variable. For a 13-variable problem, there are 26 simulations in this step.

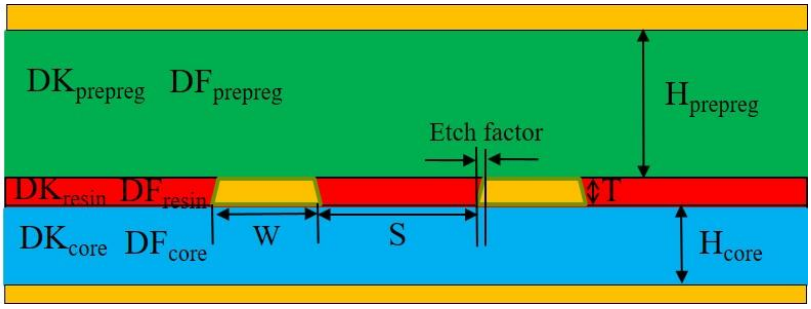

Figure 4.9. Variables in a differential stripline.

Then the impedance constraint can be constructed by linear inequalities. Take the high impedance and loss as an example, the constraints can be expressed as the inequalities in (42) – (43).

$$\alpha_{i,low} \le \alpha_i \le \alpha_{i,high} \ , \tag{8}$$

$$(Z_{high} - Z_n + \delta_z) \ge \sum_{i=1}^{n} w_{i,z}\alpha_i \ge (Z_{high} - Z_n - \delta_z) \ , \tag{9}$$

where $\alpha_{i,low}$ and $\alpha_{i,high}$ are the encoded bounds of each variable, Z_{high} and Z_n are the high impedance and the nominal impedance in this case, δ_z is the tolerance value. The above equation represents the constraint that the characteristic impedance is around the high impedance value.

To find the case with high loss, the weighted linear summation of all variables needs to be maximized. Therefore, the objective of this integer program is:

$$Maximize \sum_{i=1}^{n} w_{i,loss}\alpha_i \tag{44}$$

The constraint inequalities for nominal impedance and high loss can be similarly constructed in (45) – (48).

$$A_{nominal,h} \geq \sum_{i=1}^{n} \alpha_{i,z}x_i \geq -A_{nominal,l} \tag{45}$$

$$A_{nominal,h} = \delta_h / \left(\frac{(A_{0,z}-B_{0,z})}{N_{x0}}\right)\alpha_{i,z} \tag{46}$$

$$A_{nominal,l} = \delta_l / \left(\frac{(A_{0,z}-B_{0,z})}{N_{x0}}\right)\alpha_{i,z} \tag{47}$$

$$\delta_h = Z_{n,h-}Z_{nominal},\ \delta_l = -Z_{n,l} + Z_{nominal} \tag{48}$$

For other corner cases, the integer program can be constructed similarly using the weights calculated previously.

4.4.2. Corner Case Searching Validation. The proposed method is tested on a practical design: trace width is 5 mil; trace spacing is 6.5 mil; trace thickness is 1.2 mil; core height is 3.5 mil; prepreg height is 10 mil; the dielectric constant is 3.8 and loss tangent is 0.012 for all dielectric materials. This nominal design will generate an 85-ohm differential stripline. To search the corner cases of this nominal design, a certain variation for each variable is assumed. The low bound and high bound for all variables are shown in Table 4.1. As mentioned above, this stripline model contains three dielectric layers: the core layer, the resin layer, and the prepreg layer. The material property for each dielectric layer can be different so the characteristic impedance and insertion loss of the differential stripline pair can be modeled more accurately.

Table 4.1. Bounds of input variables.

Variable	Low	Nominal	High
Trace width	4.3 mil	5 mil	5.7 mil
Trace spacing	5.8 mil	6.5 mil	7.2 mil
Trace thickness	1.05 mil	1.2 mil	1.35 mil
Core height	2.9 mil	3.5 mil	4.1 mil
Prepreg height	8 mil	10 mil	12 mil
Core DK	3.65	3.8	3.95
Prepreg DK	3.65	3.8	3.95
Resin DK	3.65	3.8	3.95
Core DF	0.01	0.012	0.014
Prepreg DF	0.01	0.012	0.014
Resin DF	0.01	0.012	0.014
Roughness level	3	5	7
Etch factor	0.35	0.5	0.65

Since the integer program constraint is constructed from linear approximations, it is necessary to validate the assumption first. The characteristic impedance and per-unit-length loss results are shown in Figure 4.10 when trace width is swept from 4.3 mil to 5.7 mil. Though the outputs don't strictly change linearly with trace width, the relationship can be approximated as a linear function in this small range. The calculated weights in this example is shown in Table 4.2.

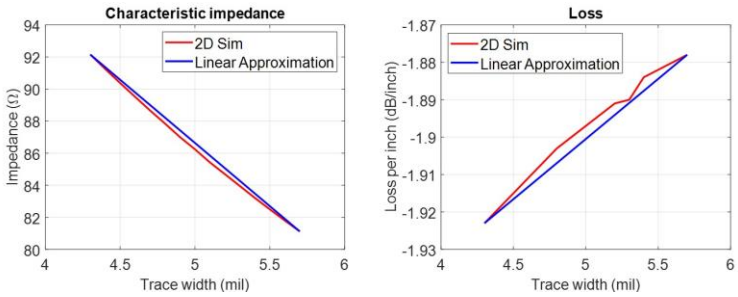

Figure 4.10. Linear approximation.

Table 4.2. Calculated weights.

Variable	Impedance	Loss
Trace width	-47	-9
Trace spacing	+11	-4
Core height	+49	-44
Prepreg height	+6	-2
Trace thickness	-25	-19
Core DK	-4	0
Core DF	0	+87
Prepreg DK	-2	+2
Prepreg DF	0	+54
Resin DK	-1	+1
Resin DF	0	+23
Roughness level	3	+67
Etch factor	+17	+8

The results are compared to brute-force searching. In this validation, a pre-trained neural network model replaces the 2D simulation solver to save searching time. The results comparison is shown in Table 4.3. The accuracy of proposed method can be guaranteed.

Table 4.3. Searching results.

	Integer program searching	1 million brute-force searching
High loss, high impedance	94.01Ω and 2.231 dB/inch	94.01Ω and 2.231 dB/inch
High loss, nominal impedance	86Ω and 2.371 dB/inch	86Ω and 2.371 dB/inch

To reduce the searching time when running with 2D simulation solvers in practical use, a parallel engine is developed using python scripts to launch 2D simulations in parallel. The searching time is shown in Table 4.4. Assuming 20 solutions are desired for each corner case, there are 146 simulations that need to be done to find 6 corner cases. By using the parallel engine to launch the 2D cross-sectional analysis, the simulation time can be reduced significantly.

Table 4.4. Searching time.

# of solutions for each corner case	# of simulations running in parallel	Total Simulation Time
10	10	12 min
20	10	25 min
20	20	15 min

5. CONCLUSION

In Section 2, CE noises from an ac-dc power supply in an LED TV are analyzed and modeled. An EMI receiver model is built to evaluate the conducted EMI from time domain noise waveforms. The dominant DM noise mechanism varies with frequency ranges and time intervals. Below 700 kHz, the differential loop of the PFC is the main noise current path and this mechanism happens when the rectifier is on. When one diode in the rectifier is forward biased and three other diodes are reverse biased, mode-conversion happens, and it is the dominant DM EMI mechanism above 700 kHz. The parasitic capacitances between the PCB layout and the metallic chassis are the main current paths for CM EMI noise. A loop inductance is introduced by the closed loop formed by the metallic chassis, earth ground and the power cable. This loop inductance and the total parasitic capacitance cause a resonance in EMI noise. A transient simulation model is built to predict CE noises. The prediction from the transient simulation matches well with measurement results.

In Section 3, A machine learning based dipole source reconstruction method is proposed. A multi-label classification analysis is performed by a convolutional neural network to determine the types of the dipole moment sources. This algorithm further uses the class activation map technique to determine the location of the dipoles. Three simulation examples and one measurement example are presented to validate the proposed algorithm and show how the class activation map can help locate the dipoles.

In Section 4, An integer programming based method for PCB stack-up arrangement in real designs is introduced. Constraints and rules in this problem are converted to

equalities and inequalities using mathematical programming techniques. Then integer programming solvers are called to solve the mathematical integer programming problems. The proposed method can generate all possible combinations and solutions that satisfy users' desired constraints efficiently. This method is also scalable to the number of layers and flexible to the input constraints.

Then the application of integer programming is further extended to corner case searching. The searching range is first narrowed down by applying constraints using an integer program. Then brute-force searching is applied to search the corner cases. A parallel engine is developed to run 2D cross-section simulations in parallel. The whole process is automated and the accuracy is good.

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