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Modeling, Analysis, and Control Design of a Single-Stage Boost Inverter

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Abstract: A single-phase, single-stage, differential boost inverter comprises two independently-controlled boost DC-DC converters, with the load connected between their outputs. The net voltage on the load is sinusoidal and has a controllable frequency and magnitude that is larger than that of the DC source. The present work first derives steady-state and small-signal models of the inverter with parasitic elements. The results obtained from the line-to-output transfer function, control-to-output transfer function, open-loop input impedance, and open-loop output impedance models are compared with that of the ones obtained from the experimental testbed. Using the new models, a voltage mode controller is designed in the synchronous reference frame. The regulator design is explored through the use of an example. The results are verified against the small-signal model, then PLECS simulations, and finally a laboratory experiment. The results indicate excellent agreement between the model and experiment during transients in voltage reference, input source voltage, and output load. A sensitivity analysis is performed based on the inverter model considering the parameter variation. Finally, loss and efficiency estimations are provided in this work.

Keywords: boost inverter; synchronous reference frame; small-signal model; voltage mode controller

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1. Introduction

Traditional full-bridge inverters are buck type, meaning that the generated output voltage magnitude is lower than that of the DC input voltage. To generate an output voltage that is larger in magnitude than the input voltage, an additional boost stage is needed. With the two-stage configuration, the input DC signal is first stepped up using a boost converter and then passed through a buck-type full-bridge inverter. The drawbacks of the two stage configuration are discussed in [1]. Additionally, the efficiency and footprint of the two stage system are not attractive. Considering the complexity of this multistage design, a simple single-stage boost inverter was first proposed by Cáceres and Barbi [2]. The proposed system was designed for a single-phase system. Using this method only four electronic switches are engaged, in contrast to the six switches that are used in a traditional two-stage inverter. Xue et al. in [3] reported that the inverter presented by Cáceres in [2] is one of the topologies of single-phase inverters for small distributed power generators. It is reported that this particular inverter topology has the capability to operate both as a stand-alone and grid-connected power supply unit. The suggested applications of this type of inverter can be found in solar photovoltaic units, wind turbine systems, and fuel cell inverters [4–6].

Several single-phase, single-stage, current-source-based inverters (CSI) are discussed in [7]. In [1], a modified modulation technique and a double-tuned resonant filter has been proposed to improve the harmonic response on the DC side with relatively small

inductance. The literature review in [7] discusses some challenges associated with the basic boost inverter structure. For improved operation, a new type of single-stage boost inverter is proposed in the same literature. However, the proposed model uses a series capacitor at the output to filter out the DC component which carries the fundamental current. In addition, the inverter fails to operate if a capacitive load is connected. The switched-capacitor differential boost inverter (SCDBI) discussed in [8,9] implemented a gain linearization strategy with the use of unipolar modulation (3L-PWM) resulting in a significant reduction of total harmonic distortion (THD) of the output voltage. However, the SCDBI inverter uses four additional switches. Although several single-stage inverter topologies exist in the literature [10–12], the one discussed in [2] has the simplest configuration.

Considering the simplicity of its operation, the inverter in [2] is discussed in this work. The inverter consists of two DC-DC synchronous boost converters. These converters are controlled independently. The inverter has four MOSFET/IGBT switches (two for each boost configuration), two inductors, and two capacitors. Identical inductors and capacitors are used for both converters. The load is connected differentially across the two output capacitors. With this configuration, the inverter was analyzed in [13] considering four different switching states. In [14], only two switching modes are considered. However, both analysis techniques excluded component parasitic from the discussion. The latter technique assumed one of the converters to be a fixed DC source which reduced the system dynamics to only one converter. The models describing the control-to-output relationship in [2,15] do not include component parasitic. The derived transfer functions contain higher-order polynomials in the denominator, which complicates controller design. In addition to that, the transfer functions for the open-loop input impedance and output impedance are not well explained in the previous work. In this work, the boost inverter operation is discussed using two operating modes. Converter dynamics from both the boost operations are considered in deriving the control-to-output transfer function. The mathematical modeling includes the component parasitic resulting in a more accurate representation of the system dynamics. Furthermore, the open-loop input and output impedance are derived and analyzed.

The primary control objective of a single-stage boost inverter is to regulate the individual converters in a way so as to generate a sinusoidal waveform with the nominal operating frequency added to a DC offset. The AC waveforms are 180° out of phase with respect to each other. The differential connection at the load terminals cancels out the DC offsets from both the converters, leaving a sinusoidal signal. The two algorithms that are commonly used in controlling boost inverters are the sliding mode controller and the current mode controller [4,16–22]. The major issues involving the sliding mode controller are variable switching frequency and complex operating theory [2,23]. The current-controlled theory presented in [18,24] overcomes these issues. However, linearization of the current-controlled model is difficult once control variables and states are considered. Both sliding mode and current-controlled mode controllers require the use of multiple voltage and current sensors.

To overcome these issues, a simple voltage-mode controller for operating the boost inverter is proposed in this work. The proposed controller requires only two voltage measurements. This results in a simpler controller algorithm that eliminates the need for an extra inner loop for current control. This in turn eliminates the need for current sensors and results in a cost-effective design. The voltage mode control of such an inverter was proposed in [25,26], in which a conventional proportional integral derivative (PID) regulator is used in both cases. However, that method suffers from a significant steady-state error in tracking the reference magnitude. Additionally, the presence of harmonic distortion and even harmonic components makes implementing such controllers impractical [27]. The other types of controller algorithm employed to control SCDBI-type inverters are a proportional resonant controller [8] and a modified proportional integral (PI) structure with an extra pole adjusted to attenuate the converter gain close to the resonance frequency [9].

In this work, a synchronous reference frame proportional integral controller (SRFPI) is proposed to control the boost inverter. The proposed controller overcomes the error

tracking issues. The SRFPI technique has been used previously in controlling the traditional voltage source inverters [28]. A list of novel contributions in this work includes:

- A detailed derivation of the quasi-steady state equivalent model of the system;
- An accurate AC small-signal mathematical modeling of the system considering the component parasitic;
- Experimental verification of the line-to-output transfer function, control-to-output transfer function, open-loop input impedance, and open-loop output impedance;
- Design of a voltage mode controller in the synchronous reference frame and selection of controller parameters;
- Estimation of loss and efficiency of the system.

The rest of the paper is organized as follows: Section 2 discusses the basics of the boost inverter operation using the duty cycle variation. Accurate mathematical models are proposed describing the converter dynamics in Section 3. The voltage mode controller design is explained in Section 4. Finally, the results from the simulation and the experimental procedure are presented with discussions in Section 5.

2. Basics of a Boost Inverter

The boost inverter proposed by Cacéres [2] is provided in Figure 1. The inverter uses two synchronous boost converters, marked as "Boost 1" and "Boost 2", that enable continuous current flow with no zero states or discontinuous conduction. The original model was proposed based on the assumption that the values of the passive components are identical in both the converters. In practice, inductor values are chosen such that $L_1 = L_2 = L$ and capacitor values are chosen as $C_1 = C_2 = C$. The boost sections are controlled separately to produce output voltages, v_{c1} and v_{c2}, appearing across the respective capacitors. The controllers are coordinated in a way that v_{c1} and v_{c2} are phase-shifted by 180° at all times, i.e.,

$$\begin{aligned} v_{c1} &= V_{dc} + \frac{V_m}{2}\cos\omega t \\ v_{c2} &= V_{dc} + \frac{V_m}{2}\cos(\omega t + \pi) \end{aligned} \tag{1}$$

where, V_{dc} denotes the dc offset voltage, V_m is the magnitude of the ac output, and ω is the nominal operating frequency in rad/s. If the load is connected across the capacitors, the final output voltage across the load is:

$$v_o = v_{c1} - v_{c2} = V_m \cos\omega t. \tag{2}$$

Notice the cancellation of the DC terms in (2). The cancellation occurs regardless of the power factor of the load. The output voltage has a magnitude that is twice of that of the one obtained from the individual converter's AC portion.

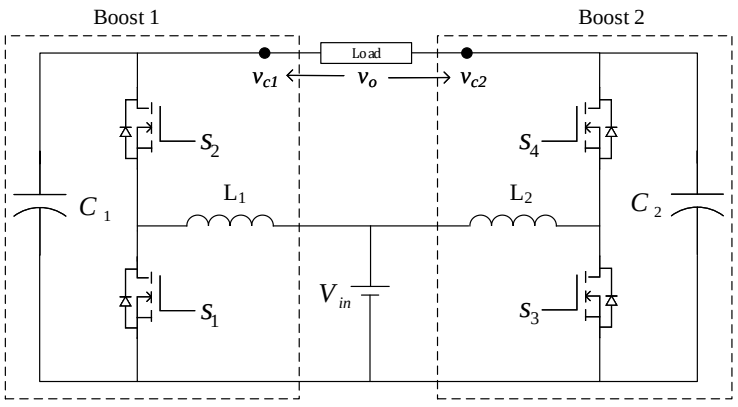

Figure 1. A DC-AC boost inverter.

The waveform analysis in [29] explains that the boost inverter switching may not be realized using only one duty cycle variation. Assuming duty cycles for the individual boost sections to be D_a and D_b respectively, four different cases can occur. These four cases are depicted in Figure 2.

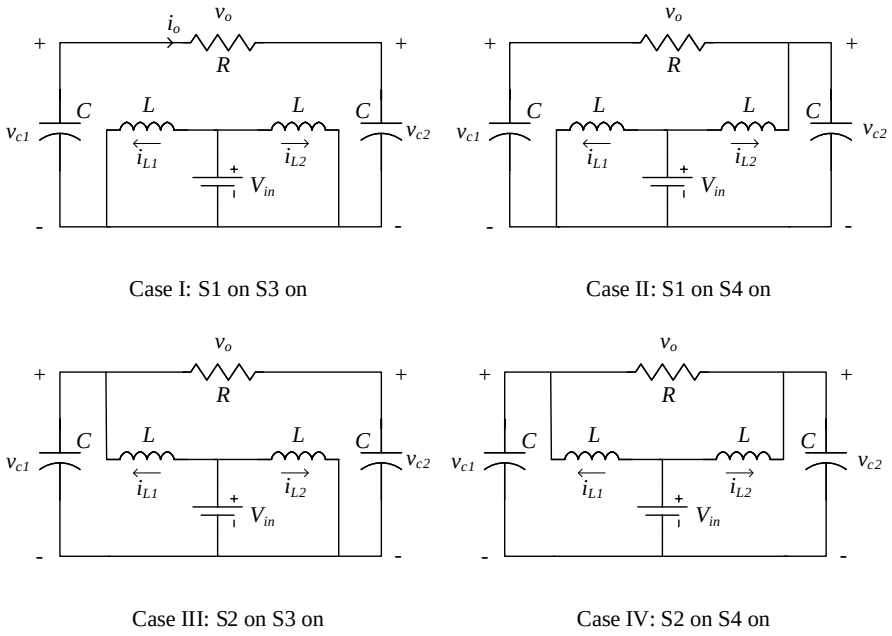

Figure 2. Four different switching cases for the boost inverter.

Only two out of these four cases can result in a sinusoidal voltage at the output. The following discussion provides a graphical representation of the duty cycles D_a and D_b and their relationship to the boost inverter output.

At steady-state, a conventional DC-DC boost converter produces an output voltage higher than the input voltage. The output is a fixed DC voltage with some high frequency switching ripple that is within an acceptable limit defined in the design process. In this particular configuration, the inverter consists of two boost converters, each producing a sinusoidally varying signal at a frequency much lower than the switching frequency with some DC offset. As a result, the duty cycle variations are very similar to the ones depicted in Figure 3. With the expectation that the duty cycles vary sinusoidally, both the waveforms in Figure 3 need to be centered around $D = 0.5$. That way the waveform symmetry is preserved as the waveforms neither clip at the floor nor saturates at the top. In that case, the AC variation has an amplitude of $\hat{d}$. These two duty cycle variations, D_a and D_b, maintain a 180° phase shift with respect to each other. To generalize the duty cycle variation expressions considering $D_a = d = D + \hat{d}$, the relationship between the duty cycles is:

$$D_b = 1 - D_a = 1 - (D + \hat{d}) = D' - \hat{d} = \hat{d}' \tag{3}$$

where, $D = D' = 0.5$.

This outcome indicates that Boost 1 inductor stores energy at the same time when Boost 2 inductor transfers energy to the load during $0 \leq \omega t < \pi$. This process reverses during the next half cycle when $\pi \leq \omega t < 2\pi$. The boost inverter operation is then limited to only two modes, Q_s and Q_s'. The switching signals S_1 and S_4 have identical switch commands Q_s, whereas switching signals S_2 and S_3 have commands Q_s'. This simplifies the mathematical modeling of the inverter to a great extent. The following section proposes a steady-state equivalent model and a small-signal model of the inverter system considering the component parasitic.

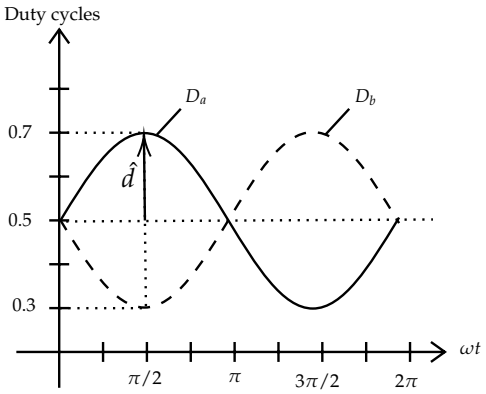

Figure 3. Boost inverter waveform analysis.

3. Mathematical Modeling of the System

The operating modes of the boost inverter are depicted in Figure 4. For the sake of simplicity, "Load" will be replaced by a linear resistor, R, during the discussion. The parameter definitions are provided in Table 1. The average current through the left capacitor over a complete cycle is:

$$\langle I_{C1} \rangle = 0 = -D\frac{V_o}{R} + D'(I_1 - \frac{V_o}{R}).$$

From which the value of I_1 is obtained as:

$$I_1 = \frac{V_o}{D'R}. \tag{4}$$

Following the same method, the average value of the inductor voltage found from the left inductor over a complete cycle is:

$$\langle V_{L1} \rangle = 0 = D(V_{in} - (r_L + r_{DS})I_1) + D'(V_{in} - (r_L + r_{DS})I_1 - r_C I_{C1} - V_{C1}).$$

In the second time interval, $I_{C1} = I_1 - \frac{V_o}{R}$. From this and from (4) we obtain:

$$0 = V_{in} - \frac{V_o}{D'R}r_1 - D'(V_{C1} - \frac{V_o}{R}r_C) \tag{5}$$

where, $r_1 = r_L + r_{DS} + D'r_C$.

Similarly, the average current through the second capacitor is:

$$\langle I_{C2} \rangle = 0 = -D'\frac{V_o}{R} + D(I_2 - \frac{V_o}{R})$$

which results in the value of I_2 as:

$$I_2 = \frac{V_o}{DR}. \tag{6}$$

Finally, considering $I_{C2} = I_2 - \frac{V_o}{R}$ in the first time interval and $r_2 = r_L + r_{DS} + Dr_C$ the average value of the remaining inductor voltage over a complete cycle is:

$$\langle V_{L2} \rangle = 0 = D(V_{in} - (r_L + r_{DS})I_2 - r_C I_{C2} - V_{C2}) + D'(V_{in} - (r_L + r_{DS})I_2)$$

resulting in:

$$0 = V_{in} - \frac{V_o}{DR}r_2 - D'(V_{C2} - \frac{V_o}{R}r_C). \tag{7}$$

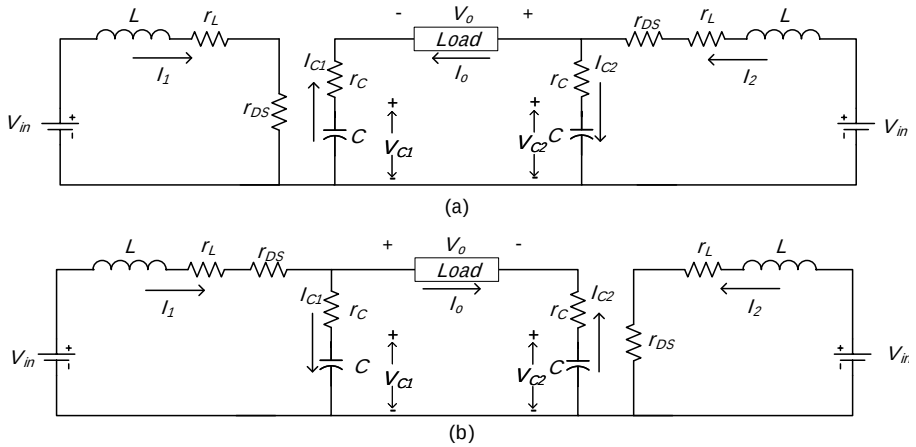

Figure 4. Boost inverter active operating modes for (**a**) $S_1 = S_4 = 1, S_2 = S_3 = 0$ and (**b**) $S_1 = S_4 = 0$, $S_2 = S_3 = 1$.

Table 1. Sample boost inverter parameters.

Component	Parameter	Value
Capacitors	C_1, C_2	10 µF
Capacitor ESR	r_C	0.1 Ω
Inductors	L_1, L_2	270 µH
Inductor ESR	r_L	0.20 Ω
MOSFET 'on' Resistance	r_{DS}	0.10 Ω
Load Resistance	R	50 Ω
Supply Voltage	V_{in}	10 V

3.1. Quasi-Steady-State Equivalent Circuit Modeling

Taking (4) through (7) into considerations, the steady-state equivalent model of the boost inverter is formulated. The proposed steady-state equivalent model of the inverter is presented in Figure 5. From Figure 5c the individual converter outputs are:

$$V_{o1} = V_{C1} - \frac{V_o}{R} r_C = \frac{V_{in}}{D'} - \frac{r_1}{D'^2} \frac{V_o}{R} \tag{8}$$

$$V_{o2} = V_{C2} - \frac{V_o}{R} r_C = \frac{V_{in}}{D} + \frac{r_2}{D^2} \frac{V_o}{R}. \tag{9}$$

Since, the output voltage across the load resistor is $V_o = V_{o1} - V_{o2}$, after subtracting (9) from (8) and then rearranging the terms gives the output-to-input ratio as:

$$G_V = \frac{V_o}{V_{in}} = \frac{2D-1}{D(1-D)} \times \frac{1}{1 + \frac{1}{R}\left(\frac{r_1}{D'^2} + \frac{r_2}{D^2}\right)}. \tag{10}$$

If the loss terms are not included, the voltage gain in (10) simply contains the gain factor M where, $M = \frac{2D-1}{D(1-D)}$.

After substituting the parameter values from Table 1 the steady-state characteristic plots are obtained for different values of duty cycles. They are presented in Figure 6. The plot for G_V in Figure 6a shows that at $D = 0.5$ the output-to-input ratio becomes zero.

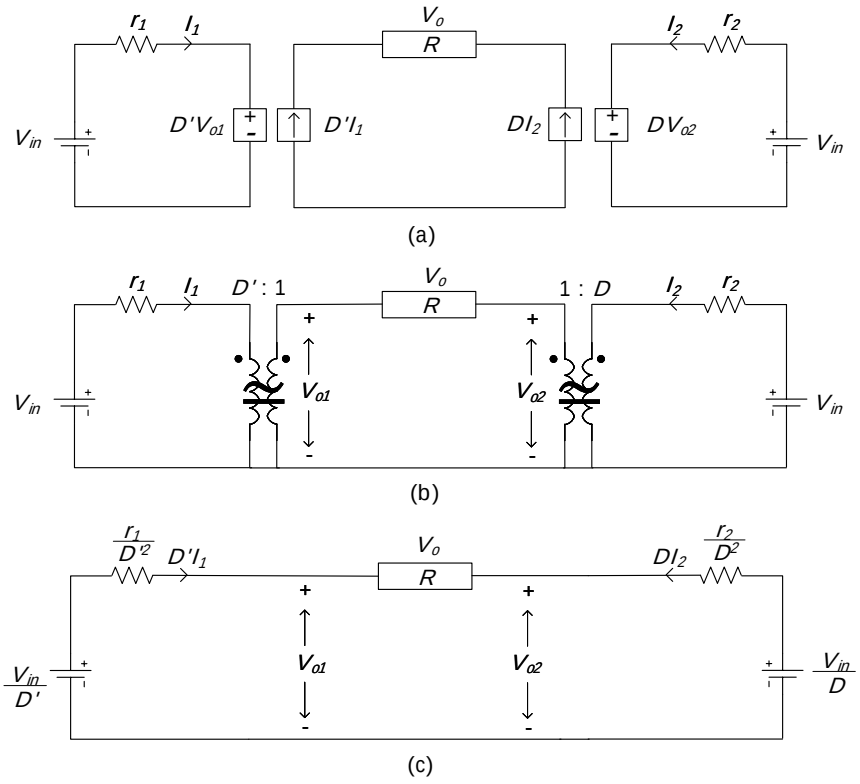

Figure 5. The steady-state equivalent model of the boost inverter. (**a**) Steady-state equivalent from the equations, (**b**) standard canonical approximation, and (**c**) simplified equivalent model.

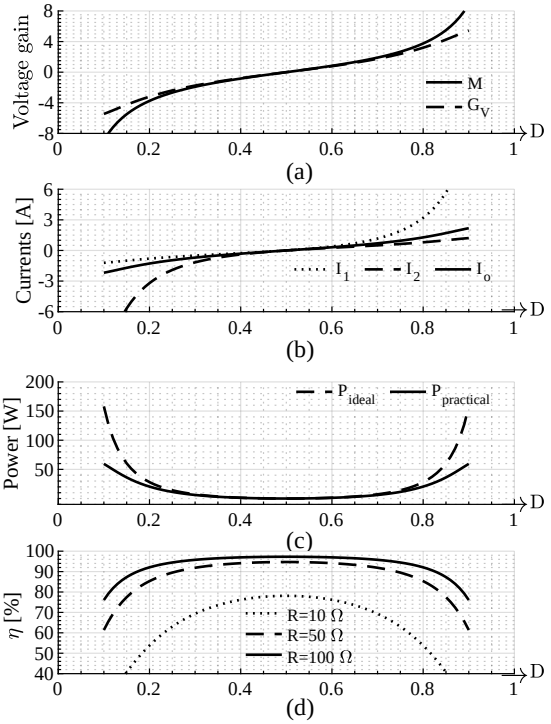

Figure 6. The characteristic plots obtained from the steady-state equivalent model as the duty cycle is varied: (**a**) Voltage gain with and without parasitic losses included, (**b**) individual converter and inverter currents, (**c**) inverter power considering the conduction losses only, and (**d**) efficiency considering the conduction losses only for three different load values as the duty cycle is varied.

The voltage gain lines, G_V and M, start to deviate away from linearity noticeably below $D = 0.2$ and above $D = 0.8$. Those are the practical limits of the inverter duty cycle. The gain curves match very closely between $0.25 \leq D \leq 0.75$. To know the current limits of individual converters, inductor currents at different duty cycles are determined. Referring to (4) and (6), the individual inductor currents are:

$$I_1 = \frac{V_{in}}{R} \times \frac{2D-1}{D(1-D)^2} \times \frac{1}{1+\frac{1}{R}\left(\frac{r_1}{D'^2}+\frac{r_2}{D^2}\right)} \tag{11}$$

$$\text{and } I_2 = \frac{V_{in}}{R} \times \frac{2D-1}{D^2(1-D)} \times \frac{1}{1+\frac{1}{R}\left(\frac{r_1}{D'^2}+\frac{r_2}{D^2}\right)}. \tag{12}$$

The two inductor currents, I_1 and I_2, and the output current, I_o, are plotted for varying duty cycles in Figure 6b. A significant increase in inductor currents is noticed outside the range of $0.3 \leq D \leq 0.7$. These currents follow non-linear characteristics for a wide range of duty cycle meaning that the inductor currents are non-sinusoidal for the most part of the inverter operation. However, the output current stays linear for a range determined by the G_V curve in Figure 6a. The system conduction loss depends on I_1, I_2, and the component parasitic. Since, $D'I_1 = -DI_2$ the efficiency of the inverter is:

$$\eta = \frac{P_o}{P_{in}} = \frac{V_o D' I_1}{V_{in}(I_1+I_2)} \times 100 = \frac{1}{1+\frac{1}{R}\left(\frac{r_1}{D'^2}+\frac{r_2}{D^2}\right)} \times 100\%. \tag{13}$$

A comparison of active power output with and without the conduction losses is depicted in Figure 6c. As expected, the output power reduces significantly as the loss terms are included in the mathematical model. In Figure 6d, the system efficiency is presented at three different load values as the duty cycle is varied. With the increase in load resistance, fewer I^2R losses occur due to low current through the component parasitic. The efficiency calculation in (13) is significant in determining the load value that can be used in this particular boost inverter arrangement. For an accurate determination of the system efficiency, the other forms of losses such as the switching loss, dead time loss, gate charge loss, core losses in the inductor, etc. are needed to be calculated. The relationship between equivalent resistances, r_1 and r_2, due to the parasitic components of the circuit elements is:

$$r_2 = r_1 + r_C(1-2D'). \tag{14}$$

At $D = 0.5$, these two resistances become equal.

3.2. Small-Signal AC Modeling

The inverter small-signal AC model is obtained considering a small perturbation around the stable operating points. The quantities averaged over a cycle of the switching frequency, f_{sw}, is the summation of the DC components and the AC: components

$$v_{in} = V_{in} + \hat{v}_{in} \tag{15}$$
$$v_{L1} = V_{L1} + \hat{v}_{L1} \tag{16}$$
$$i_1 = I_1 + \hat{i}_1 \tag{17}$$
$$v_{L2} = V_{L2} + \hat{v}_{L2} \tag{18}$$
$$i_2 = I_2 + \hat{i}_2 \tag{19}$$
$$v_{C1} = V_{C1} + \hat{v}_{C1} \tag{20}$$
$$i_{C1} = I_{C1} + \hat{i}_{C1} \tag{21}$$
$$v_{C2} = V_{C2} + \hat{v}_{C2} \tag{22}$$
$$i_{C2} = I_{C2} + \hat{i}_{C2} \tag{23}$$

$$d = D + \hat{d} \tag{24}$$

$$d' = D' - \hat{d}. \tag{25}$$

Substituting (15) through (25) in (4)–(7) and then equating the AC terms and neglecting the terms given by the product of two AC terms on both sides results in:

$$0 = \hat{v}_{in} + \hat{d}(I_1 r_C + V_{C1} - \frac{V_o}{R} r_C) - \hat{i}_1 r_1 - D'(\hat{v}_{C1} - \frac{\hat{v}_o}{R} r_C) \tag{26}$$

$$0 = \frac{\hat{v}_o}{R} + \hat{d} I_1 - D' \hat{i}_1 \tag{27}$$

$$0 = \hat{v}_{in} - \hat{d}(I_2 r_C + V_{C2} - \frac{V_o}{R} r_C) - \hat{i}_2 r_2 - D(\hat{v}_{C2} - \frac{\hat{v}_o}{R} r_C) \tag{28}$$

$$0 = \frac{\hat{v}_o}{R} - \hat{d} I_2 - D \hat{i}_2. \tag{29}$$

The small-signal AC model of the boost inverter is obtained based on the results in (26) through (29). The AC equivalent model is depicted in Figure 7 where, $\hat{v}_{o1} = \hat{v}_{C1} - \frac{\hat{v}_o}{R} r_C$ and $\hat{v}_{o2} = \hat{v}_{C2} - \frac{\hat{v}_o}{R} r_C$.

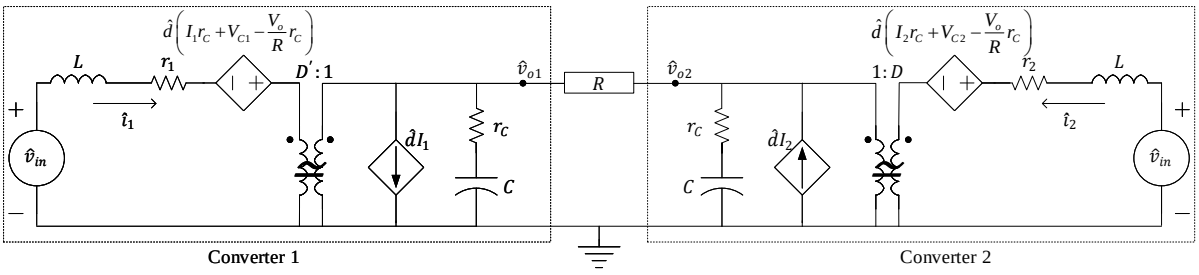

Figure 7. The AC equivalent model of the boost inverter.

3.3. Line to Output Transfer Function

To obtain the line-to-output transfer function, $G_{vg} = \frac{\hat{v}_o}{\hat{v}_{in}}$, the small-signal perturbation value $\hat{d}$ is set to zero. The equivalent diagram is presented in Figure 8. After that, a Thévenin equivalent circuit with a source, $\hat{v}_{th}$, and an impedance, Z_{th}, is determined from the load's perspective.

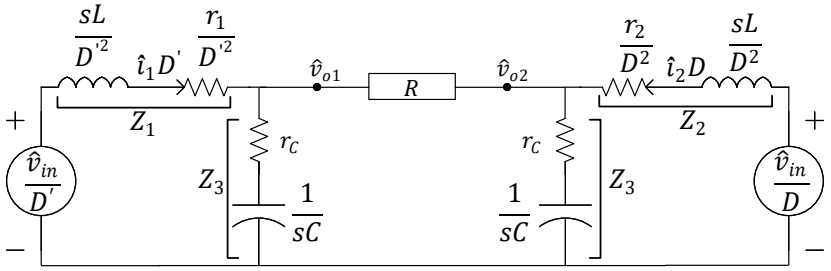

Figure 8. The ac equivalent model for obtaining the line to output transfer function.

Removing the load and looking back from the load terminals the Thévenin's equivalent impedance is:

$$Z_{th} = Z_1 || Z_3 + Z_2 || Z_3. \tag{30}$$

where:

$$Z_1 = \frac{sL + r_1}{D'^2}; Z_2 = \frac{sL + r_2}{D^2}; Z_3 = \frac{1}{sC} + r_C. \tag{31}$$

The Thévenin's equivalent source is determined as:

$$\hat{v}_{th} = \hat{v}_{in}\left(\frac{1}{D'}\frac{Z_3}{Z_1 + Z_3} - \frac{1}{D}\frac{Z_3}{Z_2 + Z_3}\right). \tag{32}$$

Finally, applying the voltage divider rule, the line-to-output transfer function is:

$$G_{vg}\Big|_{\hat{d}=0} = \frac{\hat{v}_o}{\hat{v}_{in}} = \left(\frac{1}{D'}\frac{Z_3}{Z_1 + Z_3} - \frac{1}{D}\frac{Z_3}{Z_2 + Z_3}\right)\frac{1}{1 + \frac{Z_{th}}{R}}. \tag{33}$$

It is interesting to note that the impedances Z_1 and Z_2 become equal at $D = 0.5$. The expression then becomes equal to that of the one in (10). At $D = 0.5$, the transfer function becomes equal to zero. That means this configuration is immune to any perturbation in the input source provided D (that is, the center point of duty ratio variation) always stays at 0.5. For any other values, any variation in the input will have an effect on the output response. The Bode plots in Figure 9 obtained from the small-signal model and the experimental results match closely at $D = 0.7$. The Bode plots overlap for a large range of frequencies.

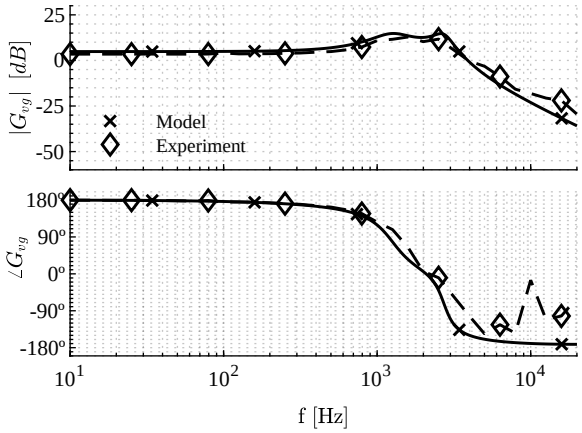

Figure 9. Bode plot comparison of audio susceptibility at D = 0.7. The results obtained from the small-signal line-to-output transfer function is compared with that of the one obtained from the experimental test bed.

3.4. Control-to-Output Transfer Function

The control-to-output transfer function, $G_{vd} = \frac{\hat{v}_o}{\hat{d}}$, is determined by setting $\hat{v}_{in}$ to zero in the AC equivalent model. The equivalent diagram is given in Figure 10 where, $\hat{v}_{left}$ and $\hat{v}_{right}$ are $\hat{d}\left(I_1 r_C + V_{C1} - \frac{V_o}{R} r_C\right)/D'$ and $\hat{d}\left(I_2 r_C + V_{C2} - \frac{V_o}{R} r_C\right)/D$ respectively. After applying the source transformation technique and determining the equivalent current sources, the currents going into nodes $\hat{v}_{01}$ and $\hat{v}_{02}$ are:

$$\hat{i}_{left} = \hat{d}\left(\frac{1}{Z_1 D'}\left(I_1 r_C + V_{C1} - \frac{V_o}{R} r_C\right) - I_1\right) \tag{34}$$

and

$$\hat{i}_{right} = \hat{d}\left(I_2 - \frac{1}{Z_2 D}\left(I_2 r_C + V_{C2} - \frac{V_o}{R} r_C\right)\right) \tag{35}$$

respectively. Since, the duty cycle is varied around 0.5, the average duty cycle becomes:

$$D = D' = 0.5. \tag{36}$$

This in turn results in:

$$Z_1 = Z_2. \tag{37}$$

Moreover, from Figure 5c we obtain:

$$V_o = 0 \quad \text{as a result,} \quad V_{C1} = V_{C2}, \tag{38}$$

$$|I_1| = |I_2|. \tag{39}$$

The rest of the calculations are greatly simplified as $\hat{i}_{left}$ becomes equal to $-\hat{i}_{right}$.

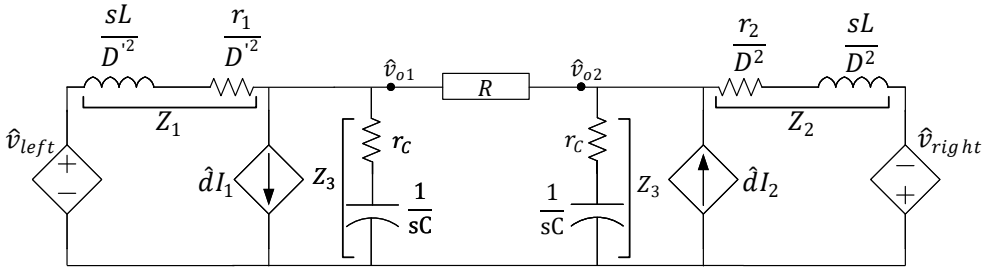

Figure 10. The ac equivalent model for obtaining the control-to-output transfer function.

Afterwards, the superposition theorem is applied to the network to determine the node voltages considering one source at a time. With the presence of $\hat{i}_{left}$ alone in the system, the equations relating to the node voltages are:

$$\hat{d}\left(\frac{1}{Z_1 D'}(I_1 r_C + V_{C1}) - I_1\right) = \hat{v}'_{o1}\left(\frac{1}{Z_1||Z_3} + \frac{1}{R}\right) + \hat{v}'_{o2}\left(\frac{-1}{R}\right) \tag{40}$$

$$0 = \hat{v}'_{o1}\left(\frac{-1}{R}\right) + \hat{v}'_{o2}\left(\frac{1}{Z_1||Z_3} + \frac{1}{R}\right). \tag{41}$$

For simplified representation of the terms assuming:

$$\beta = \frac{1}{Z_1 D'}(I_1 r_C + V_{C1}) - I_1 \tag{42}$$

$$\gamma = \frac{1}{R} \tag{43}$$

$$\Delta = \frac{1}{Z_1||Z_3} + \frac{1}{R}. \tag{44}$$

Solving (40) and (41):

$$\frac{\hat{v}'_{o1}}{\hat{d}} = \beta\left(\frac{\Delta}{\Delta^2 - \gamma^2}\right) \tag{45}$$

and

$$\frac{\hat{v}'_{o2}}{\hat{d}} = \beta\left(\frac{\gamma}{\Delta^2 - \gamma^2}\right). \tag{46}$$

After that, considering the $\hat{i}_{right}$ source alone and following a similar approach gives:

$$\frac{\hat{v}_{o1}''}{\hat{d}} = \beta\left(\frac{-\gamma}{\Delta^2 - \gamma^2}\right) \tag{47}$$

and

$$\frac{\hat{v}_{o2}''}{\hat{d}} = \beta\left(\frac{-\Delta}{\Delta^2 - \gamma^2}\right). \tag{48}$$

By considering (49) and by substituting in it (45) through (48) the control to output transfer function becomes:

$$\left(\frac{\hat{v}_{o1}'}{\hat{d}} + \frac{\hat{v}_{o1}''}{\hat{d}}\right) - \left(\frac{\hat{v}_{o2}'}{\hat{d}} + \frac{\hat{v}_{o2}''}{\hat{d}}\right) = \frac{\hat{v}_o}{\hat{d}} \tag{49}$$

$$G_{vd}\Big|_{\hat{v}_{in}=0} = 2\beta\left(\frac{1}{\Delta+\gamma}\right). \tag{50}$$

The control-to-output transfer function in (50) is much less complicated compared to the transfer functions derived in [2] or [25]. Furthermore, the proposed transfer function includes the component parasitic resulting in an accurate mathematical model of the system. The complete expression of the transfer function is given in (51):

$$G_{vd}(s) = 2V_{in} \times \frac{1 + sCr_C}{s^2\left(LC + \frac{2LCr_C}{R}\right) + s\left(2\frac{L}{R} + 2\frac{Cr_Cr_1}{R} + D'^2Cr_C + Cr_1\right) + \left(\frac{2r_1}{R} + D'^2\right)}. \tag{51}$$

Ignoring the parasitic losses the transfer function becomes:

$$\frac{\hat{v}_o}{\hat{d}} = \frac{2(D'V_{C1} - I_1sL)}{s^2LC + 2s\frac{L}{R} + D'^2} = \frac{2V_{in}}{s^2LC + 2s\frac{L}{R} + D'^2}. \tag{52}$$

This helps to quickly determine the dominant poles of the system. It is interesting to note that unlike (52), the transfer function including the loss terms in (51) contains a zero. This results from using our assumption at (36) into (10) resulting in DC average values $V_o = 0$ and $I_1 = 0$ from (5). This eliminates the zero and using (8) the numerator simply becomes $2V_{in}$. The physical interpretation of (52) is that when the individual DC-DC converters operate at an average duty cycle of 0.5, the average DC voltage output from both the converters becomes equal. Since the load is connected differentially, the average load voltage would then become zero which results in an average inductor current from each converter being zero. As a result, the right half-plane zero vanishes leaving the input voltage in the numerator with a gain factor of two.

The validity of the proposed transfer function is tested using the experimental test bed. The Bode plots of the control-to-output transfer function obtained using both the mathematical model and the experimental results are provided in Figure 11. The Bode magnitude and phase responses match closely. The only discrepancy that happens around 15 kHz is mainly due to the inclusion of the switching frequency during the experiment. However, this region is beyond the range where the averaging performed in preceding sections is valid. The resonant frequency occurs at:

$$\omega_o = \sqrt{\frac{2r_1 + D'^2R}{RLC + 2LCr_C}}. \tag{53}$$

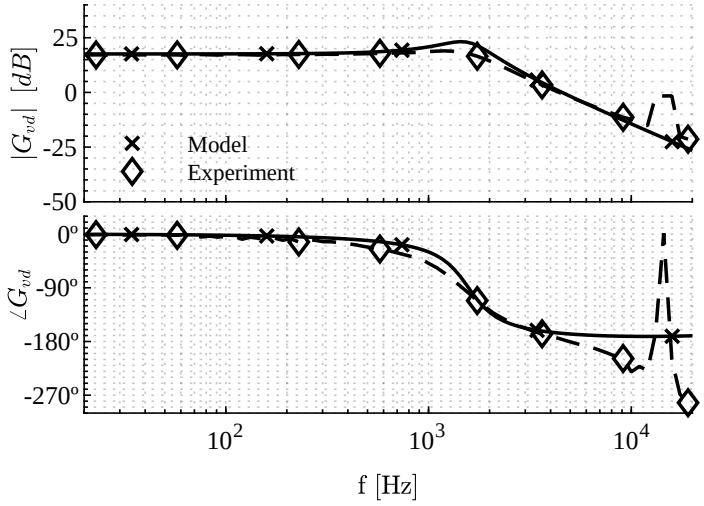

Figure 11. Bode plot comparison of control-to-output transfer function from the small-signal model and experimental test bed.

The control-to-output Bode plot has a peak value that occurs at the resonant frequency, f_r, of 1570 Hz and the measure of the dissipation in the system, $Q = 5$ dB from the model whereas from the experimental results it is 1.8 dB. Both f_r and Q are impacted by the boost inverter capacitor selection. Figure 12 illustrates the impact of capacitance, C, and the capacitor ESR, r_C, on the transfer function. Capacitance primarily affects the resonant frequency with only a modest impact on Q; whereas, ESR primarily affects Q with only a modest impact on f_r. Thus a slight increase in ESR can substantially improve the transient behavior of the boost inverter by reducing Q. However, such a design selection can significantly impact converter efficiency. Therefore, ESR can be an important tradeoff to optimize.

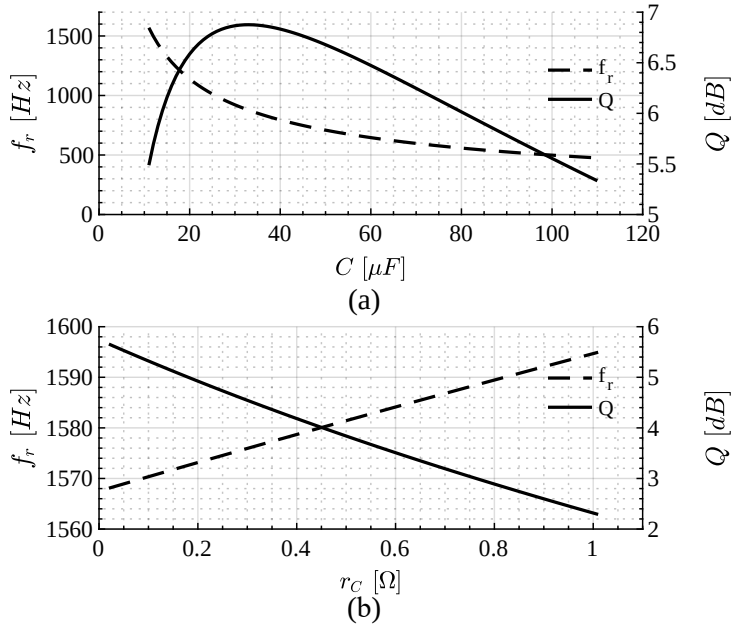

Figure 12. Variation of the resonant frequency and Q as: (**a**) C is varied and (**b**) r_C is varied.

3.5. Open-Loop Input Impedance

The open-loop input impedance, Z_i, is determined after setting the duty cycle perturbation $\hat{d}$ to zero. Under this condition, the equivalent diagram becomes very similar to that of the one presented in Figure 8. The equivalent voltage sources produce $\hat{i}_1$ and $\hat{i}_2$ through Z_1 and Z_2 respectively. The expression of the input impedance then becomes:

$$Z_i = \left.\frac{\hat{v}_i}{\hat{i}_1 + \hat{i}_2}\right|_{\hat{d}=0}. \tag{54}$$

Considering the current $\hat{i}_o$ flowing from node $\hat{v}_{o1}$ to node $\hat{v}_{o2}$, the three mesh equations are:

$$\begin{bmatrix} (Z_1+Z_3)D' & 0 & -Z_3 \\ -Z_3D' & Z_3D & 2Z_3+R \\ 0 & (Z_2+Z_3)D & Z_3 \end{bmatrix} \begin{bmatrix} \hat{i}_1 \\ \hat{i}_2 \\ \hat{i}_o \end{bmatrix} = \begin{bmatrix} \frac{\hat{v}_{in}}{D'} \\ 0 \\ \frac{\hat{v}_{in}}{D} \end{bmatrix}. \tag{55}$$

This results in $\frac{\hat{i}_1}{\hat{v}_{in}}$, $\frac{\hat{i}_2}{\hat{v}_{in}}$, and $\frac{\hat{v}_{in}}{\hat{i}_1+\hat{i}_2}$ as follows:

$$\frac{\hat{i}_1}{\hat{v}_{in}} = \frac{Z_3^2(2D-1) + DR(Z_2+Z_3) + 2DZ_2Z_3}{DD'^2(Z_3^2(R+Z_1+Z_2) + R(Z_1Z_2+Z_1Z_3+Z_2Z_3) + 2Z_1Z_2Z_3)} \tag{56}$$

$$\frac{\hat{i}_2}{\hat{v}_{in}} = -\frac{RZ_1 + RZ_3 + 2Z_1Z_3 - Z_3^2(2D-1) - DR(Z_1+Z_3) - 2DZ_1Z_3}{D^2D'(Z_3^2(R+Z_1+Z_2) + R(Z_1Z_2+Z_1Z_3+Z_2Z_3) + 2Z_1Z_2Z_3)} \tag{57}$$

$$\begin{aligned} Z_i &= \frac{\hat{v}_{in}}{\hat{i}_1 + \hat{i}_2} \\ &= \frac{D^2D'^2(Z_3^2(R+Z_1+Z_2) + R(Z_1Z_2+Z_1Z_3+Z_2Z_3) + 2Z_1Z_2Z_3)}{R(Z_1+Z_3)(1+2D) + 2D'^2Z_1Z_3 + 2D^2Z_3(R+Z_2) - Z_3^2(4DD'-1) + D^2R(Z_1+Z_2)}. \end{aligned} \tag{58}$$

3.6. Open-Loop Output Impedance

The open-loop output impedance of the boost inverter is determined considering perturbation at the load side. Considering $\hat{d} = 0$ and $\hat{v}_{in} = 0$ in Figure 7 the output impedance becomes:

$$Z_o = \left.\frac{\hat{v}_o}{\hat{i}_o}\right|_{\hat{d}=0;\hat{v}_{in}=0} = (Z_1||Z_3 + Z_2||Z_3)||R. \tag{59}$$

Substituting (31) in (58) and in (59) gives the input impedance and output impedance transfer functions respectively. Furthermore, using the values listed in Table 1, the transfer functions Z_i and Z_o are determined at $D = D' = 0.5$. The corresponding Bode plots depicted in Figure 13 compares the small-signal results with the experimental results. The input impedance reaches the lowest value at a frequency that produces a resonating effect in the system. The output impedance becomes maximum at that same resonance frequency. Although, the magnitude plots match very closely, the phase plots show some deviation which can be largely attributed to the length of the cables attached to both the input and output sides of the inverter along with the possible impedance mismatch during the measurement.

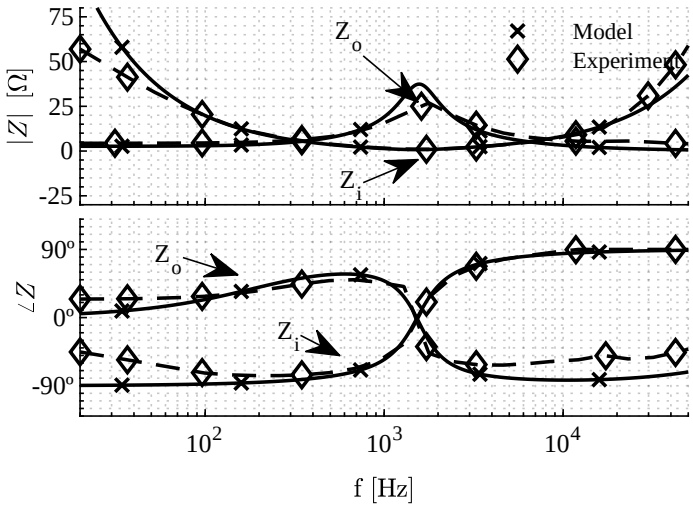

Figure 13. Bode plot for the open-loop input and open-loop output impedances at D = D′ = 0.5.

4. Voltage Mode Controller Design

In this section, the control-to-output transfer function in (51) is used to design a voltage mode controller for the boost inverter. A conventional voltage mode controller uses a simple proportional integral (PI) controller for reference tracking. However, this approach suffers from errors in terms of magnitude mismatch and phase delay when tracking a sinusoidal signal. For a precise reference tracking, the synchronous reference frame proportional integral (SRFPI) controllers are often deployed in power electronics. An SRFPI provides control over both the direct and quadrature axis components of the reference sine wave. The top view of the overall system architecture is depicted in Figure 14. Only one voltage controller is needed to operate the system. The output of this controller produces the required duty cycle variation $\hat{d}$. This variation is then combined with the fixed duty cycle D to produce the final duty cycles, $D \pm \hat{d}$. The PWM signals for the respective boost converters are generated for controlling the individual boost sections.

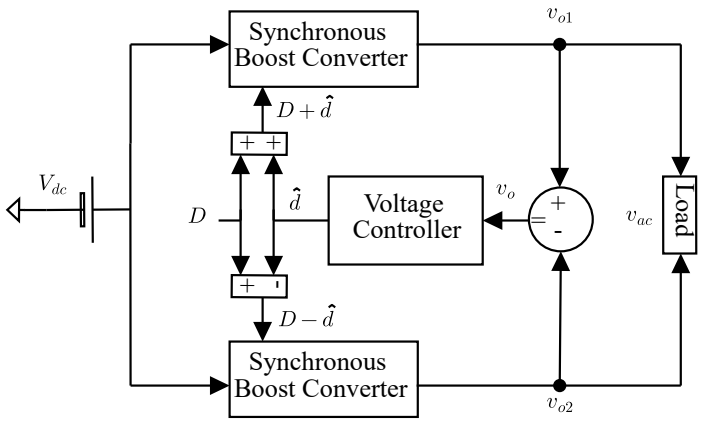

Figure 14. Top view of the overall system.

The SRFPI voltage control algorithm applied to the current system is presented in Figure 15. The measured load voltage, $\hat{v}_o$, is reduced by a factor of two because each converter produces half the output voltage. This scaled-down voltage is termed as v_α. After that, a fictitious orthogonal signal, v_β, is generated by applying an all-pass filter that produces a $\frac{\pi}{2}$ delay at ω:

$$G_{shift}(s) = \frac{-s + \omega}{s + \omega}. \tag{60}$$

The $v_{\alpha\beta}$ signals are then converted into direct and quadrature axis components, v_d and v_q, using the Park transformation matrix:

$$T_{\alpha\beta\to dq} = \begin{bmatrix} \cos\omega t & \sin\omega t \\ -\sin\omega t & \cos\omega t \end{bmatrix}. \tag{61}$$

The v_{dq} signals are compared against the reference values, v_d^* and v_q^*. The resulting error signals are passed through the PI controllers. The PI controller outputs are transformed back to $v_{i\alpha}$ and $v_{i\beta}$ using the inverse Park transformation matrix, $T^{-1}_{\alpha\beta\to dq}$. In the final step, $v_{i\alpha}$ goes through the pulse-width-modulator to generate the switching signals. The transfer function of the PWM is:

$$G_m(s) = \frac{1}{v_d^*} e^{-j\omega T_d} \tag{62}$$

where, T_d is the digital control delay and $\frac{1}{v_d^*}$ is the static gain. The overall system uses only one frequency, i.e., one time-base, as a reference.

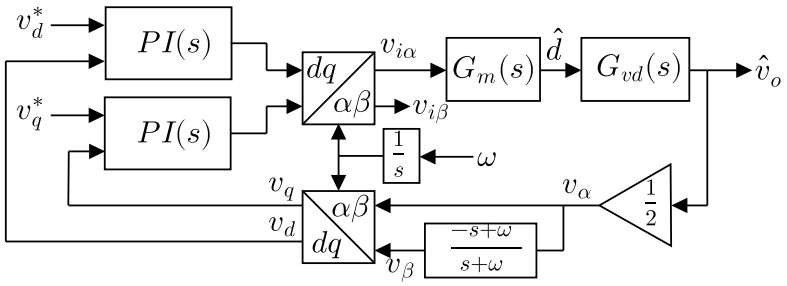

Figure 15. Boost inverter voltage mode controller block diagram.

Tuning an SRFPI controller is challenging. The process is simplified by first rearranging the blocks in Figure 15 and then applying the well-known control theories. The simplified block diagram presented in Figure 16 has the reference expressed in the rotating reference frame.

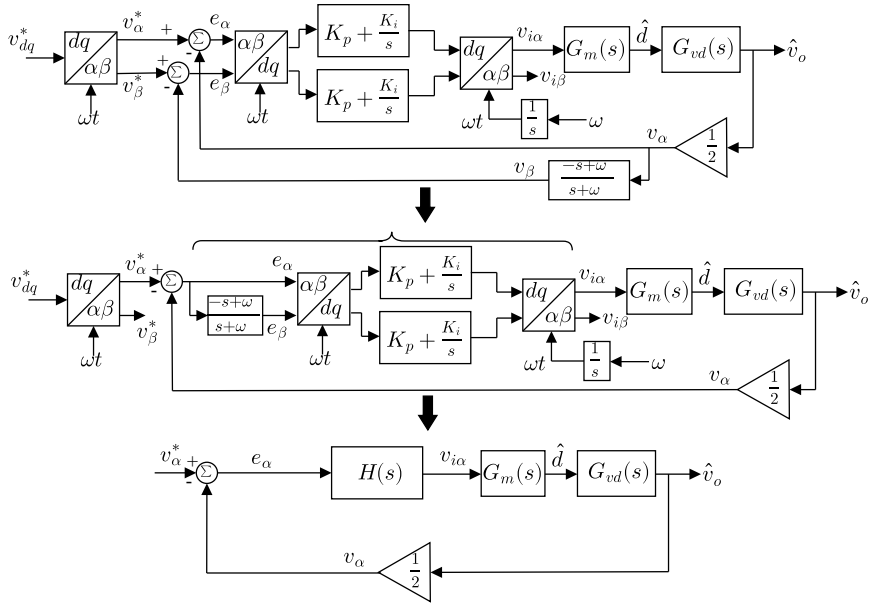

Figure 16. Controller block diagram is rearranged and simplified.

The error signal, e_β, is realized using (60) when the sinusoidal voltage is maintained at ω. The e_β can be written in terms of e_α as:

$$e_\beta = v_\beta^* - v_\beta = G_{shift}(v_\alpha^* - v_\alpha) = G_{shift} \cdot e_\alpha. \tag{63}$$

This results in an additional reduction in the block diagram as only v_α^* exists in the simplified model. Setting the q axis reference, v_q^*, to 0, the reference reduces to:

$$v_\alpha^* = v_d^* \cos \omega t - v_q^* \sin \omega t = v_d^* \cos \omega t. \tag{64}$$

A further simplification is performed following the same technique described in [30,31]. The stationary reference frame equivalent of the voltage loop is deduced as shown inside the curly braces in Figure 16. The transfer function relating the expected output voltage, $v_{i\alpha}$, to the voltage error, e_α is:

$$H(s) = K_p + \frac{K_i}{s^2 + \omega^2}\left(s - \omega \times \frac{-1 + \frac{\omega}{s}}{1 + \frac{\omega}{s}}\right). \tag{65}$$

The controller design objectives are: (a) The loop-gain bandwidth (ω_c) is $\frac{1}{9.21}$ of the switching frequency (ω_{sw}) and (b) the ω_c is achieved at a phase margin (ϕ_m) of 45°. The loop gain of the simplified system is:

$$G_{ol}(s) = H(s) \times G_m(s) \times G_{vd}(s) \times 0.5. \tag{66}$$

For faster calculations of regulator parameters, K_p and K_i, the $H(s)$ can be approximated to:

$$\begin{aligned} H(j\omega_c) &= K_p + \frac{K_i}{-\omega_c^2 + \omega^2}\left(j\omega_c - \omega \times \frac{-1 + \frac{\omega}{j\omega_c}}{1 + \frac{\omega}{j\omega_c}}\right) \\ &\approx K_p + \frac{K_i}{-\omega_c^2 + \omega^2}(j\omega_c + \omega) \\ |H(s)| &\cong |K_p|. \end{aligned} \tag{67}$$

This approximation is valid as long as $\omega_c > \omega$ and $|K_p|^2 \gg \left|\frac{K_i}{\omega_c}\right|^2$. The condition $\omega_c > \omega$ is usually satisfied, since ω_c is set about $\omega_{sw}/10$, and $\omega_{sw} >> \omega_c$.

Applying the values listed in Tables 1 and 2 to (66) for an input voltage of 22 V and load reistance of 220 Ω and then setting $|G_{ol}(j\omega_c)| = 1$, the proportional gain becomes:

$$K_p \approx 0.077218. \tag{68}$$

The parameter K_i is calculated based on the phase margin requirement:

$$\angle G_{ol}(j\omega_c) = -180^\circ + \phi_m. \tag{69}$$

Evaluating the angular contributions from (51) and (62), and using the value of K_P in (65), the K_i value is found from (69). The integral gain becomes:

$$K_i \approx 33.732\,\text{rad/s}. \tag{70}$$

A quick check on the assumptions made earlier shows that $\omega_c (= 10.2\,\text{krad/s})$ is 27 times greater than $\omega (= 377\,\text{rad/s})$. In addition, the value of $|K_p|^2 (= 0.006)$ is approximately 545 times larger than the value of $|K_i/\omega_c|^2 (= 1.1 \times 10^{-5})$.

Table 2. Boost inverter operating conditions

Component	Parameter	Value
Nominal frequency	ω	377 rad/s
Switching frequency	f_{sw}	15 kHz
Set point voltage	v_d^*	25 V
Closed loop bandwidth	ω_c	10.2 krad/s
Phase margin	ϕ_m	45°

The closed-loop transfer function and the loop-gain Bode plots are depicted in Figure 17. A very high loop gain of 300 dB is achieved at the nominal frequency of 60 Hz. To observe the gain plots around 0 dB more closely, a truncated magnitude plot is presented. The phase plot confirms that the desired phase margin of 45° is obtained.

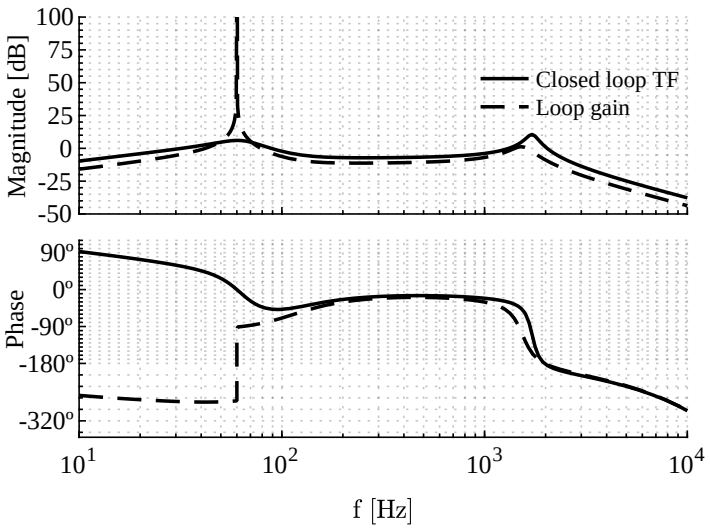

Figure 17. Bode plots for the CLTF and the loop gain.

5. Results and Discussions

The inverter operation is tested with the newly designed regulator gains. The results obtained from the small-signal mathematical model, the full order PLECS simulation, and the experimental test bed are compared and discussed in this section.

5.1. Simulation Results

Both the small-signal mathematical model and the full order model with the component parasitic are simulated in the PLECS platform. Three different perturbation cases are considered to check the system dynamics. These cases are discussed below.

5.1.1. Change in Reference

A step-change in the reference voltage is made at $t = 0.1$ s. The input voltage is kept constant at 22 V. The output voltage reference v_d^* increases from 15 V to 25 V. Figure 18 shows that, as a consequence, the peak value of the output voltage increases from 30 V to 50 V. In Figure 18, the transient responses closely agree when the full order model results are matched with that of the one obtained from the small-signal (SS) model results. The transients cease within a cycle or two. After that, a zero steady-state error is maintained. The 15 kHz switching transients are visible in the v_{dq} waveform. These switching ripples do not appear in the final output due to the natural low-pass filter characteristics of the inverter.

In Figure 19, the individual converter output voltages are depicted. The voltages represent an AC variation at the fundamental frequency added to a DC offset. The DC offset is equal in magnitude in both waveforms. The AC components are 180° out of phase.

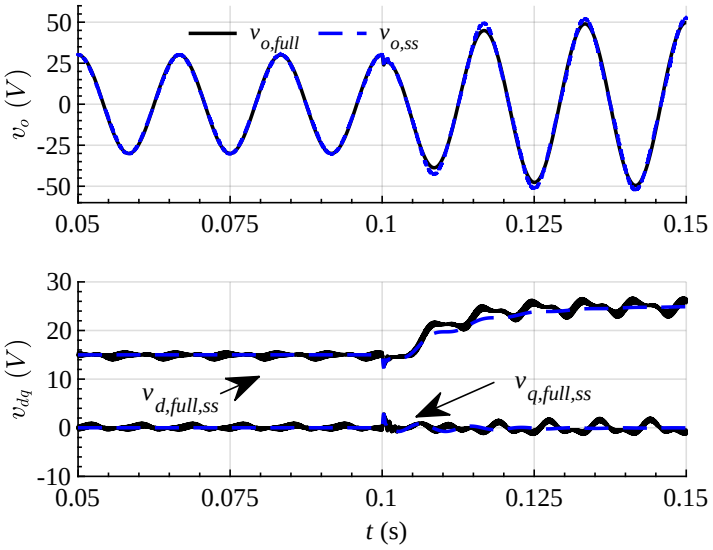

Figure 18. Comparison of the output voltages and the dq axis voltages from both the full order model and the small-signal model of the boost inverter. The d axis reference jumps from 15 V to 25 V and the q axis reference remains fixed at 0 V.

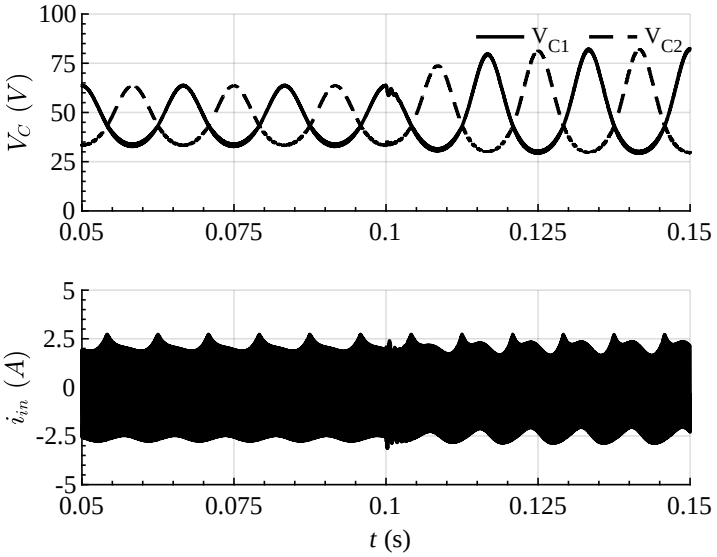

Figure 19. The output capacitor voltages and the supply current due to a step change in reference.

5.1.2. Change in Input

A step change in the input from 22 V to 18 V is made at $t = 0.2$ s. The individual capacitor voltages and the final output voltage are shown in Figure 20. An expected drop in the DC offset is observable due to the fixed part, D, in the duty cycle. The output voltage level recovers fast and shows minimal change during this event.

5.1.3. Change in Output Impedance

Initially, a 343 Ω resistance is used as the load. At $t = 0.3$ s, a second load consisting of 690 Ω is added in parallel to the original one to get an equivalent of 229 Ω load. The output voltage and output current values are recorded and presented in Figure 21. The current magnitude increases during the step change in load. The output voltage remains steady throughout the event.

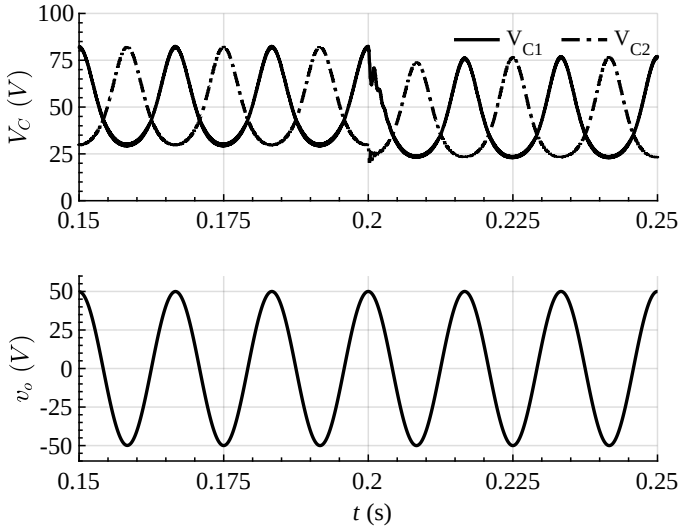

Figure 20. Voltages across the individual converters and the differential output due to a step change in the input supply. The input drops from 22 V to 18 V.

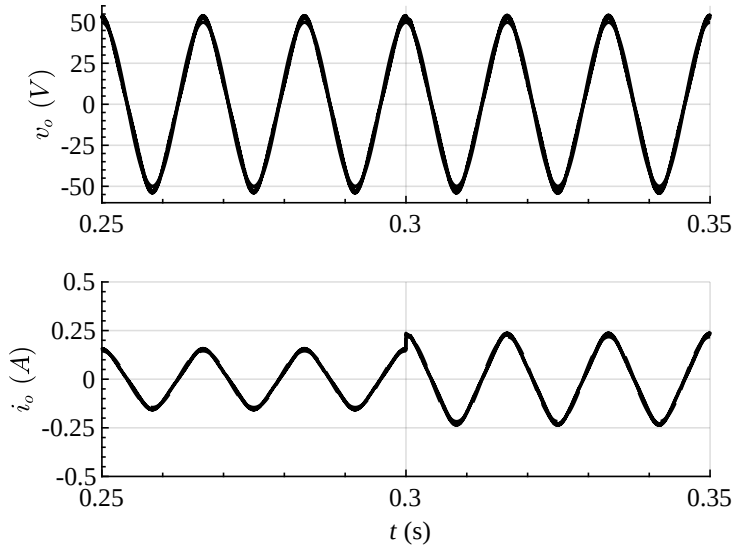

Figure 21. Output voltage and current due to an increase in the load.

5.2. Experimental Results

The mathematical model and the controller gains are verified using a hardware testbed. The single-phase single-stage boost inverter discussed here consists of two DC-DC boost converters. The converters are designed with identical inductor and capacitor values. The selection of inductors and capacitors is made following the formulas provided in [32]. The controller algorithm is implemented using a Texas Instrument's TMS320F28379D digital signal processor (DSP). The complete set up is depicted in Figure 22.

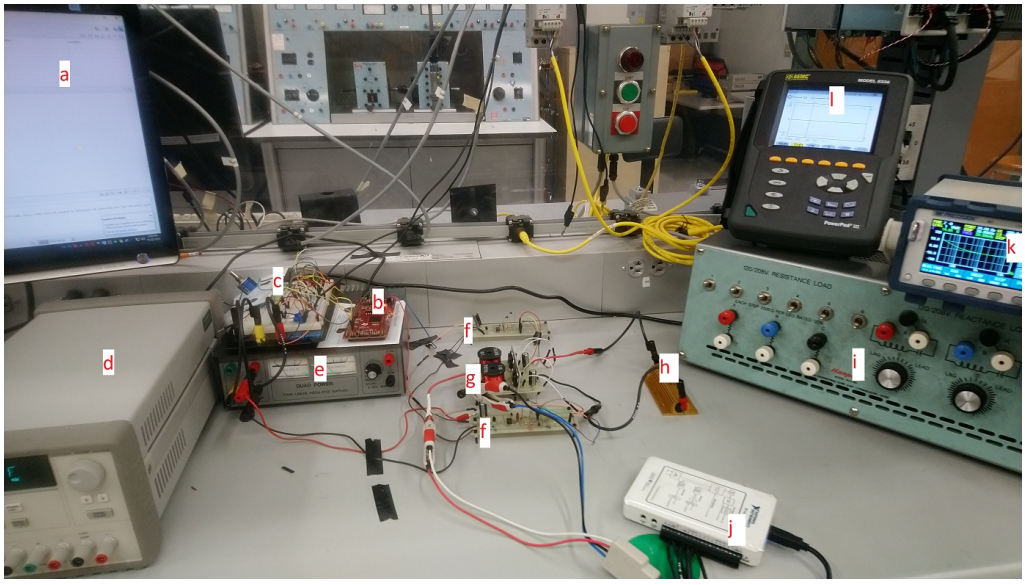

Figure 22. Experiment testbed. (**a**) Code composer studio, (**b**) TI DSP, (**c**) sensor board, (**d**) DC power supply for the inverter, (**e**) sensor board power supply, (**f**) gate driver boards, (**g**) inverter, (**h**) 50 Ω load, (**i**) RLC load, (**j**) NI myDAQ for verification of G_{vg} and G_{vd}, (**k**) BK precision LCR meter for impedance verification, and (**l**) AEMC power quality analyzer.

At first, the reference voltage, v_d, is changed from 15 V to 25 V. In Figure 23, the output voltage magnitude changes from 30 V to 50 V. The dq axis voltage calculations are internal to the DSP. As a result, their measurement required first passing the variables through two separate PWM channels and then measuring them across an active low-pass filter output. The cut-off frequency of the filter was selected high enough to preserve the dynamics of the signals. A volt on the oscilloscope display means an actual measurement of 10 V. The q-axis voltage swings between positive to negative values with an average of 0 V. The transient in the v_{dq} signal subsides within half-cycle. The dynamics match very closely with that of the ones presented in Figure 18.

Figure 23. Measurement of output voltage and dq axis voltages as the reference is changed.

In the second experiment, the DC input is reduced from 22 V to 18 V. This step change has a minimal effect on the output voltage as seen in Figure 24. The DC offsets in V_{C1} and V_{C2} drop as expected due to the fixed part in the duty cycle. The signal dynamics match very closely with that of the ones in Figure 20. The AC variations in the capacitor voltages are 180° out of phase.

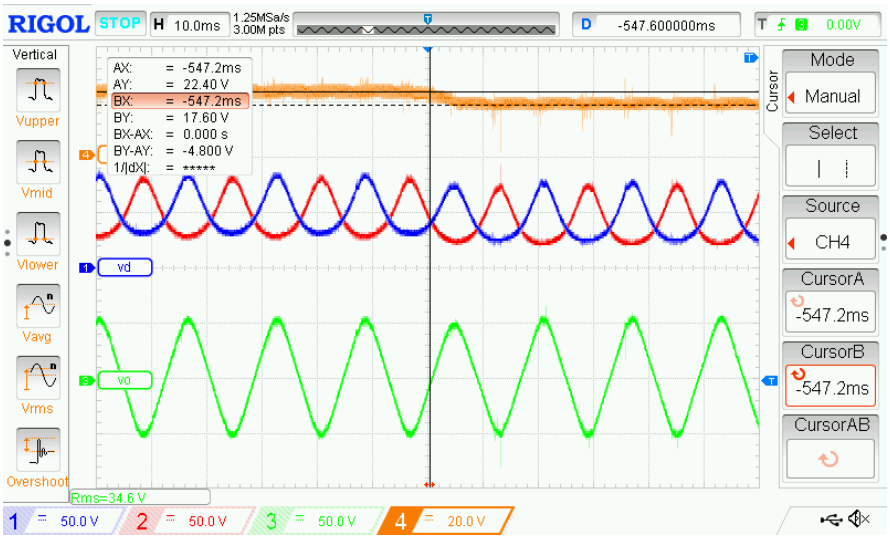

Figure 24. Measurement of capacitor voltages and voltage across the load when the supply is changed.

In the next experiment, a step-change in load is provided. The new load values were mentioned previously. The change in load has not resulted in any change in the magnitude or in the phase of the output voltage as seen in Figure 25. The load current has increased when the new load is added in parallel to the system. Due to the drops in the switches and in the connecting terminals, the current magnitude varies slightly when compared to that of the one in Figure 21. The transients in the experimental results are once again consistent with the simulation results.

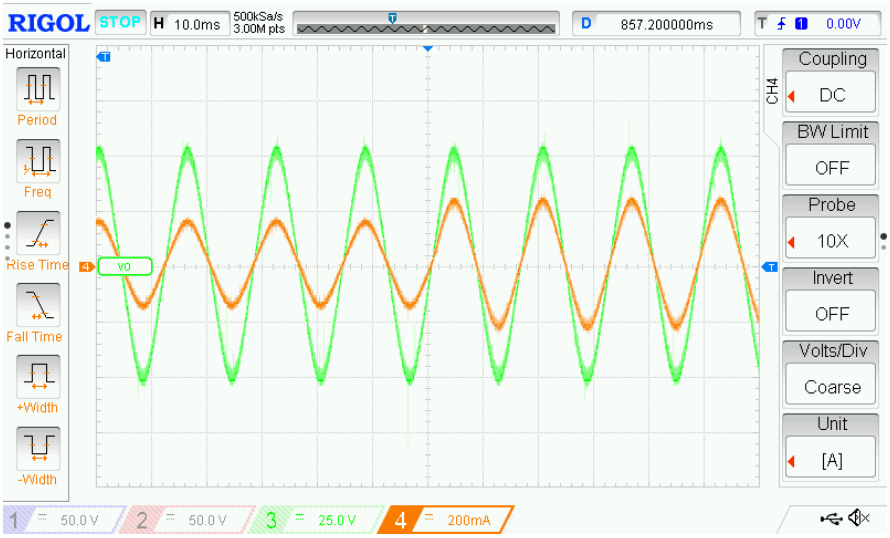

Figure 25. Measurement of load voltage and load current due to a step change in resistive load.

The inverter system is then tested using an RC load with the resistor and the capacitor values of 243 Ω and 15.4 µf respectively. The measurement of output voltage and current is presented in Figure 26. The current waveform leads the voltage waveform in this case.

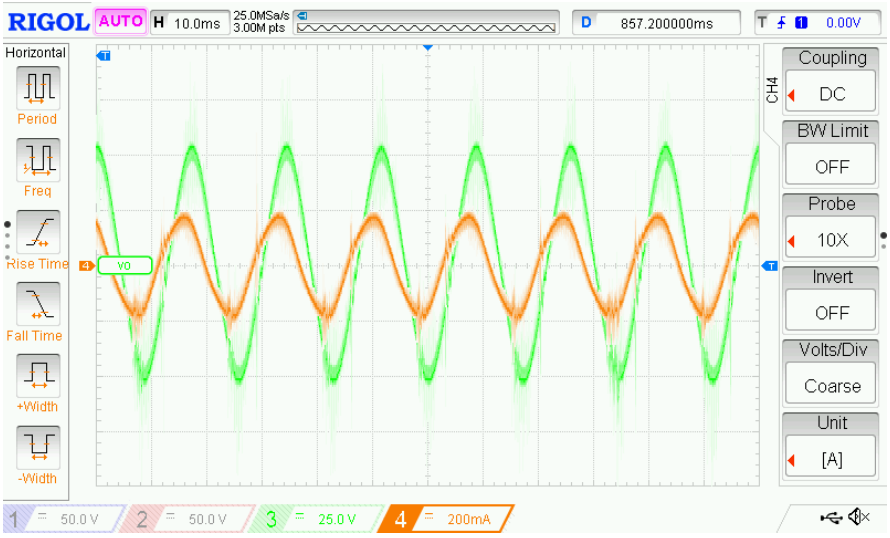

Figure 26. Measurement of output voltage and output current with an RC load.

The testbed is then subjected to an RLC load with the same resistor and capacitor values as mentioned previously. This time an inductor of 0.8 H is added to the system. The current in Figure 27 is lagging the voltage waveform, indicating that the load is more inductive. A step change in load is applied, which is noted by an increase in current magnitude.

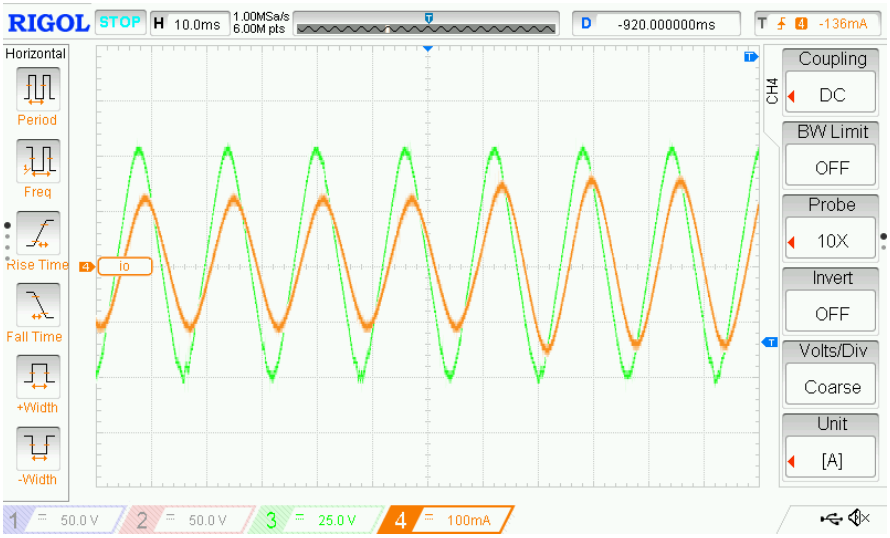

Figure 27. Measurement of output voltage and output current with an RLC load.

A system is tested using a non-linear load. A full bridge rectifier is used to test the system. The waveforms in Figure 28 represent the inverter output voltage and output current along with the voltage measured across the diode bridge combination.

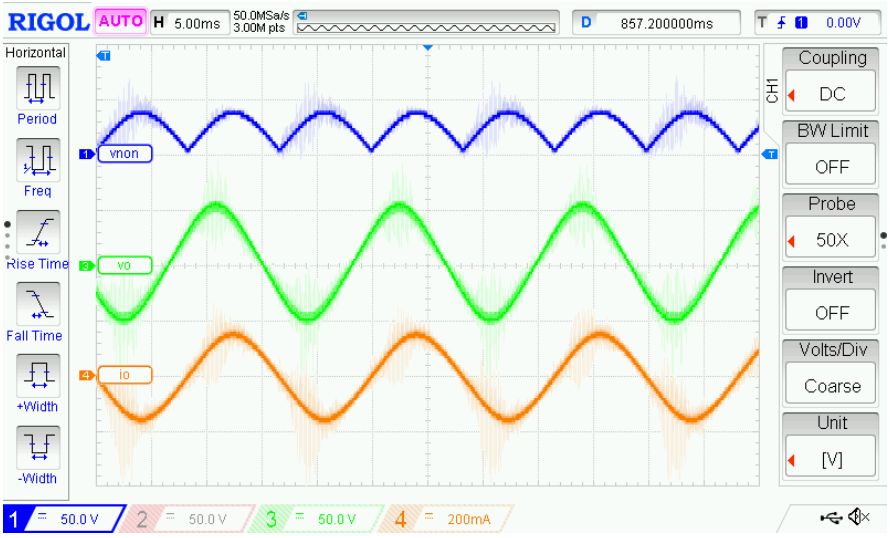

Figure 28. Measurement of output voltage, output current, and the voltage across the full wave rectifier diode bridge circuit.

To demonstrate the switching ripple in the input current waveform, the measured input current in Figure 29 is zoomed at 50 us/div. The inset cursor measurement shows a 15 kHz ripple in the current output.

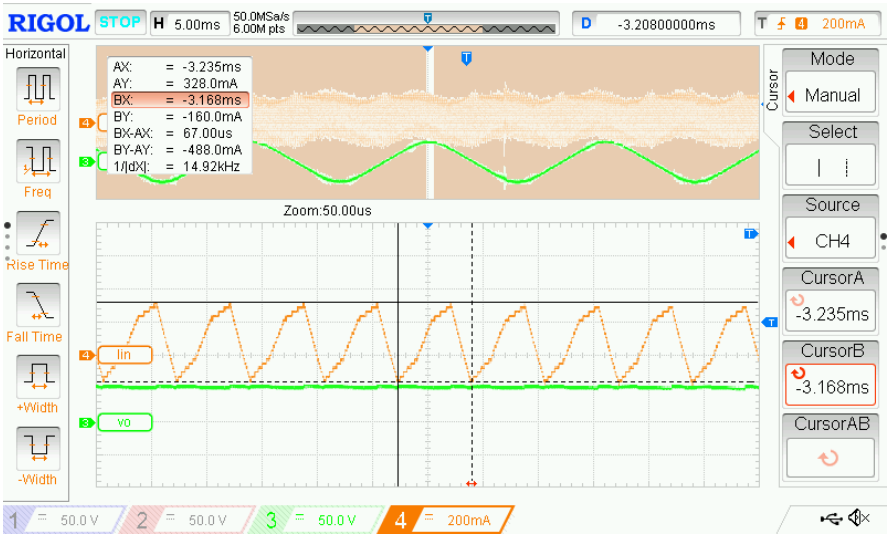

Figure 29. Measurement of output voltage and input current. The ripple in the current waveform demonstrates the 15 kHz switching frequency.

The total harmonic distortion (THD) of the output voltage is measured using an AEMC 8336 PowerPad III Power Quality Analyzer. The THD measurement is depicted in Figure 30. The measurement gives a THD value of 3.88% which is comparable to the values presented in [8,27,33]. When compared with the THD values reported in [8], the inverter discussed here has less THD level compared to the 2L-PWM and the 3L-PWM modulation techniques. However, in the same article, the L3L modulation technique shows better performance in terms of harmonics mitigation. The proportional resonant converter used to control the single-phase inverter in [33] provides a much higher THD level (11.8 %) when compared to that of the one from the proposed controller. The THD values reported in [27] are slightly lower compared to the values measured in Figure 30 and below the limit mentioned in IEEE Std. 519-1992 [34]. However, the voltage control algorithm presented in this work shows a better performance in terms of tight regulation of output voltage magnitude. The peak-to-peak magnitude is maintained exactly at 100 V in this work compared to the one

presented by Jha et al. which is 96 V. This is because there is a 300 dB gain at the operating frequency as shown in Figure 17. This high gain at the operating frequency is absent as shown in Figure 6 in [27] which results in a decreased magnitude at the operating frequency. Among the three voltage-mode controllers presented in their work, only two uses a negative feedback loop. In contrast to the method presented in this work (Figure 14), two different control loops are present and two different voltage references are required. The proposed method in this work needs only one set of references, v^*_{dq}, and compares the DC signals to generate errors that are passed through the PI controllers to produce the desired PWM signals. Whereas the control loop structure by Jha et al. uses a sinusoidal reference tracking mechanism. Using this scheme introduces steady-state amplitude and phase errors whenever a PI controller is used for tracking a sinusoidal reference signal. It is possible to reduce the error by increasing the controller gain. However, it compromises the system stability due to noise amplification.

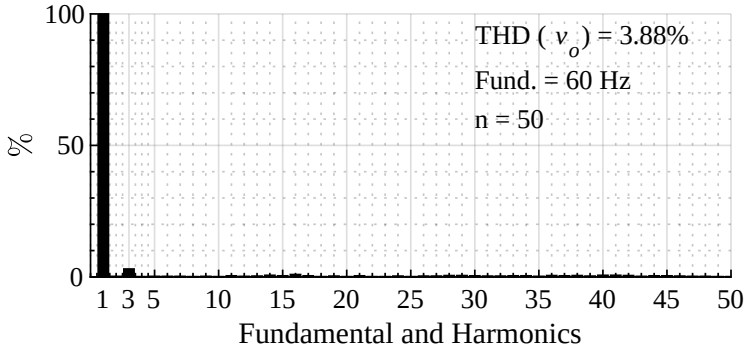

Figure 30. Measurement of harmonics and THD.

5.3. Stability Margins and Sensitivity

The minimum load impedance required for the system to remain stable at all frequencies can be obtained by applying the Middlebrook's stability criterion. For that, the Thévenin equivalent output impedance of the inverter, $Z_{o,th}$, is determined from (59) by setting $R = \infty$. The peak value of the output impedance magnitude under this condition is 43.2 dB. Thus, the system is locally stable if the magnitude of the load impedance, Z_{load}, is greater than 145 Ω. If impedance magnitudes are lower, then the system will still be stable provided that the impedance ratio of the transfer function, $\frac{Z_{o,th}}{Z_{load}}$, satisfies the Nyquist stability test. The system stability margins for the closed-loop system in Section 4 are determined from the loop-gain Bode plot. The gain margin of the system is found to be approximately 8.43 dB at 1.62 kHz and the phase margin is found as 45° at 1.97 kHz.

To perform a sensitivity analysis, the closed-loop transfer function, G_{cl}, is determined from (66). The sensitivity of G_{cl} with respect to parasitic components, r_L, r_C, and r_{DS} are determined as S_{r_L}, S_{r_C}, and $S_{r_{DS}}$ respectively. The Bode plots respresenting the magnitude of these functions are given in Figure 31. It is observed that the system is less sensitive to changes in both r_L and r_{DS} at various frequencies. The sensitivity in both the cases becomes maximum at the resonant frequency which is expected. However, the magnitude of the sensitivity due to the different values of these two parasitic are tightly bounded in that region. The sensitivity due to the capacitor ESR, however, starts to increase as the frequency progresses. This indicates that several parallel capacitors are needed to be placed at the output side to reduce the overall r_C.

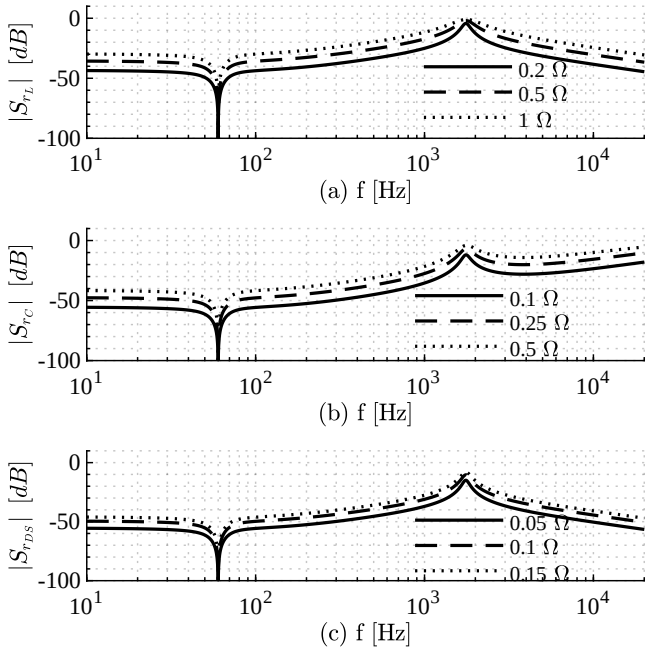

Figure 31. Sensitivity due to: (**a**) r_L, (**b**) r_C, and (**c**) r_{DS}.

The sensitivity analysis is then carried considering variations in L, C, and load resistor, R. The Bode plots corresponding to the sensitivity functions, S_L, S_C, and S_R are shown in Figure 32. It can be noted that the closed-loop transfer function's sensitivity is highly influenced by both the inductors and capacitors as the frequency approaches the resonant frequency and above. The sensitivity due to the load remains low at all frequencies other than the resonant peak as expected. The sensitivity in this case lowers as the load value is increased.

In all three cases, the sensitivity is lowest at 60 Hz.

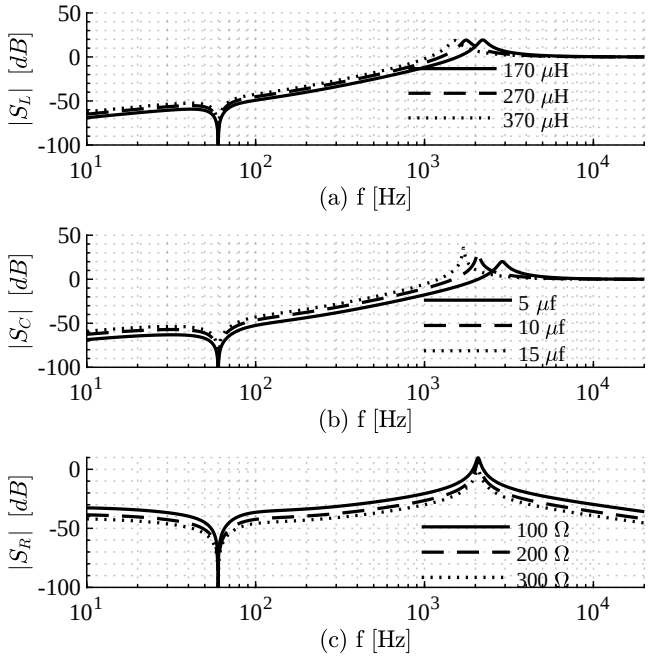

Figure 32. Sensitivity due to: (**a**) L, (**b**) C, and (**c**) R.

5.4. Loss Estimation and Efficiency

The two main sources of losses in this system are the semiconductor device losses and the inductor I^2R losses. The low power inverter prototype in this work is constructed to verify the small-signal models and the controller algorithm. At this power level, the losses tend to dominate, resulting in poor system efficiency. To represent a practical system, the output voltage level is raised to 110 V_{rms} in the PLECS simulation platform. The system losses are then estimated using a high power MOSFET switch (C2M0025120D) for which a detailed thermal model suitable for PLECS simulation is readily available. The efficiency curve at different power levels in Figure 33 shows that the maximum efficiency occurs around 240 W. The loss breakdown for the inverter system is listed in Table 3.

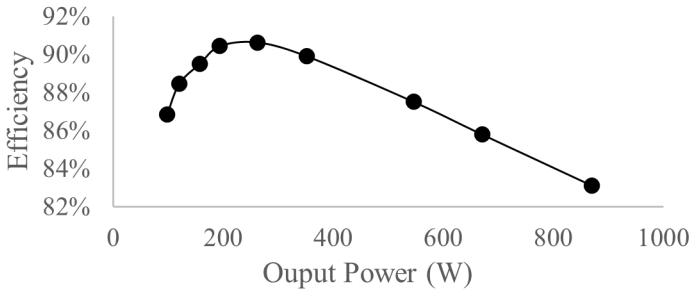

Figure 33. Efficiency at different power levels.

Table 3. Power loss distribution at the maximum output power.

Loss Type	Component	Value	%
Conduction	Switch S_1	0.91 W	3.64 %
Switching	Switch S_1	0.01 W	0.06 %
Conduction	Switch S_2	0.55 W	2.18 %
Switching	Switch S_2	0.02 W	0.04 %
Copper loss	r_L	9.60 W	38 %
ESR loss	r_C	1.53 W	6.06 %
	Per converter	12.63 W	50 %
	Total	25.26 W	100 %

It is important to notice that a significant amount of loss is incurred due to the inductor parasitic. This loss can be reduced by an inductor with a lower ESR. When compared to the most recent single-phase boost inverter topologies researched in [35–37] the discussed inverter appears to be less efficient. This is mainly due to the fact that the latter topologies are inductor-less. However, the discussed topology has a much lower THD which makes it suitable for grid integration.

6. Conclusions

A single-phase single-stage boost inverter is analyzed. Both steady-state equivalent and AC small-signal mathematical models are derived that include component parasitic. The proposed models are not only accurate but also simpler compared to the existing models found in the literature review. The boost inverter open-loop input impedance and output impedance are expressed mathematically for the first time. The control-to-output transfer function including the loss terms helps to determine the appropriate controller gains in a practical inverter system. To improve the converter performance, the transfer functions for the input impedance and output impedance can be used to determine the input filter size and to calculate the load impedance for stable operation using the Middlebrook's stability criteria.

For accuracy verification purposes, the Bode plots obtained from the proposed transfer functions are compared with that of the ones found using the experimental results.

A simple voltage mode controller developed in the synchronous reference frame is proposed for the first time to control the inverter operation. The controller gains are designed following the steps found in the classical control theory. The newly designed regulator gains are used in the full-order model as well as in the small-signal model. Finally, the control algorithm is implemented in a hardware setup. The experimental results match closely with that of the ones obtained from the simulation results. The advantages of using such inverter lies in its simple design, single-stage operation, and smaller footprint when compared to a double stage buck type inverter. Having said that, the inverter requires the use of two inductors and suffers from low device utilization as found in both the quasi-steady-state equivalent circuit model and efficiency estimation. The suggested future work for this system would be the determination of the lifetime of the capacitors that will include the measurement of fundamental and the harmonics of the voltage waveform and a detailed thermal model of the components. Additionally, the proposed models can be used to determine losses in the system more accurately.

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