# Development of an Alternative Droop Strategy for Controlling Parallel Converters in Standalone DC Microgrid

By

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# Abstract

Most of parallel-connected DC-DC converters schemes are based on a high-bandwidth communication network to achieve minimum circulating current, proper load current sharing, and acceptable voltage regulation. However, in DC microgrids, the use of communication network can be costly and unsuitable considering the data reliability and cost investment because the load and renewable energy sources are connected to the point of common coupling. Therefore, the droop control as a decentralized method has gained more attention. However, the challenge for the conventional droop method is to overcome the issue of circulating current, poor load current sharing, and the drop in DC grid voltage due to the droop action. This thesis develops and tests an approach for minimizing the circulating current, as well as improving the voltage regulation and the load current sharing for the droop method. The developed approach is based on the concept of synchronized switching, which is implemented using an alternative droop strategy for controlling different sizes of parallel-connected DC-DC boost converters.

In this thesis, synchronous switching, based on an optimized controller, is presented to eliminate the initiation of circulating current and minimize the ripple in the output current for parallel-connected boost converters. Furthermore, a modified droop method, including the cable resistance, is introduced. The modified droop method uses the measurements of the voltage and current at the point of common coupling to estimate the voltage set point for each converter locally. The communication network is eliminated by utilizing the modified droop method because, in the proposed method, there is no current and voltage measurement data transmitted from one converter to the other converter. Additional loop control is also applied for equal current sharing between parallel converters to overcome the issue of mismatch in parameters of the parallel converters. The additional loop control is added to improve the load current sharing in the modified droop control.

The modified droop control method with additional loop control is verified using MATLAB/SIMULINK and validated with experimental results.

However, the droop action of the modified droop and different cable resistances degrades the voltage regulation and load current sharing. Therefore, an improved droop method, which utilizes the virtual droop gain and voltage droop control gain, is proposed to overcome the problem of load current sharing and voltage regulation. The virtual droop gain compensates the differences in the cable resistances, and the voltage droop control gain regulates the voltage at the point of common coupling. This maintains the common DC bus at its rated value. The effectiveness of the improved droop method is demonstrated by MATLAB/Simulink and Laboratory prototype results. Finally, the proposed method is utilized in a standalone DC microgrid. An example of a DC microgrid of a residential building powered by a PV solar system illustrates the feasibility and the effectiveness of the proposed methods.

# Acknowledgment

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# List of Abbreviation and key terms

| | |
|---|---|
| DC | Direct Current |
| AC | Alternative Current |
| RESs | Renewable Energy Sources |
| DERs | Distributed Energy Resources |
| VDG | Virtual Droop Gain |
| AVCG | Adaptive Voltage Control Gain |
| VR | Virtual Resistance |
| PWM | Pulse Width Modulation |
| CCM | Continuous Conduction Mode |
| DCM | Discontinuous Conduction Mode |
| PCS | Percentage of Current Sharing |
| ADCs | Analog-Digital Converters |
| PCC | Point of Common Coupling |
| PSO | Particle Swarm Optimization |
| PV | Photovoltaic |
| BNA | Bisection Numerical Algorithm |
| FOCV | Fractional Open Circuit Voltage |
| FSCC | Fractional Short Circuit Current |
| BESS | Battery Energy Storage System |
| MPPT | Maximum Power Point Tracking |

| | |
|---|---|
| Circulating current | In case of parallel-connected converters, the differences in the out voltages of the converters cause circulating currents to flow |
| Current sharing | The technique of current sharing for converters that are connected in parallel to provide more load current or redundant power to a load. This technique increases the amount of current available for the load at the same level of contribution. |
| Voltage regulation | The measure of how well a power converter can maintain constant voltage at the point of common coupling. The converter is given a constant input voltage and wide variance in load current |

# Chapter 1

# Introduction

## 1.1 Background

Most of today's residential users and office loads are based on electronic DC loads such as televisions, computers, printers, laptops, phones, tablets, and LED lighting. In some industrial applications, such as DC electric arc furnaces used in the steel industry, the consumed energy is less compared to the consumption energy of AC electric arc furnaces. Thus, considering an increasing ratio of residential DC end-user loads and efficiency of converters, DC microgrids are more beneficial than AC microgrids [1,2]. Moreover, renewable energy sources (RESs) are a global trend toward friendly environmental energy sources. Some of the RESs are basically DC sources such as photovoltaic PV. Others, such as offshore wind turbines, are integrated to an AC grid through a DC link [3,4]. One stage of conversion can be eliminated when the distribution system is converted to DC, which consequently improves the overall efficiency of the system [5-7]. Furthermore, one of the advantages of DC microgrids is their capabilities of utilizing the static storage. Most of the storage systems, such as batteries and ultra-capacitor, are purely DC. Also, the integration of mechanical storage systems such as flywheels, which use a permeant magnetic synchronous machine, is mostly through a DC link [8,9].

In recent years, with the goals of more efficient integration of distributed renewable energy and storage systems, the DC microgrid has gained more attention due to the elimination of the rectification and inversion stages [10]. For distributed energy resources (DERs), parallel-

connected converters can be employed, as shown in Fig. 1. The schematic diagram of parallel-connected converters is required because this type of configurations offers serval advantages compared to a single unit structure.

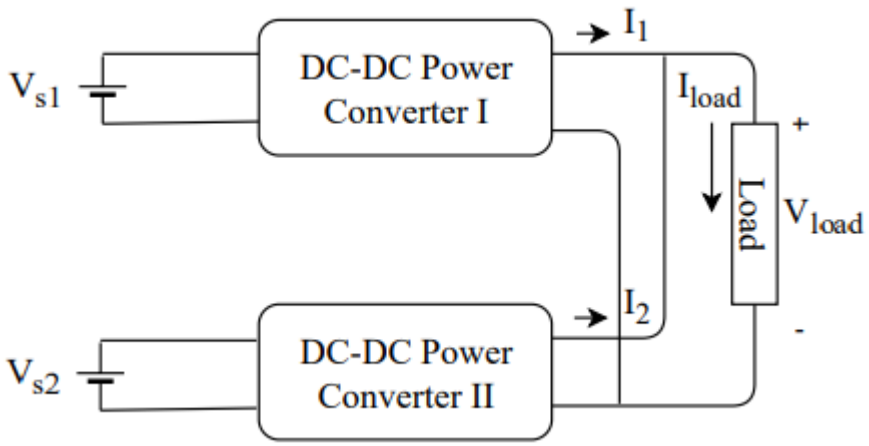



Figure 1. 1 Schematic diagram of two parallel-connected converters supplied from different DC sources

In general, The main purpose of using parallel-connected converters is to achieve the following features [11-14]:

- Thermal management: In the parallel configuration, each converter handles a part of the total load power, which leads to less power dissipated in each module. Thus, the thermal design for the paralleling configuration is simplified.
- Reliability: In parallel configuration, electrical and thermal stress on the semiconductor devices is reduced. Although the number of power electronic devices is increased due to the paralleling configuration, the reliability of such a configuration is increased.

- Redundancy: Using more converters in parallel configuration than the minimum requirements of the load makes a redundant system. The redundancy is necessary for high-reliability systems such as mainframe computer, space, and military applications.
- Modularity: The parallel configuration is appropriate for designing a modular system. The advantages of modular design include expandability and flexibility. When the power demand grows, additional converters in parallel configuration can be added to meet the required power. This allows the expansion of the system at a lower cost.
- Maintainability: The suitable design of paralleling configuration provides flexibility for the online replacement of the defective converters. Hence, the paralleling configuration provides a non-interrupting power supply during the maintenance and repairs, which are very desirable characteristics in the power system.
- Size reduction: lowering the power rating of the converters in a parallel configuration, which can operate at a higher frequency, reduces the size of filter components. The interleaving mode of operation of parallel converters also leads to the reduction of the overall filter size.

However, employing parallel operation of DC-DC converters is associated with major challenges such as circulation current between converters, unequal load current sharing, and deterioration of load voltage regulation [15]. Any mismatch of the output voltages for the parallel-connected converters causes the initiation of circulating currents, which results in higher current through the power electronic switches and different load current sharing between the converters. The current imbalance will result in excessive thermal and switch stress on specific units and reduce the reliability of the system. Thus, increasing the rating of the switches is required with costly effects.

Considerable efforts have been made to mitigate and overcome the operational challenges of parallel converters in DC microgrid. Therefore, several schemes for controlling parallel-connected DC-DC converters have been proposed, developed, and analyzed in the past [16-20]. In general, parallel controlling methods are classified into two categories, which are basically identified based on operating mechanisms to current sharing, i.e., droop methods and active current sharing methods [16]. Fig. 1.2 shows the two categories of parallel-controlling methods, which are the droop method and the active current sharing method.

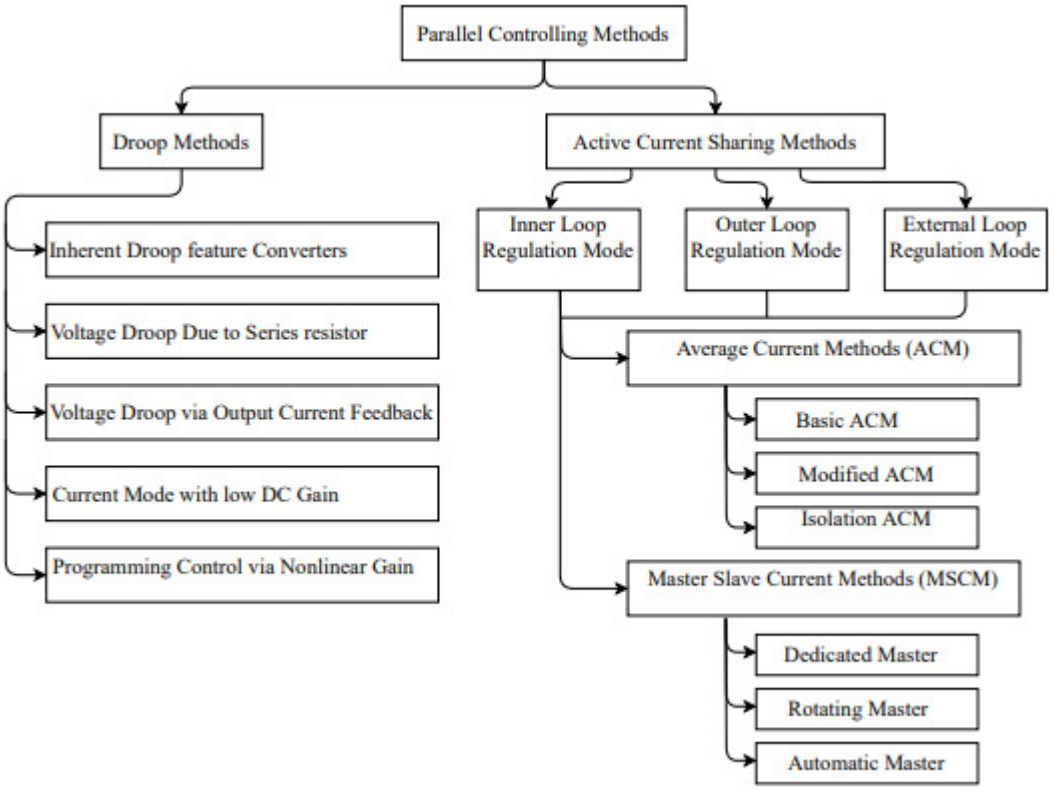



Figure 1. 2 Classification diagram for parallel controlling methods

The active current sharing can be classified into two types of control methods, which are the averaged current methods and master-slave current methods. The active current sharing methods

provide better accuracy in terms of current sharing and voltage regulation, but it requires error signal processing of the current sharing. The active current sharing methods mainly consist of a specific control mode of operation, which can be inner, outer, or external loop mode. The three control modes are categorized from the viewpoint of current sharing error signals, which vary from the basic mode regulation to the developed mode regulation. The inner loop mode regulation is associated with the use of common error signal, which is the use of the voltage measurements at the common DC bus as feedback signal. The outer loop regulation uses the current error signal to modify the references voltage for the achieving equal current sharing. The external loop mode uses and compares all load sharing signals from the individual power converters and adjusting the corresponding feedback control signal to balance the load currents. In general, current sharing error signals are required to achieve better sharing between parallel converters. Thus, most of the active current sharing methods are based on a high-bandwidth communication network, which is a costly and unsuitable choice for a DC microgrid due to the connection of the load and distribution energy resources to the point of common coupling [17]. In terms of reliability, the droop methods are more reliable because they do not use a communication scheme. On the other hand, the accuracy of current sharing and voltage regulation for the droop methods are lower.

As shown in Fig. 1.2, the droop methods can be further categorized into five controlling types, which are based on how to get the droop characteristics for the parallel-connected converters. Although the processing signal between parallel converters is not required, the accuracy of current sharing and the voltage regulation is the main drawback of conventional droop methods. The method of conventional droop also has poor voltage regulation and load sharing current due to the droop action. Therefore, low bandwidth communication is used to improve load sharing and voltage regulation [18]. The proper load current sharing and voltage regulation are limited by the

use of a communication network between converters, which is a factor of cost and reliability of DC microgrid. Each strategy of the proposed method for controlling parallel-connected converters has its limitation in terms of its application or implementation. However, the superior advantages of these methods are to achieve a precise load current sharing and better voltage regulation. At the same time, factors such as complexity, cost, modularity, and reliability are improved. A successful selection of the paralleling control scheme depends on the advantages and limitations of different methods. Although the benefits of parallel-connected converters are well known and understood, choosing one of the parallel controlling methods must consider some of the factors such as complexity, cost, modularity, and the reliability for a certain application. The thesis focuses on the droop method.

## 1.2 Motivation

Numerous approaches for controlling parallel-connected converters have been presented in the literature [19-41]. The cost, accuracy, complexity, and reliability of these approaches are the essential factors in the evaluation of their performance. In DC microgrid, the point of common coupling makes some of the methods more attractive. These methods are called passive droop methods. Extensive research contributions have attempted to improve one or more factors to enhance the performance of the droop methods. Although the accuracy of the modified droop methods is achieved, the accuracy improvement of the droop methods is based on a communication network to transmit the current and voltage data from one converter to the other.

The goal of this research is to develop an improved droop method that meets the requirements of paralleling operation of DC-DC converters, such as elimination of circulation current, precise current sharing, and voltage regulation. The desired operation is achieved by eliminating the data transfer between parallel converters, which leads to a reduction in the total cost and complexity

while simplifying the control scheme. The goals will be achieved through the following objectives:

1. Ensure synchronous switching for different sizes of parallel-connected boost converters during various conditions such as a change in load to eliminate the initiation of circulating current.
2. Use measurements at the point of common coupling to eliminate the need to transfer the voltage and current data between parallel converters. This is achieved by proposing a modified droop method with cable resistance implementation for different sizes of parallel-connected boost converters. The analytical load regulation characteristic of the droop method is developed and modified by treating the cable resistance as part of the load regulation characteristic for each converter.
3. Improve load sharing between parallel converters with mismatches in their parameters by adding a control loop to regulate the output voltages of parallel converters for a precise current sharing.
4. Introduce a virtual droop gain based on differences in cable resistance to compensate for the mismatches in current sharing for parallel-connected boost converters to achieve proper load current sharing.
5. Regulate the voltage at the point of common coupling by implementing adaptive voltage control gain to ensure a constant voltage at the common DC bus.

## 1.3 Outline of the Thesis

The contents of this thesis are divided into seven chapters and organized in a way to show the steps of developing the proposed method

Chapter 1

This Chapter is the introduction of the thesis. It gives a brief classification of controlling methods for parallel-connected converters. It highlights the benefits of using parallel configuration instead of using a single power unit. The motivation of the developed work in this thesis is illustrated to shows the value of this research. Finally, the research objectives and outline of the thesis are provided.

Chapter 2

A survey of the literature on controlling methods for parallel-connected DC-DC converters is given in Chapter 2. Controlling methods are classified into two categories, passive droop methods and active current sharing methods. The chapter shows the rationality of using the passive methods in controlling parallel-connected DC-DC converters and highlights the limitation of the conventional and improved droop methods, which are presented in the literature.

Chapter 3

The elimination of circulating current between different sizes of parallel converters are investigated in Chapter 3. In this chapter, the relationship between synchronous switching and the initiation of circulating current is developed and tested. Furthermore, a modified droop method based on master current control is proposed. The technique considers an optimized controller, which guarantees synchronous switching during various operating conditions of loading.

Chapter 4

Cable resistance implementation in the droop methods is discussed in Chapter 4. Including the cable resistance in the modified droop method eliminates the need for transferring the current and

voltage measurements between the parallel-connected DC-DC converters. In the proposed scheme, the voltage and current at the point of common coupling are used to estimate the voltage set point for each converter. The estimated voltage reference is fed locally to the outer voltage loop of each converter. This ensures that the load current is shared based on the load regulation characteristics for each converter. Furthermore, a control algorithm is presented to overcome the mismatches in the parameters of the parallel converters. The proposed algorithm utilizes the modified droop method with cable resistance implementation and guarantees load current sharing equally while there is a mismatch in the parameters of the parallel-connected converters. Experimental results of 6-12 V parallel-connected DC-DC converters are also presented to validate the proposed control algorithm with the modified droop method.

Chapter 5

In Chapter 5, different cable resistances and voltage regulation issues are presented and improved based on an alternative droop control method. The proposed method overcomes the differences in cable resistance by implementing a virtual droop gain (VDG). The virtual droop gain compensates for the differences in cable resistances to ensure equal load current sharing between parallel converters. For the voltage restoration, an adaptive voltage control gain (AVCG) is implemented to maintain the voltage at the point of common coupling to its rated voltage. The procedure of VDG and AVCG is the main structure of the improved droop method to eliminate the use of a communication network. Experimental validation of the improved droop method is presented as well.

Chapter 6

A standalone DC microgrid powered by a PV system is presented in Chapter 6. The illustrative model consists of parallel tracks, each track consisting of two types of DC converters: (i) DC-DC renewable side buck converter and (ii) the DC-DC load side boost converter. The DC-DC renewable side converter, which is responsible for extracting the highest power, is implemented based on the Bisection numerical algorithm. The DC-DC renewable side converter extracts maximum power from the PV unit to charge a battery storage system. The DC-DC load side converter connects to the load through a cable resistance. In the DC-DC load side converters, the improved droop method is simulated using MATLAB. This allows the same size of storage system to share the load equally and regulate the DC bus at its rated voltage.

Chapter 7

In Chapter 7, the primary outcomes and major contributions of the investigation are summarized. Suggestions for further extension of the research are also discussed in the Chapter.

# Chapter 2

# Literature Review

## 2.1 General

Several advantages in a DC power system can be achieved by employing parallel operation of DC-DC converters. These advantages are associated with improving the reliability of the system, increasing in the maximum output power, lowering stress on the power electronic components, enhancing the heat management, and reducing the required maintenance and repair. However, the main challenges of parallel operation are associated with the circulating current, current sharing, and voltage regulations. Due to these challenges, several methods have been presented in the literature. These methods mitigate and overcome the operating difficulties of parallel-connected DC-DC converters. They have been introduced and implemented to improve the load current sharing and voltage regulation, along with the elimination of circulating current between parallel converters. These methods vary in their complexity, cost, reliability, and applicability for DC microgrid. The main objective of this chapter is to review these methods briefly and discuss the relevant research contributions of paralleling control methods. This chapter highlights the advantages, disadvantages, and the limitation of each method in order to establish the main context and demonstrate the rationality of the proposed research work.

## 2.2 Passive Droop Current Sharing Methods

The passive droop method can be modeled using circuit elements as a voltage source in series with an impedance to create a Thevenin equivalent circuit [19,20]. The schematic diagram of the passive droop method is shown in Figure 2.1.

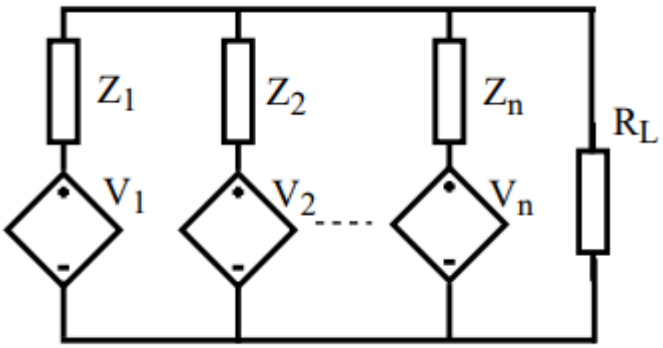


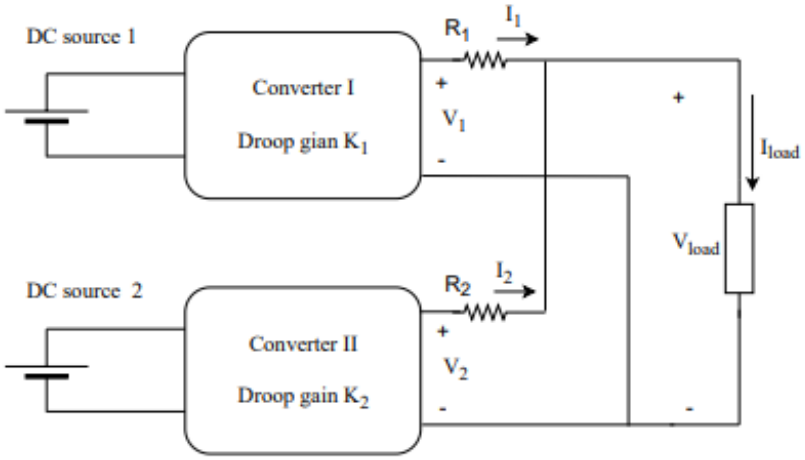

Figure 2. 1 Thevenin equivalent circuit for parallel-connected DC-DC converters

In this method, parallel-connected DC-DC converters are represented by dependent voltages, each of which is in series with an impedance (see Figure 2.1). Dependent voltage sources are used to model the operation of parallel DC-DC converters to regulate the output voltage and specify the current sharing between parallel converters.

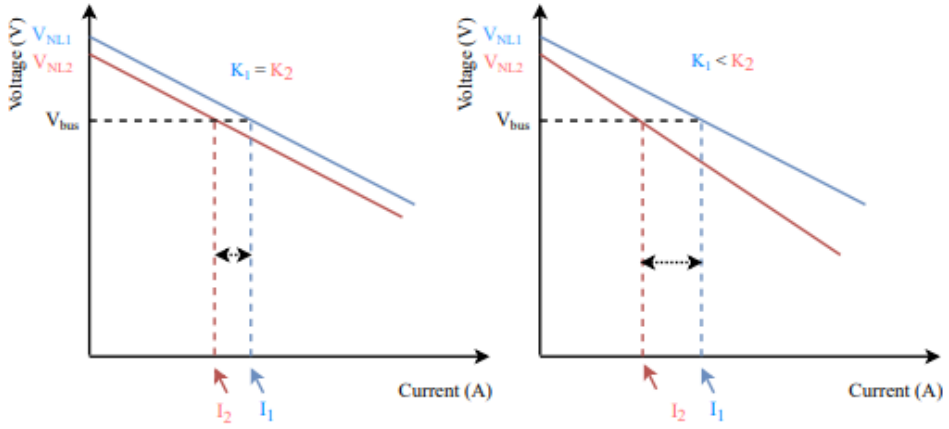
### 2.2.1 Conventional Droop Method

Different schemes of the conventional droop methods are presented in the literature for controlling parallel-connected DC-DC converters. These techniques have been implemented and practiced by industry. Among them, the simplest scheme for the droop method implementation is using converters with inherent droop features. The scheme is valid for controlling parallel-connected converters, which are properly chosen with a droop feature. The converters in the droop method are represented by a voltage source with series resistance. The series resistance is the virtual gain

of the droop characteristics $K_1$ and $K_2$ for converter I and II, respectively, as shown in Figure 2.2. Therefore, the converters with small droop gains would have a large current imbalance compared to converters with high droop gains, as shown in Figure 2.2 (b) and (c).




(a)




(b) (c)

Figure 2. 2 Parallel-connected converters and output characteristics with $R_1 = R_2$, (a) two converters with droop characteristics $K_1$ and $K_2$ connected in parallel, (b) output characteristics with equal droop gains ($K_1 = K_2$) (c) Output characteristics with unequal droop gains ($K_1 < K_2$)

The DC source 1 and DC source 2 in Figure 2.2 (a) have the same voltage level and the cable resistances $R_1$and $R_2$are equal. However, Figure 2.2 shows the problem of load current sharing, which is associated with different droop gains. Figure 2.2 (b) has a lower mismatch in load current sharing compared to Figure 2.2 (c) because the droop gains are different in Figure 2.2 (c). In general, converters, such as the boost, the buck operating in discontinuous conduction mode, and the series resonant converters, which have inherent load sharing ability, can be used in parallel operation [21].

Another droop scheme for parallel-connected converters, which uses a series resistor, is presented in [22]. The initial setting of the droop gains for the series resistor scheme is made identical via potentiometer, as shown in Figure 2.3.

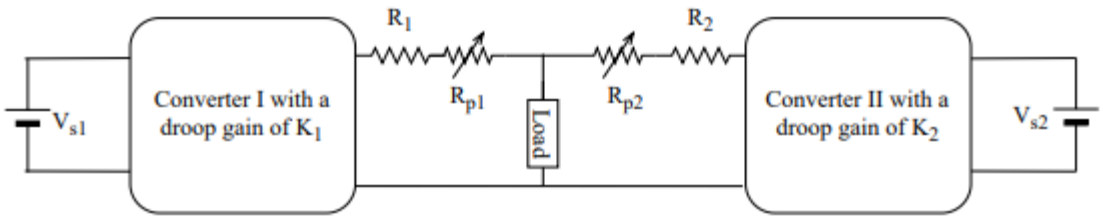
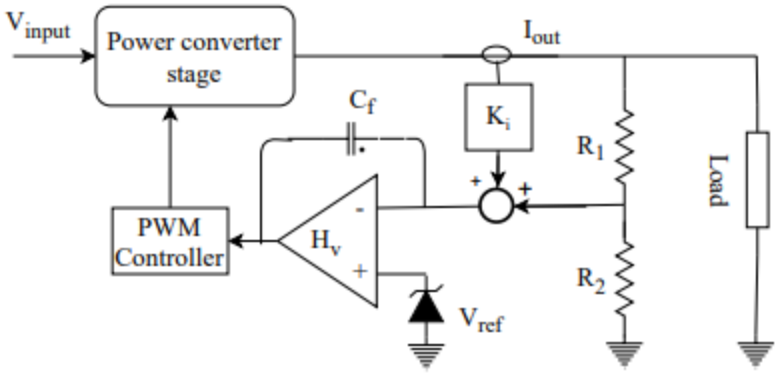


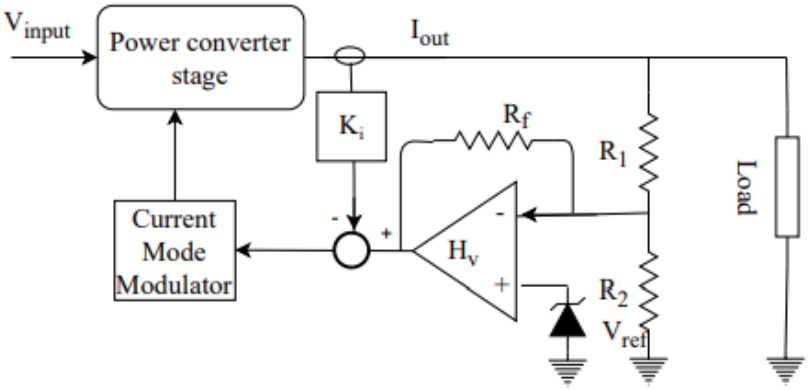

Figure 2. 3 Series resistor scheme for improving the load current sharing

The output of each converter is connected in series with the adjusted potentiometer ($R_{p1}$ or $R_{p2}$). The changes in $R_{p1}$ and $R_{p2}$ can match the voltage drop for both converters. However, the main disadvantage of the series resistor scheme is the high-power losses in $R_{p1}$ and $R_{p2}$, especially if the drop in output voltage is large. Thus, it is applicable for low power linear regulators.

A voltage droop scheme, which uses output current feedback to regulate the output voltage, is presented in [23]. The output voltage across a series resistor is measured and amplified to produce a droop in the output voltage that is proportional to the output current of the source, as shown in Figure 2.4 (a). An alternative implementation of the current-mode control uses a low voltage compensator DC gain, which provides an improved load current sharing and better transient response. This scheme is implemented by eliminating the series capacitance in the feedback path of the error amplifier, which provides a low droop gain, as shown in Figure 2.4 (b). However, due to the nonlinearity associated with the DC-DC converters, a droop scheme is implemented based on a nonlinear gain programming, as shown in Figure 2.4 (c). Since high droop gain causes a degradation in the load current sharing, the operating range for achieving good load current sharing can be programmed with different values of the droop gain to ensure better sharing between parallel converters [22].




(a)

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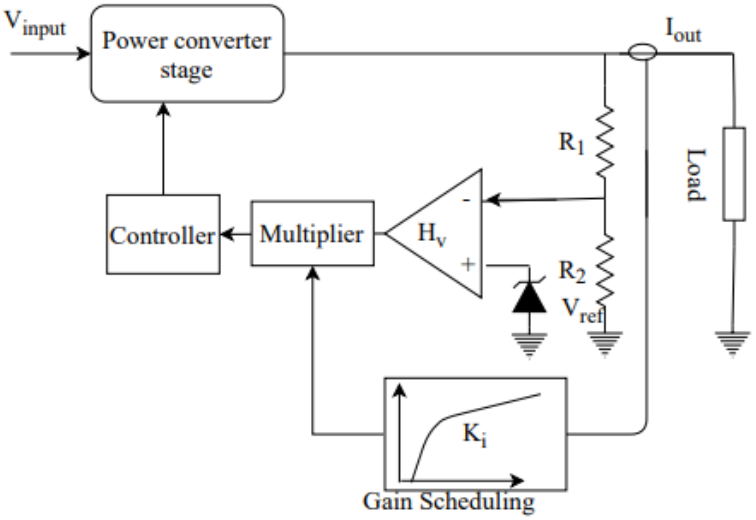



(c)

Figure 2. 4 Voltage droop via different schemes: (a) voltage droop via output current feedback (b) voltage droop for a current-mode converter with low voltage DC gain (c) programming voltage droop control via nonlinear gain

Conventional droop methods have a few advantages. These advantages are associated with decentralization control circuits of parallel converters, high modularity, and reliability. However, the aforementioned conventional droop methods are associated with degradation in voltage regulation at the load and poor current sharing. Furthermore, differences in cable resistances, which connect individual converters to the point of common coupling, can worsen the load current sharing in the conventional droop methods.

### 2.2.2 Improved Droop Methods

The high reliability and low cost achieved by the traditional droop methods for controlling parallel DC-DC converters are due to the elimination of interconnected communication links between parallel converters. Nonetheless, the main drawbacks of the droop method are associated with ineffective voltage regulation and low accuracy of load current sharing as a result of the cable resistance impact [24-27]. Different techniques have been presented in the literature to overcome these drawbacks. The main aim of the presented method is to improve the load current sharing and voltage deviation due to the increase of loading. One of these methods depends on mathematical optimization to find the optimal gain value. The method considers an offline approach. This approach is based on the optimal values of droop resistance, which is obtained from minimizing the total current sharing error using the particle swarm optimization (PSO) technique [28]. The approach is a heavy mathematical burden resulting in a long time to find optimal value. The most effective approach presented in the literature is based on updating the droop gain for the parallel-connected converters. The adaptive droop control method is based on the current sharing, which requires knowledge of the converters' currents. The converter currents are shared between the parallel-connected converters by a low bandwidth communication network [29]. Kim, et al. [30] proposed a novel droop method, which improves the load current sharing and regulates the output

voltage. The technique, which adaptively regulates the reference voltage for each converter, improves load current sharing and voltage regulation. However, the novel droop method does not include the effect of cable resistance. Due to the change in load, input power, or the error in the voltage feedback measurements, the output voltage can vary for parallel-connected converters. Hence, a modified droop controller is proposed by Anand and Fernandes to overcome the output voltage mismatch of the error in the measurements [31]. Also, to reduce the output voltage error of the parallel converters, the nominal voltage setpoint is modified by the circulating current measurement between converters. The converter, which experiences negative circulating current, has less nominal voltage. Therefore, the local controller increases its nominal voltage to ensure zero circulating currents. The modified droop controller does not include the cable resistance, which is the main drawback of unequal load current sharing between parallel converters.

For wireless load current sharing between converters, a virtual resistance (VR) droop method is proposed in [32]. A tertiary optimization control for parallel-connected DC-DC converter is implemented in this method to improve the efficiency of VR droop method. By varying VR, the load sharing between converters decision is made to adjust the load current sharing. Stability analysis is studied to demonstrate the effectiveness of varying VR on the dynamic performance of the system. The tertiary optimization control, which is based on a hierarchical control system (centralized control), requires a communication network, as shown in Figure 2.5.

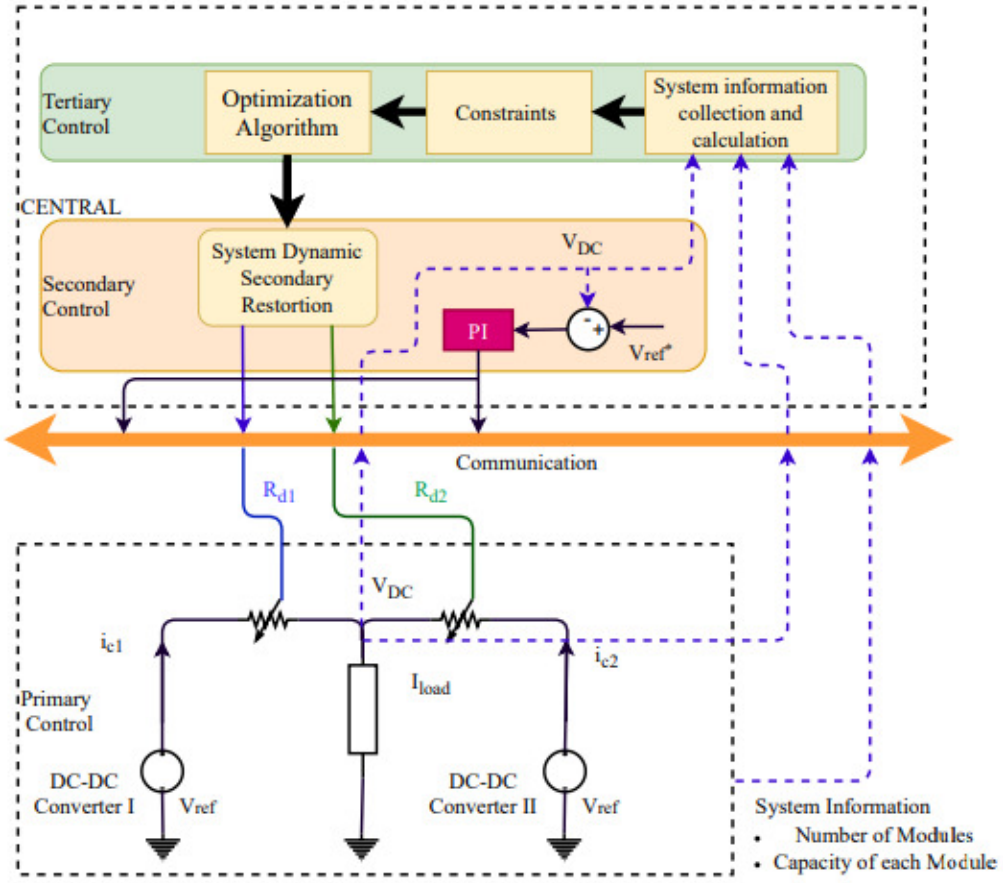



Figure 2. 5 Hierarchical Control in DC system

Another virtual resistance method is presented in [33]. The virtual resistance method is based on the droop index algorithm to minimize the circulating current and improve the load current sharing differences between parallel-connected converters. For the droop index algorithm, a virtual resistance value is calculated based on the output voltage mismatch between parallel-connected converters and normalized current sharing. The minimization of circulating current is achieved, and load current is improved during the transient and steady-state conditions. However, the droop index is calculated instantaneously. It uses the measurements of the output currents and voltage for each converter, which requires a communication network for the droop index algorithm, as shown in Figure 2.6.

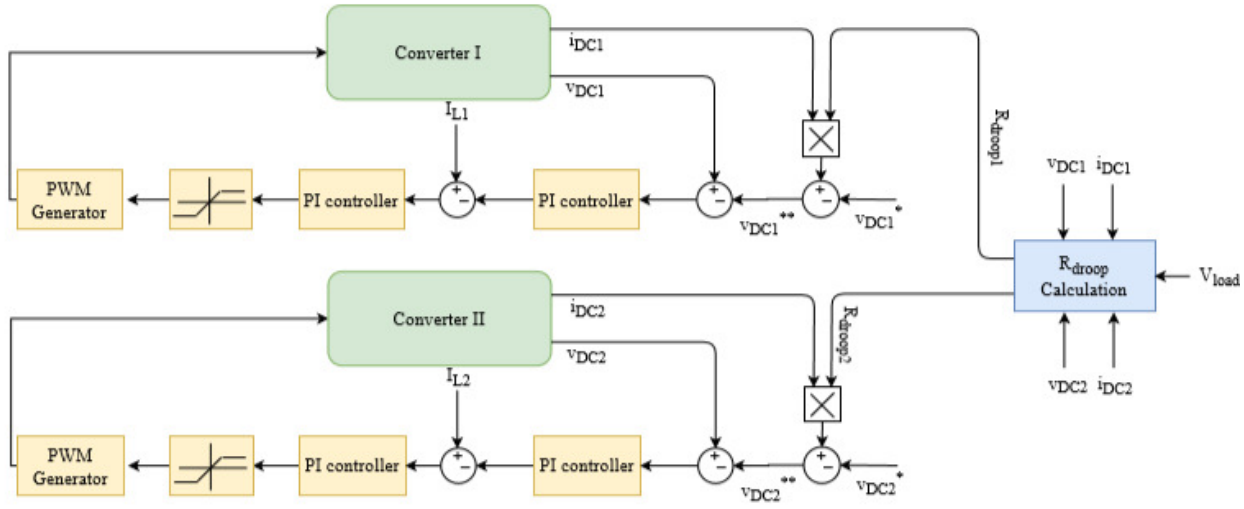



Figure 2. 6 Block diagram of parallel-connected converters with $R_{droop}$ calculation

A low bandwidth communication network is used in a three-level hierarchical control algorithm, which is presented in [34]. The three-level hierarchical control algorithm is used to minimize the mismatch in the output voltage of the parallel-connected converters due to the droop method. However, the cable resistance is not considered. A decentralized controller is presented in [35], which is based on the droop controller. The voltage in the DC microgrid varies due to the change in load. Thus, achieving current sharing is hard. However, the load current sharing is improved by using another control loop, which uses low bandwidth digital communication between the converters, as shown in Figure 2.7.

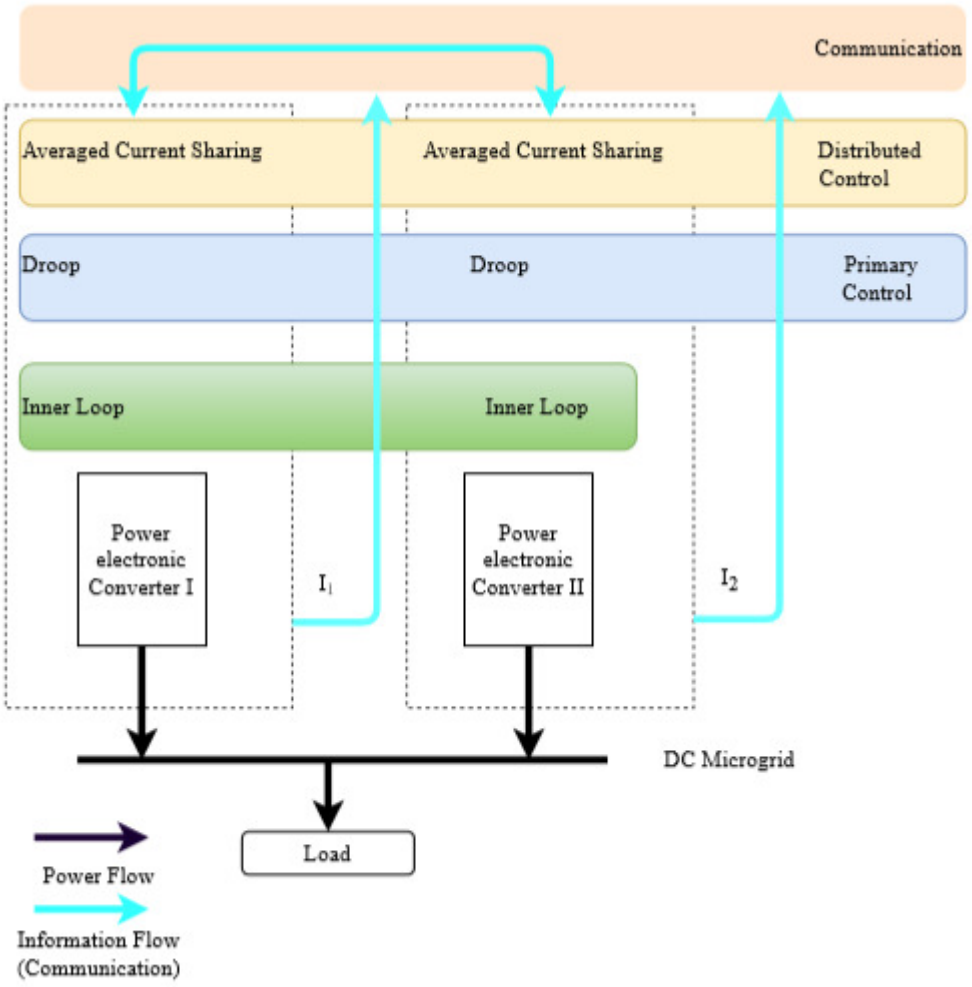



Figure 2. 7 Distributed control for parallel-connected DC-DC converters in a DC microgrid.

Another virtual droop gain is presented in [36], which is based on an adaptive droop control method. The method uses instantaneous virtual resistance to eliminate the voltage difference. It also minimizes the current sharing difference when a different cable resistance is presented. However, the instantaneous virtual droop gain is calculated based on the normalizing current sharing differences and the losses in the output side of the converters, which are a function of the individual output voltage and current for both converters. Thus, it means a communication link is needed between parallel-connected converters.

An enhancement in the performance of the droop methods is associated with using communication links such as given in [37]. The improved method uses a low bandwidth communication to exchange the measurement of the current and voltage between parallel converters. It uses the average voltage and current controllers locally to enhance the current sharing and voltage restoration, as shown in Figure 2.8. The low bandwidth is used for changing the values of current and voltage during the various operating condition in the DC microgrid. The local controller is achieved by the decentralized controller scheme.

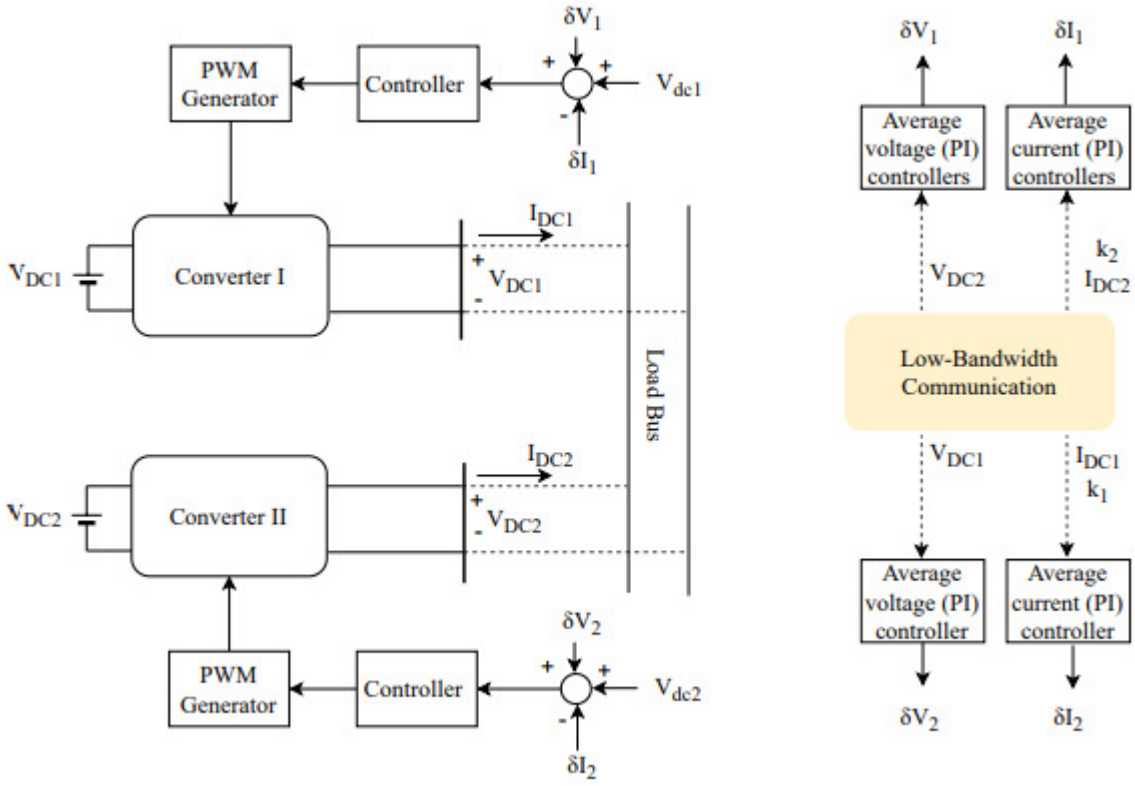


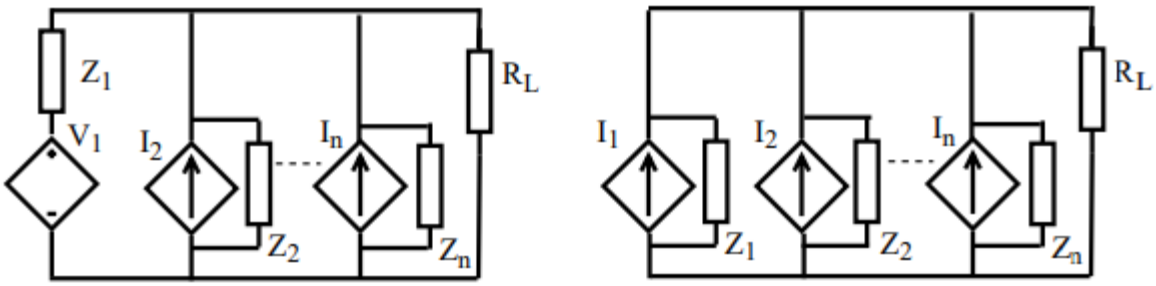

Figure 2. 8 Block diagram of the improved droop method based on the averaged voltage and current controller

Although the modified droop methods, such as virtual resistance, adjust the output voltage by making their slopes steeper, an improved droop method uses a digital communication scheme to

regulate the output voltage [38]. The improved droop method regulates the output voltage set point by sending a digital signal from a converter, which experiences the highest load current to the other converters. The highest current depends on a selected current setpoint, which is chosen in advance. When the converter, which experiences the highest current, reaches its set point, a digital signal is sent to the other parallel-connected converters to regulate their output voltage. The sender converter does not respond to its digital signal. When the output voltage is regulated for the other converters, the session for this set point is terminated. Therefore, a new process is started. Similarly, the newer session is based on the converter experiencing the highest load current, which determines the selected current set point.

## 2.3 The Active Current Sharing Methods

Most of the active current sharing methods have a common basic feature, namely, the need for signal processing of sharing current error between parallel converters. The distributed common reference signal between the parallel converters modifies and adjusts the controller of each converter to achieve a precise current sharing. The active sharing current can be classified based on the signal processing approach of sharing current into master-slave current methods and averaged current methods. From the circuit theoretical viewpoint, the master-slave current methods can be represented by one Thevenin source with many Norton sources in parallel, as shown in Figure 2.9 (a), while the average current methods can be presented by Norton sources in parallel only as shown in Figure 2.9 (b) [19,20].




(a) (b)

Figure 2. 9 Circuit theoretical viewpoint of the active current sharing methods

According to the current sharing strategy, there are three control modes of operation, which are inner and outer loop regulation modes and external controller mode. In the inner loop regulation mode, the sharing signal processor is used to adjust the output voltage for each controller. It is utilized to determine the output voltage setpoint for each converter to achieve a desired current sharing. The outer regulation mode of operation uses the current-sharing error signal to adjust the output voltage of each converter until equal load current distribution is achieved. The difference between the inner and outer loop regulation modes of operation is that the voltage compensator for the outer loop regulation of each converter is independent compared to the inner loop regulation. The external controller mode is achieved by comparing all load current sharing signal of individual power converters. The comparison is used to adjust the feedback controller for each converter to achieve equal load current sharing.

### 2.3.1 Master-Slave Current Method

The master-slave current control method can be implemented in different ways [39-41]. One of the initial implementations is based on the current mode control of PWM converters, as shown in

Figure 2.10. The master converter only has one voltage compensator, and it generates a current reference signal, which is sent to the slave converters. An accurate current sharing is obtained, and the master converter regulates the output voltage. An analog wireless communication scheme for the master-slave current control is implemented in [39]. The master converter provides the current reference value through a high-speed communication link [40,41]. The reference current signal is sent through a high-speed communication link to the slave converters, which operate in current-controlled mode only. The high-speed communication between converters improves system performance and minimizes the time delay. The total cost for master-slave current control is increased due to the use of high-speed communication link such as a digital communication scheme. In the case of medium and high -power applications, increasing the total cost would not be appropriate, but, in low power applications, an analog controller with wires is applicable, where the converters are located close to each other.

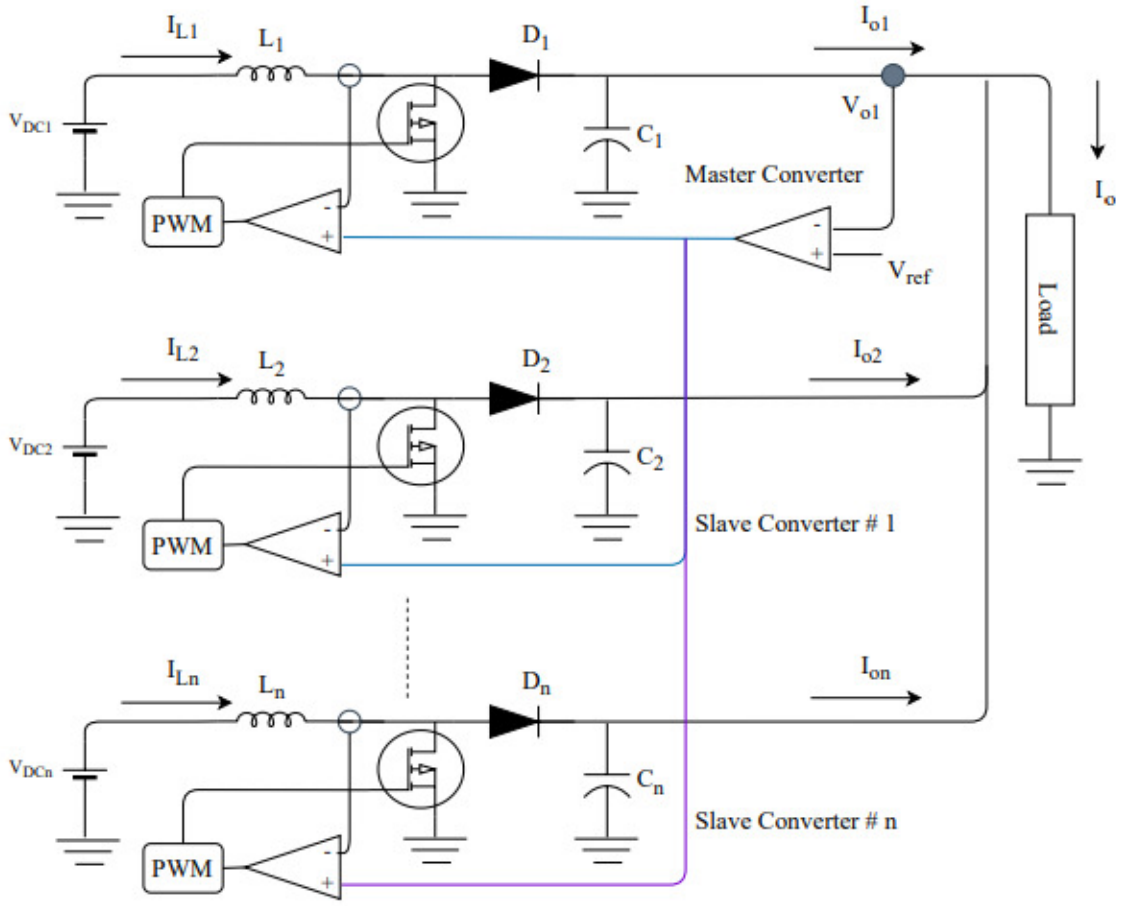



Figure 2. 10 Master-slave current sharing with current-mode control

The master-slave approach is more expensive to implement and less reliable compared to the droop method due to the use of an analog wireless or intercommunication link between converters and the presence of a single master controller.

### 2.3.2 Average Current Method

The desired current sharing is achieved by active feedback controls, which require a single wire communication or current sharing bus. The current reference for each converter is provided by the current sharing bus. However, the need for output voltage regulation requires all parallel converters to have the same voltage level. The voltage references for individual converter will have slight differences, which will be needed to overcome the issue of voltage regulation conflict problems.

A few schemes of the averaged current method are proposed in [42-44]. The basic scheme is proposed in [42], which is an automatic average current sharing technique. In this method, a uniform load current sharing is achieved without sacrificing the voltage regulation performance. The deviation of the output current of the parallel converters is eliminated by adjusting the reference voltage of the voltage feedback error amplifiers of the individual converters, as shown in Figure 2.11. There is no master or slave module, as shown in Figure 2.10, and the information of the average current is obtained at the shared bus via a resistor. The adjusted amplifier senses if there is a differential across the resistors, and it regulates the control loop of the converter to achieve an equal load current sharing.

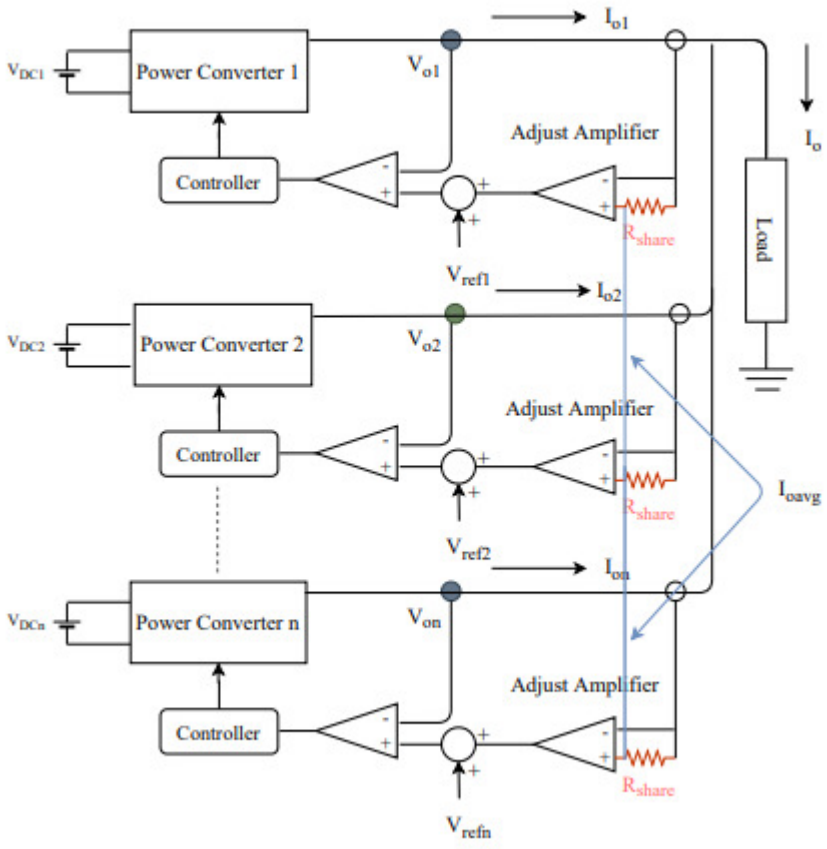



Figure 2. 11 Average current sharing technique

Although the current information of all parallel converters is included in the current sharing bus, as shown in Figure 2.11, the whole system crashes in case of the failure of a converter of the parallel scheme. Furthermore, the disadvantages of average current sharing are the complexity of the control structure for achieving an accurate current sharing and low modularity due to the need for interacting current sharing loops.

## 2.4 Limitation of Existing Methods

The conventional droop methods are known to linearly reducing the output voltage as the load current increases. However, conventional droop methods suffer from the following performance limitations:

- The conventional droop method has poor load sharing currents as the output currents are increased; furthermore, with the consideration of the cable resistance, the current sharing degradation increases.
- Voltage regulation is raised when the load current increases. When a step increase in the load is applied, the DC microgrid voltage is dropped due to the droop action.
- The mismatch in the output voltage of the parallel-connected converters due to the cable resistance differences will raise the issue of circulating current.

The improved droop control methods are presented to overcomes the drawback of the conventional droop method, but they use a communication network to improve voltage regulation and load sharing currents. The communication network increases the investment cost and lowers the reliability of the system. The active current sharing methods, such as the master-slave, is also implemented using a high-speed communication link to minimize the time delay and improve system performance. The high-speed communication link, such as a digital communication

scheme, increases the total cost. Furthermore, the failure of the master converter affects the reliability of the system. The avenging current sharing technique is associated with the complexity in the control structure and low modularity due to the need for interacting current sharing loop.

## 2.5 Modeling DC-DC Converters

There are a few approaches for modeling and analyzing of DC-DC converters. However, the most widely used approach is the small-signal stability analysis based on the state space averaging technique, which is presented by Middlebrook and Cuk in [45]. The state-space description for the switching network was replaced by representing the averaged switching effect for one cycle of the operation. The state-space average model for one cycle is simplified by perturbing the averaged effect of the switching around a steady-state operating point. The averaged system around a point is then linearized and results in perturbed equations from which the system characteristics can be obtained.

The validity of the averaged model varies with the switching frequency even for the same topological structure. Certain assumptions are made in the continuous technique for achieving the final simplified averaged model. The linear ripple approximation is the first assumption, which is valid and accurate when the switching frequency is higher than the natural frequency of the circuit. The second approximation affects the output duty ratio function, which is generated from a closed-loop regulator. The second approximation may be affected by the accuracy of the averaging technique when the natural frequencies approach one-half the switching frequency, which is known as the fast-scale dynamic response or the high-frequency regime. The accuracy of the averaged model degrades when the switching frequency of the converter decreases [46]. Thus, for complex hybrid power electronic systems, the methodologies of averaged technique mode can be affected.

## 2.6 The Objectives of the Research

The objective of the present study is to propose an improved droop method, referred to as an alternative droop method. The proposed method achieves precise load current sharing, improved voltage regulation, minimization of circulating current, and elimination of communicating data between parallel converters. It decentralizes the control scheme for each converter to increase the reliability of the system. The proposed method ensures synchronous switching for different sizes of parallel-connected boost converters during various conditions such as a change in load. It eliminates the initiation of circulating current. The analytical load regulation characteristic of the proposed method is developed and modified by treating the cable resistance as part of the load regulation characteristic for each converter. The implementation of cable resistances in the proposed method is used to estimates the operating setpoint for the parallel-connected converters. The estimated setpoint values are based on the measurement of voltage and current at the point of common coupling. The setpoint for each converter is determined locally and does not require transferring data between parallel converters. The elimination of communication network, which is used to optimize or determine the virtual gain in the other improved droop methods, reduces the complexity and the cost and increases the system reliability. The proposed method utilizes a control algorithm loop to overcome the issue of the mismatches in the parameters of parallel-connected boost converters. Proper load current sharing is achieved while the mismatches in the parameters of the parallel-connected converters are presented.

The improved droop method uses a virtual droop gain, which is a predetermined value. The virtual droop gain compensates for the differences in the cable resistances. The virtual droop gain modifies the droop gains of each converter by making the slope of the load regulation characteristics steeper or flatter. The results of the virtual droop gain improve the load sharing of

parallel-connected converters. Furthermore, an adaptive voltage control gain (AVCG) for controlling parallel-connected boost converters is the last implemented part of the proposed method. The AVCG improves the voltage regulation at the point of common coupling. Therefore, The alternative droop strategy technique does not require transferring the current and voltage measurements between parallel converters. It maintains the voltage at the point of common coupling at its rated value. The proposed method ensures precise current sharing between parallel converters when different cable resistances and mismatches in the parameters of the converters are presented. Finally, a developed MATLAB model is simulated for a residential standalone PV system. The MATLAB model is used to illustrate the improved droop control method for a particular application of controlling two parallel-connected boost converters in the standalone PV system, as shown in Figure 2.12. The PV system uses a maximum power point tracking (MPPT) approach based on a bisection numerical algorithm to extract the maximum power from the PV system. The schematic diagram of the conventional PV system with a storage system is shown in Figure 2.12 [47]

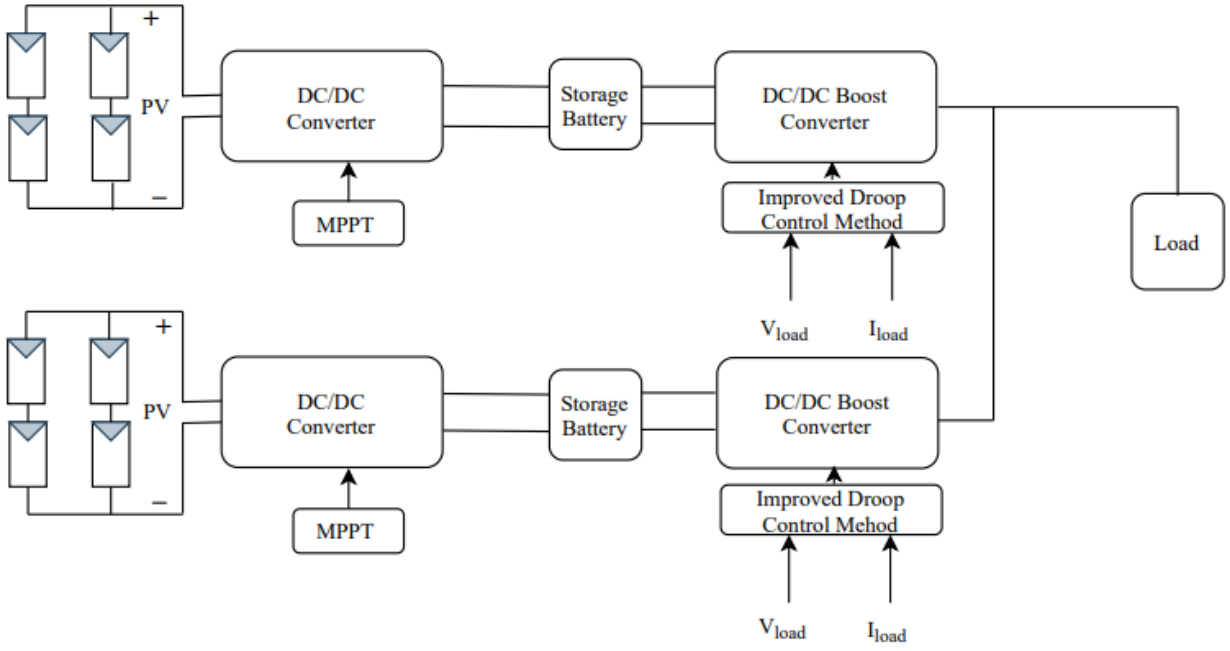



Figure 2. 12 Schematic diagram of a standalone PV system with storage

## 2.7 Summary

This chapter gave a categorized introduction about the classification of control methods for parallel-connected converters. Some of the droop methods and the active current sharing methods were presented. The advantages, disadvantages, and limitations of each method were discussed. A literature review of the improved droop method is included in the previous discussion. This exploration led to the realization of the common challenges of implementing the improved droop methods in a DC microgrid. Since the point of common coupling is present in a DC microgrid, the necessity of eliminating the communication network between parallel-connected converters is addressed. The discussion shows the need to find an improved droop method to overcome the issue of transferring the measurements between parallel converters. The subsequent chapters are assigned to addressing the development, analysis, and experimental implementation of the proposed improved droop control method.

# Chapter 3

# Circulating Current Minimization in Parallel-connected DC-DC Converters

## 3.1 General

Renewable energy resources (RESs) have become a popular source for producing electric energy in many countries around the world. These energy sources can offer the following advantages: (i) the creation of generation mixes to offset the fossil-fuel-based electric power generation. (ii) the improvement of clean and sustainable electrical energy production [48]. The integration of RESs into the grid utilizes power electronics technology, which gives flexibility in the DC conversion and power regulation. This makes the DC microgrid highly efficient, reliable, controllable, and economical compared to AC microgrid [49,50].

In a DC microgrid, DC-DC converters are used to interconnect the renewable sources and the load. The operation of parallel-connected DC-DC converters in DC microgrid is gaining more attention due to its possible advantages over a single power electronic supply. Such advantages include the improved efficiency, reliability, flexibility of maintenance, and system expansion are some of these advantages. However, the control of parallel-connected Dc-DC converters is challenging because a small mismatch in the output voltage ($\pm 1\%$) can initiate a circulating current, which leads to load current sharing differences. The parametric variation of the converter, errors in measurement voltage and current feedback, and sudden changes in the load, are the main reasons for the differences in output voltage [51].

In this chapter, the investigation of synchronous switching with circulating current initiation for two parallel-connected converters is presented. For different sizes of converters, the initiation of circulating current is caused by asynchronous switching, which is a result of the differences in time delay of the control loops for the parallel-connected converters. Therefore, an optimized controller is designed based on the droop control method to eliminate the circulating current. Based on the previous analysis, a modified droop method based on master current control for parallel-connected dc-dc boost converters is presented. An optimized controller for the modified droop method is used to set the droop gain for the droop load characteristic for each converter. As a result, synchronous switching is achieved during the change in the operating condition, such as load change.

## 3.2 Design of PI controllers for Parallel-connected DC-DC converters

The operating parameters for two boost converters with different sizes are shown in Table 3.1. The parameters are calculated based on Continuous Conduction Mode (CCM) operating condition [52].

Table 3. 1 Operating values for boost converter

| Parameters | Converter I | Converter II |
|---|---|---|
| Switching frequency $\boldsymbol{f_s}$ | 25 KHz | 25 KHz |
| Inductance $\boldsymbol{L}$ | 23.712 mH | 11.856 mH |
| Capacitance $\boldsymbol{C}$ | 86.667 µF | 173.333 µF |
| Power $\boldsymbol{P}$ | 96 W | 192 W |

$PI_{id}$ controller for the inner current loop and $PI_{vi}$ controller for the outer voltage loop are designed based on the small-signal model given in Appendix A and using SISO Tool from Matlab/Simulink to tune the controller and evaluate the stability of the converter [53,54]. The parameters of the $PI_{vi}$ and $PI_{id}$ controllers for the two parallel-connected boost converters are given in Table 3.2.

Table 3. 2 Parameters of the PI controller for boost converter

| Type of Controller / Gains | | $PI_{id}$ Controller | $PI_{vi}$ Controller |
|---|---|---|---|
| Converter I | Proportional gain $k_p$ | 0.07045 | 0.018204 |
| | Integral gain $k_i$ | 25.161 | 12.136 |
| Converter II | Proportional gain $k_p$ | 0.0180914 | 0.0398199 |
| | Integral gain $k_i$ | 10.642 | 17.313 |

## 3.3 Parallel Operation of DC-DC Boost Converters

Figure 3.1 shows asynchronous switching mode. In this mode of operation, SW1 and SW2 do not open and close simultaneously. If SW1 is closed while SW2 is opened, diode D1 is OFF and diode D2 is ON, and vice versa.

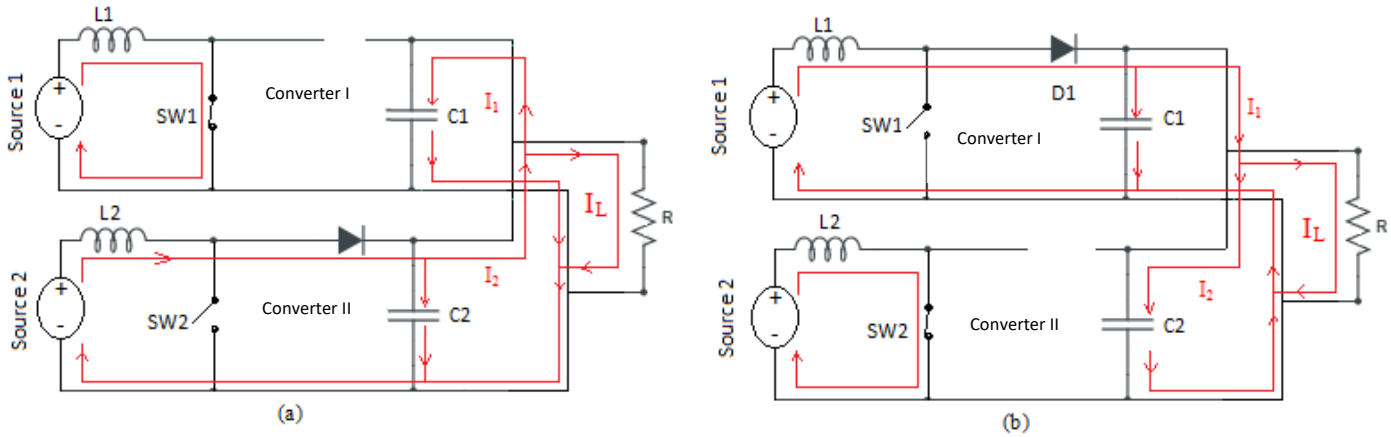



Figure 3. 1 Asynchronous switching of two parallel-connected converters

The circulating current is initiated from converter II to charge capacitor C1 if SW1 is ON and SW2 is OFF as shown in Figure 3.1 (a). Similarly, the initiation of circulating current that flows from converter I to charge capacitor C2 occurs if SW1 is OFF, and SW2 is ON as shown in Figure 3.1 (b). Thus, circulating current is initiated between parallel-connected boost converters during the asynchronous mode of operation when the switching of the parallel-connected converter is not

synchronized. Figure 3.2 shows synchronous switching for two parallel-connected converters. In this case, there are two modes of operation. The switches SW1 and SW2 are synchronized during their operation.

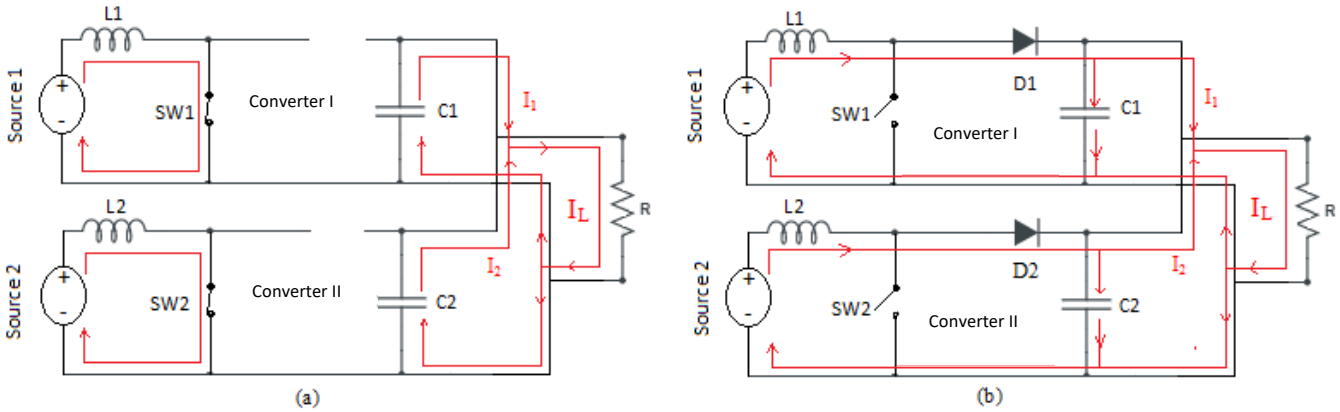



Figure 3. 2 Synchronous switching of two parallel-connected boost converters

As illustrated in Figure 3.2 (a), the switches SW1 and SW2 are closed simultaneously, the diodes D1 and D2 are opened due to the reverse biased. During this mode of operation, both capacitors will be discharging through the load. After the switches, SW1 and SW2 are opened, as shown in Figure 3.2 (b), the charging mode for both capacitors is started. At the same time, the load current is supplied directly from both sources (source 1 and source 2).

## 3.4 Droop Control Method

Figure 3.3 shows a schematic diagram of two parallel-connected DC-DC boost converters.

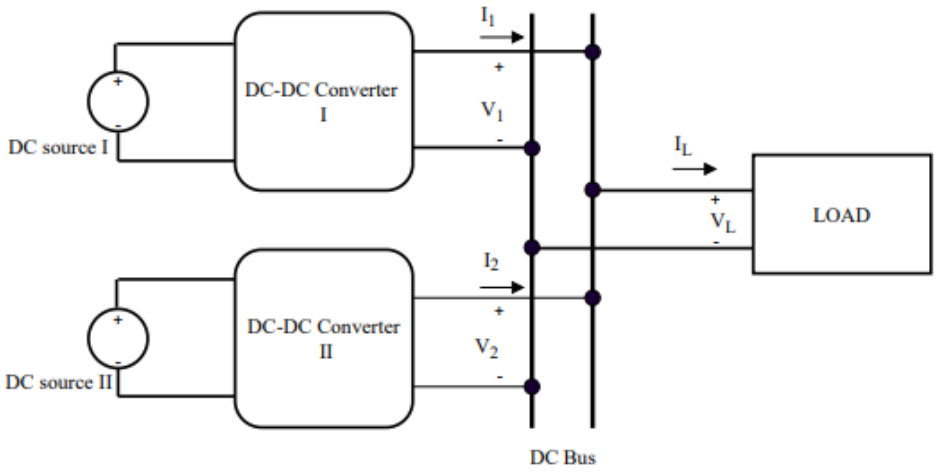



Figure 3. 3 Schematic diagram of the two parallel-connected converters

The two boost converters in Figure 3.3 connect the two different DC sources I and II to the load. They are connected in parallel to a common DC bus. Because this study focuses on the synchronous switching of parallel-connected converters, the cable resistances, which connect the converters to the common DC bus, are assumed to be part of the load resistance. Therefore, the output voltage of each converter is equal to the load voltage, and the load current is the sum of the individual current of both converters. The output voltage and current can be determined based on the load regulation characteristic for each converter [55,56]. Figure 3.4 shows the load regulation characteristic of the droop method along with the two dc-dc boost converter droop gains ($K_1$ and $K_2$). As indicated in Figure 3.4, although the droop gains of boost converters I and II are set based on their rating, the droop gain for converter I is higher than the droop gain of convert II. However, the voltage setpoint is updated locally based on the droop load characteristics for each converter because there is no interconnection between both converters. In general, for $n$ converters connected in parallel, the output voltage of each converter droops as the output current increases and is expressed as

$$V_n = V_{n(sp)} - K_n * I_n \tag{3.1}$$

Where $V_{n(sp)}$, $V_n$, $K_n$ , and $I_n$ are the setpoint of output voltage, droop gain (virtual resistance), and output current respectively of unit $n$. $n$ in this study is either 1 or 2 for converter I and converters II, respectively.

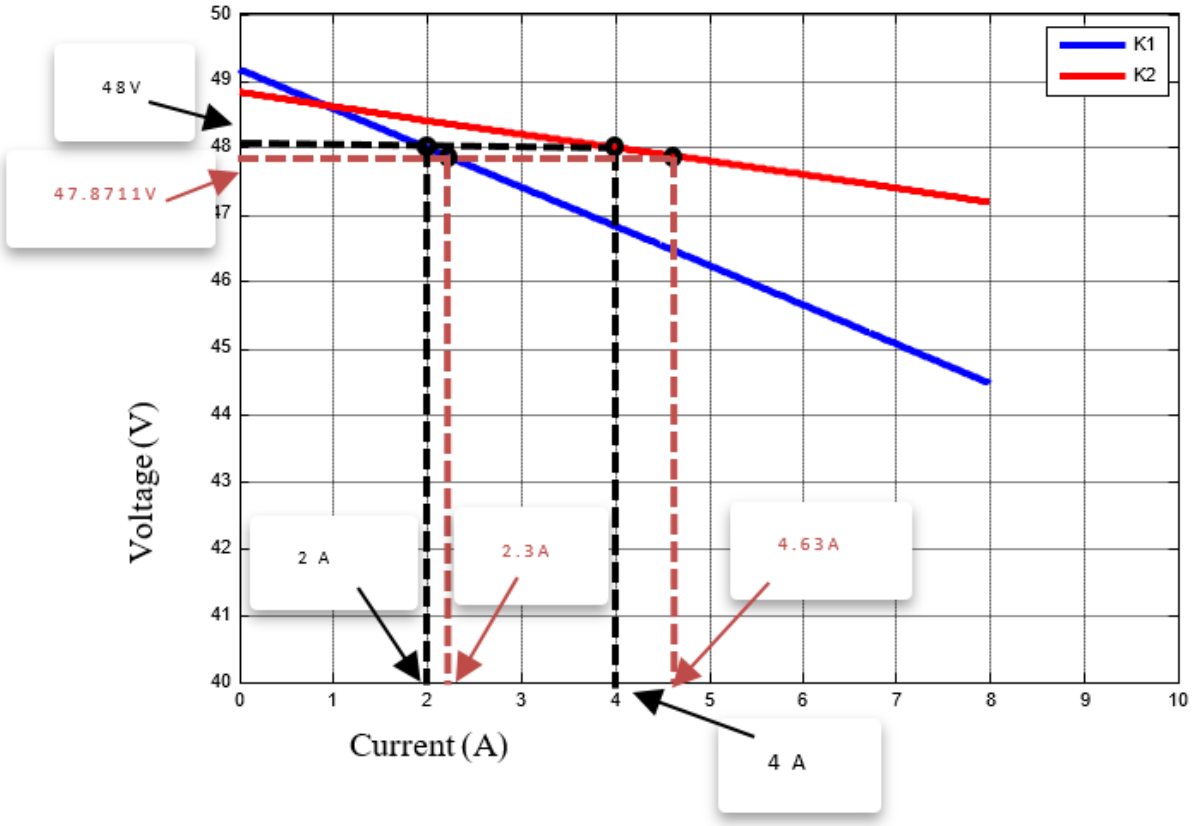



Figure 3. 4 Load regulation characteristic of the droop method with $K_1$ and $K_2$

The setpoints for voltage ($V_{1(sp)}$, $V_{2(sp)}$) Figure 3.5 are regulated based on the load regulation characteristic shown in Fig.3.4. The set point for both converters is equal because the resistances of connecting cables are considered as part of the load resistance in this study. Thus, the value of $V_{1(sp)}$ and $V_{2(sp)}$) are equal to the value of $V_{sp}$. For a set point $V_{sp} = 48\,V$ , the total load current is $I_L = 6\,A$. The load current is shared between both converters based on their load characteristic droop. The load current sharing is $2\,A$ and $4\,A$ for converter I and II respectively as shown in Figure 3.4.

However, if the voltage is decreased to a new set point, $V_{sp} = 47.87\ V$, the load current sharing will be $2.3\ A$ and $4.63\ A$ for converter I and II respectively as shown in Figure 3.4. Therefore, for different sizes of converters, the load current sharing is based on their ratings.

## 3.5 Optimized Controller

The parameters for the optimized controller are designed based on the small-signal model analysis given in Appendix A and are summarized in Table 3.3.

Table 3. 3 Optimized PI controller parameters for boost converters

| Gains \ Type of Controller | | $PI_{id}$ Controller | $PI_{vi}$ Controller |
|---|---|---|---|
| Converter I | Proportional gain $k_p$ | 0.0119196 | 0.0145848 |
| Converter II | Integral gain $k_i$ | 29.799 | 12.154 |

The block diagram of the two cases of study is shown in Figure 3.5 [57]. The two parallel-connected boost converters with a non-optimized controller are shown in Figure 3.5 (a), and Figure 3.5 (b) shows the case of the optimized controller.

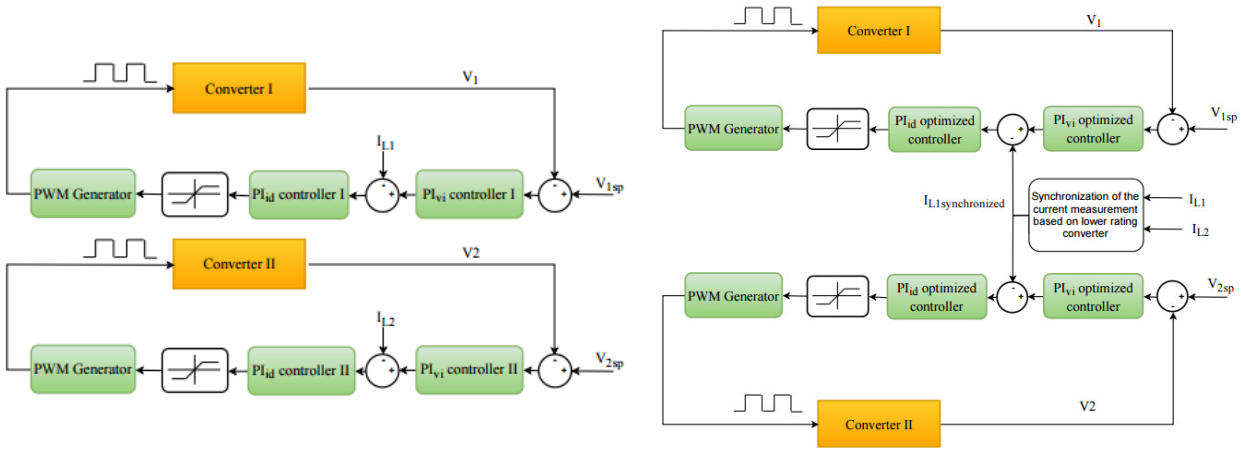



Figure 3. 5 Block diagram of two parallel-connected dc-dc boost converters with (a) Non-optimized control loop and (b) Optimized control loop

As can be seen in Figure 3.5 (b), the current measurements for both converters are synchronized to avoid any mismatch in the feedback signal of the optimized controller loop. The load sharing based on the converter rating is used, as shown in Figure 3.5 (b). This concept synchronizes the current measurements as

$$I_{L1synchronized} = (I_{L1} + I_{L2}) * (\frac{P_{converter\ I}}{P_{converter\ I}+P_{converter\ II}}) \quad (3.2)$$

$$I_{L2synchronized} = (I_{L1} + I_{L2}) * (\frac{P_{converter\ II}}{P_{converter\ I}+P_{converter\ II}}) \quad (3.3)$$

Where $P_{converter\ I}$ and $P_{converter\ II}$ are the rated power of converter I and II, respectively. The values of $I_{L1synchronized}$ and $I_{L2synchronized}$ are simultaneous measurements, which are scaled based on the converters' rating and their contribution to the load current.

## 3.6 Simulation Results of Synchronous and Asynchronous Switching Cases

The block diagram in Figure 3.5 (a) and (b) are simulated using MATLAB environment to examine the relationship between the initiation of circulating current and the asynchronous switching of parallel-connected DC-DC converters. The idea of asynchronous and synchronous switching is presented in Figure 3.1, and Figure 3.2. MATLAB/Simulink environment is used to verify this idea. The output current for each converter and the total load current are shown in Figure 3.6 (a) and (b) for asynchronous switching and synchronous switching, respectively. For the synchronous switching case, the MATLAB/Simulink model uses equation (3.2) because it provides a better dynamic response, which is based on the rising time and the settling time.

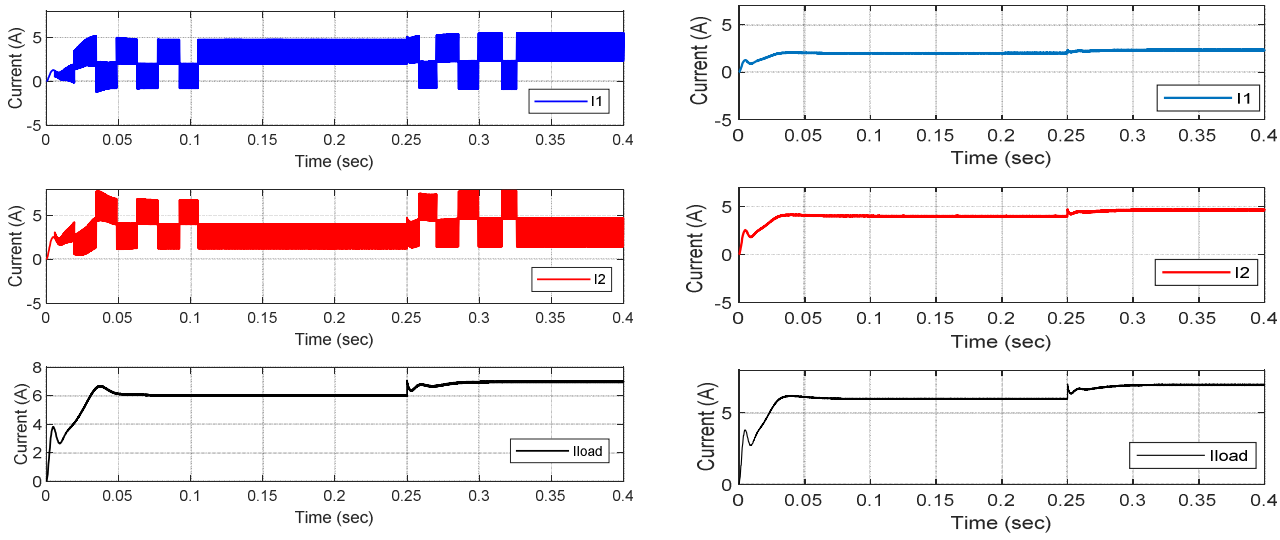
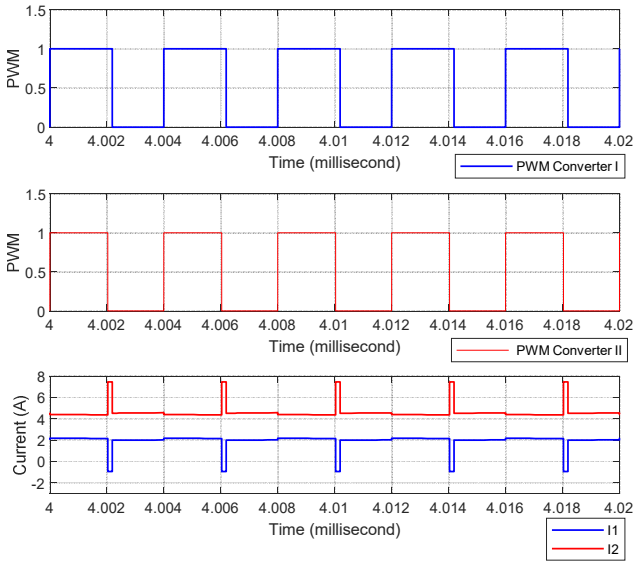
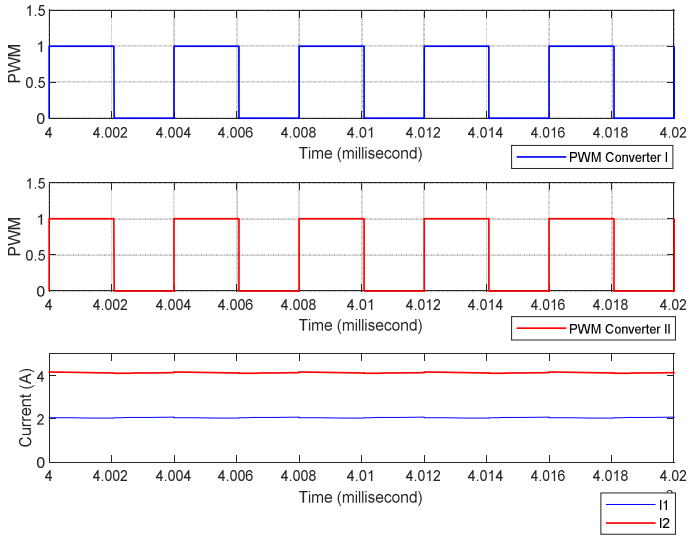



Figure 3. 6 Output current waveforms for each converter and the total load current of the simulation results. (a) Asynchronous switching (b) Synchronous switching

When asynchronous switching is applied, as shown in Figure 3.6 (a), each converter experienced a circulating current. On the other hand, the optimized controller ensures the synchronous switching of parallel converters. As indicated in Figure 3.6 (b), the output current for each converter has no initiation for circulating current because the optimized controller is implemented. In order to illustrate, Figure 3.7 (a) and (b) show the Pulse Width Modulation (PWM) for both converters. The PWM illustrates the asynchronous mode of operation versus the synchronous mode of operation. Because the switching frequency is 25 kHz, Figure 3.7 illustrates a period between 4 milliseconds to 4.02 milliseconds.




(a)

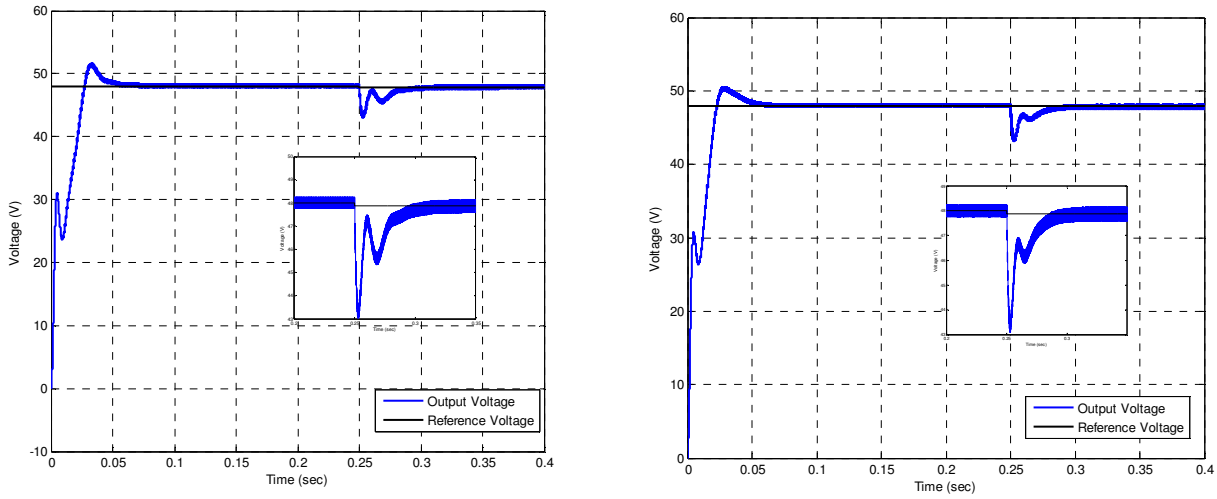



(b)

Figure 3. 7 PWM with output current for both converters. (a) Asynchronized PWM (b) Synchronized PWM.

The initial observation from Figure 3.7 (a) is that the switch of converter II is turned off at 4.01 milliseconds, but the switch of converter I is still on. The asynchronous switching forces the current to circulate from converter II to converter I. The direction of converter I current is opposite. Therefore, converter II experiences current that is higher than its sharing load current. The results in Figure 3.7 (b) have less distortion in the output current waveform for each converter compared to the results shown in Figure 3.7 (a). As shown in Figure 3.7 (b), both switches for converter I and II are synchronously closed at 4.008 milliseconds and synchronously opened at 4.010 milliseconds. For the case of the optimized controller, the control loops for both converters have the same time delay.

Figure 3.8 (a) and (b) show the output voltage waveforms for asynchronous switching and synchronous switching cases. The output voltage is regulated according to the droop method when a step increase in the load is applied at 0.25 sec.




(a) (b)

Figure 3. 8 Output voltage with the reference voltage. (a) Synchronous switching (b) Asynchronous switching

In both cases, the setpoint for the controller is adjusted at 0.25 sec. Initially, the voltage is set to 48 V, but the voltage is changed to 47.87 V at 0.25 sec. This regulation for the voltage is according to the droop method. Thus, the simulated results in MATLAB/Simulink for both cases follow the load regulation characteristic of the droop method, as shown in Figure 3.4.

## 3.7 Modified Droop Method based on Master Current Control for Parallel-connected DC-DC Boost Converters

For the two parallel-connected converters shown in Figure 3.3, zero-circulating current can be achieved by synchronizing the output voltage for both converters during the changes in the load or

the input power. The proposed modified droop method ensures current distribution based on the rating of the parallel-connected converters [58] as shown in Figure 3.10. The method adjusts the output voltage level by adjusting the reference voltage according to the droop method. For each converter, there are two control loops, which are the outer voltage loop and the inner current loop. The voltage control loop regulates the terminal voltage for each converter, and the current control loop uses one of the converters' input current as master current feedback. An algorithm based on the analytical load regulation is used to calculate the voltage setpoint for each controller to avoid any mismatch in the output voltage.

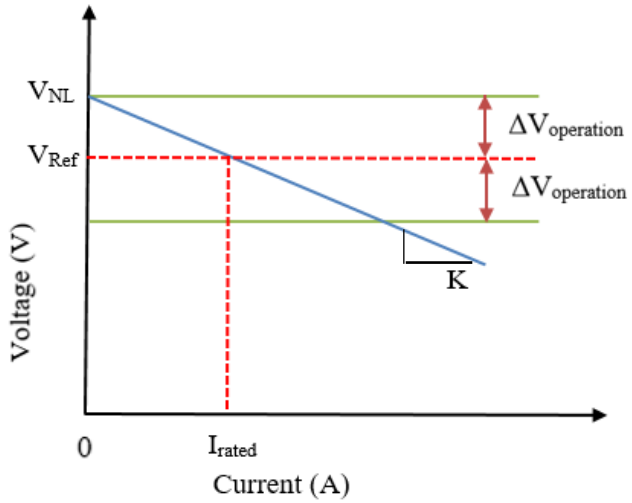



Figure 3. 9 Load regulation characteristic of the droop method with a gain of *K*

Figure 3.9 shows the general load regulation characteristics of the droop method [55,56]. As shown in the figure, $V_{ref}$ is the reference voltage, $V_{NL}$ is the no-load voltage, K is the droop gain and the value of $\Delta V_{operation}$ is the selected voltage range for the proposed algorithm. The value of $\Delta V_{operation}$ is used to calculate the voltage setpoint. Therefore, if the output voltage is not in the selected voltage range of the algorithm, the voltage setpoint for the outer loop will be constant and equal to the rated voltage of the converter. The block diagram of the two parallel-connected boost converters along with the flow chart of the proposed algorithm is shown in Figure 3.10 (a) and (b),

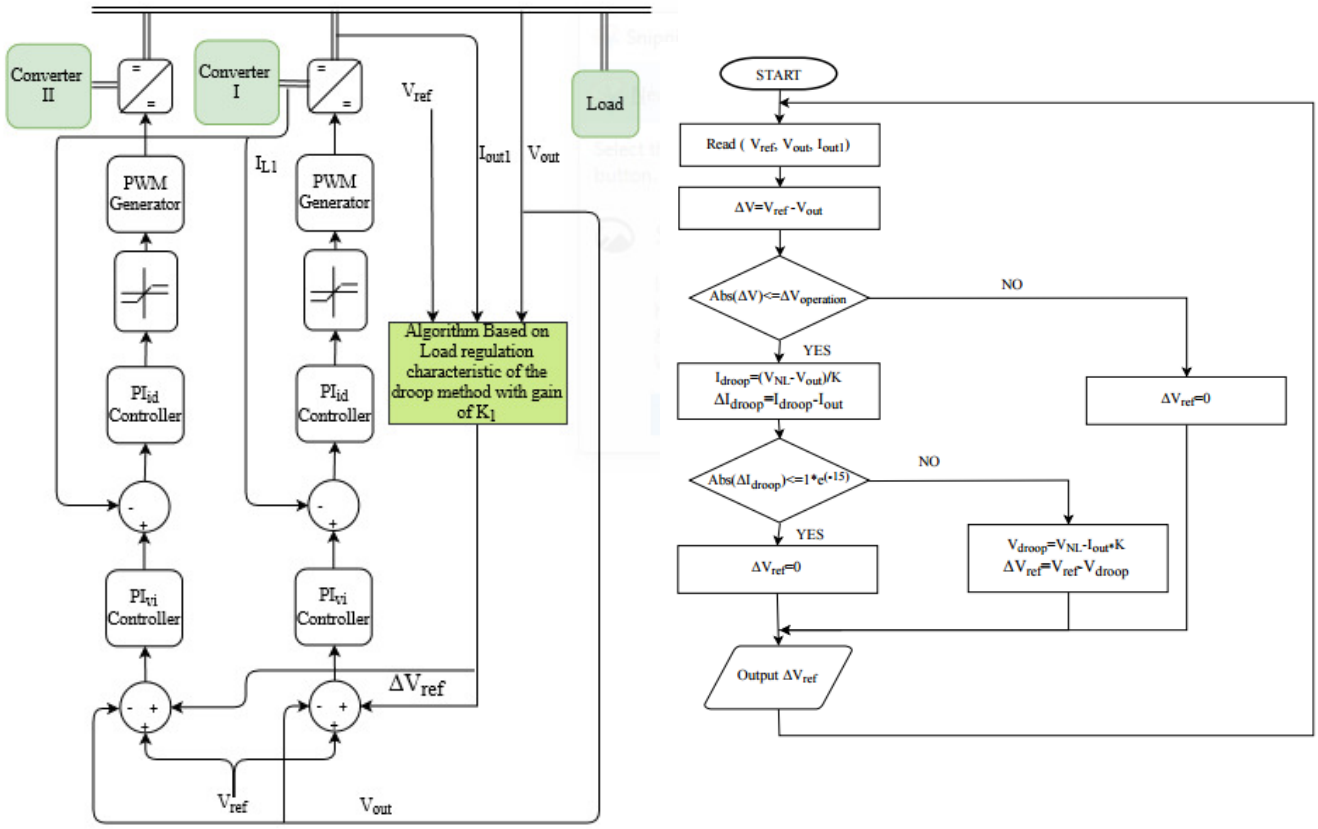
respectively. The input parameters for the proposed algorithm are the reference voltage and the measurements of voltage and current at the common DC bus. Due to the synchronous switching, the current is measured for one of the parallel-connected converters. The load regulation characteristics for one of the converters is used to calculate the voltage setpoint during the change in load. The calculation of the reference voltage is valid when the synchronous switching is achieved. From the flow chart, the first step is to check if the output voltage is within the selected voltage range. If the absolute value of $\Delta V$ is not equal to or less than the value of $\Delta V_{operation}$, the value of $\Delta V_{ref}$ is set to zero. Thus, the voltage setpoint remains at its rated value.

However, if the absolute value of $\Delta V$ is equal to or less than the value of $\Delta V_{operation}$, the output current for the selected converter is compared with the droop current ($I_{droop}$). Based on the load regulation characteristics, the droop current is calculated as:

$$I_{droop} = \frac{(V_{NL} - V_{out})}{K} \tag{3.4}$$

$$\Delta I_{droop} = I_{droop} - I_{out} \tag{3.5}$$

Where $\Delta I_{droop}$ is the difference between the calculated droop current and the actual current measurement of the selected converter.




(a) Block diagram (b) Flowchart of the proposed algorithm

Figure 3. 10 Block diagram of two parallel-connected converters with their control loops and the proposed algorithm

If the absolute value of $\Delta I_{droop}$ as per unit numerical value is less than or equal to a tolerance error $(1 * e^{-15})$, the operating point remains the same as the calculated operating point. The operating point is determined based on the load regulation characteristics for the selected converter. Thus, the reference setpoint for the voltage remains at its rated value. On the other hand, if the absolute value of $\Delta I_{droop}$ is not less than or equal to the tolerance error $(1 * e^{-15})$, the reference voltage must be adjusted based on the load regulation characteristics for the selected converter as:

$$V_{droop} = V_{NL} - I_{out} * K \tag{3.6}$$

$$\Delta V_{ref} = V_{ref} - V_{droop} \tag{3.7}$$

Where $\Delta V_{ref}$ is the difference between the reference voltage and the calculated droop voltage. The droop voltage is obtained based on the load regulation characteristics for the selected converter. The positive value of $\Delta V_{ref}$ is subtracted from the reference voltage, as shown in Figure 3.10 (a). Thus, the output voltage is required to be decreased according to the load regulation characteristics. However, the negative value of $\Delta V_{ref}$ is added to the reference voltage. This increases the output voltage. The parameters of the boost converters that are simulated in MATLAB have a mismatch of 10% and 20% in the power rating, as summarized in Table 3.4. The first case uses the parameter of DC-DC boost converter I and the DC-DC boost converter with 10 % mismatches, as shown in Table 3.4.

Table 3. 4 Operating values for DC-DC boost converters

| **Parameters** | **DC-DC Boost Converter I** | **DC-DC Boost Converter with 10% mismatch** | **DC-DC Boost Converter with 20% mismatch** |
|---|---|---|---|
| Switching frequency $\boldsymbol{f_s}$ | 25 KHz | 25 KHz | 25 KHz |
| Inductance $\boldsymbol{L}$ | 15.986 mH | 14.533 mH | 13.322 mH |
| Capacitance $\boldsymbol{C}$ | 128.646 µF | 141.51 µF | 154.375µF |
| Power $\boldsymbol{P}$ | 144 W | 158.4 W | 178.8 W |

The PI controllers for the outer and inner loops are designed based on SISO Tool in MATLAB [46]. The gains for the voltage and current PI controllers are $Kp_v = 0.016874$, $K_{Iv} = 12.98$, $Kp_i = 0.0809484$, and $K_{Ii} = 20.756$ respectively. For the first case, the load regulation characteristics have 10% mismatch, as shown in Figure 3.11. Even though there is 10% mismatch in the power rating, the load current sharing is identical to the analytical load regulation characteristics and the circulating current is eliminated because of the synchronous switching.

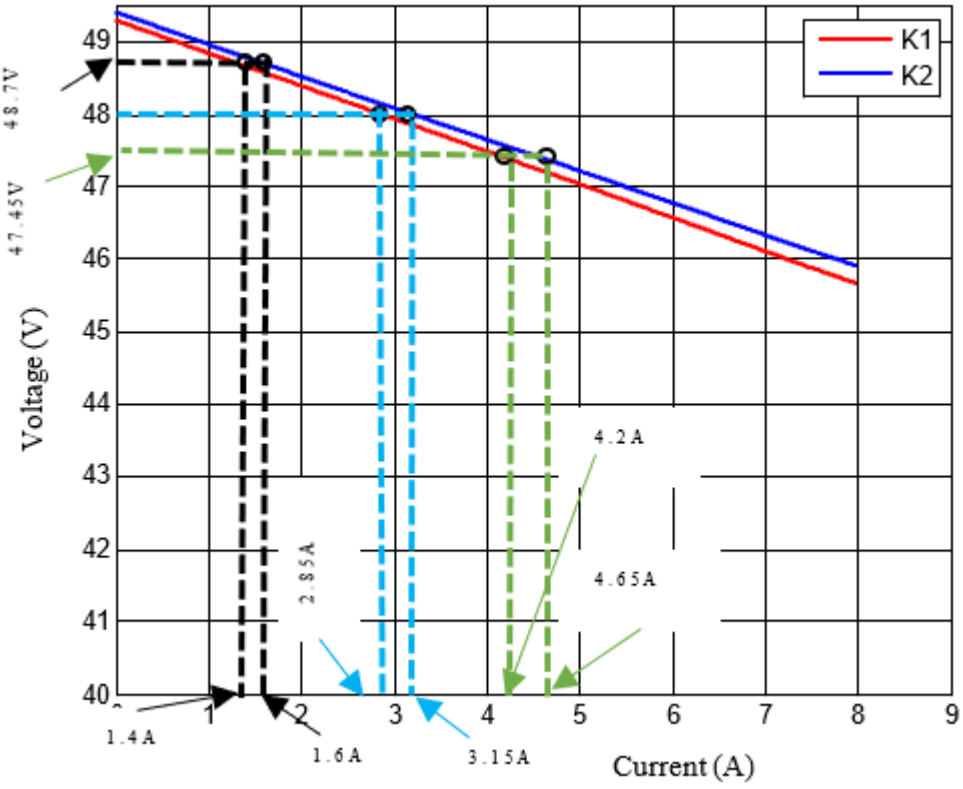
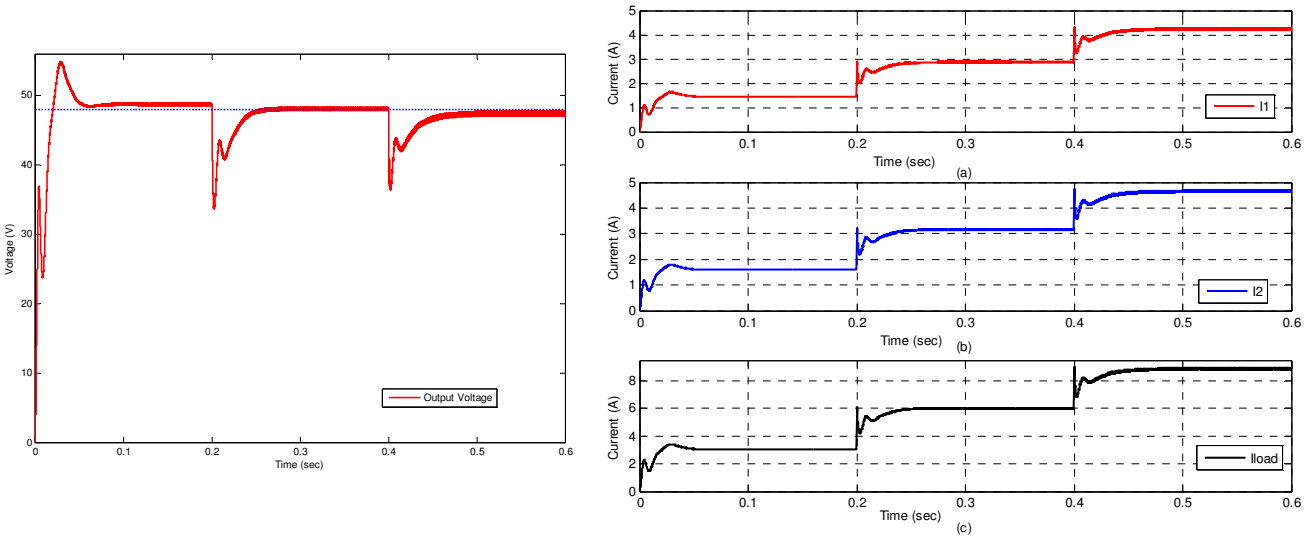



Figure 3. 11 10% mismatch in load regulation characteristic of the droop method for the two converters

Starting with an initial load is 16 Ω, the load is changed at 0.2 seconds and 0.4 seconds to values of 8 Ω and 5.33 Ω respectively. The output voltage is regulated by the proposed algorithm shown in Figure 3.10 (b). Figure 3.12 (A) shows that the regulation of the voltage follows the load regulation characteristic for each converter. The load sharing characteristics are shown in Figure 3.12 (B). When the reference voltage is set to the value of 48.7 V, the output current for converter I and converter II are 1.4 A and 1.6 A, respectively. Similarly, when a step increase in the load is applied, the load current sharing becomes 2.85 A and 3.15 for converter I and converter II, respectively. However, the voltage of 48 V is maintained, as shown in Figure 3.12 (A). When the load is increased at 0.4 seconds, the load sharing for converter I and converter II becomes 4.2 A and 4.65 A, respectively. The output voltage drops to 47.4 V, which follows the droop action. Therefore, the

load current sharing and voltage regulation based on the proposed method follow the analytical load regulation characteristic for each converter in Figure 3.11.




(A) Output voltage (B) Output currents

Figure 3. 12 Regulation characteristics for 10% mismatch. (A) Output voltage and (B) Output currents: (a) Converter I output current, (b) Converter II output current, and (c) Load current

The second case uses the parameters of DC-DC boost converter I and the DC-DC boost converter with 20 % mismatches, as shown in Table 3.4. It is implemented based on 20% mismatches of the load regulation characteristic, as shown in Figure 3.13.

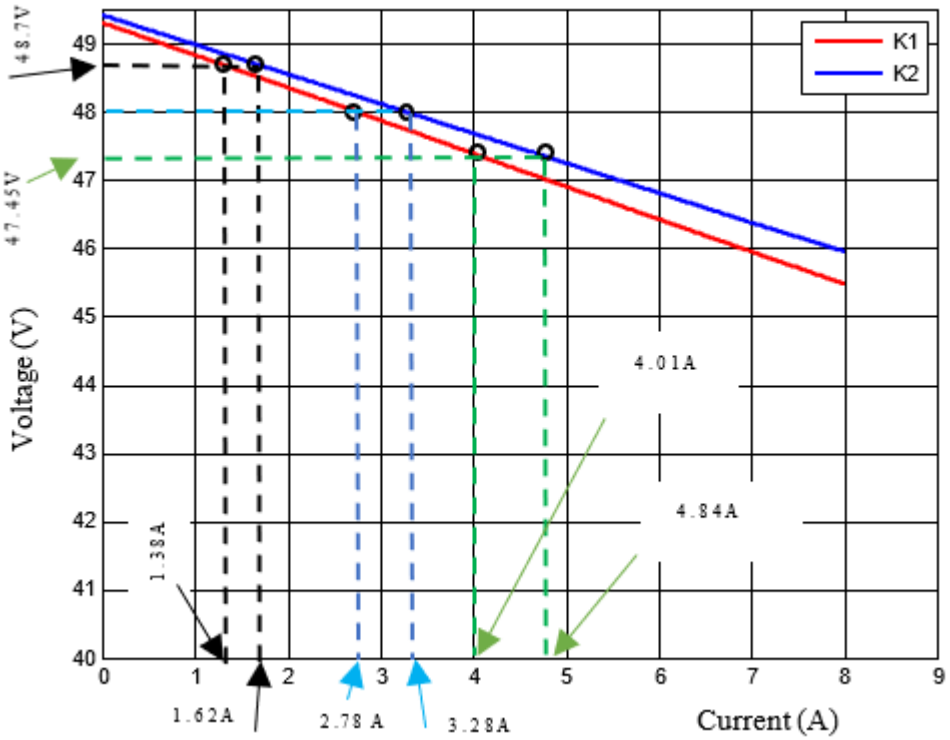
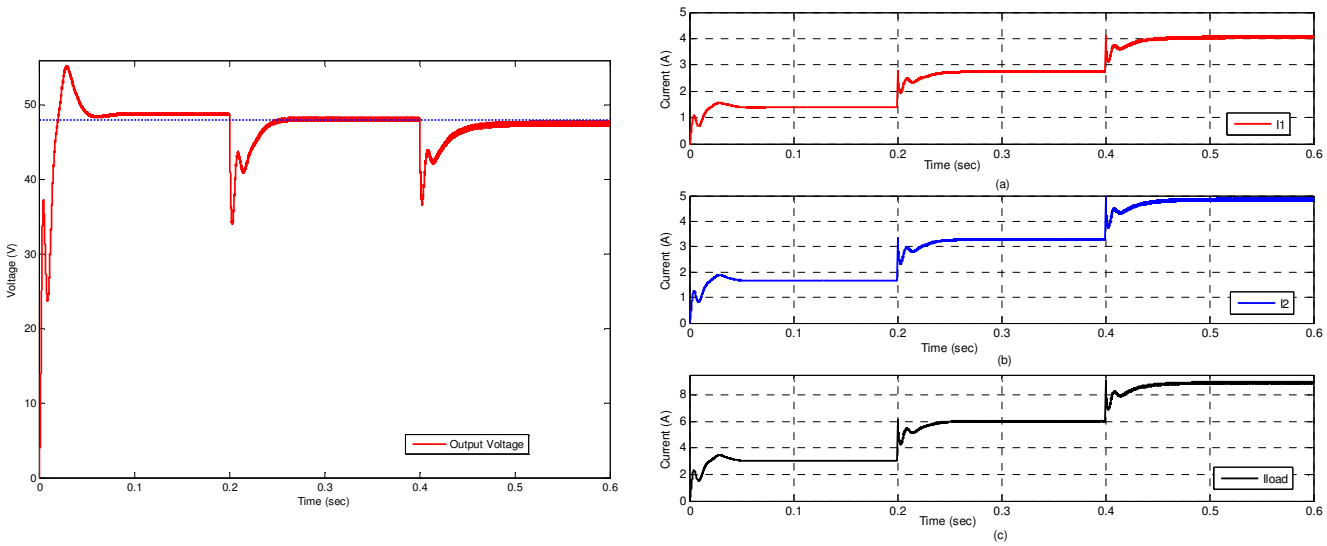



Figure 3. 13 20% mismatch in load regulation characteristic of the droop method for the two converters

Similar to the previous case, a step increase in the load is applied at 0.2 seconds and at 0.4 seconds. This is accomplished by changing the load from 8 Ω to 5.33 Ω, respectively. The voltage setpoint is calculated based on the load regulation characteristic for various load conditions to synchronize the output voltage. Initially, the output voltage is 48.7 V. The initial load current sharing for converter I and converter II is 1.38 A and 1.62 A, respectively. After the load is changed at 0.2 sec, the voltage setpoint recovers to 48 V, as shown in Figure 3.14 (A). The load current sharing for converter I and converter II is increased to the values of 2.78 A and 3.28 A, respectively. Finally, the load is increased at 0.4 seconds. This causes a drop in the voltage to 47.45 V, as shown in Figure 3.16 (A). The load current is shared based on the regulation characteristics of converter I and converter II, as shown in Figure 3.16 (B). Thus, the load current sharing for each converter is based on the analytical load regulation characteristic.




(A) Output voltage (B) Output currents

Figure 3. 14 Regulation characteristics for 20% mismatch (A) Output voltage and (B) Output currents: (a) Converter I output current, (b) Converter II output current, and (c) Load current

## 3.8 Summary

The relationship between synchronous switching and circulating current for parallel-connected boost converters is discussed. The principle of the synchronous and asynchronous switching is described for different converter sizes. The description includes the effect of the switching pattern on the initiation of circulating current. An optimized PI controller is introduced to overcome the issue of circulating current. The results show that the optimized PI controller ensures synchronous switching mode of operation, which leads to eliminating the circulating current. Furthermore, a modified droop method based on master current control is proposed for parallel converters. The modified droop method based on master current control is verified using MATLAB/Simulink environment. The proposed algorithm adjusts the output voltage according to the load regulation characteristic of the parallel-connected converters while maintaining synchronous switching. The optimized gain of the load regulation characteristics is extracted based on the optimized PI controller to achieve proper load sharing for different converter power rating.

# Chapter 4

# Load Current Sharing with Cable Resistance Implementation in Droop Method

## 4.1 General

Chapter 3 have demonstrated some of challenges for controlling and operating parallel-connected DC-DC converters. One of these challenges is related to sharing the load current equally between the parallel-connected converters [56]. At the same time, the output voltage of parallel converters must maintain acceptable voltage regulation. The parallel-connected converter might have a mismatch of their parameters due to manufacturing tolerance. The variation in parameters affects the load current sharing between parallel converters. Consequently, the output current of the parallel converters becomes higher than the other converters. The higher current, which flows through the power electronic switches, increases the losses and rating of these switches [60].

In the previous chapter, a modified droop method based on master current control was proposed for parallel-connected DC-DC converters. Practically, the converters are connected in parallel to the point of common coupling through cables that have finite resistances. In the investigation of the previous chapter, the cable resistance was assumed to be included in the load. Therefore, the modified droop method in this chapter is reformed to account for the cable resistances.

The main goal of this chapter is to achieve proper load current sharing while the parallel-connected converters have a mismatch of their parameters. Thus, the modified droop method based on cable resistance implementation for two parallel-connected boost converters is presented. A small-signal stability model for the two parallel-connected boost converters is developed based on the modified droop control to study the impact of cable resistance on the system transient stability. Although

the cable resistance lowers the efficiency of the system, the dynamic response of the two boost converters is improved. Furthermore, the proper choice of cable resistances can enhance dynamic response and load sharing of parallel converters. However, the current sharing between parallel converters cannot be achieved in the conventional droop method because of the mismatches in parameters of parallel-connected converters. To overcome the previously mentioned drawback, a control algorithm that supervises the modified droop method in order to achieve precise current sharing between parallel converters is proposed. The proposed control algorithm depends on the current sharing for each converter as a percentage of the total load current. The measured output current of each converter is compared to the total load current. The percentage results from the proposed algorithm are used locally to modify the nominal voltage of each converter. The algorithm ensures equal current sharing between parallel converters. MATLAB/Simulink is used to examine the effectiveness of the proposed algorithm, and the algorithm is verified by experimental results.

## 4.2 Modified Droop Control Method

The parameters of the two boost converters, which have 10% mismatch in the power rating, are given in Table 4.1.

Table 4. 1 The parameters for the two boost Converters

| Parameters | Converter I | Converter II |
|---|---|---|
| Switching frequency $\boldsymbol{f_s}$ | 25 KHz | 25 KHz |
| Inductance $\boldsymbol{L}$ | 9.592 mH | 8.72 mH |
| Capacitance $\boldsymbol{C}$ | 214.4 µF | 235.8 µF |
| Power $\boldsymbol{P}$ | 240 W | 264 W |

The SISO Tool in MATLAB is used for tuning the PI controller [54]. The gains for the voltage and current PI controllers are $Kp_v = 0.002604$, $K_{Iv} = 16.275$, $Kp_i = 0.04387$, and $K_{Ii} =$

11.251 respectively. The schematic diagram of the two parallel DC-DC converters is shown in Figure 4.1. The two converters are connected to two isolated DC sources 1 and DC source 2. They are connected to the DC load through cable resistances $R_{c1}$ and $R_{c2}$.

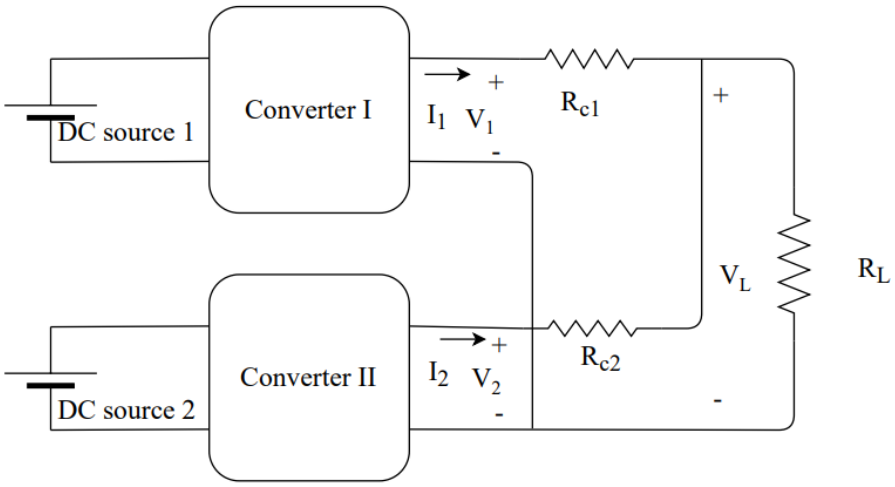



Figure 4. 1 Parallel-connected converter supplied from different sources

Figure 4.2 show the proposed modified load regulation characteristics for the modified droop including cable resistance implementation. The proposed load regulation characteristic considers the cable resistance as part of the droop gain for each converter [61].

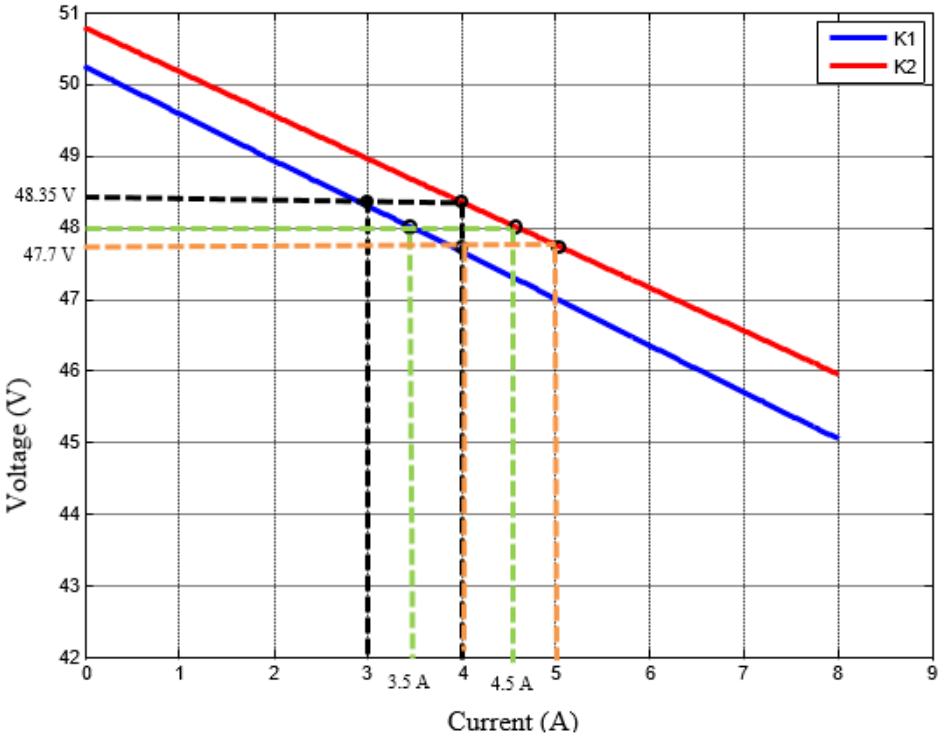



Figure 4. 2 Load regulation characteristic for converter I and II with $K_2$>$K_1$

Based on Equation (3.1), the output voltage $V_L$ at the common DC bus for each converter including the cable resistance is given by

$$V_L = V_{1NL} - (K_1 + R_{c1}) * I_1 \tag{4.1}$$

$$V_L = V_{2NL} - (K_2 + R_{c2}) * I_2 \tag{4.2}$$

Where $V_{1NL}$, and $V_{2NL}$ are the no-load output voltage of converter I and converter II, respectively. Similarly, $I_1$, and $I_2$ are the output currents of converter I and converter II, respectively. Equations (4.1) and (4.2) consider the cable resistances in the load regulation characteristics. The output voltage can be written as a function of the load resistance and the converter currents current as

$$V_L = R_L * (I_1 + I_2) \tag{4.3}$$

Equations (4.1) and (4.2) can be rewritten by substituting Equation (4.3) into Equations (4.1) and (4.2) as

$$R_L * (I_1 + I_2) = V_{1NL} - (K_1 + R_{c1}) * I_1 \tag{4.4}$$

$$R_L * (I_1 + I_2) = V_{2NL} - (K_2 + R_{c2}) * I_2 \tag{4.5}$$

Equations (4.4) and (4.5) can be rearranged and written as

$$(R_L + R_{c1} + K_1) * I_1 + R_L * I_2 = V_{1NL} \tag{4.6}$$

$$R_L * I_1 + (R_L + R_{c2} + K_2) * I_2 = V_{2NL} \tag{4.7}$$

By solving the linear Equations (4.6) and (4.7), the output currents $I_1$ and $I_2$ are obtained as

$$I_1 = \frac{{}^{V_{2NL}}/_{R_L} - ({}^{V_{1NL}}/_{{R_L}^2}) * (K_2 + R_{c2} + R_L)}{1 - ({}^{1}/_{{R_L}^2}) * (K_1 + R_{c1} + R_L) * (K_2 + R_{c2} + R_L)} \tag{4.8}$$

$$I_2 = \frac{{}^{V_{1NL}}/_{R_L} - ({}^{V_{2NL}}/_{{R_L}^2}) * (K_1 + R_{c1} + R_L)}{1 - ({}^{1}/_{{R_L}^2}) * (K_1 + R_{c1} + R_L) * (K_2 + R_{c2} + R_L)} \tag{4.9}$$

The value of the load resistance ($R_L$) in Equations (4.8) and (4.9) can be predicted based on the actual measurements of the common DC bus voltage $V_o$ and the total load current. Therefore, the load sharing current can be obtained by using Equations (4.8) and (4.9). Finally, the setpoint for the local controllers can be determined by using Equations (4.1) and (4.2).

Figure 4.3 shows a schematic diagram of $n$ converters connected in parallel, which are used to generalize the concept of the modified droop control method.

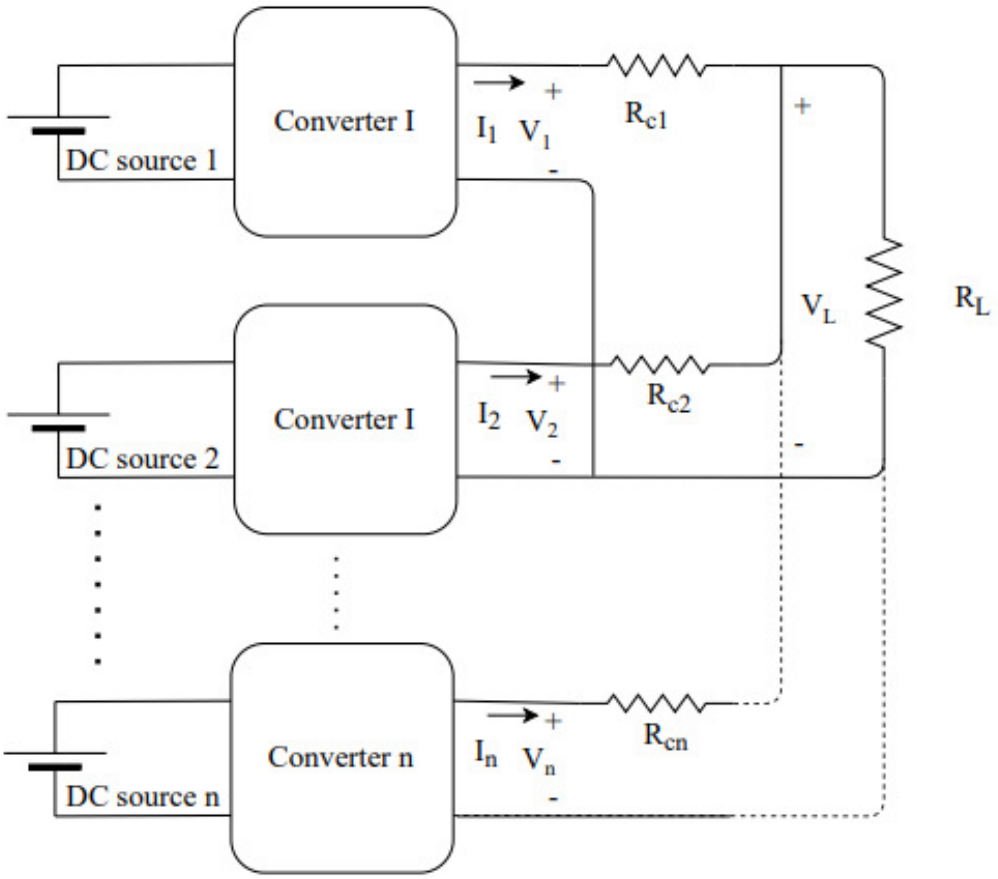



Figure 4. 3 $n$ parallel converters connected to DC load through different values of cable resistances

The load regulation characteristics of $n$ converters connected in parallel, considering the cable resistance, is shown in Figure 4.4.

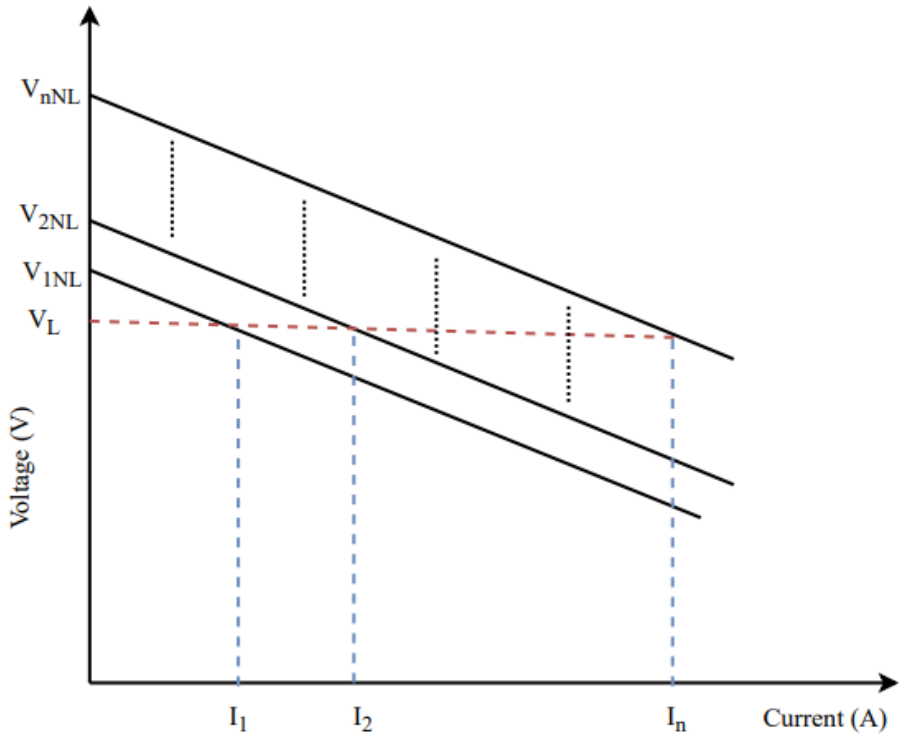



Figure 4. 4 Load regulation characteristics for $n$ plallel converters taking into account the cable resistances

For the $n$ parallel-connected converters, the output voltage at the common DC bus is given by

$$V_L = R_L * (I_1 + I_2 + \cdots + I_n) \tag{4.10}$$

Another expression for the output voltage at the common DC bus can be obtained as a function of output current for $n$ parallel-connected converters as

$$\begin{aligned} V_L &= V_{1NL} - (K_1 + R_{c1}) * I_1 \\ V_L &= V_{2NL} - (K_2 + R_{c2}) * I_2 \\ &\vdots \\ V_L &= V_{nNL} - (K_n + R_{cn}) * I_n \end{aligned} \tag{4.11}$$

By substituting (4.10) into (4.11), a set of $n$ linear equations for $n$ parallel-connected converters can be written in the form of an $n * n$ square matrix as

$$RK_{coefficeint} * \mathrm{I} = V_{NL} \tag{4.12}$$

Where $RK_{coefficeint}$ parameters are the droop gains for $n$ parallel-connected converters, the series cable resistances, and the load resistance, and it is given by:

$$RK_{coefficeint} = \begin{bmatrix} (K_1 + R_{c1} + R_L) & R_L & \dots & R_L \\ R_L & (K_2 + R_{c2} + R_L) & \cdots & R_L \\ \vdots & \vdots & \ddots & \vdots \\ R_L & R_L & \dots (K_n + R_{cn} + R_L) & \end{bmatrix} \tag{4.13}$$

The matrix $I$ is a matrix of $n * 1$, which represents load sharing currents for $n$ parallel-connected converters, and it can be written as:

$$I = \begin{bmatrix} I_1 \\ I_2 \\ \vdots \\ I_{\mathrm{n}} \end{bmatrix} \tag{4.14}$$

The matrix $V_{NL}$ is a matrix of $n * 1$, which consists of the no-load voltage for each of the $n$ parallel-connected converters, and it is given by:

$$V_{NL} = \begin{bmatrix} V_{1NL} \\ V_{2NL} \\ \vdots \\ V_{\mathrm{n}NL} \end{bmatrix} \tag{4.15}$$

The total load resistance $R_L$ is determined by the voltage and total current measurements at the common DC bus. The estimated load current sharing for n parallel-connected converters can be obtained by multiplying the matrix inverse of $RK_{coefficeint}$ and the no-load matrix $V_{NL}$. Estimating the voltage drop across the cable resistance is the next step. Finally, the reference voltage for each converter of the n parallel-connected converters can be obtained to provide the estimated load current sharing from each converter. The block diagram for the simulated case of two parallel-connected boost converters is shown in Figure 4.5. The figure indicates the steps for calculating the voltage set point for each converter. The step calculation is based on the modified

droop method. The voltage setpoint is updated for each converter by implementing the following steps:

- Measure the common DC bus voltage $V_L$ and the total load current $I_L$.
- Determine the load resistance as:

$$R_L = {V_L}/{I_L} \tag{4.16}$$

- Obtain the load current sharing for each converter.
  - $I_1$ is calculated based on (4.9) for converter I.
  - $I_2$ is calculated based on (4.10) for converter II.
- The theoretical values of $V_{out1}$ and $V_{out2}$ are calculated based on (4.1) and (4.2) for converter I and II, respectively.
- The voltage setpoint for each converter is calculated based on the voltage drop across the cable resistance for each converter. The voltage setpoint is also calculated with respect to the reference voltage as:

$$\Delta V_1 = V_{ref} - (V_1 + I_1 * R_{c1}) \tag{4.17}$$

$$\Delta V_2 = V_{ref} - (V_2 + I_2 * R_{c2}) \tag{4.18}$$

Where $V_{ref}$ is the rated value of the bus voltage. The reference voltage in the simulated case is equal to 48 V. The reference voltage is adjusted for converter I and converter II, as shown in Figure 4.5.

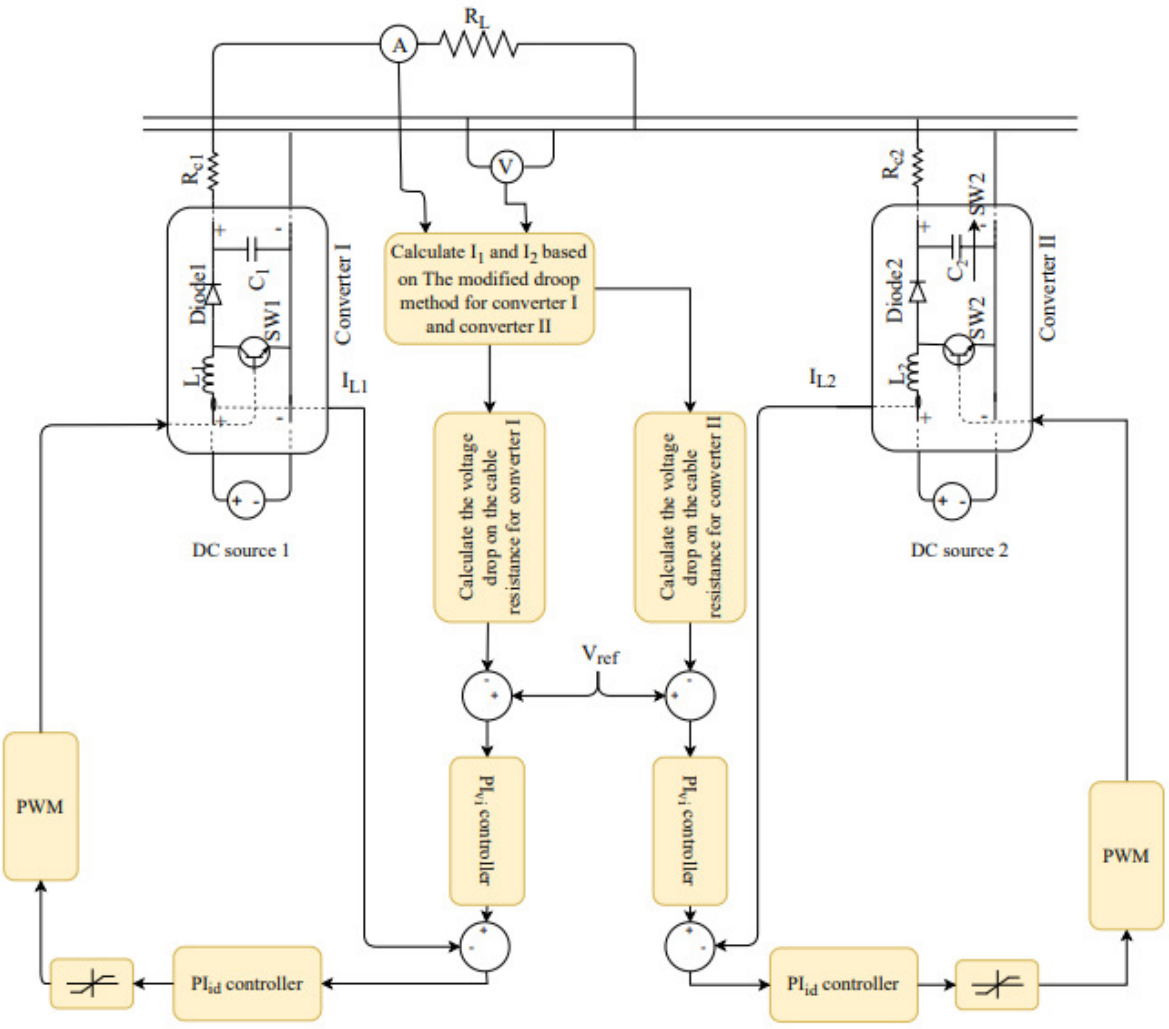
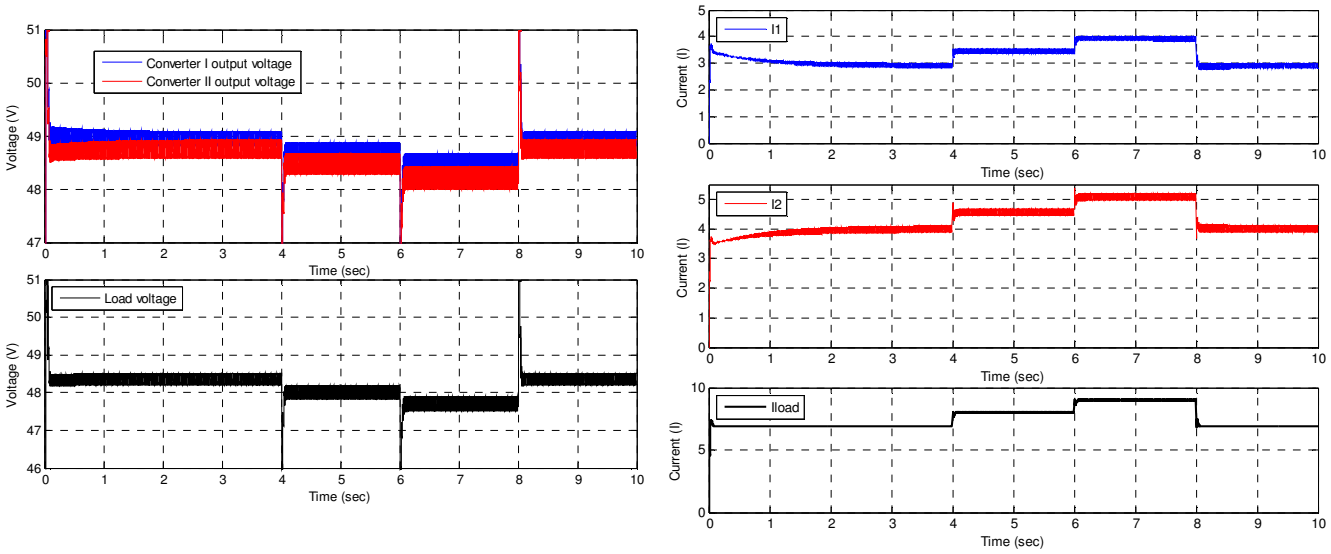



Figure 4. 5 Block diagram of the two parallel converters showing their control loops

The block diagram shown in Figure 4.5 is simulated in MATLAB/Simulink environment. Based on the analytical modified droop method with cable resistance implementation, the output voltage for each converter is adjusted individually. For various load conditions, the reference voltage for each converter is updated locally to ensure an equal common DC voltage. Figure 4.6 (a) and (b) show the waveforms for the output voltage and current for both converters, the common DC bus voltage, and the total load current. The output waveforms indicate step changes in the load condition at 4, 6, and 8 seconds.




(a) Output voltages (b) Output currents

Figure 4. 6 Output voltage and current waveforms at each converter and the common DC bus

The output voltage at the common DC bus is regulated synchronously when a step-change in the load is applied at 4 seconds, 6 seconds, and 8 seconds, as shown in Figure 4.6 (a). The load current sharing for each converter is determined according to the modified droop method, which is used to regulate the output voltage for each converter individually. Initially, the output voltages for converter I and converter II are 48.9 V and 48.75 V, respectively. The voltage values correspond to load current sharing of 3 A and 4 A for converter I and II, respectively. The proposed method ensures a common DC bus voltage of 48.35 V. These results are identical to Figure 4.2 and calculated based on the use of the modified droop method. Similarly, the voltage setpoints for converter I and converter II are reduced from 48.35 V to 48 V, respectively, when an increase in the load is applied at 3 seconds. The load current sharing becomes 3.5 A and 4.5 A for converter I and converter II, respectively. The setpoint values are the estimated values based on the measured voltage and current at the common DC. Thus, the common DC bus voltage is synchronized for both converters when the load is changed. In the same way, the setpoint voltage is regulated for

each converter using the modified droop method when the load is increased at 6 seconds. Thus, the load current sharing becomes 4 A and 5 A for converter I and II, respectively. The output voltages for converter I and converter II are 48.5 V and 48.2 V, respectively. These values for reference voltages ensures an equal voltage of 47.5 V at the common DC bus.

## 4.3 The Effect of Cable Resistance on Stability of the Modified Droop Method

A state-space averaging technique is developed and used to study the effect of cable resistance on the stability of the parallel-connected converter system. Figure 4.7 shows the basic diagram of the two parallel-connected converters, which are connected to a resistive load through a cable resistance.

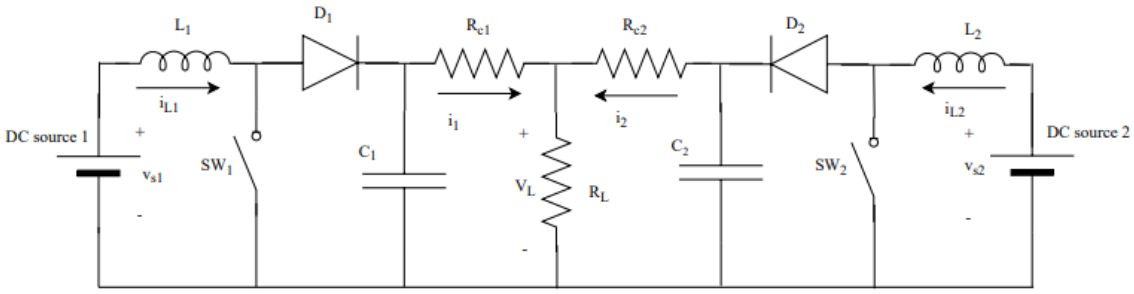



Figure 4. 7 Circuit diagram of two parallel-connected boost converters

From Figure 4.7, $i_{Lx}$ indicates the input current of the $x^{th}$ power supply, $i_x$ indicates the contribution current of the $x^{th}$ converter, $R_{cx}$ indicates the cable resistance between the $x^{th}$ boost converter and the load, $R_L$ represents the resistive load. The circuit diagram in Figure 4.7 can be simplified by using Wye-Delta transformation, as shown in Figure 4.8.

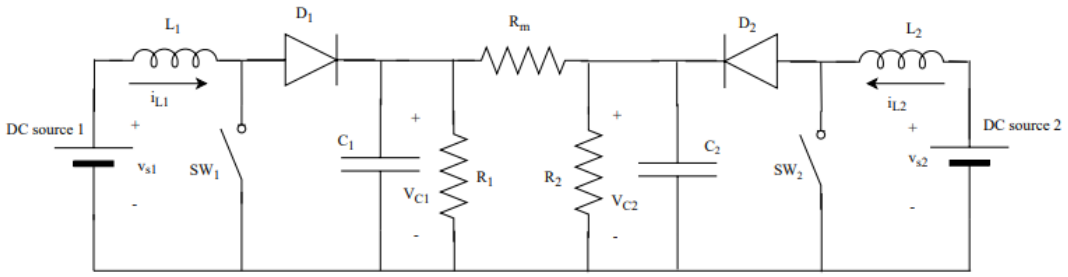



Figure 4. 8 The equivalent circuit using way-delta transformation of two parallel-connected boost converters

$R_m$, $R_1$, and $R_2$ in Figure 4.8 are given by

$$R_m = \frac{R_{c1}*R_{c2}+R_{c1}*R_L+R_{c2}*R_L}{R_L} \tag{4.19}$$

$$R_1 = \frac{R_{c1}*R_{c2}+R_{c1}*R_L+R_{c2}*R_L}{R_{c2}} \tag{4.20}$$

$$R_2 = \frac{R_{c1}*R_{c2}+R_{c1}*R_L+R_{c2}*R_L}{R_{c1}} \tag{4.21}$$

The time-averaged model of the two parallel-connected converters system can be described by neglecting the switching transient and using the volt-second principle, and it is given by:

$$\frac{di_{L1}}{dt} = \frac{1}{L_1}V_{s1} - \frac{(1-d_1)}{L_1}V_{c1} \tag{4.22}$$

$$\frac{dv_{c1}}{dt} = \frac{(1-d_1)}{C_1}i_{L1} - \left(\frac{1}{R_1C_1} + \frac{1}{R_mC_1}\right)V_{c1} + \frac{1}{R_mC_1}V_{c2} \tag{4.23}$$

$$\frac{di_{L2}}{dt} = \frac{1}{L_2}V_{s2} - \frac{(1-d_2)}{L_2}V_{c2} \tag{4.24}$$

$$\frac{dv_{c2}}{dt} = \frac{(1-d_2)}{C_2}i_{L2} - \left(\frac{1}{R_2C_2} + \frac{1}{R_mC_2}\right)V_{c2} + \frac{1}{R_mC_2}V_{c1} \tag{4.25}$$

A derived small-signal model for the two parallel-connected boost converters is used to investigate

the effect of cable resistance. The small-signal model for the two parallel-connected boost converters can be obtained by perturbing and linearizing the time-average model around the steady-state operating point. Therefore, the small-signal model for the two parallel-connected boost converters system can be written in the matrix form as

$$\dot{\tilde{x}} = A\tilde{x} + B\tilde{u} + F\tilde{v} \tag{4.26}$$

$$\tilde{y} = C\tilde{x} \tag{4.27}$$

Where $\tilde{x} = [\tilde{\imath}_{L1} \quad \tilde{\imath}_{L2} \quad \tilde{v}_{c1} \quad \tilde{v}_{c2}]^T$, $\tilde{u} = [\tilde{d}_1 \quad \tilde{d}_2]^T$

$\tilde{v} = [\tilde{v}_{s1} \quad \tilde{v}_{s2}]^T$, $\tilde{y} = [\tilde{\imath}_{L1} \quad \tilde{\imath}_{L2} \quad \tilde{v}_{c1} \quad \tilde{v}_{c2}]^T$

$$A = \begin{bmatrix} 0 & 0 & -\frac{(1-D_1)}{L_1} & 0 \\ 0 & 0 & 0 & -\frac{(1-D_2)}{L_2} \\ \frac{(1-D_1)}{C_1} & 0 & -\left(\frac{1}{R_1C_1} + \frac{1}{R_mC_1}\right) & \frac{1}{R_mC_1} \\ 0 & \frac{(1-D_2)}{C_2} & \frac{1}{R_mC_2} & -\left(\frac{1}{R_2C_2} + \frac{1}{R_mC_2}\right) \end{bmatrix}, \quad B = \begin{bmatrix} \frac{V_{c1}}{L_1} & 0 \\ 0 & \frac{V_{c2}}{L_2} \\ -\frac{I_{L1}}{C_1} & 0 \\ 0 & -\frac{I_{L2}}{C_2} \end{bmatrix}, \quad F = \begin{bmatrix} \frac{1}{L_1} & 0 \\ 0 & \frac{1}{L_2} \\ 0 & 0 \\ 0 & 0 \end{bmatrix},$$

$C = I$

A linearized small-signal model, which accounts for the cable resistance, is derived in the previous steps. The model identifies the state variables, which are the variations in power source output current and the output voltage of each converter. The control input is the variation in the duty cycle, and external disturbance is the variation in the DC power source voltage. Therefore, the entire system of two parallel-connected converters can be defined as a multiple-input-multiple-output system, as shown in Figure 4.9.

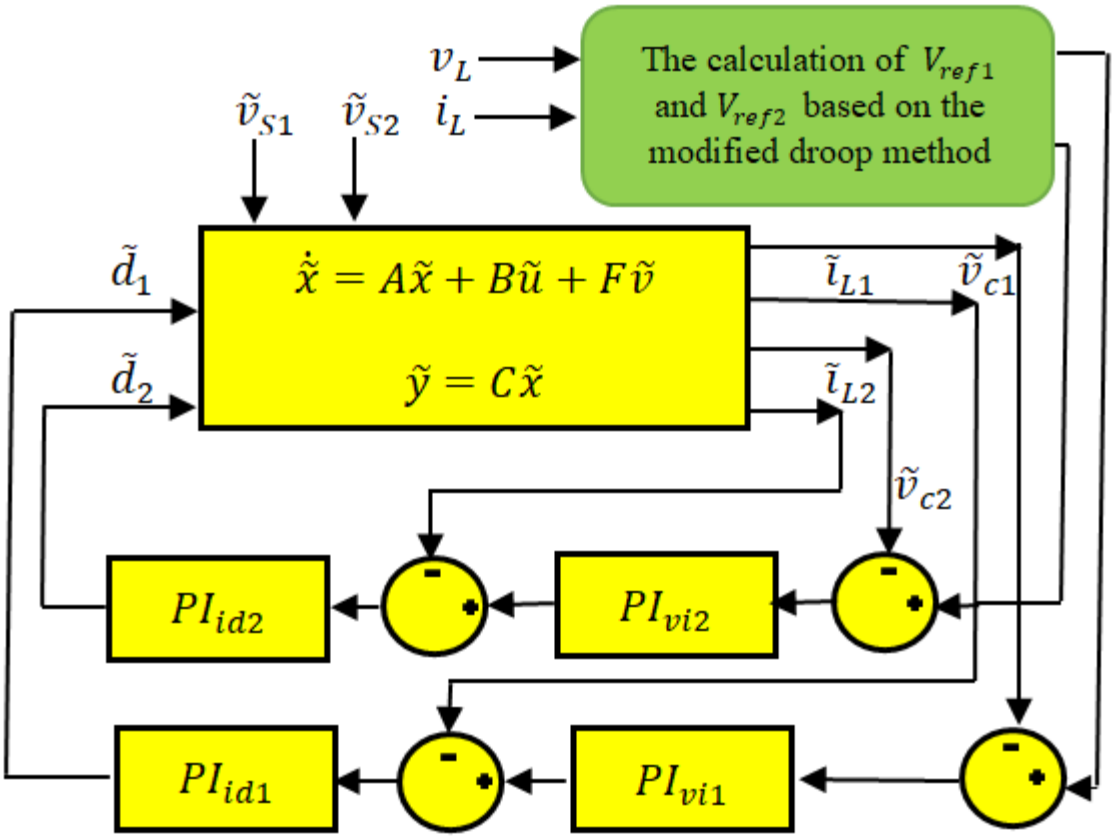


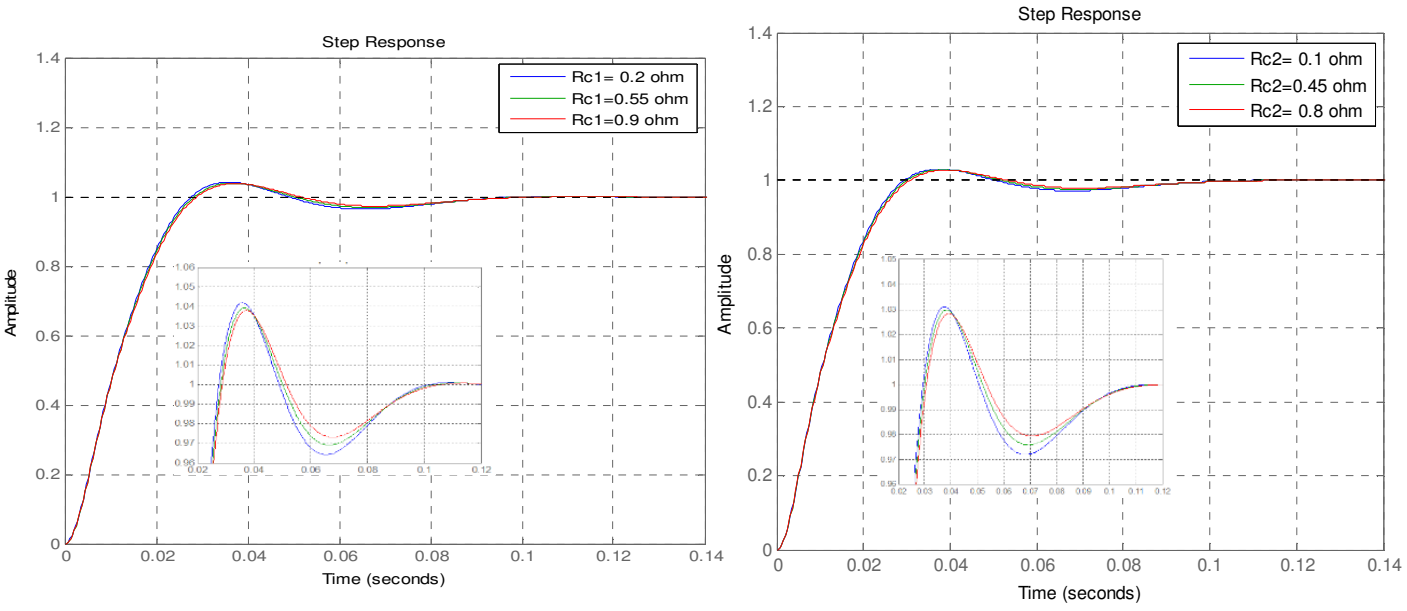

Figure 4. 9 Block diagram of the model representing the dynamics of the two parallel-connected boost converters system

Different values of cable resistances are used to study their effect on the dynamic response of the parallel-connected converters. Firstly, the step response of the system model is used to evaluate the impact of different cable resistances. The operating point for the steady-state is determined to observe the step response for the two boost converters. The steady-state operating points are given in Table 4.2.

Table 4. 2 Steady-State Operating Points

| $I_L$ (A) | $I_1$ (A) | $I_2$ (A) | $V_{C1}$(V) | $V_{C2}$ (V) | $D_1$% | $D_2$% |
|---|---|---|---|---|---|---|
| 8.13 | 3.5 | 4.63 | 48.67 | 48.44 | 50.69 | 50.45 |

The transfer functions $\tilde{v}_{c1}$ to $\tilde{d}_1$ and $\tilde{v}_{c2}$ to $\tilde{d}_2$ are determined based on the small-signal model of the interconnected two parallel converters, as given in Appendix B. The closed-loop transfer function, along with the PI controller parameters, is obtained. Therefore, the step response for the closed-loop transfer functions $\tilde{v}_{c1}$ to $\tilde{d}_1$ and $\tilde{v}_{c2}$ to $\tilde{d}_2$ is shown in Figure 4.10 (a) and (b), respectively.




(a) (b)

Figure 4. 10 Step response for $\tilde{v}_{c1}$ to $\tilde{d}_1$ and for $\tilde{v}_{c2}$ to $\tilde{d}_2$: (a) Step response for $\tilde{v}_{c1}$ to $\tilde{d}_1$ with different values of $Rc_1$ and (b) Step response for $\tilde{v}_{c2}$ to $\tilde{d}_2$ with different values of $Rc_2$

From Figure 4.10 (a) and (b), when the cable resistances that connect converter I and converter II to the common DC bus are increased, the damping ratio increases, and the overshoot decreases. Therefore, the dynamic response of the two parallel-connected converter system is enhanced.

The trainset analysis is used to investigate the effect of increasing the cable resistance. The two parallel-connected boost converters shown in Figure 4.7 are simulated in MATLAB. Two values of the cable resistances, which were used in the state space averaging technique model, are investigated. The first case is simulated by using cable resistances of 0.2 Ω and 0.1 Ω for $R_{c1}$ and

$R_{c2}$ respectively. The results of the first case are compared with the transient response of the second case, which uses different cable resistance of 0.9 Ω and 0.8 Ω for $R_{c1}$ and $R_{c2}$ respectively. Figure 4.11 shows the voltage waveforms of the transient response for the simulated two cases.

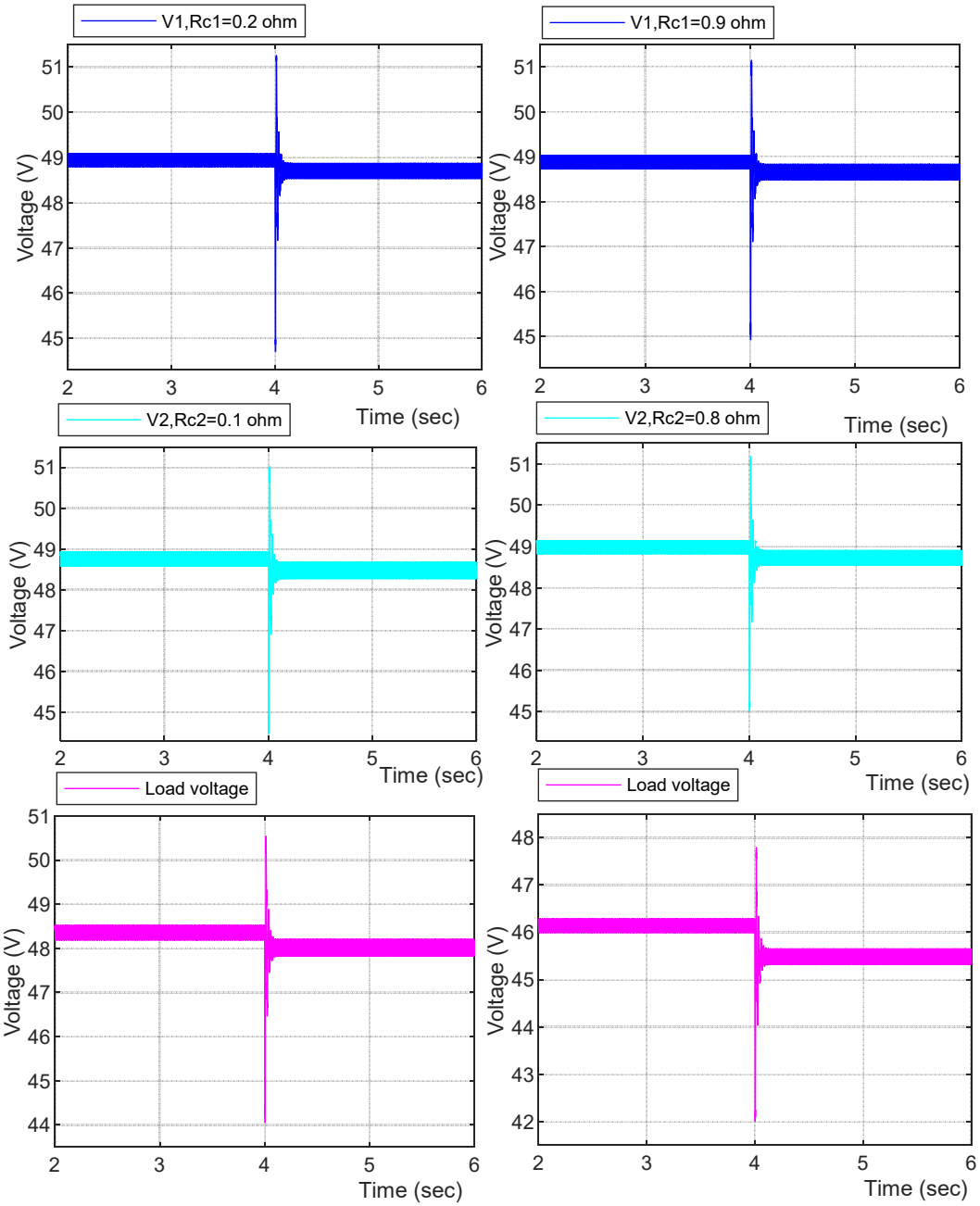



Figure 4. 11 Output voltage waveforms of the transient response for a step increase in the load

Figure 4.11 shows the transient response of the output voltage waveforms. The undershoot of the output voltage is lowered for both converters when the cable resistances are increased. The improvement of transient response is due to the increase of the damping ratio in the system parameters. Furthermore, the ripple in the output current waveform, shown in Figure 4.12, is lowered due to the increase in the cable resistance.

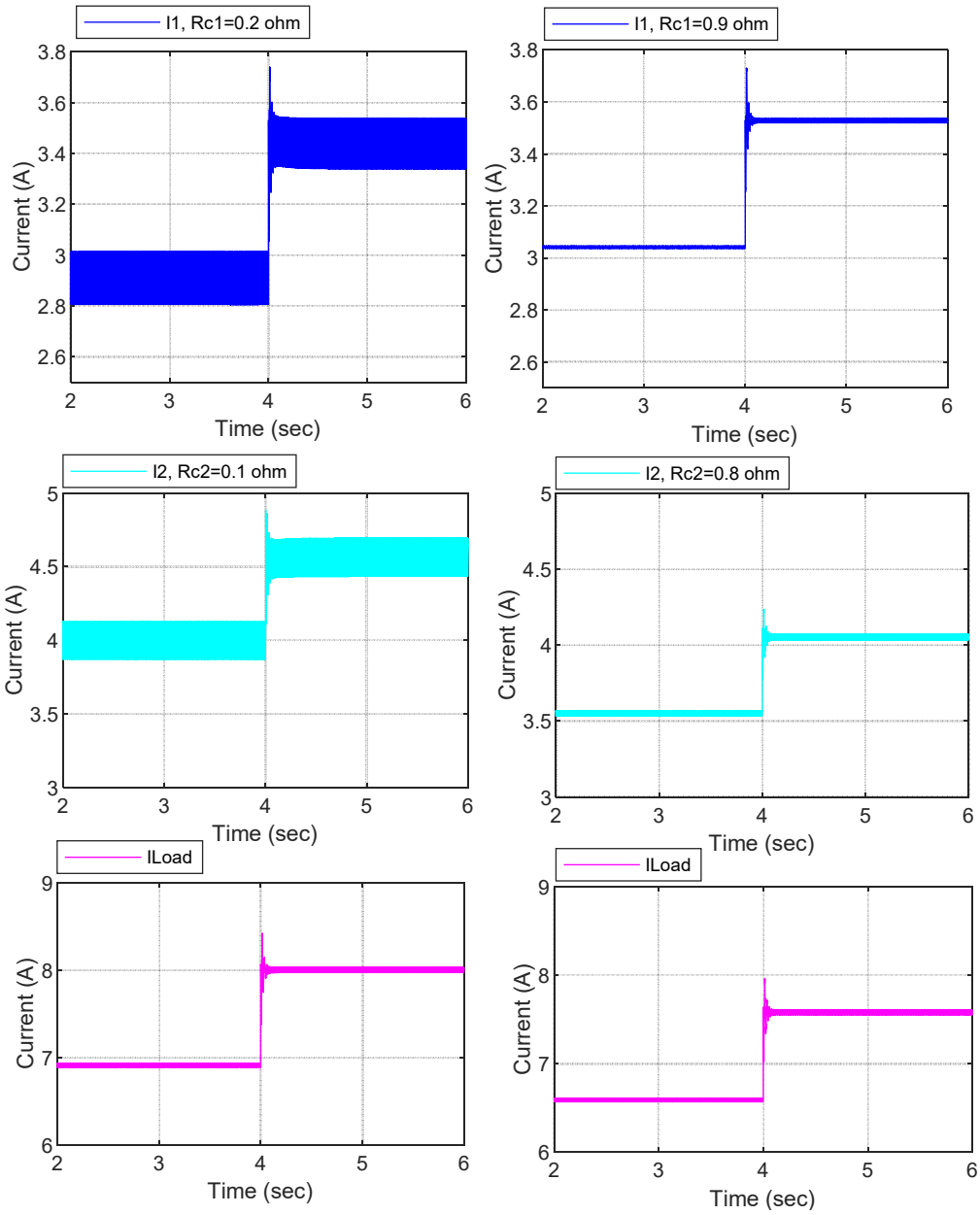



Figure 4. 12 Output current waveforms of the transient response for a step increase in the load

It can be observed that the ripple in the output current of converter I and II is decreased when the cable resistance is increased. Since both converters are controlled by the pulse width modulation, the switching ON and OFF causes an increase and decrease in the output current of each converter around the steady-state operating point. The increase is associated with charging and discharge of the output capacitor for each converter. However, when the cable resistance increases, the time constant of each of the converters increases resulting in a decrease in the ripple in the output current waveforms, as shown in Figure 4.12. Therefore, the transient response for the two parallel-connected converter system is improved by applying higher cable resistance. Although the dynamic response of the two parallel-connected converters is enhanced in the case of higher cable resistances, the degradation of voltage regulation is observed, as shown in Figure 4.11.

## 4.4 Control Algorithm for Equal Current Sharing between Parallel-connected Converters

The droop gains of the load regulation characteristics play an important role in the load current sharing between parallel-connected converters. These gains depend on the parameters of the converters, which are impossible to have the exact numerical characteristics due to manufacturing tolerance [62]. By considering the aforementioned limitation, the parameters of two boost converters in Table 4.1 are implemented in MATALB/Simulink environment. The mismatch in the parameters can be observed in Table 4.1. The percentage of the mismatch is approximately 10% and 1% for the inductor and the capacitance, respectively. The consequences of these mismatches lead to unequal load current sharing between parallel converters. To illustrate this concept, Figure 4.13 shows the two parallel-connected converters, which are connected through cable resistances ($R_{c1}$,$R_{c2}$) to a resistive load. The load current sharing of the two parallel

converters depends on the load regulation characteristics of the converters, which is shown in Figure 4.14.

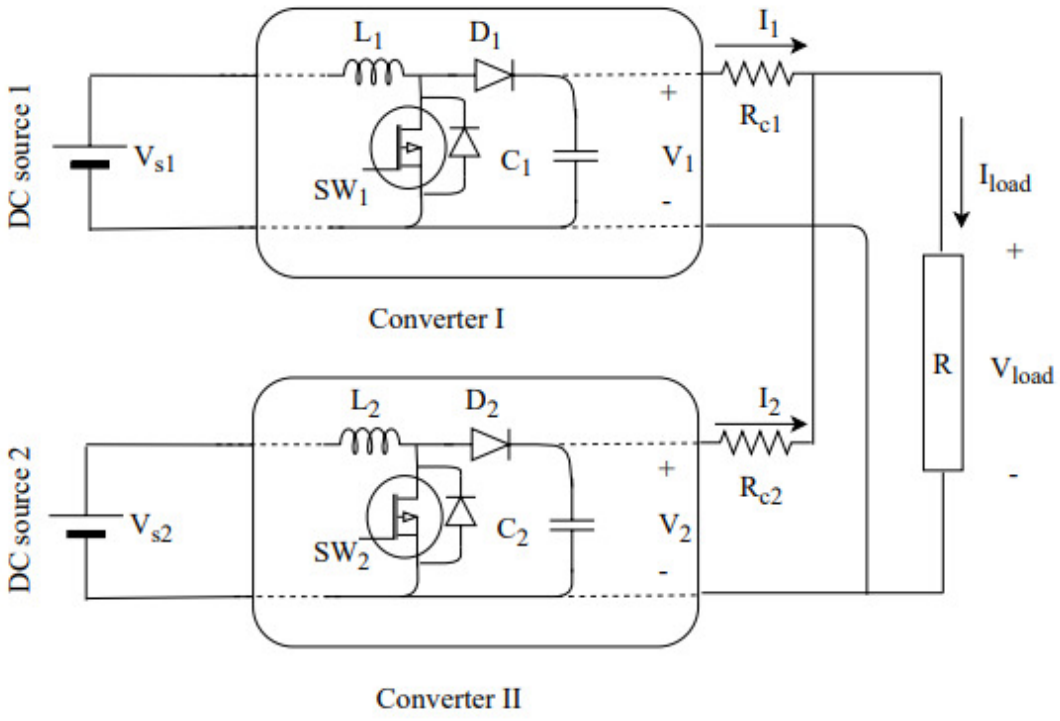



Figure 4. 13 Circuit diagram of the two parallel-connected boost converters to a resistive load through cable resistances

The droop gains for converter I and converter II are determined based on the parameters given in Table 4.1 [55,56]. They are considered as the slope of the load regulation characteristics of each converter, as shown in Figure 4.14. They are determined based on an approach, which is described in [54]. Based on that approach, the droop gain values for converter I and converter II are determined to be $K_1 = 0.4304$ and $K_2 = 0.3927$.

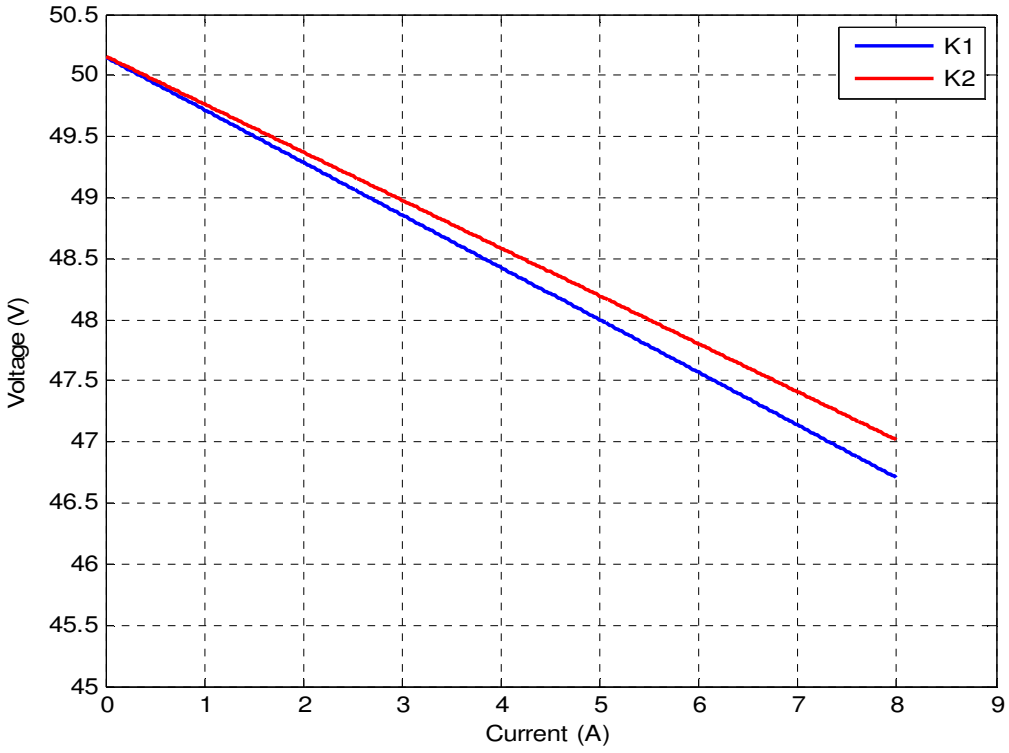



Figure 4. 14 Load regulation characteristic for converter I and II with $K_1$ $and$ $K_2$

From Figure 4.14, it can be observed that the mismatches in the parameters of the parallel-connected converters cause poor load current sharing for a specified load voltage. Figure 4.14 shows the load regulation for the parallel-connected converter with including a cable resistance of 0.1 Ω. Although both converters are connected to the resistive load through the same value of the cable resistance, the load current is not shared equally. Furthermore, considering the same loading condition, the cable resistances in Figure 4.14 affect the voltage regulation. The control algorithm proposed here modifies the output voltage for each converter to achieve precise load current sharing [63]. The flow chart of the proposed algorithm is shown in Figure 4.15. The voltage setpoint for the outer voltage loop is modified based on percentage of current sharing percentage (PCS) for each converter. The PCS for converter ($n$) is determined based on dividing the actual measurements of the output current of converter ($n$) by the total load current as

$$PCS_n = \frac{I_n}{I_{load}} * 100 \quad (4\text{-}28)$$

In the case of equal load current sharing, the PCS for each converter must be 50% of the load current. To illustrate, if converter I contributes to the total load current with a percentage of less than 50%, the setpoint for the outer voltage loop of converter I is increased by $\Delta V_{CA}$. On the other hand, if the PCS for converter I is higher than 50%, the reference voltage is decreased by $\Delta V_{CA}$ to achieve equal load current sharing.

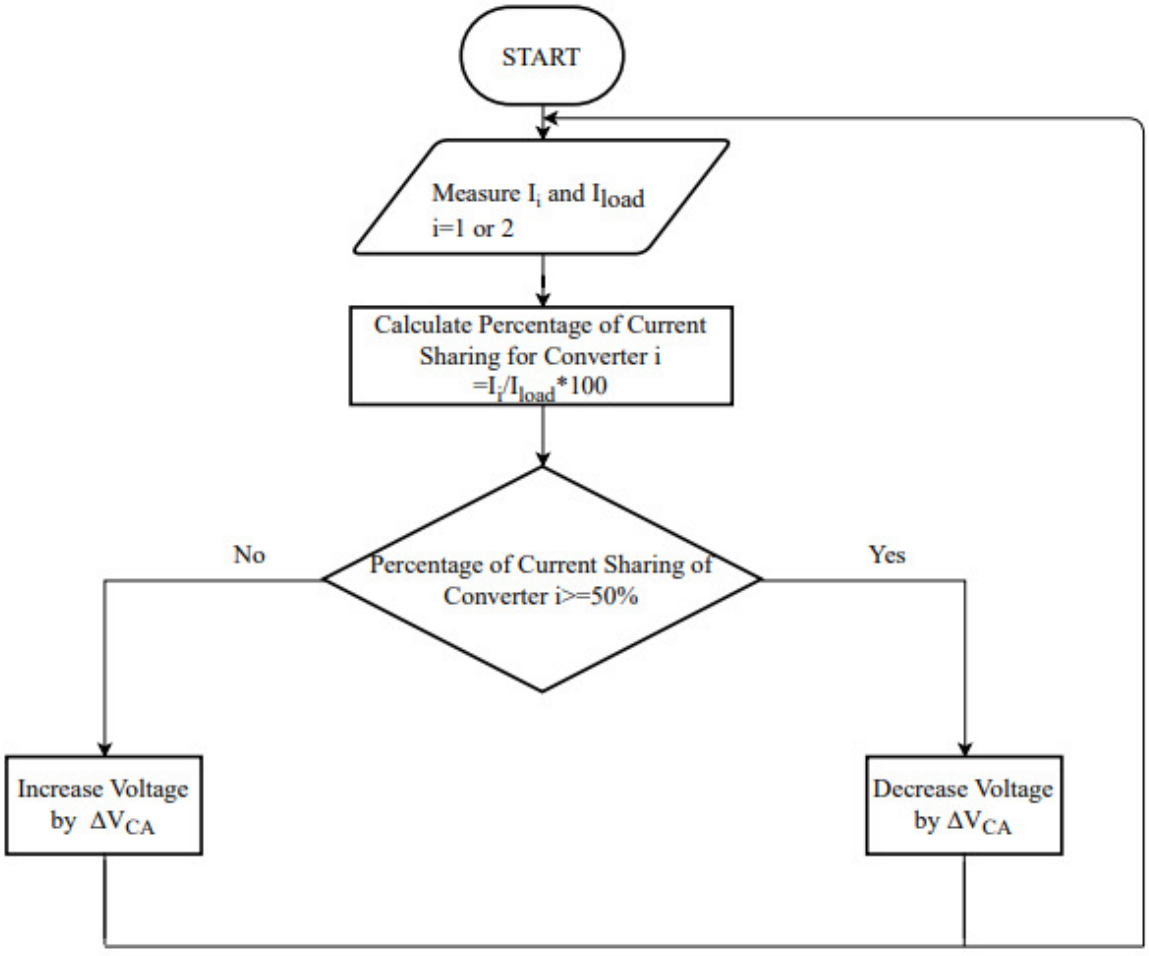



Figure 4. 15 Flow chart of the proposed algorithm

The precise load current sharing between parallel-connected converters is achieved with the implementation of the proposed algorithm. However, the proposed algorithm produces an oscillating output current for each converter around the operating point. The oscillation around the operating point, as shown in Figure 4.16, can be minimized by choosing a small value of $\Delta V_{CA}$. The droop gain of the load regulation characteristics of each converter also can reduce the oscillation in the output current. If the droop gain has high value (i.e, $K > K`$), the oscillation around the operating point can be minimized, as shown in Figure 4.16.

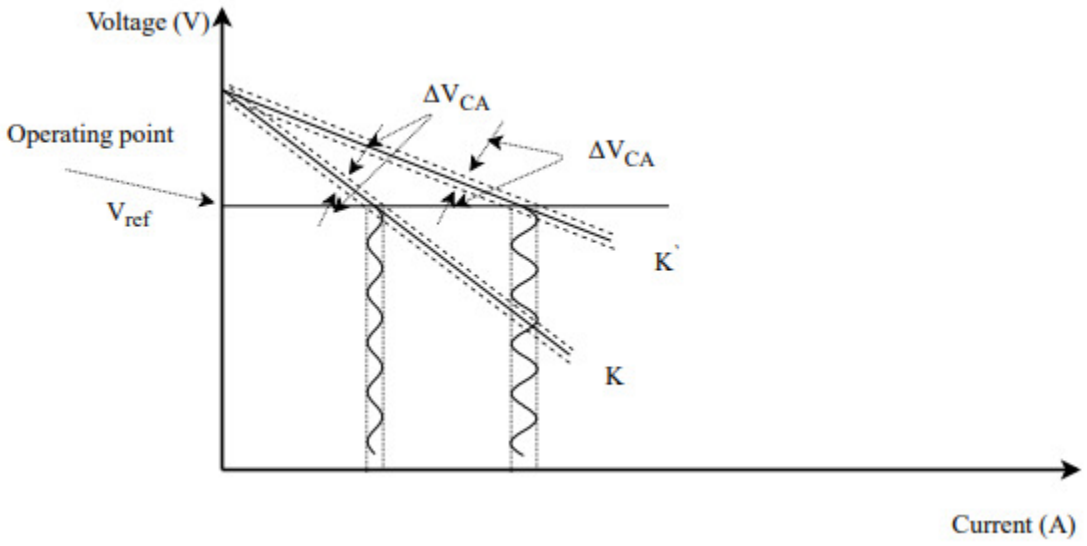



Figure 4. 16 Oscillatory current around the desired operating point for two droop gains with $K > K`$

Figure 4. 17 (a) shows the block diagram of the two parallel-connected converters along with the proposed algorithm.

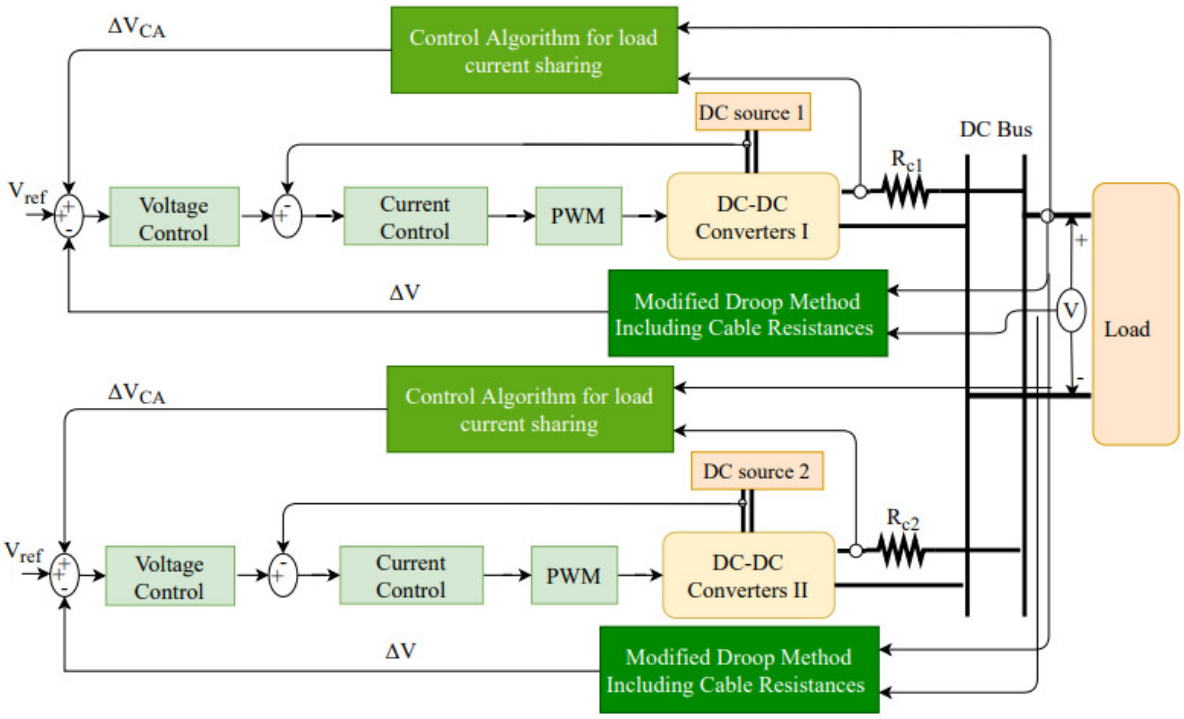



Figure 4. 17 Block diagram of the two parallel-connected converters with the proposed algorithm

## 4.5 Simulation Results

The two block diagrams in Figure 4.5 and Figure 4.17 are simulated in MATLAB to examine the performance of the proposed algorithm. The first case is associated with the modified droop with cable resistance implementation, as shown in the block diagram of Figure 4.5. The cable resistances have the same value of 0.1 Ω. They connect the output of each converter to the load. The load current sharing for step increase in the load is shown in Figure 4.18.

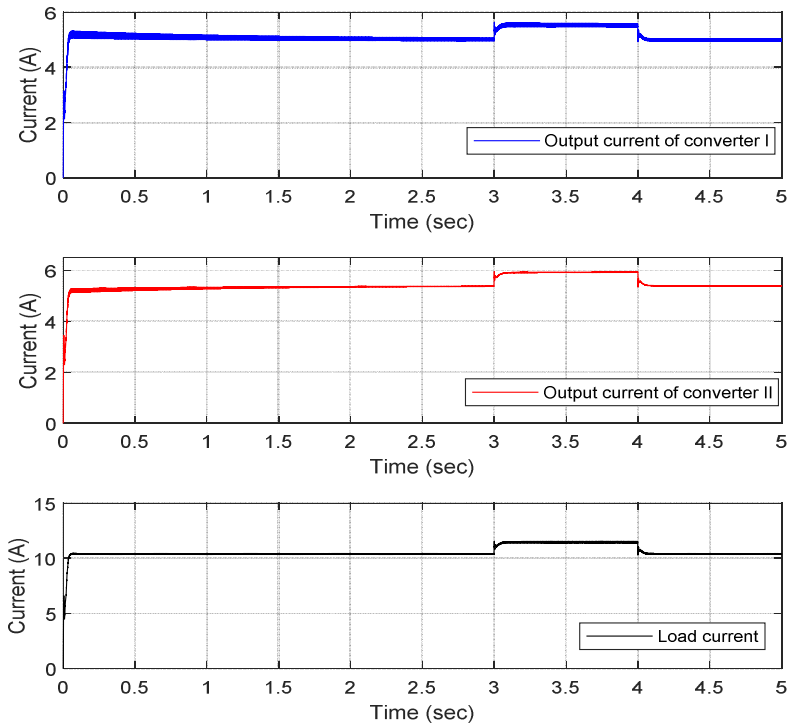



Figure 4. 18 Output waveforms of the converters' current and the load current

From Figure 4.18, the current sharing of converter I to the total load current is lower compared to the current sharing of converter II. Although the cable resistances are equal, the mismatches in parameters of the parallel-connected converter are the main cause of unequal current sharing. However, the second case is associated with the implementation of the proposed control algorithm, as shown in Figure 4.17. The output current for both converters and the load current is shown in Figure 4.19.

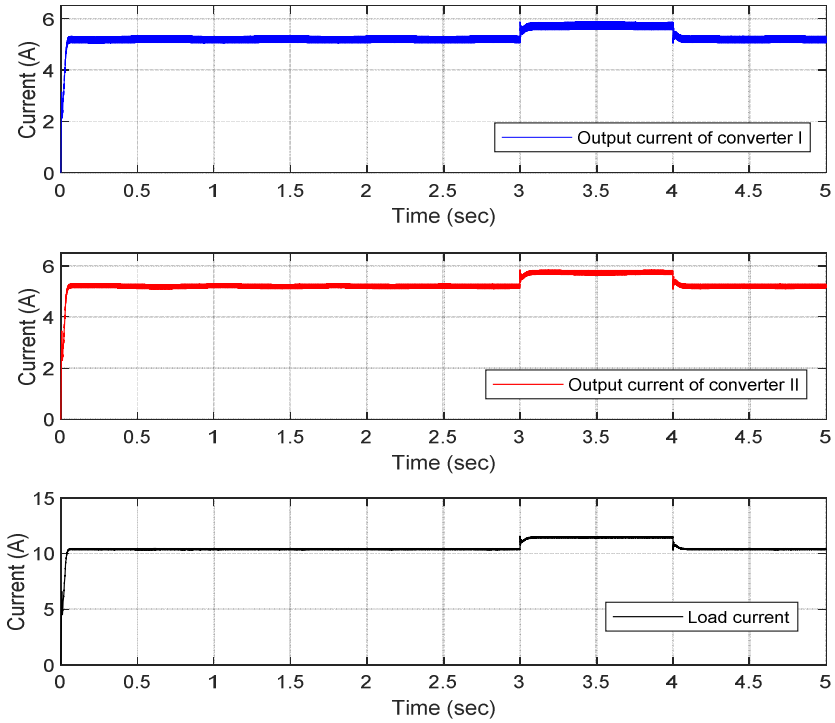



Figure 4. 19 output waveforms of both converters and the load current

Equal current sharing is achieved by the proposed control algorithm, as shown in Figure 4.19. The control algorithm modifies the nominal voltage for each converter. The adjusted voltage results in a precise load current sharing between the parallel converters. The percentage of current deviation for both cases is shown in Table 4.3. The current deviation percentage with the implementation of the control algorithm becomes zero compared to the modified droop method including cable resistance only.

Table 4. 3 Load current sharing for parallel-connected converters and the percentage of current deviation

| Case | Time | Converter I | Converter II | Load current | Percentage of current deviation % |
|---|---|---|---|---|---|
| Equal | 0-3 sec | 5.0 A | 5.4 A | 10.4 A | 3.9 % |
| Cable | 3-4 sec | 5.5 A | 5.9 A | 11.4 A | 3.5 % |
| Resistance | 4-5 sec | 5.0 A | 5.4 A | 10.4 A | 3.9 % |
| Control | 0-3 sec | 5.2 A | 5.2 A | 10.4 A | 0 % |
| Algorithm | 3-4 sec | 5.7 A | 5.7 A | 11.4 A | 0 % |
| | 4-5 sec | 5.2 A | 5.2 A | 10.4 A | 0 % |

As can be seen from Table 4.3, the proposed algorithm with the control loop overcome the issue of the mismatches in the parameters for the parallel converters.

Small-scale boost converters are used to accomplish the experimental part of the proposed algorithm. Firstly, the two parallel-connected boost converters are simulated in the MATLAB model, and then the results are validated experimentally. The parameters of the two boost converters are given in Table 4.4.

Table 4. 4 The parameters for the two boost converters

| **Parameters** | **Converter I** | **Converter II** |
|---|---|---|
| Switching frequency $\boldsymbol{f_s}$ | 25 KHz | 25 KHz |
| Inductance $\boldsymbol{L}$ | 12.49 mH | 12.75 mH |
| Capacitance $\boldsymbol{C}$ | 570 µF | 620 µF |
| Nominal Voltage $\boldsymbol{V}$ | 6-12 V | 6-12 V |

There are two simulated cases, namely, the modified droop method, as shown in Figure 4. 5 and the modified droop method with the proposed algorithm, as shown in Figure 4.17. In the first and second cases, the values of cable resistance are selected to have the same value. In this study, the main intention is to examine the performance of the proposed algorithm under a mismatch in parameters of the two parallel-connected boost converters. The selected cable resistances have

values of $R_{c1} = R_{c2} = 0.4\Omega$. Furthermore, the proposed algorithm is examined under a step increase in the load. The simulation of the two cases is performed under the same condition of a step increase in the load. The step increase in the load is applied at 2.5 seconds. Figure 4.20, and Figure 4.21 show the output waveforms of the current and the voltage for the modified droop method.

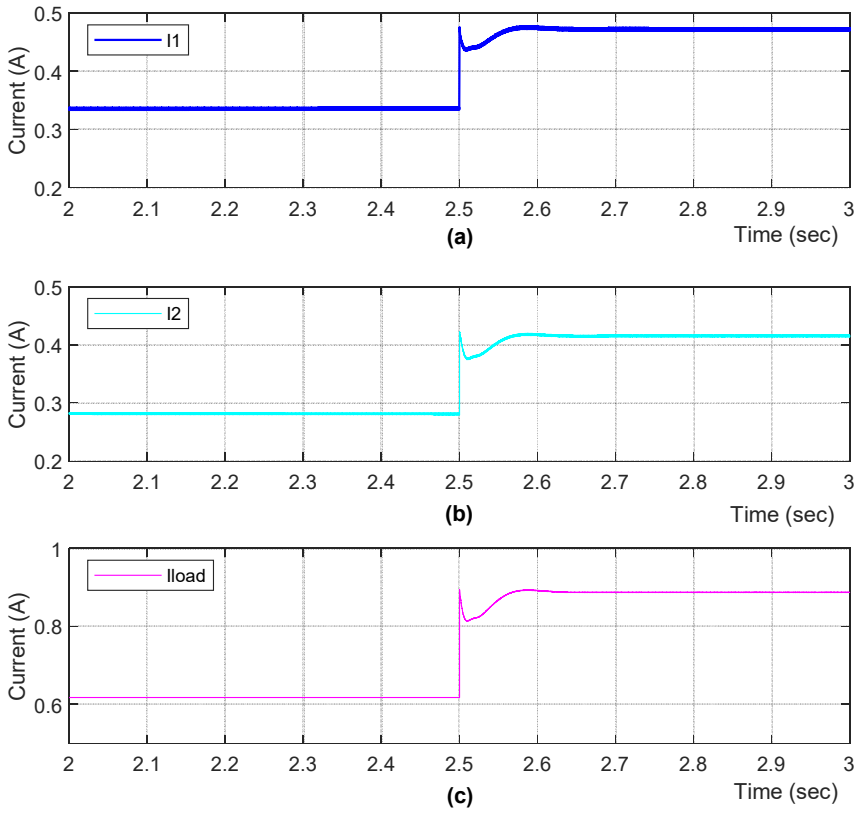



Figure 4. 20 Simulation results for an increase in the load. (a) Output current of converter I. (b) Output current of converter II. (c) Total load current.

Despite the same value of cable resistance, the mismatch in the parameters of the parallel-connected boost converter affects load current sharing, as shown in Figure 4.20. Converter I contributes a higher current to the load current compared to the current contribution of converter II. Before a step increase in the load, the load current sharing for converter I and converter II are

0.33 A and 0.28 A, respectively. The load current sharing for converter I and converter II increases to 0.47 A and 0.41 A, respectively, after a step increase of the load is applied at 2.5 seconds.

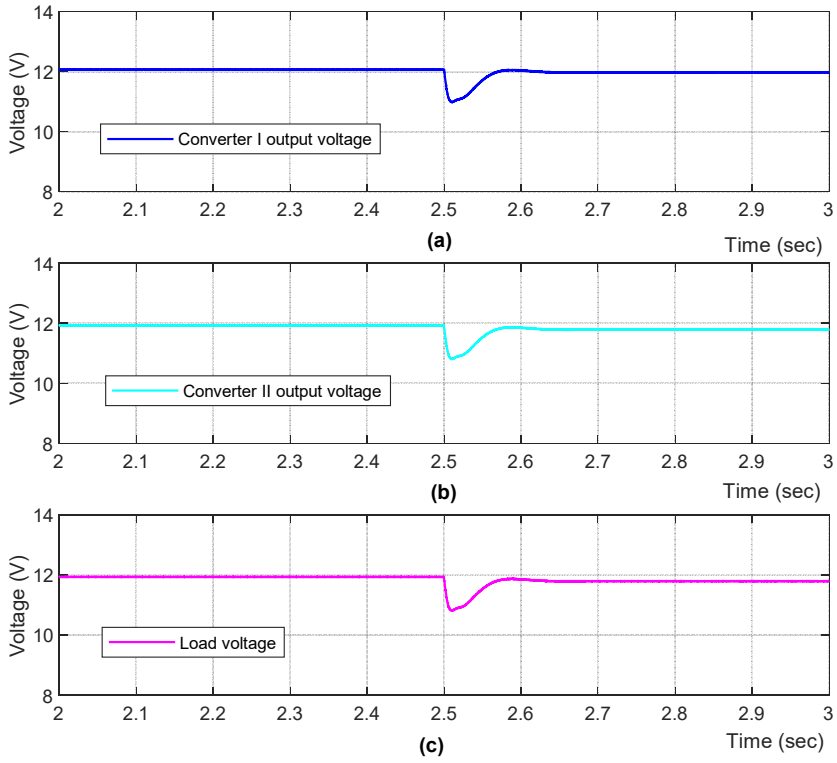



Figure 4. 21 Simulation results for an increase in the load. (a) The output voltage of converter I. (b) The output voltage of converter II. (c) The voltage at the common DC bus.

The load regulation characteristics for the parallel-connected boost converter determine the load current sharing and the voltage regulation, as shown in Figure 4.20, and Figure 4.21. The steady-state values of voltages and currents for a step increase in load, as well as the percentage deviation in current sharing for the first case, are given in Table 4.5.

Table 4. 5 Simulation results for the modified droop method.

| Time (sec) | $V_{out1}$ (V) | $V_{out2}$ (V) | $V_{load}$ (V) | $I_1$ (A) | $I_2$ (A) | $I_{load}$ (A) | $\Delta I$ % current sharing differences |
|---|---|---|---|---|---|---|---|
| 0-2.5 | 12.06 | 12.04 | 11.93 | 0.33 | 0.28 | 0.61 | 8.778 |
| 2.5-5 | 11.98 | 11.96 | 11.79 | 0.47 | 0.41 | 0.88 | 6.254 |

Based on the steady-state results shown in Table 4.5, The main observation is that the load current is not shared equally, and the percentage deviation in current sharing for different loading conditions is higher than 6%. However, with the same loading condition in the first case, the performance of the proposed algorithm shown in Figure 4.17 is also simulated, and its results of the load current sharing are shown in Figure 4.22.

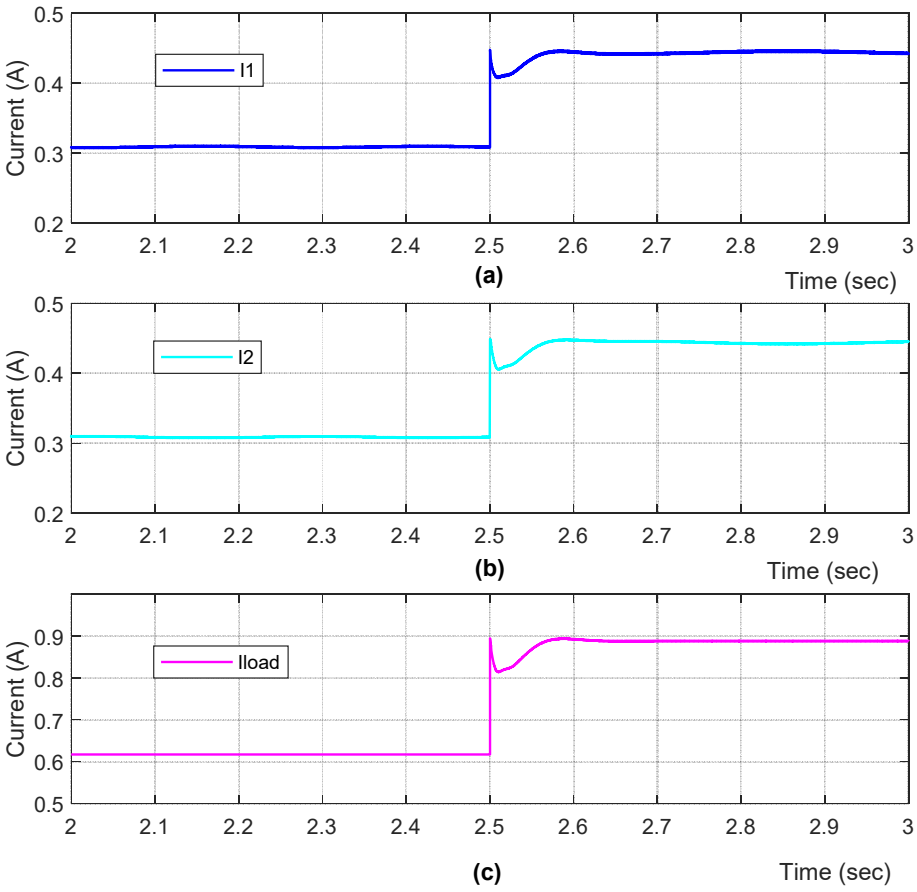



Figure 4. 22 Simulation results for the proposed algorithm with an increase in the load. (a) Output current of converter I. (b) Output current of converter II. (c) Total load current.

The improvement in the load current sharing of the proposed algorithm can be observed from Figure 4.22. Converter I and converter II contribute to the total load current with the same values of the current. The control algorithm modifies the reference voltage for each converter locally to

ensure a precise load current sharing between the parallel-connected converter. Thus, the load current sharing is 0.3085 before a step increase in the load is applied at 2. 5 seconds. Furthermore, the load current sharing is maintained while a step increase in the load is applied at 2.5 seconds. The regulated output voltage for each converter and the voltage at the common DC bus are shown in Figure 4.23.

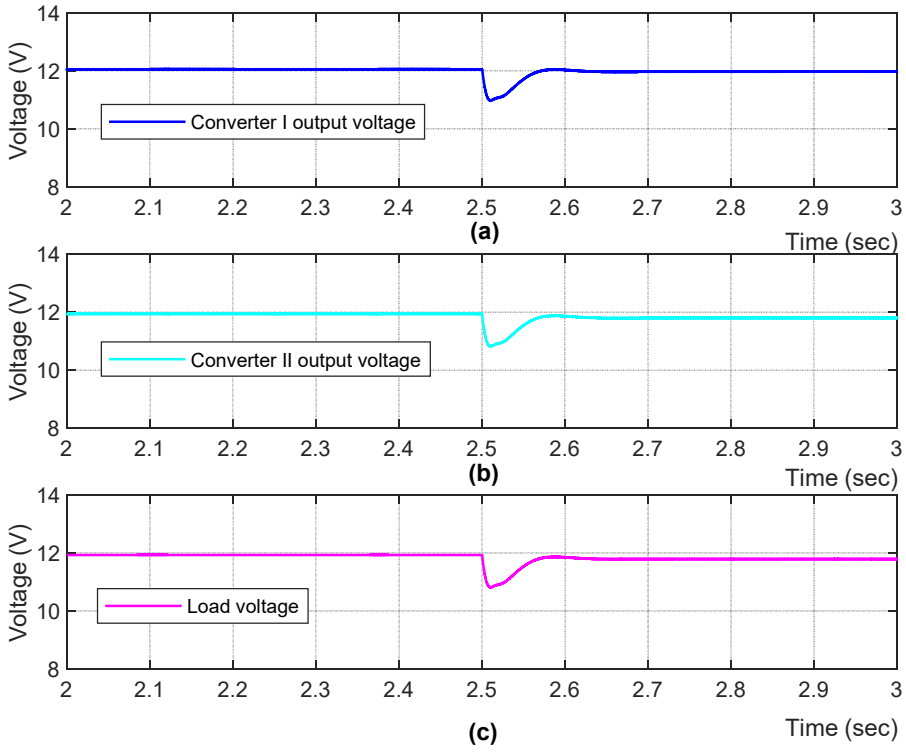



Figure 4. 23 Simulation results for the proposed algorithm with an increase in the load. (a) The output voltage of converter I. (b) The output voltage of converter II. (c) The voltage at the common DC bus.

The numerical steady-state values of output currents and voltages for the second case, as well as the percentage deviation in current sharing for the proposed algorithm, are given in Table 4.6.

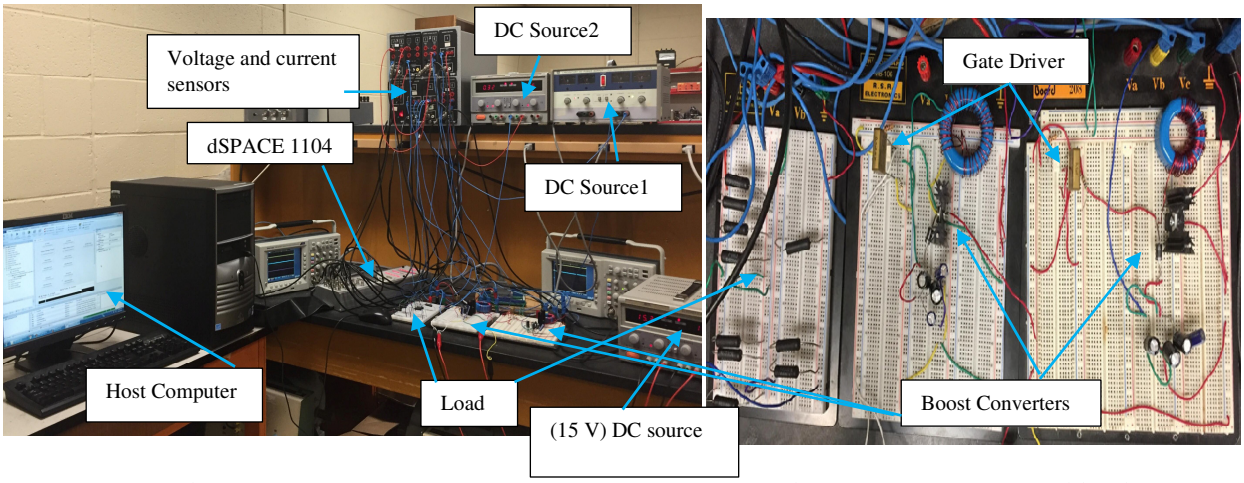
Table 4. 6: Simulation results with the proposed algorithm.

| Time (sec) | $V_{out1}$ (V) | $V_{out2}$ (V) | $V_{load}$ (V) | $I_1$ (A) | $I_2$ (A) | $I_{load}$ (A) | $\Delta I$ % current sharing differences |
|---|---|---|---|---|---|---|---|
| 0-2.5 | 12.05 | 12.05 | 11.93 | 0.308 | 0.308 | 0.61 | 0 |
| 2.5-5 | 11.97 | 11.96 | 11.79 | 0.44 | 0.44 | 0.88 | 0 |

Based on the results of Table 4.6, a precise load current sharing is achieved by the implementation of the proposed algorithm. Moreover, the improvement of the proposed algorithm can be observed by comparing the percentage deviation in the current sharing in Table. 4.5 and Table 4.6. the percentage deviation in current sharing becomes zero when the proposed algorithm is implemented.

## 4.6 Experimental Validation

Experimental validation is used to verify the proposed algorithm, which is implemented using dSPACE 1104 in real-time. The dSPACE 1104 develops the personal computer (PC) to a powerful improvement system for rapid control prototyping. Real-time interface provides Simulink blocks in MATLAB for graphical configuration of analog to digital, digital to analog, digital input/output lines, incremental encoder interface and PWM generation. The actual measurements in the circuit such as voltage and current can be captured by the analog-digital converter on the dSPACE 1104. These measurements are compared with the reference voltage and current. The designed controller is defined in the MATLAB/Simulink will generate the control signal and is sent back to the dSPACE 1104. The dSPACE converts the control signal by the digital-analog converter and the result data is used in the real time for controlling the circuit. However, Figure 4.24 shows the laboratory prototype of the developed model in Figure 4.17. The constructed experimental setup of two boost converters uses the small-scale parameters, which are given in Table 4.4. The cable resistance of 0.4 Ω is used to connect the two parallel-connected converters to a resistive load.




(a) Laboratory prototype. (b) Boost converters and load.

Figure 4. 24 Photograph of the experimental setups

Load resistances of 19.33 Ω and 42.5 Ω are connected to the parallel converters. The load resistances provide a step increase in the load. The MOSFETs in the converters are driven by 15 V PWM signals through gate drivers that isolate the MOSFETs from the dSPACE board. The sensors for the voltage and the current measurements provide an analog signal of 3:1 conversion ratio between the input and the output. Since the absolute values of the input signals to the analog-digital converters (ADCs) of the dSPACE are limited to ± 10 V, software protection is implemented in Maltable/Simulink to prevent signals that are greater than ± 10V. For the experimental results, the output current waveforms for converter I and converter II along with the total load current waveform are shown in Figure 2.25. A step-change in the load is applied to test and validate the proposed algorithm experimentally.

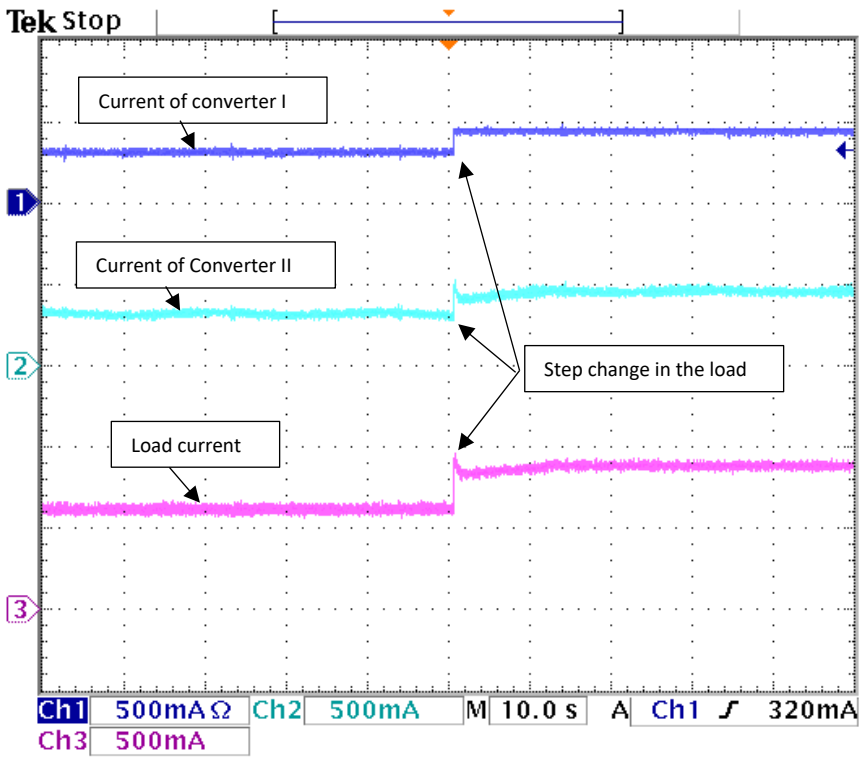



Figure 4. 25 Output current waveforms for each converter and the total load current of the proposed algorithm.

The load current in Figure 4.25 is shared equally between converter I and converter II. The initial loading has a load current sharing of 0.305 A for both converters. Furthermore, after a step increase of the load is applied, the voltage setpoint is successfully modified by the proposed algorithm to achieve equal load current sharing between the two converters. The output current of converter I and II becomes the same, and their value is 0.437 A. Thus, the experimental results of the proposed algorithm achieve zero percentage deviation in current sharing. The experimental results match the simulation results in Table 4. 6. The output waveforms of each converter and the DC bus voltage profile are shown in Figure 4.26.

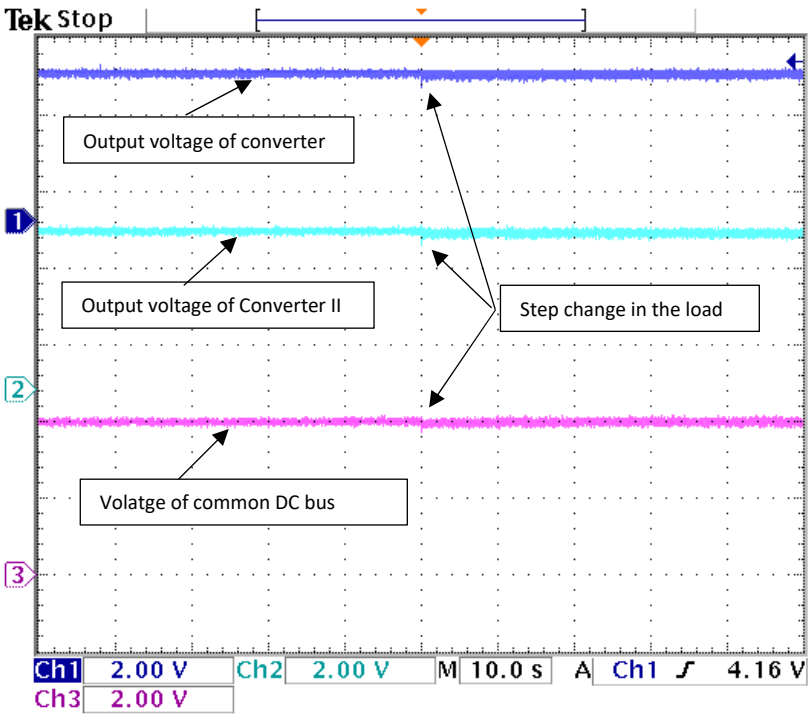



Figure 4. 26 Output voltage waveforms at each converter and the common DC bus of the proposed algorithm.

The initial voltage at the common DC bus is 11.89 V before a step increase in the load, which decreases slightly to 11.83 V after a step increase in the load is applied. By taking into account the conversion ratios of the voltage sensors and the scope scaling measurements, the experimental results are in agreement with the simulated results.

## 4.7 Summary

A modified droop method based on cable resistance implementation is presented. The proposed method includes the cable resistances in the load regulation for each converter, which helps to estimate the voltage setpoint for each converter. The voltage setpoint is estimated locally and based on the measurements at the common DC bus. Furthermore, the state-space averaging technique model for two parallel converters is developed based on synchronous switching. The developed state-space averaging model is used to study the effect of cable resistance. The cable resistance

provides a damping element in the parallel-connected converters and improves the dynamic response. The transient analysis based on the modified droop method verifies the improvement of the increase in the cable resistances. Although the proper choice of cable resistance improves the dynamic response of the system and enhances the load sharing, it decreases the system efficiency. A control algorithm is proposed to overcome the unequal sharing due to the mismatches in the parameters of parallel-connected boost converters. The proposed control algorithm improves the load current sharing by modifying the voltage setpoint. The concept is implemented by adding a control loop, which supervises the modified droop method. Finally, experimental results validate the control algorithm along with the proposed modified droop.

# Chapter 5

# Improved Droop Control Method

## 5.1 General

The concept of microgrid was proposed several years ago due to the integration of distributed energy resources (DERs) [64]. Using DC-DC converters in DC microgrids is a more efficient technique for connecting the DERs to the DC load directly [65-67]. Because DERs are decentralized and connected to the point of common coupling (PCC) in DC microgrids, several control issues of interfacing parallel-connected converters such as maximum power point tracking, voltage control, and load current sharing arise. Although utilizing parallel-connected converters in DC microgrids has several advantages, the voltage regulation at the PCC and load current sharing are the major control issues of their operation [68,69].

In the previous chapter, a control algorithm was developed to improve the load current sharing between parallel-connected converters. The control algorithm ensures equal current sharing for the mismatch of the converter parameters. The control algorithm does not account for the differences in the cable resistances. The algorithm also does not restore the voltage at the PCC to its rated value. Thus, in this chapter, an improved droop method is presented. The proposed technique overcomes the issues of current sharing and voltage regulation, while cable resistance differences are considered in the system. The unequal current sharing, which is due to the mismatch in the cable resistances, is improved by implementing a virtual droop gain (VDG). The VDG compensates for the mismatches in the cable resistance. The voltage of the common DC bus is restored using an adaptive voltage control gain (AVCG). The AVCG estimates the voltage at the common DC bus and shifts the droop gains up and or down based on the load condition to ensure

a constant voltage at the load bus. The dynamic performance of the proposed method is tested by using MATLAB simulation and validated using experimental results.

## 5.2 Cable Resistance Differences in the Droop Control Method

The load regulation characteristics for the parallel-connected converters and the differences in cable resistances affect the voltage deviation of the PCC and the load current sharing. To illustrate, for a DC microgrid shown in Figure 5.1, the two parallel-connected converters are simplified by Thevenin equivalent. They are connected to the common DC bus through cable resistances.

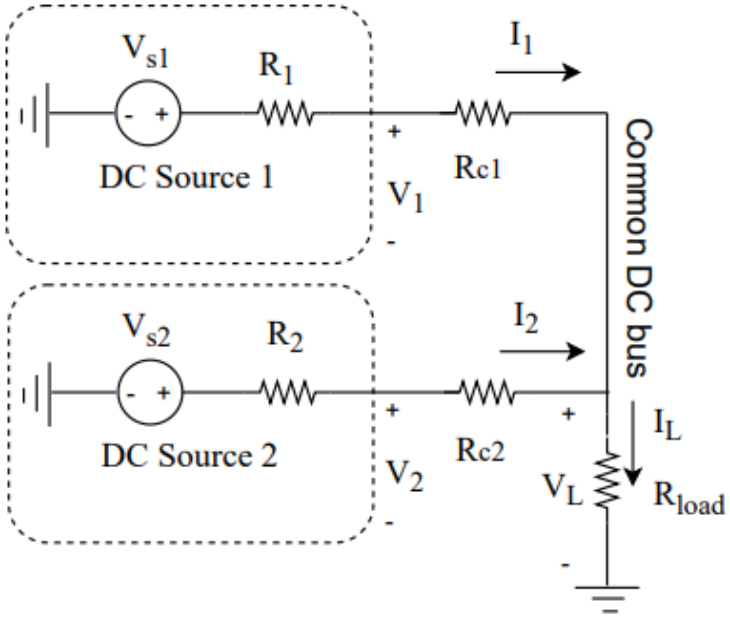



Figure 5. 1 Thevenin equivalent model for two parallel-connected converters

Based on Equations (4.1), (4.2), and (4.3), the voltage at the common DC bus based on Figure 5.1 can be derived as

$$V_L = V_{1NL} - (K_1 + R_{c1}) * I_1 \tag{5.1}$$

$$V_L = V_{2NL} - (K_2 + R_{c2}) * I_2 \tag{5.2}$$

$$V_L = (I_1 + I_2) * R_{load} \tag{5.3}$$

As can be seen in Figure 5.2 (a), due to a mismatch in the parameters of parallel-connected converters, the load current is not shared equally. The mismatch in the parameters of the parallel converters could result from manufacturing tolerance. Therefore, if the voltage at the common DC bus is $V_L$, the current sharing for converter I and II are $I_1$ and $I_2$ respectively, which are unequal. Furthermore, the increase in load changes the operating point from $V_L$ to $V`_L$, but the load current sharing $I`_1$ and $I`_2$ are still unequal. Moreover, if the cable resistances that connect the parallel converters to the common DC bus are different, the load current sharing is degraded, as shown in Figure 5.2 (b). If the cable resistance $R_{c2}$ is higher than the cable resistance $R_{c1}$, the load current sharing for converter I and II is degraded from $I_1$ and $I_2$ to $I`_1$ and $I`_2$ respectively. In other words, the differences in cable resistance worsen the load current sharing according to the droop method.

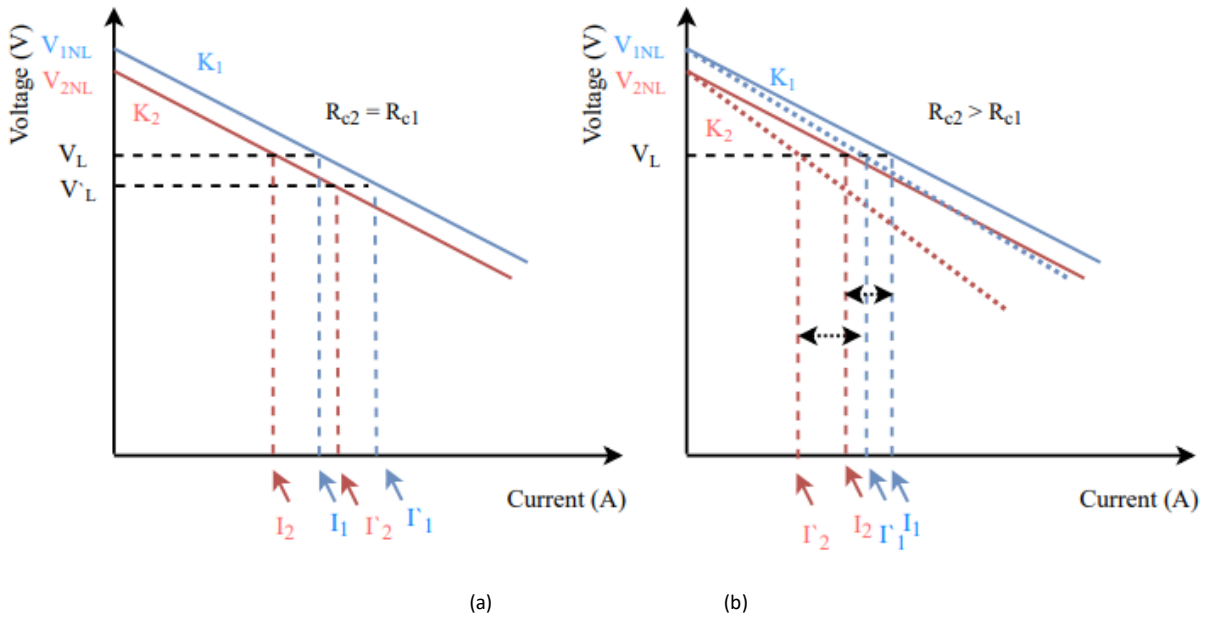



Figure 5. 2 Load regulation characteristics of parallel-connected converters (a) Connected to the load through equal cable resistance (b) Connected to the load through different cable resistances

## 5.3 The Effect of Droop Gains on the Voltage Regulation of Parallel-connected Converters

One of the limitations of the droop methods is the voltage deviation. According to Equations (5.1) -(5.3), the droop gains for converter I and converter II cause the output voltage to be lower when the load current increases. Figure 5.3 shows the load regulation characteristics of two parallel converters with different droop gains $K_1$and $K_2$. However, the voltage deviation increases when the droop gain is higher, as shown in Figure 5.2. Therefore, the droop gains $K`_1$and $K`_2$, which are higher than $K_1$and $K_2$ for converter I and II, respectively, increase the voltage deviation for the same load currents.

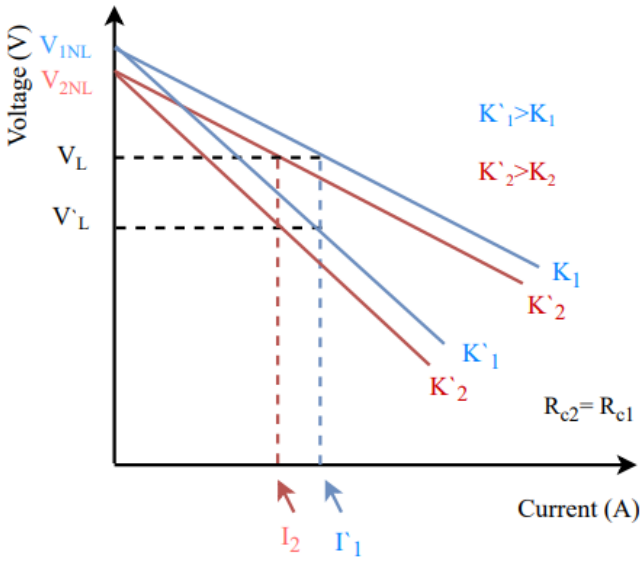



Figure 5. 3 Load regulation characteristics of the droop method for two converters

## 5.4 The Improved Droop Control Method

The proposed approach can overcome the drawbacks of the modified droop method with control algorithm. The proposed method is based on utilizing the modified droop method with cable

resistance implementation, which is reported in [61]. The load resistance is determined from the measurements of voltage and current at the common DC bus as

$$R_{\text{load}} = \frac{V_L}{I_L} \tag{5.4}$$

The modified droop method including cable resistances estimates the load current sharing, which is determined by solving Equations (5.1), (5.2), and (5.3) as

$$I_1 = \frac{{}^{V_{2NL}}/_{R_{load}} - {}^{V_{1NL}}/_{{R_{load}}^2 * (K_2 + R_{c2} + R_{load})}}{1 - {}^{1}/_{{R_{load}}^2 * (K_1 + R_{c1} + R_{load}) * (K_2 + R_{c2} + R_{load})}} \tag{5.5}$$

$$I_2 = \frac{{}^{V_{1NL}}/_{R_{load}} - {}^{V_{2NL}}/_{{R_{load}}^2 * (K_1 + R_{c1} + R_{load})}}{1 - {}^{1}/_{{R_{load}}^2 * (K_1 + R_{c1} + R_{load}) * (K_2 + R_{c2} + R_{load})}} \tag{5.6}$$

The voltage setpoints for the parallel-connected converters are determined based on the estimated current sharing values and the voltage at the common DC bus. The setpoint of the output voltage for each converter is determined locally without transmitting voltage and current data from one converter to the other as

$$V_{setponit\_1} = V_L + R_{c1} * I_1 \tag{5.7}$$

$$V_{setpoint\_2} = V_L + R_{c2} * I_2 \tag{5.8}$$

The block diagram and flowchart for estimating current sharing and the output voltage setpoint of the modified droop with cable resistance are shown in Figure 5.4, and Figure 5.5, respectively.

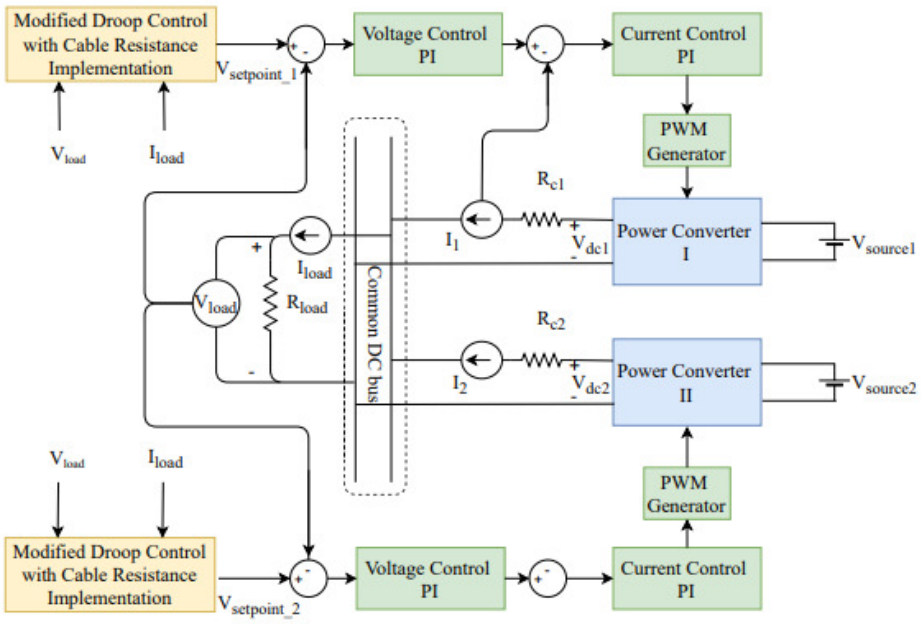



Figure 5. 4 Block diagram of the modified droop method with cable resistance

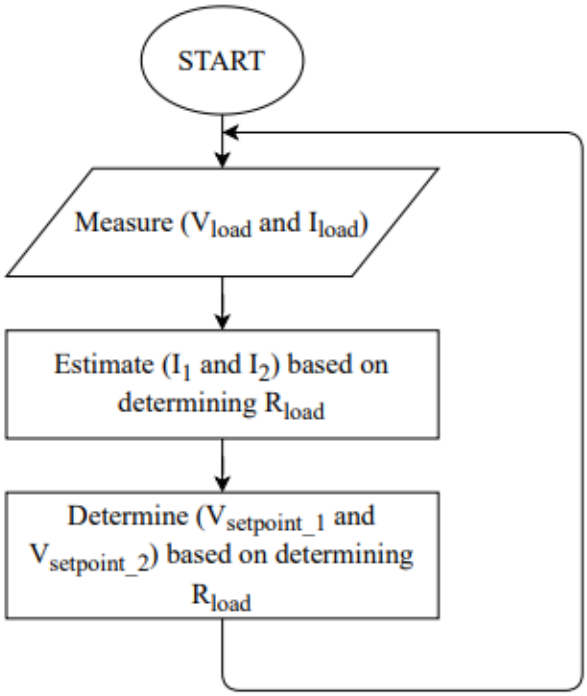



Figure 5. 5 Flow chart of the modified droop control for determining the set point of each loop controller

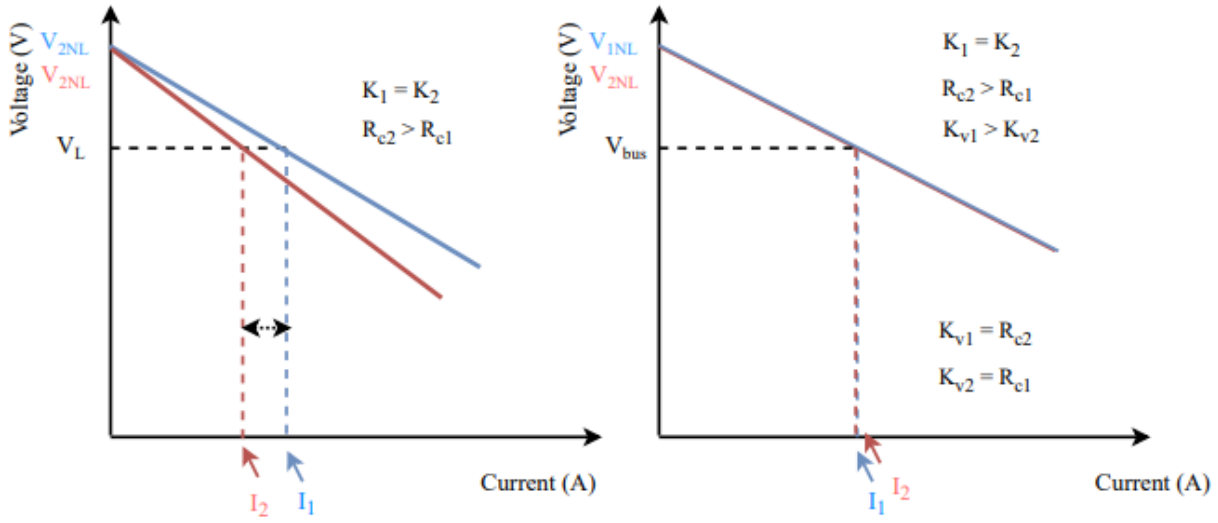
In the proposed approach, two virtual gains ($K_{v1}$, $K_{v2}$) are introduced into the modified droop control method to improve the load current sharing. $K_{v1}$and $K_{v2}$ are referred to as virtual droop

gains (VDGs). An adaptive voltage control gain (AVCG) is then introduced to regulate the load voltage. First, the virtual droop gain can be added to the droop Equations (5.1) and (5.2) as

$$V_L = V_{NL1} - (K_1 + R_{c1} + K_{v1}) * I_1 \tag{5.9}$$

$$V_L = V_{NL2} - (K_2 + R_{c2} + K_{v1}) * I_2 \tag{5.10}$$

Where $K_{v1}$ and $K_{v2}$ are the virtual droop gain for converter I and converter II, respectively. The virtual gains can be selected based on the differences in cable resistances. To illustrate, Figure 5. 6 (a) shows the load regulation characteristics for two parallel-connected converters. It is assumed that $R_{c2}$ is higher than $R_{c1}$. Thus, according to the droop method, converter I experiences higher current compared to converter II.




(a) (b)

Figure 5. 6 Implementing virtual droop gain with the load regulation characteristics of the droop method for two converters

Since the current sharing between the two parallel-connected converters is unequal, the values of $K_{v1}$ and $K_{v2}$ can be chosen based on the cable resistance compensation. To retrieve the original

load regulation characteristics, the virtual gains $K_{v1}$ and $K_{v2}$ can compensate for $R_{c2}$ and $R_{c1}$ respectively as shown in Figure 5.6 (b).

Secondly, the adaptive voltage control gain is determined based on the estimated voltage at the common DC bus. Firstly, the estimated voltage is determined by the modified droop method. Next, the estimated voltage is compared with its rated value of the voltage. The proposed adaptive control gain efficiently determines the adjusted value of the voltage to maintain the voltage at the point of common coupling at its rated value. Thus, the AVCG can be determined as

$$AVCG = V_{CC} - V_{rated} \tag{5.11}$$

Where $V_{CC}$ is the measured load voltage ($V_L$) at the PCC, and $V_{rated}$ is the rated volatge of the system. For various load conditions, the voltage at the PCC is regulated by using its estimated value, as shown in Figure 5.7.

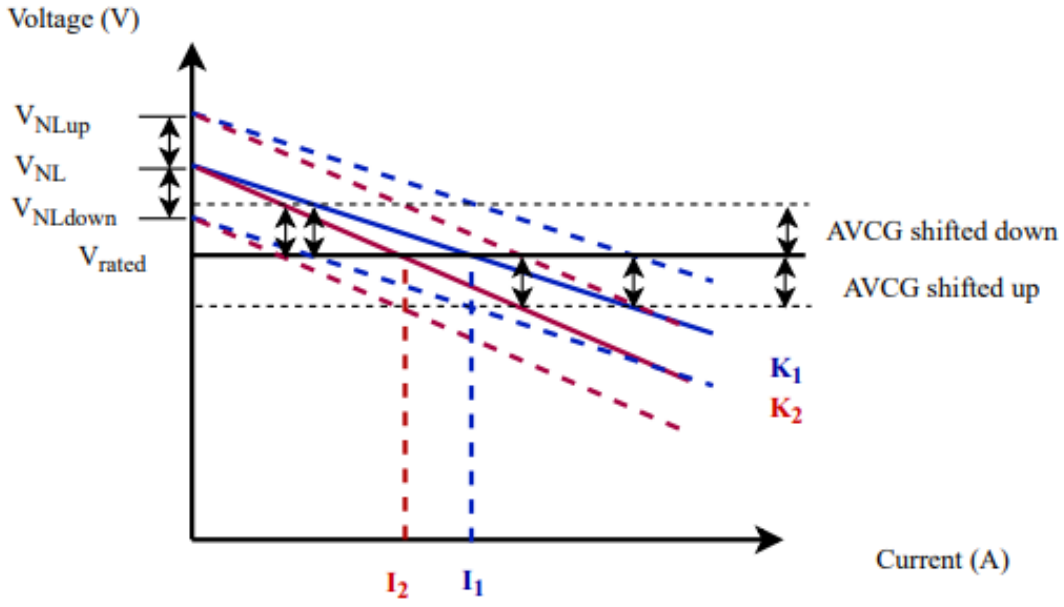



Figure 5. 7 load regulation characteristics of the droop method with AVCG implementation

The steps that are used to regulate the voltage at the common DC bus by utilizing the AVCG are:

1- Measure the voltage at the PCC ($V_L$) and the total load current ($I_L$). The load resistance can be determined as given in equation (5.4)
2- Based on the modified droop method with cable resistance implementation, the estimated output current for converter I and converter II can be determined by using equation (5.5) and (5.6).
3- The estimated voltage at the PCC (common DC bus) can be obtained as

$$V_{CC} = V_{NL1} - (R_1 + K_1) * I_1 \tag{5.12}$$

$$V_{CC} = V_{NL2} - (R_2 + K_2) * I_2 \tag{5.13}$$

The AVCG can be determined by using Equation (5.11). If the AVCG has a negative value, the load characteristic regulation of the droop method is shifted up to a newer load characteristics regulation, as shown in Figure 5.6. Since the measurements are at the PCC, the AVCG has the same value for the local controller of the two converters. Thus, the newer load characteristics regulations for both converters are shifted from the load regulation characteristics synchronously. The voltage position ensures the voltage at the PCC is at the rated voltage. However, if the AVCG has a positive value, the load characteristic regulations of the droop method, for both converters, are shifted down to a newer load characteristics regulation, as shown in Figure 5.7. Therefore, the newer load characteristic regulation adjusts the voltage at the PCC synchronously to its rated value.

The modified droop method with cable resistance implementation and control algorithm discussed in Chapter 4 is added to this algorithm to ensure precise current sharing when there is a mismatch in the parameters of the parallel converters. The overall block diagram for implementing the proposed approaches to improve the current sharing due to different cable resistances and voltage regulation is shown in Figure 5.8.

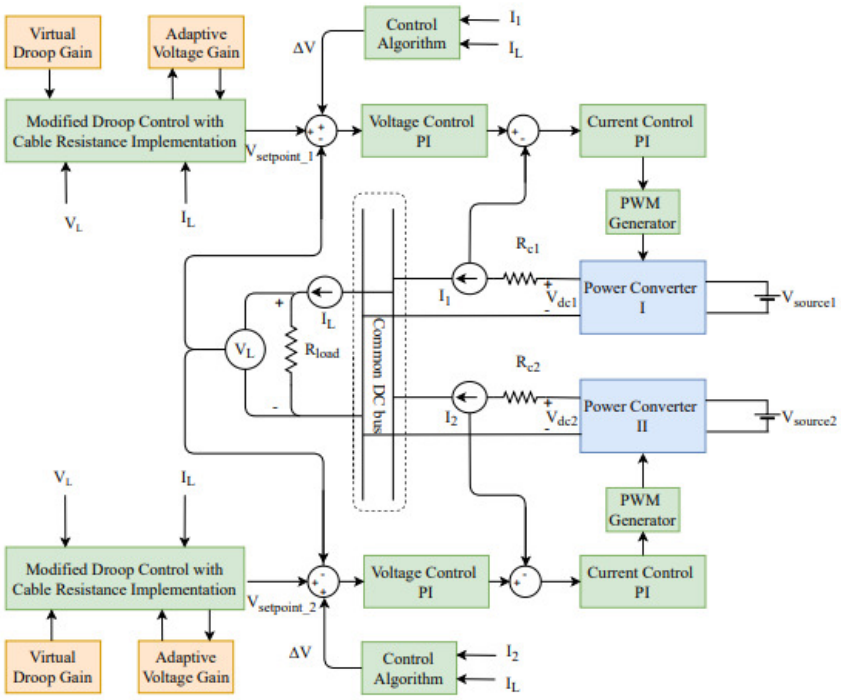



Figure 5. 8 Block diagram of the improved droop method

## 5.5 Simulation Results

The circuit diagrams in Figure 5.3, and Figure 5.8 are simulated using MATLAB/Simulink to examine the performance of the proposed droop method. The proposed droop method is compared with the conventional droop method. The parameters for the two boost converters, which have 10% mismatch in the power rating, are shown in Table 5.1.

Table 5. 1 Operating parameters of two boost converters with 10% mismatches

| Parameters | Converter I | Converter II |
|---|---|---|
| Switching frequency $\boldsymbol{f_s}$ | 25 KHz | 25 KHz |
| Inductance $\boldsymbol{L}$ | 19.2 mH | 17.4 mH |
| Capacitance $\boldsymbol{C}$ | 107.2 µF | 117.9 µF |
| Power $\boldsymbol{P}$ | 120 W | 132 W |

The PI controllers for the outer and inner loop are designed based on SISO Tool in MATLAB [54]. The gains for the voltage and current PI controllers are determined as $Kp_v = 0.001298$, $K_{Iv} =$

10.817, $Kp_i = 0.04857$, and $K_{Ii} = 12.454$ respectively. Figure 5.9 shows the load regulation characteristics for converter I and converter II. The droop gains for converter I and converter II are determined as $K_1 = 0.5734$ and $K_2 = 0.5673$.

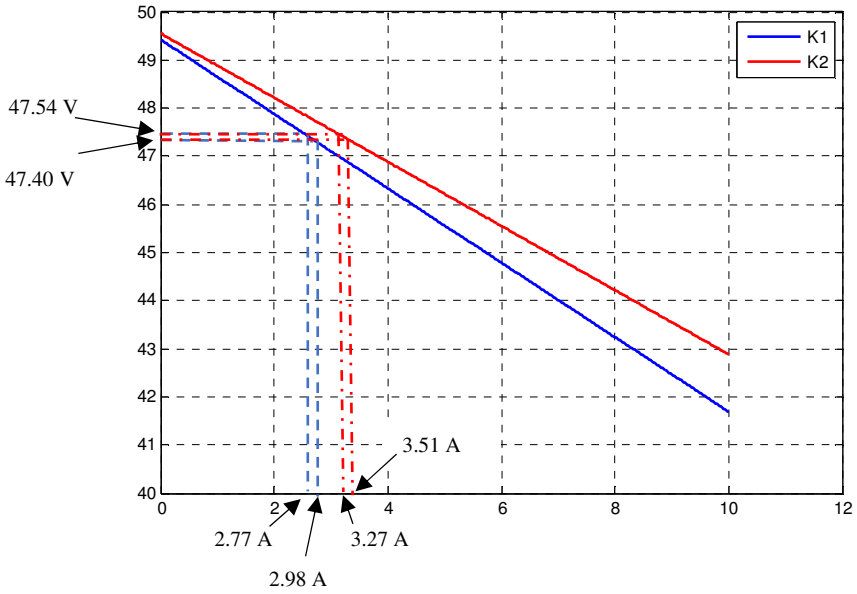
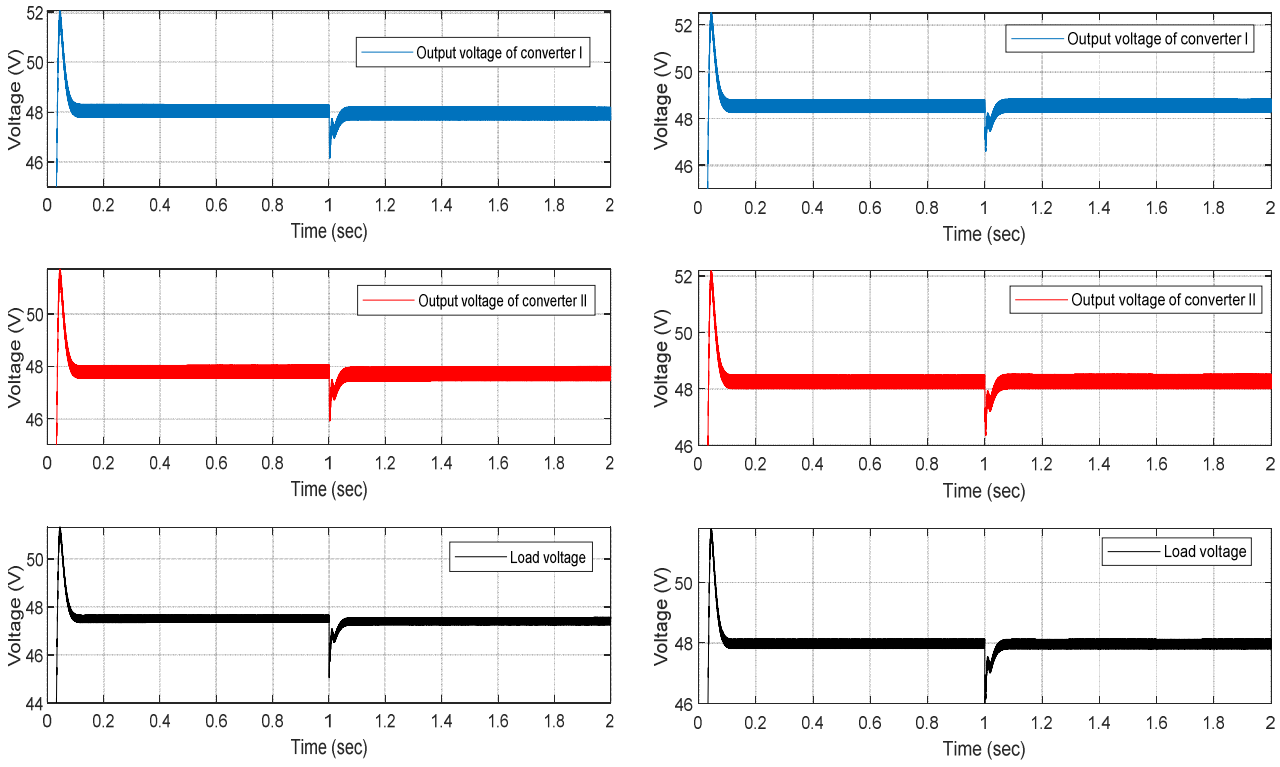



Figure 5. 9 Load regulation characteristic for converter I and II with $K_1$ *and* $K_2$

The droop action can be observed from Figure 5.9. When the load current of converter I is increased from 2.77 A to 2.98 A, the voltage at the PCC drops from 47.54 V to 47.40 V. In the same way, the output current of converter II is increased from 3.27 A to 3.51 A. Thus, in the conventional droop method, the drop in the output voltage for the parallel converters is a result of the droop action. Furthermore, the load current sharing for both converters is unequal. However, the proposed method modifies the load regulation characteristics. It adds two gains, which are implemented to improve load sharing and voltage regulation. Different load resistances are used to evaluate the performance of the proposed method. The initial load resistance has a value of $R_L = 8.6\ \Omega$, and then the load is increased at 1 second to be $R_L = 8.1\ \Omega$. The cable resistances value that connects converter I and converter II to the PCC have values of 0.2 Ω and 0.1 Ω, respectively. Two

cases are simulated in MATLAB and utilized to indicate the improvement of load sharing and the voltage regulation. The improved results for the proposed method are compared to the results of the conventional droop method. Figure 5.10 (a) and (b) shows the output voltage of each converter and the voltage at the common DC bus for two cases.




(a) (b)

Figure 5. 10 Voltage response at each converter output and at the point of common coupling for a step increase in the load: (a) Output voltages for the conventional droop method and (b) Output voltages for the proposed method

For the proposed method, the response of the voltage restoration at the PCC is improved, as shown in Figure 5.10 (b). The improvements of the results can be observed by comparing the steady-state and transient response of a step increases in the load demand at 1 second, as shown in Figure 5.10 (a) and (b). The dc voltage of each converter is modified locally by the proposed method to restore

and maintain the load voltage at its rated value of (48 V). Figure 5.11 (a) and (b) show the current response of the conventional and proposed method.

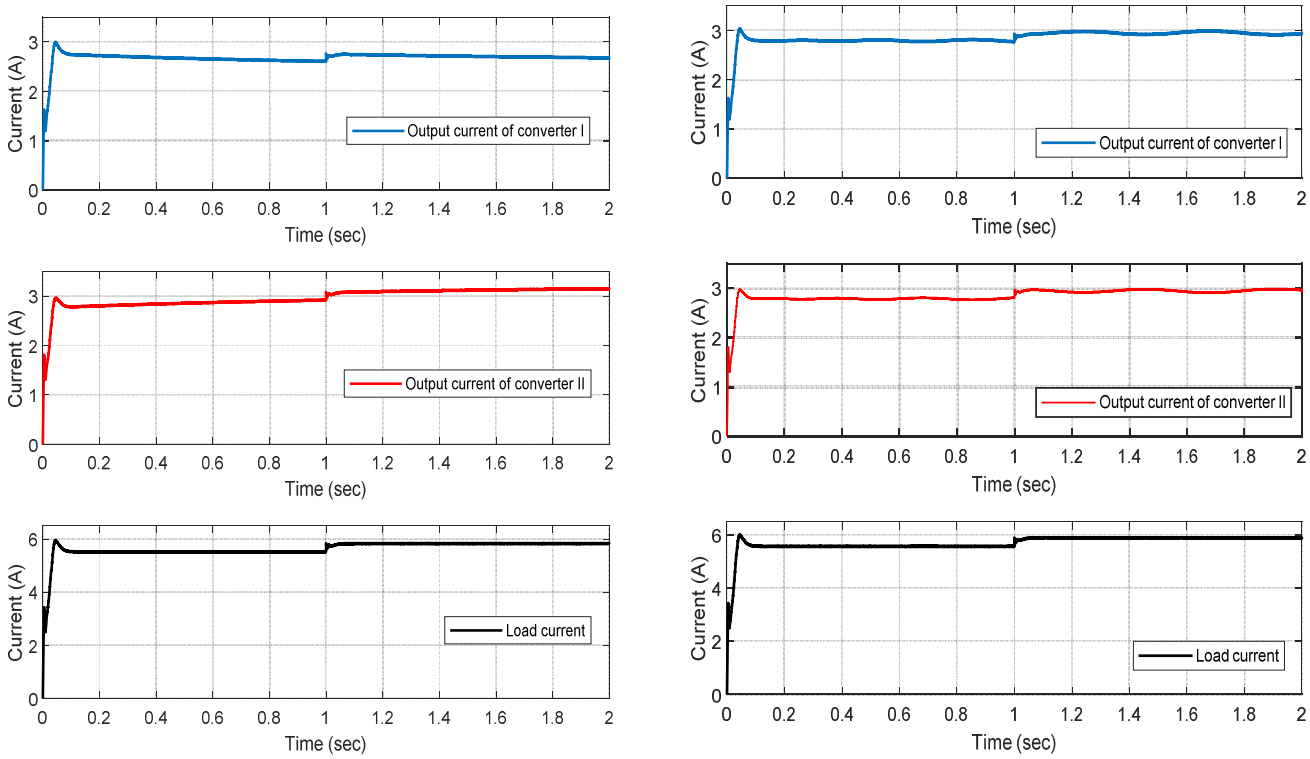



Figure 5. 11 Load current response for the two converters and the total load response: (a) Output currents for the conventional droop method and (b) Output currents for the proposed method

As shown in Figure 5.11 (a), the load current sharing is affected by the difference between the cable resistances. The output current of converter II is higher than the output current of converter II. However, for the proposed method, the load sharing accuracy between the two parallel-connected boost converters is achieved, as shown in Figure 5.11 (b). The voltage and current steady-state values for the conventional and proposed methods are summarized in Table 5.2. The percentage deviation of the current sharing for the simulated conventional and the proposed

improved droop method are also compared in Table 5.2. The percentage deviation of the current sharing for the proposed method is zero, which indicates the precise load sharing current between the two converters. The voltage at the PCC for the proposed method is maintained at its rated value as well.

Table 5. 2 Steady-state values for the simulation results for the voltage and current

| **Method** | **Conventional Droop Method** | | **The improved Droop Method** | |
|---|---|---|---|---|
| **Time (s)** | 0-1 | 1-2 | 0-1 | 1-2 |
| $\boldsymbol{I_1}$ **(A)** | 2.6 | 2.68 | 2.79 | 2.94 |
| $\boldsymbol{I_2}$ **(A)** | 2.92 | 3.14 | 2.79 | 2.94 |
| $\boldsymbol{I_L}$ **(A)** | 5.52 | 5.82 | 5.58 | 5.88 |
| $\boldsymbol{V_{dc1}}$ **(V)** | 48.1 | 48 | 48.5 | 48.6 |
| $\boldsymbol{V_{dc2}}$ **(V)** | 47.8 | 47.75 | 48.29 | 48.31 |
| $\boldsymbol{V_L}$ **(V)** | 47.5 | 47.4 | 48 | 48 |
| $\boldsymbol{\Delta I}$ **(%) current sharing differences** | 5.8 | 7.9 | 0 | 0 |

A small scale of the two parallel-connected converters is simulated and experimentally validated to verify the theoretical concept of the proposed method. The small scale of the two-boost converter is designed in continuous conduction mode and have a small mismatch in the parameters. The small scale considers similar steps of the design for the two boost converters in Table 5.1. However, the parameters of the laboratory system are given in Table 5.3. The boost converter parameters are determined based on the continuous current conduction mode of operation [52].

Table 5. 3 Parameter of boost converters

| Parameters | DC-DC Boost Converter I | DC-DC Boost Converter II |
|---|---|---|
| Switching frequency $\boldsymbol{f_s}$ | 25 KHz | 25 KHz |
| Inductance $\boldsymbol{L}$ | 9.136 mH | 10.20 mH |
| Capacitance $\boldsymbol{C}$ | 452 µF | 430 µF |
| Voltage $\boldsymbol{V}$ | 6-12 | 6-12 |

The voltage and current PI controllers, as shown in Table. 5.4 are designed based on the state space averaging technique [53]. The SISO Tool in MATLAB is used to determine the parameters of the PI controllers, which are given in Table 5.3 [70].

Table 5. 4 The PI controller parameters of voltage and current loops

| Parameters | Voltage control loop | Current control loop |
|---|---|---|
| **Proportional Gain $\boldsymbol{k_P}$** | 0.182 | 0.114 |
| **Integral Gain $\boldsymbol{k_I}$** | 23.364 | 19 |

The droop gains for converter I and converter II are determined based on two operating points, which are the no-load and full-load voltage and current [47,48]. The values for the droop gains $K_1$ and $K_2$, which are used in the simulated and experimental converters, are 0.8133 and 0.8182, respectively. The cable resistance values are $R_{c1} = 0.2\ \Omega$ and $R_{c2} = 0.1\ \Omega$. The virtual gains are selected to compensate for the differences in the cable resistances $R_{c1}$ and $R_{c2}$. Hence, the values of the virtual gains $K_{v1}$ and $K_{v2}$ are 0.1 and 0.2 respectively. Two different values of load resistances are used to compare the performance of the proposed method and the modified droop method. In the Matlab simulation study, case-1 and case-2 are tested to demonstrate the feasibility of the proposed method, whereas case-1 is for the modified droop method, and case-2 is for the proposed method. The simulated case-1 of the modified droop method is based on the block diagram shown in Figure 5.3.

In Case-1, the response of the voltage and current response is tested with an increase in the load current. The load resistance is changed from 15.5 Ω to 13.8 Ω. The transient responses of the current for converter I and converter II and the total load current are shown in Figure 5.12. The step increase in load occurs at 3 sec. It can be noticed that the load current sharing is not shared equally between the two parallel-connected converters.

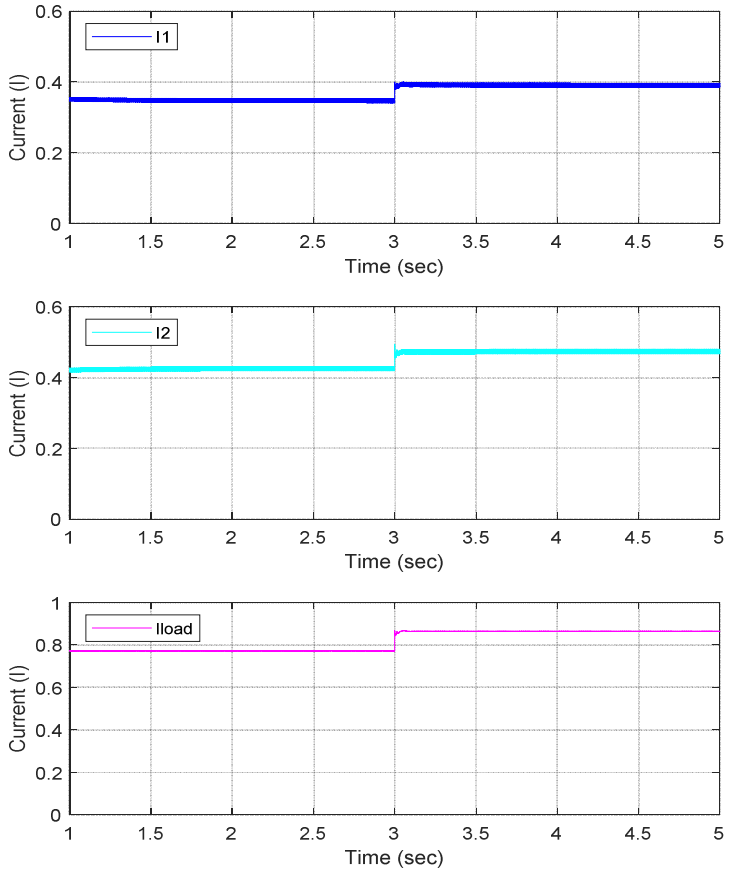



Figure 5. 12 Simulation results of current sharing for a step increase in the load with the conventional droop method

The transient responses of the output voltage for converter I and converter II and the load voltage are shown in Figure 5.13. It can be observed that after the step increase in the load is applied, the

voltage at the load or common DC bus drops. The decrease in the voltage at the PCC is the main drawback of the conventional droop method.

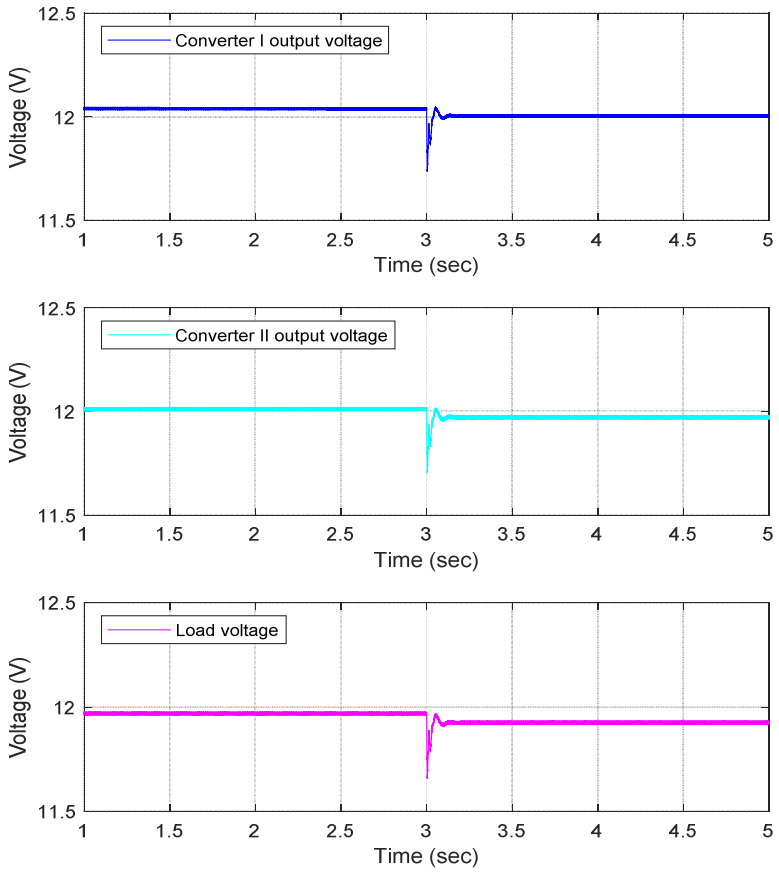



Figure 5. 13 Simulation results of output voltage for a step increase in the load with the conventional droop method

The steady-state values for the output voltage of converter I and II, the voltage at the common DC bus, load current, and the percentage deviation of the current sharing are summarized in Table 5.5.

Table 5. 5 Steady-state values for the simulation results of case 1

| **Time** | **1-3 second** | **3-5 second** |
|---|---|---|
| $\boldsymbol{I_1}$ **(A)** | 0.346 | 0.39 |
| $\boldsymbol{I_2}$ **(A)** | 0.425 | 0.475 |
| $\boldsymbol{I_L}$ **(A)** | 0.771 | 0.864 |
| $\boldsymbol{V_{dc1}}$ **(V)** | 12.04 | 12 |
| $\boldsymbol{V_{dc2}}$ **(V)** | 12.01 | 11.975 |
| $\boldsymbol{V_L}$ **(V)** | 11.97 | 11.925 |
| $\boldsymbol{\Delta I}$ **(%) current sharing differences** | 10.25 | 9.84 |

From Table 5.5, it can be observed that the voltage drops from 11.97V to 11.93 V at the common DC bus when the load increases. Furthermore, the load current sharing is unequal due to the mismatches in the parameters of the converters and the differences in cable resistance. To compare the proposed method with the conventional droop method, the block diagram of the proposed method in Figure 5.8 is simulated using MATLAB/Simulink environment. The simulate results consider the same loading condition and cable resistances in case 1. In the case study 2, the cable resistances that are connected to each converter to the common DC bus have values of 0.2 Ω and 0.1Ω for $R_{c1}$ and $R_{c2}$ respectively. The virtual droop gains are entered with values of 0.1 and 0.2 for $K_{v1}$ and $K_{v2}$ respectively. Different load resistances are used to test the performance of the proposed method.

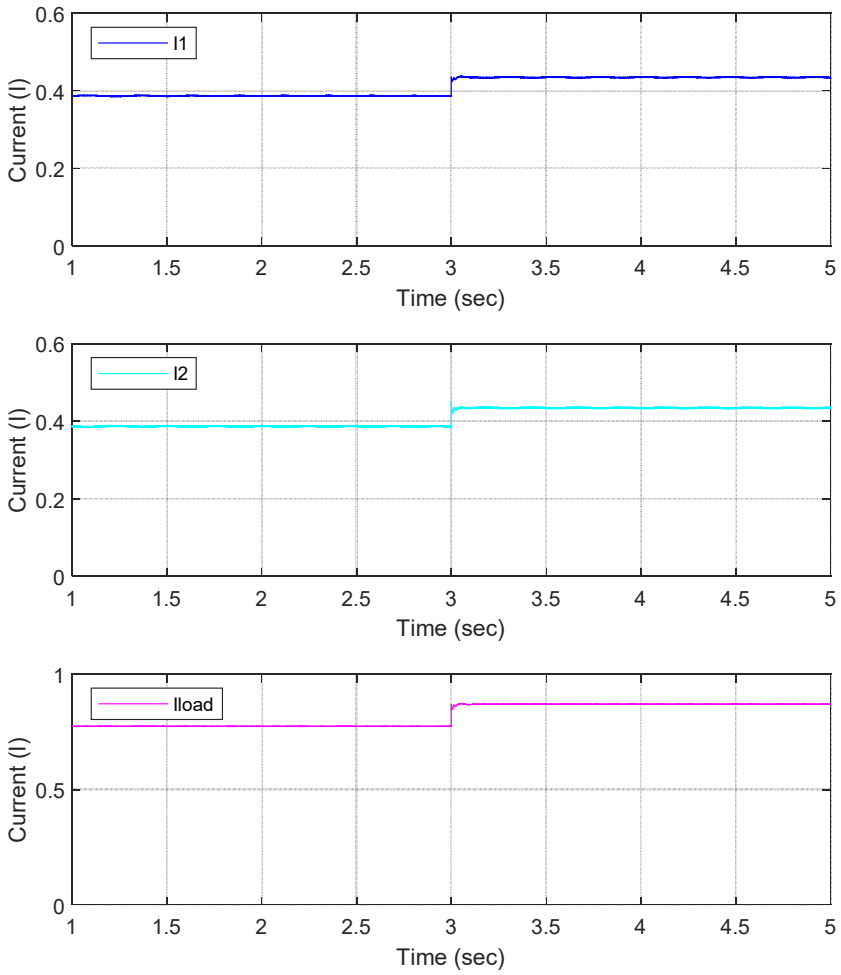



Figure 5. 14 Simulation results of current sharing for a step increase in the load with the proposed droop method

The transient response of the current sharing accuracy enhancement for converter I and II, along with the load current, is shown in Figure 5.13. Load resistances of 15.5 Ω and 13.8 Ω are applied, respectively. The response of the output voltage for converter I and II and the voltage at the common DC bus are shown in Figure 5.14. It can be observed that the proposed method is capable of restoring the voltage at the PCC when a step increase in the load demand is applied. In other words, the voltage at the common DC bus is restored at its rated value.

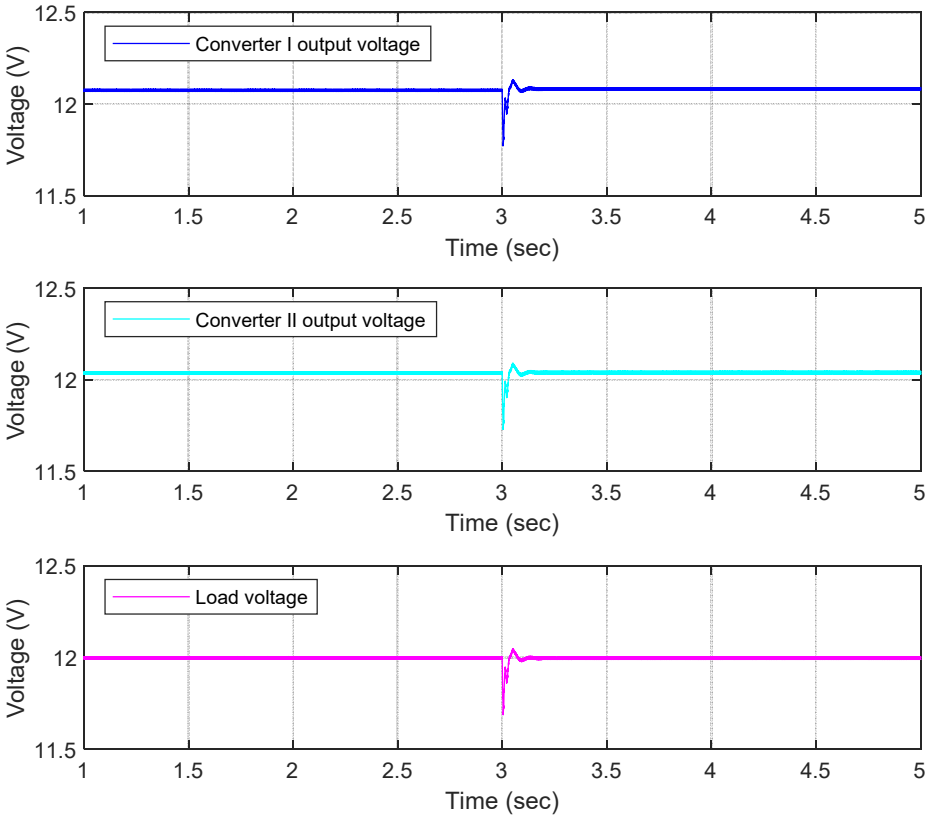



Figure 5. 15 Simulation results of output voltage for a step increase in the load for the proposed droop method

The steady-state values of the simulated results for the proposed method are summarized in Table 5.6. The current sharing accuracy is enhanced because the percentage of current deviation becomes zeroes, and the voltage at the common DC bus is restored at its rated values.

Table 5. 6 Steady-state values for the simulation results of case 2

| **Time** | **1-3 second** | **3-5 second** |
|---|---|---|
| $\boldsymbol{I_1}$ **(A)** | 0.387 | 0.435 |
| $\boldsymbol{I_2}$ **(A)** | 0.387 | 0.435 |
| $\boldsymbol{I_L}$ **(A)** | 0.774 | 0.87 |
| $\boldsymbol{V_{dc1}}$ **(V)** | 12.08 | 12.09 |
| $\boldsymbol{V_{dc2}}$ **(V)** | 12.04 | 12.04 |
| $\boldsymbol{V_L}$ **(V)** | 12 | 12 |
| $\boldsymbol{\Delta I}$ **(%) current sharing differences** | 0 | 0 |

## 5.6 Experimental Results

Experimental results are used to validate the proposed droop method. The laboratory prototype of two boost converter is implemented, as shown in Figure 5.16. In real-time control, the simulated model is compiled by dSPACE 1104. The parameters of the two boost converters that are given in Table 5.3 are used. Furthermore, to test the proposed control method, different cable resistances of 0.2Ω and 0.1Ω are used to connect converter I and II respectively to the common DC bus. Two different load resistance of 15.5 Ω and 13.8 Ω are employed, respectively. The same loading conditions of the simulated case 2 is used to compare the simulated MATLAB model with real-time implementation.

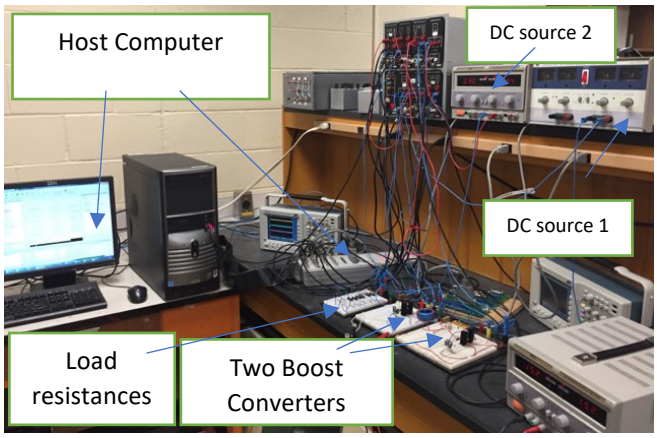



Figure 5. 16 Prototype parallel-connected DC boost converters system

Furthermore, since the signal applied to dSPACE 1104 A/D channel is limited to ± 10 V, the measurements of voltage and current sensors have a conversion ratio of 30-10 V and 10-1V, respectively, and software protection in Matlab/Simulink is used to prevent signal higher than ±10V. The actual voltage and current are measured by sensors and converted by the A/C converter in the dSPACE 1104. However, the generated control signal in the host computer is sent to the dSPACE, 1104 which converts it by D/A converter. Because the D/A channel of the dSPACE 1104 is limited to ±10 V, a gate driver is used to provide PWM of 15 V and to isolate the dSPACE 1104 from the actual hardware. Initially, the load is set up to 15.51 Ω, and the output currents for converter I and II and the load current are shown in Figure 5.17. When a step increases in the load from 15.5 Ω to 13.8 Ω is applied, the transient response for the proposed method validates the accuracy of current sharing between the two converters, as shown in Figure 5.17.

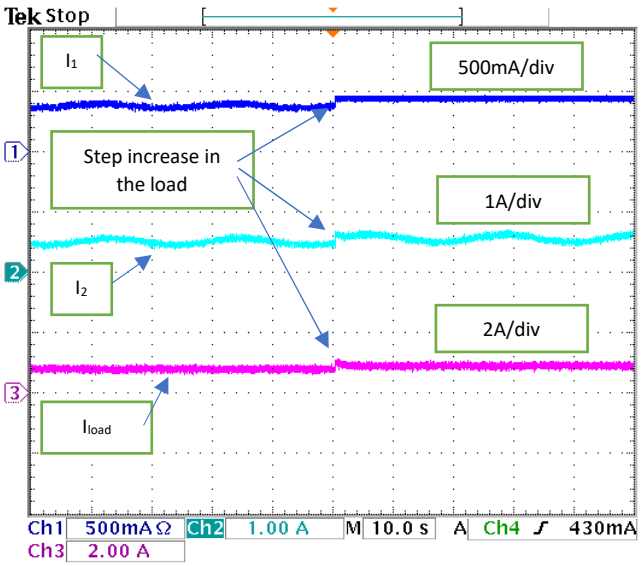



Figure 5. 17 Experimental results of load current sharing accuracy for a step increase in the load current

The output voltage responses of converter I and II and at the common DC bus are shown in Figure 5.18. It can be observed that the voltage at the common DC bus is maintained at its rated value of 12 V after the step increase in the load.

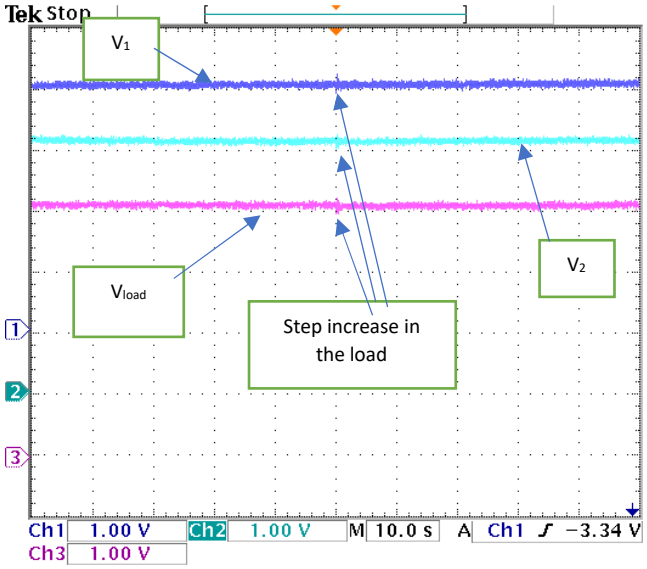



Figure 5. 18 Experimental results of the output voltage of each converter and the voltage at the common DC bus for step change in the load current

For the step increases in the load, the steady-state values of the load current sharing and the voltage at the common DC are given in Table 5.7. The percentages of current deviation that is carried out from the real-time implementation validate the proposed method.

Table 5. 7 Steady-state values for experimental results

| **Load resistance** | **15.5Ω** | **13.8Ω** |
|---|---|---|
| $\boldsymbol{I_1}$ **(A)** | 0.388 | 0.436 |
| $\boldsymbol{I_2}$ **(A)** | 0.388 | 0.436 |
| $\boldsymbol{I_L}$ **(A)** | 0.776 | 0.872 |
| $\boldsymbol{V_{dc1}}$ **(V)** | 12.11 | 12.09 |
| $\boldsymbol{V_{dc2}}$ **(V)** | 12.09 | 12.10 |
| $\boldsymbol{V_L}$ **(V)** | 12 | 12 |
| $\boldsymbol{\Delta I}$ **(%) current sharing differences** | 0 | 0 |

Furthermore, the voltage at the PCC or load is maintained at its rated value during different load conditions, as shown in Table 5.7.

## 5.7 Summary

The improved droop control method for controlling parallel-connected converters is presented. The proposed method enhances current sharing by implementing the VDG, which modifies the load regulation characteristics for each converter. The modified load regulation characteristics overcome the mismatches in the load current sharing due to the differences in the cable resistances. Furthermore, the improved droop method restores the voltage at the PCC by using the AVCG. The AVCG maintains the voltage at the common DC bus at its rated value by shifting the load

regulation characteristics for each converter to restore the voltage at the PCC to its rated value. The improved droop method is verified using MATLAB/ Simulink, and the experimental validation of the simulated method is proved

# Chapter 6

# Dynamic Modeling, Simulation, and Control of a Residential Building Microgrid

## 6.1 General

Microgrids are gaining more attention around the word due to the increase in the electricity demand and the desire for green power. The advocacy for low-carbon future from governments around the world presents the microgrid powered by renewable resources promising electricity generation options now and in the future. A report from the International Energy Association indicates that 622 million people out of 1.3 billion in Africa do not have access to electricity [71]. In the African region, the report reveals that Sub-Saharan Africa has the lowest access rate to electricity in the world. Thus, governments in African regions consider that increasing electricity access is one of the important programs on their agenda. Microgrids, which can be deployed to achieve these programs, mainly depend on renewable energy sources such as wind, hydropower, biomass, and solar.

Standalone microgrids have become popular around the world because they provide more reliable, efficient, flexible, and economical power supply. Standalone microgrids are defined as an independent entity, which can sustain its load demand without the need for an external grid. Usually, the load demand is met by using renewable energy sources and storage systems. Microgrid systems are designed for powering remote communities remote area power supply systems, distribution network loads and commercial buildings, universities, residential buildings, etc. The essential rule of designing renewable microgrid is the availability of renewable resources such as wind or solar irradiation. However, since the world's most abundant and permanent

renewable power source is solar irradiation, solar power is the most accessible source, especially in remote communities such as rural areas [72], where connecting these communities to the electrical grid is more expensive [73].

This chapter focuses on the sizing and dynamic modeling of a standalone DC microgrid powered by PV system for a residential building in an example location (Messallata) in Libya. The solar-powered microgrid is chosen as a renewable energy source because the average solar irradiation in Libya is about $5.05\ kWh/m^2/day$ [74]. The sizing of the system is accomplished based on the feasibility of the solar PV power system under different average daily solar exposure patterns at the selected location to generate sufficient power to feed a $1000\ ft^2$ house in Libya. The outcome of Homer Pro suggested the components' size and cost, which is required to meet the hourly load demand for the house. Finally, The microgrid is modeled in MATLAB/Simulink, and the dynamic response for the microgrid is studied under different scenarios of solar irradiance, feasibility, and load. The results indicate that the use of the improved droop method for the parallel converters guarantees precise load sharing and acceptable voltage regulation for the system under consideration.

## 6.2 Proposed Standalone DC Microgrid

The standalone PV system is one of the popular applications in PV generation because it has highly practical values in off-grid area. The proposed standalone PV system architecture in this chapter is shown in Figure 6.1. It has two types of converters: (1) the renewable side converter and (2) the load side converter. The renewable side converter interconnects the PV system to the storage system. The objective of the renewable energy side converter is to extract the maximum power from the PV system because the output power of a PV system fluctuates according to the variation of the solar irradiation and ambient temperature. The maximum power point tracking converter is

needed to increase the efficiency of the PV system. In general, maximum power tracking methods are presented in the literature, such as fractional open circuit voltage FOCV and fractional short circuit current FSCC methods, which are the easiest to implement and have high and medium convergence speed under dynamic weather conditions respectively [75-77]. However, steady-state tracking accuracy is medium. Therefore, the Bisection Numerical Algorithm (BNA) is presented in this chapter to increase the steady-state tracking accuracy. Thus, The BNA indicates more accuracy in terms of tracking the maximum power from a PV.

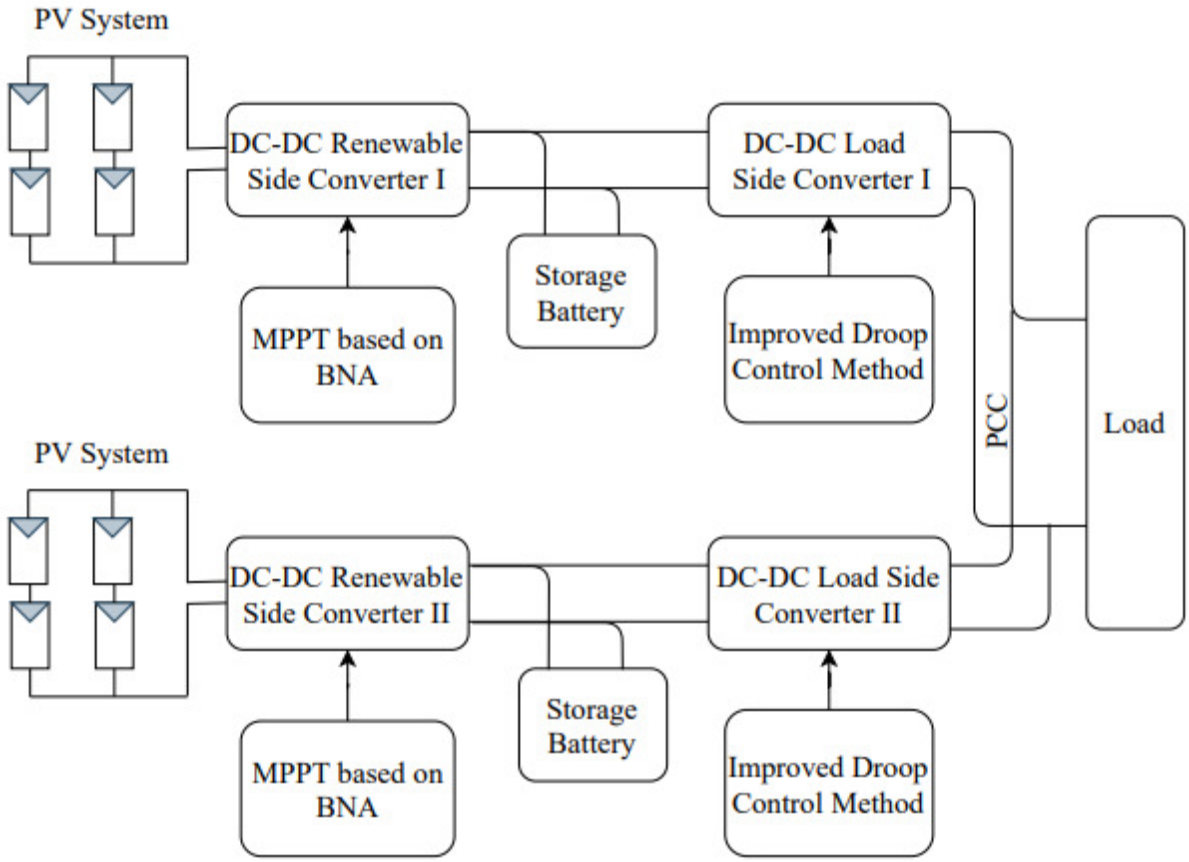



Figure 6. 1 Proposed standalone DC microgrid

The purpose of the load side converter, as shown in Figure 6.1, is to regulate the voltage of the PCC to the nominal value through a voltage regulator unit. The load side converter also ensures

equal load current sharing between parallel converters. In this chapter, the load side converter utilizes the improved droop method to restore the voltage at the PCC and ensure equal current sharing.

## 6.3 Sizing of Microgrid Components

The specified components' size and cost of the proposed standalone microgrid are evaluated from a techno-economic point of view, which utilizes the HOMER Pro software. The structure of the microgrid, which is considered in this study, is shown in Figure 6.2. It consists of PV systems combined with the Battery Energy Storage System (BESS). The BESS takes into account the periods of prolonged lack of sunshine and nighttime.

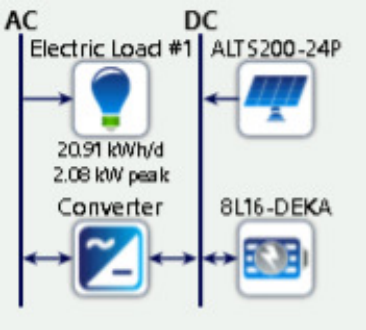



Figure 6. 2 Schematic diagram of a standalone microgrid

### 6.3.1 Electrical Load

The sized solar PV system and storage system supplies a daily load curve for the 1000 $ft^2$ house in Libya for weekdays throughout the year. The annual load curve on an hourly basis for the house is illustrated in Figure 6.3. The load curve has been created by the homer Pro software taking into account the daily and seasonal variation, which matches the peak load profile for the same weather condition (specified by the location and the user). It is evident that the peak load occurs in the summer.

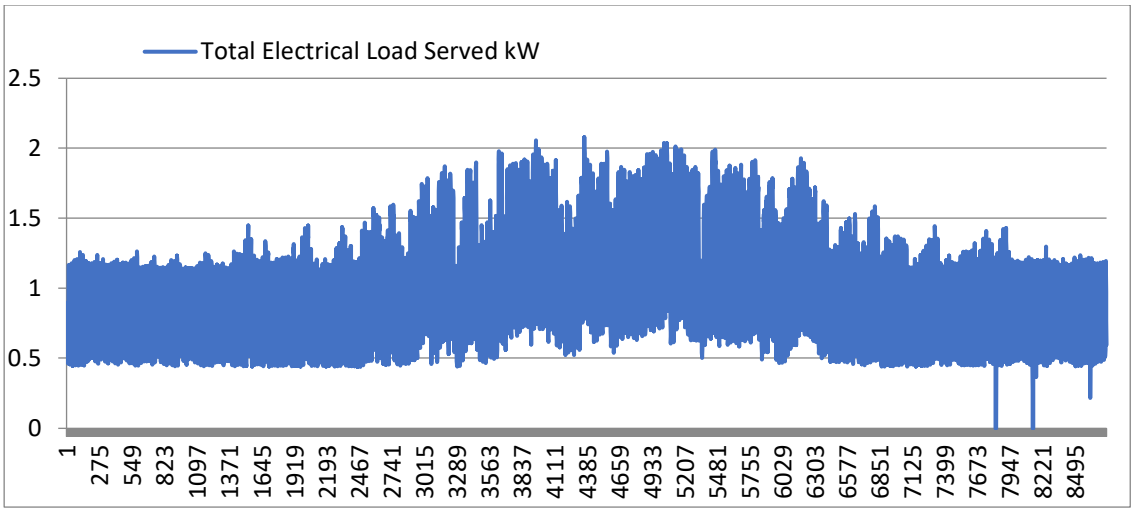



Figure 6. 3 Hourly load curve of 1000 $ft^2$ *house in Libya*

### 6.3.2 Solar irradiation

The Homer Pro optimization software includes a library of solar resources worldwide, as determined by NASA's data [78]. Based on the selected location in Libya, the solar resource shown in Figure 6.4 has been carried out. The annual average solar irradiation is $kWh/m^2/day$.

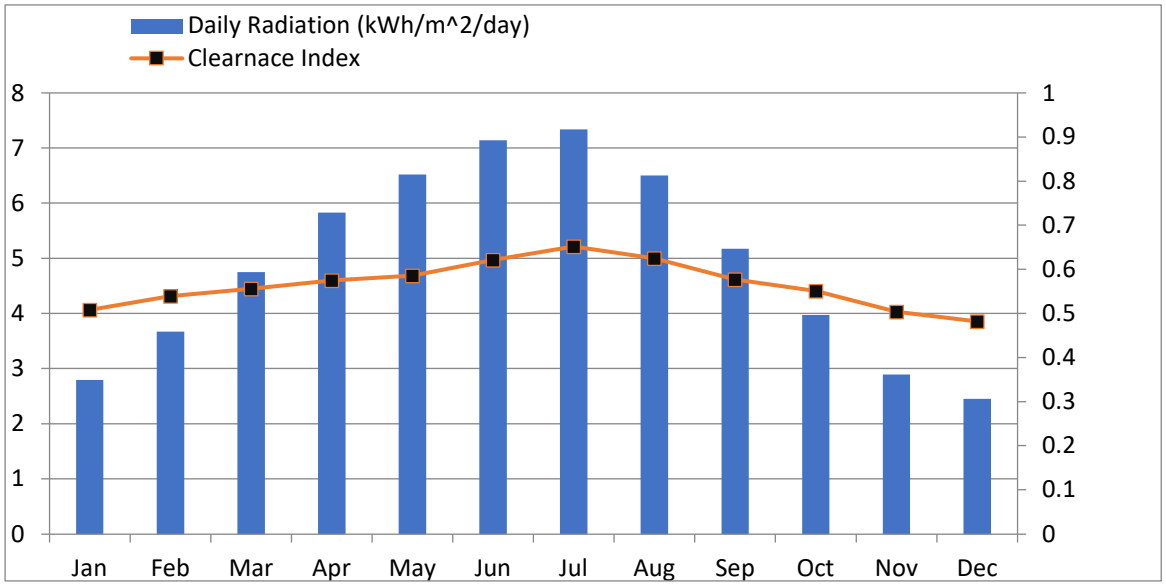



Figure 6. 4 Yearly solar resource in Mesallata, Libya

### 6.3.3 Economics

The parameters for various microgrid components given in Table 6.1 loaded to the Homer Pro for optimizing the size of various components. The estimated costs for the PV system, converter, and lead-acid battery are based on the $/kW for ALTE 200 Watt 24V Poly Solar Panel, and of MK battery 8L16-DEKA, and Magnum Energy MS2812 converter, which are given in Appendix C [79,80].

Table 6. 1 Input data regarding system components

| System component | Capital cost ($/kW) | Replacement Cost ($/kW) | O & M cost ($/kW/year) | Lifetime (years) | Efficiency (%) |
|---|---|---|---|---|---|
| PV system | 1095 | 1095 | 13 | 25 | 15.72 |
| Converter | 572 | 572 | 20 | 15 | 90 |
| Lead acid battery | 129 | 129 | 1.35 | 10 | 80 |

The Homer Pro is utilized to simulate the autonomous microgrid to assess the capital, operational, cost with the size of the components. The assessment takes into account the peak load and the minimum state of charge of the storage system. The economic results are shown in Figure 6.5 is based on the input data given in Table 6.1 and technical constraints such as maximum load and the minimum state of charge for the BSSE system.

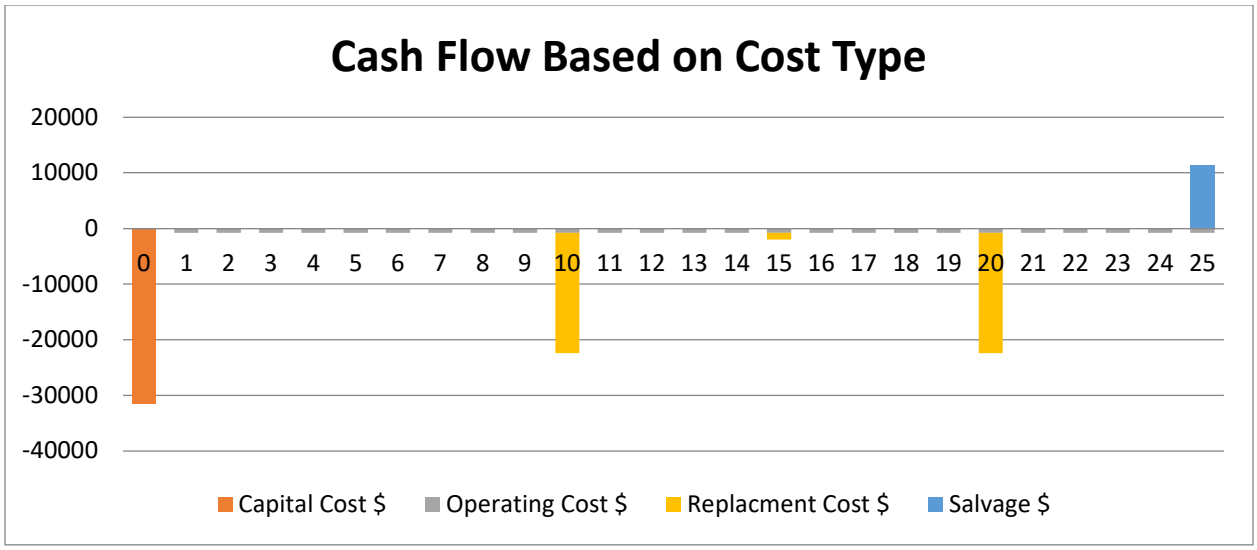



Figure 6. 5 Cash flow of standalone solar home system for the entire life span

The cost summary in Figure 6.5 for the solar home system includes the capital cost, the annual cost of operation, replacement cost, and salvage. For the proposed system, a user will spend an initial cost for the installation of the solar home system and replace the battery every ten years due to the life span for the battery. Furthermore, the converter cost will be added when fifteen years are passed. However, the long lifespan of the PV system and converter contribute to the feasibility of the user. Thus, at the end of the life span of the system, the salvage or will contribute to the newer system installation. The state of charge for the battery storage system has a contribution to lower or increase the capital cost or replacement cost if the limits of discharge are considered. However, for the optimized solar home system, the state of charge is shown in Fig. 6.5. It considers the minimum discharge of 60%.

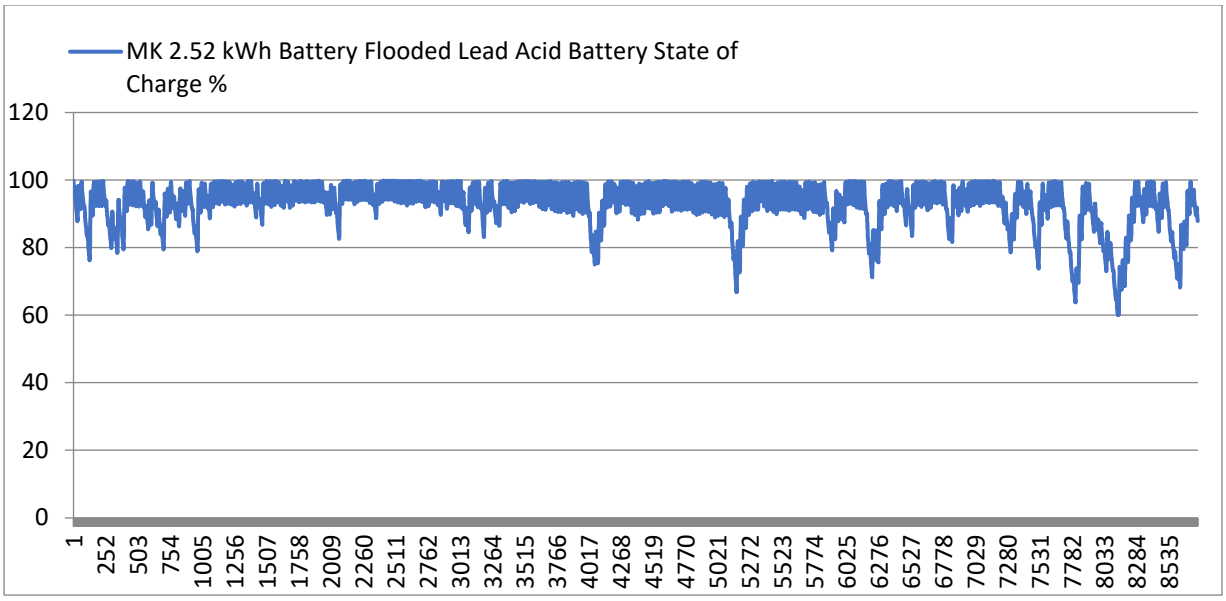



Figure 6. 6 State of charge of the battery storage system based on the load curve and available solar irradiation

From the analysis of Homer Pro, the optimal results are carried out for the arrangements of 8 kW PV panel, 2.2 kW inverter, and 70 batteries ( 420 Ah, 6 V). The Homer Pro results are based on the selected location, load curve, and minimum state of charge along with the input cost data of microgrid components. Because the proposed standalone microgrid has two parallel systems that are connected at the PCC, as shown in Figure 6.1, the 8 kW is divided into two parallel PV systems of 4 kW. Each solar PV system, which is connected to the storage system of 35 batteries through a DC-DC renewable side converter. The load side converters connected the two separated storage systems to the load, as shown in Figure 6.1.

## 6.4 The Solar PV System

The solar-PV system comprises the solar-PV array and the renewable side DC-DC converter that incorporates a maximum power point tracking (MPPT) algorithm to extract maximum power from the solar-PV array is described in the following subsections.

### 6.4.1 Model of the Solar Array

The solar-PV array is modeled using the five-parameter model for the photovoltaic cell, as shown in Figure 6.7 [81]. The most important part that affects the accuracy of a simulation of the solar-PV array is modeling, which mainly involves the estimation of the non-linear I-V and P-V characteristics curves. The five-parameter model is capable of analytically describing the I-V and P-V curves of a solar-PV array for various conditions of solar irradiance and operation temperature.

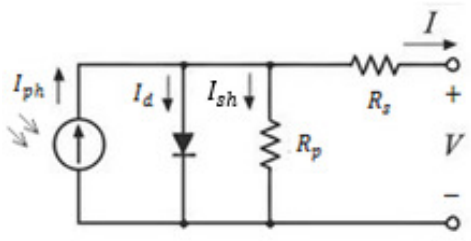



Figure 6. 7 Practical single diode model of the PV cell

As shown in Figure 6.7, the equivalent circuit of five parameter model consists of a photocurrent source connected in parallel with a single diode and shun resistance $R_p$ expressing a leakage current and series resistance $R_s$ describing an internal resistance to the flow of current $I$. The five parameters that describe the non-linear Equations (6.1) to (6.6) are photocurrent $I_{ph}$, The diode saturation current, the diode ideality factor $a$, the series resistance $R_s$ , the parallel resistance $R_p$. From the practical diode model for the PV cell shown in Figure 6.7, the PV system output current ( $I$ ) by using Kirchhoff's current law is given by:

$$I = I_{ph} - I_d - I_{sh} \tag{6.1}$$

The cell photocurrent $I_{ph}$ in (6.1) depends on the ambient temperature and solar irradiation, which is given by:

$$I_{ph} = \frac{G}{G_n} * (I_{sc} + k_i * (T_{OP} - T_{ref})) \tag{6.2}$$

Where $G$ and $G_n$ are the actual solar irradiance and nominal solar irradiance ($1000W/m^2$) respectively. $I_{sc}$ is the PV short circuit current, and $k_i$ is the temperature coefficient of the short circuit current. $T_{op}$ and $T_{ref}$ are the operating temperature and the nominal temperature ($25^oC$), respectively. However, the diode current $I_d$ in equation (6.1), which is proportional to the saturation current is given by:

$$I_d = I_0 * (e^{(q*(V+I*R_s)/(a*N_s*K*T_{op})} - 1) \tag{6.3}$$

Where $q$ and $K$ are the charge of the electron ($1.61 * 10^{-19}\ C$) and Boltzman's constant ($1.38 * 10^{-23}\ J/K$), respectively. $V$ is the terminal voltage of the photovoltaic array, $a$ is the diode ideality factor, and $N_s$ is the number of cells in series of cells in the PV array module. The diode saturation current $I_0$ in (6.1) is given by:

$$I_0 = I_{rs} * (\frac{T_{OP}}{T_{ref}})^3 * e^{(q*E_g/(K*a))} * (\frac{1}{T_{ref}} - \frac{1}{T_{OP}})) \tag{6.4}$$

Where $E_g$ is the band-gap energy of a semiconductor. The cell reverse saturation current $I_{rs}$ is given by:

$$I_{rs} = \frac{I_{sc}*k_i*(T_{OP}-T_{ref})}{e^{(q*V_{oc}*(k_v*(T_{OP}-T_{ref}))/(a*N_s*K*T_{op}))}} \tag{6.5}$$

$V_{oc}$ in (6.5) is the open-circuit voltage of the photovoltaic array. $k_v$ is the temperature coefficient of $V_{oc}$.

Finally, the leakage current in the parallel resistance $I_{sh}$ in (6.1) is given by:

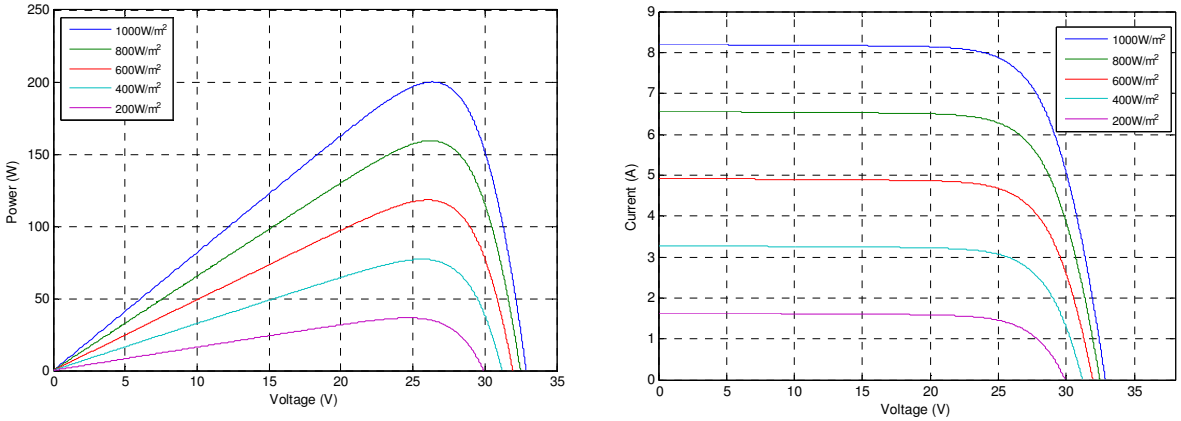
$$I_{sh} = \frac{(V+I*R_s)}{R_p} \tag{6.6}$$

The characteristic of the PV module for various solar irradiation and ambient temperature can be determined by modeling (6.1) - (6.6) in Matlab/Simulink. The standard test condition (STC) parameters for a KYOCERA KC200GT photovoltaic module ($1000W/m^2$ and $25^oC$) are shown in Table 6.2 [82]. For this module, the nominal solar irradiance, $G_n$ in equation (6.2) is $1000W/m^2$.

Table 6. 2 Parameters of the KYOCER KC200GT PV module at $25^oC$ and $1000W/m^2$

| **Parameters** | **Value** |
|---|---|
| Short circuit current ( $\boldsymbol{I_{sc}}$) | 8.21 A |
| Open-Circuit Voltage ( $\boldsymbol{V_{oc}}$) | 32.9 V |
| MPP Current ( $\boldsymbol{I_{mpp}}$) | 7.61 A |
| MPP Voltage ($\boldsymbol{V_{mpp}}$) | 26.3 V |
| Temperature coefficient of $\boldsymbol{I_{sc}}$ ($\boldsymbol{k_i}$) | 0.0032 A/K |
| Temperature coefficient of $\boldsymbol{V_{oc}}$ ($\boldsymbol{k_v}$) | -0.123 V/K |
| Number of cells in series ($\boldsymbol{N_s}$) | 54 |
| Diode ideality factor ($\boldsymbol{a}$) | 1.3 |
| Series resistance ( $\boldsymbol{R_s}$) | 0.221 Ω |
| Parallel resistance ( $\boldsymbol{R_p}$) | 415.405 Ω |

For different solar irradiance and at $25^oC$ , the P-V and I-V characteristics for the KYOCERA KC200GT PV module are shown in Figure 6.8 (a) and (b).




(a) (b)

Figure 6. 8 P-V and I-V characteristics with different irradiance for PV module

As expected, the increase in solar irradiance in Figure 6.8 (a) and (b) results in an increase of the output power and short circuit current for the photovoltaic module.

### 6.4.2 MPPT based on Bisection Numerical Algorithm

The bisection numerical algorithm (BNA), which is used to implement the MPPT at various values of solar irradiance, is reported in [83]. Equation (6.1) is used to determine an expression for the power as a function of the photovoltaic array output voltage. Therefore, Equation (6.1) can be rewritten as follows:

$$I = \frac{1}{1+{R_s}/{R_p}} * (I_{ph} - I_0 * (e^{(q*\frac{V+I*R_S}{a*N_S*K*T_{op}})} - 1) - \frac{V}{R_p}) \tag{6.7}$$

The output power of the photovoltaic as a function of the output voltage and current is given by

$$P = \frac{V}{1+{R_s}/{R_p}} * (I_{ph} - I_0 * (e^{(q*\frac{V+I*R_S}{a*N_S*K*T_{op}})} - 1) - \frac{V}{R_p}) \tag{6.8}$$

Equation (6.8) can be rearranged by assuming that the maximum current is equal to $I = 0.9\, I_{sc}$ at the maximum power point. This assumption has no major effect on the accuracy of the BNA, as shown in Table 6.3. Thus, the output power in Equation (6.8) is rewritten as a function of output voltage $V$ at the maximum output PV current of approximately $0.9\, I_{sc}$.

$$P = \frac{V}{1+{R_s}/{R_p}} * (I_{ph} - I_0 * (e^{(q*\frac{V+0.9*I_{SC}*R_S}{a*N_S*K*T_{op}})} - 1) - \frac{V}{R_p}) \tag{6.9}$$

By taking the derivative of the output power in Equation (6.9) with respect to the output voltage, the results in the following expression.

$$\frac{dP}{dV} = \frac{1}{1+{}^{R_s}/_{R_p}} * (I_{ph} - I_0 * (e^{\left(q*\frac{V+0.9*I_{SC}*R_S}{a*N_S*K*T_{op}}\right)} + V * e^{\left(q*\frac{V+0.9*I_{SC}*R_S}{a*N_S*K*T_{op}}\right)} * \frac{1}{({}^{q}/_{a*N_S*K*T_{op}})} - 1) - \frac{2*V}{R_p})$$

(6.10)

The output power in Equation (6.9) and its derivative form in Equation (6.10) for ($1000W/m^2$ and $25^oC$), are shown in Figure 6.9. By solving Equation (6.10), the maximum power can be determined.

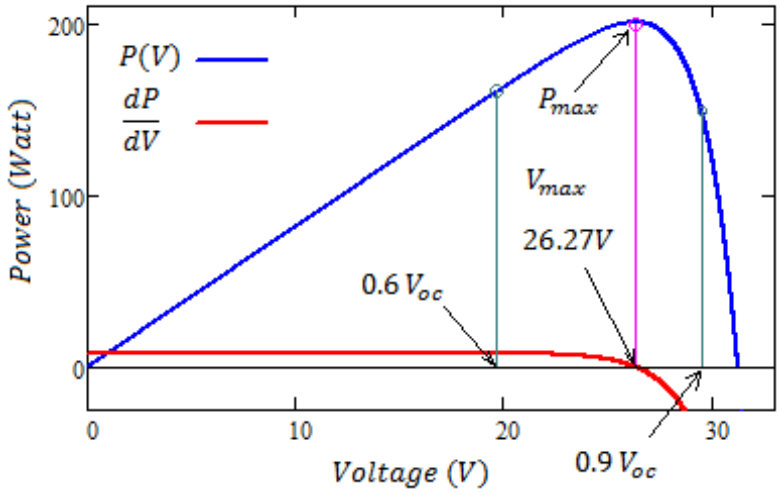



Figure 6. 9 P-V and $\frac{dP}{dV}$-V curves at STC

A bisection numerical algorithm is developed to solve Equation (6.10). The flow chart for the algorithm is shown in Figure 6.10 [84].

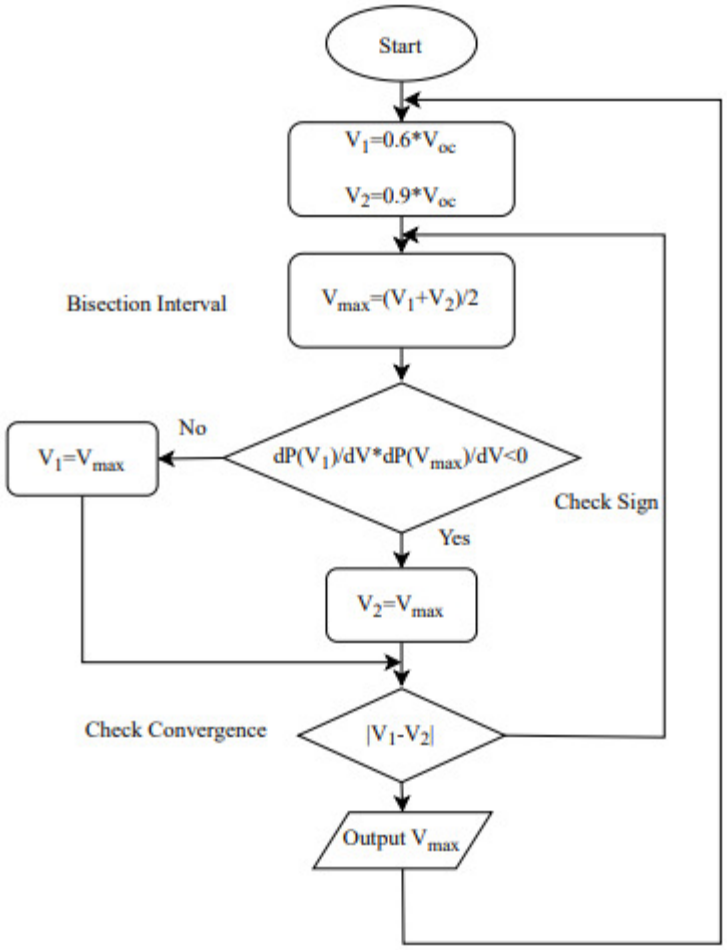



Figure 6. 10 Flow chart of the bisectional numerical algorithm

In order to implement the MPPT, the calculated output $V_{max}$ in the flow chart of the bisection numerical algorithm is used as input and compared with the actual output voltage of the PV model, as shown in Figure 6.11.

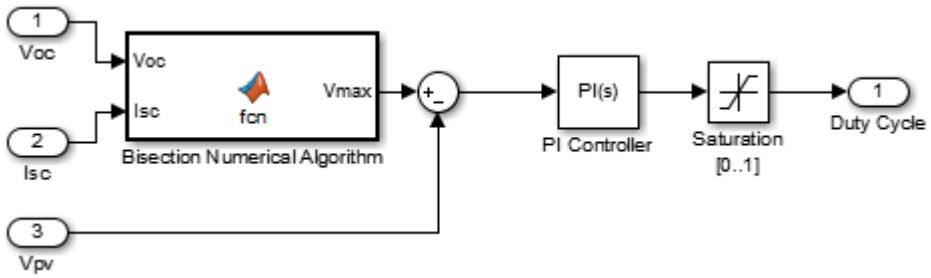



Figure 6. 11 Block diagram of the MPPT based on BNA

Although the BNA involves the assumption term ($e^{\left(q*\frac{V+0.9*I_{SC}*R_S}{a*N_S*K*T_{op}}\right)}$) in equation (6.10), in Appendix D, it is demonstrated that its tracking accuracy of maximum power is better compared to the FOCV and the FSCC methods.

### 6.4.3 Simulation Results of MPPT Based on BNA

Figure 6.12 shows the photovoltaic system connected to a resistive load through the renewable side DC-DC boost converter.

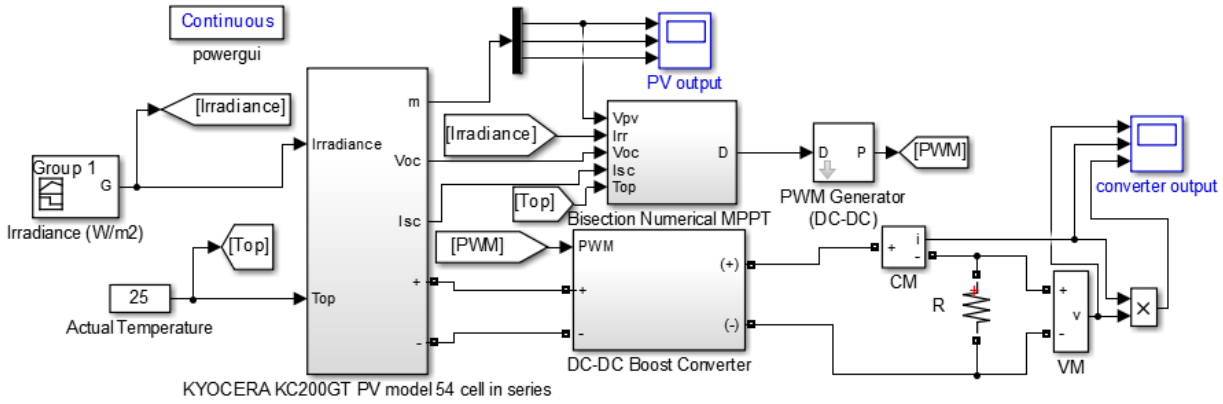
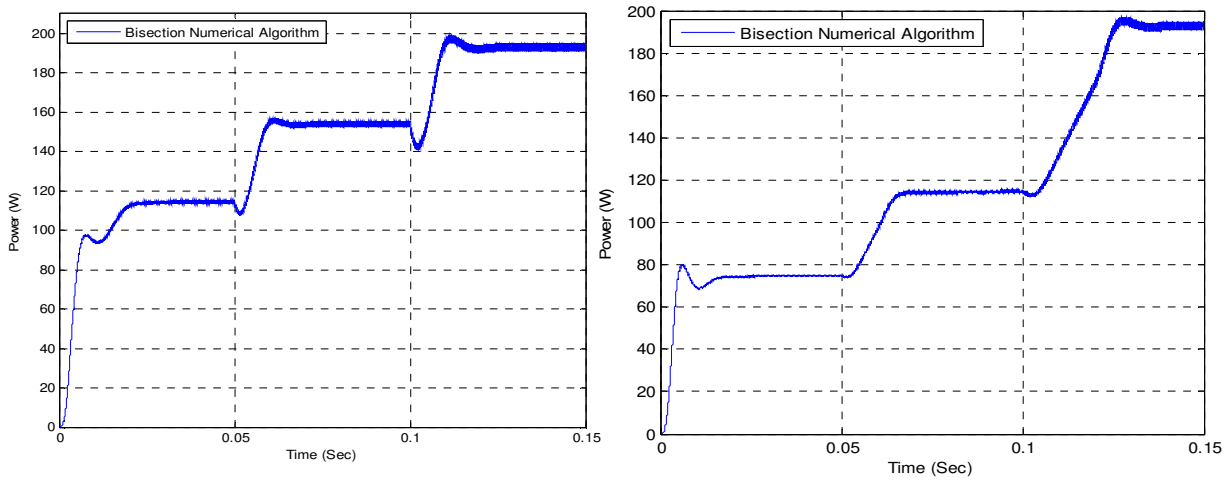



Figure 6. 12 Matlab/Simulink diagram of the photovoltaic system including the BNA for MPPT

In order to demonstrate the performance of the photovoltaic array and illustrate the steady-state tracking accuracy (TA) for the maximum power point, a step input and ramp input of the solar irradiation are implemented. These inputs provide conditions that are similar to climate change at the chosen location. The responses are shown in Figure 13 (a) and (b). In the step input case, during a 0.15 second simulation interval, three values of solar irradiations $600W/m^2$, $800W/m^2$, and $1000W/m^2$ are set as input, as shown in Figure 6.13 (a). Similarly, the ramp input case of the solar

irradiation is gradually changed for three values $400W/m^2$, $600W/m^2$, and $1000W/m^2$ as shown in Figure 6.13 (b). Both cases are performed at $25^oC$.




(a) Step input solar irradiance case (b) Ramp input solar irradiance case

Figure 6. 13 Performance of the MPPT based on BNA under step and ramp input of solar irradiation

The BNA calculates the setpoint $V_{max}$ based on the flow chart in Figure 6.10 and equation (6.10). The setpoint determines the point of the power tracking accuracy from the P-V curve. The result of the assumption term ($e^{\left(q*\frac{V+0.9*I_{SC}*R_S}{a*N_S*K*T_{op}}\right)}$) in equation (6.10) is negligible compared with the actual value, which is ($e^{\left(q*\frac{V_{mpp}+I_{mpp}*R_S}{a*N_S*K*T_{op}}\right)}$). The calculation of the error in the result is determined as:

$$Error = \frac{\boldsymbol{V_{mpp}}(based\ BNA)-\boldsymbol{V_{mpp}}}{\boldsymbol{V_{mpp}}} * 100\% \qquad (6.11)$$

For different values of the irradiance, the error in the maximum voltage point and tracking accuracy of the BNA is obtained, as summarized in Table 6.3 and Table 6.4, respectively. It can be observed that the assumption has a negligible effect on the maximum power point result, which is determined by the bisection algorithm.

Table 6. 3 Error in the result of BNA compared to the actual voltage at the maximum power point

| **Irradiance $W/m^2$** | **Actual MPP Voltage ($V$)** | **BNA MPP Voltage ($V$)** | **Error in the result of BNA%** |
|---|---|---|---|
| 400 | 25.65 | 25.58 | 0.25% |
| 600 | 26.05 | 25.99 | 0.23% |
| 800 | 26.26 | 26.18 | 0.30% |
| 1000 | 26.34 | 26.27 | 0.28% |

The results are used to evaluate their performance based on the steady-state tracking accuracy (TA) for the maximum power point are shown in Table 6.4.

Table 6. 4 Steady-state tracking accuracy for the MPPT based on BNA

| **MPPT Algorithm** / **Irradiance** | | **Bisection numerical algorithm** |
|---|---|---|
| 1000 $W/m^2$ | $P_{max}$ | 192.8 W |
| | TA % | 96.4 % |
| 800 $W/m^2$ | $P_{max}$ | 154 W |
| | TA % | 96.7 % |
| 600 $W/m^2$ | $P_{max}$ | 114.4 W |
| | TA % | 96.8 % |
| 400 $W/m^2$ | $P_{max}$ | 74.65 |
| | TA % | 96.8% |

As indicated in Table 6.4, the bisection numerical algorithm accurately tracks the voltage at the maximum power point, and hence the maximum power. The BNA is compared with the FOCV and FSCC method, and it indicates better TA in terms of extracting the maximum power, as shown in Appendix D.

### 6.4.4 Performance of Solar-PV System Conncetd to a Battery Storage System (BESS)

The proposed DC microgrid consists of two solar PV systems. Each solar-PV system, which has a rated power of 4 kW connected to the storage system of 35 batteries through a DC-DC renewable energy side converter. Since the selected voltage level at the load side converter is 48 V, the DC-DC renewable side converter is a buck converter. The dynamic model of each solar-PV system is represented by series and parallel modules of PV panels. The array consists of 10 string and each string modeled by two series of ALTE 200 watt 24 V poly solar panels. The parameters for the ALTE 200 watt 24 V poly solar panel are given in Appendix C. Furthermore, the parameters of the buck converter for each solar-PV system are given in Table 6.5. The PI controller parameters for the MPPT based on the BNA is 0.9 and 0.09 for the proportional and integrals gains, respectively [85].

Table 6. 5 Operating parameters of buck converter

| Parameters | Buck Converter I |
|---|---|
| Switching frequency $f_s$ | 25 KHz |
| Inductance $L$ | 0.3 mH |
| Capacitance $C$ | 6533.33 µF |
| Voltage $V$ | 73-35 V |

The BESS consists of 7 string, and each string is modeled by five series of MK 8L16LTP FLA lead-acid batteries. The parameters for the battery storage system are entered in the MATLAB/Simulink model, as given in Appendix C. The dynamic model of the MPPT based on the BNA for one solar 4 kW PV system is implemented in MATLAB/Simulink, and its schematic diagram connected to the BESS is shown in Figure 6.14.

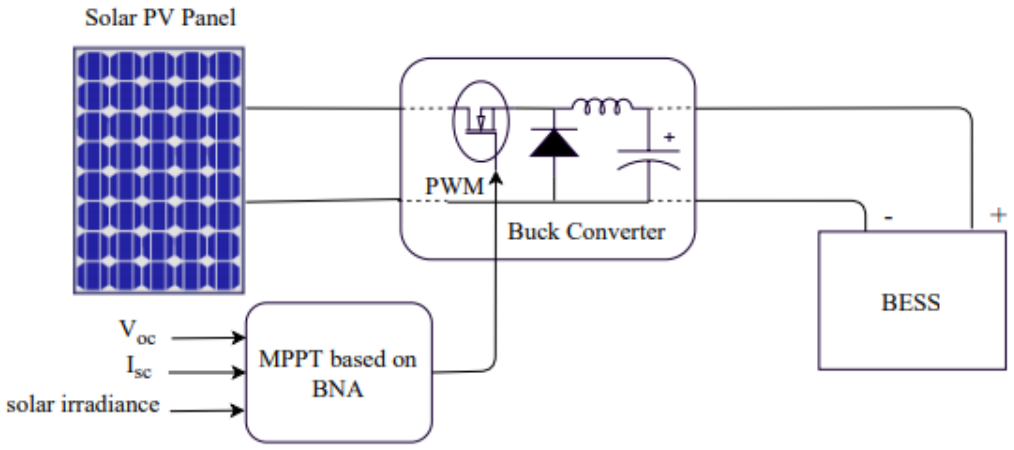



Figure 6. 14 Schematic diagram of the dynamic simulation model of MPPT base on BNA for solar-PV

The PV solar panel is simulated at a temperature of 25° C, and the solar irradiance data uses a signal builder block in the MATLAB/Simulink. Figure 6.15 shows the input solar irradiance, output voltage, current of the MPPT, and the output power of the MPPT. Different solar irradiance levels are applied with respect to the time as happens in real life. Thus, the BNA is investigated with the aid of a real-time simulator to check the dynamic response of the system. The solar irradiance, which is varied from 500 $^{W}/_{m^2}$ to 1000 $^{W}/_{m^2}$ Produces 1937 Watt and 3866 Watt, respectively. Thus, the MPPT based on the BNA tracks the maximum power efficiently, as shown in Figure 6.15. Furthermore, the charging voltage and current are within the acceptable values for charging the BESS. For input solar irradiance of 500 $^{W}/_{m^2}$ , the charging voltage and current are 33.8 V and 57.3 A, respectively. When a ramp increase of the solar irradiance from 500 $^{W}/_{m^2}$ to 1000 $^{W}/_{m^2}$ is applied, the charging voltage and current become 34.4 V and 112.3 A, respectively. Therefore, the charging voltage and current are within the limits of the acceptable values for charging lead-acid battery.

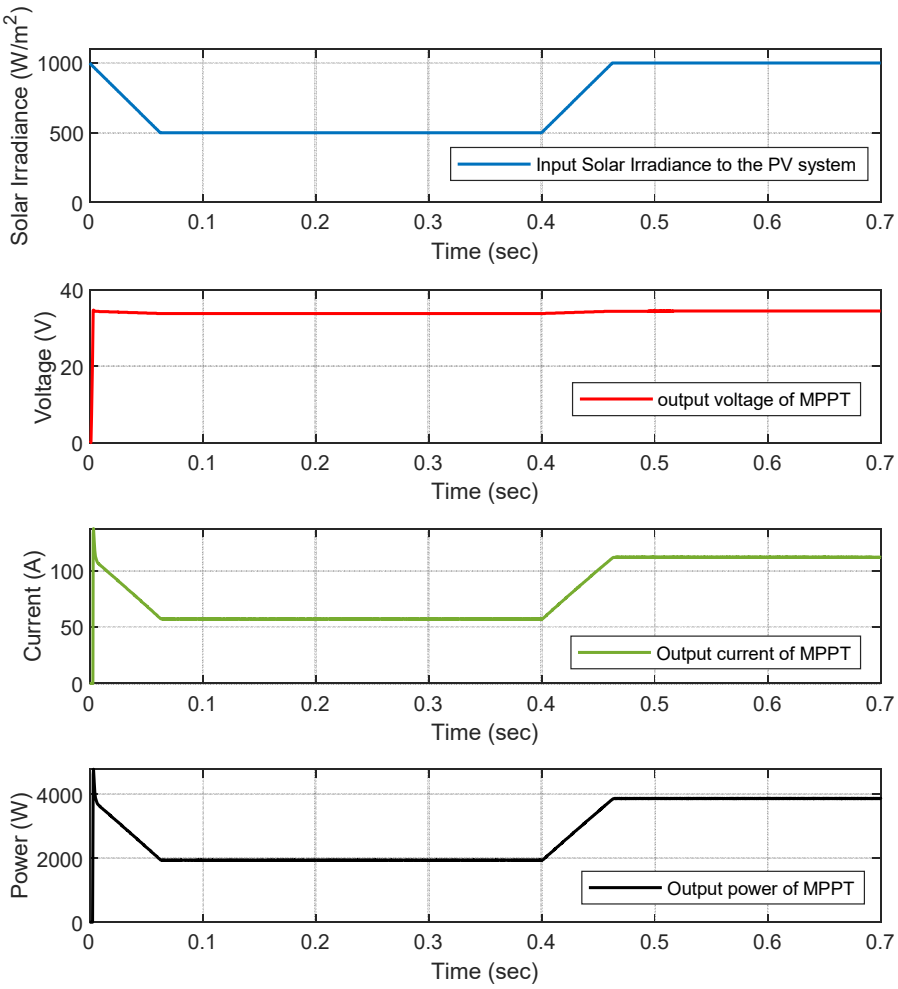



Figure 6. 15 Input solar irradiance, output voltage, output current, and output power of the MPPT based on the BNA for 4kW PV solar system

Moreover, the BESS charging mode, which includes the state of charge, charging voltage, and current for the input solar irradiance, is shown in Figure 6.16. The slope of the state of charge becomes sharper when the ramp increase of the solar irradiance is applied at 0.4 seconds. The ramp increase of the solar irradiance is from 500 $^{W}/_{m^2}$ to 1000 $^{W}/_{m^2}$.It indicates that there is more energy stored in the BSSE. The charging current also experiences a gradual increase from -57.3 A to -112.3 A. The negative sign of the charging current means that the battery is being charged. As

more charges are tapped into the battery, the charging voltage and the state of charge are increased, as shown in Figure 6.16.

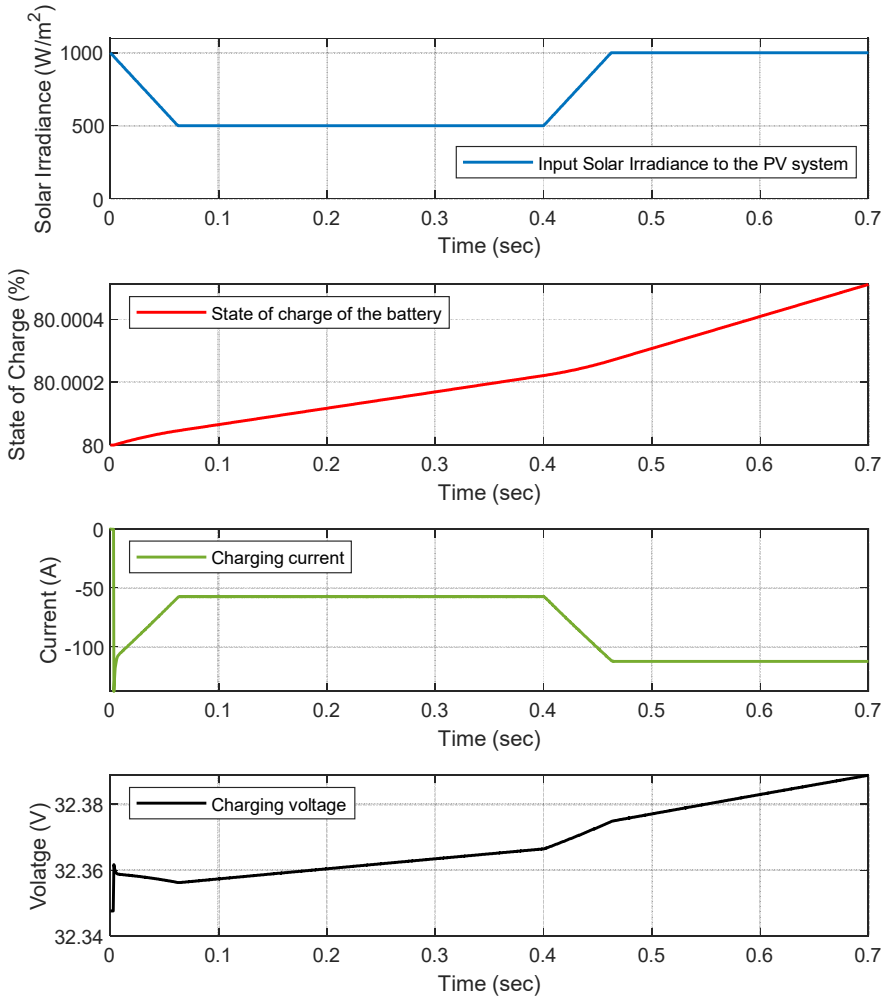



Figure 6. 16 Input solar irradiance, state of charge, charging current, and charging voltage of the BSSE

## 6.5 Performance of the Solar-PV Array connected to the BESS and the Load Side Parallel-connected DC-DC converters

The performance of the solar-PV connected to the BESS and the two parallel-connected DC-DC converters under various different operating scenarios is presented in this section. The schematic

diagram of the system shown in Figure 6.17 represents a standalone DC microgrid. It consists of two solar-PV systems, two buck converters, two BESSs, and two boost converters. Each buck converter of the renewable side converters extracts the maximum power and charges the battery for various conditions of solar irradiance. The two boost converters are connected in parallel to the PCC, and their objectives are to maintain the voltage at the PCC and share the load current equally. The battery side converters are connected in parallel to a common DC bus through different cable resistances. The values of cable resistances are chosen based on the operating voltage [86]. For 48 V systems, if the system's Ampere and power are 45A/2520W, the type of cable can be a wire gauge of 8. Furthermore, this type of cable was chosen with a maximum length of 78 ft. However, the cable resistances is selected to have values of 0.02 and 0.01 Ω for boost converter I and II, respectively. The selection is with a limited range of voltage regulation and power losses. Since the cable resistances have different values, the improved droop method is used to achieve equal load current and maintain the voltage at the PCC at 48 V for different load conditions.

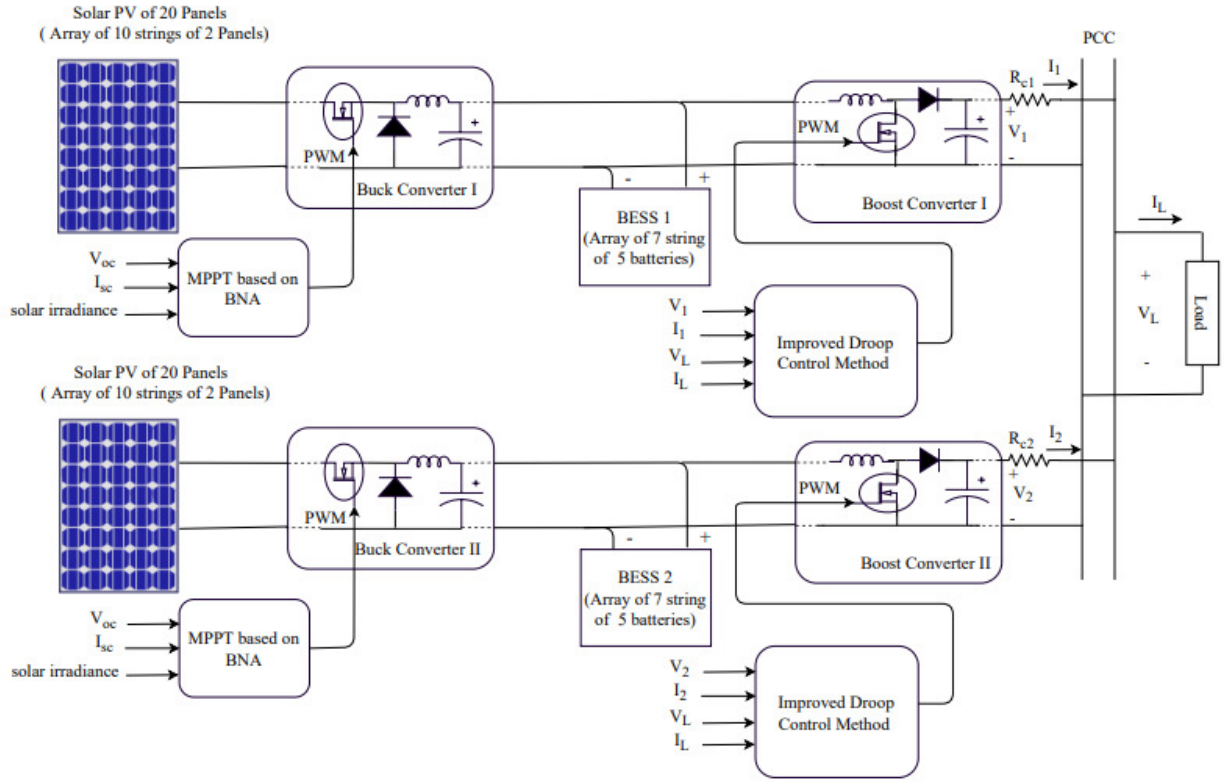


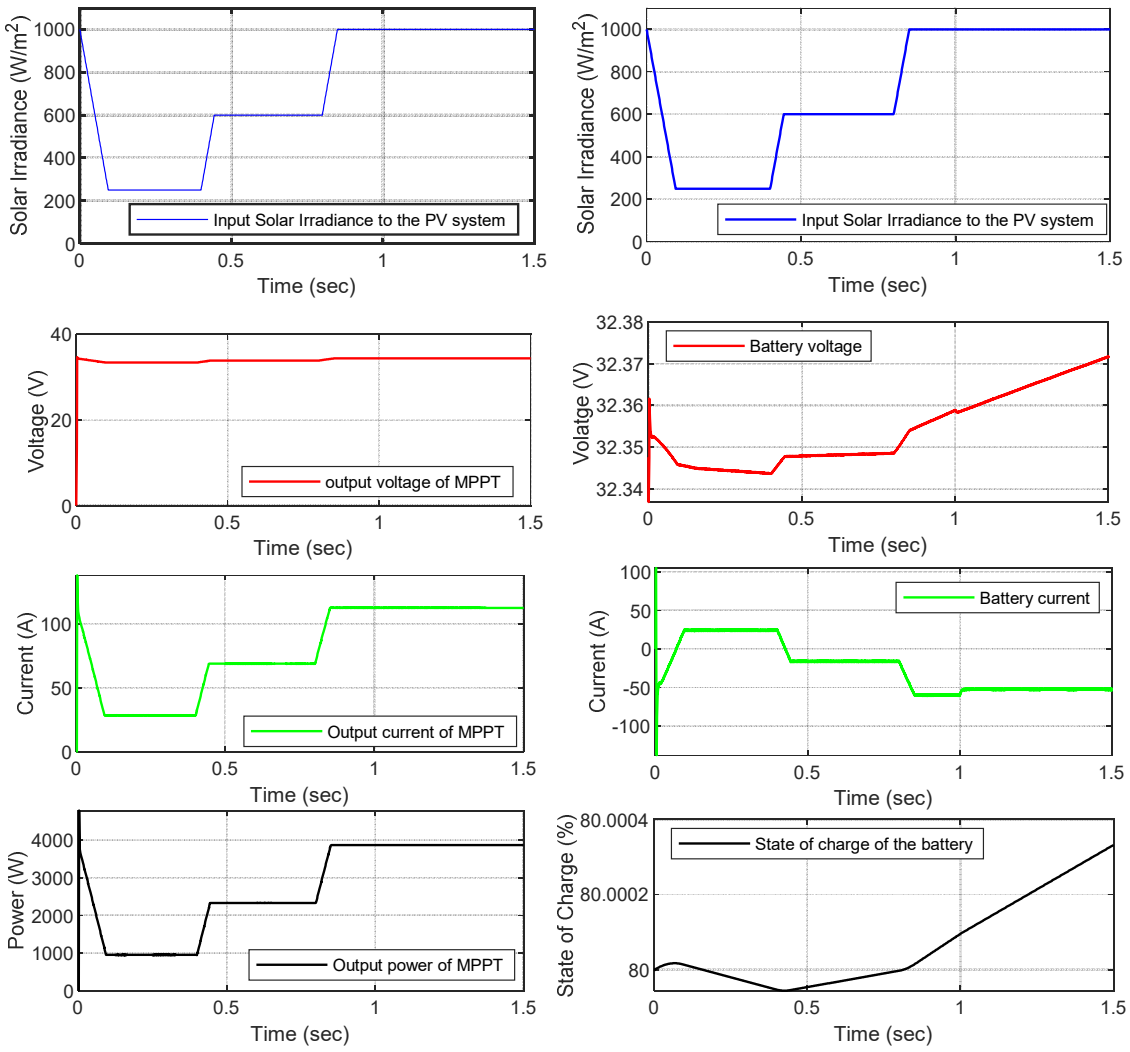

Figure 6. 17 schematic diagram of standalone DC microgrid

The two boost converters shown in Fig. 6.17 have mismatches in the parameters as summarized in Table 6.6. The SISO Tool in MATLAB is used to tune the PI controller for the voltage loop and current loop. The proportional and integral gains for the outer control loop are 0.586 and 586.24, respectively. Furthermore, the proportional and integral gains for the inner control loop is 0.042 and 20, respectively.

Table 6. 6 Parameter of load side converters

| **Parameters** | **DC-DC Boost Converter I** | **DC-DC Boost Converter II** |
|---|---|---|
| Switching frequency $f_s$ | 25 KHz | 25 KHz |
| Inductance $L$ | 0.27 mH | 0.244 mH |
| Capacitance $C$ | 2759.55 µF | 3035.504 µF |
| Voltage $V$ | 30-48 | 30-48 |

The operating scenarios are developed considering different solar irradiance and different load conditions. This case study is associated with the absolute DC load. Each PV system of 4 kW is connected to BSSE through the solar-side DC-DC buck converter, which tracks the MPPT based on the BNA. The initial state of charge of the BSSE is assumed to be 80%, and the solar irradiance data is provided for each PV system using a signal builder block in the Simulink. The MPPT for each 4 kW PV system is used to track the highest power during the various conditions for the input of the solar irradiance, as shown in Figure 6.18. The input irradiance data is changed in a shape of ramp function, and its different values are 250 $^{W}/_{m^2}$, 600 $^{W}/_{m^2}$, and 1000 $^{W}/_{m^2}$. The different solar irradiances are applied in sequences at 0.4 and 0.8 seconds. In this study, the mismatch in the parameters associated with the load side parallel DC-DC boost converters in Figure 6.17 is 10 %. Figure 6.18 shows the responses at various points in the system for change input irradiance over 1.5 second simulation time.



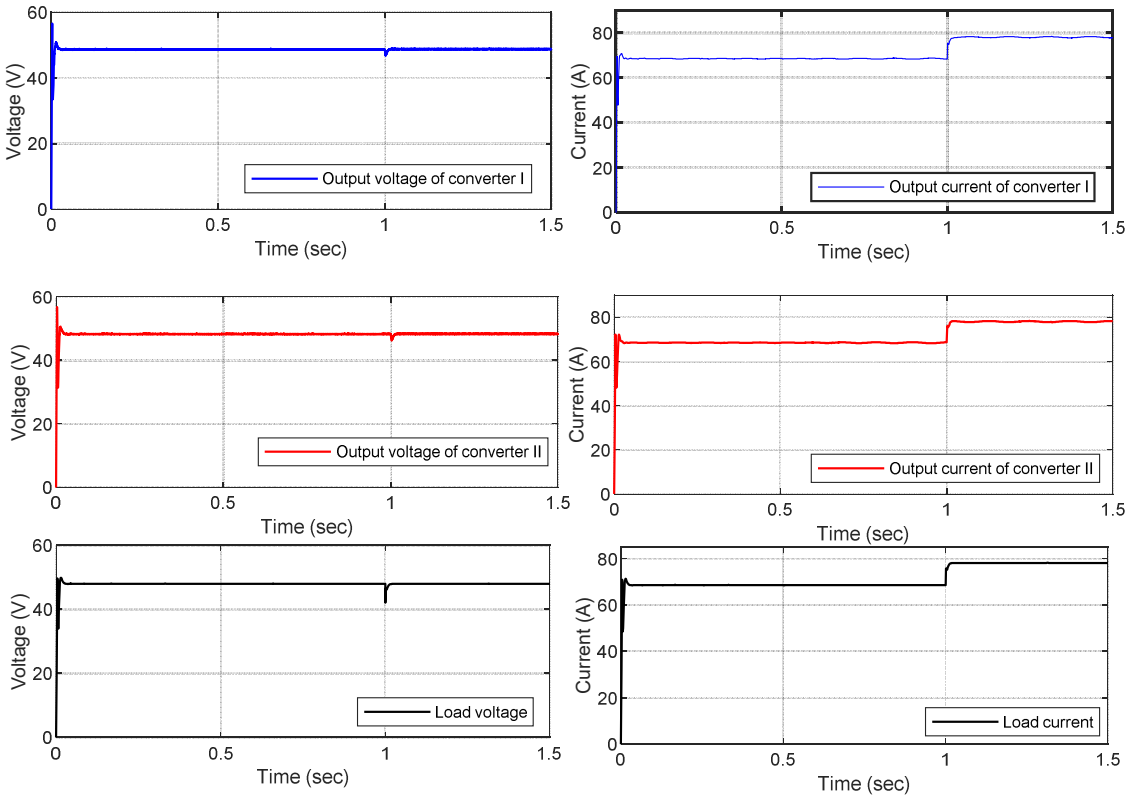

(a) (b)

Figure 6. 18 Response at solar side converter (a)Input solar irradiance, output voltage, output current, and output power of the MPPT based on the BNA for 4kW PV solar system (b) Input solar irradiance of the 4 kW PV System, voltage of the battery, battery current, and the state of charge

As can be seen in Figure 6.18 (a), the power production of each 4 kW PV system is variable in terms of time. The output power depends on the solar irradiation input data. According to the interval of 250 $W/m^2$, the power produced by the two 4 kW PV systems is lower than the DC load

demand. This causes a decrease in the state of charge of the BSSE, as shown in Figure 6.18 (b). The battery current is a positive value since the BSSE contributes to the load demand, and the battery voltage is declining at the same time. However, for the intervals of 600 $^{W}/_{m^2}$ and 1000 $^{W}/_{m^2}$, the power production of the two 4 kW PV systems is higher than the DC load demand. This results in an increase in the state of charge of the BSSE, but for 1000 $^{W}/_{m^2}$ the state of charge is increasing with a higher rate compared to the 600 $^{W}/_{m^2}$. The higher rate of the charge is due to the higher power production from the two 4 kW PV systems at the same level of load demand. The battery current shows a negative sign since the battery is in charge mode. In the charge mode, the battery voltage level increase, as shown in Figure 6.18 (b). When the solar irradiance is 1000 $^{W}/_{m^2}$, the PV system produces 3865 Watt, which is the highest power and closer to its rating at almost 4 kW. At the maximum power point, the output voltage and current with values of 34.4 V and 112.3 A are applied to the BSSE. For various solar irradiance conditions, the PV array cannot produce less than the battery charging voltage and higher than the charging current.

There are two boost converters that regulate the DC voltage of the battery to the common DC bus voltage (PCC), as shown in Figure 6.17. The rated voltage of the PCC has a value of 48 V. The case is simulated with previous considerations and a step increase in the load at 1 second. Therefore, the voltage of the common DC bus, the output voltage of each converter, load current sharing and the total load current are shown in Figure 6.19 (a), and (b), respectively.




(a) (b)

Figure 6. 19 Response of the parallel-connected boost converter for various load conditions (a) Output voltage of converter I and II and voltage at the common DC bus (b) Load current sharing accuracy and the total load current

In the proposed control method, the voltage of the common DC bus is restored according to the estimated voltage at the point of common. Therefore, for a step increase in the DC load, the voltage at the load or the common DC bus is maintained at 48 V. However, for the first interval, the output voltage of converter I and II are 48.65 V and 48.3 V, respectively. When the additional load is connected, the output voltage of the converter I and II are 48.75 and 48.3 V, respectively. Furthermore, the current sharing accuracy is achieved in the improved droop method, while different cable resistance and mismatch of parallel DC-DC boost converters are presented. It can

be observed from Figure 6.19 that the load current is shared equally between converter I and II. The initial loading current of 68.6 A is shared equally with the value of 34.3 A for each converter. When the load is increased to draw a current of 78.1 A, each boost converter contributes to the total load current with 39.05 A.

## 6.6Performance of the Solar-PV Array connected to the BESS and the Load Side Parallel-connected DC-DC converters with a Partial AC Load

In this section, a study case is developed by considering a partial AC load as shown in Figure 6.20. It is used to verify the performance of the improved droop method with partial AC load. It is implemented in MATLAB/Simulink environment with the presented DC microgrid along with partial AC load.

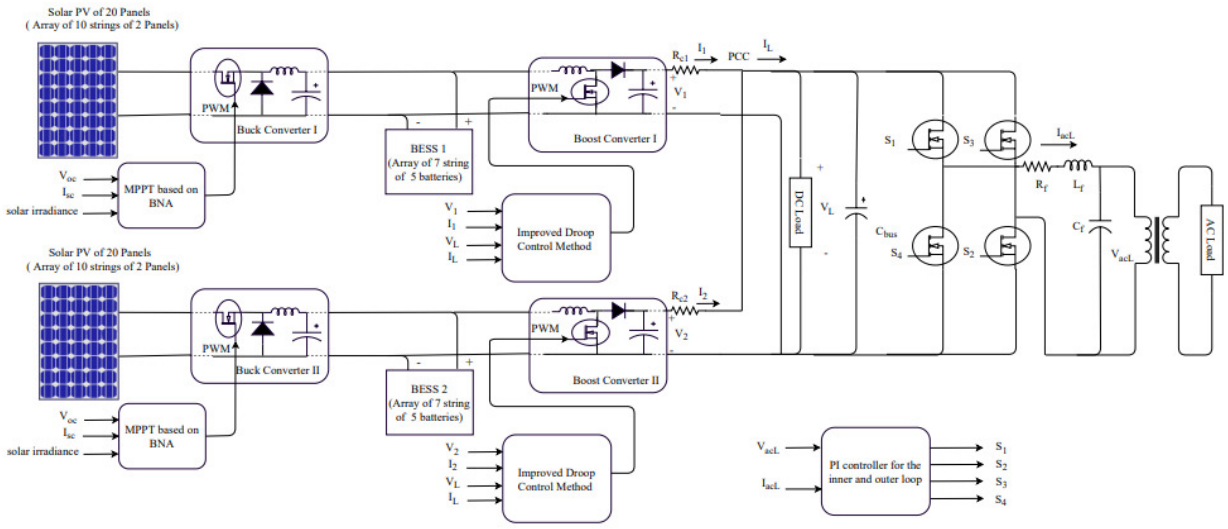



Figure 6. 20 Schematic diagram of standalone DC microgrid with partial AC load

The DC/AC inverter parameters are presented in Table 6.7 [87], [88]. The proportional and integral gains of the outer voltage control loop are 10 and 1, respectively. For the inner current loop, the proportional and integral parameters are 20 and 1, respectively [89,90].

Table 6. 7 Simulation testing parameters of DC/AC single phase Inverter

| Parameters | Buck Converter I |
|---|---|
| DC bus Voltage $V_{dc}$ | 48 V |
| frequency $f_s$ | 25 KHz |
| $r_L$ | 0.03 Ω |
| Filter Inductor $L$ | 6.5407 µH |
| Filter Capacitor $C$ | 1000 µF |

The same input solar irradiance of the previous case is provided for the model in Figure 6.20, but there is an additional AC load. The initial AC load has a value of 100 Watt, and a step increase of 130 Watt is applied at 0.5 seconds. The load sharing current and voltage restoration at the PCC is achieved by the improved for the parallel-connected DC-DC boost converter. Boost converter I and II are connected to the common DC bus through different cable resistances of 0.02Ω and 0.01Ω, respectively. While the AC load is connected through DC/AC inverter, the DC bus voltage is maintained at a constant voltage, and both boost converters share the load current equally. The input solar irradiation data to the two 4 kW PV system model is shown in Figure 6.21.

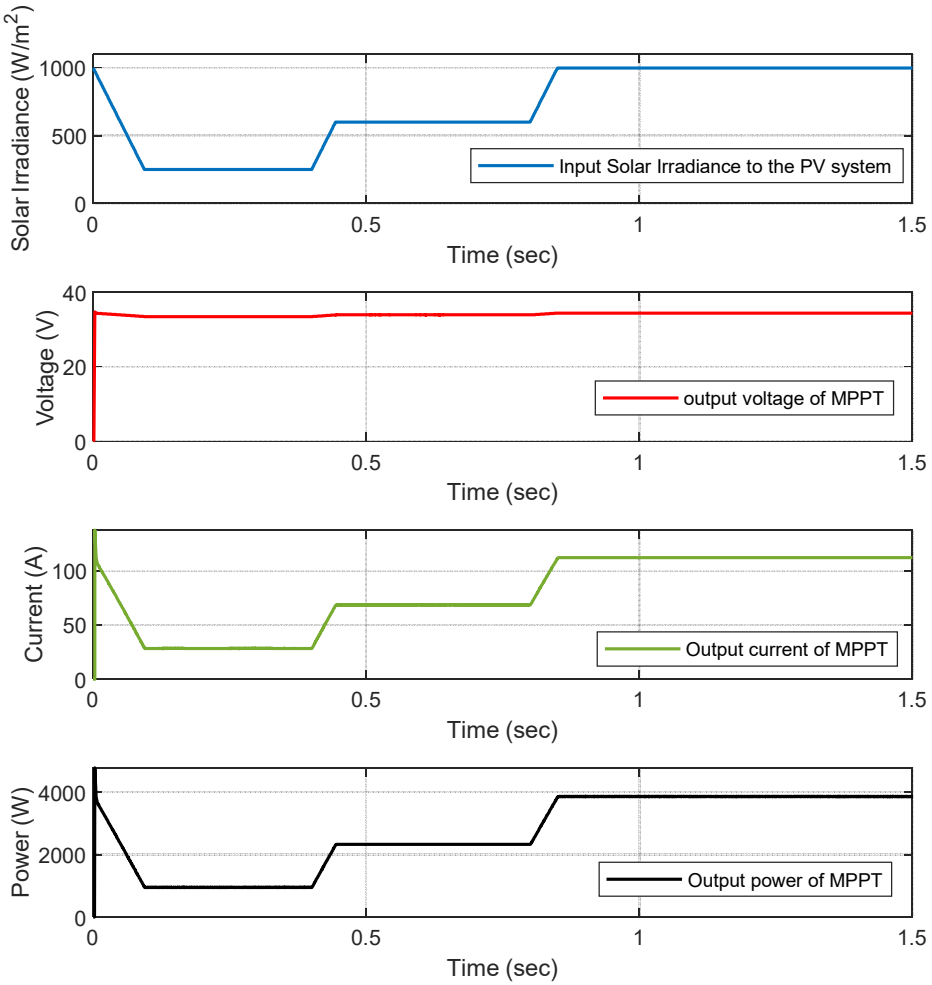



Figure 6. 21 Input solar irradiance, output voltage, output current, and output power of the MPPT based on the BNA for 4kW PV solar system

For the two 4 kW PV solar system, the simulation is performed for three different values of solar irradiation, which are at 250 $^{W}/_{m^2}$, 600 $^{W}/_{m^2}$, and 1000 $^{W}/_{m^2}$. It can be observed from Figure 6.21, when an increase of solar irradiation is applied, the produced power from the 4 kW PV system is increased. Table 6. 8 summarizes the maximum power produced for the provided solar irradiation.

Table 6. 8 MPPT tracking for different solar irradiation

| Solar irradiance ($W/m^2$) | Voltage (V) | Current (A) | Power (W) |
|---|---|---|---|
| **250** | 33.46 | 28.4 | 950 |
| **600** | 33.903 | 68.7 | 2330 |
| **1000** | 34.4 | 112.3 | 3865 |

The output voltage and current of the MPPT based on the BNA are within the limits of charging voltage and current for the BSSE. The state of charge, battery voltage, and currents are shown in Figure 6. 22.

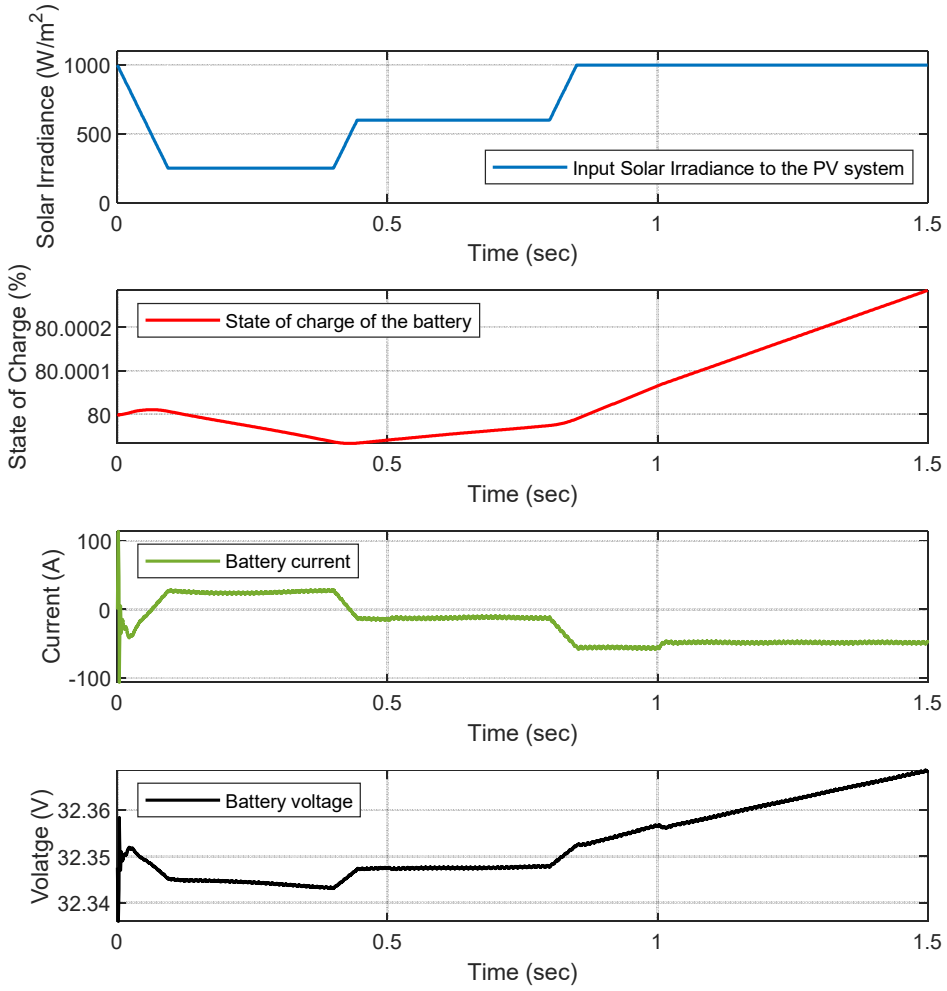



Figure 6. 22 input solar irradiance, and state of charge, battery voltage and current of the BSSE

It can be observed that the state of charge and battery voltage is decreasing for the first interval of the loading, as shown in Figure 6.22. The load demand of the first interval is higher than the highest extracted power from the two 4 kW PV systems. There is extra power, which is provided by the BSSE. This can be observed by the positive sign of the battery current, as shown in Figure 6.22. However, since the solar irradiance is increased at 0.4 seconds for the simulated case, the two 4 kW PV system provides higher power than the load demand. The observation of this transition can be seen in the battery current at 0.4 seconds. The battery current becomes a negative value, and the battery state of charge and voltage are increased. However, since the AC is increased at 0.5 seconds, there is a small change in the battery voltage and current. Furthermore, an additional DC load is applied at 1 second. It causes a slight change in the battery voltage and current, as shown in Figure 6.23. The battery side converters, which are the parallel-connected DC-DC boost converters, are responsible for sharing the load and regulate the common DC bus at its rated value of 48 V. The output voltage of each converter and the voltage at the common DC bus are shown Figure 6. 23. It can be observed that the load voltage or the common DC bus voltage is maintained at a constant value while the applied AC and DC load are increased at 0.5 and 1 second, respectively. However, As can be seen in Figure 6.23, there is a ripple in the output voltage of each converter and the voltage at the common DC bus. The small ripple is associated with the AC load, and it has a sinusoidal waveform of the second harmonic of the fundamental of 60 Hz. When the AC load is increased at 0.5 seconds, the ripple in DC bus, which is the second harmonic of the fundamental AC waveform, is increased.

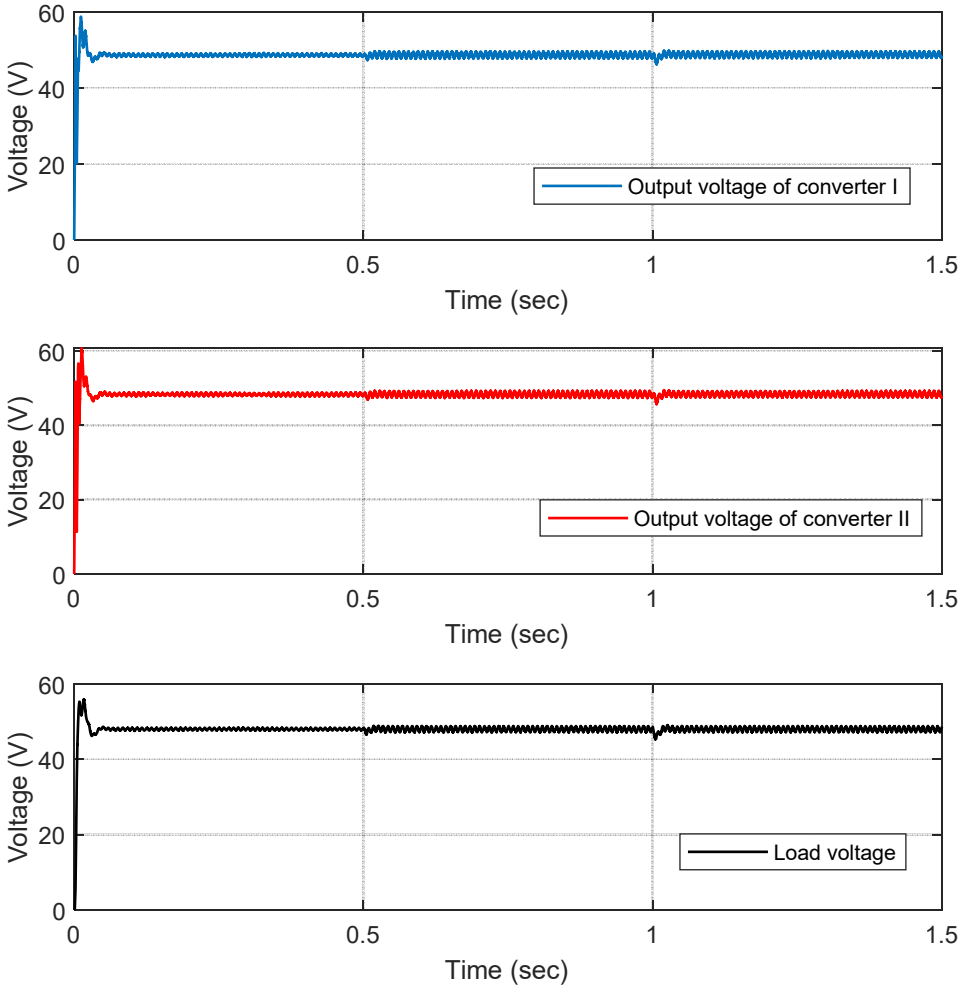
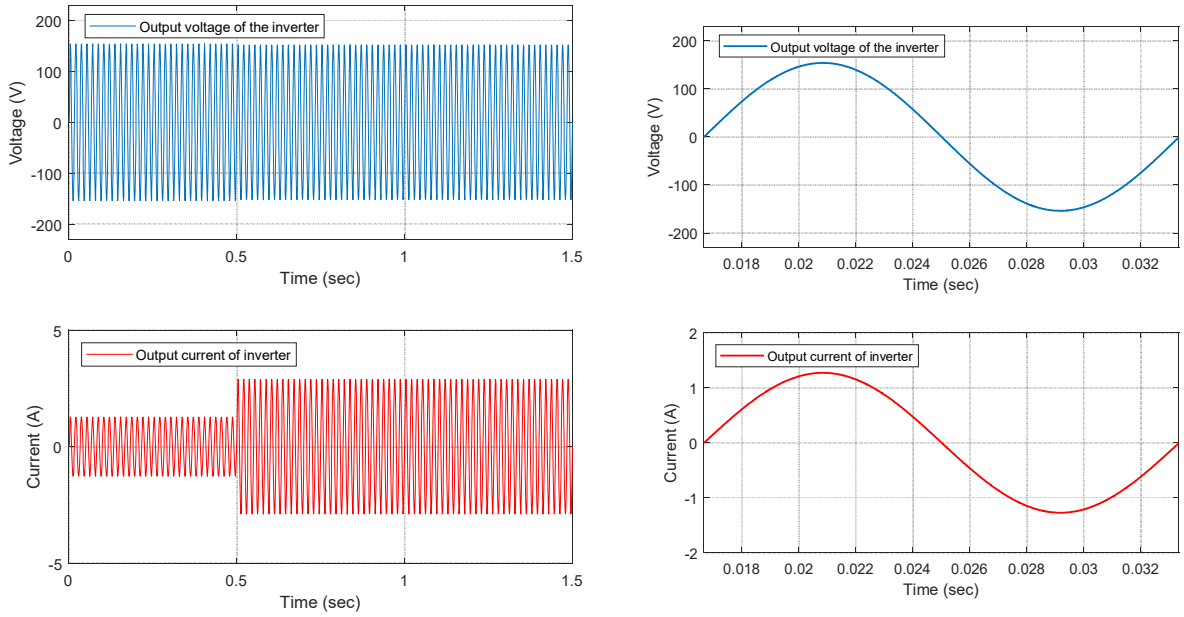



Figure 6. 23 Output voltage of converter I and II and the load voltage

The AC load waveforms of the voltage and current indicate the increase in the load at 0.5 seconds, as shown in Figure 6.24 (a). Furthermore, Figure 6. 24 (b) shows one cycle of the output waveforms of the voltage and current. The observation of increasing AC load can be seen clearly from the voltage of DC bus, and the DC current drawn from the parallel converter. The observation is associated with the increase in the ripple of the DC bus voltage and current, as shown in Figure 6.23 and Figure 6.25.




(a) (b)

Figure 6. 24 Output voltage and current of the AC load

In the DC side of the inverter, the current drawn by the single-phase inverter from the dc side is not constant, but it has a second harmonic component (of the fundamental frequency at the inverter output). The form for the second harmonic is given as [91]

$$I_{s2} = \frac{V_o * I_o}{V_d} * \cos(2\omega_1 - \phi) \tag{6.14}$$

Where $\omega_1$ is the fundamental frequency $(2 * \pi * f_1)$, $\phi$ the power factor, $V_o$ is the output voltage of the inverter, $I_o$ is the output current of the inverter, and $V_d$ is the voltage of DC bus.

However, the load current sharing is achieved by the implementation of the improved droop method, as shown in Figure 6.25. For the first interval of the loading, the output currents of boost converters I and II have the same value of 35.5 A, as shown in Figure 2.25. Similarly, when the load is increased at 0.5 and 1 seconds, the load current is shared equally between the two boost

converters. Each converter supplies 37 A when a step increase in the AC load is applied at 0.5 seconds. Furthermore, boost converter I and II contribute to the total load current with a current of 42 A when a step increase in the DC load is applied at 1 second.

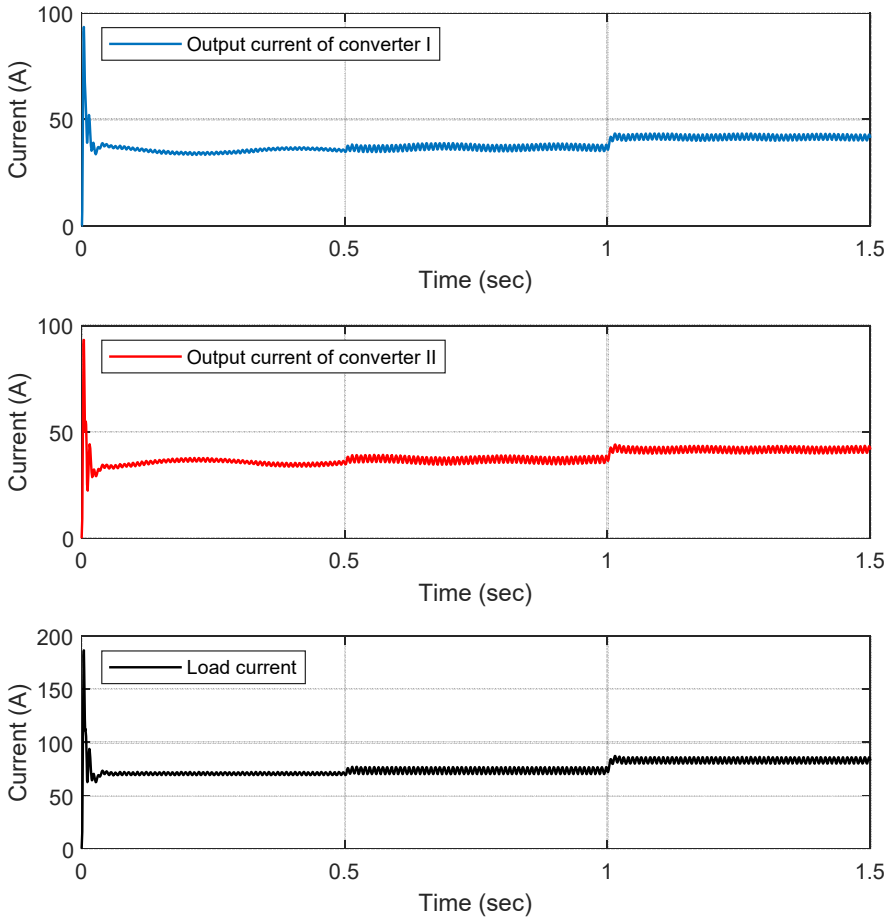



Figure 6. 25 Load current sharing accuracy and the total load current

## 6.7 Summary

In this chapter, the improved droop method presented in Chapter 5 is implemented in a model residential standalone DC microgrid and a DC microgrid with partial AC load. Step-by-step

development of the model residential system is presented. The system incorporated the algorithms for the improved droop method and the bisection numerical method developed in the previous chapters to evaluate the performance of the MATLAB model of a residential system. The main aim of using the improved droop method is to ensure equal load current sharing and voltage restoration at the PCC. The MPPT based on the BNA extracts the highest power for various weather conditions. The proposed MPPT based on the BNA method provides high tracking accuracy. The two PV systems of 4 kW are used to charge two BSSEs. The two BSSEs are connected to the PCC through different cable resistances. Two boost converters, which have mismatches in parameters, are used to regulate the voltage at the PCC to the rated value of 48 V. The performance of the improved droop method is verified with the residential standalone DC microgrid. The load is shared equally between the parallel converters, and the voltage of the 48 V is maintained while different solar irradiances and load conditions are applied.

# Chapter 7

# Conclusion and Future Work

Connecting DC-DC converters in parallel is very important in an application such as standalone DC microgrids because the parallel configuration provides serval advantages compared to a single large power converter supply. The parallel configuration increases the output power capability by connecting two or more DC-DC converters. Two small DC-DC converters can be more efficient compared to a single large unit. Lowering the power of the DC-DC converters can operate them at a higher frequency, which reduces the size of the components. Two small sizes of DC-DC converters in a place of a single large converter can spread the heat dissipated across a larger area, which increases the reliability of the system. The parallel operation provides modularity, which ensures expanding the system by adding more DC-DC converters in parallel when the load demand grows. Operating parallel-connected DC-DC converters offer flexibility for the online replacement of the defective converter. The parallel configuration provides a non-interrupting power supply, which is an essential requirement of standalone DC microgrid. An improved droop control method for controlling parallel-connected DC-DC converters is proposed and investigated in this thesis. Compared to the other improved droop methods, the proposed method eliminates the communication network between parallel converters and simplifies the control scheme by providing a local controller. Furthermore, the proposed method provides a precise load current sharing, an improvement in the voltage regulation, and minimization of circulating current.

## 7.1 Conclusion

The main drawbacks of the conventional droop method are associated with poor load current sharing, drop-in dc grid voltage due to the droop action, and circulation currents due to the mismatches in the output voltage. Several modified and improved droop methods have been presented in the literature to overcome the mentioned drawbacks. However, the majority of the improved method relies on a low bandwidth communication network to enhance the load current sharing and voltage regulation of the parallel converters. Thus, an improved droop method is presented in this research to overcome the conventional droop method drawbacks. In the first part, the relationship between synchronous switching for two different sizes of parallel-connected DC-DC boost converters and the initiation of circulating current is investigated. The synchronous switching is achieved based on an optimized PI controller. The synchronous switching for different sizes of parallel converters leads to improve the dynamic response of the parallel-connected boost converter. It eliminates the circulating current between parallel converters and minimizes the ripple in the output current for each converter. In the second part, the aim of using synchronous switching and load current sharing based on the droop method is to implement the proposed modified droop method taking into account the cable resistances. The state-space averaging technique is also developed based on synchronous switching. The state-space averaging model is used to study the transient response for the two parallel-connected boost converters with different cable resistance values. The MATLAB simulation model is used to carry out the dynamic response for the two different sizes of parallel-connected converters with different cable resistances. The results indicate that the cable resistances lower the overshoot and enhance the dynamic response of the system.

Furthermore, the control algorithm, which is introduced in Chapter 4, supervises the modified droop method to overcome the mismatches in the parameters of parallel converters. The additional control loop provides an adjustment for the voltage setpoint locally. The voltage adjustment is based on the percentage of the current of each converter to the total load current. The experimental validation of the proposed algorithm is verified. The two boost converter laboratory prototype uses the modified droop method with cable resistances implementation. The load is shared precisely between the parallel-connected converters. However, the differences in the cable resistances and the voltage drop issues in the modified droop is solved with the improved droop method in Chapter 5. The improved droop method introduces two gains, which are the virtual droop gain (VDG) and The adaptive voltage control gain (AVCG). The VDG overcomes the issues of the differences of cable resistances, and the AVCG restores the voltage at the PCC at its rated value. The practical solution for proper load current sharing is the VDG. The VDG is determined based on compensating the difference in the cable resistances. Moreover, the voltage at the common DC bus can be regulated synchronously to overcome the issue of voltage drop due to the droop characteristics. The AVCG in the load regulation characteristics, which are presented in Chapter 5, can shift the setpoint locally and synchronously. The AVCG ensures a constant voltage at the PCC under different loading conditions. Thus, the fixed voltage at the common DC bus, which can be achieved, eliminates the circulation current and improves the voltage regulation for the two parallel-connected boost converters. Experimental validation is presented to verify the effectiveness of the improved droop method. Two small scall boost converter is used in the lab using dSPACE 1104. The experimental results match the simulated cases based on MATLAB/Simulink model.

Chapter 6 implement the improved droop method in a standalone DC microgrid powered by a PV system. Furthermore, a MPPT based on the BNA is also presented. The BNA improves the steady-state tracking power accuracy for a PV system. Finally, an implementation MATLAB model for the outcomes of the improved droop method along with the MPPT based on the BNA is utilized in a residential DC microgrid power by a PV system. The results verified the load current sharing and voltage regulation of the proposed method.

## 7.2 Contribution of the Research

The specific and significant contributions of this research are categorized in the same sequence as presented in the chapters as follows:

1. The relationship between the synchronous switching and the initiation of circulation current for different sizes of parallel-connected converters is discussed in Chapter 3. The results show that a small mismatch in the switching pattern between parallel-connected boost converters can initiate a circulating current. An optimized PI controller is presented to ensure synchronous switching for the parallel-connected converters. The concept of an optimized controller is to overcome the issue of different delays in the control loop, which might cause the initiation of circulating current. Furthermore, a modified droop method based on master control is introduced. The proposed method implements the synchronous switching between parallel-connected converters, which have mismatches in their parameters. The method ensures load current sharing based on the converter power rating.

   The results of the relationship between the synchronous switching and the initiation of circulating current were presented at The *17th annual IEEE Canada Electrical Power and Energy Conference (EPEC 2017)* in Saskatoon, Saskatchewan, Canada [57]. The method of

modified droop control based on master control was published in *Journal of Electrical and Computer Engineering, Hindawi* [58].

2. The modified droop method with cable resistances implementation is introduced in Chapter 4. The modified droop includes the cable resistance as part of the load regulation characteristics for each converter. This concept allows the control loops for each converter to estimate the voltage setpoint locally. State-space averaging techniques, which consider the synchronous switching is used to study the effect of the cable resistance on the dynamic response of the parallel-connected converters system. Simulation of the parallel-connected converter based on the modified droop verifies the results from the state-space averaging technique. Furthermore, a control algorithm is presented to ensure equal load current sharing between parallel converters. The algorithm compares the output current for each converter with the total load current. The result of this comparison modifies the violate setpoint for each converter to achieve a precise load current sharing. Experimental results of the modified droop and the proposed control algorithm is presented to validate the MATLAB/Simulink model. The experimental prototype is used to test the proposed control algorithm based on the modified droop with cable resistance implementation.

   The results of the modified droop method with cable resistances implementation were presented at *the 18th annual IEEE Canada Electrical Power and Energy Conference (EPEC 2018) in Toronto, Ontario, Canada* [61]. The results of the control algorithm for equal current sharing between parallel-connected boost converters were published in the *Journal of Electrical and Computer Engineering, Hindawi* [63].

3. The improved droop control method is presented in Chapter 5. There are two gains in the improved droop method. The first gain, which is the VDG is used to compensate for the

differences in the cable resistances. The second gain, which is the AVCG is utilized to restore the PCC voltage to its rated value. The improved droop method used the control algorithm loop as well. The improved droop method eliminates the low bandwidth communication for transferring data between the parallel converters. The improved droop method decentralizes the control of the parallel-connected boost converters. An experimental prototype of the improved droop method is used to validate the MATLAB/Simulink Model.

4. Dynamic Modeling of residential DC microgrid, which is powered by PV system, is developed in Chapter 6. Since PV system is used as a renewable source of energy, a MPPT based on the BNA is proposed. The detail of the comparison between the presented BNA and the two methods of the FOCV and FSCC is carried out based on MATLAB/Simulink. The BNA provides better tracking accuracy compared to the FOCV and FSCC method. However, the DC microgrid employees parallel configuration of DC-DC converters to supply the electrical load. The parallel-connected converter uses the improved droop method to provide a precise load sharing and voltage restoration at the PCC. The DC microgrid model in MATLAB/Simulink environment is investigated using various load conditions and solar irradiances. The load current sharing and voltage restoration are achieved based on implementing the improved droop method.

   The results of the MPPT based on the BNA and its comparison with the FOCV and FSCC were presented in *the 16th annual IEEE Canada Electrical Power and Energy Conference (EPEC 2016) in Ottawa, Ontario, Canada* [83].

   The results of the improved droop control method, along with its application of residential standalone DC micrgrid is under the preparation for the submission.

## 7.3 Future Work

While the thesis proposes the improved droop method to overcome the issue of unequal load current sharing, voltage regulation, and circulation current, and eliminate the need of low bandwidth communication link between parallel converters, the researcher may find other way to extend the proposed work. Some of the suggestions to improve the utilization of the improved droop method.

- In the improved droop method, the VDG is determined based on the presented cable resistances in the parallel-connected converters system. The improvement in this part is associated with presenting an adaptive PI controller, which might use the PCS in order to adjust the virtual droop gain.
- The AVCG is used in the improved droop method to restore the voltage at the PCC to its rated value. This part can be enhanced by using an adaptive PI controller, which might be used to modify the voltage setpoint locally to restore the voltage at the PCC.
- For DC microgrid, balancing the state of charge for the battery energy storage systems (BESSs) with different capacities is very important. The method of improved droop control can be manipulated to balance the state of charge of BESSs with different capacities. This increases the reliability of PV-system with different capacities of the BESSs.

# Appendix A

## State Space Averaging Technique for Boost Converter

The equivalent circuit of the basic boost converter considered in this work is shown in Figure A.1. The operating condition for the boost converters can be classified into two modes, which are Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM) [52].

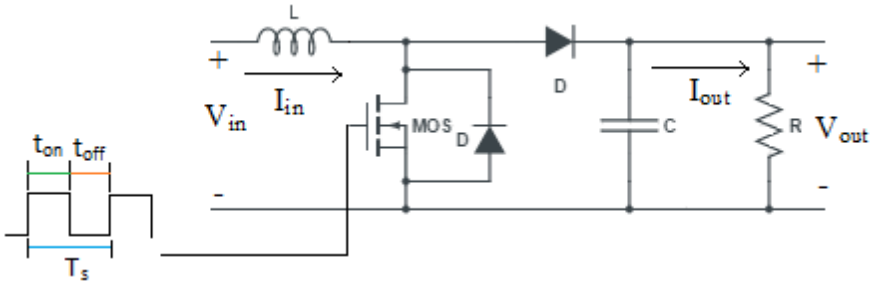



Figure A. 1 DC-DC boost converter

For the boost converter in Figure A.1, the state-space model for the ON interval ($^{(D)}/_{f_s}$) is given by:

$$\begin{bmatrix} \dot{i_L} \\ \dot{v_c} \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & \frac{-1}{RC} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} V_{in} \tag{A.1}$$

$$v_{out} = [0 \quad 1] \begin{bmatrix} i_L \\ v_c \end{bmatrix} \tag{A.2}$$

The switch is OFF for the second half of the interval ($^{(1-D)}/_{f_s}$). Therefore, the state-space model is obtained as:

$$\begin{bmatrix} \dot{i_L} \\ \dot{v_c} \end{bmatrix} = \begin{bmatrix} 0 & \frac{-1}{L} \\ \frac{1}{C} & \frac{-1}{RC} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} V_{in} \tag{A.3}$$

$$v_{out} = [0 \quad 1]\begin{bmatrix} i_L \\ v_c \end{bmatrix} \tag{A.4}$$

The state-space averaging technique over one switching cycle is employed and is obtained as

$$\begin{bmatrix} \dot{i_L} \\ \dot{v_c} \end{bmatrix} = \begin{bmatrix} 0 & \frac{-(1-\mathrm{D})}{L} \\ \frac{(1-\mathrm{D})}{C} & \frac{-1}{RC} \end{bmatrix}\begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} V_{in} \tag{A.5}$$

$$v_{out} = [0 \quad 1]\begin{bmatrix} i_L \\ v_c \end{bmatrix} \tag{A.6}$$

For a small perturbation, the standard linearization technique is used as shown below

$$\begin{aligned} i_L &= i_L + \tilde{\imath}_L \\ v_c &= v_c + \tilde{v}_c \\ d &= D + \tilde{d} \\ v_{in} &= v_{in} + \tilde{v}_{in} \end{aligned} \tag{A.7}$$

By applying the small perturbation in the state space averaging model [53], a small-signal model for the DC-DC boost converter is obtianed as

$$\begin{bmatrix} \dot{\tilde{\imath}}_L \\ \dot{\tilde{v}}_c \end{bmatrix} = \begin{bmatrix} 0 & \frac{-(1-\mathrm{D})}{L} \\ \frac{(1-\mathrm{D})}{C} & \frac{-1}{RC} \end{bmatrix}\begin{bmatrix} \tilde{\imath}_L \\ \tilde{v}_c \end{bmatrix} + \begin{bmatrix} \frac{V_c}{L} \\ \frac{-I_L}{C} \end{bmatrix}\tilde{d} \tag{A.8}$$

$$V_{out} = [0 \quad 1]\begin{bmatrix} \tilde{\imath}_L \\ \tilde{v}_c \end{bmatrix} \tag{A.9}$$

The transfer function $\tilde{v}_0/\tilde{d}$ can be obtained from (A.8) and (A.9). Similarly, the transfer function $\tilde{\imath}_{in}/\tilde{d}$ is determined by replacing (A.9) with the following equation.

$$i_{in} = [1 \quad 0]\begin{bmatrix} \tilde{\imath}_L \\ \tilde{v}_c \end{bmatrix} \tag{A.10}$$

# Appendix B

# Step Response for the Closed-loop Transfer Functions $\tilde{v}_{c1}$ to $\tilde{d}_1$ and $\tilde{v}_{c2}$ to $\tilde{d}_2$

## B.1 Closed-loop Transfer Function $\tilde{v}_{c1}$ to $\tilde{d}_1$

The following M-File is used to determine the open loop transfer function $\tilde{\imath}_{L1}$ to $\tilde{d}_1$. The M-File is based on the linearized small signal model of the two parallel-connected converters given in equation (4.26) and equation (4.27)

```
%  Open Loop transfer function iL1/d1
Vg1=24,                 % Voltage of DC source 1 (V)
D1=0.5069;              % steady state duty ratio of converter I
D2=0.5045;              % steady state duty ratio of converter II
L1=9.592e-3;            % Inductance of converter I (H)
C1=214.409e-6;          % capacitance of converter I (F)
R=5.8984;               % Load resistance (ohm)
Rc1=0.2;                % cable resistance, connected to converter I (ohm)
L2=8.72e-3;             % Inductance of converter II (H)
C2=235.851e-6;          % capacitance of converter II (F)
Rc2=0.1;                % cable resistance, connected to converter II (ohm)
R1=((Rc1*Rc2+Rc1*R+Rc2*R)/Rc2)
R2=((Rc1*Rc2+Rc1*R+Rc2*R)/Rc1)
Rm=((Rc1*Rc2+Rc1*R+Rc2*R)/R)
Vc1=48.6724;
Vc2=48.4357;
IL1=3.5/(1-D1);
IL2=4.6332/(1-D2);
% A Linearized Small-Signal Model for the Two Parallel Boost Converters
% Given by As, Bs, Cs and Ds matrices
As=[0 0 -(1-D1)/L1  0;0 0 0 -(1-D2)/L2; (1-D1)/C1  0 -(1/(R1*C1)+1/(Rm*C1))
(1)/(C1*Rm);0 (1-D2)/(C2) (1)/(Rm*C2) -(1/(R2*C2)+1/(Rm*C2))]
Bs=[Vc1/L1 0;0 Vc2/L2;-IL1/C1 0;0 -IL2/C2];
Cs=[1 0 0 0;0 0 0 0;0 0 0 0;0 0 0 0];
disp(['iL1/d1 (s)']);
TFb=zpk(tf(ss(As,Bs(:,1),Cs,[0])))     % Open loop transfer Function iL1/d1
```

The open loop transfer function $\tilde{\imath}_{L1}$ to $\tilde{d}_1$For three different values of cable resistance are determined for cable resistance values of $R_{c1} = 0.2\Omega, 0.55\Omega, and\ 0.9\Omega$, then the closed-loop

transfer function including the PI controller for the inner and outer loop is determined based on the block diagram of the two parallel connected converter model shown in Figure 4.9. The M-File for obtaining the close loop transfer function $\tilde{v}_{c1}$ to $\tilde{d}_1$ and the step response of different cable resistance is given by

```
Z1 = [-2.988e04 -353.2 -180.6];
P1 = [-4.00e+00 -1.86e+02+2.90e+02i -1.86e+02-2.90e+02i  -2.97e+04];
K1 = 5074.3;
Ga = zpk(Z1,P1,K1); % Open loop transfer Function iL1/d1 for Rc1=0.2 ohm

Z2 = [-1.402e04 -353.1 -181.5];
P2 = [-8.58e+00 -1.83e+02+2.92e+02i -1.83e+02-2.92e+02i  -1.38e+04];
K2 = 5074.3;
Gb = zpk(Z2,P2,K2); % Open loop transfer Function iL1/d1 for Rc1=0.55 ohm


Z = [-9285 -353.1 -182.3];
P = [-1.30e+01 -1.81e+02+2.93e+02i -1.81e+02-2.93e+02i  -9.11e+03];
K = 5074.3;
G = zpk(Z,P,K); % Open loop transfer Function iL1/d1 for Rc1=0.9 ohm

G1=tf(11.275*[0.0039 0.3],[1 0]);   % PI controller for the inner loop
G2= tf(16.275*[0.00016 5],[1 0]);   % PI controller  for the outer loop

sys_cA = feedback(G1*Ga,1);
sys_cb = feedback(G2*sys_cA,1); % close loop transfer function vc1/vd1
sys_cc = feedback(G1*Gb,1);
sys_cd = feedback(G2*sys_cc,1); % close loop transfer function vc1/vd1
sys_cl = feedback(G1*G,1);
sys_c2 = feedback(G2*sys_cl,1); % close loop transfer function vc1/vd1
step(sys_cb,sys_cd,sys_c2)      % Step response of a closed-loop system
```

## B.2 Closed-loop Transfer Function $\tilde{v}_{c2}$ to $\tilde{d}_2$

The open loop transfer function $\tilde{\imath}_{L2}$ to $\tilde{d}_2$ is obtained similarly to section B.1. The linearized small signal model of the two parallel-connected converter given in equation (4.26) and equation (2.27) is used in the M-File to determine the open loop transfer function $\tilde{\imath}_{L2}$ to $\tilde{d}_2$ as

```
%  Open Loop transfer function iL2/d2
Vg2=24,                   % Voltage of DC source 2 (V)
D1=0.5069;                % steady state duty ratio of converter I
D2=0.5045;                % steady state duty ratio of converter II
L1=9.592e-3;              % Inductance of converter I (H)
C1=214.409e-6;            % capacitance of converter I (F)
R=5.8984;                 % Load resistance (ohm)
Rc1=0.2;                  % cable resistance, connected to converter I (ohm)
```

```
L2=8.72e-3;                % Inductance of converter II (H)
C2=235.851e-6;             % capacitance of converter II (F)
Rc2=0.8;                   % cable resistance, connected to converter II (ohm)
R1=((Rc1*Rc2+Rc1*R+Rc2*R)/Rc2)
R2=((Rc1*Rc2+Rc1*R+Rc2*R)/Rc1)
Rm=((Rc1*Rc2+Rc1*R+Rc2*R)/R)
Vc1=48.6724;
Vc2=48.4357;
IL1=3.5/(1-D1);
IL2=4.6332/(1-D2);
% A Linearized Small-Signal Model for the Two Parallel Boost Converters
% Given by As, Bs, Cs and Ds matrices
As=[0 0 -(1-D1)/L1  0;0 0 0 -(1-D2)/L2; (1-D1)/C1  0 -(1/(R1*C1)+1/(Rm*C1))
(1)/(C1*Rm);0 (1-D2)/(C2) (1)/(Rm*C2) -(1/(R2*C2)+1/(Rm*C2))]
Bs=[Vc1/L1 0;0 Vc2/L2;-IL1/C1 0;0 -IL2/C2];
Cs=[0 0 0 0;0 1 0 0;0 0 0 0;0 0 0 0];
disp(['iL2/d2 (s)']);
TFb=zpk(tf(ss(As,Bs(:,2),Cs,[0])))  % Open loop transfer function of iL2/d2
```

In the similar manner of section B.1, the closed-loop transfer function $\tilde{v}_{c2}$ to $\tilde{d}_2$ is determined based on the block diagram of the small signal model shown in Figure 4.9. The closed-loop transfer function $\tilde{v}_{c2}$ to $\tilde{d}_2$ and the step response are determined for the cable resistance values of $R_{c1} = 0.1\Omega, 0.45\Omega$, and $0.8\Omega$ as

```
Z1 = [-1.396e04 -454.1 -130.5];
P1 = [-8.63e+00 -1.83e+02+2.92e+02i -1.83e+02-2.92e+02i  -1.38e+04];
K1 = 5554.6;
Ga = zpk(Z1,P1,K1);   % Open loop transfer Function iL1/d1 for Rc2= 0.1 ohm

Z2 = [-9245 -454 -131.7];
P2 = [-1.31e+01 -1.80e+02+2.94e+02i -1.80e+02-2.94e+02i  -9.05e+03];
K2 = 5554.6 ;
Gb = zpk(Z2,P2,K2);   % Open loop transfer Function iL1/d1 for Rc2=0.45 ohm

Z = [-2.99e04 -454.3 -129.3];
P = [-4.00e+00 -1.86e+02+2.90e+02i -1.86e+02-2.90e+02i  -2.97e+04];
K = 5554.6;
G = zpk(Z,P,K);      % Open loop transfer Function iL1/d1 for Rc2=0.8 ohm


G1=tf(11.275*[0.0039 0.3],[1 0]);   % PI controller for the inner loop
G2= tf(16.275*[0.00016 5],[1 0]);   % PI controller  for the outer loop
sys_cA = feedback(G1*Ga,1);
sys_cM = feedback(G2*sys_cA,1);     % closed-loop transfer function vc2/vd2
sys_cc = feedback(G1*Gb,1);
sys_cH = feedback(G2*sys_cc,1);     % closed-loop transfer function vc2/vd2
sys_cl = feedback(G1*G,1);
sys_cL = feedback(G2*sys_cl,1);     % closed-loop transfer function vc2/vd2
step(sys_cL,sys_cM,sys_cH)          % Step response of a closed-loop system
```

# Appendix C

# Parameters for Microgrid Components

## C.1 Alte 200-Watt 24V Poly Solar Panel

Alte solar modules are designed specifically for use in off grid applications The electrical parameters for the Alte 200-Watt 24V Poly Solar Panel is given in Table C.1 [92].

Table C. 1 Electrical parameters for the Alte 200-Watt 24V poly solar panel

| | |
|---|---|
| Open-Circuit Voltage ($V_{oc}$) | 44.56V |
| Optimum Operating Voltage ($V_{mp}$) | 36.70V |
| Short-Circuit Current ($I_{sc}$) | 5.99A |
| Optimum Operating Current ($I_{mp}$) | 5.45A |
| Maximum Power at STC ($P_{max}$) | 200 W |
| Module Efficiency | 15.72% |
| Operating Temperature | -40°C to 85°C |
| Maximum System Voltage | 1000V DC |
| Power Tolerance | 0/ +5% |

The temperature characteristics for the Alte 200-Watt 24V Poly Solar Panel is given in Table C.2 [92].

Table C. 2 Temperature Characteristics for the Alte 200-Watt 24V poly solar panel

| | |
|---|---|
| Nominal Operating Cell Temperature (NOCT) | 45 ± 2°C |
| Temperature Coefficient of $P_{max}$ | -(0.410 ± 0.05)%/K |
| Temperature Coefficient of $V_{oc}$ | -(0.320 ± 0.01)%/K |
| Temperature Coefficient of $I_{sc}$ | +(0.050 ± 0.05)%/K |

The Alte 200-Watt 24V poly solar panel has 25 Year Performance Warranty.

## C.2 MK BATTERY 6V FLOODED BATTERY - 8L16-DEKA

Deka Solar Flooded Monobloc batteries are designed to offer reliable, low-maintenance power for renewable energy applications. The specification of MK battery 8L16 is shown in Table C.3[92].

Table C. 3 Specification of MK battery 8L16

| | |
|---|---|
| Nominal Voltage (V) | 6V |
| Capacity at C/100 (Ah) | 420 Ah |
| Capacity at C/20 (Ah) | 370 Ah |
| Max. Charging Current | 30% of C/20 (Ah) |
| Max. Charging Voltage | 7.05V – 7.35V |
| Depth of Charge | 60% |
| Efficiency | 80% |

The MK battery 8L16 has 10 Year Performance Warranty.

## C.3 Magnum Energy MS2812 2800 W Inverter

The electrical efficiency of the Magnum Energy is 90%.

The cost $/kW is 572 $ [92].

The residential size inverter has 15 Year Performance Warranty [93].

# Appendix D

# Comparing Bisection Numerical Algorithm with Fractional Short Circuit Current and Open Circuit Voltage Methods for MPPT PV-solar System

## D.1 MPPT based on Bisection Numerical Algorithm (BNA)

The BNA is developed in Chapter 6, and the flow chart of bisection numerical method shown in Figure 6.10 is used to calculate the theoretical maximum voltage set point ($V_{max}$). The maximum voltage is used as input and compared with the actual output voltage of the PV model to extract the maximum power at various weather conditions. In this appendix, The Matlab model for the MPPT based on the BNA shown in Figure 6.12 is used to compare the tracking accuracy with the two methods of Fractional Short Circuit Current and Open Circuit Voltage Methods.

## D.2 MPPT based on Fractional Short Circuit Current

The block diagram for implementing the FSCC method in Matlab/Simulink environment is shown in Figure D.1

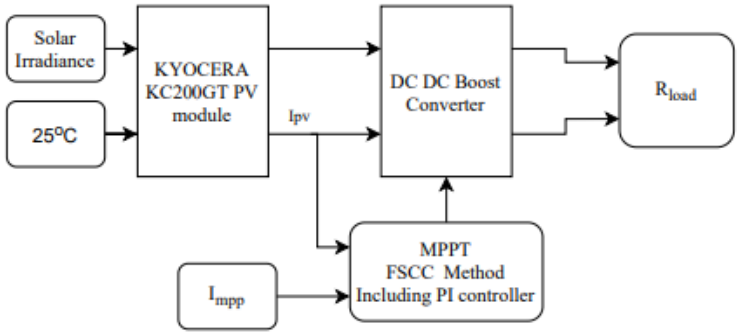



Figure D. 1 Block diagram of MPPT based on FSCC method

The short circuit current technique is one of the simplest methods due to its dependence on the photovoltaic system characteristics. The maximum power is determined by the maximum current, which is estimated as a fraction of the short circuit current. Thus, the reference current for the controller is given by:

$$I_{mpp} = k_1 * I_{sc} \quad \text{(D.1)}$$

The constant $k_1$ is a factor, which is chosen between 0.78 and 0.92 [94].

## D.3 MPPT based on Fractional Open Circuit Voltage

Figure D.2 shows the block diagram of the FOCV method. The block diagram shows the photovoltaic diagram system, which is connected to a resistor load through a DC-DC boost converter. The model is implemented in Matlab/Simulink model to examine the performance of the FOCV under various weather conditions.

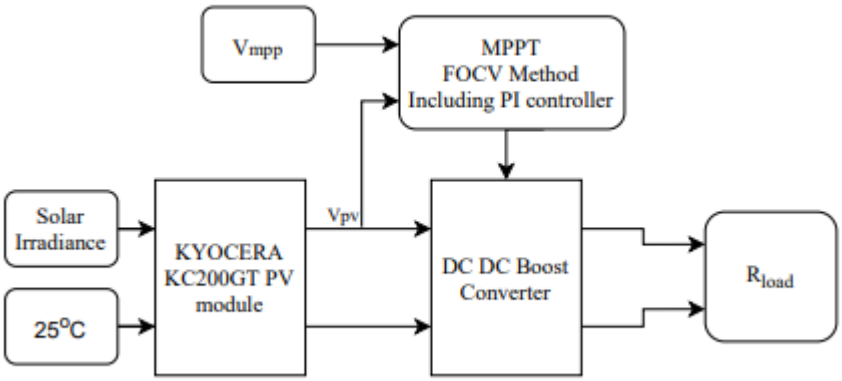



Figure D. 2 Block diagram of MPPT based on FOCV

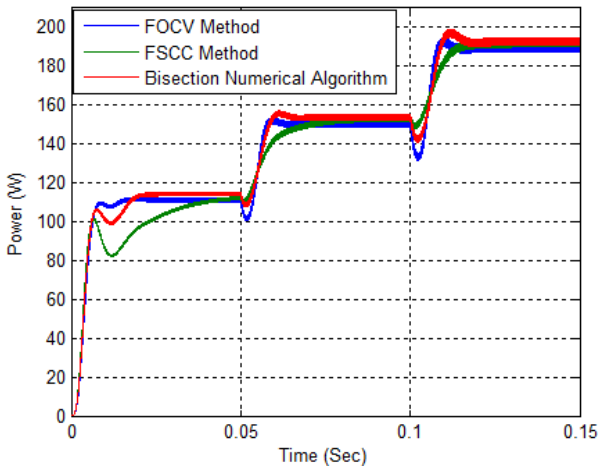
A fraction of the open-circuit voltage of the photovoltaic system is used as a reference value for the controller to extract the maximum power [94]. The 76% of the open-circuit voltage is used as given in the following formula:

$$V_{mpp} = k_2 * V_{oc} \tag{D.2}$$

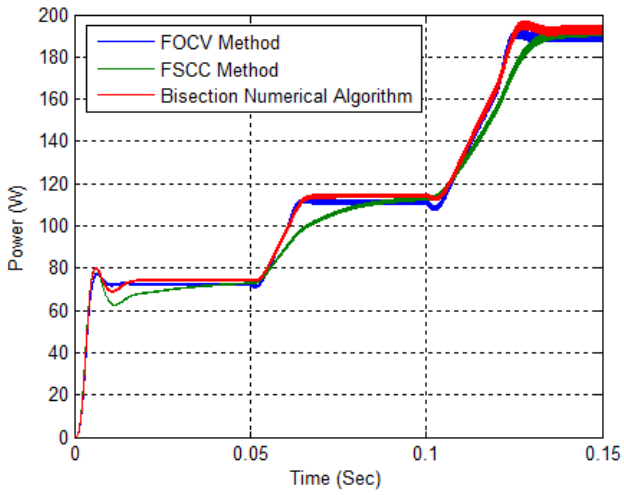
The constant $k_2$ varies from 0.71 to 0.8.

## D.4 Simulation Results for MPPT algorithms

Figure 6.12, Figure D.1, and Figure D.2 show the photovoltaic diagram system, which is connected to a resistor load through a DC-DC boost converter. The reference signal for the PI controller of the BNA is determined by the bisection numerical method, and the reference signal for the PI controller is determined based on a fraction of the short circuit current or open voltage circuit for the FSCC and FOCV, respectively. To compare the steady-state tracking accuracy between the BNA, FSCC, and FOCV, a step input and ramp input of the solar irradiance is provided. The step and ramp input function is ssimilar to climate change, as shown in Figure D.3 (a) and (b). There are three values of $600W/m^2$, $800W/m^2$, and $1000W/m^2$ for the step input case, which is entered into the Matlab/Simulink model during 0.15 second simulated case, as shown in Figure D.3 (a). Similarly, the ramp input case is simulated for three values of $400W/m^2$, $600W/m^2$, and $1000W/m^2$, which are gradually changed, as shown in Figure D.3 (b). The two cases are performed at $25^oC$.




(a) Step input solar irradiance case




(b) Ramp input solar irradiance case

Figure D. 3 Performance of three algorithms under step and ramp input of solar irradiation

A comparative analysis for the proposed bisectional numerical algorithm, and the FSCC method, and FOCV method is observed by using MATLAB simulation results. The results for the three algorithms are tested at $25^{o}C$. The results are used to evaluate their performance based on the steady-state tracking accuracy (TA) for the maximum power point are shown in Table D.1.

Table D. 1 Steady-state tracking accuracy for three MPPT algorithms

| **MPPT Algorithm** / **Irradiance** | | **Bisection numerical algorithm** | **FSCC method** | **FOCV method** |
|---|---|---|---|---|
| 1000 $\boldsymbol{W/m^2}$ | $\boldsymbol{P_{max}}$ | 192.8 W | 192.5 W | 189.3 W |
| | TA % | 96.4 % | 96.2 % | 94.6 % |
| 800 $\boldsymbol{W/m^2}$ | $\boldsymbol{P_{max}}$ | 154 W | 153.4 W | 150.5 W |
| | TA % | 96.7 % | 96.3 % | 94.5 % |
| 600 $\boldsymbol{W/m^2}$ | $\boldsymbol{P_{max}}$ | 114.4 W | 114.15 W | 111.2 W |
| | TA % | 96.8 % | 96.6 % | 94.2 % |
| 400 $\boldsymbol{W/m^2}$ | $\boldsymbol{P_{max}}$ | 74.65 | 74.5 | 72.25 |
| | TA % | 96.8% | 96.6% | 93.7% |

As indicated in Table D.1, the bisection numerical algorithm accurately tracks the voltage at the maximum power point. This comparison is based on the steady-state tracking accuracy of the peak

power point at different solar irradiation. The results in Table D.1 shows that the bisection numerical algorithm gives more power than the other two algorithms for various solar irradiations. Furthermore, the FSCC method accuracy has lower and closer accuracy to the BNA, but if the temperature of the PV panel is changed due to the variation in the weather condition, the tracking accuracy of the BNA is better. To illustrate, the maximum extracted power at $20^oC$ for the FSCC and the BNA is examined at $700W/m^2$. The BNA extracts 140.1 Watt, which is higher than 139.5 Watt, extracted by the FSCC. Furthermore, the extracted power for the BNA at $15^oC$ and at $700W/m^2$ is 146.1 Watt, which is higher than 145.4W, extracted by the FSCC.

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