Analysis and Design of High Voltage Gain Three-Elements Resonant Soft-Switching Current-fed DC/DC Converters

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Abstract

Analysis and Design of High Voltage Gain Three-Elements Resonant Soft-Switching Current-fed DC/DC Converters

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Transportation electrification and distributed generation are proven effective strategies to counter climate change. Modern generation and transportation aim to bring down the carbon footprint by transforming the fossil fuel-driven society with alternate energy sources and electric propulsion, respectively. However, harnessing energy from renewable sources is not straight forward but demands a suitable power electronic interface. Similarly, electric transportation propulsion system demands for specific power conversion stages. These power electronic conversion systems include dc-dc converter and dc-ac inverter. Cost, efficiency, power density, and weight are the major requirements of these converters. To obtain these merits, high-frequency soft-switching converters are selected and designed. Resonant converters with a suitable resonance have been usually explored for voltage-fed switching converters to obtain soft-switching of the semiconductor devices at high-frequency. However, owing to the high voltage gain requirements of the solar/fuel cells/batteries, this thesis explores current-fed topologies with different resonant circuits with natural voltage gain.

In traditional voltage-fed resonant converters, it is observed that the converter characteristics can be fine-tuned to design the requirements by proper selection of resonant tank. In addition, the resonant tank can integrate the transformer non-idealities and circuit/device parasitic in circuit operation thereby suppressing the consequent voltage spikes across the semiconductor devices. Since voltage-fed converters is fundamentally not suitable for high voltage gain and low voltage applications, this thesis attempts to improve current-fed dc/dc converter characteristics with resonant tanks.

In this thesis, a current-fed load resonant DC/DC converter topology is proposed whose characteristics are tuneable with the adopted resonant tank. Further, this thesis proposes a simple

technique to ease and improve accuracy of the Fundamental Harmonic Analysis (FHA), which would have been complex otherwise due to capacitive termination of proposed converter. Initially, the characteristics of the proposed converter topology with a parallel resonance derived LCC-T resonant tank is studied to implement zero voltage switching (ZVS) and zero current switching (ZCS) of the semiconductor devices. Three-phase topology of the same has been investigated and analysed. Following the study and a need to further improve the characteristics of resonant dc/dc converter, a series resonance based LCL resonant converter, a dual of the parallel resonance tank is studied and analysed. The load resonant converters are redeemed for integration of PV/fuel cells. Further, for high power applications, suitability of load resonant converters is verified by adopting resonant tank in three-phase topology. Proof-of-concept hardware prototypes are designed and developed in the laboratory to demonstrate the performance and the merits of the proposed soft-switching resonant converter topologies as well as to prove the proposed theory and the claims.

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List of Abbreviations

PTO	Power Take-off System
ePTO	Electric Power take-off systems.
DC	Direct Current quantities
AC	Alternating Current quantities
PWM	Pulse Width Modulation
ZVS	Zero Voltage Switching
ZCS	Zero Current Switching
QRC	Quasi Resonant Converter
MRC	Multi Resonant Converter
FEI	Front End Inverter
RER	Rear End Rectifier
EMI	Electro Magentic Interference
LC	Inductor Capacitor
LCL	Inductor Capacitor Inductor
LCC-T	Inductor Capacior Capacitor in T shape

List of Symbols

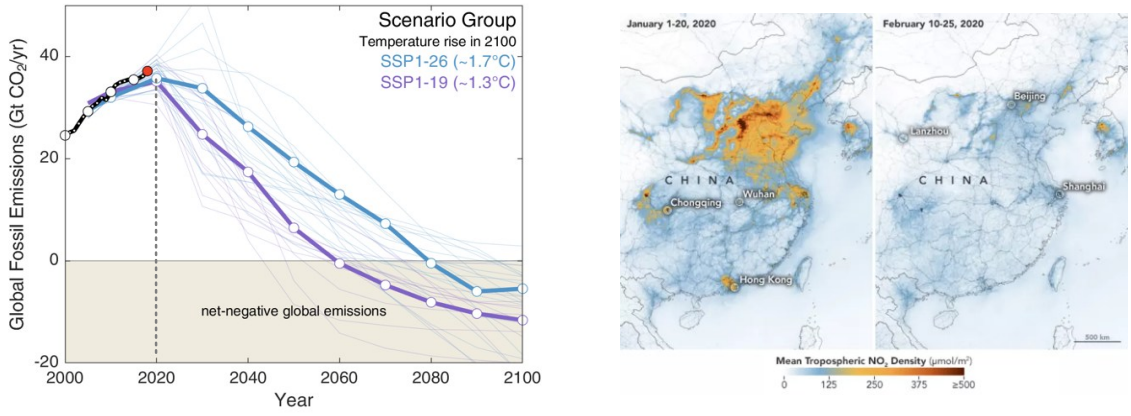
z_{oeq}	The equivalent impedance of the resonant tank as referred from its input terminals.
v_{Cp}	The parallel resonant capacitor voltage of LCC or LCC-T resonant tank.
i_{Lr}	Current drawn by the resonant tank.
i_{Lm}	The Peak of the current drawn by the resonant tank.
C_p	The parallel resonant capacitor in LCC and LCC-T resonant tanks.
v_{rer}	The input voltage of the rear-end rectifier or voltage doubler.
i_{rer}	The input voltage of the rear-end rectifier.
v_{ab1}	The first harmonic voltage of the FEI output voltage.
V_o	The output voltage of the dc/dc converter.
n	The transformer turns ratio, primary to secondary (>1).
θ	RER diodes conduction period in radians.
R_o	The output load resistance.
v_{Cpa1}	The coefficient of 'cos' term in v_{Cp}
v_{Cpb1}	The coefficient of 'sin' term in v_{Cp}
R_{eq}	The resistance part of z_{oeq}

C_{eq}	The capacitance part of z_{oeq}
FHA	Fundamental Harmonic Approximation
ELS circuit	Equivalent Linear Sinusoidal circuit
EDF	Extended Describing Function
v_{sq}	The square component of v_{Cp}
v_{η}	The residual portion of v_{Cp} after eliminating v_{sq}
i_{tfp}	The current entering into the transformer primary dotted terminal.
v_{tfp}	The voltage is subjected to the primary terminal of the transformer with the dot being higher potential.

Chapter 1 Introduction

1.1 Non-conventional Energy Sources

Silent contributions of the automobiles and the power generating stations to the degradation of the living environment through emissions of fossil fuel combustion are behind the unbridled raise of environment temperature and climate change, Fig. 1(a), [1]-[3]. Concerns for bridling the rampant pollution caused by the automobiles are expressed by the U.S. in mandating aggressive fuel economy standards (54.3 miles per gallon) [4]. The potency of Standards limiting the fuel consumption to curtail environmental pollution is evident from reduced fossil fuel consumption during COVID-19 lockdown throughout the world. Within two months of lockdown, the carbon monoxide level in New York alone is reduced by 50% [5], [6]. To recover environmental pollution,



(a) *(b)*

Fig. 1.1. (a) Prediction of raise in temperatures in coming future [1] (b) Potency of reduction of fossil fuel consumption in controlling environment temperature [2].

there is a necessity for the development of new power management techniques. The following are two of the popular techniques.

1.1.1 ePower take-off systems

Transportation through automobile systems has contributed significantly towards the advancement of the world through several years [7]. Automobile systems can be broadly categorized into light-duty such as passenger vehicles and medium and heavy-duty vehicles in applications such as construction, farming, and transportation of goods and utility [8]. In a light-duty passenger vehicle, the propulsion loads are driven by ICE, while the non-population loads such as lighting and sound are driven by a battery which is replenished by an alternator driven by fossil fuel-fed ICE as shown in Fig. 1.2(a). On the other hand, in the case of medium and heavy-duty vehicles such as recreation vehicles (RV) and refrigerated trucks the cooling requirements are significantly large to be directly driven by the main ICE. Therefore classical PTO approach, as shown in Fig. 1.2(a), use an auxiliary generator to meet those requirements. Further, applications such as welding and drilling also come into this category. In an electrified PTO system, the non-propulsion loads such as lightening, sound, AC, refrigeration, drilling, etc are met by PV/fuel cell/batteries interfaced with high voltage gain DC/DC converter followed by a DC/AC inverter.

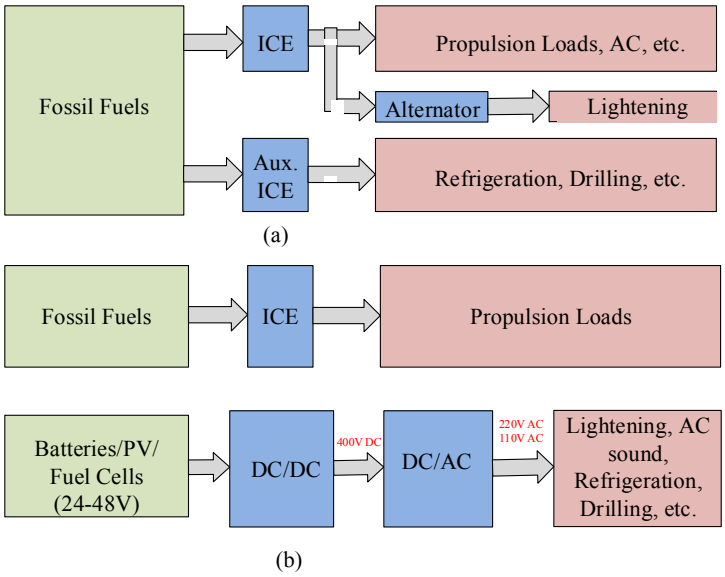


Fig. 1.2. Power train flow with (a) conventional PTO system (b) electrified PTO system to feed propulsion and non-propulsion loads in specialty vehicles for heavy-duty applications such as construction, farming and transportation of goods and utilities [7].

Further, the need for an alternator in existing PTO systems is eliminated as the lighting and recreation loads can be driven by PV/fuel cell.

The ePTO system has significantly improved the quality of experience in recreation vehicles by eliminating the need for an auxiliary generator making it noise free while resting and light and comfortable for transits. Similar improvements of ePTO architecture in other applications be observed in [9]. However, the Power electronic converter in ePTO system needs to be higher in efficiency, lower in size, weight, and volume [10]. The requirements of such a converter are described below.

1.1.2 Micro grid architecture

This technology aims at decentralizing the fossil fuel-based central power generation strategy using non-conventional and distributed energy sources such as solar and fuel cells [11]. This architecture in the modern day can cater according to the customer needs, unlike centralized power generation. Further, this architecture able to electrify castaway living places, hilly area,

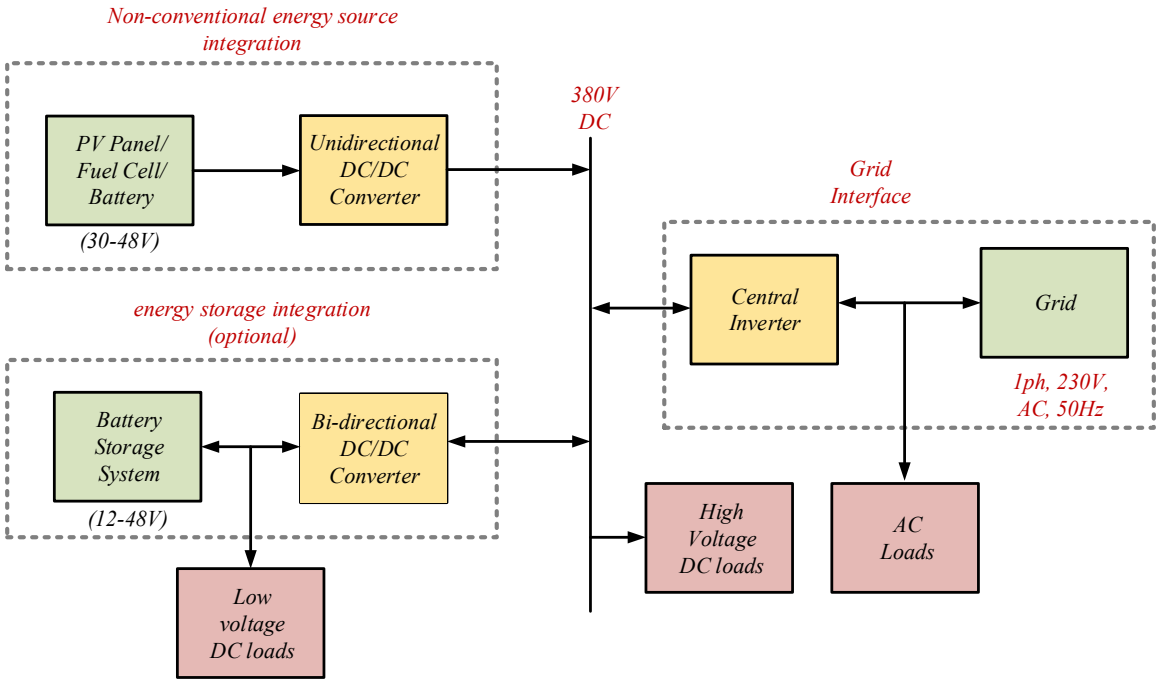


Fig. 1.3. Architecture of DC microgrid involving PV panels and storage system to grid through central inverter.

deserts, army, and navy bases where central power systems can't even imagine reaching on. Rural electrification is another application of it. Standalone micro-grids are popular in this respect [12]-[13].

For the desirable operation of the microgrid, a high voltage gain dc/dc converter as shown in Fig.1.3, to interface PV panel/fuel cell to high voltage DC bus [14]. A central inverter is used to interface the DC bus to the grid. An energy storage system such as a battery pack is necessary in case of a standalone micro-grid and optional in the case of the grid-connected microgrid [12]. Storage is interfaced with the grid with the help of a bidirectional converter to charge and discharge battery [15]. On the other hand, battery, PV panels, fuel cells generate very low voltage [16] as a comparison to the high voltage dc bus [17], [18]. Therefore, a high voltage gain dc/dc converter is essential to interface. Exploration of such a converter is the topic of this thesis and the requirements are discussed in the following section.

1.2 High voltage gain DC/DC converter requirements

To extract power strategically, interfacing DC/DC converter between PV/fuel cells and high voltage DC bus must satisfy the following requirements.

1.2.1 High voltage gain

PV/ fuel cell/ batteries offer low output voltage (30-48V) at their input terminals, while the DC bus is maintained at 380V. Series connection of cells of these individual sources to meet high voltage DC bus does not allow to extract maximum generated power thus practically not feasible [19]. Since PV and fuel cell are modeled as a current source, therefore, parallel connection of each source is practically feasible. To meet high voltage DC bus, high voltage gain DC/DC converter is essential [18]. Also, the output voltage level of the DC/DC converter stage is a standard voltage to (380V-400V) obtain a grid integrable 230V, 50Hz AC supply through a single phase DC/AC inverter.

1.2.2 Suppression of source uncertainty

PV panels generate low dc voltage when subjected to sun irradiation while a fuel cell generates low dc voltage when supplied with necessary fuel. Since sunlight and fuel flow are variable and subject to weather and load demand respectively, the voltage generated by these sources is also highly variable. However, these uncertainties should not reflect in the output voltage. Therefore, the proposed dc/dc converter should be able to suppress these variations to regulate the high voltage DC bus.

1.2.3 Stiff input current

Time required to recover the investment on the solar power system is termed as Return on Investment (RoI). It is the duty of the designer to ensure RoI is as minimum as possible to start earning profits. However, once installed, PV panels are expected to serve the system ideally for 25 years. Such longer life cycle favors to maximize the profits. However, to preserve the lifetime of PV and fuel cell, stiff and ripple free current should be drawn [16], [19]. Further, it favors an MPPT technique for precise and stable MPPT operation.

1.2.4 Safety isolation

PV panels, at times contribute to the common mode currents, which can pass through utility equipment thus putting the safety of the customer into risk. In order to ensure the safety of the operator while working on the system, these common mode currents should be suppressed. This can be achieved by including a transformer in the DC/DC converter. This ensures high voltage gain and provides electrical isolation between source and load [20].

1.2.5 High efficiency and power density

It should be observed that higher efficiency of a converter means lower power losses in the system resulting in maximum utilization of the energy. This ensures faster RoI. Therefore, converter should operate at maximum possible efficiency under all load and input conditions.

Converter circuit configuration should involve minimum possible components for power conversion and simple modulation methods to control the devices to result in minimum losses to achieve high efficiency [21] and high-power density [22]. Soft-switching technique and high-frequency operation are desired in achieving this requirement.

1.2.6 High frequency and scalability

The values of the components should be practically feasible upon extending for higher power ratings or higher switching frequency operation.

1.2.7 Range of soft-switching

The converter should maintain soft-switching over a wide range of load current and source voltage variations to maintain high efficiency and performance. With soft-switching in the devices, especially during turn-on, device voltage of the switch is forced to zero prior to its turn on. This significantly reduces the need of miller charge for gate to source voltage build up. This also improves the quality of the gate signal by suppression of dv/dt noise generated and EMI which improves the EMC compatibility.

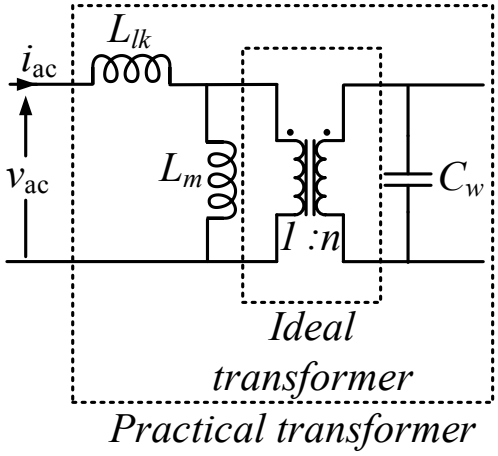


Fig. 1.4. Significant non-idealities in practical transformer when operated at high frequency [23]

1.3 Literature review high voltage gain DC/DC converters

Practical implementation of a power electronic converter is always associated with cost, volume, weight, payback period (efficiency). Considering these requirements, this section provides a relevant literature review of the DC/DC converters intending to match the requirements of high voltage gain DC/DC converter as mentioned in the previous section.

The isolation element, the high-frequency transformer, in power electronic converters for high voltage gain applications such as PV/fuel cell integration exacerbates its non-idealities due to large turn ratio and higher switching frequency [23]. Unnegotiable leakage inductance and winding capacitance, as shown in Fig. 1.4, interfere with the underlying operation of the converter generates unwanted voltage and current spikes respectively. This increases conduction losses, switching loses thus demands bulky snubber circuits and heat sinks to maintain thermal stability [24]. It also demands overrated components.

Resonant converters offer a lucrative solution to such cases [25]. The philosophy of the resonant conversion involves engaging transformer non-idealities such as leakage inductance and winding capacitance into converter operation, thereby eliminating the unnecessary current and voltage spikes. A properly designed resonant tank can reshape device current and voltage, thereby eliminating the switching losses to consequentially elevate the efficiency, the switching frequency, and the power density further [26]. Few resonant conversation techniques allow to integrate device and diode parasitic into soft-switching resonant components [27]. Depending on the load current, input voltage, and converter operation, resonant converters can be broadly classified into the following groups.

a. Quasi-resonant soft-switching converters
b. Load resonant soft-switching converters.

1.3.1 Quasi-Resonant Converters

In quasi-resonant converters, resonant elements contribute only to soft-switching transitions. Conventional switches, in combination with the auxiliary reactive elements, can be

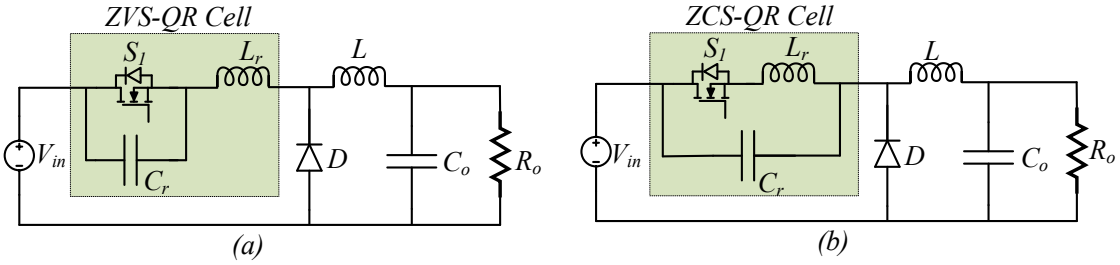


Fig. 1.5. Converting classical dc/dc converters into quasi-resonant converters. (a) Buck derived ZVS quasi-resonant converter. (b) Buck derived ZCS quai-resonant converter.

forced to carry quasi-sinusoidal currents and/or voltages to eliminate switching losses [27]. Such switches are called the resonant switches. Replacing conventional switches of PWM converters with such resonant switches results in quasi-resonant converters. As an example, Quasi-resonant ZVS (resonant capacitor is in parallel with the device) switching buck converter, is shown in Fig. 1.5(a) and Quasi-resonant ZCS (resonant inductor is in series with device) switching buck converter, is shown in Fig. 1.5(b). Quasi-resonant converters resemble conventional PWM converters. Besides, to reduce the switching losses, quasi-resonant converters can integrate non-idealities of switches, diodes, inductors, and transformers into converter operation which otherwise generate spikes is a major advantage [28], [29]. However, quasi-resonant converters no longer able to compensate load and input disturbances through duty ratio modulation thus adopt frequency modulation. Further, non-idealities introduced by resonant components incurs additional voltage drops and thus limits higher voltage gains and power levels. Also, switches are subjected to a higher voltage and current stress. A unified approach in analyzing quasi-resonant converters are presented in [30]. Detailed advantages and drawbacks of the quasi-resonant converters are reported in [28], [29]. Abilities of the quasi-resonant converters in comparison to the conventional PWM converters are reported in [31]. Two major classes of quasi-resonant converters, ZCS-QRC (favors smooth device turn-off) and ZVS-QRC (favors smooth device turn on) at an expense of increased switch current and voltage stress are detailed in [32]. Also, constant frequency quasi-resonant converters are detailed in [33]–[35].

Multi-resonant converters (MRC) can integrate the merits of ZCS and ZVS quasi-resonant converters by replacing the PWM switches of the classical dc/dc converters at an expense of

increased circuit complexity and components' count [36]–[38]. However, the switches still suffer from the soaring current, and the voltage stress and variable frequency operation remain a major disadvantage. The operating frequency range is highly vulnerable to the PV voltage fluctuations. Constant frequency MRC with clamped switch voltage is presented in [39], [40].

Compared to the QRC and MRC topologies, constant switching frequency active-clamped quasi-resonant flyback converters are more attractive for PV/fuel cell integration applications at lower power levels due to their simplicity. A basic flyback converter suffers from the huge voltage and current impressions on its switches and high di/dt turn-off of the secondary diodes. Solutions such as RCD snubber [41], [42] clamps the voltage across the switches to a lower level by dissipating the leakage energy into the snubber resistance. Instead of dissipating, active-clamp technique [43]–[45] recycles the leakage energy. Further, it magnetizes the flyback transformer with the bi-directional current to eliminate switching losses at the expense of increased conduction losses in the transformer. On the other hand, the range of soft-switching is highly limited, which is extended by adding a resonant inductor in series with the flyback transformer. The leakage inductor upon resonating with switch capacitance eliminates switching losses in semiconductor devices. Besides, the transformer is magnetized with the unidirectional current to limit conduction losses in the transformer [46]–[48]. Soft turn-off of secondary diode offers significantly reduced voltage ringing across secondary and snubber free operation. High voltage gain applications expect slow diodes across secondary, thus active-clamped flyback converters are of choice for low power applications [23]. A secondary active-clamped flyback converter [49] and auxiliary cell assisted flyback converter [50] are also discussed.

The symmetrical and asymmetrical voltage-fed full-bridge converters augmented with the voltage doubler are presented in [51], [52]. Such converters are also intended for PV applications as they offer higher voltage gain, isolation, clamped switch voltages, and constant operating frequency. However, due to voltage-fed front end inverter (FEI), input current ripple demands a bulky unreliable electrolytic capacitor. Also, better MPPT with constant current approved.

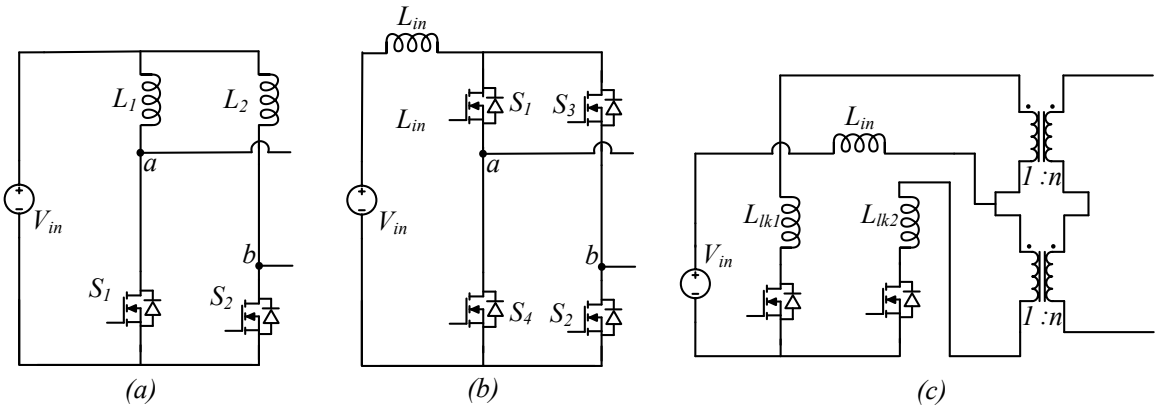


Fig. 1.6. Clampless FEI (a) half-bridge (b) full-bridge (c) push-pull

Converters with constant input current, i.e., current-fed type, can eliminate the requirement of a bulky capacitive input filter. Such converters can extend converter reliability in par with PV panel lifetime. However, the current-fed converters suffer from the switch turn-off voltage spike, which forces them to adopt the FEI with an active-clamping technique [53]–[58]. A current-fed transformer assisted auxiliary circuit based non-isolated quasi-resonant converter can offer high voltage gain at the expense of the increased components' count limited at lower power level [57]. A current-fed quasi-resonant boost half-bridge dc/dc converter can offer high voltage gain at the expense of a bulky inductive output filter [55]. An interleaved version with a capacitive output filter eliminates these demerits [58]. Integrated boost quasi-resonant converter with FEI, as shown in Fig. 1.10 (c) with leakage inductor as resonant element is discussed in [53], [54], [55]. They adopt voltage doubler as rear-end rectifier (RER) for high voltage gain and low transformer turns ratio. Though [53]–[58] offer compact size, constant input current, and fixed-frequency operation, a clamping capacitor is mandatory thus compromises the reliability and volume.

Unclamped current-fed quasi-resonant converters certainly enhance the lifetime of the converter in par with PV panel under such conditions. A high-efficiency clampless half-bridge current-fed multi resonant converter (FEI: Fig. 1.6 (a); Resonant tank: Fig. 1.7 (c7)) offers soft transition in the switches [59]. A clampless full-bridge counterpart (FEI: Fig. 1.6 (b)), discussed in [60], offers high voltage gain and reliability at the expense of variable operating frequency.

Impulse resonant converters, an improved version of LL type PWM soft-switching converters [61], are a special class of quasi-resonant converters. This technique has been verified

on various FEIs such as push-pull (as shown in Fig. 1.6 (c)) [62]–[64], full-bridge [65] (as shown in Fig. 1.6 (b)), and half-bridge [66] (as shown in Fig. 1.6(a)). Impulse resonant converters also offer high voltage gain, high reliability at expense of compromised efficiency, and variable switching frequency. Conventional time-domain analysis for steady-state and dynamic modeling is valid for quasi-resonant converters. The major drawbacks of the impulse converters are variable frequency operation and higher peak currents at light load.

1.3.2 Load Resonant Converters

In this type of conversion, the resonant elements not only contribute to the soft-switching but also participate during the complete high frequency switching cycle. Therefore, the characteristics of the load resonant converters are highly influenced by the type of resonant tank employed [67], [68]. A basic load resonant DC/DC converter with various stages involved is depicted in Fig. 1.7 (a). In a nutshell, the operation of a load resonant converter involves inversion of input DC voltage by a front end inverter (FEI) to feed a resonant tank with high-frequency AC waveform. Resonant tank in turn processes and passes it onto the transformer followed by the rear end rectifier (RER), which rectifies and filters the available high-frequency AC voltage to feed the DC bus. Depending on the application, the RER could be a full-wave rectifier or full-bridge rectifier [23], [68].

Applications with low voltage and high current such as voltage regulators [69], by nature, favors full-wave rectifier as RER with fewer devices for minimum voltage drop and power losses. Further synchronous rectification abates conduction losses with minimum possible (two) active switches [23]. On the other hand, high voltage and low current applications such as PV/fuel cell integration, by nature go with full-bridge rectifier as RER. Further RER allows the extension of full-bridge into voltage doubler and quadrupolar configurations [68]. Also, operating resonant converter above resonance manifests ZVS switching and below resonance results in ZCS operation [26]. However, soft switching of the devices is vulnerable to variations in the values of the resonant components. This may be sue to change in the environment temperature, ageing or manufacturing imperfectness. The study concerning to the effects of component variations on the soft-switching

comes under observer theory. In practical design, a significant margin is considered for soft-switching design.

1.3.2.1 Voltage-fed type

In this type of converters, FEI is directly driven by the voltage source, which is responsible to supply high frequency switching current to the resonant converters. Such converters when used in connection with the PV need a bulky electrolytic capacitor rated at input voltage to supply high harmonic ripple current, which extends the PV lifetime.

In a half-bridge series resonant converter (FEI, Fig. 1.7 (b1); Resonant tank, Fig. 1.7 (c1)), interestingly, the resonant capacitor appears in series with the transformer helps to block DC voltage to prevent the transformer from flux walking [67]. Also, currents through the switches are in proportion with the load currents and offer acceptable light load efficiency. But limited selectivity of the resonant tank complicates light load operation. Therefore, the series resonant converters cannot offer wide load variation as required by the PV/fuel cell integration. Further, frequency modulation is another major drawback [23], [26], [70]–[72]. Further, high voltage gain demand by the PV/fuel cell integration and step-down nature of FEI pushes up the transformer turns ratio.

PV/fuel cell integration demands high power density. Therefore, operating a converter at a fixed frequency helps to optimize the magnetic design, control circuitry, and EMI filters [12]. Therefore clamped mode series resonant converter with full-bridge FEI, which operates under fixed switching frequency, is more suitable for PV/fuel cell integration rather than half-bridge FEI [74]–[77].

The resonant inductor appears in series with the leakage inductance of the transformer, but winding capacitance is not included in the converter operation. Therefore, for every high-frequency voltage reversal in the resonant tank, none of the RER diodes are forward biased for power transfer unless the parasitic capacitor (C_w) is charged/discharged. This abnormal subinterval hinders the power flow and increases output current ripple. Therefore, voltage-fed series resonant converters need an overdesigned output filter capacitor [23].

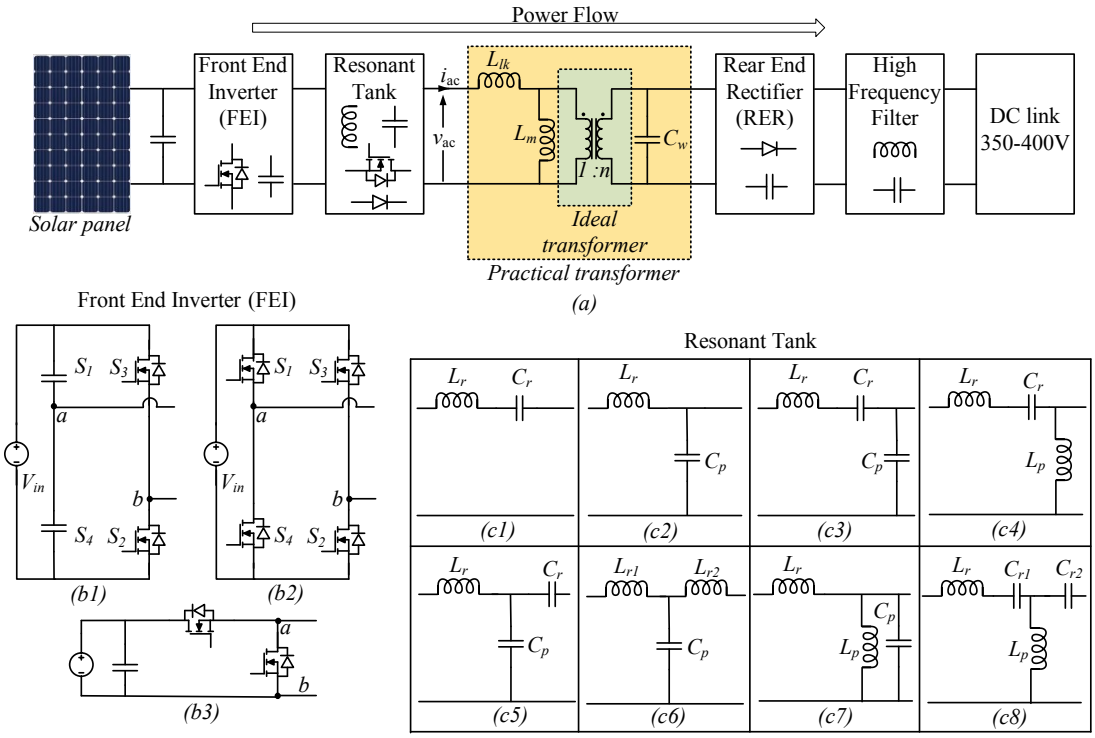


Fig. 1.7. (a) Block diagram of resonant converters. (b1) Half-bridge FEI, (b2) Full-bridge FEI, (b3) Class-D FEI, (c1) Series resonant tank, (c2) parallel resonant tank (c3) series parallel (LLC) resonant tank (c4) LLC-SRC (c5) LCC-T resonant tank (c6) LCL-T resonant tank (c7) (LC)(LC) resonant tank (c8) (LC)LC resonant tank.

On the other hand, a half-bridge parallel resonant converter (FEI, Fig. 1.7 (b1); Resonant tank, Fig. 1.7 (c2)) integrates both leakage inductance and winding capacitance into converter operation [78]–[80]. However, the output LC filter turns as bulky as the transformer in case of high output voltage applications such as PV/fuel cell integration. Therefore, both the series and the parallel resonant converters suffer from a bulky output filter [23]. However lower currents on the secondary side can increase the resonant capacitor lifetime and thus, the reliability of the converter [67]. Further, this converter offers inherent short circuit protection. However, energy stored in the resonant tank is independent of the load current. Therefore, light load efficiency is poor [26].

Unlike half-bridge parallel resonant converter, full-bridge counterpart (FEI: Fig. 1.7 (b2)) offers fixed switching frequency operation as required by the PV/fuel cell integration [81].

However, the parallel resonant converter is devoid of series capacitance, which exposes the transformer to the risk of flux walking.

Drawbacks of series (inability to regulate under no load) and parallel (stored resonant energy independent of load) resonant converters are alleviated in the half-bridge series-parallel resonant converter (FEI, Fig. 1.7 (b1); Resonant tank, Fig. 1.7 (c3)), which could be a suitable candidate for PV/fuel cell integration [82]. It carries advantages of both series and parallel resonant converters. However, bulky LC filter at the output, wide-range frequency operation, and compromised light load efficiency remain major drawbacks of this converter. Even though LC filter can be replaced with a capacitive filter [83]–[87], variable frequency operation is checked with a clamped voltage capacitance method [88]–[90], and the domination of parallel resonant tank characteristics deteriorate light load efficiency.

Another half-bridge LLC-SRC resonant converter (FEI, Fig. 1.7 (b1); Resonant tank, Fig. 1.7 (c4)), a modified version of the series resonant converter, is studied to alleviate the drawbacks of the series resonant converter i.e., light load regulation sensitivity [91]. LLC-SRC resonance tank is formed by placing an inductor in parallel to the transformer of a series resonant converter. Such a modified resonant tank gain characteristics have load-independent gain near the ZVS region and thus need minimum variation in frequency for load compensation. Like the series resonant converter, the resonant capacitor *(C_r)* can block DC offset across the transformer. A constant frequency LLC-SRC resonant converter (FEI, Fig. 1.7 (b2); Resonant tank, FA simple big. 1.7 (c4)) is studied in [92]–[95]. Further enhancement in voltage conversion ratio, the extended input,

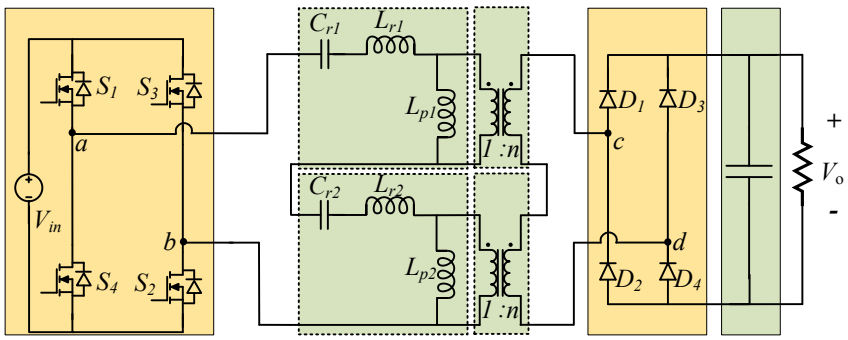


Fig. 1.8. Voltage-fed split LCC-SRC resonant converter for wide input voltage and load disturbances.

and load range is achieved by the split LLC-SRC resonant tank as shown in Fig. 1.8 [96], [97]. Four element based resonant converters is also analyzed [98], [99] for better performance.

The design and optimization of the above-mentioned resonant converters against load fluctuations are not easy due to the load-dependent resonant tanks. A simple two-stage, buck followed by a voltage-fed push-pull resonant converter is proposed in [100]. The front-end buck stage compensates the load and input fluctuations to decouple its influence on the frequency of operation. On the other hand, a voltage-fed push-pull load resonant converter needs a very simple gate driver circuit as opposed to [101]–[103]. Further, it offers fixed-frequency of operation and for wide load and input range.

However, inherently voltage-fed resonant converters demand bulky electrolytic capacitor rated at maximum input to enhance the lifetime of PV panels. But it limits the lifetime of the converter relative to PV panel life. The current-fed converter offers a suitable compact solution.

1.3.2.2 Current-fed type

Current-fed converters adopt an inductive input filter, which offers stiff input current and enhances the reliability of the converter. The popular duality technique is instrumental in deriving the current-fed converter topologies from well-established and verified voltage-fed converters. Depending on the nature of the switching devices, the current-fed converters are classified as converters with a unidirectional voltage blocking switches and bi-directional voltage blocking switches [104]–[106]. Converters [104]–[106] obtained by applying the duality principle to each

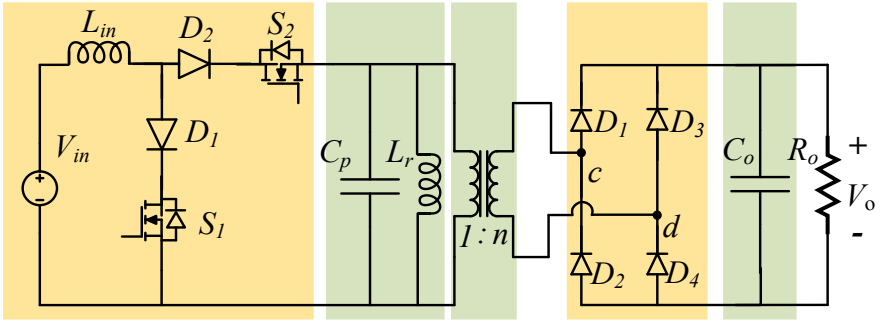


Fig. 1.9. Class-D current source parallel resonant converter using bidirectional voltage blocking switch.

operating mode of respective voltage-fed converter counterpart; on the other hand, [103]-[108] obtained by applying the duality principle to each stage [107].

1.3.2.2.1 Bidirectional voltage blocking switches

A simple bidirectional voltage blocking switch-based class-D current source parallel resonant converter, as shown in Fig. 1.9, studied in [104]. Full-bridge FEI with similar switches, as shown in Fig. 1.10(a), is presented in [105], [106]. (LC)(LC) resonant tank and LC resonant tank are adopted in [105] and [106] respectively. A bidirectional voltage blocking switch is achieved by a series connection of diode and MOSFET such that the series diode disables the body diode of the MOSFET. Such diodes carry complete load current and not suitable for higher current as they compensate recovered switching losses with blocking diode conduction losses. This worsens with full-bridge configuration. Further, the optimization of magnetics and control circuitry is not possible due to variable frequency operation [105], [106].

1.3.2.2.2 Unidirectional voltage blocking switches

On the other hand, a basic current-fed converter with a unidirectional voltage blocking switches (MOSFET) includes a cascaded boost converter followed by an unregulated voltage-fed class-D LLC-SRC resonant converter [108] or a push-pull resonant converter [109]. The front end boost converter compensates load and input disturbances and operates the converter at a fixed

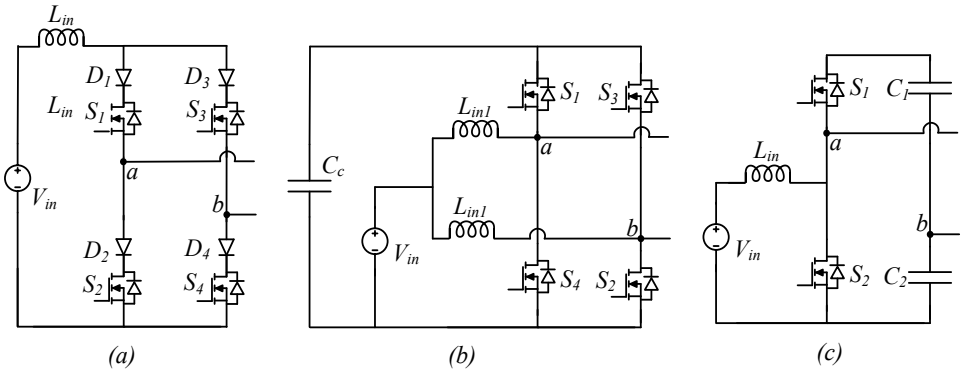


Fig. 1.10. FEI with (a) Full bridge (bidirectional voltage blocking switches) (b) Active clamped dual boost (c) Active clamped boost.

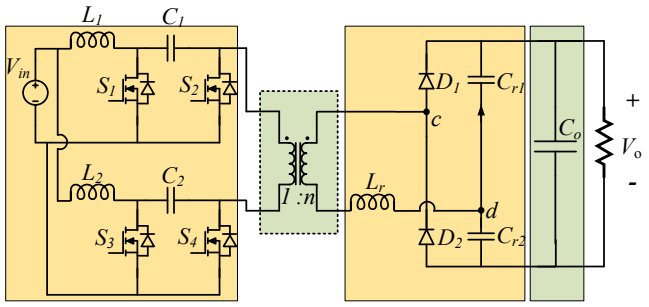


Fig. 1.11. Current-fed load resonant converter (54).

frequency at the expense of higher conduction losses. The push-pull converter [110] eliminates front end buck converter but operates at the variable switching frequency. A fixed frequency current-fed push-pull [111], [112] load resonant converter adopts clamped switches. However, high side switches complicate the driving scheme and increases component count, and power losses. By shifting active-clamp onto the input inductor [113] maintains all merits offered by [108]-[111].

Active-clamped interleaved boost converters based FEI (Fig. 1.10(b)), two LLC resonant tanks, each connected to one boost converter, is presented in [114] that operates in variable frequency mode with the stiff input current. Like [114], the converter presented in [115] as shown in Fig. 1.11 needs high components' count but operates at the fixed frequency and maintains soft-switching against wide input and load disturbances. However, [116]–[117] adopt the simplest FEI (Fig. 1.10 (c)) to maintain fewer components' count and soft-switching of all devices under wide input and load disturbances. Similarly, converters adopt the LCC tank [116], LCL-T tank [117], and LCL resonant tank [117] successfully to operate at the constant switching frequency, constant input current, and wide load range and input operation to support PV/fuel cell integration. However, the clamp capacitors in FEI reduces the reliability of the converter.

1.4 Research problems and objective.

Given curtailing consumption of fossil fuels to control unbridled pollution and global warming, sophisticated inclusion of non-conventional alternate energy sources and distributed generation must be ineluctable [1], [2]. As presented in section 1.2, it is evident that high voltage

gain DC/DC converters play an important role in extracting power from these sources [17], [18]. A brief presentation of the expected requirements for the high voltage gain DC/DC converter are elaborated in section 1.3.

Achieving high voltage gain, stiff input current, and extended light load operation with acceptable efficiency, high density, modularity for power scaling capability, and high reliability in a single converter is challenging [61]. Though current-fed converters, popularly clamped quasi-resonant, and uncapped quasi-resonant converter, can be a suitable choice for application under study due to stiff input current and high voltage gain characteristics, developing other requirements is still a challenge due to insufficient resonant tank energy [54], [66]. On the other hand, reduction of stress in the devices can inherently achieve high reliability of the converter.

Major challenges to deal with are 1) pushing power processing capability 2) power density and 3) extending input voltage range and load current range of the converter while maintaining voltage regulation.

1.4.1 Pushing power processing capability:

The majority of the converters presented in the literature are experimentally verified for a scaled-down version i.e., 150W to 500W. In practice, applications understudy needs converter rated for 3 to 5kW to integrate non-conventional energy sources. Therefore, the paralleling of low rated converters to meet higher power ratings is not practically feasible. Redesigning a resonant converter to handle increased power also requires selecting a resonant tank that stores proportional energy to charge/discharge MOSFET's drain-to-source capacitance [118]. This translates to maintain increased currents through the resonant tank which is only possible under lower characteristic impedance of the resonant tank. Therefore, lower resonant inductors are needed to achieve lower characteristic impedances in the circuit which is practically not realizable by the transformer. Therefore, the power processing capability of this technique is limited.

1.4.2 Pushing power density

Power density in a converter is improved by reducing the size of the components, which is possible by operating at the higher switching frequency. Quasi-resonant converters need to operate far below resonant frequency to complete the resonance cycle as soon as the switching transition gets over. Typically, the ratio of the resonant frequency to switching frequency is 5 to 10. From the above discussion, two conclusions can be observed.

1. For a given switching frequency, a quasi-resonant converter needs smaller resonant inductance to achieve the required resonant frequency. In some cases, the resonant inductor (leakage inductance of transformer) demanded by a quasi-resonant converter is extremely small which is not feasible to design practically by a practical transformer.
2. Due to the high ratio of the resonant frequency to the switching frequency, a quasi-resonant converter must be designed at a relatively low switching frequency to maintain a practically feasible resonant inductor. Further, in converters like unclamped quasi-resonant converter, which operates at a variable switching frequency, the situation is worsened. Thus, the power density of this technique is limited.

1.4.3 Extending the input voltage range and load current range.

Due to excess energy spent in a series-parallel resonant converter in maintaining voltage in the parallel capacitor, soft-switching in unclamped quasi-resonant technique is lost at 20% of the rated load, and efficiency is also compromised. Further, due to the same reason, soft-switching cannot remain intact above 115% of the minimum input voltage [62]. On the other hand, a clamped quasi-resonant converter operates at a constant switching frequency though maintain soft-switching till 10% of rated load and 115% of minimum input voltage [54].

Upon close observation, it is evident that the limitations in power processing capability and power density are due to the high resonant frequency of the resonant tank, which leads to a small resonant inductance design. The solution to this problem can be achieved by bringing resonant frequency close to the operating switching frequency. This is possible through a load resonant converter concept, which is well explored in the voltage-fed converter type [67]-[90].

Considering the benchmarks set by LL type PWM converter [61], unclamped quasi-resonant converter [62]-[66], and clamped quasi-resonant converters [54] in terms of components' stress, components' count, and transformer utilization factor, the proposed converter adopts a resonant tank based on either series, parallel or modification of both to alleviate the above setbacks with the help of merits of load resonant converter as presented below.

In a load resonant converter resonant frequency lies close to the operating switching frequency. The ratio of resonant frequency to switching frequency is around 0.6 to 1.2. Therefore,

1. For a given switching frequency, a load resonant converter needs a higher and practically realizable resonant inductor than a quasi-resonant inductor [118].
2. The minimum ratio of resonant frequency to switching frequency of load resonant converter allows it to design at a very high switching frequency to increase power density while maintaining a practically feasible resonant inductor in the transformer [117].
3. A quasi-resonant converter allows a very limited range of soft-switching against variations in input voltage. On the other hand, a flexible resonant tank in a load resonant converter helps it to widen its input voltage and load current range [62].

This thesis studies load resonant converters characteristics' in the case of various resonant tanks to eliminate the above setbacks. The load resonant converters are studied to improve the efficiency of the interfacing converter especially under light load conditions to conserve maximum available energy and accelerate the RoI. On the other hand, the increase in switching frequency capacity, power processing capability, input and load range and flat efficiency curve of the load resonant converters opens up for medium and heavy duty applications like refrigerator trucks, long haul vehicles etc., as these applications need a power processing capability of tens of kilo watts for tens of hours which is otherwise not possible with available techniques intended which are intended for low power applications. In this direction, the following load resonant converters are studied.

1. A simple technique to model capacitive ended resonant converts using Fundamental Harmonic Approximation (FHA) analysis.
2. Current-fed high voltage gain LCC-T resonant converter in ZCS mode.

3. Current-fed high voltage gain LCC-T resonant converter in ZVS mode.
4. Three-phase current-fed LCC-T resonant converter in ZVS mode.
5. Current-fed high voltage gain LCL-SRC resonant converter in ZVS mode.
6. Current-fed high voltage gain (C)(L)(L)-SRC resonant converter in ZVS mode.

1.5 Thesis contribution.

The following are considerable contributions of the proposed thesis.

1. Though load resonant converters find several significant applications, due to their complexity in mathematical modeling and approximations, researchers find it difficult to explore in-depth. The easier technique, FHA analysis solves this issue except in case of parallel resonant tank adopted capacitive ended converters. Therefore, this thesis proposes a simple technique to ease the modeling of such converters. The proposed methodology is verified in theory and practice. Later, this method is instrumental in modeling the proposed load resonant converter topologies.
2. Various stages of a high voltage gain isolated DC/DC converter are explored to propose one with a facility to tune its characteristics based on the adopted resonant tank. Initially, a parallel resonance-based LCC-T resonant tank is considered and detailed steady-state operation, analysis, and modeling are done for below and above resonance regions. On designing and testing the converter finds to match with theoretical studies. Further, it showed an improvement in input voltage range and load range in both regions. However, the converter maintains constant switching frequency and ZCS switching if operated below resonance and needs hybrid modulation and maintains ZVS switching if operated above the resonance region. In both cases, the ratio of resonance frequency to switching frequency is maintained below one.
3. A three-phase topology of the proposed converter with the LCC-T resonance tank is also studied in this thesis. The operation and testing of this converter showed that the proposed technique is suitable for extending to higher power ratings while maintaining practically

realizable leakage inductance of the transformer. Also, there is a significant increase in input voltage range and load range.

4. To overcome setbacks that appeared on using a parallel resonance tank, a series resonance derivative tank LCL-SRC is studied and analyzed. On operating and testing of this converter revealed that the ratio of the resonance frequency to the switching frequency is as low as 1.1, current and voltage stress on the components of these converters are lesser, transformer utilization is significantly improved when compared to quasi-resonant converters. With an acceptable efficiency, the converter maintains soft-switching for a wide range of input voltage and load current variations. Also, expected complications in case of adopting an (L)(LC) -SRC a series resonance derived tank is also presented in this thesis.

1.6 Thesis outline

This section presents an outline of the thesis as follows.

1. Chapter 2 of this thesis explores various stages of a high-frequency high-gain isolated DC/DC converter. A DC/DC converter is proposed to tune characteristics based on the adopted resonant converter. On the other hand, modeling of a capacitive ended load resonant converter with parallel/series-parallel resonant tank is complex. Chapter 2 presents a simplified modeling technique using FHA analysis that becomes instrumental in modeling the proposed converter topologies in Chapters 3, 4, and 5.
2. Parallel resonance derived LCC-T tank is adopted in the proposed high voltage gain DC/DC converter and operated in below resonance mode to have ZCS switching of the switches. The steady-state operation, analysis, modeling, and design of the converter are presented in Chapter 3. The hardware prototype is developed to verify the claims such as wide range input voltage variations and load disturbances. This converter operates with simple PWM modulation.
3. Chapter 4 presents the variations in characteristics of the converter obtained by operating the converter, proposed in chapter 3, in the above resonance mode. The operation, analysis,

and design of the converter are presented. A proof-of-concept hardware prototype is developed and testing results are presented. This Chapter shows ZVS mode operation and maintains soft-switching for a wide range of input voltage variations and load disturbances. This converter offers reduced efficiency in the case of light loads and demands hybrid modulation.

4. Chapter 5 presents a three-phase topology of the converter studied in Chapter 4. It is designed for a relatively higher power rating. The operation, analysis, modeling, and design of the converter are presented. A hardware prototype is developed and testing results are presented to demonstrate the soft-switching and performance.
5. Chapter 6 presents LCL-SRC resonant high voltage gain DC/DC converter. This resonant tank is a dual of resonant tank used in Chapters 3, 4, and 5. The operation, analysis, modeling, and design of the converter are presented. The hardware prototype is developed, and experimental results are presented. A review of characteristics of the converter obtained with adoption of LCL-SRC resonant tank over LCC-T resonant tank is extensively discussed and presented. A comparison of the proposed topologies in this thesis with the existing converters in literature is also presented.
6. Chapter 7 presents the contributions and the concluding remarks of this thesis along with recommendations for possible future work.

1.7 Conclusion

This Chapter delineates the importance of reducing fossil-fuel consumption in saving the environment through the integration of non-conventional energy sources and distributed generation. Further, the role of high voltage gain isolated DC/DC converters is presented in interfacing the renewable sources, with the grid or micro-grid. The major requirements for the power conditioner are studied and discussed in this Chapter. Detailed literature review in view of finding a suitable DC/DC converter to match the requirements are studied. It is concluded that all the available voltage-fed and current-fed converters are not suitable to match the requirements of integrating a DC/DC converter for the given specifications and applications. Major challenges that appeared in matching the requirements are limitations in power processing capability, power

density, load regulation capability soft-switching range for input voltage and load current variations, and complexity in converter modulation. From the literature review, it is found that the load resonant converter holds the key to solve these challenges. Therefore, a current-fed load resonant converter is considered to pursue in this thesis to match the requirements of high voltage gain DC/DC converters because of inherent voltage gain capability, stiff input current, and reliability of it. This thesis's contributions and outlines are presented in this Chapter.

The next Chapter discusses of a high voltage gain dc/dc converter followed by a modeling technique to simplify FHA analysis.

Chapter 2 Simplified FHA Technique for Modeling of Resonant Converters with Capacitive Filter.

2.1 Introduction

High voltage gain DC/DC converters find several applications such as integration of PV panels, fuel cells, and batteries in microgrids [12], nano grids, battery chargers [13], electric power take-off systems [8], [9], etc., Further a high voltage gain converter with current-fed characteristics is preferred than a voltage-fed due to stiff input current and inherent voltage gain [16]. Also, load resonance is preferred over quasi resonance due to wide input voltage and load range [117] and simple PWM modulation. Therefore, section 2.2 of this Chapter aims at discussing a simple, low cost, efficient topology for current-fed high voltage gain soft-switching dc/dc converter [117]. Various stages of the high-gain dc/dc converter are studied in detail along with the merits and the demerits as available in the literature.

On the other hand, the high-gain dc/dc resonant converter, based on the load resonance technique, can be terminated with a capacitive filter. As presented in the literature, modeling of such a converter for the analysis and design turns complex mathematically. Therefore, section 2.3 presents a brief overview of existing techniques reported in the literature to model a resonant converter. Section 2.4 delineates the proposed modeling technique and verifies it in theory. Section 2.5 presents a detailed comparison of the proposed technique with conventional approaches. Section 2.6 presents simulation and experimental results and section 2.7 concludes.

2.2 Evolution of high voltage gain DC/DC converter

DC-DC converters play an important role in processing power harnessed from PV/fuel cells/battery [119]. Such converters need exceptionally high voltage gain, high power density, low

input current ripple, and high efficiency, higher reliability. Conventional boost converters are not able to meet the requirements. Voltage boosting techniques such as voltage multiplier cells [120] voltage lift techniques [121], and multi-stage converters [122] appear to be a suitable alternative. However, their need for high components' count to offer high voltage gain as demanded by these applications force them to compromise reliability. Converters [120]-[122] are hard switched, so they operate at relatively low switching frequency which leads to bulky magnetics.

On the other hand, DC-DC resonant converters with intermediate high-frequency (HF) AC link, as shown in Fig. 1.7 (a), can promise high voltage gain with soft-switching ability. Various stages of this kind of converters are 1. Front end inverter, 2. Soft-switching elements 3. HF transformer 4. Rectifier 5. Output filter. This soft-switching feature is interesting because it uses the leakage inductance of the transformer to eliminate switching losses, thus the converter can push its switching frequency to higher limits. Higher frequency helps magnetics to assume a much smaller size [25], making the converter compact and lighter.

2.2.1 Front-end inverter

In general, front-end inverters produce AC waveform to feed the following stages of the converter. For applications related to PV/fuel cell, a current-fed front-end inverter is preferable because of its continuous, ripple-free stiff input current and inherent voltage gain characteristic. Basic current source inverter, a dual of class-D voltage source counterpart, is reported in [123], which operates with parallel resonant tanks. The main advantage of this topology is that it needs only one inductor and 2 switches to generate the required AC waveform. But the requirement of bidirectional voltage blocking switches (realized by MOSFET and anti-series diode) complicates the design of the converter. Also, the converter should operate only at duty cycle 0.5 and with certain cross over conduction period to produce a balanced AC current waveform. This resorts the converter to adopt a frequency modulation technique for output voltage regulation.

Current-fed half-bridge converter (CFHB) proposed in [124], eliminates the need for bidirectional blocking switches for a current source inverter operation. Both the legs operate in an interleaved fashion with mandatory overlap time. This overlapping time ensures a closed

Table 2.1. Comparison of front-end inverters

	[123]	[124]	Active Clamped		
			Interleaved		[117]
			Boost [125], [126]	Cuk [9]	
Switches	2	2	4	4	2
Anti-series diodes	2	NA	NA	NA	NA
Inductors	1	2	2	2	1
Capacitors	-	-	1	2	2
d	0.5	>0.5	0<d<1	0<d<1	0<d<1
Soft turn- on	x	x	Yes	Yes	Yes

conduction path for input boost inductor currents and prevents switches from overvoltages. But the consequences of the overlap time are as follows. It imposes a minimum duty cycle for which each switch should operate for more than 0.5. The inability of the converter to operate in a lower duty cycle limits the converter to exhibit gains lower than 2N. Also, during start-up, jumping of duty ratio to 0.5 favors high inrush currents at start-up, which increases the switch current ratings.

To eliminate the requirement of overlap time, an active-clamping circuit is proposed for each leg called active clamped interleaved boost inverter [125], [126]. The auxiliary switch and main switch of each leg are operated in a complementary fashion to ensure continuous conduction for input boost inductor. This helps the converter to operate in full duty cycle ranging from 0 to 1 and the start-up problem is also eliminated. But this solution demands additional footprints of switches and clamp capacitor.

Ref. [54] uses an active clamped boost inverter, which uses only one leg of inverter proposed in [125], [126], and two clamp capacitors to produce AC waveform. The main advantage of this front-end inverter is a lesser number of components as seen in Table 2.1. On the contrary to the current fed inverters proposed in [125], [126], this inverter feeds a voltage waveform into the transformer. This is explained as follows. The input voltage v_{in} is transformed into a current

source through switching action on the input inductor and again converted to a voltage source by charging C_1, C_2. Later a quasi-square voltage is generated using C_1, C_2 to feed the transformer. This intermediate conversion looks unnecessary if a half-bridge voltage source inverter is directly used to feed the transformer [127]. But this inverter topology, with this intermediate conversion, provides two major advantages over half-bridge voltage source inverter. 1) A half-bridge voltage source inverter should operate at d=0.5 only to generate a transformer friendly AC waveform. So ultimately this converter needs frequency modulation for output voltage regulation. But the high-gain dc/dc current source inverter naturally provides AC voltage with zero DC component independent of the operating duty ratio. Therefore, this inverter can operate through a complete range of 0 to 1. Further, this converter can use simple PWM to regulate the output voltage. 2) A voltage source inverter is a buck type converter while this current source inverter is a buck-boost type converter. This inherent boost feature is needed to achieve high voltage gain. The common drawback of half-bridge voltage source inverter and current source inverter is that split capacitors should carry the circulating currents.

From Table 2.1, it can be observed that the active clamped boost inverter has a minimum number of switches, a minimum number of inductors, and can operate over a complete duty cycle range with no requirement of anti-series diode with soft turn-on capability. Due to these reasons, active-clamped boost inverter is selected as the front-end inverter in the high-gain dc/dc converter.

2.2.2 Rear-end rectifier and output filter

At the output port, a rectifier is needed. A simple class E rectifier is proposed in the literature for rectification purposes, which provides the soft-switching of the diodes [128]. It uses a capacitor across the diode for shaping its voltage so that it avails soft-switching. Marium mentions various types of rectifiers such as half-bridge, full-bridge, and Centre tapped in [129]. The voltage rating of the center-tapped rectifier diode is twice the output voltage and it needs dissipative snubber for operation. To eliminate these drawbacks in the centre tapped configuration, the Taiwan tech rectifier is proposed [130]. However, it comes with a complex transformer design. But [54] uses a voltage doubler (VDR), which offers rectification of ac voltage with soft-switching of diodes complemented with voltage doubling characteristic. Therefore, 2x voltage gain is merit

for application under study. Further, soft-switching of the diodes eliminates the need for snubbers across diodes, the ringing of diodes at the turnoff, and the need for fast recovery diodes.

2.2.3 Soft-switching strategy/elements

In the case of unidirectional converters, the soft-switching of the semiconductor devices is achieved through resonance caused by L_r and C_r. This resonance is segregated into 2 types.

2.2.3.1 Complete resonance/ Load resonance

A resonant tank is employed in power converters primarily to attain the soft-switching of the semiconductor devices. This resonant tank draws sinusoidal current from the inverter. These tanks also contribute to the overall voltage gain of the converter. Converters in [127] with *LC* filter and [125], [126] with *C* filter, employ a resonant tank between the inverter and the transformer for resonance, which not only brings soft-switching to the front-end inverter switches but also contributes to the overall voltage gain of the converter consequently reducing the transformer turns ratio. For a given power rating, as analyzed in [83], the overall *LC* filter is bulkier than a *C* filter, though the capacitor in *C* filter alone is bulkier than the one in the *LC* filter. Also, the type of filter used is independent of the type of input. Though resonant tanks of converters proposed in [127] and [85], [87] draw sinusoidal currents from the inverter, [127] can maintain sinusoidal currents through the transformer, while [85], [87] don't, because of the absence of *L* in output filter. i.e., [85], [87], show the merits of compact *C* filter at the output, and sinusoidal current in the transformer cannot be maintained simultaneously. Higher current stress in the transformer owing to non-sinusoidal current indicates poor transformer utilization. Under prolonged operation with high harmonic content in the transformer aggravates the temperature of the core and often leads to saturation.

2.2.3.2 Quasi resonance

In this method, for achieving soft voltage and current transition in switches, during turn-on or turn-off, resonance is invoked. This invoked resonance helps in the smooth transition of

switches. Resonance ceases at the end of transition [124]-[126], [61]. In general leakage inductance and/or magnetizing inductance of transformer and switch capacitances act as resonance components in quasi-resonant converters. The key advantage of this method is to utilize parasitic of the switch and transformer for resonance. But this method introduces non-sinusoidal currents through the transformer though it is connected in series with the resonating inductor. Also, elements L_r and C_r create a series resonance which does not contribute any voltage gain in the converter.

Akshay *et.al.,* [61] uses active clamped interleaved boost type as front end inverter for soft-switching. This converter can maintain soft-switching against wide load current and input voltage variations as required by the application. However, more components' count and poor utilization of the transformer are set back for this converter. Fei Shang *et.al.,* [9] uses an active clamped interleaved cuk as front end current source inverter. Though this converter has better transformer utilization, it is limited to one operating point i.e., at d=0.5. In other words, in course of regulating output voltage using d, harmonic content in current through the transformer is highly compromised. Also, the switch that carries a large portion of the current is completely hard switched during turn on and off. Dobakshari *et.al.,* [54], also uses active clamped boost type front

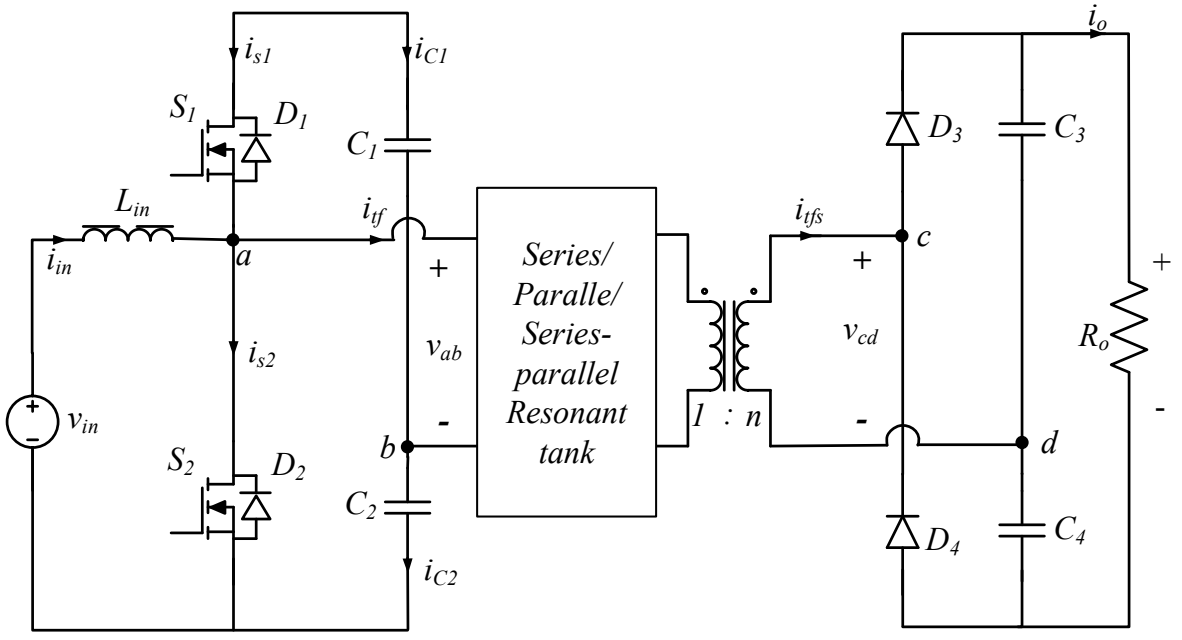


Fig. 2.1. Current-fed LCC-T resonant soft-switching converter operated in ZCS mode.

end inverter and quasi resonance for soft-switching. However, capacitors C_1, C_2 are difficult to design in this converter because, C_1, C_2 are resonating with transformer leakage to bring S_1, S_2 into soft-switching. So resonating capacitors C_1, C_2 cannot maintain a constant voltage across them. Since the total voltage across C_1, C_2 appear across the primary switches, the voltage peak across the switches will increase and so the voltage ratings of the switches. Even though soft-switching is maintained down to 20% of the load, the transformer is poorly utilized. Soft-switching against input voltage variation is also not reported.

2.2.4 The high-gain dc/dc resonant converter

In this Chapter a current-fed isolated load resonant DC-DC converter is discussed as shown in Fig. 2.1. The resonant tank can be based on either series resonance or parallel resonance or a combination of both. This converter uses an active clamped boost type front end inverter and complete resonance for soft-switching. The resonant tank, which is used for soft-switching of the front-end inverter switches, can completely integrate non-idealities of the high-frequency transformer. This is maintained down to 10% of full load and 150% of the minimum input voltage. The voltage doubler (VDR) employed at the output stage eliminates reverse recovery problems in VDR diodes by operating them in ZCS mode. This also enhances the gain of the converter by 2. Unlike [10], the discussed converter can ease the design of the capacitors C_1, C_2 by decoupling them from the resonance. This decoupling is made possible by selecting higher C_1, C_2 values relative to the capacitor (C_s) in the resonant tank. This makes the series equivalent of C_1 or C_2 with C_s equal to C_s itself so that they do not influence the resonance condition. Since C_1 and C_2 are not involved in resonance, the voltage across them is constant, thus switch voltage ratings are reduced. Also, the proper ratio among resonant tank components (such as series capacitor to parallel capacitor in LCC resonant tank and series inductor to the parallel inductor in LCL resonant tank) minimizes circulating currents through the components.

The main advantages of the high voltage gain dc/dc converter are 1) Its current source feature helps to draw PV/fuel cell/battery-friendly current. 2) ZCS of the switches is possible if the switching frequency is less than the resonant frequency. 3) ZVS of the switches is possible if the switching frequency is greater than the resonant frequency. 4) The converter can be operated

with simple PWM modulation at constant switching frequency if a suitable resonant tank and operating point are selected. 5) The secondary diodes are always commutated with ZCZVS, eliminating the need for reverse recovery. Therefore, rectifier grade diodes can be used. 6) Transformer parasitics do not create any spike across the switches because they are integrated into the operation of the resonant tank of the converter. On the other hand, the clamp capacitor, C_2, is destined to carry major portion of the resonant current and input current alternately. This effects the reliability of the converter from the point of view of electrolytic capacitors.

2.3 Modeling of Resonant Converters.

To keep up with the progressive demand for the compact and efficient power conversion technologies, a reduction in footprint, weight, and volume is necessary [119]. Resonant conversion technology, as shown in Fig. 2.2, can be a potential alternative. As reported in the literature, popular resonant converters such as the series resonant converter with capacitive filter [133],

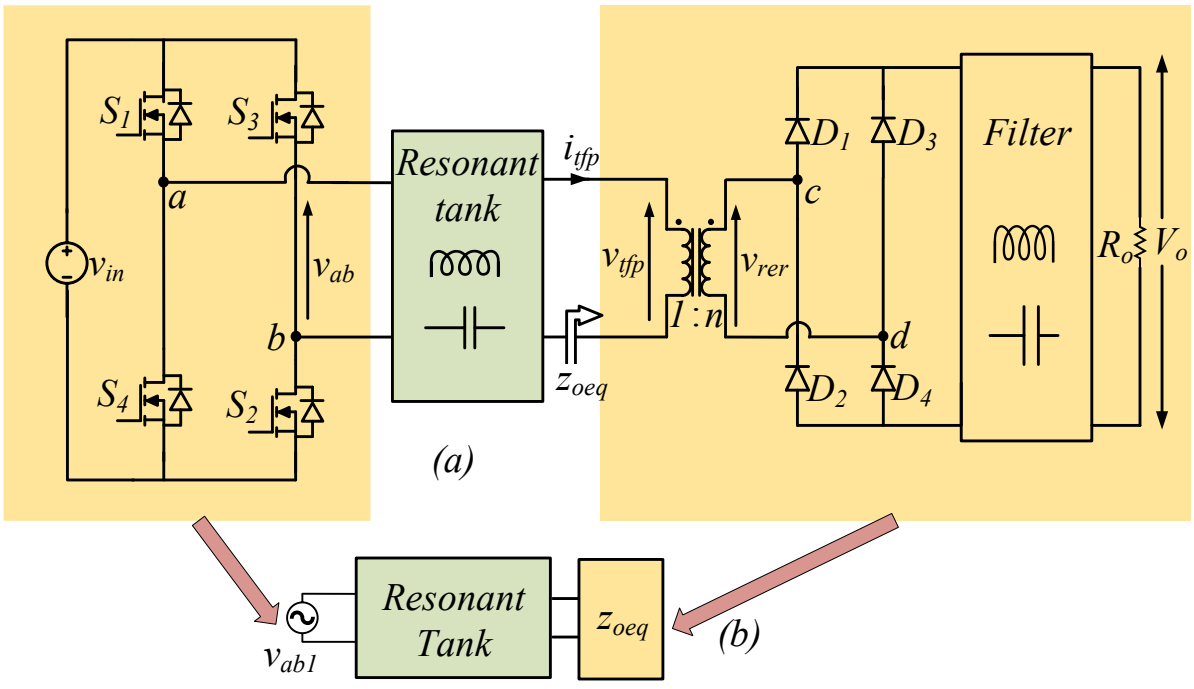


Fig. 2.2. (a) Block diagram of a voltage-fed isolated dc/dc resonant converter. (b) Equivalent Linear Sinusoidal (ELS) circuit

parallel and series-parallel resonant converter with LC and C filters [85], [127], [134]-[136], and LLC resonant converter [137], [138] are obtained by various combinations of inductor and capacitor in Fig. 2.2. These converters, due to their soft-switching abilities, can operate at high switching frequency resulting in reduced magnetics weight and footprint. Among them, series-parallel resonant converters carry all major advantages individually offered by series and parallel resonant converters while eliminating their drawbacks. With the proper selection of the resonant components, these converters offer reduced circulating current and better regulation under no-load condition, which is crucial to maintain high part load efficiency. Moreover, they turn transformer non-idealities into an asset by integrating them with the resonant tank. However, resonant converters are inherently non-linear thus suffer from complexity in the analysis and mathematical modeling of the converter.

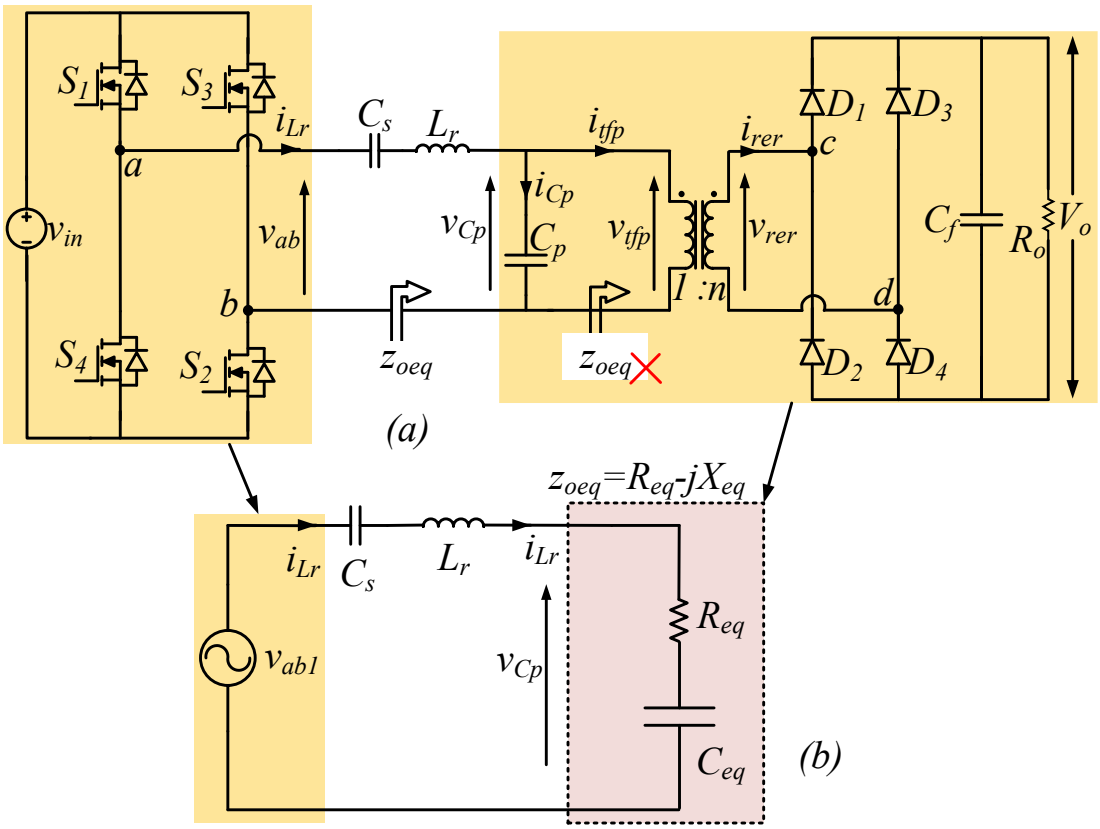


Fig. 2.3. (a) Voltage-fed LCC resonant converter with capacitive filter. (b) ELS model of voltage-fed LCC resonant converter with capacitive filter.

To design a converter in practice, analysis and mathematical modeling are necessary. But in the case of the resonant converters due to 1) higher number of state variables, 2) load-dependent operating intervals, and 3) nonlinearities offered by front-end inverter and RER, conventional techniques such as time-domain [133], [135], [136], state-space [85], [127], [134] and state-plane [138] approaches proved to be cumbersome. Grove, as an alternate, introduced generalized technique, grove's method that can model PWM, resonant and quasi-resonant converters simultaneously. Further, complexities in the implementation of the grove's method are addressed through the Extended Describing Function (EDF) method [139]. However, all these methods are inherently complex and resort to computer-aided techniques to determine the mathematical model, which eventually frustrate designers to explore.

To alleviate the labor involved in the mathematical modeling, Steigward proposed Fundamental Harmonic Approximation (FHA) analysis, which avails classical AC analysis

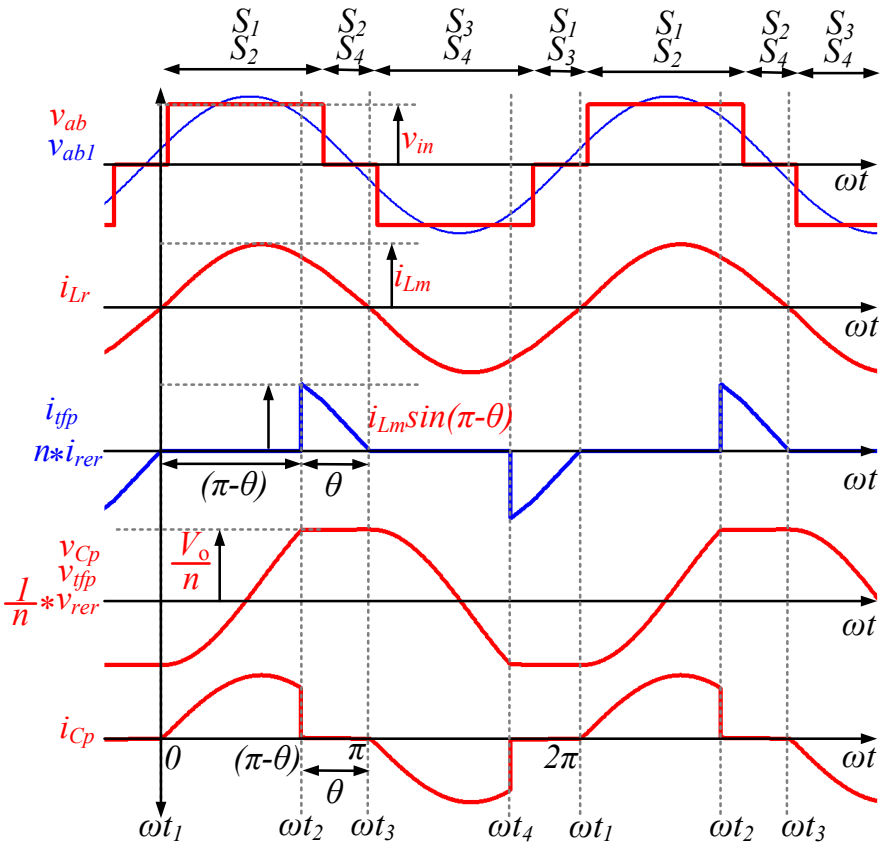


Fig. 2.4 Operating waveforms of voltage fed isolated LCC resonant converter with capacitive filter

techniques to derive mathematical models with relative ease [140]. This method briefly, converts nonlinear, non-sinusoidal resonant converter, as shown in Fig. 2.2(a), into Equivalent Linear Sinusoidal (ELS) circuit with RLC components as shown in Fig. 2.2(b) [26]. Later, vital modeling relations such as voltage gain, current and voltage stress, etc. can be developed with classical AC analysis techniques. Derivation of ELS circuit involves 1) replacing the nonlinear front-end inverter with an equivalent sinusoidal first harmonic voltage source and 2) replacing the transformer, RER, filter, and load with equivalent resistance or impedance (z_{oeq}), which accounts for the non-linear behavior of loaded RER. Calculation of z_{oeq} with minimum efforts maintains the simplicity and elegance of FHA analysis. For this, the following three conditions are to be satisfied [141].

1) Operation under steady-state
2) Continuous current flow into z_{oeq}
3) Power consumed by z_{oeq} is through the first harmonic.

Converters such as the series resonant converter terminated with a capacitive filter, a parallel resonant converter terminated with an *LC* filter, *LCC* resonant converter terminated with an *LC* filter, and *LLC* resonant converters satisfy the above conditions to develop z_{oeq} with ease. Therefore, FHA looks simple and elegant as adopted in those cases [140]. However, in the case of the parallel *(LC)* and series-parallel *(LCC)* resonant converters with a capacitive filter, conditions 2 and 3 from the list are violated [83], [86], [87], [142], [143]. Therefore, the calculation of z_{oeq} turns cumbersome and needs computer-aided techniques such as numerical analysis [143] and curve-fitting methods [86]. Overall, this shows that FHA analysis, when applied to parallel *(LC)* and series-parallel *(LCC)* resonant converter with a capacitive filter, loses its simplicity, elegance, accuracy, and suffers from the similar drawback as in the case of time-domain and state-plane approaches [86], [87], [143].

On the other hand, the parallel resonant capacitor is included in z_{oeq} to expedite modeling of four [144], [145], and five [99] element resonant converter. This chapter extends this simple technique to alleviate complexities in calculating z_{oeq}, which in turn restores the simplicity of FHA analysis for *LC* and *LCC* resonant converters with capacitive filters. Further, a detailed comparison

$$V_{Cpa_1} = \frac{2}{\pi}\frac{V_o(1-\cos\theta)}{n(1+\cos\theta)}\left[\sin\theta - \frac{(\pi-\theta)-\sin\theta\cos\theta}{(1-\cos\theta)}\right] + \frac{2V_o}{n\pi}(-\sin\theta) \tag{2.10}$$

$$V_{Cpa_1} = -\frac{2V_o}{n\pi}\left(\frac{(\pi-\theta)+\sin\theta\cos\theta}{1+\cos\theta}\right) \tag{2.11}$$

$$V_{Cpb_1} = \frac{2}{\pi}\frac{V_o(1-\cos\theta)}{n(1+\cos\theta)}\int_0^{\pi-\theta}\left[1-\frac{2\cos\omega t}{(1-\cos\theta)}\right]\sin\omega t\, d(\omega t) + \frac{2V_o}{n\pi}\int_{\pi-\theta}^{\pi} 1.\sin\omega t\, d(\omega t) \tag{2.12}$$

$$V_{Cpb_1} = \frac{2}{\pi}\frac{V_o(1-\cos\theta)}{n(1+\cos\theta)}\left[(1+\cos\theta) - \frac{\sin^2\theta}{(1-\cos\theta)}\right] + \frac{2V_o}{n\pi}(1-\cos\theta) \tag{2.13}$$

$$V_{Cpb_1} = \frac{2V_o}{n\pi}(1-\cos\theta) \tag{2.14}$$

$$z_{oeq} = \frac{v_{Cp1}}{i_{Lm}} = \left(\frac{sin^2\theta}{\pi\omega C_p}\right) - j\left(\frac{\pi-\theta+sin\,\theta\,cos\,\theta}{\pi\omega C_p}\right) \tag{2.15}$$

$$R_{eq} = \frac{sin^2\theta}{\pi\omega C_p}; \qquad C_{eq} = \frac{\pi C_p}{\pi-\theta+sin\,\theta\,cos\,\theta} \tag{2.16}$$

$$z_{oeq[142]} = \frac{8n^2}{\pi^2}R_o \tag{2.17}$$

with existing modeling techniques [86], [142], [143] is presented, and the proposed theory is validated through simulation and experimental results. Though the proposed method is demonstrated through the series-parallel *(LCC)* resonant converter with a capacitive filter, it is being equally valid for the parallel *(LC)* resonant converter terminated with a capacitive filter.

2.4 Proposed ELS Circuit

The voltage fed *LCC* resonant converter terminated with a capacitive filter is shown in Fig. 2.3(a) and its operating waveforms are shown in Fig. 2.4. The operation of the converter under discussion is elaborated in several manuscripts [86], [87], therefore discussed briefly here. The front-end inverter generates a quasi-square voltage. During power transfer mode ($\omega t_2 < \omega t < \omega t_3$), parallel capacitor voltage (v_{Cp}) is clamped by output voltage (V_o) and resonant current (i_{Lr}) supplies

$$v_{\eta} = v_{cp} - v_{sq} \tag{2.18}$$

$$r_{sq[143]} = \frac{8R_o}{\pi^2\left(1 + 4R_o f_s C_p\right)} \tag{2.19}$$

$$r_{\eta[143]} = \frac{-32 f_s C_p R_o^2}{\pi^2\left(1 + 4R_o f_s C_p\right)^2} \tag{2.20}$$

$$c_{\eta[143]} = \frac{\pi I_{in}^2 C_p\left(16 f_s^2 C_p^2 R_o^2 + 8R_o f_s C_p + 1\right)}{\left(16 I_{in}^2 R_o^2(\pi - \gamma_1) f_s^2 C_p^2\right) + \cdots\cdots\cdots + (\pi - \gamma_1) I_{in}^2 - 4\gamma_2 I_{in}} \tag{2.21}$$

$$z_{oeq[143]} = R_{l[143]} + R_{eq[143]} \text{-} j\left(\frac{1}{\pi\omega C_{eq[143]}}\right) \tag{2.22}$$

the load. Similarly, during non-power transfer mode ($\omega t_1 < \omega t < \omega t_2$), the entire i_{Lr} engages in charging the parallel capacitor (C_p) and the filter capacitor feeds the load. Due to this reason C_p voltage (v_{Cp}) or RER input voltage (v_{rer}) is a clamped sinusoidal. Further, the current drawn by RER (i_{rer}) and i_{tfp} are discontinuous i.e., neither sinusoidal nor square as shown in Fig. 2.5.

Respecting bandpass filter characteristics of LCC resonant tank, FHA analysis allows to approximate i_{Lr} as sinusoidal given by (2.1), and the front-end inverter with equivalent first harmonic voltage (v_{ab1}), given by (2.2). To restore the simplicity and elegance of FHA, the proposed analysis suggests considering z_{oeq} as seen from C_p, instead of the transformer. This modification helps the converter under discussion to satisfy all the conditions to develop z_{oeq} with the minimum efforts such as continuous current flowing into z_{oeq} and power consumed by z_{oeq} be first harmonic. With this modification, the development of z_{oeq} turns simpler and is calculates as follows.

Eq (2.3) gives resonant current flowing into C_p, while the peak of resonant current is given by (2.4). The secondary diode conduction angle (θ) is given by (2.5) [83], [86], [87]. Using (2.3), (2.5) v_{Cp} and its first harmonic component (v_{Cp1}) are defined as (2.6) and (2.7) respectively. Eq. (2.8) represents v_{Cp1} in rectangular coordinates. Further, components of first harmonic, v_{Cpa1} and v_{Cpb1}, are defined by (2.9)-(2.14). Since current drawn by z_{oeq} is sinusoidal, power consumed by z_{oeq} is contributed by first harmonic. Therefore, z_{oeq} is calculated as (2.15) and equivalent resistance

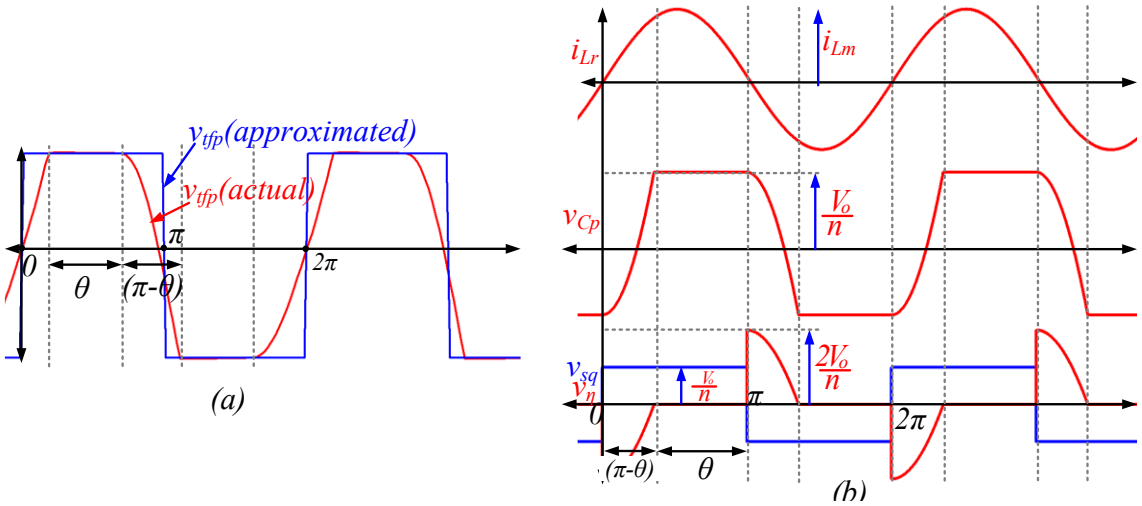


Fig. 2.5. (a). Approximations adopted in [142], (b). Splitting of v_{Cp} adopted in [143].

(R_{eq}) and equivalent capacitance (C_{eq}) as (2.16). Using classical AC techniques, vital relations such as voltage gain of the converter, resonance current stress, voltage stress on series and parallel capacitors of the series-parallel resonant converter with capacitive filter can be derived easily.

2.5 Comparison with existing techniques

Unlike [86] and [143], the development of z_{oeq} in the proposed method is simpler. Though z_{oeq} developed in [142] is simple, it is based on another approximation: the input voltage of the transformer is a square wave, as shown in Fig. 2.5(a). This assumption is invalid under light load conditions. Therefore, as the load demand or input voltage drops, developed the ELS circuit, as shown in Fig. 2.6(a), and vital relationships predicted by the ELS circuit deviate significantly from actual conditions. Equivalent impedance is given by (2.17).

Another technique proposed to develop z_{oeq} as a part of the FHA analysis involves the splitting of v_{Cp} into two components v_{sq} and v_η as shown in Fig. 2.5(b) [143]. Of them, v_{sq} is a square voltage with magnitude equal to the reflected output voltage and is in phase with the resonant current (i_{Lr}) and v_η is the residual voltage as defined by (2.18). This approach of splitting voltages to calculate z_{oeq} leads to the ELS circuit, shown in Fig. 2. 6(b), with complex z_{oeq} as given by (2.19), (2.20), (2.21) and (2.22). To develop vital relations such as voltage gain, current and voltage stress on

$$k_v = \frac{2\sqrt{(\theta-\pi)^2 + sin^4\theta}}{\pi(1+\cos\theta)} \cong 1 + 0.27sin\frac{\theta}{2} \tag{2.23}$$

$$\beta = \tan^{-1}\left[\frac{\left((\theta-\pi)(2\theta - sin2\theta) + (1-cos2\theta)sin^2\theta\right)}{(sin^2\theta)(2\theta - sin2\theta) - (\theta-\pi)(1-cos2\theta)}\right] \cong -25sin\theta \tag{2.24}$$

$$R_{eq[86]} = \frac{R_o}{2n^2}k_v^2 \tag{2.25}$$

$$C_{eq[86]} = \frac{2n^2}{\omega R_o}\frac{tan\beta}{k_v^2} \tag{2.26}$$

$$z_{oeq[86]} = R_{eq[86]} // \left(\frac{1}{j\pi\omega C_{eq[86]}}\right) \tag{2.27}$$

resonant capacitors involves complicated terms and thus mandates to approach iterative methods such as the Newton-Rapson method for the solution.

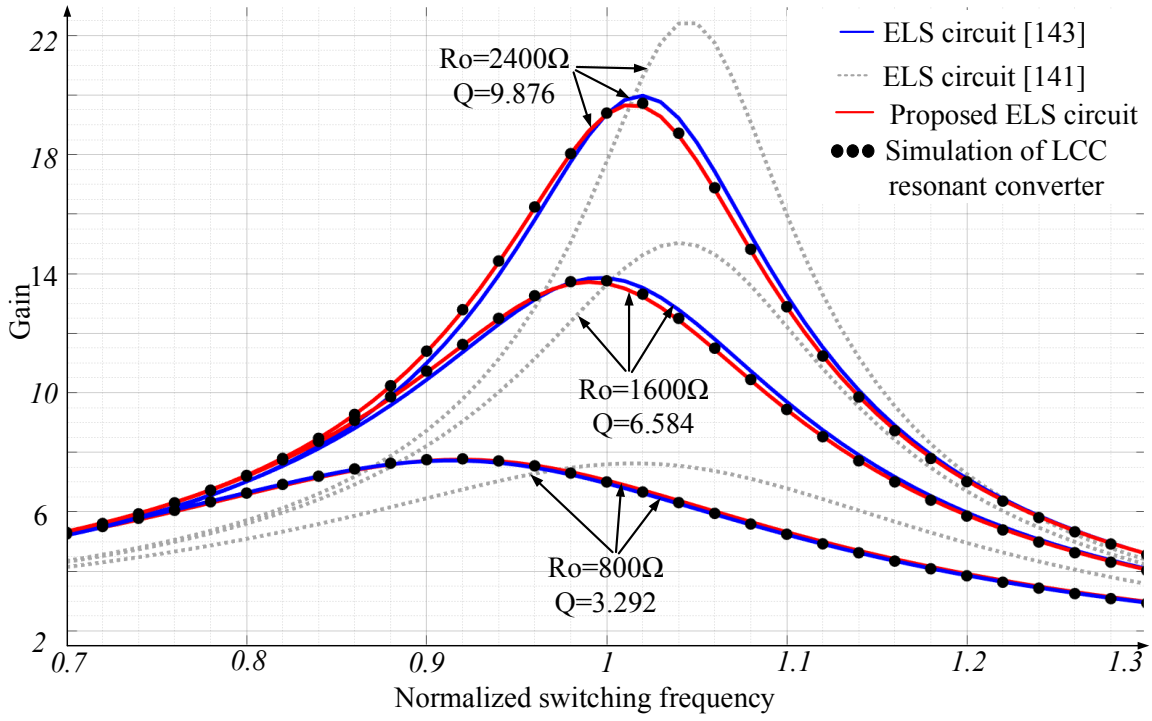


Fig. 2.6. Comparison of voltage gain predicted by proposed ELS circuit, [141], [143] with voltage gain obtained through simulation of actual LCC resonant converter.

Similarly, [86] proposes a technique to obtaining an ELS circuit for a series-parallel resonant converter with a capacitive filter using FHA analysis. This method, to calculate $z_{oeq,}$ focuses on replacing the transformer, RER, filters, and loads with equivalent impedance z_{oeq}, which consumes the same power as consumed by the load and subtends the required phase angle. Calculation of z_{oeq} is highly complex since it completely depends on discontinuous i_{tfp} and v_{tfp}, which includes huge harmonic content as shown in Fig. 2. 4. This resort to curve fitting methods to approximate (2.23) and (2.24) which compromises accuracy. z_{oeq} is given as (2.25), (2.26), and (2.27) without that developing equivalent model and its further analysis would be complicated. The corresponding ELS circuit is given as Fig. 2.6(c).

The Proposed method arrives at the ELS circuit, as shown in Fig. 2.6(d), with minimum approximations, which is calculated using a free hand; eliminating the requirement of the computer aided techniques such as iterative or cure fitting. This accelerates the calculations and analysis of the converter with accuracy. A comparison is provided in table 2.2. Besides, the proposed ELS circuit agrees with the steady-state model of the LCC resonant converter derived by the EDF method [85], [146], and verifies the authenticity of the proposed FHA analysis.

2.6 Simulation and Experimental Results.

The purpose of the developed ELS circuit is to mimic the original circuit mathematically. Therefore, currents drawn by and voltages developed in the ELS circuit are expected to comply with the actual voltage-fed LCC resonant converter. Further, vital relations such as voltage gain, resonant current and voltage stress predicted by the ELS circuit should in accordance with actual converter performance. Therefore, for verification, operation of voltage-fed LCC resonant converter defined by V_{in}=30V, L_r=150.4uH, C_p=206nF, C_s=2.06uF, f_{sw}=17-40kHz is considered as reference. A simulation set-up of the proposed ELS circuit is mounted in PSIM 11.0. Tests are repeated for various loads and frequency of operations covering below and above resonance regions. Simulation results for the two different conditions are presented in Fig. 2.7. This shows that the developed ELS circuit can mimic the actual converter.

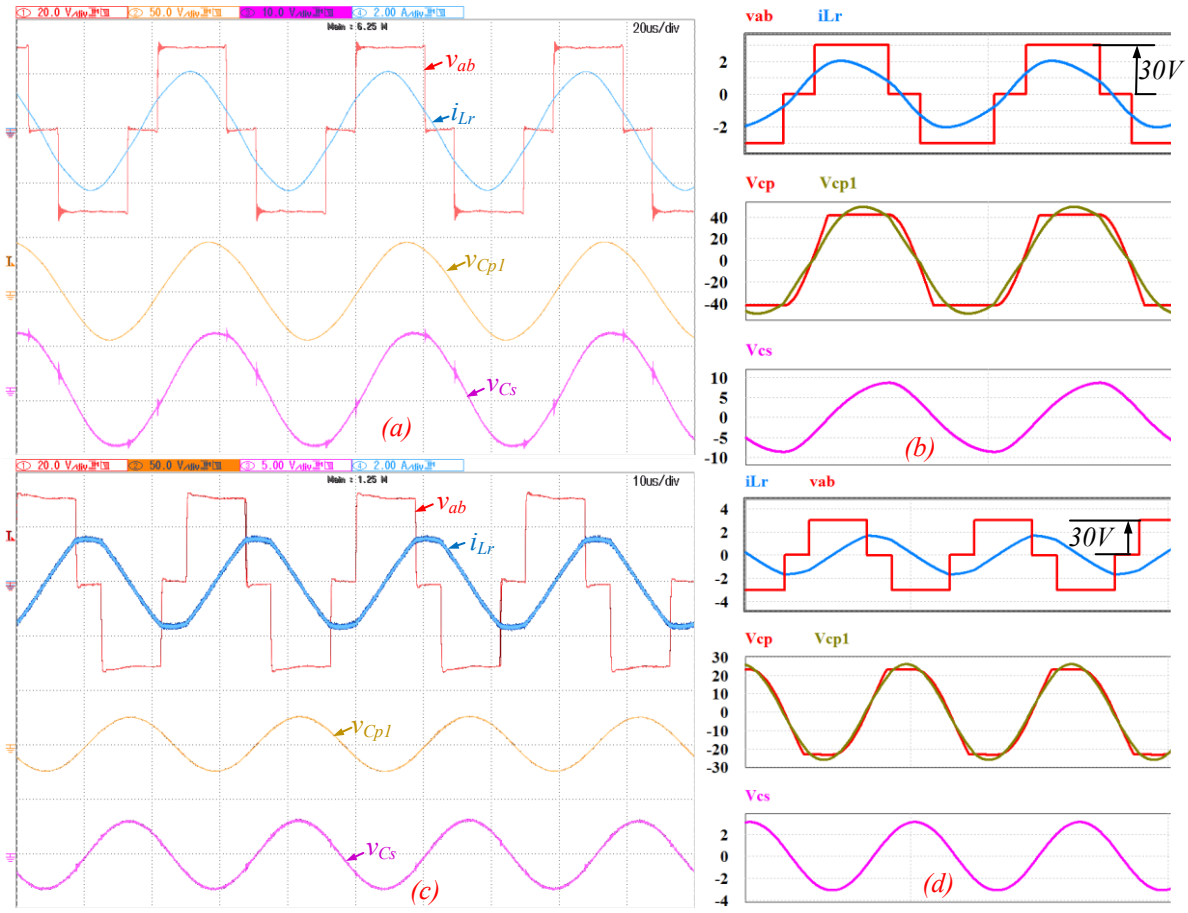


Fig. 2.7. (a) Testing of proposed ELS circuit for R_o=600Ω and f_{sw}=17kHz (b) Simulation of LCC resonant converter for R_o=600Ω and f_{sw}=17kHz (c) Testing of proposed ELS circuit for R_o=800Ω and f_{sw}=40kHz (d) Simulation of LCC resonant converter for R_o=800Ω and f_{sw}=40kHz.

Resonant capacitor voltage (v_{Cp}) of the LCC resonant converter is piecewise linear, while it's first harmonic (v_{Cp1}) given by (2.8) is linear, as shown in Fig. 2.7. Comparisons shown in Fig. 2.8 also reaffirms this fact. The accuracy of the proposed method in comparison to the existing methods is demonstrated through Fig. 2.9 in Table 2.2. Due to unjustified approximations in Fig. 2.5(a), [142] exhibits significant error from the original operation and

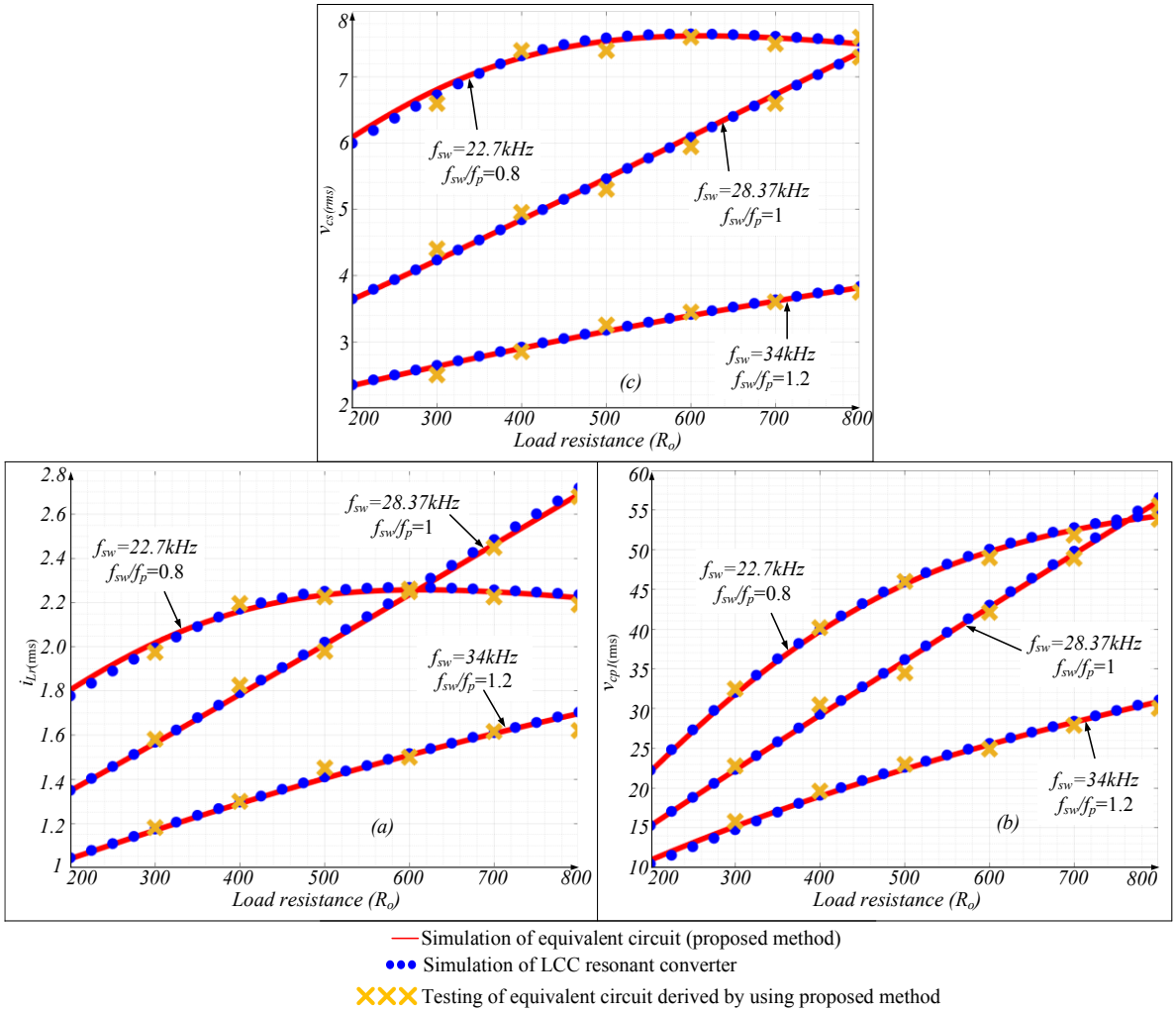
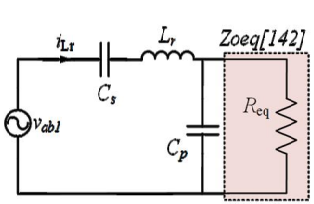
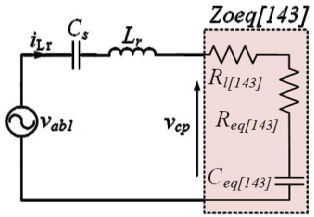
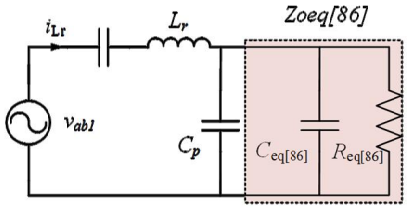
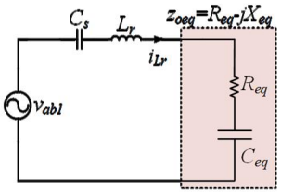


Fig. 2.8. Comparison of actual converter simulation with proposed ELS circuit simulation and experimental for (a) resonant inductor current stress (i_{Lr}), (b) parallel resonant capacitor voltage stress (v_{Cp}), (c) series resonant capacitor voltage stress (v_{Cs})

worsens with load reduction. Similarly, approximations adopted in (2.22), (2.23) in [86] also appear as an error in predicted values, which dominates under the light load. However, the proposed method, which is free from approximations except for FHA is able to develop an accurate ELS model and is valid through all loading conditions and frequencies.

Table 2.2. Comparison of proposed technique with various techniques proposed in literature

	[142]	[143]	[86]	Proposed technique
ELS Circuits	 Fig. 2.9 (a)	 Fig. 2.9 (b)	 Fig. 2.9 (c)	 Fig. 2.9(d)
z_{oeq}	(2.17)	(2.19), (2.20), (2.21) and (2.22)	(2.23), (2.24), (2.25), (2.26) and (2.27)	(2.15), (2.16)
Remarks	Highly inaccurate due to assumption in Fig. 4(a).	Accurate but unclosed solution (2.21).	Slightly less accurate due to approximation in (2.23), (2.24).	Accurate, closed solutions, no approximations
	Simple and easy to develop	Requires numerical methods	Requires curve fitting methods.	Simple, easy and elegant to develop

2.7 Conclusion

This Chapter discusses a high voltage gain DC/DC load resonant converter followed by a simplified technique to model it. The characteristics of the high-gain dc/dc converter can be tuned with the resonant tank adopted with it. Several merits of the discussed converter are 1) Its current source feature helps to draw PV/fuel cell/battery-friendly current. 2) ZCS of active switches is attained if the switching frequency is less than the resonant frequency. 3) ZVS of active switches is attained if the switching frequency is greater than the tank resonant frequency. 4) Converter can be operated with simple PWM modulation at constant switching frequency if a suitable resonant tank and operating point are selected. 5) Secondary diodes or RER diodes are always operated with ZCZVS turn off, eliminating the need for reverse recovery. Therefore, rectifier grade diodes can be used. 6) Transformer parasitics cannot create any spike across the switches as they are integrated into the operation of the resonant tank of the converter.

Simplified modeling of resonant converters is a challenge due to numerous steady-state variables. Conventional time domain, state-space, and state plane approach, though accurate, are laborious and complicated in approach thus resort to computer aided techniques. Even though the FHA technique can simplify the modeling of resonant converters, it fails in the case of parallel and series-parallel resonant converters with capacitive filters. Existing FHA techniques allow a few approximations to simplify the modeling of such converters at the cost of inaccuracy and complexity. This chapter proposes a technique to restore the simplicity of FHA analysis for such cases. This technique reports modifications in calculation of the equivalent impedance, which in turn simplifies and improves the accuracy of modeling. The accuracy and ability of the proposed equivalent linear sinusoidal (ELS) circuit to mimic the actual series-parallel resonant converter with the capacitive filter are verified through simulation and experimental platforms. Further, the proposed technique is equally valid in the case of a parallel resonant converter terminated with a capacitive filter.

The next chapter focusses on tuning the characterstics of the discussed converter to match the requirements laid down in Chapter 1 using a resonant tank derived from the parallel resonance.

Chapter 3 Analysis and Design of ZCS Current-fed Isolated LCC-T Resonant Converter

In Chapter 2, the evolution of a high voltage gain soft-switching dc/dc converter and corresponding modeling technique is proposed. This Chapter evaluates the characteristics and operation of the proposed converter in the case of the resonant tank, LCC-T, which is based on parallel resonance with the hope of achieving converter requirements as mentioned in Chapter 1. Since the LCC-T resonant tank is based on parallel resonance, the gain offered by the resonance tank to overall converter gain helps in relaxing turns ratio burden on the transformer.

3.1 Introduction

The proper interconnection of inductors and capacitors can form a resonant tank. This resonant tank, when connected to an alternating voltage source, can draw currents either lagging or leading with the voltage source waveform. Such lagging/leading current drawn by the resonant tank in DC/DC converters as proposed in Chapter 2, can make the converter operate in ZVS/ZCS type of soft-switching. A series resonant tank under resonance condition offers a maximum gain, unity. On the other hand, dual of series resonance and parallel resonance tank can offer gain higher than unity.

In this Chapter, boost characteristics of parallel resonance tank are sought to lighten the burden on the transformer turns ratio to achieve high voltage gain in the proposed converter. However, only a parallel resonant tank is not preferred in the soft switching because of the nature of the parallel resonant tank to maintain constant resonance current in the converter irrespective of the load current. This leads to higher conduction losses in the resonant tank components and the front end inverter (FEI) switches. Therefore, to avail the boosting capability of the parallel resonant tank, the three-element resonance tank, LCC as shown in Chapter 1, is analyzed. Upon adding a

Table 3.1. Comparison of stress on LCC and LCC-T resonant tank components

	LCC	LCC-T	% decrement in stress
I_{Lm}	18.02A	16.66A	7.5
V_{Cp}	126.9V	124.98V	1.5
V_{Cs}	16.13V	3.29V	79.6
d	0.354	0.372	-
f_{sw}	150k	150k	-
I_{Cspeak}	18.02A	12.22A	32.1
I_{Cs_rms}	12.74A	4.47A	64.9

resonant capacitor in series with resonant inductor forms LCC resonant tank. The ratio of the parallel capacitor to the series capacitor (λ) decides the domination of either parallel or series resonance in the converter. Furthermore, proper selection of λ brings down circulating currents in converter under light load conditions.

One can observe that a series resonant capacitor in the LCC tank is not only attenuating resonant current under light load conditions but also enduring entire resonant current stress that in turn increases conduction losses. Therefore, using the equivalence resonance concept, equivalence of LCC, i.e., LCC-T resonant tank is introduced in this chapter which carries all merits of parallel resonance as an LCC resonant tank with reduced current stress and voltage stress across resonant tank components as an added advantage. This is verified for resonance tank LCC and LCC-T in a classical voltage source dc/dc converter, shown in Fig. 2.3(a) and a comparison is presented in Table 3.1. A list of components used for simulation is mentioned in Table 3.2. This shows that an LCC-T resonant tank based on the parallel resonance can offer voltage gain while maintaining lower stress on the resonant tank.

Table 3.2. Resonant tank components used for evaluating stress on LCC and LCC-T tank

	LCC	LCC-T
n	3	3
L_r	9.31μH	8.73μH
C_p	0.1149μF	0.10787μF
C_s	1.149μF	1.0787μF

3.2 Proposed converter with LCC-T resonant tank.

In this Chapter, a current-fed isolated LCC-T resonant DC-DC converter is proposed as shown in Fig. 3.1. This converter uses an active clamped boost type front end inverter and complete resonance for soft switching. A resonant tank, LCC-T, which completely integrates the non-idealities of the transformer, is used to achieve zero current switching (ZCS) operation of the front-end inverter switches. This is maintained down to 10% of full-load and 150% of the input voltage. In this tank, the series resonance capacitor, in series with resonance inductor unlike LCC, is not supposed to carry complete circulating currents. Since the resonant inductor maintains sinusoidal current, so the same is injected into the transformer and thus better transformer utilization is assured against wide load and input variations.

The voltage doubler (VDR) employed at the output eliminates reverse recovery problems in VDR diodes by operating them in ZCS mode. This also enhances the gain of the converter by 2x. Unlike [54], the proposed converter can ease the design of the capacitors C_1, C_2 by decoupling them from resonance. This decoupling is made possible by selecting higher C_1, C_2 values relative

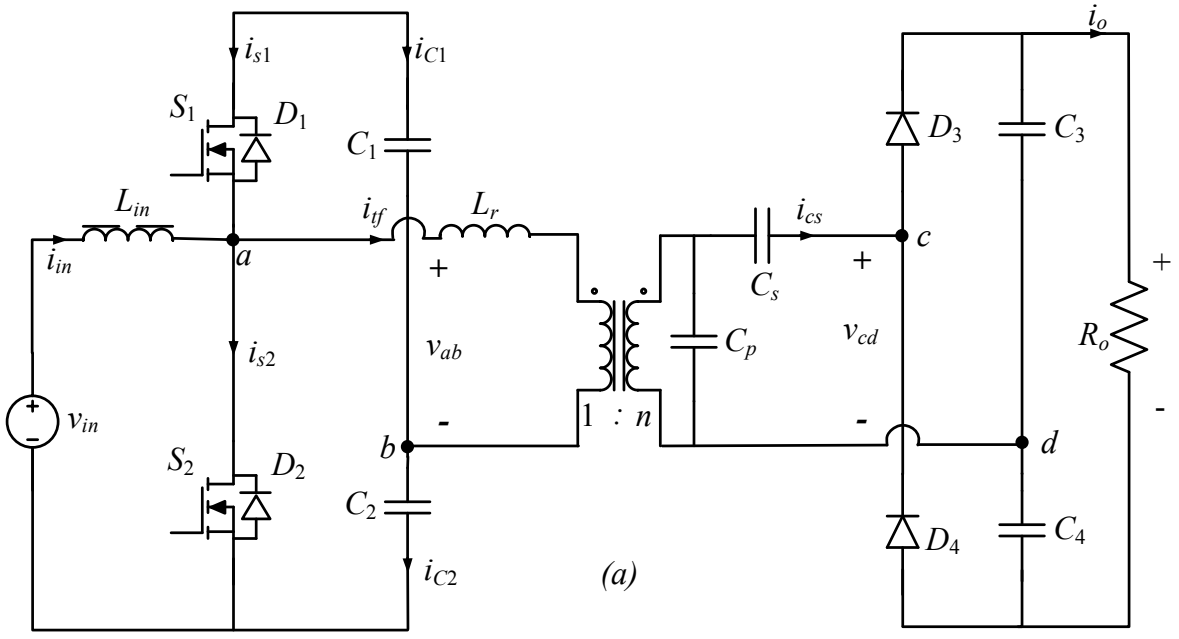


Fig. 3.1. Current-fed LCC-T resonant soft switching converter operated in ZCS mode.

to C_p in the LCC-T tank. This makes the series equivalent of C_1 or C_2 with C_p equal to C_p itself so that they do not influence the resonance condition. Since neither C_1 nor C_2 is involved in resonance the voltage across them is constant and thus switch voltage ratings are reduced. Also, a proper ratio among resonant tank capacitors (λ) minimizes the circulating currents. The main advantages of the proposed converter are 1) Current source feature helps to draw PV/fuel cell friendly stiff dc current. 2) ZCS of all semiconductor switches at a constant frequency of operation is maintained against wide load and input voltage variation. 3) Simple pulse width modulation is adopted for load regulation.

3.3 Operation of the Proposed Converter in ZCS mode

This section is dedicated to delineating the various operating modes of the converter for one complete high-frequency switching cycle. The operation of the converter is presented with reference to resonant inductor current, i_{Lr}. The following assumptions are made for the steady-state analysis of the converter. *1)* The resonant inductor current i_{Lr} is assumed as sinusoidal current. *2)* The input inductor L_{in} is large enough to maintain stiff input current. *3)* The output capacitors C_3, C_4 are large enough to maintain constant load voltage. *4)* The transformer has infinitely large magnetizing inductance. *5)* L_r is the leakage inductance of the transformer or an external series inductor that can integrate with the leakage inductance of the transformer. 6) G_1, G_2 are the gate to source voltage signals for S_1, S_2 respectively. 7) D_1, D_2 are the body diodes of S_1, S_2 respectively.

Diodes D_3 and D_4 are connected to develop the output rectifier stage. Diodes D_3 and D_4 get forward bias if v_{cd} is $V_o/2$ and $-V_o/2$ respectively, else they are in blocking mode. The operation of the converter at high frequency is explained with the help of waveforms presented in Fig. 3.2 and corresponding equivalent circuits are shown in Fig. 3.3. Capacitors C_1 and C_2 are considered as non-resonant elements because C_1, C_2 values are far larger than C_p, thus their series equivalent equals to C_p value itself.

3.3.1 Mode 1. (Fig. 3.3 (a). $\omega t_o<\omega t<\omega t_1$)

This mode begins with the i_{Lr} turning to positive and this time instant is taken as reference for operation and analysis of the converter. From Kirchoff's current law (KCL), it is obvious that switch S_2 carries a combination of i_{Lin}, i_{Lr}. Since i_{Lr} turned positive, this helps in diverting a portion of i_{Lin}, which is being carried by switch S_2, directly into L_r. This can be seen by falling current in S_2 and is given as i_{Lin}-i_{Lr}. Since $V_{dc}<V_o/2$ D_3 turns off. During this mode, as no current is flowing through C_s, it maintains a constant voltage. This mode ends when the current through the S_2 reaches zero.

3.3.2 Mode 2. (Fig. 3.3 (b). $\omega t_1<\omega t<\omega t_2$):

This mode begins as soon as the body diode of S_2 starts conducting. From KCL, $i_{S2}=i_{in}$-i_{Lr}. C_p keeps charging and C_3, C_4 are feeding the load. This mode ends with the withdrawal of the gate to source voltage signal, G_2. At this turn-off instant, negative switch current in S_2, according to [129], [132], indicates zero current turn-off (ZCS).

3.3.3 Mode 3. (Fig. 3.3 (c). $\omega t_2<\omega t<\omega t_3$):

This mode begins with the turn-on of S_1. The turn-off current in the body diode of S_2 is transferred to S_1. In this mode, i_{Lin} is fed to C_2 to charge it. Since D_3, and D_4 is still off, i_{tfs} is completely feeding C_p alone. C_3 and C_4 are feeding the load.

3.3.4 Mode 4. (Fig. 3.3 (d). $\omega t_3<\omega t<\omega t_4$)

This mode begins when v_{cd} reaches $Vo/2$ and so D_3 gets forward bias allowing i_{tfs} share between C_p and C_s. A portion of the current that is entering C_s *i.e.,* i_{Cs} charges C_3 while C_4 and i_{Cs} are feeding the load. This mode ends with S_1 current reaching zero.

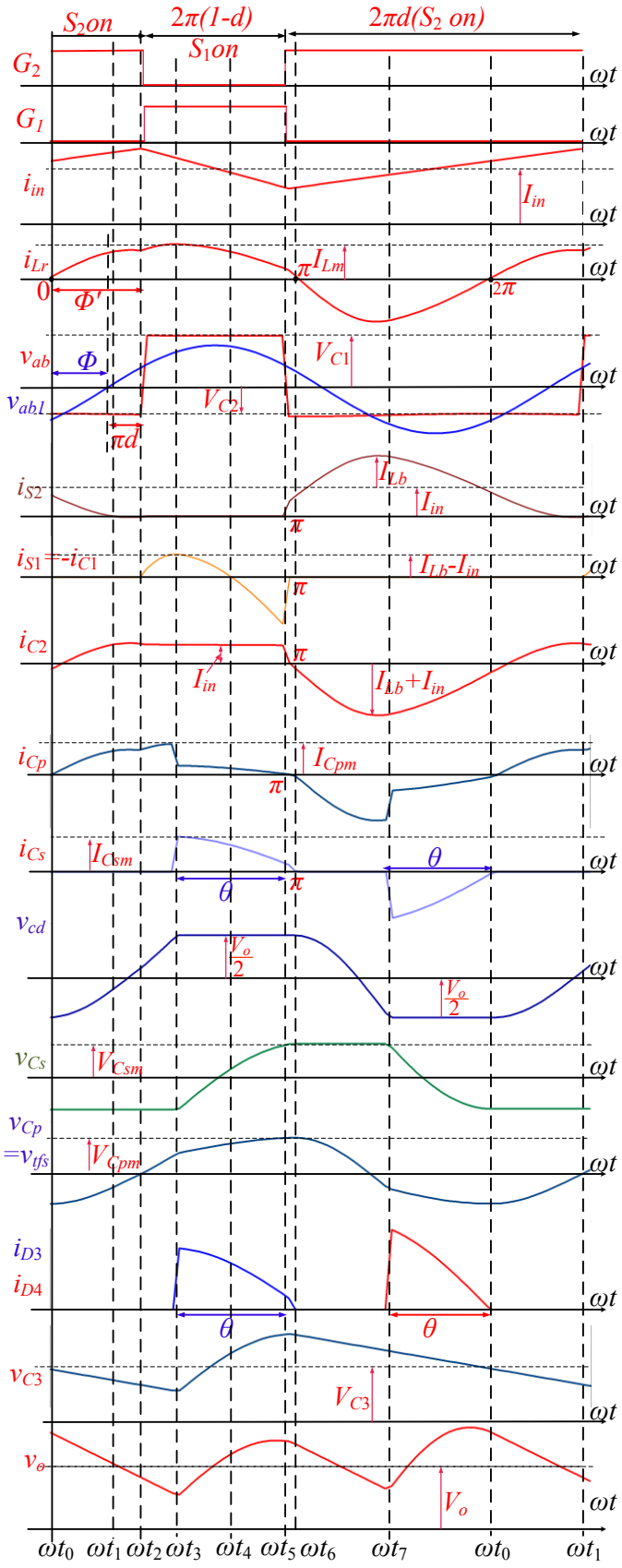


Fig. 3.2. Operating waveforms for the proposed converter under steady state.

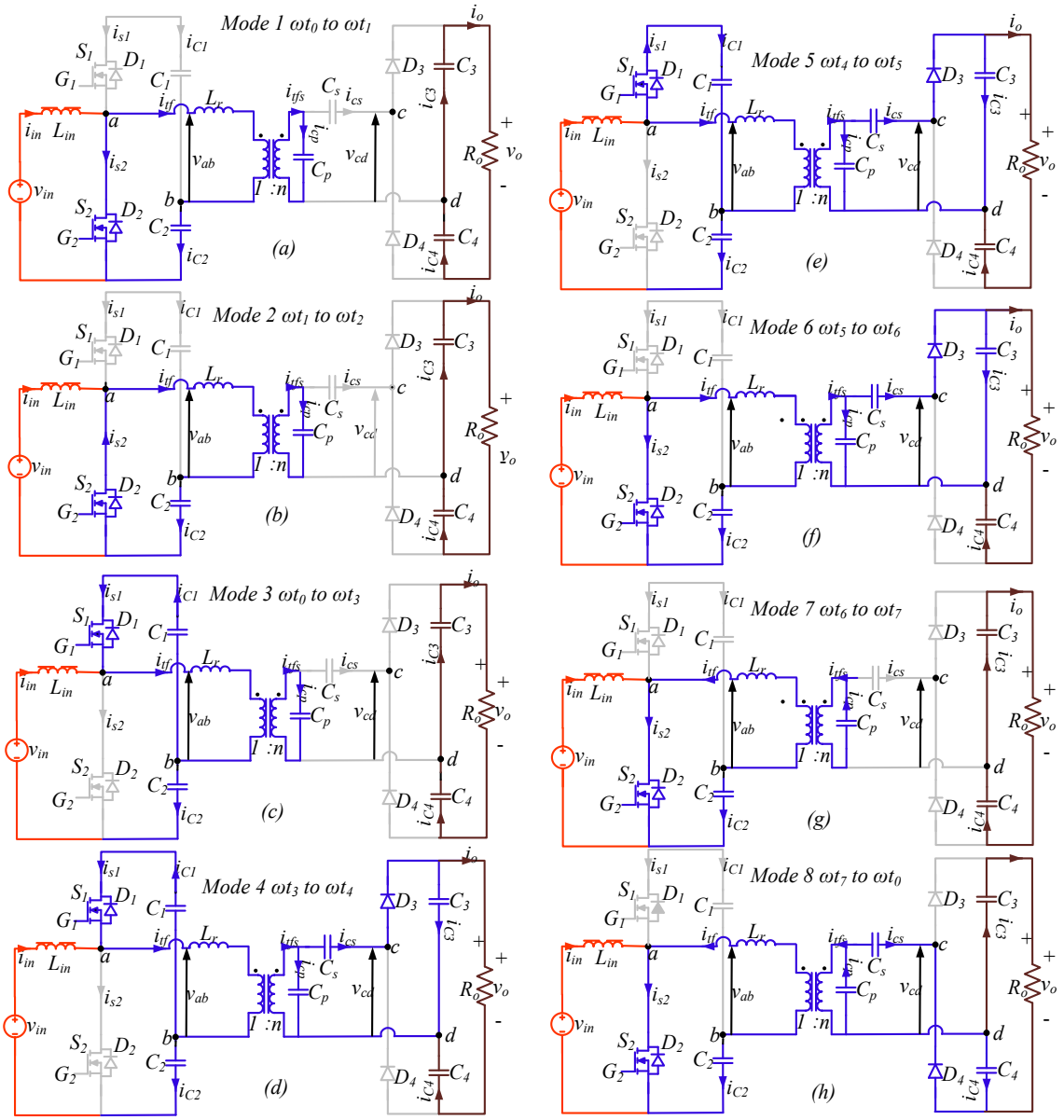


Fig. 3.3. Equivalent circuits for various operating modes of proposed converter.

3.3.5 Mode 5. (Fig. 3.3 (e). $\omega t_4<\omega t<\omega t_5$)

This mode begins when the body diode of S_1 starts conducting. This mode ends with the withdrawal of the gate to voltages pulse for S_1. At this turn-off instant, since the current in S_1 is negative, according to [129], [132], S_1 is considered to be turned off with ZCS. The status of the rest of the circuit is maintained as in the previous mode.

3.3.6 Mode 6. (Fig. 3.3 (f). $\omega t_5<\omega t<\omega t_6$)

This mode begins when S_2 is turned on. The only current carried by the body diode of S_1 in the previous mode is transferred to S_2. The status of the rest of the circuit is maintained similarly to the previous mode.

3.3.7 Mode 7: (Fig. 3.3 (g). $\omega t_6<\omega t<\omega t_7$)

This mode begins when i_{Lr} changes its polarity. D_3 ceases to conduct and current i_{tfs} alone feeds C_p. Capacitors C_3, and C_4 are feeding the load.

3.3.8 Mode 8. (Fig. 3.3 (h). $\omega t_7<\omega t<\omega t_0$)

This mode begins when D_4 starts conducting. S_2 keeps on conducting a total of i_{in} and i_{Lr}. Current i_{tfs} is shared among C_p and C_s.

3.4 Modeling of the proposed converter

The purpose of the resonant tank (LCC-T), as shown in Fig. 3.1, is to achieve soft-switching of the devices in the front-end inverter. LCC-T resonant tank adopted in the proposed converter is a variant of conventional LCC resonant tank, which offers benefits such as reduced stress on the resonant tank components. Further, LCC-T resonant tank offers a compact size when compared to the conventional LCC resonant tank. A comparison of resonant tank components and their stress is provided in Table 3.1. This table shows LCC-T resonant tank offers a 79.6% and 64.9% reduction in voltage and current stress respectively on the series resonant capacitor when compared to conventional LCC. These merits of an LCC-T resonant tank qualify for its adoption in the proposed converter.

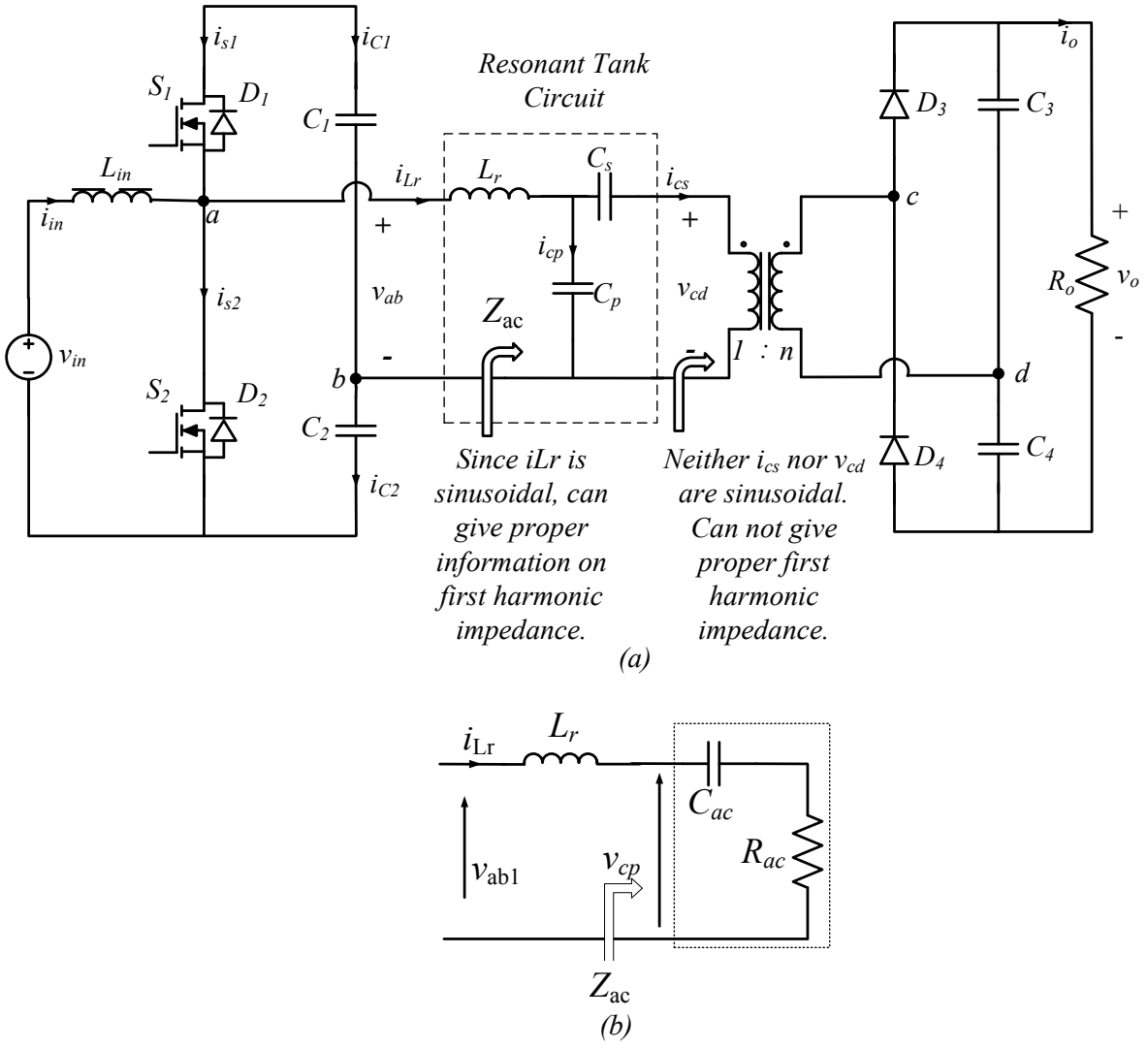


Fig. 3.4. (a) Capacitors transferred to primary side (b) Equivalent circuit using modeling method proposed in chapter 2.

$$z_{ac} = \frac{v_{cp1}}{I_{Lm}} \tag{3.1}$$

$$i_{Lr} = I_{Lm} \sin(\omega t) \tag{3.2}$$

$$i_{Cp} = I_{Cp} \sin(\omega t) \tag{3.3}$$

$$i_{Cs} = I_{Cs} \sin(\omega t) \tag{3.4}$$

$$-\frac{1}{C_p}\int_{\frac{(\pi-\theta)}{\omega}}^{\frac{\pi}{\omega}} I_{Cp} \sin(\omega t)\, dt + \frac{1}{C_s}\int_{\frac{(\pi-\theta)}{\omega}}^{\frac{\pi}{\omega}} I_{Cs} \sin(\omega t)\, dt + \frac{V_o}{2n} = 0 \tag{3.5}$$

$$i_{Cp} = i_{Lm}\left[\frac{1}{1+\lambda} + k\right] \tag{3.6}$$

$$i_{Cs} = i_{Lm}\left[\frac{\lambda}{1+\lambda} + k\right] \tag{3.7}$$

$$k = \frac{\omega C_p V_o^2}{4\pi P_o n^2 (1+\lambda)^2} \tag{3.8}$$

$$i_{Cp} = i_{Lm}\left[\frac{1}{1+\lambda}\right] \tag{3.9}$$

$$i_{Cs} = i_{Lm}\left[\frac{\lambda}{1+\lambda}\right] \tag{3.10}$$

$$v_{Cs}(\pi) = v_{Cs}(\pi-\theta) + \frac{1}{C_s}\int_{\frac{(\pi-\theta)}{\omega}}^{\frac{\pi}{\omega}} i_{Cs}\, dt \tag{3.11}$$

$$V_{Csm} = \frac{I_{Lm}(1-\cos\theta)}{2\omega C_s(1+\lambda)} \tag{3.12}$$

$$v_{Cs}(\omega t) = v_{Cs}(\pi-\theta) + \frac{1}{C_s}\int i_{Cs}\, dt \tag{3.13}$$

$$v_{Cs}(\omega t) = -V_{Csm} + \frac{I_{Lm}}{(1+\lambda)\omega C_s}(-\cos\omega t - \cos\theta) \tag{3.14}$$

$$v_{Cp}(\omega t) = \frac{V_o}{2n} - V_{Csm} + \frac{I_{Lm}}{(1+\lambda)\omega C_s}(-\cos\omega t - \cos\theta) \tag{3.15}$$

$$v_{Cp}(0) = -V_{Csm} - \frac{V_o}{2n};\ v_{Cp}(\pi-\theta) = -V_{Csm} + \frac{V_o}{2n} \tag{3.16}$$

$$v_{Cp}(\pi-\theta) = v_{Cp}(0) + \frac{1}{C_p}\int_0^{\frac{(\pi-\theta)}{\omega}} I_{Lm}\sin(\omega t)\,dt \tag{3.17}$$

$$V_o = \frac{I_{Lm} n(1+\cos\theta)}{\omega C_p} \tag{3.18}$$

$$v_{Cp}(\omega t) = v_{Cp}(0) + \frac{1}{C_p}\int I_{Lm}\sin(\omega t)\,dt \tag{3.19}$$

$$v_{Cp}(\omega t) = -V_{Csm} - \frac{V_o}{2n} + \frac{I_{Lm}}{\omega C_p}(1-\cos\omega t) \tag{3.20}$$

$$v_{Cp1}(\omega t) = I_{Lm}\left[\frac{1}{\omega C_p(1+\lambda)}\sin^2\theta - j\left(\frac{1}{\omega C_p} + \frac{\sin\theta\cos\theta-\theta}{\pi\omega C_p(1+\lambda)}\right)\right] \tag{3.21}$$

$$z_{ac} = \frac{1}{\omega C_p(1+\lambda)}\sin^2\theta - j\left(\frac{1}{\omega C_p} + \frac{\sin\theta\cos\theta-\theta}{\pi\omega C_p(1+\lambda)}\right) \tag{3.22}$$

$$R_{ac} = \frac{1}{\omega C_p}\frac{\sin^2\theta}{(1+\lambda)} \tag{3.23}$$

$$C_{ac} = C_p\frac{\pi(1+\lambda)}{\pi(1+\lambda)+\sin\theta\cos\theta-\theta} \tag{3.24}$$

For mathematical modeling, resonant capacitors are transferred to the primary side as shown in Fig. 3.4 (a). The voltages v_{cp}, v_{cs} and v_{cd} as shown in Fig. 3.4 (a) are reflected voltages at primary and are presented in Fig. 3.2. According to the proposed modeling technique in Chapter 2, equivalent circuit impedance z_{ac} as shown in Fig. 3.4 is given by (3.1). Among the required parameters, resonant current i_{Lr} according to FHA, can be assumed as (3.2) with I_{Lr} being its peak value. The other component v_{cp1} is the peak value of the first harmonic component of $v_{cp.}$

3.4.1 v_{Cp} during $(\pi-\theta)<\omega t-\pi$

During this interval, it is evident that the resonant current is being shared among two capacitors C_p and C_s. A portion of current entering into C_p is charging it further while current passing through C_s is charging it and feeding the load simultaneously. Let i_{Cp} and i_{Cs} be the portion of currents entering C_p and C_s respectively, during this period, i_{Cp} and i_{Cs} are given as (3.3) and (3.4), respectively. With the help of Kirchoff's voltage law (KVL), (3.5) is obtained, which upon solving culminates as (3.6) and (3.7).

Here, it can be observed that the proposed converter is intended for soft-switching applications. To exploit the advantages of high efficiency and low magnetic volume, the converter is operated at switching frequencies above 100kHz. Further, the resonant capacitor C_p is of the order of nF or μF. So, without losing generality, it can be concluded that 'k' as given in (3.8) has minor significance on (3.6) and (3.7) and can be disregarded. Thus, i_{Cp} and i_{Cs} during this period are given as (3.9) and (3.10).

During this interval, from Fig. 3.2, it can be observed that C_s is being charged from $-V_{Csm}$ to $+V_{Csm}$. Based on (3.11), the relation between resonant current and V_{Csm} is obtained as (3.12). Further, the equation for the capacitor charging is given by (3.13) which is further simplified as (3.14). Since v_{cd} is clamped to reflected output voltage during this interval, v_{cp} is represented as (3.15).

3.4.2 v_{Cp} during $(\pi-\theta)<\omega t-\pi$

During this interval, the entire resonant current is directed into C_p. Since capacitor C_s has no current share in it, it maintains its initial voltage throughout this interval. The boundary values for capacitor C_p is given in (3.16). With the help of (3.17), the relation between V_o and I_{Lm} is determined as (3.18). Further using (3.19), v_{cp} during $(\pi-\theta)<\omega t<\pi$ is given by (3.20).

3.4.3 The fundamental component of v_{Cp}

The FHA analysis allows to assume sinusoidal current in the resonant tank. Since the sinusoidal wave is half-wave symmetric, v_{cp} during 0 to π, which is given by (3.25), (3.20), is suffucuent for calculating v_{cp1}. Further, the fundamental component of v_{cp} is given by (3.21). Based on (3.21), z_{ac} is determined as (3.22) and equivalent resistance and capacitance are given by (3.23) and (3.24), respectively.

3.5 Analysis and Design of Proposed Converter

3.5.1 Equivalent Circuit

The transformer in the proposed converter, as shown in Fig. 3.1, draws sinusoidal current. So first harmonic impedance Z_{o1eq} can be used in developing the equivalent circuit as shown in Fig. 3.5. Since the transformer in [87] neither draws sinusoidal current nor see sinusoidal voltage, therefore, the first harmonic RC model alone cannot represent the equivalent circuit.

In this section, the design procedure is illustrated through an example for the following specifications: The minimum and the maximum input voltage: V_{in}=30V-42V, respectively. Output voltage V_o=380V, rated output power is P_o=288W, Switching frequency 128kHz. The design objective is to select all the components in such a way that the stress on the tank components is minimum so that circulating currents are minimized, at minimum input voltage. For design, FHA is adopted and is normalized with respect to the parallel resonant frequency of the resonant tank. Base values for normalization are given in (3.25). By rearranging, L_r, C_p, and C_s are expressed in terms of base values (3.26). Per unit normalization helps to reduce the number of parameters that need to be designed. The converter design can be divided into two parts, resonant tank components' design, and non-resonant components' design.

3.5.2 Design of Resonant Tank Components

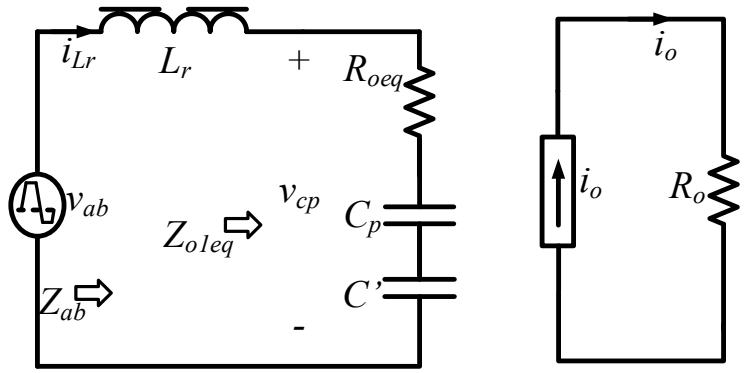


Fig. 3.5. Equivalent circuit of the proposed converter for analysis and design

Resonant tank components play an important role in maintaining the soft-switching of the converter against disturbances in load and the source end. From (3.26), it is understood that the selection of the resonant components depends on the proper selection of the base resonant frequency (ω_b) and base impedance (z_b).

3.5.2.1 Voltage Gain Relation

$$V_b=V_{in} \qquad \omega_b=\frac{1}{\sqrt{L_r C_p}} \qquad Z_b=\sqrt{\frac{L_r}{C_p}} \qquad P_b=\frac{V_b^2}{Z_b} \tag{3.25}$$

$$L_r=\frac{Z_b}{\omega_b}; \qquad C_p=\frac{1}{\omega_b.Z_b}; \quad C_s=\frac{1}{\lambda.\ \omega_b.Z_b} \tag{3.26}$$

The maximum voltage gain of the converter is given as $\hat{V}_o = \frac{380}{30} = 12.66$. Also, the per-unit voltage gain is given by (3.27). The gain represented by (3.3) can be perceived as a contribution of four stages mentioned in (3.28), where G_b is boost stage gain; G_{rt} resonant tank gain; G_{tf} transformer gain; G_{vd} Voltage doubler gain. It is observed that $\hat{V}_o=f(n,\lambda,\hat{P}_o,\hat{\omega}_o,d)$.

$$\hat{V}_o=\frac{2.\sin(\pi d)}{\pi(1-d)}\cdot\frac{1}{|Z_{ab}|}\frac{\hat{V}_o^{\,2}}{\hat{\omega}_o\hat{V}_o^{\,2}+\hat{P}_o 2\pi(1+\lambda)n^2}.n.2 \tag{3.27}$$

$$\hat{V}_o = G_b . G_{rt} . G_{tf} . G_{vd} \tag{3.28}$$

3.5.2.2 Stress on Resonant Tank Components (L_r, C_s, and C_p)

The resonant tank inductor current (i_{Lr}) is sinusoidal whose per-unit peak value is given by (3.29). Even though (3.29) gives normalized current stress, its base current, ($I_b = V_b/Z_b$) is not constant and depends on an unknown parameter Z_b. So (3.29) is transferred into absolute current stress, which is given by (3.30). Equation (3.30) is a combination of known absolute values *i.e.*, P_o, V_{in} and unknown per unit parameters $n, \lambda, \hat{P}_o$, and $\hat{\omega}_o$. In other words, $I_{Lm} = f(n, \lambda, \hat{P}_o, \hat{\omega}_o)$.

Further, (3.31) shows that per unit voltage stress across C_p depends upon C_s and (3.32) shows voltage stress across C_s, in turn, depends on $\hat{I}_{Lm}$.

$$\hat{I}_{Lm} = \frac{(\hat{\omega}_o \hat{V}_o^{\,2} + 2\pi n^2 . \hat{P}_o . (1+\lambda))}{2.n.\hat{V}_o} \tag{3.29}$$

$$I_{Lm} = \frac{P_o}{V_{in}} \left[\frac{\hat{\omega}_o \hat{V}_o}{2n\hat{P}_o} + \frac{\pi n(1+\lambda)}{\hat{V}_o} \right] \tag{3.30}$$

$$\hat{V}_{Cpm} = \hat{V}_{csm} + \frac{\hat{V}_o}{2} \tag{3.31}$$

$$\hat{V}_{csm} = \frac{\hat{I}_{Lm} \lambda (1 - \cos\theta)}{2\hat{\omega}_o (1+\lambda)} \tag{3.32}$$

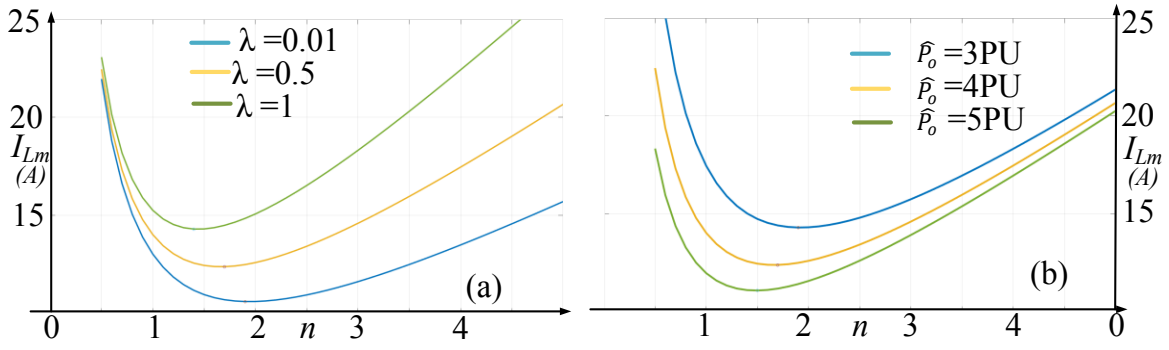


Fig. 3.6. Showing effect of (a) λ, (b) $\hat{P}_o$ on resonant current (I_{Lm})vs transformer turns ratio (n)

3.5.2.3 Soft Switching Conditions

A switch undergoes ZCS if its turn-off current is negative. So, the design should be appropriate to bring the switch current negative before a switch is turned off along with minimum stress on the resonant components at the given output voltage.

$$I_{s1(off)} = -I_{in} + i_{Lr}|_{\omega t=\omega t_5} \tag{3.33}$$

$$I_{s2(off)} = I_{in} - i_{Lr}|_{\omega t=\omega t_1} \tag{3.34}$$

Upon observing (3.27), voltage gain depends on various parameters such as $n, \lambda, \widehat{P_o}, \widehat{\omega_o}$, and d. At the same time, these parameters also influence the stress on the resonant tank components as shown in (3.30) -(3.32). Care must be taken in selecting appropriate values for these parameters so that ZCS is obtained with minimum stress on the resonant tank components. Among these parameters, $(\widehat{\omega_o}, d)$ is called the operating point. It is so because once the converter is designed, the gain of the converter and ZCS condition depend on this point. The rated output power and the per-unit maximum output power that converter can provide are P_o and $\widehat{P_o}$,

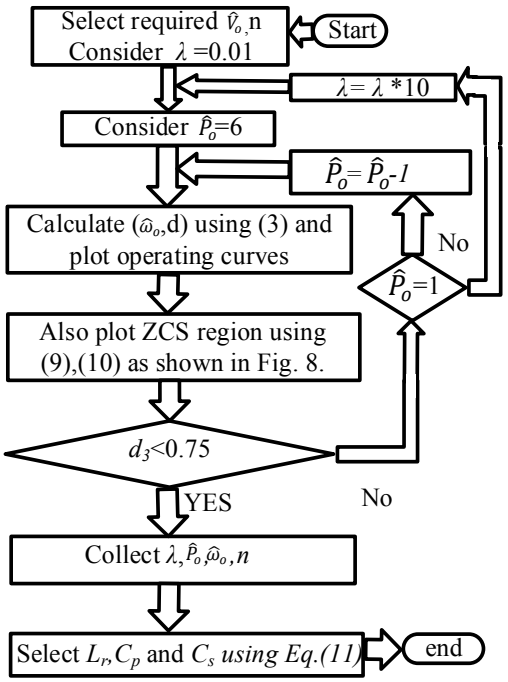


Fig. 3.7. Flow chart to design tank components with minimum stress.

respectively. It is given by $\hat{P}_o = \frac{P_o}{\hat{V}_b^2}.z_b$. Since Z_b is an unknown parameter, $\hat{P}_o$ is also unknown. Therefore, selecting a proper value of $\hat{P}_o$ can give information about Z_b which in turn decides tank components L_r, and C_p. Further, λ is the ratio of C_p to C_s. Therefore, selecting the proper value of λ can give information about C_p, and C_s.

3.5.2.4 Selecting Transformer Turns Ratio (n):

The variation of resonant tank current stress against changes in n for various $\lambda, \hat{P}_o$ are shown in Fig. 3.6 (a) and (b). From Fig 3.6 (a), and (b) it is evident that for any given $(\lambda, \hat{P}_o)$, minimum stress on resonant components can be seen around the region $1<n<2$. Therefore, selecting $n=2$ would be a wise decision since the higher turns ratio always contributes to higher gain in the circuit.

3.5.2.5 Selecting λ, $\hat{P}_o$ and operating point ($\hat{\omega}_o$, d)

Fig. 3.6 (b) concludes that current stress increases as $\hat{P}_o$ decreases. Further, Fig. 3.6 (a) concludes that current stress decreases as λ decreases. Since parameters λ, $\hat{P}_o$ and operating point $(\hat{\omega}_o, d)$ are always interdependent, a proper algorithm as shown in Fig. 3.7 is devised for optimum

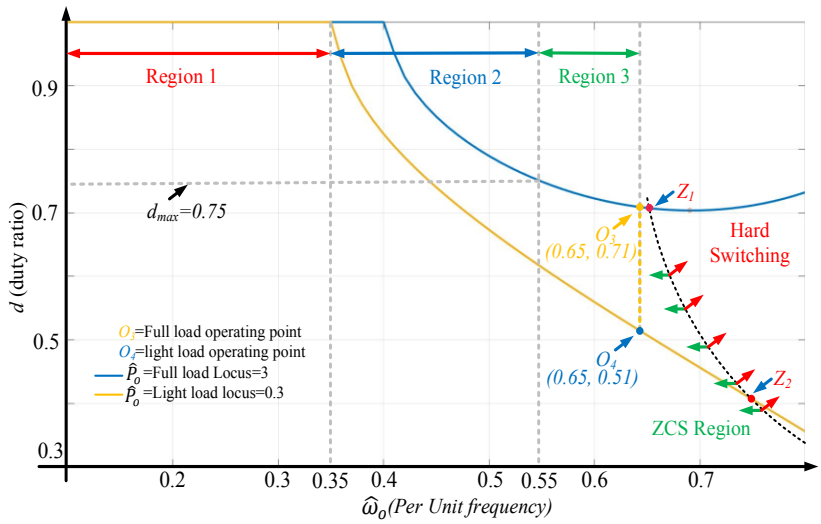


Fig. 3.8. Operating curves for the converter for optimized resonant tank stress

selection of (λ, $\hat{P}_o$) and then ($\hat{\omega}_o, d$). $\hat{V}_o$ is selected as 12.66, n=2 is determined. For minimum resonant current stress, a minimum value of λ and a maximum value of $\hat{P}_o$ are conducive. Therefore, iteration is started form λ=0.01, and $\hat{P}_o$=6.

Full load and light (10% of full) load operating point loci are plotted using (3.27). Also, the ZCS switching boundary using (3.33) and (3.34) are plotted as shown in Fig. 3.8. Below the locus of Z_1, Z_2 the region is attributed to ZCS turn-off of the switches, while ZCS switching is not retained above locus Z_1, Z_2. The normalized frequency range is split into 3 regions as shown in Fig. 3.8. It is obvious that the gain of the converter is distributed among 4 stages as given in (3.3) and (3.4). Out of the required 12.66 gain, 4 is generated by G_{tf}. and G_{vd}. The resonant tank gain (G_{rt}) and the front-end current source inverter gain (G_b) are supposed to contribute the remaining. Duty cycle d decides G_b while $\hat{\omega}_o$ decides G_{rt}. In region 1, $\hat{\omega}_o$ is far small enough to contribute significant G_{rt}, thus gain contribution expected by G_b is too high and thus d is clamped to 1. In region 2, though $\hat{\omega}_o$ is large enough to contribute significant G_{rtg}, G_b requires d between 1<d<0.75, in which inverter is not safe to operate. In Region 3, $\hat{\omega}_o$ enables G_{rt} with high voltage gain and lets the front-end inverter operate with d<0.75. In region 3, the locus of O_3, O_4 is called the operating point locus for the given wide load range. And this locus can be anywhere inside region 3. But this locus is chosen near to Z_1, Z_2 locus so that the resonant tank current is closer to sinusoidal. On properly executing the algorithm, λ=0.5 and $\hat{P}_o$=3 are selected and the obtained operating curves shown in Fig. 3.8.

3.5.2.6 Resonant tank components selection

Resonant tank components are selected using (3.35) as L_r=9.26μH, C_p=22nF, C_s=44nF. Here, O_3, O_4 are selected as operating locus for the given wide load change. Duty cycle d_3 represents the full load duty ratio at minimum input voltage required which is expected to be less than 0.75. which can be obtained by rearranging (3.26). For these components the base resonance frequency achieves is ω_b=2π*176.308Krad/s.

$$L_r=\frac{\hat{\omega}_o}{\omega_o}\left[\frac{\hat{P}_o.V_b^2}{P_{or}}\right];\quad C_p=\frac{\hat{\omega}_o}{\omega_o}\left[\frac{P_{or}}{\hat{P}_o.V_b^2 n^2}\right];\quad C_s=\frac{C_p}{\lambda} \qquad (3.35)$$

3.5.3 Non-resonant components design

3.5.3.1 Input inductor design:

Value of input boost inductors is selected as 166.66μH using $L_{in}=\frac{V_{in}.d}{f_s.\Delta I_{in}}$ for 5% of input current ripple.

3.5.3.2 C_1, C_2 capacitors design:

The function of C_1, and C_2 is to provide a constant voltage V_{c1}, V_{c2} for proper formation of v_{ab} as shown in Fig. 3.2. But C_1, C_2 are also participating in resonance with L_r and C_p as shown in

Table 3.3. List components and part numbers used for hardware prototype

	Component	Part number/remarks
1	Input inductor (L_{in})	N87, EPCOS (TDK) core, 24 turns, 166uH.
2	Transformer	N87, EPCOS(TDK) core, 12 turns primary, 24 turns secondary, leakage 1.5μH, magnetizing 2.5mH.
3	External resonant inductor	N87, EPCOS (TDK) core, 4 turns, 7.76uH.
4	Resonant capacitor C_s	44nF, 400V, film, part no: R75IN41804040J.
5	Resonant capacitor C_p	22nF, 400V, film, part no: R75PF21804030J
6	FEI capacitors (C_1, C_2)	22uF, 80V, electrolytic, Part no: EKYB800ELL-220MF11D
7	VDR capacitors (C_3, C_4)	1uF, 450V, electrolytic, Part no: 450PK1MEFC6.3X11
8	VDR diodes (D_3, D_4)	10A, 600V, Part no: RFU10TF6S
9	FEI switches (S_1, S_2)	CoolMOS, 64A, 200V, R_{DSon}=17.5nOhm, Part no IPP200N25N3GXKSA1
10	Gate driver	IR2110.

Fig. 3.3. Improper design of C_1, and C_2 leads to distortion of capacitor voltages which leads to higher ripples in v_{ab} and switch blocking voltages. To nullify their influence on the parallel resonance, C_1, and C_2 are chosen relatively larger than C_p, so that when C_1, and C_2 come in series with C_p as shown in Fig. 3.3, their series equivalent remains to be C_p.

3.6 Hardware Prototype and Experimental Results

After simulating the proposed converter in software PSIM 11.0.1 an experimental hardware prototype rated at 288W with input voltage ranging from 30 to 42V, delivering a regulated output voltage 380V at a device switching frequency of 128kHz is developed in the laboratory for testing and verification of the proposed converter's analysis and performance. A list of components selected and their respective part numbers are listed in Table 3.3

3.6.1 Component Selection

3.6.1.1 Input Inductor (L_{in})

N87, E type powder ferrite core, manufactured by EPCOS (TDK) is selected as the core. Number of turns=24, L_{in}=166.66µH. Litz wire is used for windings.

3.6.1.2 High-Frequency Transformer:

Ferrite core, primary turns=12, secondary turns=24, Litz wire for winding, magnetizing inductance=2.5mH, leakage inductance for primary=1.5µH. Resonant inductor L_r of the converter is obtained as a combination of the leakage inductor of the transformer and an externally connected inductor. The required L_r value is designed as 9.26µH. Since the transformer leakage inductance value is 1.5µH, so the remaining 7.76µH is achieved by connecting an external resonant inductor.

3.6.1.3 External Resonant Inductor:

N87, E type powder ferrite core, manufactured by EPCOS (TDK) is selected as the core. The number of turns=4, L_{re}=7.76μH. Litz wire is used for winding. Airgap is adjusted for achieving the required inductance.

3.6.1.4 Front-end Inverter Switches (S_1, S_2)

CoolMOS, Infineon made MOSFET rated 250V, 64A, RDSon=17.5mOhm whose part no is IPP200N25N3GXKSA1 is selected. Gate pulses for driving these switches are generated using DSP TMS320F28335 and further level shifted by IR2110 gate driver to suit the gate-source voltage rating of the MOSFETs.

3.7 Experimental Results

The voltage output from PV panel and fuel cell stack is variable and the converter should be able to maintain soft-switching and the rated output voltage at all load conditions against input variation. For this reason, to demonstrate the converter's ability, it is subjected to extreme wide load variations: 100% to 10% load conditions and input variations: 42V to 30V. All these extreme conditions are grouped into cases 1, 2, 3, 4 whose operating points are O_1, O_2, O_3, O_4 presented in Table 3.4. It is worth noting that the converter operates at a constant frequency in all cases which is highly desirable for simple converter control. Fig. 3.9 shows the switching waveforms for switches S_1, S_2 v_{DS} supported with their gate voltages v_{GS} for all 4 cases of operation. From all the four cases shown in Fig. 3.9, it is observed that as soon as the gate to source voltage is withdrawn, the switch is not going into blocking mode immediately. This can be noticed by zero voltage across the switch even after the withdrawal of the gate pulse. This zero voltage in absence of gate pulse

Table 3.4. Various Operating Points to validate proposed converter

	42V input	30V input
Full load	O_1= (128kHz, 0.5)	O_3= (128kHz, 0.71)
Light load	O_2= (128kHz, 0.25)	O_4= (128kHz, 0.51)

before going into blocking mode is the indication that its body diode is conducting. This also shows that switch currents are naturally reaching zero before the withdrawal of their gate pulse and thus their body diode is coming into conduction turning the switch off in ZCS mode [99]. This demonstrates the soft-switching of the converter, which is maintained against all load conditions and input voltage variations. This also verifies that the proposed operation, the mathematical analysis, and the design of the converter are accurate and effective.

For all cases, blocking voltages for switches is given in Fig. 3.9. For a given load, if the input voltage decreases, the duty ratio of the front-end inverter should be raised to maintain a constant 380V at the output. Fig. 3.9 (a), and (b) show the switching waveforms for a case 1, 3 i.e., at full load condition input voltage is dropping from 42V to 30V. As the input voltage decreasing from 42V to 30V, the output voltage is regulated by increasing d from 0.5 to 0.71 and switch blocking voltage raises from 84V to 107V. Similarly, Fig. 3.9 (c), (d) shows switching waveforms for case 2, 4 i.e., at light load condition input voltage is dropping from 42V to 30V. This is

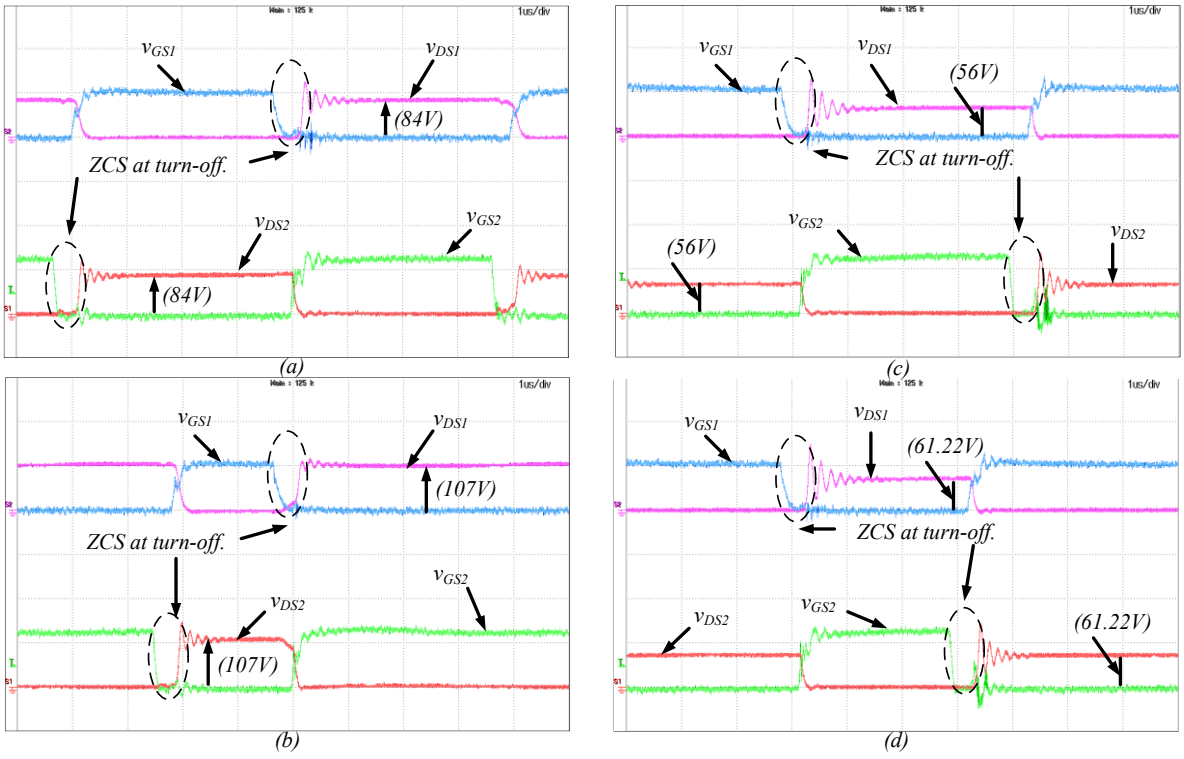


Fig. 3.9. Experimental results: Gate to Source and Drain to Source voltage of switches S_1, S_2. (a) case 1, (b) case 3, (c) Case 2, (d) case 4. Scales: v_{DS1}, v_{DS2} [100V/div], v_{GS1}, v_{GS2} [10V/div].

regulated by increasing d from 0.25 to 0.51 and switch blocking voltage is increased from 56 to 61.22V. In all conditions, the soft-switching is maintained.

Fig. 3.10 corresponds to a minimum input voltage operation of the converter at full and light loads. Similar waveforms can be obtained at 42V input voltage also. It is worth noting that from Fig. 3.9, switch blocking voltages are clamped and it is due to the proper design of the front-end inverter capacitors. This proper design of C_1, C_2 capacitors decouples C_1, C_2 from resonance, and maintains constant V_{c1}, V_{c2}. Fig. 3.10 (a1), and (b1) show constant voltage across V_{c1} and V_{c2} at full and light loads. Fig. 3.10 (a1) and (b1) show the transformer current is maintained sinusoidal against wide load variations. This feature helps in minimizing the harmonic losses in the transformer. Also, i_{Lr} leading v_{ab} shows the fact that switches availing ZCS mode of operation

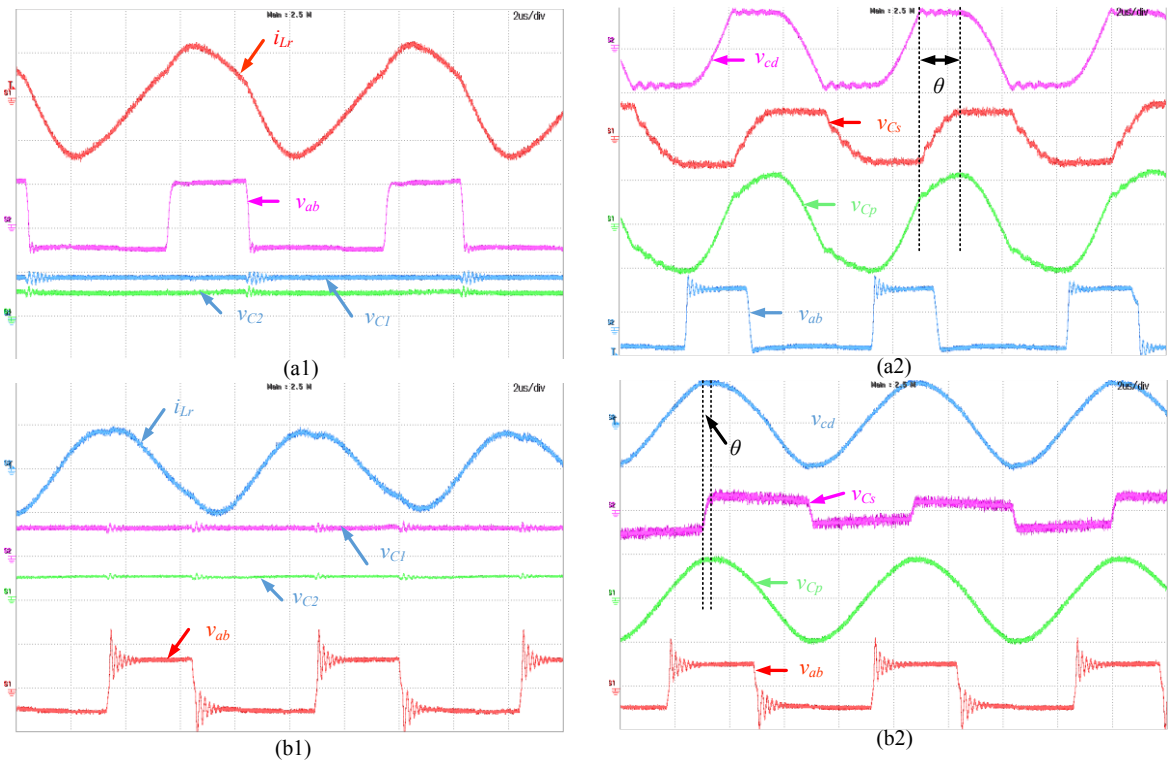


Fig. 3.10. Experimental results: Resonant tank current $i_{Lr,}$[10A/div], Front end inverter output voltage v_{ab}[50V/div], Front-end inverter capacitors $v_{C1,}$ v_{C2}[50V/div], Voltage doublar input voltage, $v_{cd,}$ [200V/div], Series resonant capacitor voltage v_{CS} [(a) 100V/div, (b) 10V/div], Parallel resonant capacitor voltage v_{Cp} [200V/div], Front end inverter output voltage v_{ab} [50V/div] for (a) Case 3 (b) Case 4

waveforms v_{cp}, v_{cs}, and v_{cd} in Fig. 3.10 (a2), and (b2) are similar to and coinciding with the theoretically predicted waveforms as shown in Fig. 3.2. It is worth mentioning that the time interval for which v_{cd} clamped to 190V is dependent on the voltage doubler conduction angle, which in turn depends on the load. Since θ decreases as load decreases, v_{cd}, and v_{cp} turn closer to sinusoidal while v_{cs} turns into a square wave. This can be seen in Fig 3.10. (a2), and (b2).

Fig. 3.11 (a1), and (b1) show output voltage is shared among two capacitors C_3, C_4 equally. Fig. 3.11 (a1), and (b1) shows that input current ripple is minimum which is conducive for PV/fuel

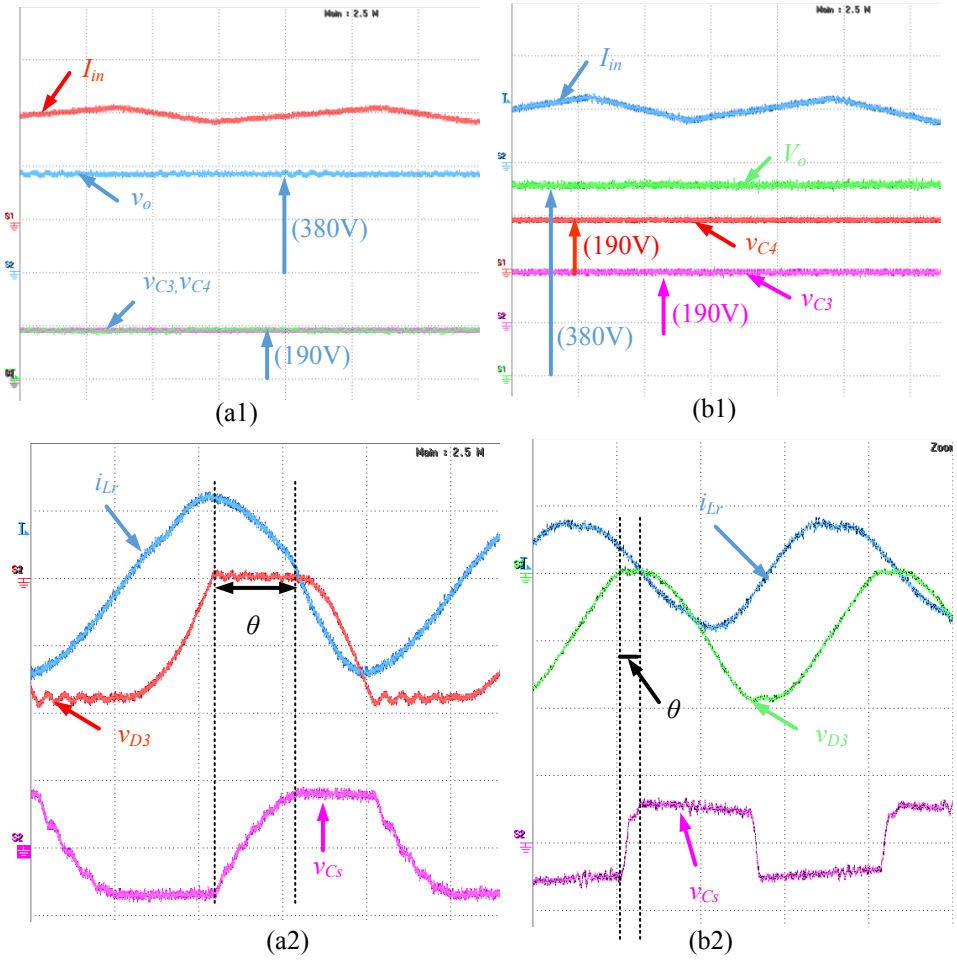


Fig. 3.11. Experimental results: Input current I_{in} [(a) 5A/div, (b) 1A/div], Output voltage V_o [(a) 200V/div, (b) 100V/div], Voltage doublar capacitors voltage, v_{C3}, v_{C4} [200V/div], transformer secondary current i_{fs} [5A/div], Voltage doublar diode anode to cathode voltage v_{D3} [200V/div], series resonant capacitor voltage, v_{Cs} [(a) 50V/div, (b) 10V/div] for (a) Case 3, (b) Case 4.

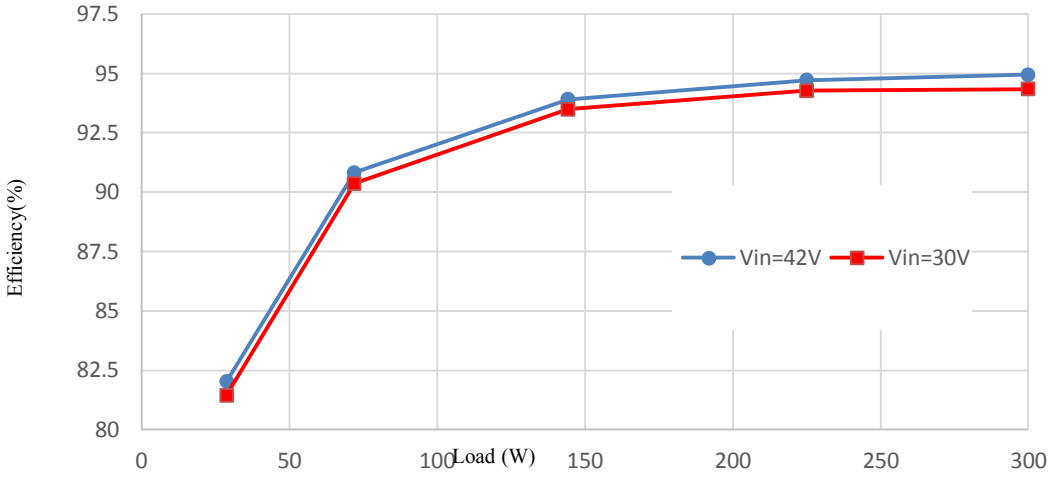


Fig. 3.12. Efficiency of proposed converter against load variation

cell application. Though load is dropped from 100% to 10%, the output voltage is maintained at 380V by adjusting the duty ratio d at a constant operating frequency. Fig. 3.11 (a2) and (b2) show the voltage doubler diode D_3 voltage in reference to the transformer secondary current i_{tfs}. For a positive half cycle, for period θ, D_3 conducts i_{tfs} and for the remaining period, it

Table 3.5. Comparison of proposed converter

	[10]	Proposed
n	7	2
I_{s1_peak}	9A	3.11A
I_{s2_peak}	15A	16.6A
V_{s1_peak}	80V	62.4V
V_{s2_peak}	75V	62.4V
I_{Lr}	15A	9.3A
L_r	2µH	14.8µH
L_m	Very high	2.5mH
C_1	47µF	22µF
C_2	1µF	22µF
C_p	-	27.97nF
C_s	-	2.79µF

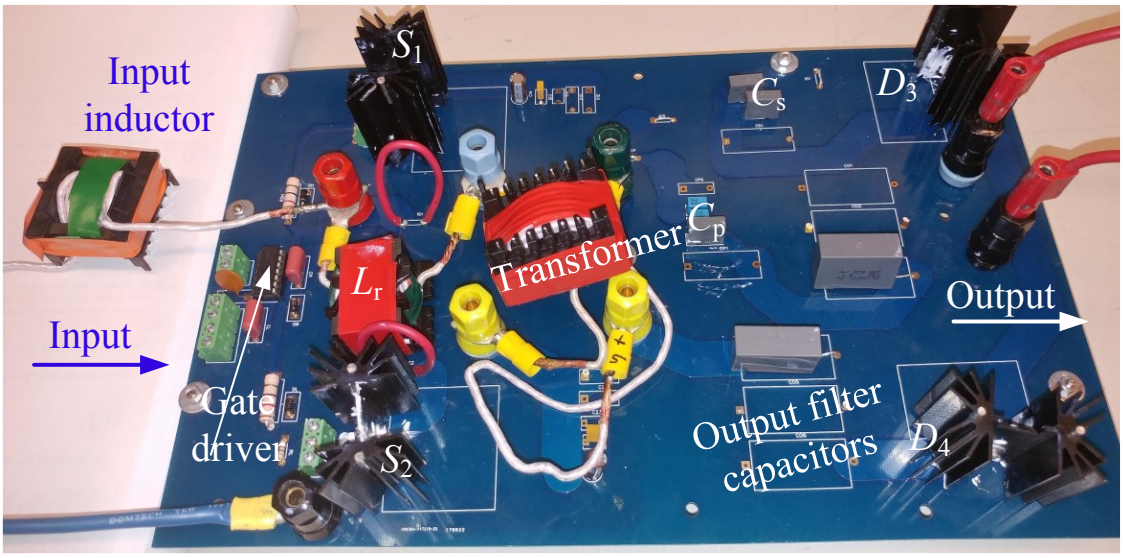


Fig. 3.13. Prototype of proposed current-fed soft-switching LCC-T resonant DC/DC converter.

is in off state. It should be observed that the conduction period of D_3 ends when i_{tfs} is passing through zero, which indicates D_3 turns-off with ZCS. Similarly, D_4 also operates with ZCS. Since C_s is connected in series with the voltage doubler, for a positive half cycle of i_{tfs}, when D_3 conducts, C_s charges to positive peak i.e., 40V in case of full load and 8V in case of light load. While in the negative half cycle when D_4 conducts, C_s discharges to negative peak, i.e., -40V in case of full load and -8V in case of light load.

Fig. 3.12 shows the proposed converter's efficiency at various operating points for minimum and maximum input voltages. The maximum global efficiency of the proposed converter is observed by nearly 95.3% at maximum input voltage and full load condition. It is observed that at full load condition, the efficiency of the converter is high. This is because of the fact that at full-load conditions, turn on current through the switches are minimum (Zero for switch S_1), causing minimum switching losses. As indicated in [139], the switching losses are analyzed for various loading conditions and calculated as 6.3W and 1.56W at full and light load conditions, respectively. The total losses of converter are 15.53W and 2.47W, respectively for minimum input voltage and full load condition. A picture of mounted setup to test the proposed analysis and recorded results is shown in Fig. 3.13.

A comparison of the proposed converter with the literature is also considered. For this purpose, the proposed converter is redesigned for the same specifications as in [139]. The converter components are listed in Table 3.5. Also, from Table 3.5, it can be concluded that in the proposed LCC-T resonant tank in the proposed converter, the transformer size is reduced from 7 in [139] to 2. Also, a decrement of 5.7A in peak circulating currents, and a reduction in harmonic content through the transformer at all load conditions verify better transformer utilization. Also, a decrement of 6A in top switch peak current, and increment of 1.6A in bottom switch peak current, a decrement of 17.6V and 12.6V in peak switch voltage is observed in top and bottom switches, respectively. Split capacitors C_1, and C_2 in the DC link are selected as 300 times larger than C_p in the proposed converter. Due to this, though C_1, C_2 appears to be bulky, actually, from Table 3.5 it can be seen that C_1+C_2=48μF for [139], while in the proposed converter it is 44μF only. All these advantages in the proposed converter are obtained with a compromise of relatively large resonating inductance (2μH in [139], 14.8μH in proposed), and extra resonating capacitance for the LCC-T tank circuit. (C_p=27.9nF, C_s=2.79μF). At the same time, it should be noted that the LCC-T resonant tank is contributing to overall converter gain.

3.8 Conclusion

Maintaining the soft-switching in a resonant converter against wide range load and input disturbances without changing the device switching frequency is a major challenge. This is due to the vulnerability of the resonant tank gain against the load changes. Therefore, a resonant tank with load-independent gain characteristics is required to achieve this objective.

Therefore, this Chapter presents a current-fed isolated LCC-T resonant converter. LCC-T resonant tank offers load-independent gain characteristic below resonance. Therefore, all the switches and diodes operate in ZCS. Further, despite the capacitive output nature of the resonant tank, this converter uses a capacitive output complemented with clean sinusoidal currents through the transformer. Also, the proposed converter is successful in maintaining sinusoidal current through the transformer against wide load and input variations, which is confirmed through experimental results. Front end inverter capacitors are decoupled from resonance with leakage

inductance of the transformer. Therefore, inverter switches are subjected to the least spikes that imply lower switching loss. Experimental results show that the proposed converter can meet this requirement without any compromise. Also, this converter operates with simple duty ratio control at a constant switching frequency. Next Chapter introduces a new modulation technique to operate the converter in ZVS mode.

Chapter 4 Analysis and Design of ZVS Current-fed Isolated LCC-T Resonant Converter.

To utilize the MOSFETs to their maximum extent, this Chapter proposes a new modulation methodology for driving current-fed LCC-T resonant converter to maintain ZVS switching during turn-on instead of a turn-off.

4.1 Introduction

The low voltage generated by the solar panels poses the switching devices to low voltage stress [120], [147]. Therefore, modern power semiconductor devices such as MOSFETs, are a suitable choice for such applications. The switching of the MOSFETs involves periodic charging and discharging of parasitic capacitances that exist across the device. These highly non-linear capacitances, especially gate to drain capacitance, determine the maximum possible switching frequency of the device, size of the device, and energy spent in switching the device. This excess energy spent is directly proportional to the switching speed and can be reduced through ZVS switching of the MOSFETs.

Load resonant converters employ a resonant tank as an intermediate stage to lead/lag current drawn by the front-end inverter [153]. A voltage-fed resonant tank offers a leading current when operated below tank resonance. On the other hand, it offers a lagging load if operated above tank resonance. Therefore, to extract maximum benefits of operating the MOSFETs in ZVS mode, the driving scheme of the dc/dc converter should be able to maintain the converter operation in lagging mode.

LCC-T tank in the current-fed resonant converter, as shown in Fig. 4.1, can regulate output voltage against load power demand and input voltage fluctuations. However, LCC-T resonant tank offers a load-independent gain characteristic under the leading region while load-dependent gain characteristics in the lagging region. Therefore, as presented in Chapter 2, the current-fed LCC-T

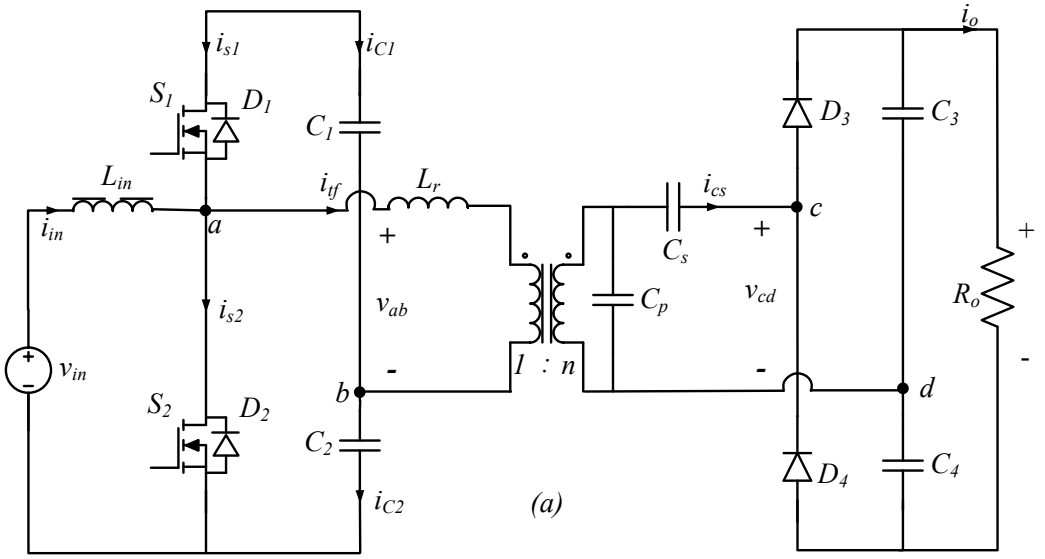


Fig. 4.1. Current-fed LCC-T resonant soft switching converter operated in ZVS mode.

resonant converter able to maintain ZCS at the constant switching frequency. However, to operate MOSFETs in the lagging region or ZVS mode, the constant switching frequency is not feasible. Therefore, this chapter proposes a new modulation methodology for the current-fed LCC-T resonant converter which maintains ZVS against the entire load and input range.

4.2 Analysis of the Proposed Converter

This section delineates the various modes in which the proposed converter is supposed to operate in one complete high-frequency switching cycle to achieve the desired objectives. The entire high switching frequency cycle is divided into 8 operating modes. The operation of the converter is presented with reference to resonant inductor current (i_{Lr}) taking the angle instant at which reference current is zero and raising positive at ω_{t0}. The following assumptions are made during the analysis of the converter. 1) During the operation resonant inductor current (i_{Lr}) is assumed as near

sinusoidal. 2) The input Inductor is large enough to maintain a constant current. 3) Output capacitors are large enough to maintain a constant output voltage. 4) The transformer is having

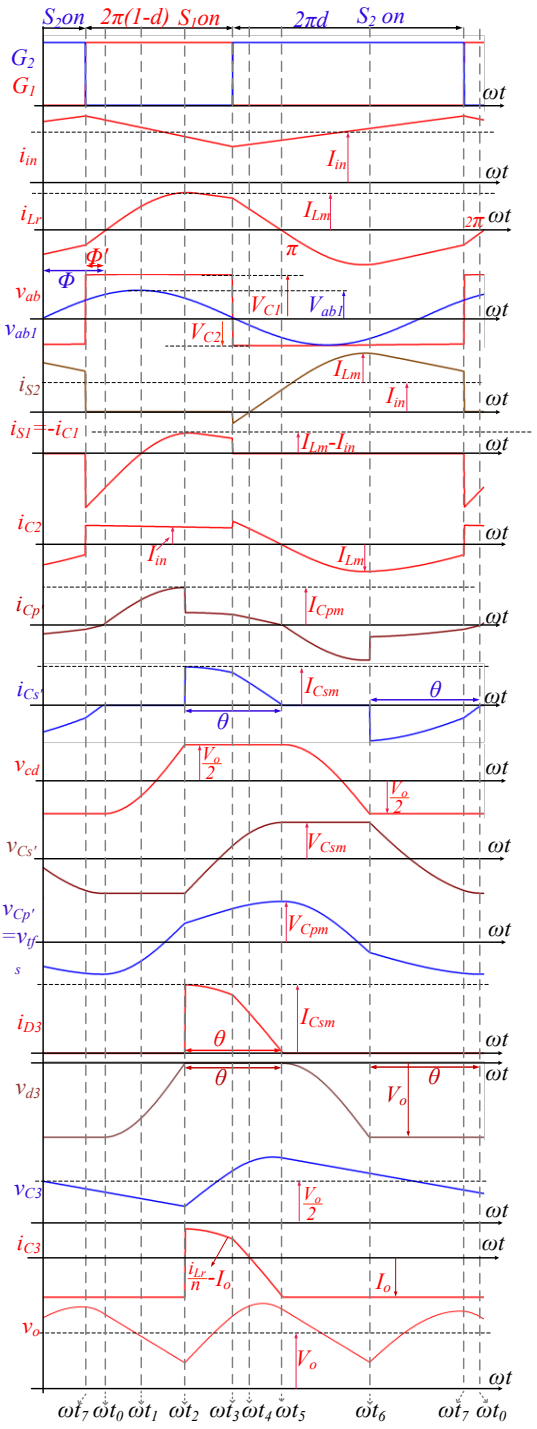


Fig. 4.2. Various operating modes of current-fed LCC-T resonant converter in ZVS mode of operation.

infinite magnetizing inductance. 5) L_r is the resonant inductance that integrates leakage inductance of the transformer into it. Voltage doubler with diodes D_3, and D_4 are connected to develop output rectifier stage. Diodes D_3 and D_4 get forward bias when v_{cd} is $V_o/2$ and $-V_o/2$ respectively, else they are in blocking mode. The operation of the converter at high frequency is explained with the help of waveforms in Fig 4.2 and equivalent circuits are shown in Fig. 4.3.

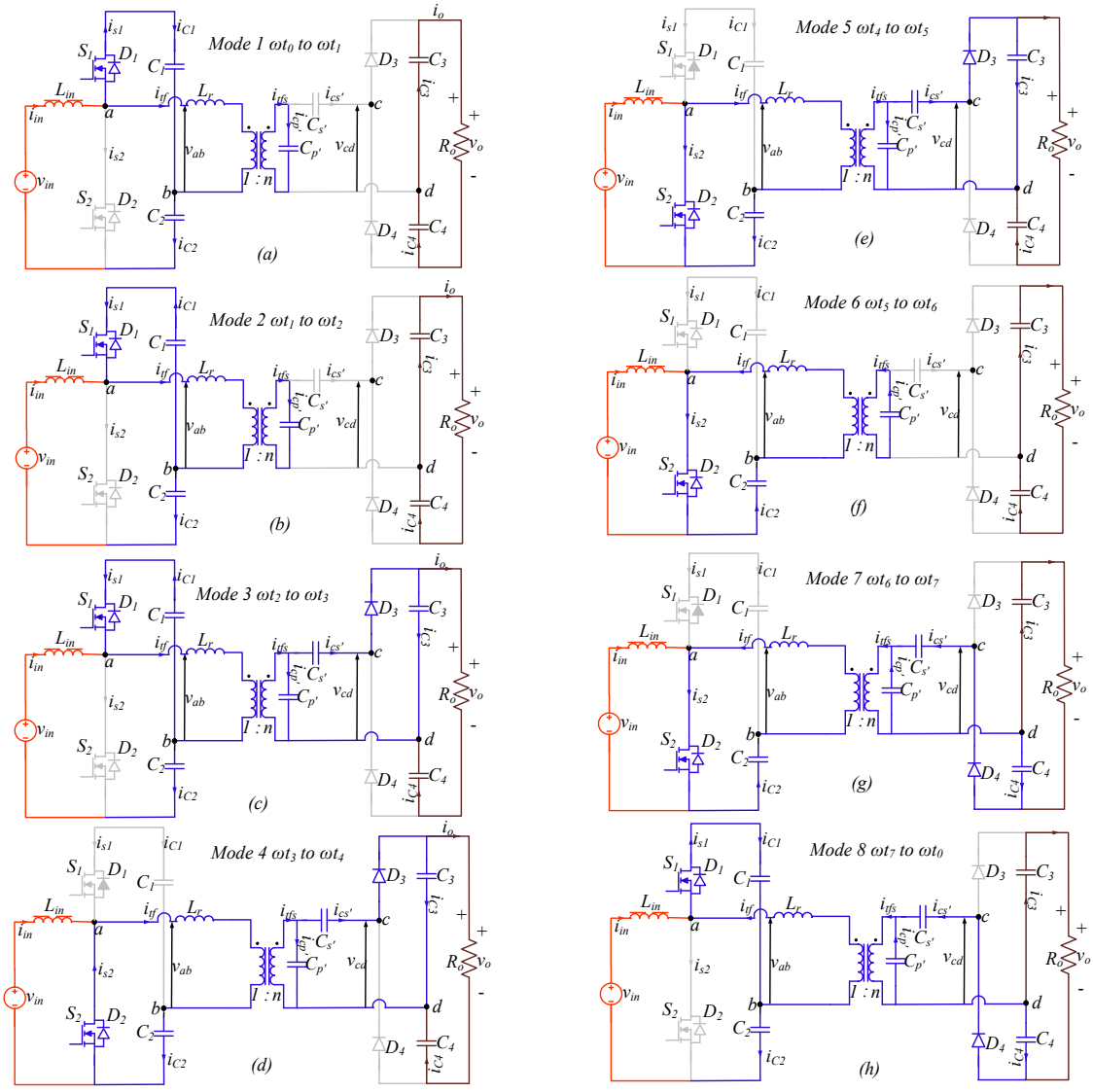


Fig. 4.3. Modes of operation of proposed current fed isolated LCC-T resonant converter.

4.2.1 Mode 1. (Fig. 4.3 (a); $\omega t_0 < \omega t < \omega t_1$)

This mode begins as soon as the resonant tank current (i_{Lr}) reaches zero and starts raising positive. During this mode, S_1 is conducting, and since current is negative showing ZVS turn-on of S_1. This current through S_1 is charging C_1. Also, it is evident from Fig. 4.2 that v_{cd} during *mode* 1 is neither clamped to $V_o/2$ nor $-V_o/2$. So diodes D_3 and D_4 are reverse biased by the output voltage, therefore, entire resonant tank current is charging the $C_{p'}$. Meanwhile, output capacitors C_3, C_4 supplying the load.

4.2.2 Mode 2. (Fig. 4.3 (b); $\omega t_1 < \omega t < \omega t_2$):

This mode begins as soon as i_{Lr} becomes equal to i_{in}. This makes the switch current S_1 zero and continues to rise in a positive direction. Secondary reflected transformer current is charging capacitor $C_{p'}$ alone, and so voltage v_{cd} is rising towards $V_o/2$. Also, D_3, D_4 are still blocking. Therefore, output capacitors feed the load.

4.2.3 Mode 3. (Fig. 4.3 (c); $\omega t_2 < \omega t < \omega t_3$)

This mode begins when the voltage v_{cd} reaches $V_o/2$, making D_3 forward bias. S_1 keeps conducting like the previous mode while i_{tfs} starts sharing between $C_{p'}$ and $C_{s'}$ according to the current division rule. Therefore, a portion of the current that is entering $C_{s'}$ *i.e.,* i_{Cs} charges

C_3 while C_4 and i_{Cs} are feeding the load. This mode ends with the withdrawal of the gate signal from S_1 to turn it off.

4.2.4 Mode 4. (Fig. 4.3 (d); $\omega t_3 < \omega t < \omega t_4$)

This mode begins with the gate signal to the switch S_2. Since the gate signal to S_1 is withdrawn in the last mode, the body diode of switch S_2, *i.e.,* D_2 conducts during the dead time. This D_2 conduction brings the voltage across switch S_2 down to zero, allowing zero-voltage turn-on for the switch S_2. Components $C_{p'}$, $C_{s'}$, D_3, D_4 maintain the same status as in the previous earlier mode.

4.2.5 Mode 5. (Fig. 4.3 (e); $\omega t_4 < \omega t < \omega t_5$)

This mode begins as soon as the current through S_2 is positive. All other elements maintain the same status as above, but the resonant tank current i_{Lr} is falling towards and reaches zero that ends this mode. At this instant, the current through D_3 is also zero, thus turning it off with ZCS mode.

4.2.6 Mode 6. (Fig. 4.3 (f); $\omega t_5 < \omega t < \omega t_6$)

Resonant tank current i_{Lr} reaches zero and then falling below zero starts this mode. Since v_{cd} is neither equal to $V_o/2$ nor $-V_o/2$, D_3, D_4 remains off. Therefore, it starts charging $C_{p'}$, and $C_{s'}$ and maintains the same voltage as the previous mode. Since voltage $v_{cp'}$ is decreasing v_{cd} voltage also starts decreasing and reaches $-V_o/2$.

4.2.7 Mode 7. (Fig. 4.3 (g); $\omega t_6 < \omega t < \omega t_7$)

As v_{cd} reached $-V_o/2$, D_4 is forward biased, and the load is connected to the tank. Switch S_2 continues conducting like the previous mode while i_{tfs} starts sharing between $C_{p'}$ and $C_{s'}$ according to the current division rule. Therefore, a portion of the current that is entering $C_{s'}$ *i.e.,* i_{Cs} will be charging C_4 while C_3 and i_{Cs} are feeding the load. This mode ends with withdrawing the gate signal from S_2 to turn it off.

4.2.8 Mode 8. (Fig. 4.3 (h); $\omega t_7 < \omega t < \omega t_0$)

This mode begins by firing the gate signal to the switch S_1. Since the gate signal to S_2 is withdrawn in the last mode, the body diode of switch S_1, i.e., D_1 starts conducting. This D_1 conduction brings the voltage across switch S_1 down to zero, preparing the switch S_1 for zero voltage turn-on. Elements $C_{p'}$, $C_{s'}$, D_3, D_4 maintain the same status as in previous mode. The resonant tank current reaches zero, which marks the end of this mode. At this instant, current through D_4 is also zero, thus turning it off with ZCS mode.

$$v_{ab}=\begin{cases} V_{C_1}=\dfrac{d.V_{in}}{(1-d)}; S_1 on \ \& \\ V_{C_2}=-V_{in}; \qquad S_2 on \end{cases} \tag{4.1}$$

$$v_{ab_1}=V_{ab_1}\sin(\omega t+\Phi) \tag{4.2}$$

$$V_{ab_1}=\frac{2.V_{in}.\sin(\pi d)}{\pi(1-d)}; \quad \Phi=-\frac{\pi}{2}+\pi d+\Phi' \tag{4.3}$$

$$I_o=\frac{I_{Lm}(1-\cos\vartheta)}{2\pi n.(1+\lambda)} \tag{4.4}$$

$$v_{cp}(\pi-\vartheta)=v_{cp}(0)+\frac{1}{C_p}\int_0^{\frac{\pi-\vartheta}{\omega}} I_{Lm}\sin(\omega t)\,dt \tag{4.5}$$

$$I_{Lm}=\frac{V_o\omega C_p}{n.(1+\cos\vartheta)} \tag{4.6}$$

$$\theta=2\tan^{-1}\sqrt{\frac{2\pi.(1+\lambda).n^2}{\omega_o R_o C_p}} \tag{4.7}$$

4.3 Analysis of the converter

For the analysis, the proposed topology, shown in Fig. 4.1 is simplified to Fig. 4.4 (a). This is achieved by reflecting the series and the parallel resonant capacitors to the primary side and are represented as $C_p=C_{p'}*n^2$; $C_s=C_{s'}*n^2$ and forms an LCC-T resonant tank that should be able to attenuate all other harmonics in v_{ab}. For this reason, (i_{Lr}) is sinusoidal. Since the transformer is connected in series with L_r, it helps in maintaining sinusoidal currents through the transformer. Fig. 4.4 (a) defines two impedance parameters Z_{o1eq} and $Z_{in,}$ represent impedance seen by terminals '*e,b*' and *'a,b',* respectively.

Fig. 4.4 (a) shows v_{ab} as input to the resonant tank or output of front-end inverter, is given as (4.3) [54]. The first harmonic voltage component in v_{ab} is given by (4.2), where (4.3) and Φ, and Φ' are defined in Fig. 4.2.

Fig. 4.4 (a) shows v_{cd} on the secondary side and is reflected as $\frac{v_{cd}}{n}$ to the primary side. Since i_{Lr} is sinusoidal, it gives us the advantage of applying the Fourier analysis tool in developing the first harmonic equivalent circuit, which is the first part in Fig. 4.4 (b). The Secondary part of Fig. 4.4 (b) is a controlled current source, which is given by (4.4). This current contributes to the output voltage.

Fig. 4.2 shows the current through the output capacitor (C_3). Using the charge balance condition at the steady-state on the filter capacitor, the output current is given by (4.4). Where θ is the voltage doubler diode conduction angle. Capacitance ratio λ is the ratio of parallel to series resonant capacitors. During period $\theta<\omega t<(\pi-\theta)$, capacitor C_p is being charged from the negative peak to the positive peak. On using condition (4.5) the peak value of circulating current is obtained as (4.6). With the help of (4.4), (4.6) θ is given by (4.7).

Upon analyzing the circuit using Fourier transformation, (4.8) to (4.14) are [26]. From the voltage expressions v_{cd}, v_{cs}, and v_{ca} impedances Z_{o1eq} is stated by (4.15). This impedance is segregated as equivalent resistance and capacitance given by (4.16), and (4.17). With the help of (4.15), Z_{in} is defined as (4.18). The voltage division rule gives (4.19). Using (4.4), (4.14) one can reach (4.20). In this design, Z_{o1eq} represents the first harmonic RC model.

A similar first harmonic RC impedance model is implemented in [3], [87], [154], which is used to represent the diode bridge rectifier (DBR). Since DBR neither draws sinusoidal current nor sees a sinusoidal voltage, absorbed by DBR is not only the first harmonic but also the various other

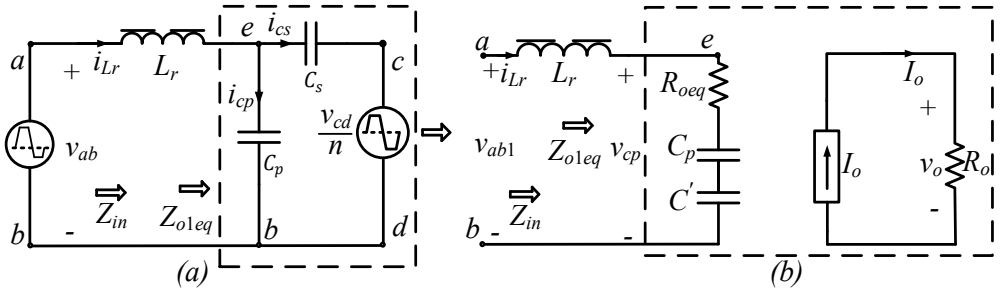


Fig. 4.4. (a) simplified circuit for the proposed topology. (b) Equivalent circuit for the proposed topology

$$v_{cd_{a1}} = -n\frac{I_{Lm}}{\pi\omega C_p}[\pi + \sin\theta\cos\theta - \theta] \tag{4.8}$$

$$v_{cd_{b1}} = n\frac{I_{Lm}}{\pi\omega C_p}[\sin^2\theta] \tag{4.9}$$

$$v_{cs_{a1}} = \frac{I_{Lm}}{(1+\lambda)\pi\omega C_s}[\sin\theta\cos\theta - \theta] \tag{4.10}$$

$$v_{cs_{b1}} = -\frac{I_{Lm}}{(1+\lambda)\pi\omega C_s}[\sin^2\theta] \tag{4.11}$$

$$v_{cp_{a1}} = -I_{Lm}\left[\frac{1}{\omega C_p} + \frac{\sin\theta\cos\theta - \theta}{\pi\omega C_p(1+\lambda)}\right] \tag{4.12}$$

$$v_{cp_{b1}} = I_{Lm}\left[\frac{\sin^2\theta}{\pi\omega C_p(1+\lambda)}\right] \tag{4.13}$$

$$v_{cp1} = v_{cp_{a1}}\cos(\omega t) + v_{cp_{b1}}\sin(\omega t) \tag{4.14}$$

$$z_{o1eq} = \frac{v_{Cp1}}{i_{Lm}} = R_{oeq} - j[X_{Cp} + X_{C'}] \tag{4.15}$$

$$R_{oeq} = \frac{\sin^2\theta}{(\lambda+1).\pi.\omega_o.C_p} \tag{4.16}$$

$$C' = C_p\frac{\pi(1+\lambda)}{\sin\theta\cos\theta - \theta}; \tag{4.17}$$

$$Z_{in} = R_{oeq} + j[X_{Lr} - X_{Cp} - X_{C'}] \tag{4.18}$$

components. Therefore, the calculation of the RC model in [15,16] is too complex and time-consuming. In [155], [156] extended describing function method for devising the equivalent circuit of the converter. The above equations are instrumental in developing the voltage gain for the proposed converter. The voltage gain of the proposed converter can be estimated as a product of 3 stages as given by (4.19) to (4.21). These 3 stages are individually derived to calculate voltage gain (4.22). Finally, voltage gain for the proposed converter is given as (4.23) that segregates the gain of the converter as contributions of 4 various stages of the proposed converter, which is front end inverter (G_f), resonant tank (G_r), transformer (G_t), voltage doubler (G_v). Of them G_r is

$$\frac{V_{Cp_1}}{V_{ab_1}} = \frac{|Z_{o1eq}|}{|Z_{in}|} \tag{4.19}$$

$$\frac{V_o}{V_{Cp_1}} = \frac{n(1+\cos\theta)}{\omega C_p |Z_{o1eq}|} \tag{4.20}$$

$$\frac{V_o}{V_{in}} = \frac{V_{ab_1}}{V_{in}} \frac{V_{cp_1}}{V_{ab_1}} \frac{V_o}{V_{cp_1}} \tag{4.21}$$

$$\frac{V_o}{V_{in}} = \frac{2.\sin(\pi d)}{\pi(1-d)} . \frac{R_o}{|Z_{in}|\left(\omega R_o C_p + 2\pi(1+\lambda)n^2\right)} . n.2 \tag{4.22}$$

$$\frac{V_o}{V_{in}} = G_f . G_r . G_t . G_v \tag{4.23}$$

$$I_{s1(on)} = -I_{in} + i_{Lr}|_{\omega t=\omega t_7} < 0 \tag{4.24}$$

$$I_{s2(on)} = I_{in} - i_{Lr}|_{\omega t=\omega t_3} < 0 \tag{4.25}$$

sensible to the output power delivered, unlike classical PWM converter. Due to this reason, the overall gain of the converter is affected as load power changes.

Thus, to regulate the output voltage against load power changes, either the switching frequency or duty cycle of the converter is regulated. Further, to operate the switches in ZVS mode, (4.24) and (4.25) should be met without any compromise.

4.4 Design of the converter

In this section, the design is illustrated by a design example for the following specifications: minimum input voltage: 30V, Output voltage 380V, Power rating (P_{or}) 288W. The objective is to have minimum circulating currents (I_{Lm}) and all ZVS operation on all of the devices the rated output voltage.

Absolute circulating current stress and voltage gain as given in (4.6), and (4.22), respectively, are dependent on 7 parameters, i.e., Output power (P_o), resonant inductor (L_r), resonant capacitor (C_p), series capacitor (C_s), transformer turns ratio (n), the duty ratio of front-end-inverter (d), and

operating frequency (ω_o) of the converter. To ease the design of these components, (4.6), and (4.22), are normalized with respect to the parallel resonant frequency of the converter (ω_b), and an input voltage (V_{in}) as base values (4.26). With the help of normalization, the design variables are reduced to 5 unknown parameters i.e., per unit output power ($\hat{P}_o$), the ratio of resonant capacitors ($\lambda=\frac{C_p}{C_s}$), transformer turns ratio (n), duty ratio (d), per unit operating frequency ($\hat{\omega}_o$) gives the base values for normalization. Equation (4.27) shows implicative base parameters for impedance, power, and current.

$$V_b=V_{in};\quad \omega_b=\frac{1}{\sqrt{L_rC_p}} \tag{4.26}$$

$$Z_b=\sqrt{\frac{L_r}{C_p}};\quad P_b=\frac{V_b^2}{Z_b};\quad I_b=\frac{V_b}{Z_b} \tag{4.27}$$

4.4.1 The voltage gain of the converter

Upon normalizing the voltage gain, (4.22) can be expressed as (4.28). Since the output voltage is 380V rated, the normalized output voltage is $\hat{V}_o=\frac{380}{30}=12.66$. So, (4.28) gives the relation between these 5 unknown parameters. *($\hat{P}_o$, λ, n, d, $\hat{\omega}_o$).*

$$\hat{V}_o=\frac{2.\sin(\pi d)}{\pi(1-d)}\cdot\frac{1}{|Z_{ab}|}\frac{\hat{V}_o^{\,2}}{\hat{\omega}_o\hat{V}_o^{\,2}+\hat{P}_o 2\pi(1+\lambda)n^2}.n.2 \tag{4.28}$$

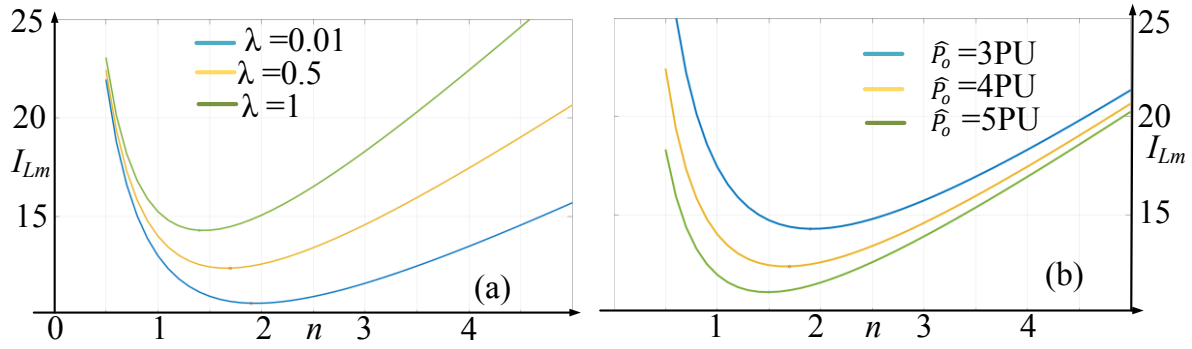


Fig. 4.5. Effect of 'n' on peak of circulating current (I_{Lm}), at (a) $\hat{\omega}_o = 0.85$, $\hat{P}_o = 3$, (b) $\hat{\omega}_o = 0.85$, $\lambda = 0.01$

4.4.2 Optimizing transformer turns ration, (n):

Equation (4.6), with the help of normalization, is expressed as (4.29). Both (4.6), and (4.29) are absolute equations. The only difference is that (4.29) is a combination of per unit and absolute values, while (4.6) is completely absolute values with more variables influencing it. Fig. 4.5 (a), and (b) show variation of I_{Lm} against 'n' with respect to λ, and $\hat{P}_o$ respectively for a given per unit operating frequency. Fig. 4.5 (a), and (b) concludes that for 1<*n*<2, minimum circulating currents occur. So '*n*=2' is selected.

$$I_{Lm} = \frac{P_o}{V_{in}}\left[\frac{\hat{\omega}_o \hat{V}_o}{2n\hat{P}_o} + \frac{\pi n(1+\lambda)}{\hat{V}_o}\right] \tag{4.29}$$

4.4.3 Optimizing $\hat{P}_o$, λ through operating curves:

Fig. 4.5 (a), and (b) conclude lower values of λ, and higher values of $\hat{P}_o$ are conducive for minimum circulating currents. Fig. 4.6 (a) shows the operating curves for various combinations of λ, $\hat{P}_o$ at n=2. These curves, upon substituting n, λ, $\hat{P}_o$, $\hat{V}_o$ in (4.28) or (4.30), resulting in a locus of points, which are plotted as operating curves shown in Fig. 4.6 (a). Further by limiting the maximum duty ratio of the front inverter to 0.75, the safe operating region is also defined in Fig. 4.6 (a). In all 3 cases, λ=0.01 but for $\hat{P}_o$=5 and $\hat{P}_o$=4 operating curves are lying in the non-safe operating region for front end inverter. But for λ=0.01, $\hat{P}_o$=3, $\hat{V}_o = 12.66$ full load operating curves enter the safe operating region of front-end inverter. This means that for full-load to light load, as shown in Fig. 4.6 (b), operating curves loci lie in the safe operating region. So out of the five-unknown variable, three are selected as n=2, λ=0.01, $\hat{P}_o$=3 for the given application.

$$f(\hat{\omega}_o, d) = \hat{\omega}_o\left[|Z_{ab}|.\hat{V}_o^{\,2}\right] + \hat{P}_o[|Z_{ab}|2\pi(1+\lambda)n^2] - \frac{4n\hat{V}_o \sin(\pi d)}{\pi(1-d)} = 0 \tag{4.30}$$

4.4.4 Optimizing Operating region

Every point on operating curves (4.30), ($\hat{\omega}_o$, d) or (ω_o, d), is called an operating point because once the converter is designed, this point alone decides the gain of the converter. For a given load, all the points on that curve are able to maintain a rated gain of 12.66 i.e., 380V output voltage for minimum input 30V.

Equations (4.24), and (4.25) are instrumental in plotting the locus of Z_1, Z_2, and Z_3 shown in Fig. 4.5 (b). The operating region above locus Z_1, Z_2, and Z_3 is attributed for ZVS turn-on for both switches the S_1, S_2, while the region below locus Z_1, Z_2, and Z_3 switches fails to retain soft switching. Obviously, a common region of both 'safe operating area' and 'soft switching area' which is shaded in Fig. 4.6 (b), becomes the operating area for the converter. Similarly, locus R_1, R_2, and R_3 show the locus of the converter resonance point. The resonance point is variable and is affected by the load. The load is open, current fed to the load falls to zero. At this condition, since full resonance current circulates through L_r and C_p, the converter resonance frequency is the same as the parallel resonance frequency of the resonant tank. The same is verified from Fig. 4.6 (b). As the load approaches to zero, the converter resonance frequency is reaching 1 PU. Since normalization is done with respect to the parallel resonance frequency of the resonant tank, this 1 PU represents the parallel resonance frequency of the tank. Thus, it is confirmed from Fig. 4.6 (b)

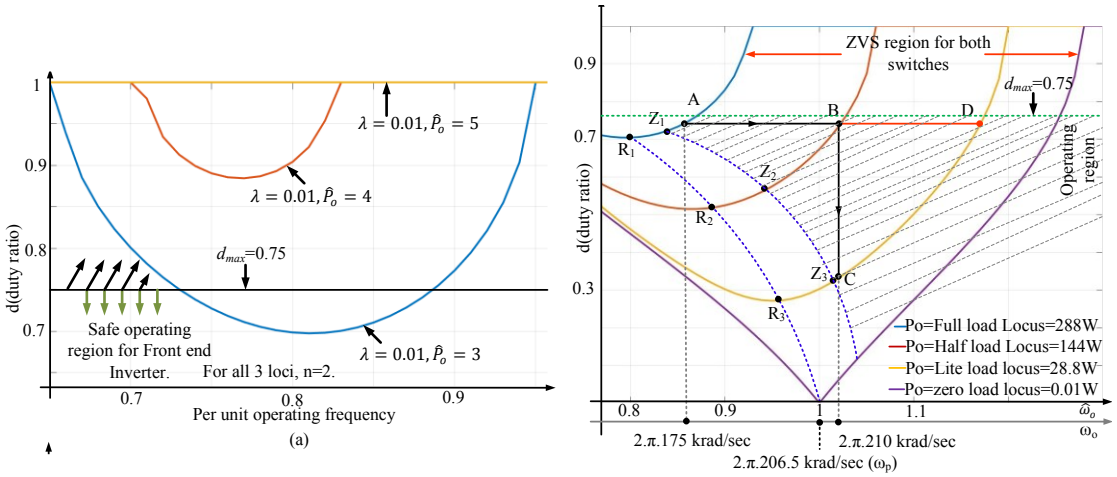


Fig. 4.6. (a) Curves showing optimization of λ, $\hat{P}_o$. (b) Operating curves for the optimim condition n=2, λ=0.01, $\hat{P}_o$=3, $\hat{V}_o = 12.66$ (for minimum input voltage=30V). AB: locus of variable frequency and constant duty cycle with d=0.73; BC: Locus of variable duty ratio and constant frequency with $\hat{\omega}_o = 1.016$

that at zero load converter resonance frequency is equal to the parallel resonance frequency of the tank.

4.4.5 Selecting operating points and resonant tank components

For full load condition, i.e., 288W, the operating point can be picked up if the point is from full load locus and lies in the shaded operating region shown in Fig. 4.6 (b). So operating point A, whose coordinates $(\hat{\omega}_o, d)$ = (0.85, 0.73) is selected. It is assumed that full load operating frequency is $\omega_o = 2\pi.175$krad/s. Since $\hat{\omega}_o = 0.85$, base frequency is given by $\omega_b = \frac{\omega_o}{\hat{\omega}_o} = 2\pi.206.5\text{krad/s}$. With this base frequency, per unit frequency is scaled to absolute values. Therefore, using (4.31), resonant tank components are selected as L_r=7.5μH, $C_{p'}$=18.56nF, $C_{s'}$=1.8μF.

$$L_r = \frac{\hat{\omega}_o}{\omega_o}\left[\frac{\hat{P}_o . V_b^2}{P_o}\right]; \quad C_{p'} = \frac{\hat{\omega}_o}{\omega_o}\left[\frac{P_o}{\hat{P}_o . V_b^2 n^2}\right]; \quad C_{s'} = \frac{C_{p'}}{\lambda} \tag{4.31}$$

From Fig. 4.5 (b), it is evident that when the converter is subjected to the load variations from full load to half load, to retain the ZVS nature of switches, the converter operates in locus AB (constant duty ratio mode). This mode of operation involves the frequency variation of the converter to regulate the output voltage while maintaining the constant duty ratio of switches. The operating frequency variation or frequency sweep demanded by the converter to regulate load from full to half is 35 kHz only. Similarly, when the converter is subjected to load variations from half to light (10% of full) load, the converter operates in locus BC. This mode of operation involves the variation of the duty ratio of the converter to regulate the output voltage at a constant frequency. Fig. 8 shows the control block diagram for the proposed isolated converter. This control block diagram accepts the required power demand and available input voltage and generates the required operating point for achieving 380V output voltage.

4.4.6 Selecting input inductor

The value of input boost inductors is selected as 100μH using $L_{in} = \frac{V_{in} . d}{f_s . \Delta I_{in}}$ for 5% of input current ripple.

4.4.7 C_1, C_2, C_3, C_4 capacitors design:

The function of C_1, and C_2 is to provide a constant voltage V_{c1}, V_{c2} for proper formation of v_{ab} as shown in Fig. 4.2. But C_1, and C_2 are also participating in resonance with L_r and C_p as shown in Fig. 4.3. Improper design of C_1, and C_2 leads to distortion of capacitor voltages, which leads to higher ripples in v_{ab} and switch blocking voltages. To nullify their influence on the parallel resonance, C_1, and C_2 is chosen relatively larger than C_p so that when C_1, and C_2 come in series with C_p as shown in Fig. 4.3, their series equivalent remains to be C_p. Thus C_1, and C_2 are selected as 22μF using (4.32).

$$C_1=C_2=300*n^2*C_{p'} \tag{32}$$

C_3, and C_4 are selected as 1μF for a 10% of output voltage ripple.

4.5 Experimental Results

The above-delineated theory is justified by simulating the topology in PSIM11.0 and then an experimental setup has been built in the laboratory, rated at 288W. The components used are listed in Table 4.1. The experimental results are satisfactory, and the performance of the converter is in harmony with the proposed theory and the anlysis. The proposed converter is tested to generate 380V form an input voltage ranging from 30V-42V, which represents the variable PV/fuel cell output voltage. Also, the load demand is uncertain. Thus, the converter is tested for the varying load conditions, load while the input voltage is varying from minimum to maximum voltage, i.e., 30-42V. Various operating points are listed in Table 4.2. Fig. 4.7 shows the gate-to-source voltage and drain to source voltage across switches $S_1$and S_2 along with their currents for all possible cases. It is observed from Fig. 4.7 that the converter to retain ZVS under any kind of disturbances both from the load side and source side.

Table 4.1. Components and respective part numbers for experimental setup.

Components	Part Number.
S_1, S_2	CoolMOS, 200V,64A, R_{DSon}=17.5mΩ, part no IPP200N25N3GXKSA1.
D_3,D_4	Manufacturer part no: RFU10TF6S, 600V, 10A rated
C_3,C_4	1μF, 450V electrolytic capacitor, part no: 450PK1MEFC6.3X11
C_1,C_2	22μF, 80V electrolytic, Part no: EKYB800ELL-220MF11D
C_p=18nF, C_s=1.8μF	400V film capacitors C_p Part no: R75PF21804030J, C_s part no: R75IN41804040J.
L_{in}	Number of turns=24, L_{in}=100μH. Litz wire is used for windings, N87, E type powder ferrite core
High-frequency transformer	Ferrite core, Primary turns=12, secondary turns=24, litz wire for winding, magnetizing inductance =2.5mH, Leakage inductance for primary=1.5μH
External Resonant Inductor	Number of turns=4, L_r=6μH. Litz wire is used for windings,

Fig. 4.7 (a)-(l) shows that for all conditions mentioned in Table 4.2, during dead time anti-parallel diode of the switch conducts thus keeping the voltage across the switch zero before it turns on. This proves the operation of S_1 and S_2 in ZVS mode, which is successfully retained in all conditions according to the requirements of the application.

Fig. 4.7 (b) and (d) show switching waveforms of the converter with input voltage 30V while delivering full load power whose operating point is given by 'A'. When the load power demand is reduced from full-load to half-load, the control circuit responds and updates the operating point with 'B'. From (4.25), it is evident that the output voltage is vulnerable to load power. This new operating point, 'B', compensates the output voltage variations and settles it to 380V, whose switching waveforms are shown in Fig. 4.7 (f), and (h). This compensation is achieved by regulating the switching frequency of the converter from 175 kHz to 210 kHz at a constant duty ratio (=0.73), which is represented by locus AB as shown in Fig. 4.6 (b).

Similarly, load variations between half-load to light load are compensated by regulating the duty ratio of the converter while maintaining constant operating frequency, given by locus BC of Fig. 4.6 (b). At input voltage of 42V, locus A' and B' and B' and C' are instrumental in compensating output voltage for load power variations.

Fig. 4.8 shows the efficiency of the proposed converter for minimum and maximum input voltages. The maximum efficiency of 95.1% is recorded for 42V input and 288W output power. Fig. 4.9

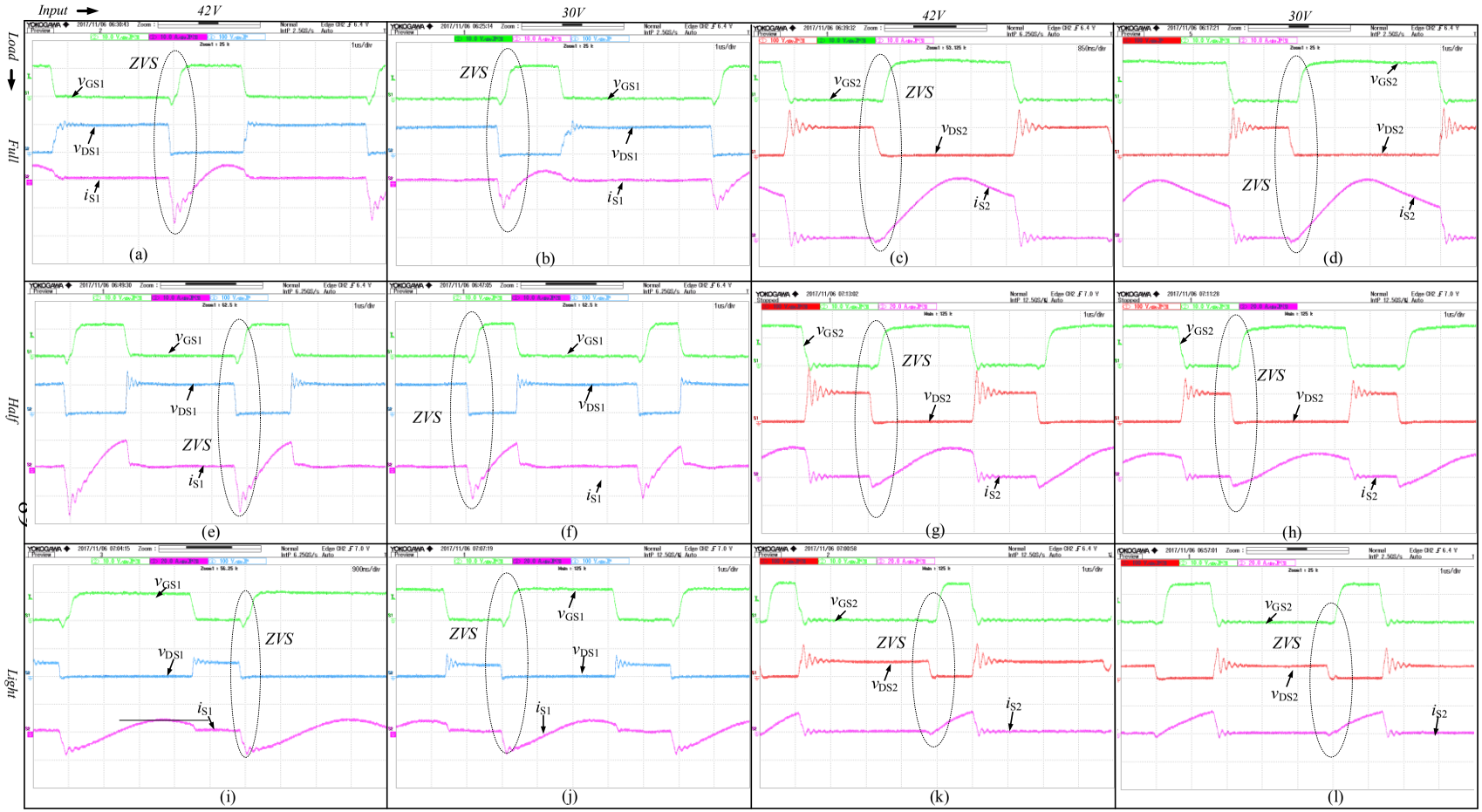


Fig. 4.7. Experimental results for converter subjected to wide load variations and input voltage variations. Output voltage in all cases is 380V. v_{GS1}, v_{GS2} gate to source voltage of switches S_1, S_2. [Scale: 10V/div], v_{DS1}, v_{DS2} gate to drain voltage of switches S_1, S_2. [Scale:100V/div], i_{S1}, i_{S2} switch currents of S_1, S_2. [Scales: (a)-(f): 10A/div, (g)-(l):20A/div].

Table 4.2. Various operating points required as per load and input voltage conditions

	Full load(288W)	Half load (144W)	Light load(28W)
Input 42V	A'=(2π.175krad/s, 0.625)	B'=(2π.210krad/s, 0.625)	C'=(2π.210krad/s, 0.2)
Input 30V	A=(2π.175krad/s, 0.73)	B=(2π.210krad/s, 0.73)	C=(2π.210krad/s, 0.31)

shows the loss analysis for the proposed converter at minimum input and maximum load conditions. It should be observed that primary switching losses are only due to turn-off. It is observed that the voltage doubler diode switching losses during turn off are zero because it turns off with ZVZCS. During turn-on, dv/dt of the switch is limited to 400V/μsec. With this low dv/dt turn-on transition, losses are negligible. A substantial amount of conduction losses is observed in the transformer, inductors, and switches.

Table 4.3, by comparing theoretical and experimental measurements, establishes the accuracy of the model derived in section II. The error in theoretical and measured values are due to small harmonic content in resonating currents of the converter and inaccuracy in measurements of transformer and inductor parameters.

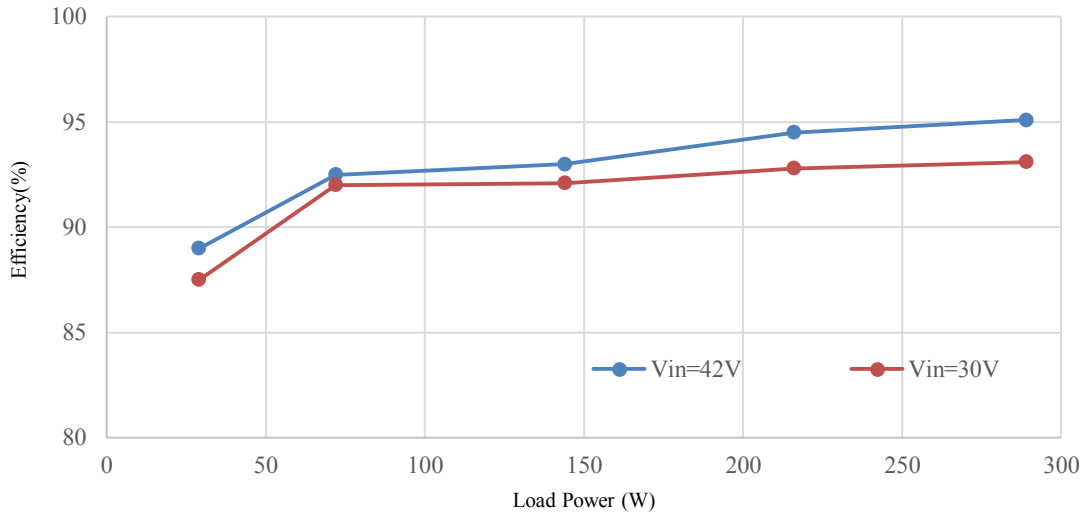


Fig. 4.8. Efficiency of proposed converter.

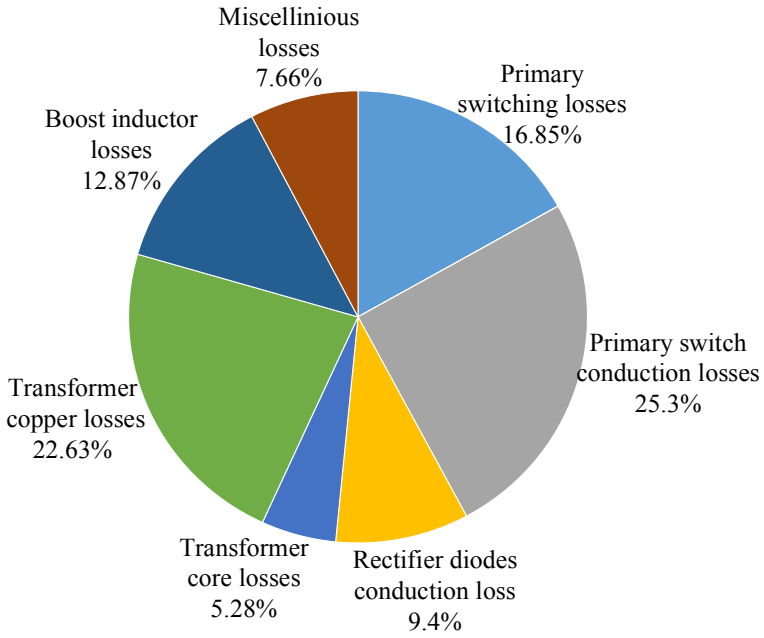


Fig. 4.9. Loss distribution in proposed converter.

Fig. 4.10 corresponds to the minimum input voltage operation of the converter at full and light load. Similar waveforms are obtained at all other operating conditions. Fig. 4.10 (a), (b) shows v_{ab}, and boost capacitors voltages v_{c1}, v_{c2}. At full load and light load v_{c2}=30V. At full load, v_{c1}=75V and at light load v_{c1}=15V. The input inductor is charging while S_2 is on and discharging while S_1 is on.

Fig. 4.10 (c)-(d) shows the operating waveforms of the resonant tank and voltage doubler stage. From Fig. 4.10 (c), (d) it is evident that the resonant tank current i_{Lr} is lagging the resonant tank

Table 4.3. Comparison of theoretical predictions against experimental measurements

	Vin=30V,FL		Vin=30V,HL		Vin=30V,LL		Vin=42V,FL		Vin=42V,HL		Vin=42V,LL	
	T	E	T	E	T	E	T	E	T	E	T	E
$\hat{I}_{Lm}$	15.4A	15A	12.1A	11.6A	9.1A	8.75A	4.7A	14.2A	11.4A	10.8A	8.7A	8.5A
d	0.78	0.73	0.78	0.73	0.36	0.31	0.68	0.625	0.68	0.625	0.24	0.2
f_{sw}	178	175	212	210	212	210	176.5	175	212	210	212	210

T: Theoretical; E: Experimental, f_{sw}: Switching frequency in kHz; FL: Full Load; HL: Half Load; LL: Light Load

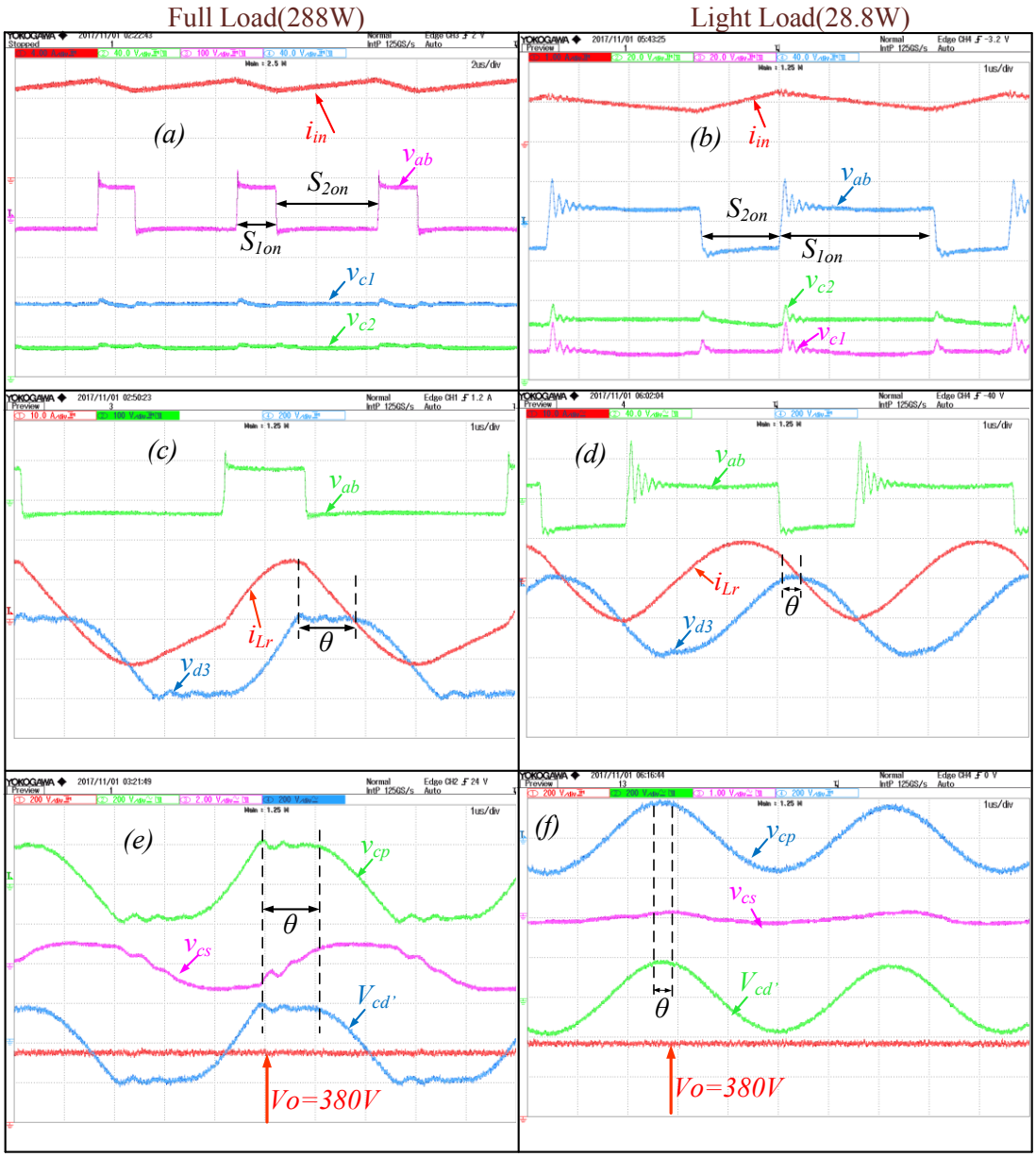


Fig. 4.10. Showing experimental results at full load and light load whose operating points are A,C respectively. Scales: (a) i_{in} 4A/div; v_{ab} 100V/div; v_{C1}, v_{C2} 40V/div. (b) i_{in} 1A/div; v_{ab} 40V/div; v_{C1}, v_{C2} 20V/div. (c) v_{ab} 100V/div; i_{Lr} 10A/div; v_{D3} 200V/div. (d) v_{ab} 40V/div; i_{Lr} 10A/div; v_{D3} 200V/div; (e) v_{Cp} 200V/div; v_{Cs} 2V/div; v_{cd} 200V/div; V_o 200V/div. (f) v_{Cp} 200V/div; v_{Cs} 1V/div; v_{cd} 200V/div; Vo 200V/div

input voltage v_{ab} inferring the fact that the resonant tank is operating in the lagging region thus able to help the input stage to operate in ZVS mode. Also, Fig 4.10 (c), and (d) host the voltage of voltage doubler diode D_3, which is conducting for duration θ, which is load-dependent and shrinks as the load falls to lower values. So, at lighter loads, v_{D3} becomes completely sinusoidal. During period θ, i_{Lr} passes through D_3, and at the end of θ duration, diode D_3 commutates with ZVZCS. Similarly, D_4 also enjoys ZVZCS. This operation of D_3 and D_4 in ZVZCS mode is independent of load and input voltage. This operation of D_3, D_4 in ZCS mode eliminates rectifier diode loss, snubber across secondary which are conducive for increasing power density.

Fig. 4.10 (e), and (f) show that the load is regulated at 380V from full load down to light-load conditions.The voltage v_{cp} is the transformer secondary voltage while i_{Lr} is the transformer primary current. From Fig. 4.10 (c)-(d) it is evident that the proposed converter can maintain continuous sinusoidal current through, the transformer against wide load variations and input voltage variations. Also, at light load transformer current and voltage are completely sinusoidal. The fact that the resonant current is sinusoidal shows that the proposed LCC-T tank can attenuate higher harmonics in the current.

Fig. 4.11 shows the prototype of the proposed converter. The only drawback of the proposed converter is its frequency modulation, which forces the converter to design components at a lower frequency (175kHz) which are 16.66% oversized to those components designed at high frequency (210kHz).

4.6 Conclusion

An isolated soft-switching current-fed LCC-T resonant DC-DC converter for PV/fuel cell application is proposed in this Chapter to extract the maximum benefits from MOSFETs by operating them in ZVS mode. The detailed operation, analysis, and design of the converter are presented. The main advantages of this proposed converter are (1) high voltage gain, (2) soft-switching (ZVS for input switches, ZVZCS for voltage doubler diodes) against wide input and load variations (3) continuous input current with minimum ripple (4) transformer with lower turn ratio, lower current stress, lower harmonic content and (4) higher power density, efficiency and

lower in size. However, to maintain converter in ZVS mode for all load and input variations, the switching frequency of the converter needs a dynamic tuning, which is a major disadvantage.

A proof-of-concept hardware prototype rated at 288W is built in the laboratory and tested to extreme load and input conditions to achieve the rated output voltage 380V. Experimental results presented demonstrate the satisfactory operation of the converter and followed the presented theory and analysis of the converter.

Next Chapter extends the single phase converter to three-phase to suit higher power levels.

Chapter 5 Analysis and Design of Current-fed Three-Phase Isolated LCC-T Resonant Converter

Non-conventional energy sources such as PV panels and fuel cells, as said in Chapter 1, offer significantly low voltage. Therefore, the power electronic converters connected to such sources are subjected to higher current stress. As shown in chapters 2, and 3 a sample 300W load was able to subject converter switches to 15A. Similarly, higher load demands such as 1kW can lead to higher rms current and conduction losses in the MOSFETs, thus significantly compromising converter efficiency. Therefore, this Chapter introduces another topology intended for higher power ratings while limiting the conduction losses.

5.1 Introduction

In residential applications, a high voltage gain DC/DC converter is mandatory to interface low voltage solar/fuel cell to high voltage DC bus [57]-[160]. Current-fed soft-switching converters operating at high switching frequency is endorsed for such applications [25]. Further, current-sharing topology is preferred, as it can offer current sharing and redundancy under failure conditions. In addition, delta-star configuration of 3-phase transformer inherently gives 73.2% extra gain than normal star-star connection. Star connection on secondary also favours voltage doubler, which halves switch voltage rating [161]-[163]. However, eliminating turn-off spike, accommodating wide input and load disturbances without compromising efficiency and power density is a major challenge. In addition, resonant converters suffer from power scalability issue as the leakage inductance is inversely proportionate to power level.

A current-fed high-power application aspirant with hard switching transitions, proposed in [164], [165], offers acceptable efficiency, which is highly vulnerable with input. Further, turn-off spike due to transformer leakage inductance limits operating frequency, efficiency and power

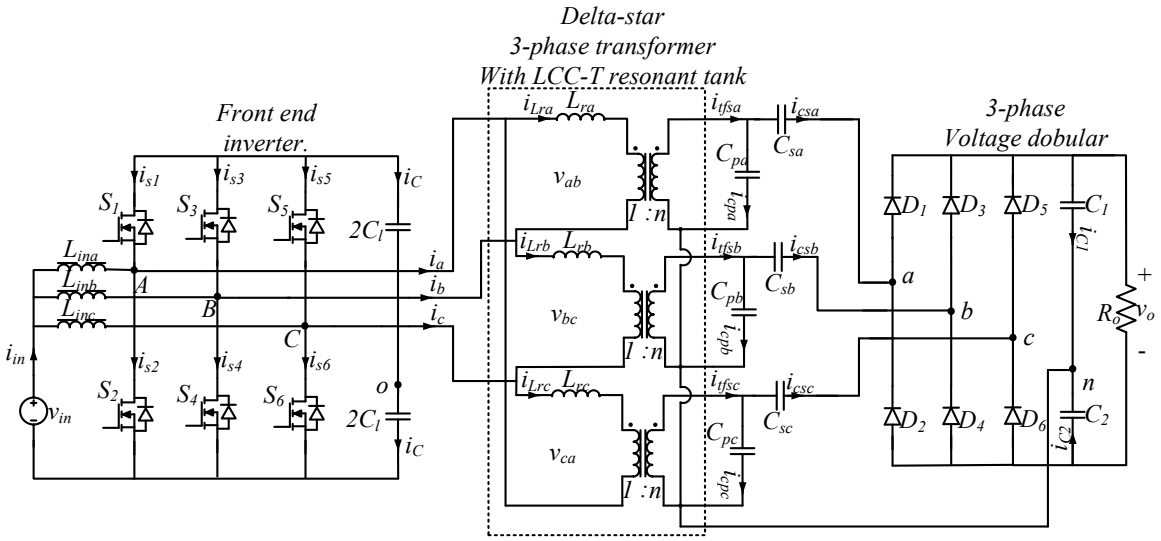


Fig. 5.1. Schematic of proposed converter "Three-phase current-fed isolated LCC-T resonant converter for low-voltage, high current applications

scaling. Cha *et.al.,* proposes active-clamp technique to clamp switch turn-off voltage spike, and tames leakage inductance for soft transitions [166]. However, higher switch count and peaky current through clamp capacitor, as reflected from transformer, makes converter unreliable. As an alternate, an active clamp converter with push-pull configuration, proposed in [167], to alleviate current though clamp capacitor. However, the concern is to achieve soft switching entirely depends on leakage inductance of the transformer. Due to this reason, under reduced load conditions, energy stored in leakage inductance fails to maintain soft switching in converter. Impulse commutated converters which uses leakage inductance and small film capacitor for soft switching [665], [163], [168] address this setback. Eliminating active clamp, impulse resonant converters offer high reliability, power density. But energy stored in parallel resonance tank is not adaptive to the load demand, thus affects the efficiency at light load and higher input voltage. Further, power scaling of impulse commutated converters is challenging as they demand impractical leakage inductance at higher power levels. Also, [163] and [168] organized as modular structure, suffers bidirectional voltage blocking switch requirement.

To overcome this limitation, a wide range ZVS topology is proposed [169] that utilizes both, the leakage and the magnetizing inductances for soft switching of the devices. To store enough energy for soft switching at light load, magnetizing inductance is reduced by adding

external inductor in parallel to the transformer. This concept was extended to 3-phase topology for higher voltage gain and higher power applications [118]. It also demonstrates soft-switching down-to 10% of full-load, and down-to 50% of nominal input voltage by keeping magnetizing inductance at low value that adds to additional current. However, at higher power ratings, the required leakage inductance value is extremely low and practically difficult to realize and implement for higher power circuit development.

To eliminate the requirement of the external inductor for light-load soft-switching and other drawbacks, this Chapter proposes and analyses a current-fed three-phase isolated LCC-T resonant converter, as shown in Fig. 5.1. The proposed converter 1) eliminates the need of external inductor for soft-switching, 2) offers practically realizable design at higher power levels, 3) reduces current through the resonant tank and semiconductor devices through proper selection of parallel and series capacitor ratio, 4) generates sinusoidal transformer currents over wide load current and input voltage variations, and 5) permits ZVS turn-on of primary switches, and ZVS turn-on and ZVZCS turn-off of secondary devices adaptive to load current and input voltage variations.

This Chapter explains steady-state operation of proposed converter in Section 5.2, detailed design and modulation technique is reported in Section 5.3 and 5.4 respectively. Simulation and experimental results on proof-of-concept hardware prototype are demonstrated and discussed in Section 5.5 and 5.6, respectively.

5.2 Steady State Operation of the Converter.

This section presents operating modes pertaining to the first 120 degrees ($1/3^{rd}$) of one complete high frequency switching cycle as the three phases in the proposed converter are shifted by 120 degrees. Similar operating modes are repeated for the remaining switching cycle with other set of devices. For the analysis, it is assumed that 1) the resonant tank currents are approximated as sinusoidal, 2) all the components are ideal and lossless, 3) boost inductors at input are sufficiently large to maintain low ripple current, 4) output capacitors are large to maintain constant output voltage, 5) magnetizing inductance of the transformers are infinitely large, 6) $C'_{pa}, C'_{pb}, C'_{pc}$

are primary referred values while C_{pa}, C_{pb}, C_{pc} are secondary, 7) i_a, i_b, i_c are line currents of delta-star transformer. operating waveforms and equivalent circuits of various operating modes of proposed topology are shown in Fig. 5.2 and Fig. 5.3 respectively. I_{Lma}, I_{Lmb}, I_{Lmc} denotes peak value of per phase transformer/resonant tank current.

5.2.1 Mode 1:($\omega t_0 < \omega t < \omega t_1$); Fig. 5.3(a)

Turn-on of S_1 initiates this interval. By Kirchhoff's Current Law (KCL), it is seen that S_1 carries difference of input current i_{ina} and transformer line current i_a. During this interval, as Fig. 5.2 shows, i_a is smaller than i_{ina}. Therefore, turn on current of S_1 is negative, which confirms zero voltage turn-on (ZVS) of S_1. Current through S_1 charges clamp capacitor. Input inductors (L_{inb}, L_{inc}) continue to charge through S_4, and S_6 respectively. Devices S_1, S_4, and S_6 circulate resonant currents of resonant tank i_a, i_b, and i_c.

On the secondary side, voltage across the resonant capacitor C_{pa} is not enough to forward bias D_1. So C_{pa} keeps charging while capacitors in other phases C_{pb}, C_{pc} are clamped to half of the output voltage to allow i_{tfsb}, i_{tfsc} feed load through C_{sb}, C_{sc}, D_4, D_5.

5.2.2 Mode 2: ($\omega t_1 < \omega t < \omega t_2$) Fig. 5.3(b)

This interval starts when i_{tfsc} reaches zero and stops feeding the load as shown in Fig. 5.3(b). In addition, voltage across resonant capacitor C_{pc} is not sufficient to forward bias D_6 and engages i_{LrC} in discharging C_{pc}. Only resonant currents in phase B, i_{tfsb}, feeds the load. During this mode, i_a keeps increasing and current in front-end inverter continues to conduct as detailed in mode 1.

5.2.3 Mode 3: ($\omega t_2 < \omega t < \omega t_3$) Fig. 5.3(c)

This mode begins when i_a reaches i_{ina} resulting in zero current through switch S_1. Current through S_1 is positive and increasing during this mode. This also discharges clamp capacitor.

All other components maintain currents as described in above mode. This mode ends when gradual charging of C_{pa} reaches $V_o/2$ resulting in zero voltage across D_1.

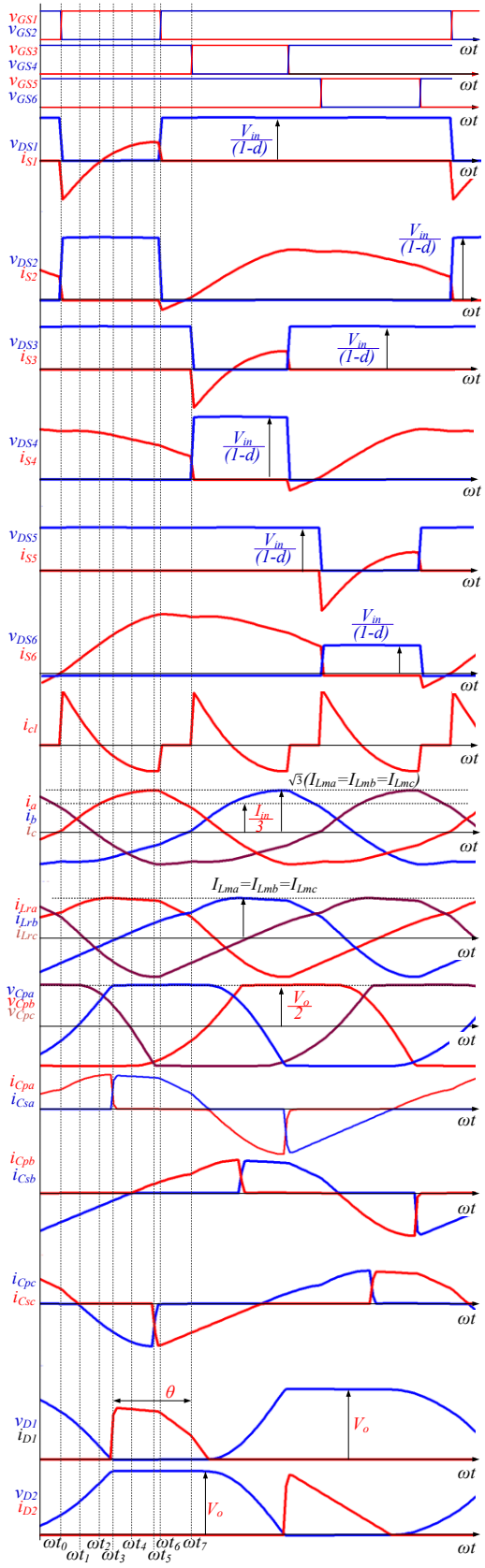


Fig. 5.2. Various operating waveforms of proposed converter.

5.2.4 Mode 4: ($\omega t_3 < \omega t < \omega t_4$) Fig. 5.3(d)

This mode begins with zero voltage conduction (ZVS) of D_1. This allows phase 'A' resonant current (i_{tfsa}) to feed the load along with phase 'B' resonant current (i_{tfsb}). This mode ends when resonant current in phase B reaches zero and stops feeding the load. This helps to turn-off D_4 under ZVZCS condition.

5.2.5 Mode 5: ($\omega t_4 < \omega t < \omega t_5$) Fig. 5.3(e)

During this mode, since resonant capacitor C_{pb} is unable to forward bias D_3, i_{tfsb} is engaged in charging C_{pb} and ceases to feed the load. Therefore, during this mode only phase A currents (i_{tfsa}) feeds the load.

Resonant currents continue to circulate through S_1, S_4, S_6. This mode ends when resonant capacitor C_{pc} charged sufficient to forward bias D_6. This also makes voltage across D_5 is zero.

5.2.6 Mode 6: ($\omega t_5 < \omega t < \omega t_6$) Fig. 5.3(f)

This mode begins with the ZVS conduction of diode D_6. This allows phase C resonant current (i_{tfsc}) to feed the load along with the phase A resonant current (i_{tfsa}). During this mode, resonant current at primary side are circulating through S_1, S_4, and S_6 and inductors L_{inb}, L_{inc} continue to charge through S_4, and S_6. This mode ends with the withdrawal of the gate-source voltage from S_1. At this instant, current through S_1 is positive and thus S_1 undergoes hard turn-off.

5.2.7 Mode 7. ($\omega t_6 < \omega t < \omega t_7$) Fig. 5.3(g)

This mode begins with the ZVS turn-on of the switch S_2. Withdrawal of the gate-source voltage of the switch S_1 leaves upper switches in three legs turned off. Due to this reason, clamp capacitor (C_l) neither charges nor discharges allowing it to maintain constant voltage across it. During this mode, input inductors L_{ina}, L_{inb}, and L_{inc} charges through S_2, S_4, and S_6 respectively. In addition, resonant currents circulate through S_2, S_4 S_6. On secondary, resonant currents in phase A,

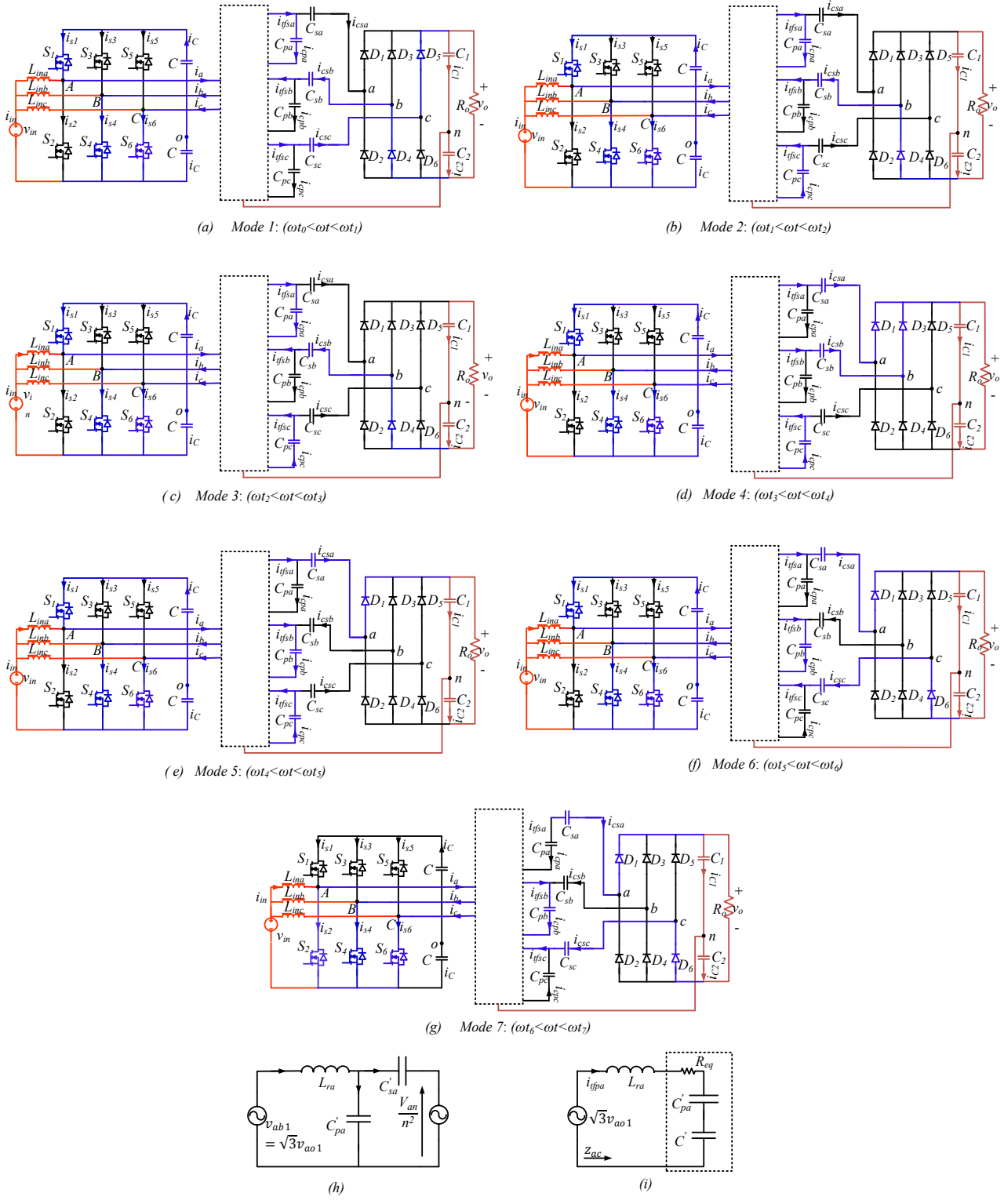


Fig. 5.3. (a)-(g) Equivalent circuits for various modes of operation of proposed converter. (h). Reduction of proposed converter into equivalent single-phase resonance tank and exciting equivalent voltage sources (i). Mathematical equivalent circuit of proposed

C continues to feed the load. This mode ends with the withdrawal of gate-source voltage from S_4 and applying it to S_3.

5.3 Design of the Proposed Converter

This section elaborates design of the proposed converter to interface a solar/fuel cell, whose input voltage ranging from 22-42V to stiff DC bus, rated at 350V to deliver 1kW load. Since the proposed converter is intended for solar/fuel cell, the main objective of the converter design is to maintain stiff DC voltage in output and high efficiency against fluctuations in input voltage and load changes. Resonant tank, LCC-T, need to store necessary energy to maintain ZVS under full load down to light load, at minimum input and maximum input voltage.

$$V_{sw\_max} = \frac{V_{in\_min}}{(1 - d_{max})} \tag{5.1}$$

$$z = \sqrt{L_{ra} \Big/ C'_{pa}} \tag{5.2}$$

$$\theta = 2\tan^{-1}\sqrt{\frac{2\pi n^2(1+\lambda)}{3\omega C'_{pa} R_o}} \tag{5.3}$$

$$R_{eq} = \frac{\sin^2\theta}{\pi\omega C'_{pa}(1+\lambda)}\ ; \quad C' = C'_{pa}\frac{\pi(1+\lambda)}{\sin\theta\cos\theta - \theta} \tag{5.4}$$

$$V_o = \frac{2\,V_{in}\sin(\pi d)}{\pi(1-d)}\frac{1}{|z_{ac}|}\frac{2\sqrt{3}n}{\left(\frac{f_s}{f_{pa}}\right)\frac{1}{z} + \frac{2\pi}{3}(1+\lambda)\left(\frac{n^2 P_o}{V_o^2}\right)} \tag{5.5}$$

$$I_m = \frac{I_{Lma}}{\sqrt{2}} = \left(\left(\frac{f_s}{f_{pa}}\right)\frac{V_o}{2\sqrt{2}n.\,z} + \frac{\pi n P_o(1+\lambda)}{3\sqrt{2}V_o}\right) \tag{5.6}$$

$$\lambda = \frac{C'_{pa}}{C'_{sa}} \qquad \lambda > 0\ ; \qquad f_{pa} = \frac{1}{2\pi\sqrt{L_{ra}C'_{pa}}} \tag{5.7}$$

$$I_{S1\_turn\_on} = i_{S1}|_{\omega t = \omega t_0} = 0 \tag{5.8}$$

$$I_{S2\_turn\_on} = i_{S2}|_{\omega t = \omega t_6} = 0 \tag{5.9}$$

5.3.1 Selecting d_{max} and switch voltage rating:

Maximum operating duty ratio of the front-end inverter is limited to 0.8 corresponding to minimum input voltage. The voltage blocked by switch during its off state is given by (5.1). A minimum input voltage of 22V, d_{max} of 0.8 translates maximum rating of switch to be 110V.

5.3.2 Selection of parallel resonance impedance (z):

Resonant impedance z offered by resonant inductor (L_{ra}) and primary referred parallel resonance capacitance (C'_{pa}), which is given by (5.2). Selection of this component plays an important role in the design of this converter because the proper selection of this component decides 1) minimum resonant currents, which ensure minimum peak, and RMS currents through switches and transformer therefore, better efficiency, 2) range of ZVS operation, and 3) type of modulation strategy needed for controlling the converter. To explore the effect of z on the converter, voltage gain and resonant current relations are needed.

5.3.3 Determining voltage gain and resonant current relation

Since the proposed converter operates with symmetry, without loss of generality, analysing one out of three phases is sufficient to determine the voltage gain and the resonant current relations. This also simplifies the design procedure. Fig. 5.3(h) shows conversion of front-end inverter and rear end rectifiers as simple voltage sources. In addition, the secondary capacitors are transferred to the primary to form LCC-T resonant tank. Assuming resonant current ($\underline{i_{Lra}}$) drawn by the transformer/resonant tank is sinusoidal; according to Fundamental Harmonic Analysis (FHA) as detailed in [26], the proposed converter can be reduced to Fig. 5.3(i) where (5.3), and (5.4) define the components of equivalent circuit. Here, θ is defined as the secondary diodes conduction time. Further, analysis culminates as voltage gain (5.5), resonant currents (5.6) and (5.7). Here f_s defines as switching frequency. Further detailed analysis is provided in [170], [171].

Equation (5.5) reveals voltage gain of the converter depends on two variables, relative switching frequency of operation (f_s/f_{pa}) and duty ratio (d) apart from design parameters such as

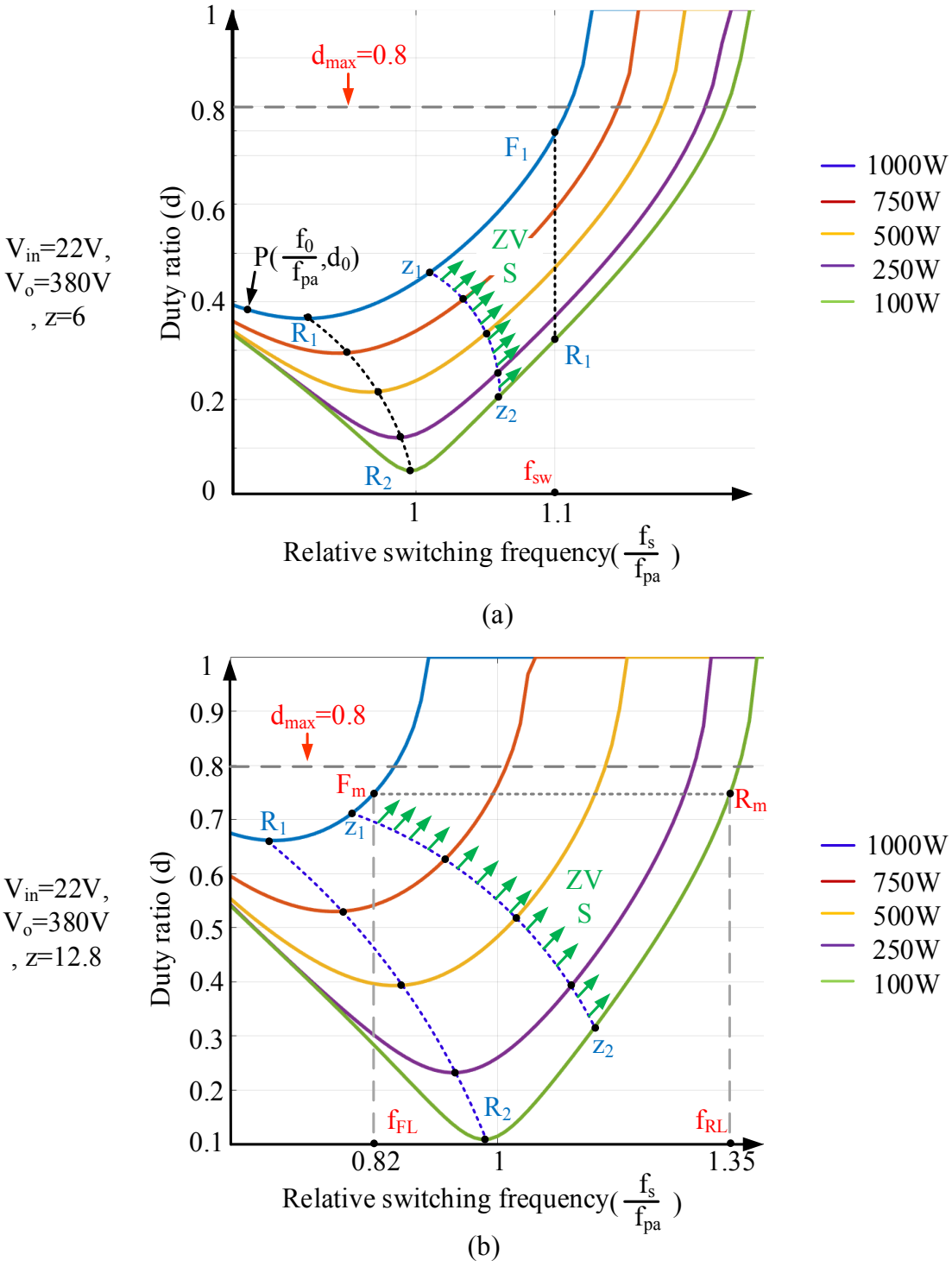


Fig. 5.4. Locus of operating points for (a) lower values of z (b) higher values of z; under minimum input voltage. ((F_1 (1.1, 0.75); F_2 (1.1, 0.31); F_m (0.82, 0.75); F_3 (1.35, 0.75); n=2 and λ=0.01 are assumed in both conditions).

turn-ratio of the transformer (n), parallel resonant tank impedance (z), and resonant capacitors ratio (λ) which are given by (5.2), and (5.7). Further, P_o, V_o, and V_{in} represents output power demand, output voltage, and input voltage

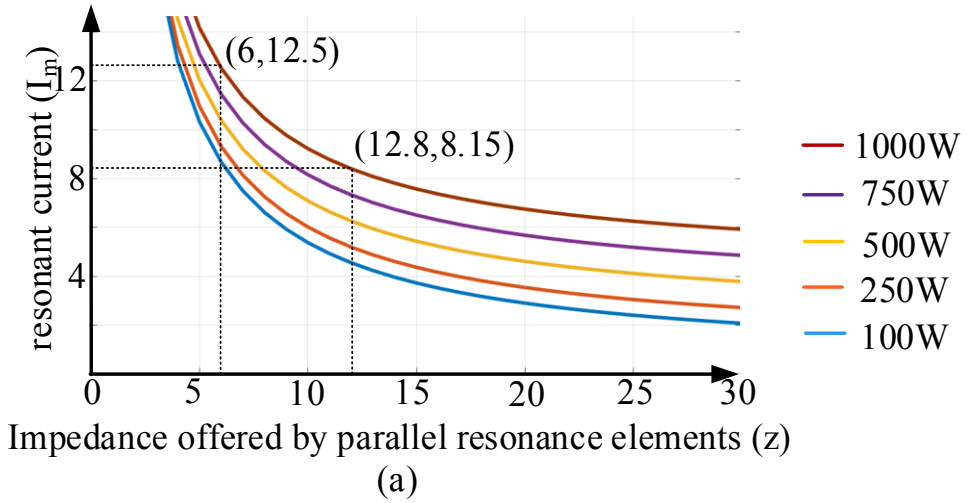
Since converter gain is influenced by f_s/f_{pa} and d simultaneously, there should exist multiple pairs of (f_s/f_{pa}, d) for a given value of P_o, V_o, and V_{in}. The locus of such points, called operating curves, with respect to various load demand at 350V output and minimum input condition (=22V) are presented in Fig. 5.4. With the knowledge of (5.8), and (5.9) boundary for ZVS region through various load is defined by locus z_1, and z_2 and tank resonance locus represented by R_1 and, R_2. A general operating point P ($\frac{f_0}{f_{pa}}$, d_0) is shown in Fig. 5.4 (a). On operating the converter designed with z=6, n=2, λ=0.01 at operating point P, i.e., relative switching frequency of $\frac{f_0}{f_{pa}}$ and duty ratio of d_0 , ought to generate 1kW at 350V from 22V input voltage. ZVS of the converter is assured if P lies in ZVS region.

5.3.4 Influence of z on modulation of converter:

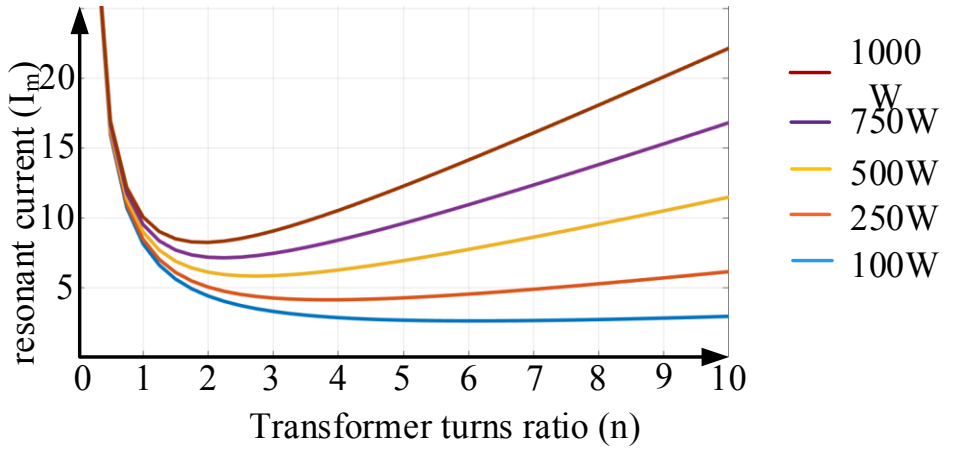
Curves are shown in Fig. 5.4 are plotted for the different values of z under minimum input voltage condition. Fig. 5.4(a) corresponds to the lower values of z such as 6Ω, while Fig. 5.4(b) corresponds to the higher values of z such as 12.8Ω.

In the case of lower z values, curves are relatively closer. By maintaining converter in ZVS, under minimum input voltage condition all the fluctuations in load power demand, say between 1kW and 100W, are compensated by operating the converter in locus F_1-R_1. Since all the operating points on locus F_1-R_1 comprise of same relative switching frequency, the converter operates at constant switching frequency or simple PWM.

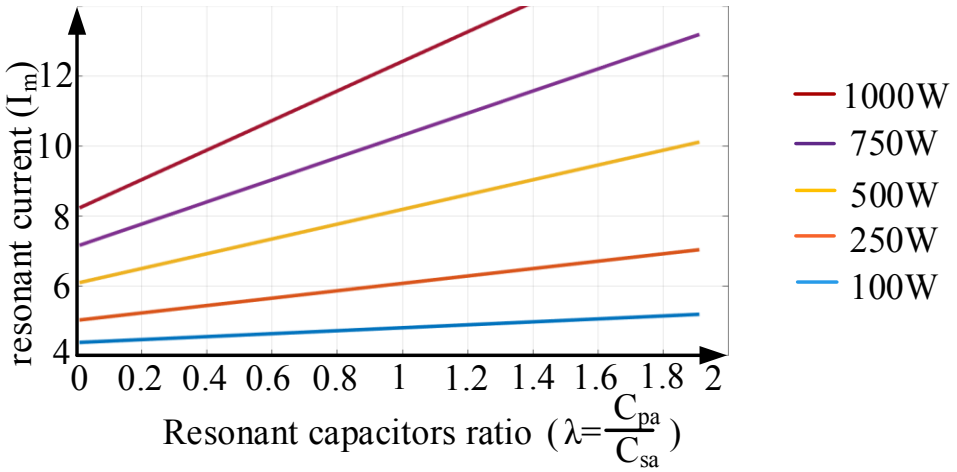
However, higher z values scatter operating curves. This forces the converter to adopt locus F_m-R_m to maintain ZVS and compensate load fluctuations between 1kW and 100W. This results in variable switching frequency operation.



(a)



(b)



(c)

Fig. 5.5. Influence of (a) z (b) n (c) λ on resonant currents (Im) (RMS) under minimum input voltage (22V).

5.3.5 Influence of z on efficiency.

Resonant currents are inversely related to z as given by (5.6) and evident from Fig. 5.5(a). It concludes lower resonant currents and higher converter efficiency are possible with higher z. On the other hand, higher values of z forces converter to operate in variable switching frequency mode. Lower values of z allow the converter to adopt simple PWM modulation but offers compromised efficiency.

Therefore, selection of z involves a trade-off between efficiency and modulation method of converter. Considering efficiency as prominent factor, higher values of z such as 12.8Ω are selected for this design. It is to be noted that, though further increment in z results in more reduction

	F_m	R_m	F_x	R_x
P_o	1000W	100W	1000W	100W
V_{in}	22V	22V	41V	41V

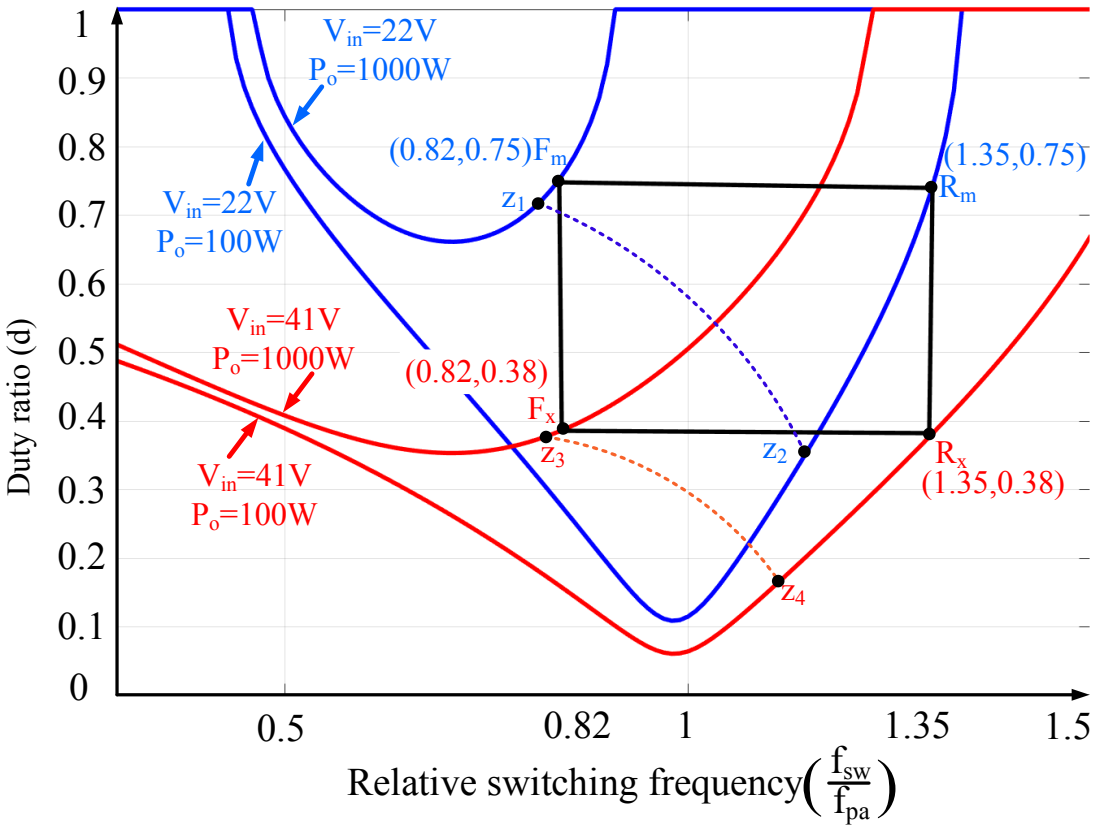


Fig. 5.6. Operating loci ensuring ZVS for all input and load condition

of resonant currents, it also pushes operating point beyond d_{max}=0.8 line (shown in Fig. 5.4) which is not recommended. So, with all above arguments, z=12.8Ω is selected.

5.3.6 Selection of transformer turns ratio (n)

As shown in Fig. 5.5(b), under full load condition, minimum resonance tank currents are possible for n=2.

5.3.7 Selection of resonant capacitors ratio (λ)

Fig. 5.5(c) shows a linear relationship between λ and resonance current. Respecting (5.7), lower values such as 0.01 are selected as λ. It is not recommended to diminish this value further, because such values demand bulky series capacitors, which are evident from (5.7).

5.3.8 Verification of ZVS condition under all extreme conditions:

Verification of ZVS when subjected to all possible extreme conditions ensures soft-switching under all operating conditions. Therefore, it is necessary to verify soft-switching in converter designed with parameters such as n=2, λ=0.01, and z=12.8 under all extreme conditions such as 1) full load-minimum input, 2) reduced load-minimum input, 3) Full load-maximum input, 4) reduced load-maximum input conditions whose operating points are given as F_m, R_m, F_x, R_x respectively.

Under minimum input voltage (22V) condition, as shown in Fig. 5.4(b), selected operating locus (F_m-R_m) lies in ZVS region defined by ZVS boundary (z_1-z_2). This ensures ZVS of converter under minimum input voltage, full and reduced load conditions. However, operating locus and ZVS boundary are vulnerable to input voltage. With rise in input voltage from minimum to maximum (22V to 41V), operating curves, operating locus, and ZVS boundary shifts downward as shown in Fig. 5.6. Further, new operating locus (F_x-R_x), which shows up in parallel to earlier operating locus F_m-R_m, also lies in ZVS region, defined by z_3-z_4, confirms soft-switching retention ability of the proposed converter under escalated input conditions.

5.3.9 Selection of resonance tank components:

Considering parallel resonance frequency (f_{pa}) as 100kHz, and z=12.8Ω, resonance components are selected as L_r, C_{pa} C_{sa} as 20µH, 31nF, 3.1µF using (5.2), an (5.7). capacitance C_{sa} is subjected to 6V as it is connected in series with the load (5.10), while C_{pa} with half of the output voltage, 180V (5.11).

$$C_l = \frac{\left(\frac{I_{in\_max}}{3} + \sqrt{3} I_{Lm\_peak}\right)\sqrt{1-d}}{6.\pi \Delta V_C f_s} \tag{5.13}$$

5.3.10 Selection of input boost inductor:

$$L_{ina} = L_{inb} = L_{inc} = \frac{V_{in} d}{f_s \Delta I_{in}} \tag{5.12}$$

$$I_{D1\_avg} = \frac{2I_{Lm}}{3} \frac{n^2(1+\lambda)}{2\pi n^2 f_s C_{pa} + \frac{2\pi}{3} n^2(1+\lambda)} \tag{5.14}$$

Since the proposed converter is a 3-phase current-sharing topology, three input inductors are necessary. Each inductor carries 1/3rd of the total input current. For a maximum power rating of 1kW and minimum input voltage of 22V, a possible maximum input current is 48A at an estimated efficiency of 95%. So current rating of each inductor is 16A. For a current ripple of 0.5A, switching frequency of 82kHz, $d_{\max}$ of 0.8, input inductor is calculated as 430µH using (5.12).

5.3.11 Selection of clamp capacitor (C_l):

Values of I_{in_max} and I_{Lm_peak} are calculated as 48A and 12A, respectively using (5.6). Assuming d=0.8, f_s=82kHz, and$\Delta V_C = 2V$, the clamp capacitor is selected as 4µF using (5.13). It is interesting to note that the frequency of current passing through the clamp capacitor is 3x the switching frequency. The voltage rating of the capacitor is the same as the switch.

$$v_{Csa} = I_{Lma} \frac{\lambda z n (1 - \cos\theta)}{\left(\frac{f_s}{f_{pa}}\right)(1 + \lambda)} \tag{5.10}$$

$$v_{Cpa} = v_{Csa} + \frac{V_o}{2} \tag{5.11}$$

5.3.12 Selection of Voltage doubler diodes:

The current rating of the voltage doublar diodes is given by (5.14). Considering for maximum power output under minimum input conditions, diode current rating is calculated as 2A. It is observed that diodes are turned off at ZVZCS. So, there is no reverse recovery time needed for the diodes. So fast grade diodes are not mandatory. Under turn off conditions, each diode blocks entire output voltage. Therefore, voltage rating of voltage doubler diodes is 350V.

5.3.13 Selection of output filter capacitors

The value of output capacitors filter is calculated as 2μF based on the relation given by (5.13) under assumption of 1V output voltage ripple. Each capacitor is charged to half of output voltage. Therefore, voltage rating of capacitor is 175V

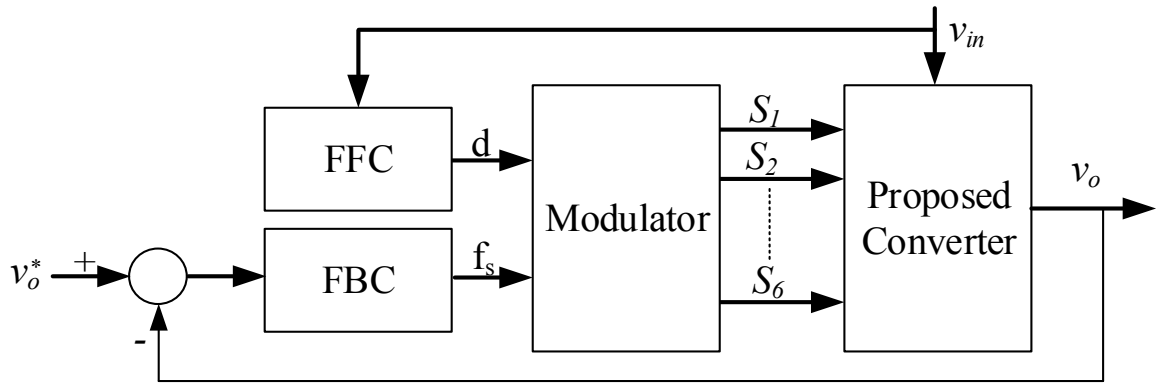


Fig. 5.7. Block diagram for closed loop control of proposed converter

5.4 Modulation strategy

A hybrid modulation strategy is proposed such that all input disturbances under constant loaded conditions are regulated by duty ratio compensation and all load fluctuations under constant input are regulated by switching frequency compensation. Although the modulation looks complex, interestingly its implementation is very simple in reality, whose block diagram is shown in Fig. 5.7.

Under constant load conditions, the proposed converter uses a feedforward controller (FFC) to compensate all input disturbances, even before they reflect on the load, by recommending appropriate duty ratio without affecting operating frequency. Such a shift in duty ratio at constant operating frequency lies in parallel to and in between loci F_m-F_x and R_m-R_x.

On the other hand, under steady input conditions, proposed topology uses a feedback controller (FBC) to compensate all load disturbances by recommending appropriate switching frequency without affecting duty ratio of operation. Such a shift in switching frequency at constant duty ratio lies in parallel to and in between loci F_m-R_m and F_x-R_x.

Fig. 5.6 shows a rectangle formed from operating loci with vertices R_x, F_x, F_m, and R_m. The proposed hybrid modulation strategy operates the proposed converter inside this rectangle to ensure the desired output voltage under all input and load disturbances. Further soft switching is maintained in all conditions.

5.5 Simulation Results

The proposed converter is designed for a power rating of 300W, whose input voltage and output voltages are selected as 22-42V, and 350V, respectively. Proposed converter is simulated in PSIM 10 to verify the proposed operation and analysis. Simulation results for two extreme cases at full load and light load are presented.

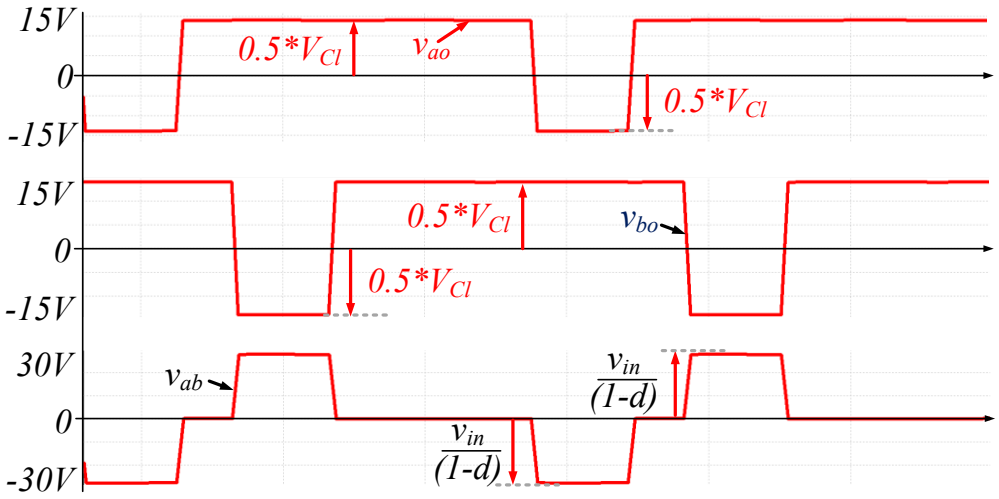


Fig. 5.8. Phase (v_{ao},v_{bo}) and line to line (v_{ab}) voltages of the front end inverter feeding light load under minimum input condition.

Figure 5.8 shows the phase (v_{ao},v_{bo}) and line to line (v_{ab}) voltage output of the front end inverter at light load condition. Phase voltage has equal positive and negative peak voltage. This is because clamp capacitors $2C_l$, $2C_l$ divide the DC bus voltage equally. Though v_{ao}, and v_{bo} have offset DC voltage, this is canceled out in the line voltage v_{ab}, which is essential for the transformer operation. Positive and negative peak voltages of v_{ab} are equal to the DC bus voltage.

Fig. 5.9 (a1) and (a2) show the line currents (i_{Lra}, i_{Lrb}, i_{Lrc}) and phase currents (i_{tfpa}, i_{tfpb}, i_{tfpc}) at 3-ph transformer primary at full load and light load respectively. It is observed that transformer currents or circulating currents are maintained sinusoidal for complete load variations. It is also observed that at light load transformer currents are more sinusoidal than full load. This is because from operating curves, it is shown that at light load, the operating point is closer to resonance than full load. Also, circulating currents with a peak value of 5.8A is observed at full load through transformer. While 5.3A is predicted through theoretical calculations as shown in Fig. 5.9. At light load, the peak of circulating currents is 3.8A.

Fig. 5.9 (c) and (d) show the ZVS turn-on of the front end inverter devices at full and light load, respectively. Though waveforms for only one leg is presented, similar ZVS switching is observed for all other switches. Fig. 5.9(c) and (d) show current for phase ‘a’ boost inductor, which is charging and discharging according to the conduction status of lower switch. Peak currents on

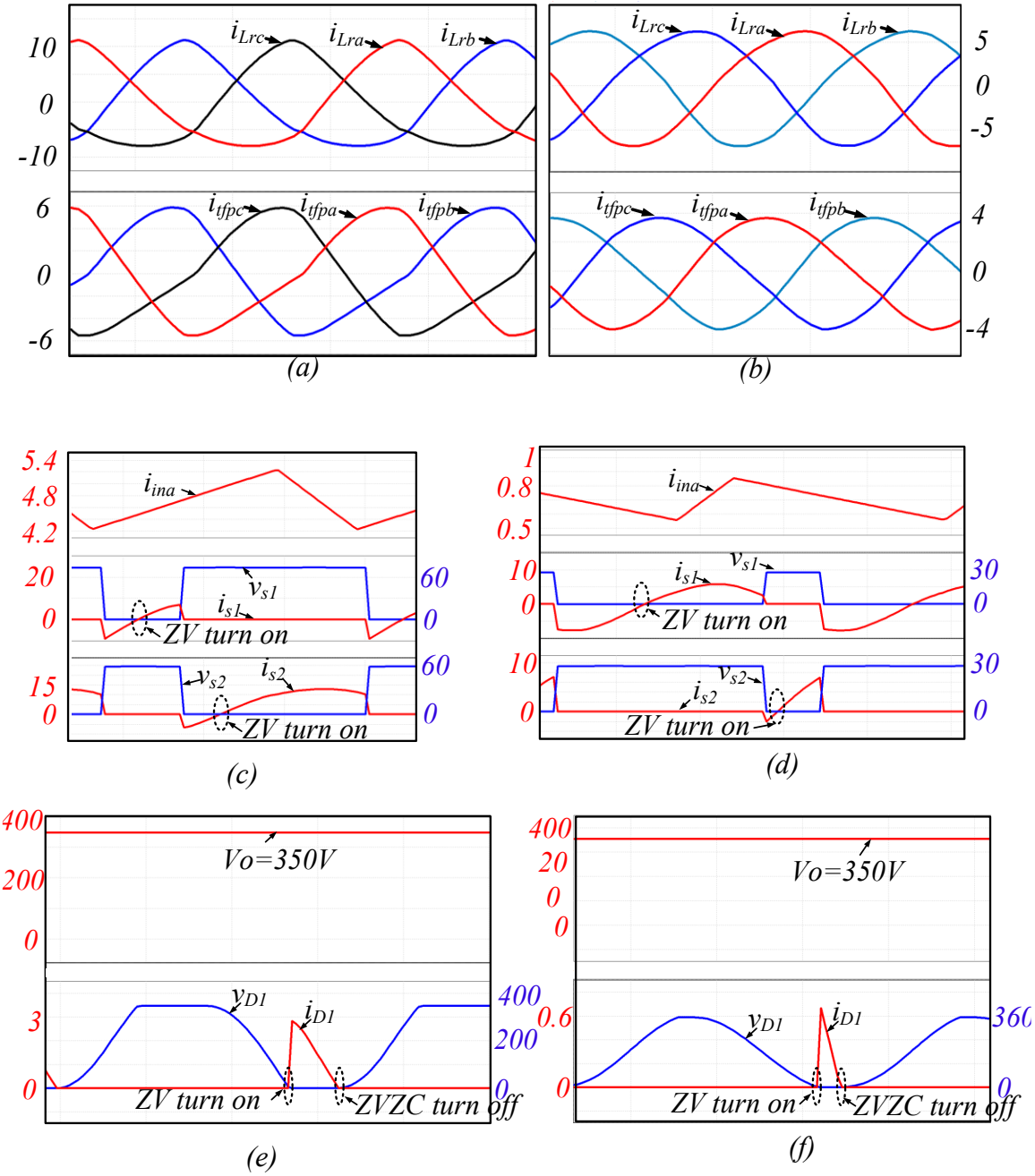


Fig. 5.9. Line and phase currents of transformer primary (a) Full load (b) Light load; Input current per phase (i_{ina}), Top and bottom switch voltages v_{s1}, v_{s2} respectively, Top and bottom switch currents i_{s1}, i_{s2} respectively at (c) full load (d) light load; Output Voltage V_o, voltage doublar diode voltage (v_{D1}), and current (i_{D1}) at (e) Full load, (f) Light load.

the switches appear at full-load condition which are given by 12.96A and 6.77A on lower and upper switches, respectively.

Fig. 5.9(e) and (f) show the output voltage of the converter is maintained at 350V from 22V input against full and light load conditions respectively. Fig. 5.9 (e) and (f) also shows the ZV turn on and ZVZC turn off of secondary diodes at all load conditions. This feature of the converter is inherent and independent of loading conditions. This feature eliminates the requirement of fast recovery diodes, losses in reverse recovery of diodes, and diode turn off ringing.

At all load conditions, a gain of 15.9, ZVS in primary, and ZV turn-on, as well as ZVZC turnoff of the secondary diodes, are maintained in the proposed topology and modulation.

5.6 Experimental Results

This section validates the proposed theory by presenting the results obtained from testing a hardware prototype as designed in section 5.3. The following is a list of components selected for prototype implementation.

5.6.1 Component Selection

5.6.1.1 Front end inverter switches S_1-S_6:

Voltage rating of switch is limited to 110V in proposed converter. Further, selecting a MOSFET with less conduction losses is conducive for maintaining possible higher efficiency. So IRFB4115PbF manufactured by Infenion is selected. Another major advantage is its brief turn off time which helps in minimizing turn-off losses at higher frequencies. Since proposed converter

Table 5.1. Comparison of calculated and components used in prototype

	T	P
L_{ra} =L_{rb} =L_{rc} (μH)	20	19.6,20.3,19.5
C_{pa} =C_{pb} =C_{pc} (nF)	31	30, 30, 30
C_{sa} =C_{sb} =C_{sc} (μF)	3.1	3.06, 3, 3.06
T- Theoretical; P-Prototype		

cannot provide soft switching during turn off, this MOSFET is highly desirable. Further, dead time in all switches is maintained constant and equal to sum of delay, rise and fall times of MOSFET.

5.6.1.2 Rear end rectifier diodes D_1-D_6:

Diodes need to block entire output voltage under turn-off conditions. Therefore, diode rating should be 400V least and RFU10TF6S diodes whose voltage rating of 600V are chosen for this application.

5.6.1.3 Transformer:

N 89 material ferrite E core is used to wind three transformers with 1:2 turns ratio. Interleaved winding is avoided in transformer to achieve higher leakage inductance, which in turn benefits converter. The obtained leakage inductances of transformers are 19.6μH, 20.3μH, 19.5μH while their magnetizing inductances are 972μH, 958μH and 975μH. Since transformer alone able to provide required leakage inductance, no extra resonant inductor is needed for proposed converter. Magnetizing current in practical converter results in slight increment of conduction loss.

5.6.1.4 Resonant capacitors:

Film Capacitors 30nF, 200V (168105J50G-F) and 3μF, 30V (103MWR400K) are selected as parallel and series resonant capacitors.

Due to constraints in practical world, it is not possible to achieve exact designed values. However, practical components are selected to respect designed parameters z, λ. A comparison is provided in Table 5.1 and a list of components selected is presented in Table 5.2.

5.6.2 Testing and Experimental Results

Fig. 5.10 presents experimental results of the proposed converter, which is tested for minimum input condition (22V) and delivering load at 350V. Fig. 5.10 (a), (b) and (c) correspond to the full load, while Fig. 5.10 (d), (e) and (f) represent reduced load conditions. Resistance of

Table 5.2. List of components and part numbers for hard-ware.

	Component	Part number/Remarks
1	The FEI switches (S_1~S_6)	200V, 64A, IRFB4115PbF.
2	The VDR diodes (D_1~D_6)	600V, 8A, RFU10TF6S.
3	Clamp capacitor	4uF, 150V electrolytic off the shelf
4	Output filter	4uF, 150V electrolytic off the shelf
5	Resonant series capacitor	3μF, 30V (103MWR400K)
6	Resonant parallel resonant capacitor	30nF, 200V (168105J50G-F)
7	Input inductors (L_{ina}, L_{inb}, L_{inc})	N89 material core, 430μH.

122.5Ω and 1225Ω are selected to emulate full load and reduced load conditions, respectively. F_m *(*89*kHz,* 0.78*),* R_m *(*153*kHz,* 0.78*)* are corresponding operating points. Table 5.2 provides a comparison of analytical and experimental operating points.

Fig. 5.10 (a) shows gate-to-source voltage and drain to source voltage of top and bottom switches. Also, for fair analysis, the switching instants are also zoomed. Zoom 1 of Fig. 5.10 (a) reveals that prior to the application of the gate voltage (v_{GS1}), the drain voltage (v_{DS1}) of switch S_1, which was in blocking mode, drops to zero. Therefore, as soon as v_{GS1} applied to S_1, it undergoes ZVS turn-on. The same argument holds good for S_2. With this discussion, it is evident that switches S_1, and S_2 as shown in Fig. 5.10 (a) are operating in ZVS under minimum input and full load conditions (also true for remaining switches S_3 ~ S_6). Fig. 5.10 (b) shows transformer secondary currents or resonant currents in the converter, which are 120-degree phase shifted confirms 3-phase operation. Further, sinusoidal transformer currents maintain reduced core losses. Fig. 5.10 (c) shows proposed converter's ability to maintain designed output voltage, 350V. In addition, Fig. 5.10 (c) shows transformer secondary voltage which, is also phase shifted by 120 degrees.

At minimum input conditions, a load disturbance from full to light or 1kW to 100W, according to hybrid modulation strategy, is subdued by pushing switching

Operating condition:
V_{in}=22V
V_o=350V
P_o=1000W
Operating point F_m(89kHZ, 0.78)

Operating condition:
V_{in}=22V
V_o=350V
P_o=100W
Operating point F_m(135kHZ, 0.78)

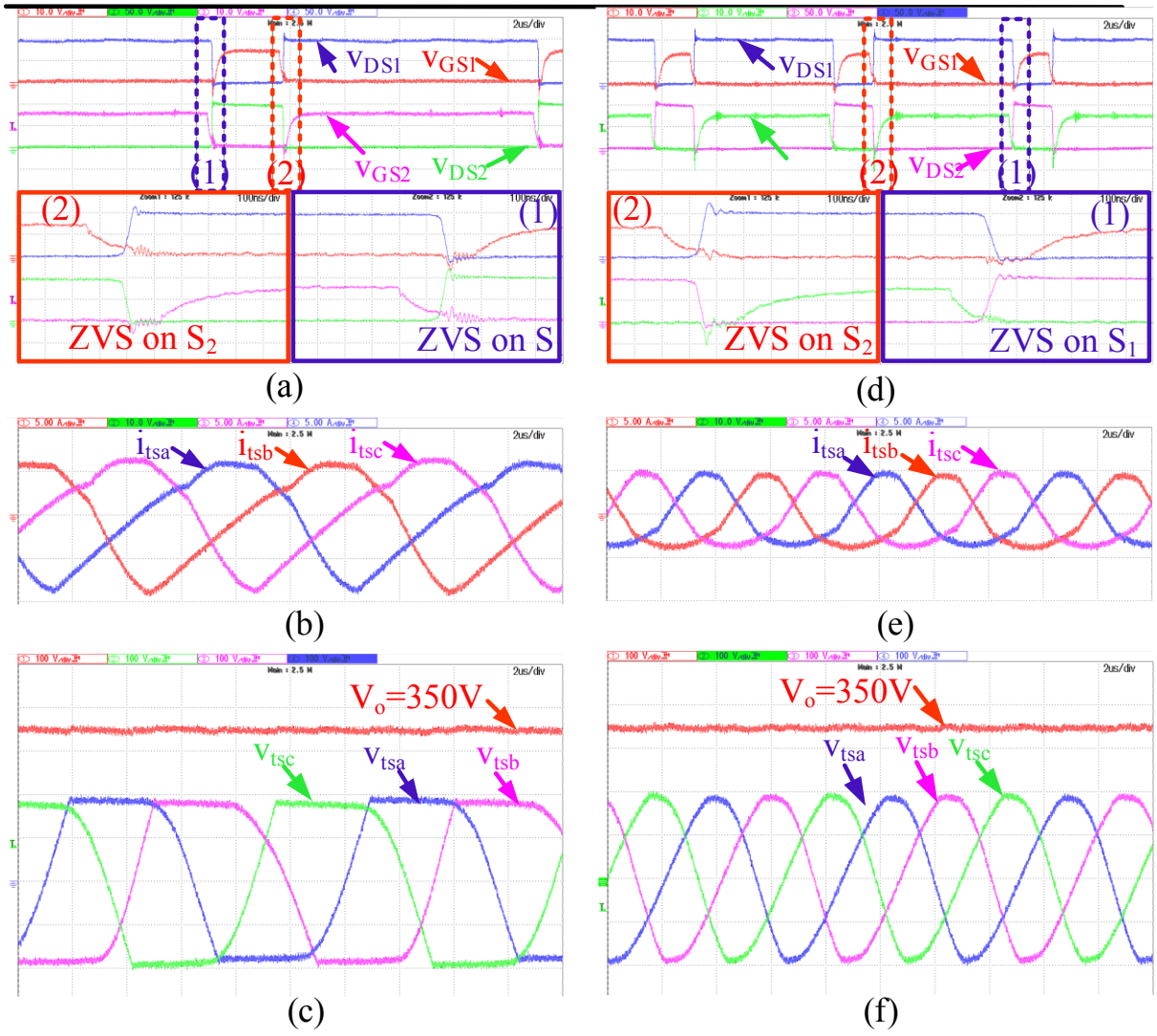


Fig. 5.10. Results obtained when developed prototype fed with constant input voltage 22V and output voltage 350V maintained. Gate to source voltage of switches S_1, S_2. (v_{GS1}, v_{GS2}) [Scale: 10V/div]; Dain to source voltage of switches S_1, S_2. (v_{DS1}, v_{DS2}) [Scale: 50V/div]; Transformer secondary currents, (i_{tsa}, i_{tsb}, i_{tsc}) [Scale: 5A/div]; Output voltage, (V_o) [Scale: 100V/div]; Transformer secondary voltage, (v_{tsa}, v_{tsb}, v_{tsc}) [Scale: 100V/div].

Operating condition:
V_{in}=41V
V_o=350V
P_o=1000W
Operating point F_m(89kHZ, 0.42)

Operating condition:
V_{in}=41V
V_o=350V
P_o=100W
Operating point F_m(135kHZ, 0.42)

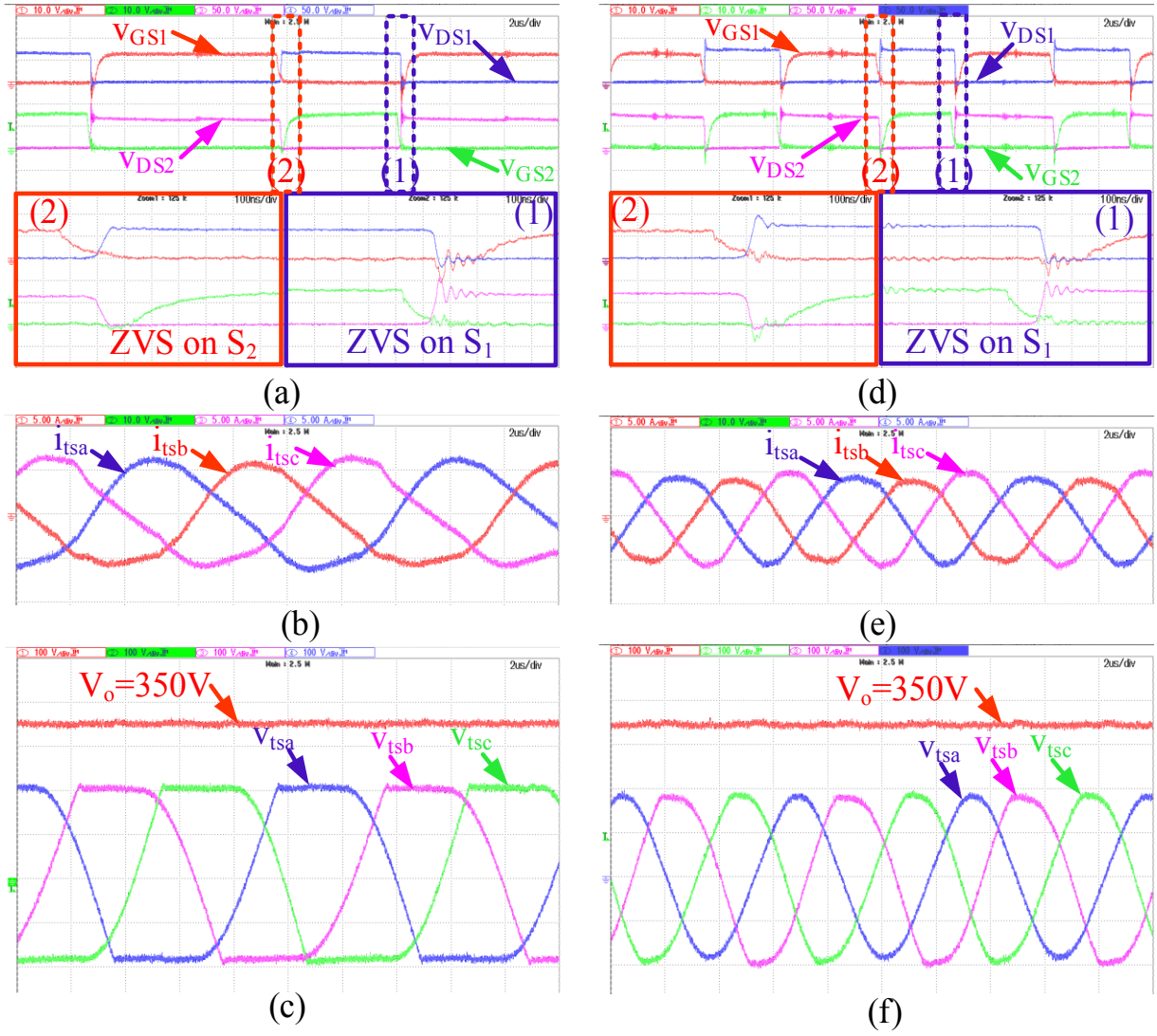


Fig. 5.11. Results obtained when developed prototype fed with constant input voltage 41V and output voltage 350V maintained. Gate to source voltage of switches S_1, S_2. (v_{GS1}, v_{GS2}) [Scale: 10V/div]; Dain to source voltage of switches S_1, S_2. (v_{DS1}, v_{DS2}) [Scale: 50V/div]; Transformer secondary currents, (i_{tsa}, i_{tsb}, i_{tsc}) [Scale: 5A/div]; Output voltage, (V_o) [Scale: 100V/div]; Transformer secondary voltage, (v_{tsa}, v_{tsb}, v_{tsc}) [Scale: 100V/div].

frequency form 89kHZ to 153kHz without affecting duty ratio (0.78) of converter. In other words, operating point is shifted from F_m to R_m. Fig. 5.10 (d) shows switching wave forms of converter under new steady state. Fig. 5.10 (d) proves converter's ability to maintain soft switching under load disturbance. Fig. 5.10 (e) shows resonant currents of converter under reduced load condition. Fig. 5.10 (f) shows transformer secondary voltage. Due to reduced diode conduction time, they appear near sinusoidal.

Like Fig. 5.10, Fig. 5.11 presents converter switching waveforms at maximum input condition (41V) and delivering load at 350V. Fig. 5.11 (a), (b), and (c) correspond to full load condition realized by operating point F_x *(*89*kHz,* 0.42*)* while Fig. 5.11 (d), (e), and (f) correspond to reduced load condition realized by operating point R_x *(*153*kHz,* 0.42*)*.

Like Fig. 5.10 (a), Fig. 5.11 (a) confirms proposed converter can maintain ZVS under maximum input condition while maintaining 350V, as shown in Fig. 5.11(c). Fig. 5.11(b) shows sinusoidal resonant currents, which are reasonable for ZVS, shifted by 120 degrees. At maximum input condition, a load disturbance form full to reduced or 1kW to 100W is stabilized by pushing switching frequency from 89kHz to 153kHz, without affecting operating duty ratio, 0.42, with to hybrid modulation technique. To put it simply, operating point is shifted from F_x (89kHz, 0.42) to R_x (153kHz, 0.42). Switching waveforms under new steady state, as presented in Fig. 5.11 (d), confirms converter's competence to maintain soft switching through wide load interruptions. Fig. 5.11 (e) shows resonant currents under reduced load conditions. Fig. 5.11 (f) shows output voltage and transformer secondary voltage.

Fig. 5.12 (a1), and (a2) show the simulated voltage and current waveforms of rear-end rectifier diode (D_1) at minimum input condition. This shows that prior to conduction of D_1, blocking voltage gradually reaches to zero due to charging of C_{pa}. Therefore, D_1 undergoes ZVS turn-on. On the other hand, at turn off instant, current through it reaches zero. Further it does not enter blocking mode instantaneously rather gently. Therefore, D_1 turns-off with ZVZCS mode. This is valid for all diodes irrespective of input and output disturbances. Since diode does not enter blocking mode immediately, fast recovery diodes are not necessary.

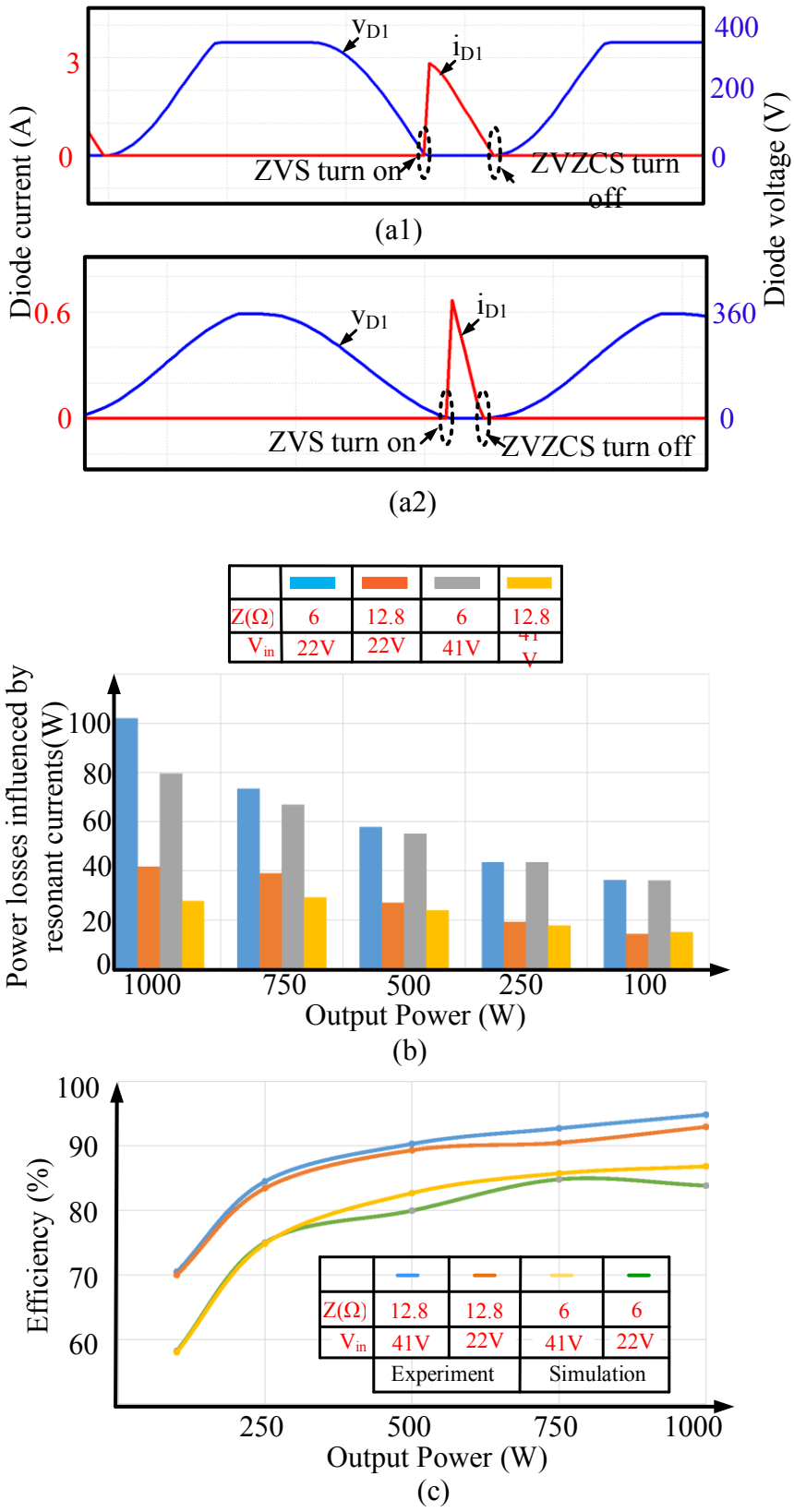


Fig. 5.12. Voltage across and current through rear end rectifier diode under minimum input and (a1) full (a2) light load conditions; (b) Power loss influenced by resonant currents; (c) Efficiency of proposed converter for lower z values and higher values of z.

Table 5.3. Comparison of theoretical and experimental operating points

P_o(W)	V_{in}		f_s/f_{pa}	d	f_s(kHz)
1000	22V(F_m)	T	0.82	0.75	82
		P	0.89	0.78	89
		e	7.8%	3.8%	7.8%
	41V(F_x)	T	0.82	0.39	82
		P	0.89	0.42	89
		e	7.8%	7.1%	7.8%
100	22V(R_m)	T	1.35	0.75	135
		P	1.53	0.78	153
		e	11.7%	3.8%	11.7%
	41V(R_x)	T	1.35	0.39	135
		P	1.53	0.42	153
		e	11.7%	7.1%	11.7%

T: Theoretical, P: Prototype, *e:* %error

To achieve better efficiency, selecting higher *z* such as 12.8Ω instead of *6Ω* is instrumental in pulling down resonant currents by 35%, as shown in Fig. 5.5(a). A comparison of calculated loses related to resonant currents are presented in Fig. 5.12 (b). Fig. 5.12 (c) shows the efficiency of proposed converter. Maximum efficiency of 94.5% is abosrved at full load conditions and

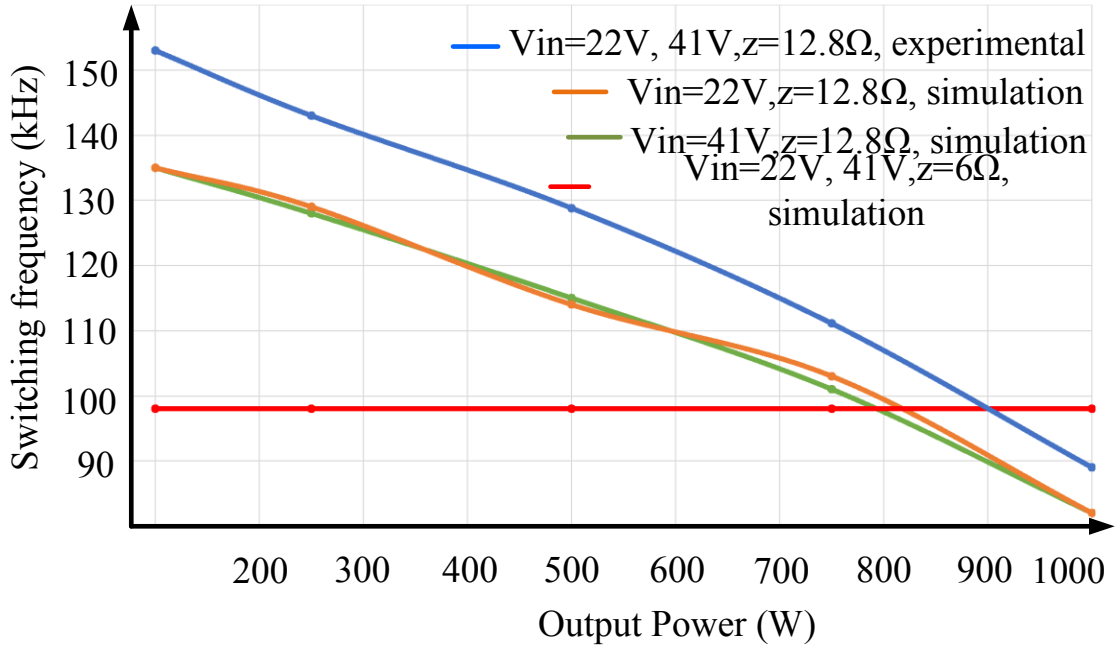


Fig. 5.13. Variation in switching frequency demanded by proposed converter with respect to various *z* values, and output power

maximum input. The fact that, proposed converter maintains above 90% efficiency till half load for all inputs can qualify this converter as potential candidate for Fuel cell applications. For comparison, Efficiency of converter under low values of z is also provided.

Proposed converter adopts a hybrid modulation technique, which involves frequency modulation under load disturbances. Therefore, Fig. 5.13 details the range of frequency required for load compensation and error in operating frequency between theory and experiment. This discrepancy is accounted for inaccuracies in transformer leakage inductance measurement, unquantified variations of transformer leakage inductance with switching frequency and finite magnetizing inductance.

Although [118] is intended for higher power applications, it was designed and tested at low power rating of 300W. To facilitate a fair comparison, [118] is redesigned and simulated using PSIM 11.0 for 1kW. A comparison, as shown in Table 5.3, reveals that proposed converter and modulation can offer reduced peak and RMS currents through transformer and devices, which is substantial to limit losses and improve efficiency. On the other hand, halved turns ratio due to inclusion of voltage doubler rectifier and reduced transformer kVA rating confirm improved power density of the proposed topology. Further, proposed topology can eliminate additional parallel inductor mandatory for soft-switching without compromising soft-switching range, peak current stress, efficiency and power density. It is also clear from area product of magnetics (A_p) that a reduction in magnetics volume by 41.25% and improvement of transformer utilization factor (TUF) by 36.86% is observed in proposed converter. Ability to integrate soft-switching elements with transformer parasitics is retained.

However, from Table 5.3, it is observed that [118], on redesigning for higher power, demands meagre leakage inductance value, which is practically challenging. On the other hand, proposed converter requires 19.6μH leakage inductance, which is practically feasible to achieve and can be further scaled for higher power.

Table 5.4. Comparison of proposed converter

Parameter	[118]	Proposed
Output voltage	350V	350V
Input voltage	22-41V	22-41V
Power	1kW	1kW
Switch peak voltage	110V	110V
Lower switches		
RMS current	21.8A	21.9A
Peak current	44.5A	34.1A
Upper switches		
RMS current	10.71A	9.3A
Peak current	24.1A	14.1A
Transformer		
RMS current	11.13A	8.11A
Peak current	22.78A	10.75A
Turns ratio	4	2
RMS voltage	69.1V	69.1V
VA rating	2.3kVA	1.68kVA
TUF	0.434	0.594
Soft-switching elements		
Series inductor	681nH	19.6μH
Parallel inductor	165μH	NA
Parallel capacitor	NA	30nF
Series capacitor	NA	3uF
Size of magnetics (A_p)		
Transformer	b(1.922)mm^2	b(1.401)mm^2
External inductor	b(0.463)mm^2	NA
Total	b(2.385)mm^2	b(1.401)mm^2

NA: Not Applicable; Ap: Area Product; $b=1/(B_{max}K_wJ)$; B_{max}=Peak Flux density of magnetic core; K_w=Window factor constant; J=Current

5.7 Conclusion

Converters intended for solar and fuel cell applications should be capable of handling wide disturbances in load current and source voltage. In addition, soft-switching is necessary to achieve reduced footprint and better efficiency when operating the devices at high-frequency. To achieve soft-switching under full-load and partial-load conditions, conventional techniques need an external inductor in parallel to transformer, which generates higher peak and RMS currents through switches and transformer resulting in high kVA rating and losses.

In this Chapter, to eliminate above-mentioned drawbacks, a 3-phase isolated current-fed dc/dc converter is proposed. Steady-state operation, analysis and design of the converter are reported. This converter uses LCC-T resonance tank, which needs two small high-frequency film capacitors to achieve ZVS turn-on of primary switches and ZVS turn-on and ZVZCS turn-off of secondary switches without affecting soft-switching range. Further, peak and RMS currents through switches and transformer are reduced. Volume of magnetics is reduced by 41.25% and TUF is improved by 36.86%.

To verify the proposed theory, 1kW rated hardware prototype was designed and developed in laboratory and experimental results are presented. Obtained results verify the claims and the performance of the proposed converter. Next Chapter studies the characteristics of the converter when a series resonant tank is used.

Chapter 6 Analysis and Design of ZVS Current-fed Isolated LCL Series Resonant DC/DC Converter

6.1 Introduction

A parallel/modified parallel resonance-based resonant tank, LCC-T, has been studied under ZCS and ZVS modes in Chapters 3, 4 to achieve high voltage gain, high efficiency, and high density. In a parallel/modified parallel resonant converter, the parallel capacitor (C_p) connected in parallel with the load (via voltage doubler) delivers the required output voltage as shown in Fig. 6.1(a). Since the application under consideration needs regulated constant output voltage, the parallel capacitor in the resonant tank is also supposed to maintain a constant peak voltage, equal to half of the output voltage, across it as shown in Fig. 6.1 (a). This demand in peak voltage is fulfilled by resonant tank current. Therefore, under light load conditions, a significant amount of the resonant current is needed in the tank, as shown in Fig. 6.1(b), to maintain peak voltage across C_p. This incurs excess conduction losses in the switches, DC link capacitors, and the resonant tanks. Therefore, parallel resonance tank-based dc/dc converter offers reduced light load efficiency. On the other hand, the main advantage of a parallel/modified parallel resonance technique is the ability of the tank to contribute to the overall gain of the converter. This reduces the transformer turns ratio significantly.

In this Chapter, dual of parallel resonance technique, a series resonance-based tank as shown in Fig. 6.1(c) is adopted to achieve soft-switching in a high voltage gain dc/dc converter. In the case of a series resonant tank adopted converter, the resonant tank inductor acts as a current source, which injects the required load current via a voltage doubler to maintain the desired output voltage. Therefore, it can be concluded that as the name suggests, both, the load and the resonant tanks are connected in series thus they share the same current irrespective of the load demand and availability of input voltage. This is also evident from Fig. 6.1(c). This concludes that the resonant current in the series resonance tank is directly dependent on the load current. This helps to maintain

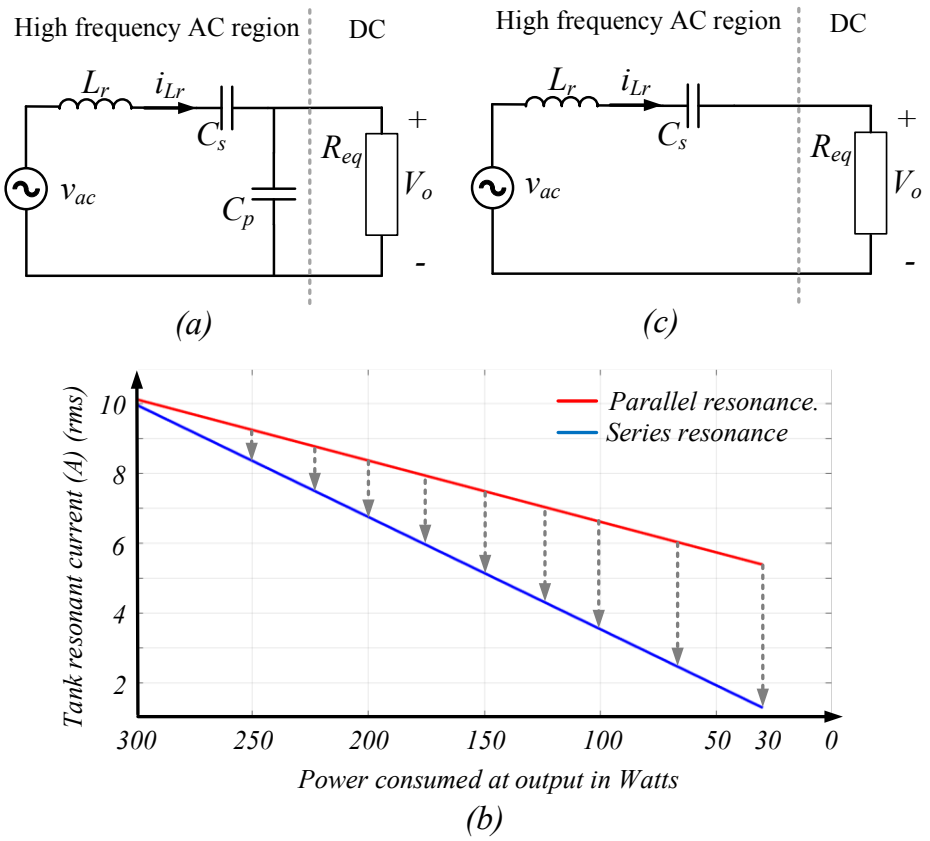


Fig. 6.1. (a) parallel/modified parallel resonant tank (LCC); (b) resonant tank currents in a high voltage gain dc/dc converter if implemented with series resonance and parallel resonance tanks; (c) series resonant tank;

t he minimum possible resonant tank current under light load to achieve the minimum. It is verified from Fig. 6.1(c). In a high voltage gain dc/dc converter, for a given power rating and specifications, a series resonance dc/dc converter can maintain minimum resonant current under light load condition when compared to a parallel resonance dc/dc converter. This shows that a series of resonance tank in high voltage gain dc/dc converter has the highest potential to maintain better efficiency at both full-load and light-load conditions.

6.2 Proposed Series Resonance Based High voltage gain DC/DC Converter

Apart from processing load power, the resonant tank in the converter also needs to maintain the soft-switching in front end inverter switches, either ZVS or ZCS depending on the operation. This is achieved by discharging/charging the drain-to-source capacitance with the help of energy stored in the resonant tank. As discussed earlier, resonance current stores available energy in the resonance tank. Under the full-load condition, maximum current in the resonant tank flows thus enough energy is available in the tank to bring soft-switching the switches. But in the case of light load condition, the energy required is naturally not enough to charge/discharge drain-to-source capacitors due to minimum load current. Therefore, the inclusion of an external parallel inductor in a series resonance tank is proposed in the literature to store required excess energy under the light load condition. Since the current flowing in the parallel inductor is not dependent on the load current alone, but also voltage appearing across it, it can be designed to maintain the required energy to charge/discharge drain-to-source capacitance of MOSFETs even under light load conditions. Modification of the series resonance tank by introducing an external parallel inductor can be achieved in three possible ways as shown in Fig. 6.2 (a), (b), and (c) and corresponding high voltage gain dc/dc converters are also shown in Fig. 6.2 (d), (e) and (f).

In the case of the LCL-SRC resonant dc/dc converter, the parallel inductor (L_p) is connected as shown in Fig. 6.2 (a), (d). The parallel inductor (L_p) is constantly subjected to alternating voltage with $V_o/2$ as its peak value. Since the converter is supposed to maintain constant output voltage, the current through L_p is hardly dependent on input voltage available and load current. Therefore, with the help of L_p, LCL-SRC resonant tank can contain enough resonant energy under all load conditions and available input voltage to bring soft-switching.

Similarly, the external parallel inductor (L_p) can be connected as shown in Fig. 6.2 (b) to form (L)(LC)-SRC resonant tank. Unlike LCL-SRC, L_p in (L)(LC)-SRC resonant converter as shown in Fig. 6.2 (e) is subjected to the alternating voltage generated due to switching action of S_1 and S_2 that is positive and negative voltages of DC-link capacitors, $v_{C1,}$ and $v_{C2.}$ Like LCL-SRC,

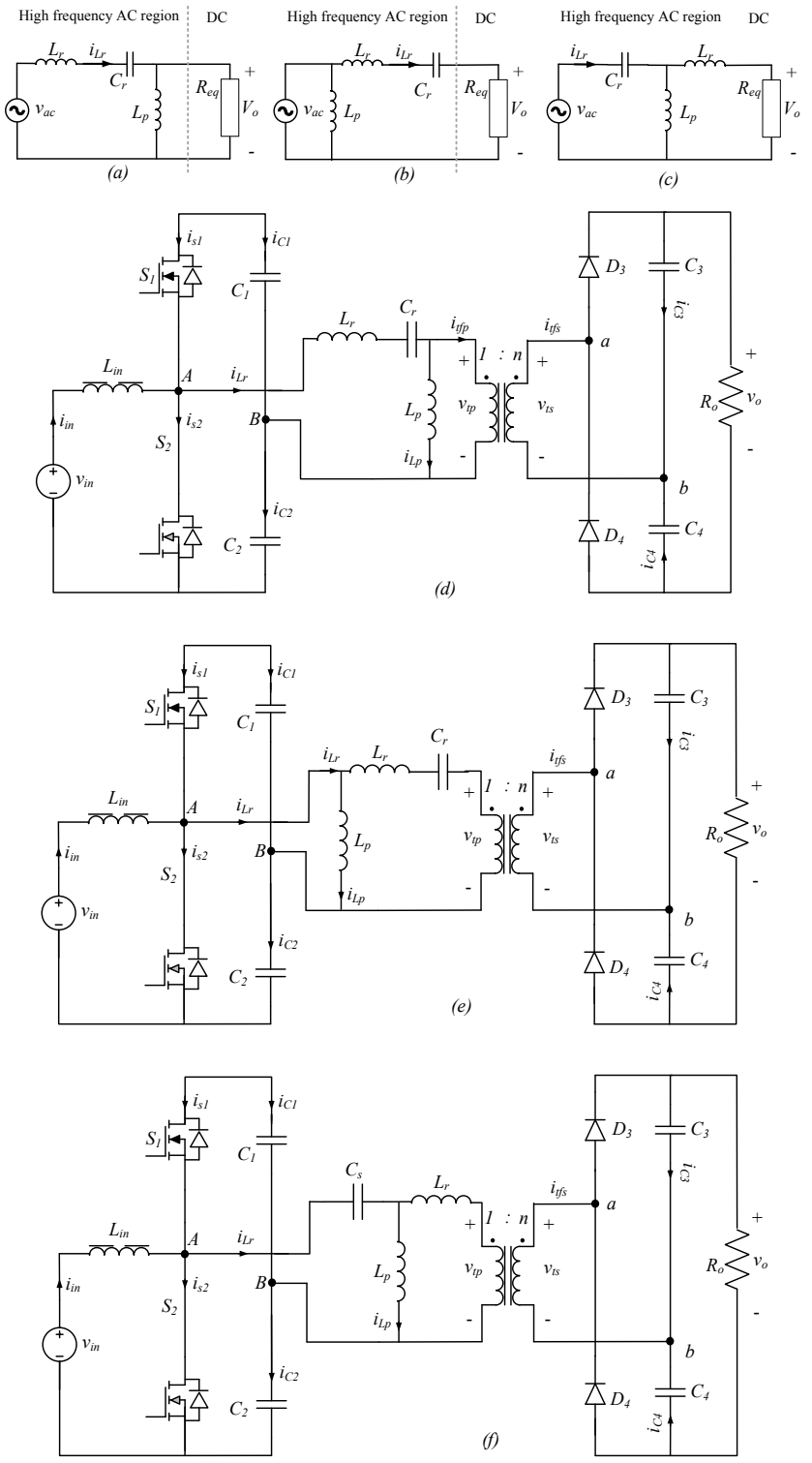


Fig. 6.2. (a) LCL-SRC resonant tank; (b) (L)(LC)-SRC resonant tank; (c) (C)(L)(L)-SRC resonant tank; (d) LCL-SRC high voltage gain resonant converter; (e) (L)(LC)-SRC high voltage gain resonant converter; (f) (C)(L)(L)-SRC high voltage gain resonant converter;

the alternating voltage across L_p is enough to contain sufficient resonant energy in the tank irrespective of the load current and input voltage to bring soft-switching. However, due to proximity between L_p and DC link capacitors, low-frequency ripple current is developed in L_p and later superimposes on DC link capacitors. This effect grows severe as the load current falls. Further, this low ripple frequency component flows through the switches, resonant tank, input and output capacitors, and the transformer. Switch with super-imposed low-frequency ripple currents periodically loses soft-switching defeating the original purpose of introducing L_p, which is to maintain soft-switching at light load. Therefore, (L)(LC)-SRC resonant high voltage gain DC/DC converter is not a feasible idea for application under study.

Lastly, the external parallel inductor (L_p) is connected as shown in Fig. 6.2 (c) to form (C)(L)(L)-SRC resonant tank and the converter with this tank is shown in Fig. 6.2 (f). Parallel resonant inductor L_p in this converter is subjected to sinusoidal voltage and the generated current is enough to contain sufficient resonant energy in the tank irrespective of load demand and available input voltage to bring soft-switching. Further, with the help of equivalent resonance circuits presented in the literature, it is observed that (C)(L)(L)-SRC resonant tank and LCL-SRC resonant tanks are equivalent in their operation. Therefore, LCL-SRC resonant high voltage gain DC/DC converter and (C)(L)(L)-SRC resonant high voltage gain DC/DC converters are equivalent in their performance and only the LCL-SRC resonant high voltage gain DC/DC converter is studied and analyzed in this Chapter. (C)(L)(L)-SRC resonant high voltage gain DC/DC converter components are determined using equivalent resonant circuits principles.

6.3 Operation of proposed high voltage gain DC/DC converter

To analyze the proposed converter, this Chapter adopts Fundamental Harmonic Approximation (FHA) analysis to ease the analysis and design of the converter without loss of generality and accuracy. The FHA analysis technique is widely accepted in the area of resonant converters for approximate analysis [21]-[23] as presented in Chapter 2.

In this section, the operation of the LCL-SRC resonant converter for one complete high switching frequency cycle is delineated. Based on the operating wavefoRMS as shown in Fig. 6.3,

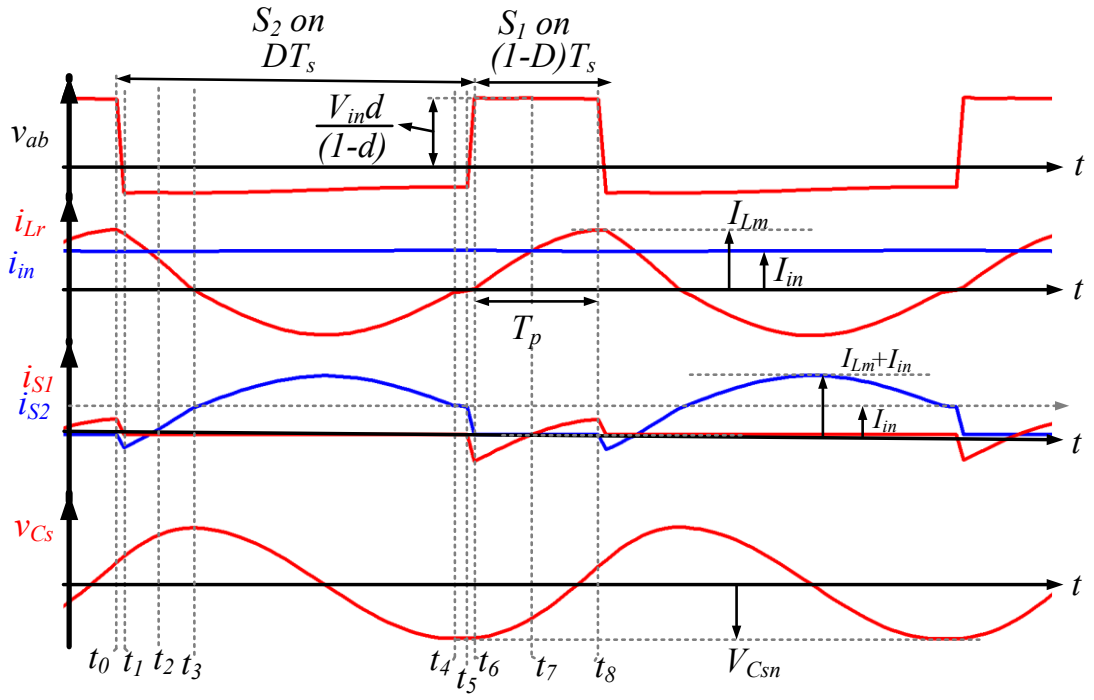


Fig. 6.3. Operating wave foRMS of proposed converter

a high switching frequency cycle is segregated into eight intervals. All the components during the analysis of the converter are considered ideal. Due to the fundamental nature of the switching element, the ripple appears in input current and output voltage. It is assumed during the analysis input inductor and output capacitor are large enough to suppress the switching ripple.

6.3.1 Mode 1 ($t_o<t<t_1$) Fig. 6.4 (a):

During this mode, both switches S_1, and S_2 remain in an off state, and a combination of input current and resonant current charges the device capacitance of S_1 and discharges the device capacitance of S_2, assuming enough dead time. This allows S_2 to turn-on with ZVS.

6.3.2 Mode 2 ($t_1<t<t_2$) Fig. 6.4 (b):

This mode begins as the bottom switch S_2 turns on. Resonant current dominates input current during this mode. Therefore, S_2 carries a negative current. Further, a positive resonant current on the transformer secondary allows D_1 to conduct. This charges output capacitor C_3 and

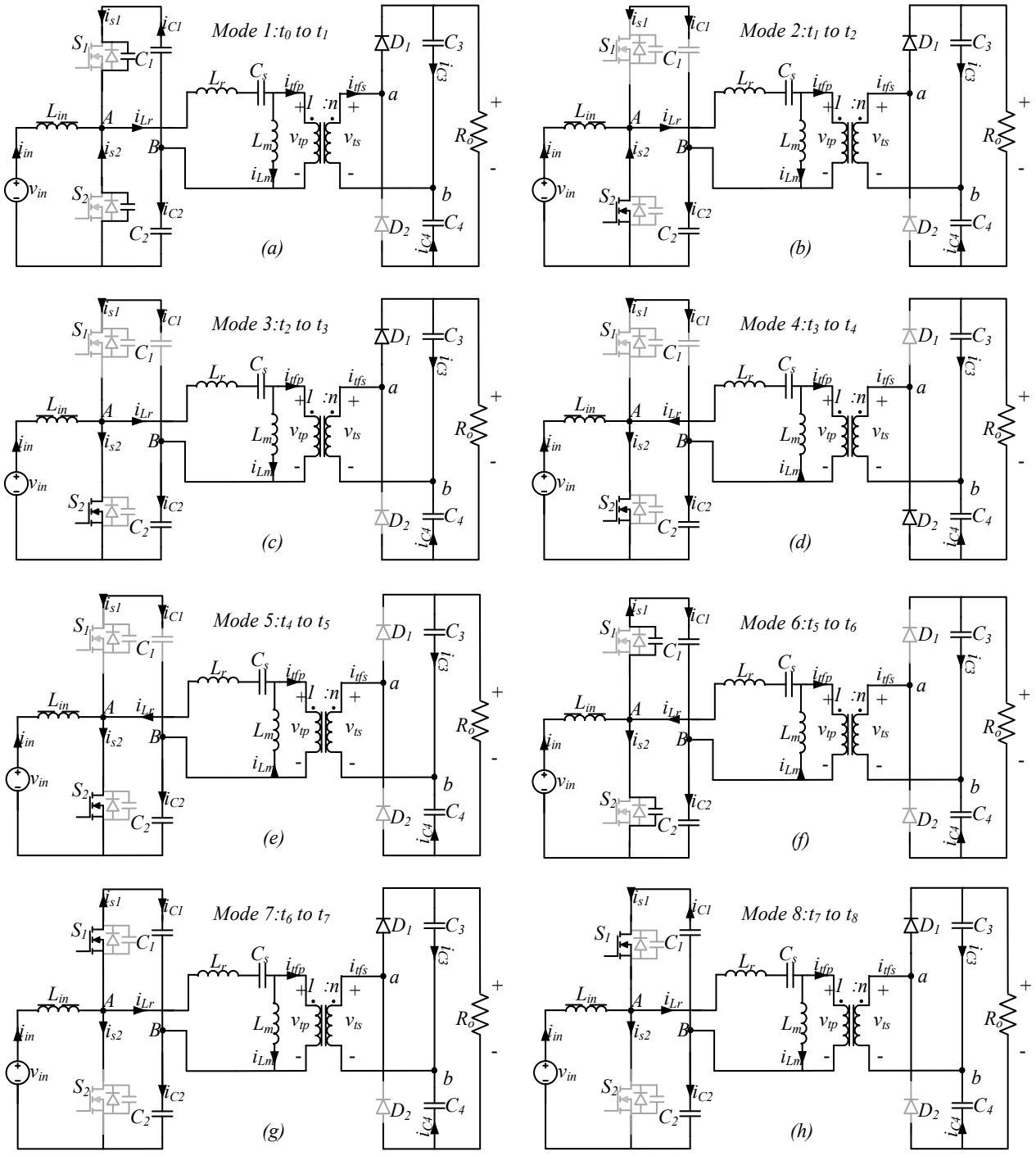


Fig. 6.4. Equivalent circuits of proposed converter while operating in various modes

discharges C_4. The equivalent circuit for this mode is given in Fig. 6.4 (a). The resonant tank is subjected to negative voltage through the bottom capacitor C_2. Therefore, the resonant current falls drops gradually to the input current at the end of this mode.

6.3.3 Mode 3 ($t_2<t<t_3$) Fig. 6.4(c):

Resonant current continues to fall but due to constant input current through switch S_2 turns positive. The resonant current expression for the previous mode continues to hold. This mode continues till the resonant current reaches zero and diode D_1 stops conducting.

6.3.4 Mode 4 ($t_3<t<t_4$) Fig. 6.4(d):

The negative voltage across capacitor C_2 voltage forces the resonant current to fall beyond zero, i.e., negative. Negative resonant current allows D_2 to conduct on the secondary side. The current in S_2 continues to increase and reaches a peak and then falls.

6.3.5 Mode 5($t_4<t<t_5$) Fig. 6.4 (e):

Resonant current reaches zero and S_2 carries only input current. At the end of this mode, S_2 turns off with current equal to the input current. Neither of the diodes on secondary conduct during this mode. Further, this mode is very short in duration.

6.3.6 Mode 6 ($t_5<t<t_6$) Fig. 6.4 (f):

During this mode, both the switches are turned off and a combination of input current and resonant tank current charges and discharges S_2 and S_1 device capacitances, respectively.

6.3.7 Mode 7 ($t_6<t<t_7$) Fig. 6.4(g):

Switch S_1 turns on and the positive capacitor voltage C_1 appears across the resonant tank. This allows the resonant current to rise from zero. Therefore, the input current dominates the resonant current in this mode forcing switch S_1 to carry a negative current. Positive resonant current

allows D_1 to conduct on the secondary side. The equivalent circuit for this mode is given by Fig. 6.4(d) and the current flowing through the resonant inductor is given as follows. Capacitor voltage C_1 makes resonant current gradually raise to input current by the end of this mode.

6.3.8 Mode 8 ($t_7<t<t_8$) Fig. 6.4(h):

The resonant current rises above the input current value during this mode making the switch S_1 carry a positive current. Diode D_1 on the secondary side continues to conduct. Equations of the previous mode continue to hold well in this mode.

6.4 Analysis of Proposed Converter

To analyze a converter, its mathematical model is necessary. It helps to derive the component's rating, design equations as well as in loss and efficiency analysis/calculation to predict the performance theoretically/analytically.

6.4.1 Modeling of the proposed converter

A mathematical model would be handy every time to crosscheck the impact of variations of one parameter on important characteristics of converter such as current stress, conduction losses, regulation capability, power deliverability, and soft-switching ability, etc., To obtain a mathematical model for a resonant converter, Chapter 2 has presented a detailed approach on the

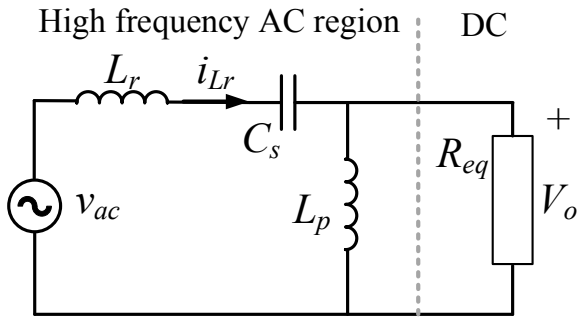


Fig. 6.5. Equivalent circuit of proposed converter

Fundamental Harmonic Approximation (FHA) analysis. According to Chapter 2, front end inverter (FEI) and the transformer along with the rear-end rectifier are replaced with equivalent voltage source and resistance. Unlike a parallel resonant tank based resonant converter, the proposed converter uses a series resonance-based resonance tank, therefore, capacitive filter at the output and current sourcing nature at the input of DBR would easily allow to model it as a resistance. The equivalent circuit of the proposed converter is shown in Fig.6.5, where equivalent voltage (peak) and resistance are given as (6.1) and (6.2), respectively.

6.4.2 Deciphering converter characteristics

Based on the developed mathematical equivalent model of the proposed converter, it is possible to derive various relations such as voltage gain, resonant tank current, switch RMS currents and capacitor RMS currents and voltage stress, etc., This information is essential for the design of the converter.

$$\frac{V_o}{V_{in}} = \frac{2sin(\pi d)}{\pi(1-d)} G_{rtg} n \frac{\pi}{2} \tag{6.3}$$

$$G_{rtg} = \frac{\omega_n^2 L_n}{(\omega_n^2(1+L_n)-1) + j\left(\omega_n L_n z_b n^2 P_o \left(\frac{\pi^2}{2V_o^2}\right)(\omega_n^2-1)\right)} \tag{6.4}$$

6.4.2.1 Voltage gain

As explained in the evolution of the proposed converter in Chapter 2, about the converter operation in stages. Therefore, the overall voltage gain of the converter is the contribution of individual stages. Various identified stages, as shown in Fig.1.7 (a), are FEI, resonant tank, transformer, and voltage doubler. The voltage gain of FEI (6.1), is dependent on the duty ratio of the converter while the voltage gain of the transformer and voltage doubler is constant. On the other hand, the voltage gain offered by the resonant tank is attenuating in nature and is dependent on the load current drawn at that instant. This is the basic characteristic of a load resonant converter. The overall voltage gain of the converter is given by (6.3) and (6.4) where G_{rtg} is gain of the resonant tank, n is transformer turns ratio, L_n ratio of parallel to the series resonant inductor,

$$I_{Lr} = \frac{2sin(\pi d)}{\sqrt{2}\pi(1-d)} \frac{1}{z_{rtg}} \tag{6.5}$$

$$z_{rtg} = jz_b \left[\frac{(\omega_n^2(1+L_n)-1) + j\left(\omega_n L_n z_b n^2 P_o \left(\frac{\pi^2}{2V_o^2}\right)(\omega_n^2-1)\right)}{\omega_n \left(j\omega_n L_n z_b n^2 P_o \left(\frac{\pi^2}{2V_o^2}\right)+1\right)} \right] \tag{6.6}$$

ω_n=ratio of switching frequency to series resonance frequency, z_r is series resonance characteristic impedance.

$$i_{C1} = \begin{cases} i_{Lr} - i_{in}, & 0 < t < (1-d)T_s \\ 0, & (1-d)T_s < t < T_s \end{cases} \tag{6.7}$$

$$I_{C1}^2 = \frac{1}{T_s} \int_0^{(1-d)T_s} [I_{Lr} \sin \omega_s (t-(1-d)T_s) - I_{in}]^2 dt + \frac{1}{T_s} \int_{(1-d)T_s}^{T_s} 0 \, dt \tag{6.8}$$

$$I_{C1}^2 = I_{in}^2(1-d) + I_{Lr}^2 \left(\left(\frac{1-d}{2}\right) - \frac{1}{8\pi} \sin\big(4\pi(1-d)\big) \right) - \frac{I_{in} I_{Lr}}{\pi} \cos\big(2\pi(1-d)\big) \tag{6.9}$$

$$i_{C2} = \begin{cases} i_{in}, & 0 < t < (1-d)T_s \\ i_{Lr}, & (1-d)T_s < t < T_s \end{cases} \tag{6.10}$$

$$I_{C2}^2 = \frac{1}{T_s} \int_0^{(1-d)T_s} [I_{in}]^2 dt + \frac{1}{T_s} \int_{(1-d)T_s}^{T_s} [I_{Lr} \sin \omega_s (t-(1-d)T_s)]^2 \, dt \tag{6.11}$$

$$I_{C2}^2 = I_{in}^2(1-d) + I_{Lr}^2 \left(\left(\frac{d}{2}\right) - \frac{1}{8\pi} \sin\big(4\pi(1-d)\big) \right) \tag{6.12}$$

6.4.2.2 Resonant tank current

With the periodical switching action of S_1, and S_2 alternatively, the voltage across capacitors C_1, and C_2 appears at the input of the resonant tank as an alternating AC voltage waveform that causes the resonant tank to draw a sinusoidal voltage. Since the proposed resonant tank is based on series resonance, the bandpass characteristic of the resonant tank allows only fundamental harmonic current to flow into the resonant tank. RMS of resonant tank current and per unit characteristic impedance is calculated as (6.5) and (6.6), where z_{rtg} is defined as impedance offered by the resonant tank.

6.4.2.3 Currents through FEI capacitors C_1, C_2.

Top capacitor C_1 carries a current that is a difference of input current and resonant tank current during top switch S_1 is conducting which is given by (6.7) and its RMS current is calculated as (6.8) and is given by (6.9). Similarly, capacitor C_2 carries input current and resonant current

$$V_{C1} + V_{C2} = \frac{V_{in}}{(1-d)} \tag{6.13}$$

$$V_{C1} = V_{C2} = \frac{V_{in}}{2(1-d)} \tag{6.14}$$

alternatively during the conduction period of S_1 and S_2, respectively as given by (6.10). Therefore, RMS current through capacitor C_2 is given by (6.11) and calculated as (6.12).

6.4.2.4 The voltage stress on FEI capacitors C_1, C_2.

The FEI of the converter is derived from a boost converter. Therefore, the voltage stress on capacitors C_1 and C_2 combined are given by (6.13). Since both the capacitors C_1 and C_2 are selected as equal value, the total DC link voltage is shared equally between C_1 and C_2, as given by (6.14).

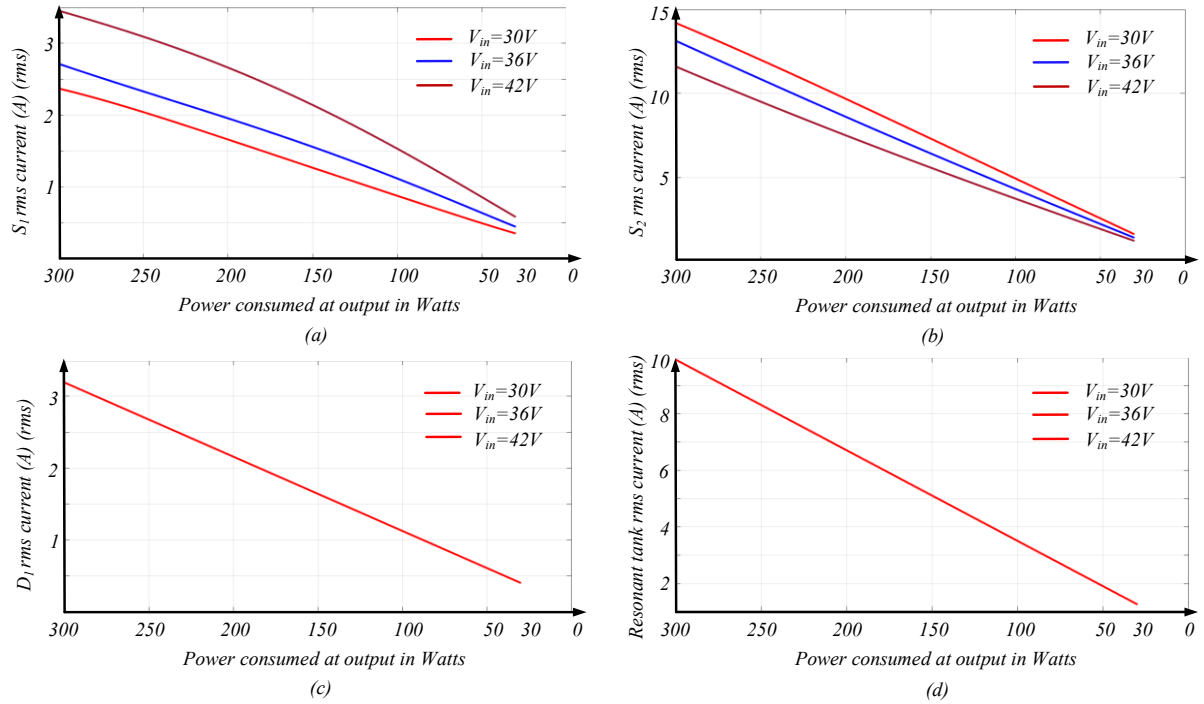


Fig. 6.6. Analysis of current stress on semiconductor devices against input voltages for (a) S_1 (b) S_2 (c) D_1, D_2 (d) I_{Lr}

6.4.2.5 Current and voltage stress on the resonant capacitor (C_r)

As the resonant capacitor is connected in series with the resonant inductor (L_r), the current stress experienced by the resonant capacitor is the same as the resonant current as given by (6.5) and (6.6). Further voltage stress experienced by the resonant capacitor is given by (6.15).

6.4.3 Current and voltage stress analysis on semiconductor devices

The proposed converter employs four semiconductor devices, S_1, S_2 (preferably MOSFETs), and two diodes as shown in Fig. 6.2 (d). In this section, the semiconductor devices (MOSFETs and diodes) relating to its current, voltage stress, and power losses are analyzed

$$V_{Cr} = \frac{I_{Lr}}{\omega_r C_r} \tag{6.15}$$

because the selection of the semiconductor devices is directly influenced by them.

$$V_{S1,S2} = \frac{V_{in}}{(1-d)} \tag{6.16}$$

$$V_{D1,D2} = V_o \tag{6.17}$$

6.4.3.1 The voltage stress on MOSFETs

The magnitude of voltage that must be blocked by the MOSFETs during their forward blocking duration is termed as voltage stress on that device. Further, in practice, to accommodate turn off ringing due to track inductance, a safety margin of 50% above device blocking voltage is considered for selection. The voltage stress on a device majorly has two significant effects on the converter losses and thus efficiency. For a given current rating, a device with a higher voltage rating exhibit a higher on-state resistance (R_{DSon}) and a higher gate charge. Higher R_{DSon} results in higher conduction losses while higher gate charge results in excess energy for switching transitions and limits maximum achievable operating switching frequency.

Unlike the voltage-fed converter, the current-fed converters are derived from the fundamental boost converter. Therefore, the devices in the case of the current-fed converters see higher voltage stress than any voltage-fed converter for the same input voltage rating. Therefore, in the case of the current fed converters, it is important to consider the effect of the voltage rating of the device. Based on the boost converter operation, voltage stress across the switches S_1 and S_2 is given by (6.16), which depends on input voltage and operating duty ratio. The maximum voltage stress on the switch occurs at maximum duty ratio operation which is needed under minimum input voltage condition.

6.4.3.2 Current stress on MOSFETs

Another major parameter in the selection of MOSFET is its current rating. As observed from the previous sub-section, the voltage rating of the device limits losses in the converter. On the other hand, the current rating of the device quantifies the ability of the device to carry current within the specified temperature limits. Unlike voltage stress, which is equal to the maximum

$$i_{S1} = \begin{cases} i_{Lr} - i_{in}, & 0 < t < (1-d)T_s \\ 0, & (1-d)T_s < t < T_s \end{cases} \tag{6.18}$$

$$I_{S1}^2 = \frac{1}{T_s} \int_0^{(1-d)T_s} [I_{Lr} \sin \omega_s (t - (1-d)T_s) - I_{in}]^2 dt + \frac{1}{T_s} \int_{(1-d)T_s}^{T_s} 0 \, dt \tag{6.19}$$

$$I_{S1}^2 = I_{in}^2(1-d) + I_{Lr}^2 \left(\left(\frac{1-d}{2} \right) - \frac{1}{8\pi} \sin\big(4\pi(1-d)\big) \right) - \frac{I_{in} I_{Lr}}{\pi} \cos\big(2\pi(1-d)\big) \tag{6.20}$$

$$i_{S2} = \begin{cases} 0, & 0 < t < (1-d)T_s \\ i_{in} - i_{Lr}, & (1-d)T_s < t < T_s \end{cases} \tag{6.21}$$

$$I_{S2}^2 = \frac{1}{T_s} \int_0^{(1-d)T_s} 0 \, dt + \frac{1}{T_s} \int_{(1-d)T_s}^{T_s} [I_{in} - I_{Lr} \sin \omega_s (t - (1-d)T_s)]^2 \, dt \tag{6.22}$$

$$I_{S2}^2 = I_{in}^2(d) + I_{Lr}^2 \left(\left(\frac{d}{2} \right) - \frac{1}{8\pi} \sin\big(4\pi(1-d)\big) \right) - \frac{I_{in} I_{Lr}}{\pi} (1 - \cos(2\pi d)) \tag{6.23}$$

$$i_{D1} = \begin{cases} \frac{i_{Lr}}{n}, & 0 < t < \frac{T_s}{2} \\ 0, & \frac{T_s}{2} < t < T_s \end{cases} \tag{6.24}$$

$$I_{D1,D2} = \frac{I_{Lr}}{2n} \tag{6.25}$$

voltage seen by the switch, the current rating is defined by RMS current passing through the switch instead of the peak current seen by the switch.

According to modes of operation, auxiliary switch S_1 conducts the difference of the input and resonant currents as given by (6.18) and its RMS is current is given by (6.19) and calculated as (6.20). Similarly, while the main switch S_2 conducts a combination of input and resonant current when it is on as given by (6.21) and its RMS is current is given by (6.22) and calculated as (6.23). On the other hand, voltage doubler diodes D_1 and D_2 conduct positive and negative half cycles of

resonant current respectively (6.24). Therefore, RMS current of D_1 and D_2 is supposed to equal, which is given by (6.25).

Based on the ratings of the converter proposed in Chapter 3, the current stress experienced by the MOSFETs and the diodes with respect to the power delivered and input voltage fluctuations for the proposed converter are shown in Fig.6.6. The following conclusions can be made from the analysis.

Variation in the input voltage affects the change in both the switches differently. Higher input voltage operation demands reduced duty ratio operation to load voltage. Since the main switch, S_2, carries a combination of input current and resonant tank current equivalent for duty ratio duration, higher input voltage results in reduced current stress as shown in Fig, 6.6 (a). On the other hand, auxiliary switch (S_1) conduction time increases with the reduction in duty ratio at higher input voltage. Therefore, higher input voltage results in higher current stress on the auxiliary switch (S_1) as shown in Fig, 6.6 (b). Also, from Fig. 6.6, it should be observed that the lower switch is subjected to higher current stress than the upper switch. It is evident from the operation of the converter. Further, a significant reduction in the switch current with respect to the power delivered is a result of a series resonance tank whose current is shown in Fig. 6.6 (d).

The current stress in the diodes is unaffected with the input voltage variation, as shown in Fig. 6.6(c). This is because load voltage is regulated to 380V despite input voltage fluctuations.

6.4.3.3 Power loss in MOSFETs

Due to turn on-state resistance, the current carried by the semiconductor devices results in conduction losses. Conduction losses of the semiconductor devices are presented in Fig.6.7. It should be observed that the major portion of the conduction of the semiconductor devices is contributed by the lower switch alone irrespective of the input voltage, as shown in Fig. 6.7 (a). Further, with an increase in input voltage, total power losses in semiconductor devices, and lower switches are decreased, Fig. 6.7 (a), (d), respectively. On the other hand, the input voltage does not affect secondary diode power losses, Fig. 6.7 (c). Further, a steep reduction in power losses in

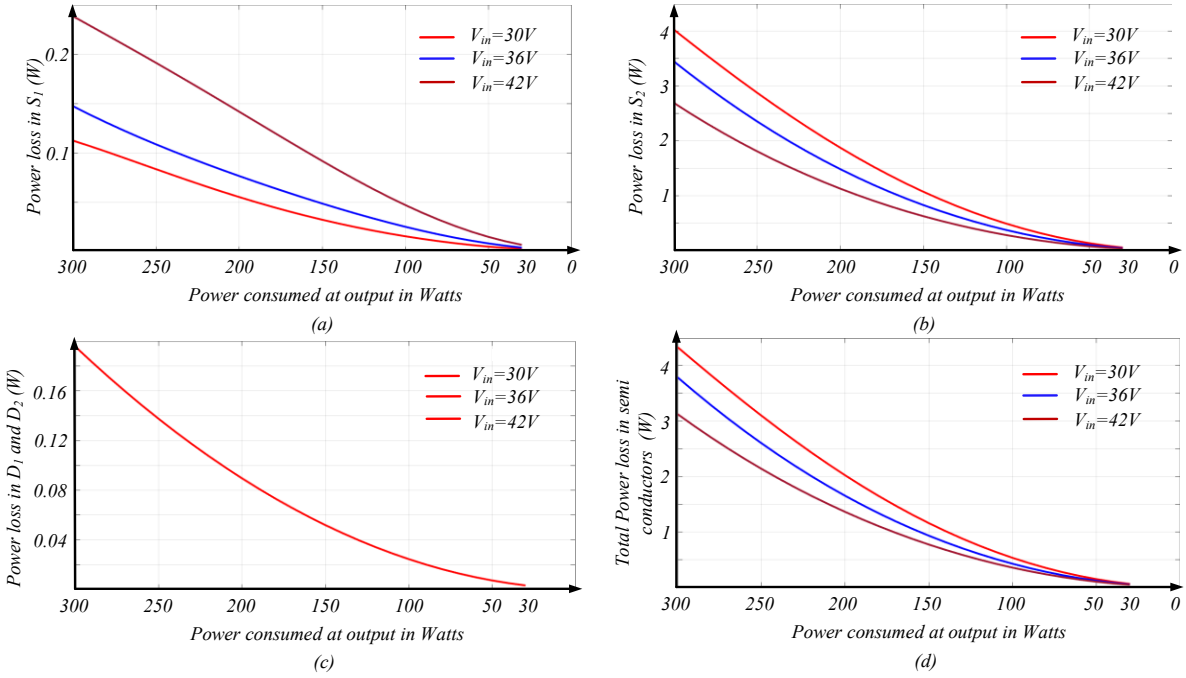


Fig. 6.7. Analysis of power loss in semiconductor devices against input voltages for (a) S_1 (b) S_2 (c) D_1, D_2 (d) Total power loss in semiconductor devices.

response to the reduction in power delivered is possible only due to the inclusion of a series resonance-based LLC resonant tank, as shown in Fig. 6.7 (a), (b), (d).

6.5 Design of the proposed converter

The proposed converter is intended to serve an application, as mentioned in Chapter 1, with a need for a high voltage gain dc/dc converter whose requirements are the same as the converter studied in Chapters 3, and 4. The design of the converter includes the selection of components to maintain the desired voltage gain, regulate voltage delivered, suppress fluctuations in input voltage, and maintain soft-switching against all disturbances from the input and output side.

Depending on (6.1) to (6.25), it can be concluded that the parameters such as transformer the turns ratio (n), relative switching frequency (f_n), series resonance characteristic impedance (z_r), inductance ratio (L_n), and operating duty ratio are to be calculated to fulfill desired objectives.

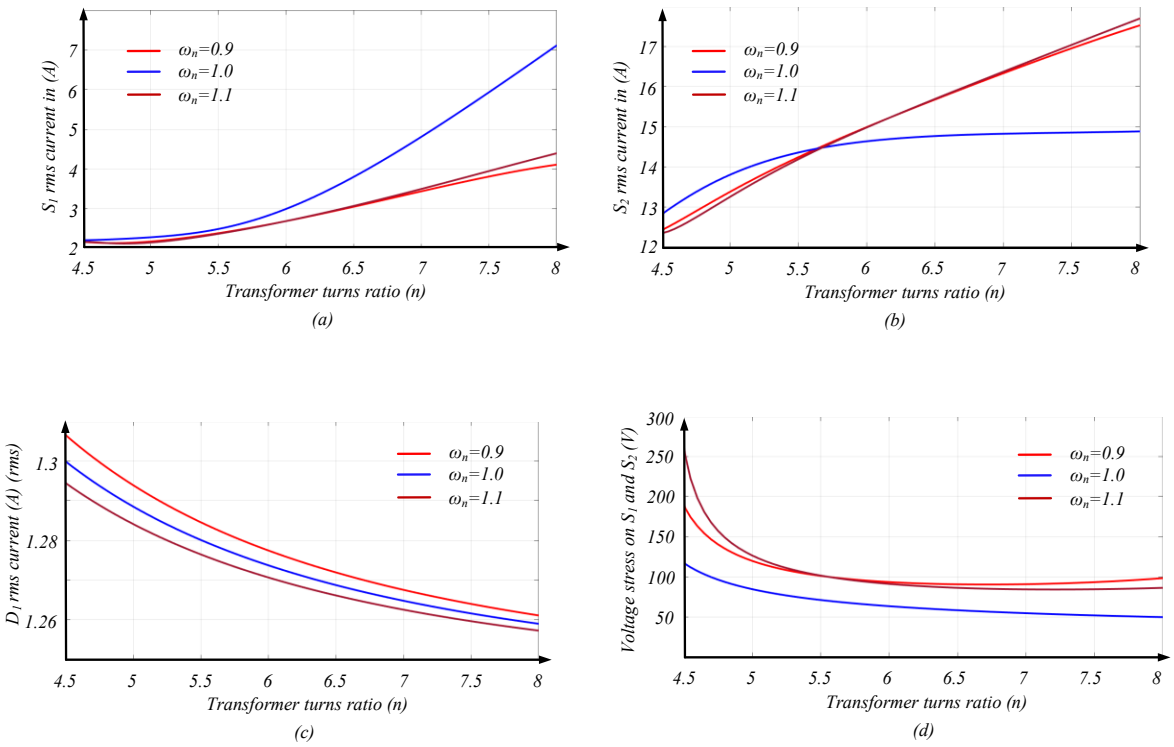


Fig. 6.8. Impact of selection of transformer turn ratio on current stress for (a) S_1 (b) S_2 (c) D_1, D_2 and (d) voltage stress in S_1, S_2.

6.5.1 Selection of the transformer turns ratio *(n)* and relative switching frequency (ω_n).

A High-frequency transformer plays a major role in the converter operation. Functions of the high-frequency transformer as follows.

1. Contributes to the overall voltage gain of the converter.
2. Offers energy stored in the leakage inductance to maintain soft-switching.
3. Assures safety to the user by isolating the load end from the source.

The high-frequency operation helps to reduce the size, weight, and volume of the converter. The small size of the transformer also means shorter magnetic paths and so the low magnetic losses.

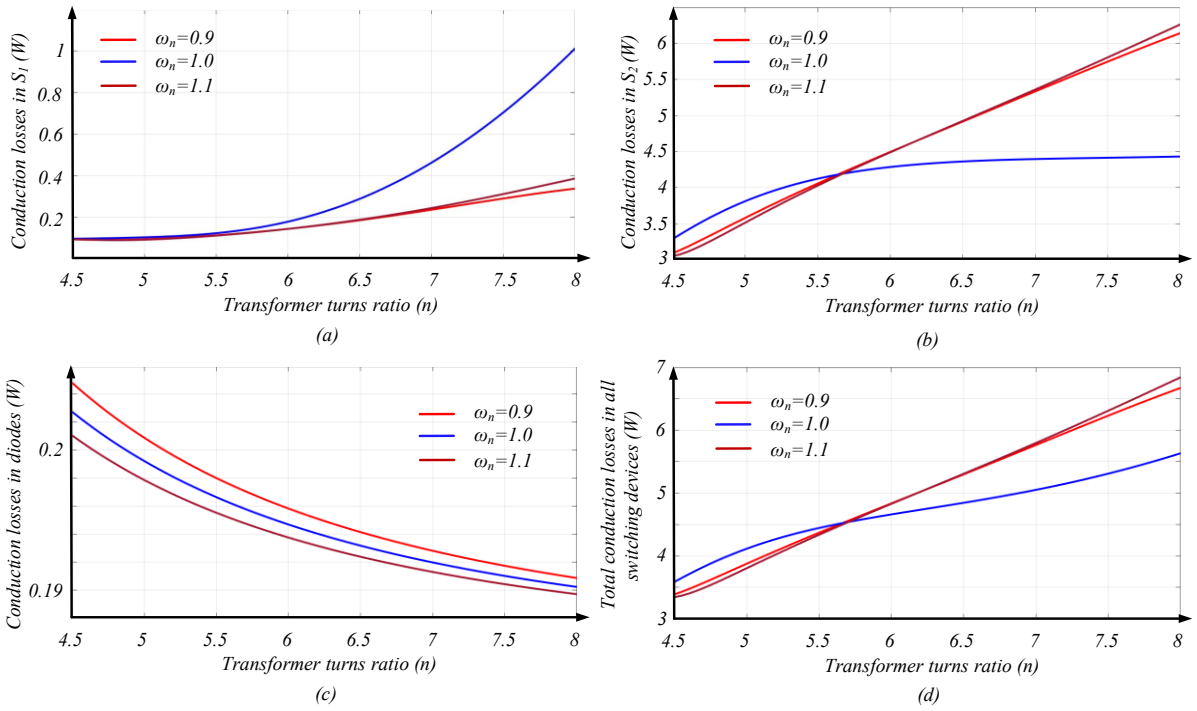


Fig. 6.9. Impact of selection of transformer turn ratio on power losses for (a) S_1 (b) S_2 (c) D_1 and D_2 and (d) total power losses in S_1, S_2, D_1 and D_2.

In the case of the resonant converters, as evident from the relations (6.1) to (6.25), all converter parameters are interdependent with each other, and variation in one parameter would affect the desired operation of the converter. Therefore, the effect of the transformer turns ratio on all other parameters is studied and also presented in Fig. 6.8, Fig. 6.9 and Fig. 6.10, under the maximum stressful condition of the converter that is minimum input voltage and rated load.

6.5.1.1 Impact on semiconductor devices

The MOSFETs conduct a combination of the input current and the resonant tank current, which is also a reflection of the load current via the transformer turns ratio. A further gain of the resonant tank is also susceptible to the load current. Since current and voltage stress on MOSFETs play an important role in their selection as well as on the efficiency and thermal stability of the converter, it is important to study the effect of the transformer turns ratio. Fig. 6.8 presents the impact of the selection of the transformer turns ratio on the semiconductor devices.

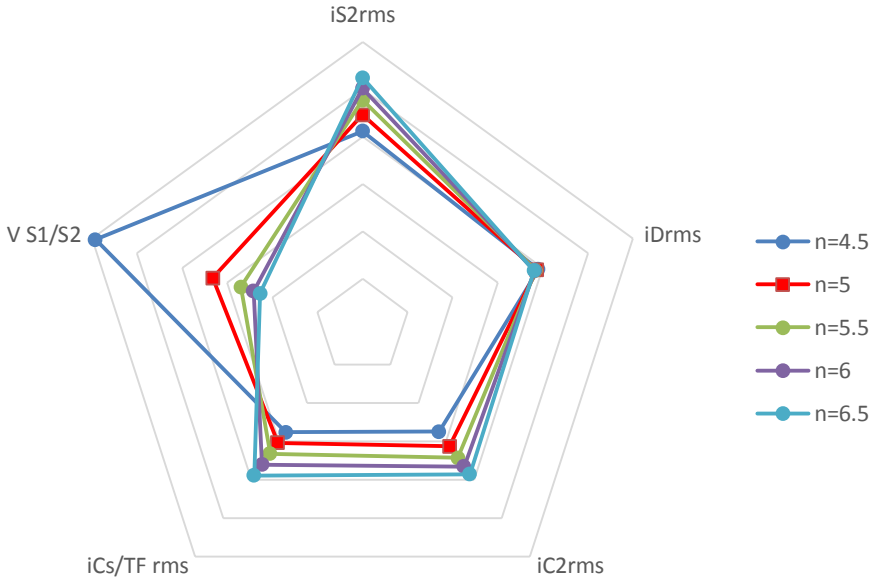


Fig. 6.10. Impact of the selection of transformer turns ratio

1. Current stress on switch S_1 increases with a higher transformer turns ratio as shown in Fig. 6.8 (a). The rate of rise of current stress on S_1 is slower for the turns ratio below 6. For turns ratio above 6, operating at series resonant frequency highly affect S_1 current stress than operating at either above or below the series resonant frequency.
2. Current stress on switch S_2 also increases with a higher transformer turns ratio, as shown in Fig. 6.8 (b). The operating converter at resonant frequency offers minimum stress on the main switch S_2 at a cost of higher turns ratio in the transformer.

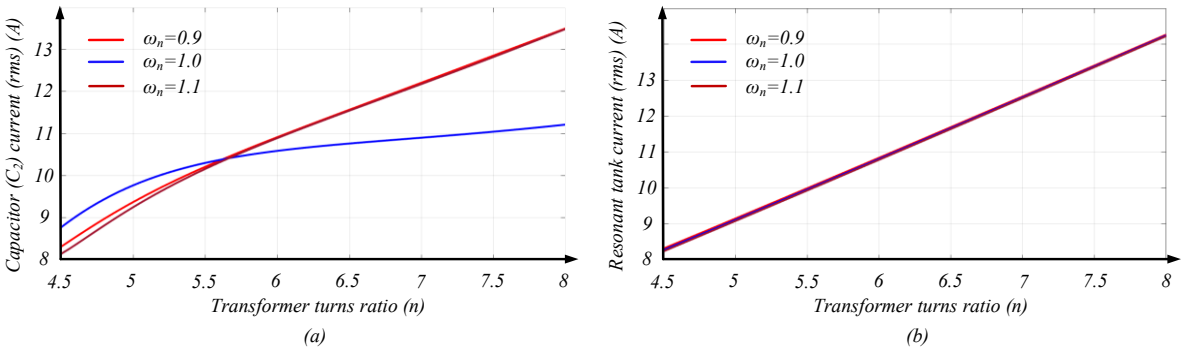


Fig. 6.11. Impact of selection of transformer turn ratio on currents tress of (a) C_2 (b) I_{Lr}

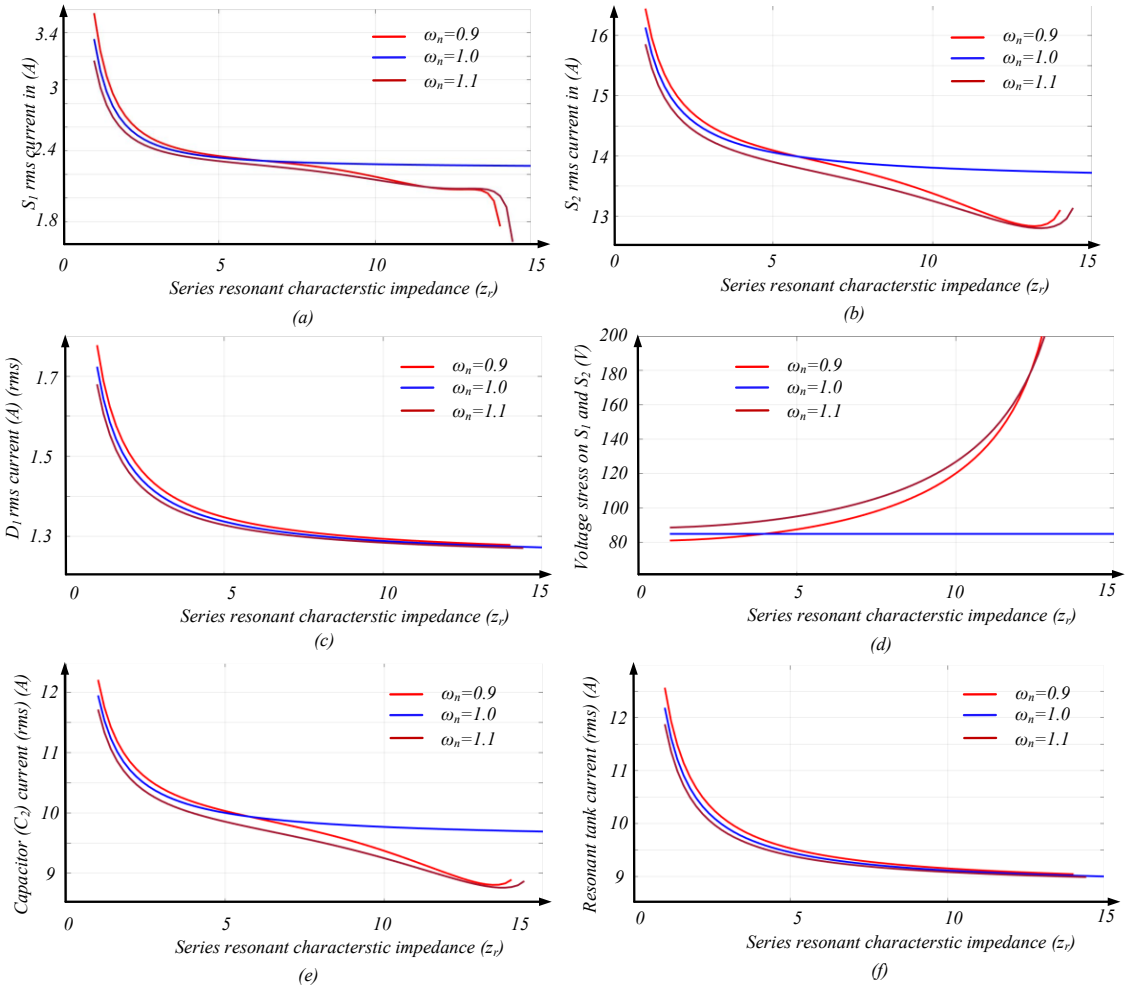


Fig. 6.12. Impact of selection of z_r on current stress and voltage stress of various components.

Alternatively, minimum current stress in switch S_2 can also be obtained by operating at the above series resonance with the minimum number of the turns ratio.

3. Diode current stress reduces with higher transfer turns ratio, as shown in Fig. 6.8 (c). This is also evident from (6.25), where diode current stress is inversely proportional to n.
4. Voltage stress across the MOSFETs have an inverse relation with the turns ratio of the transformer, as shown in Fig. 6.8 (d) and front-end inverter share converter gain to be achieved.

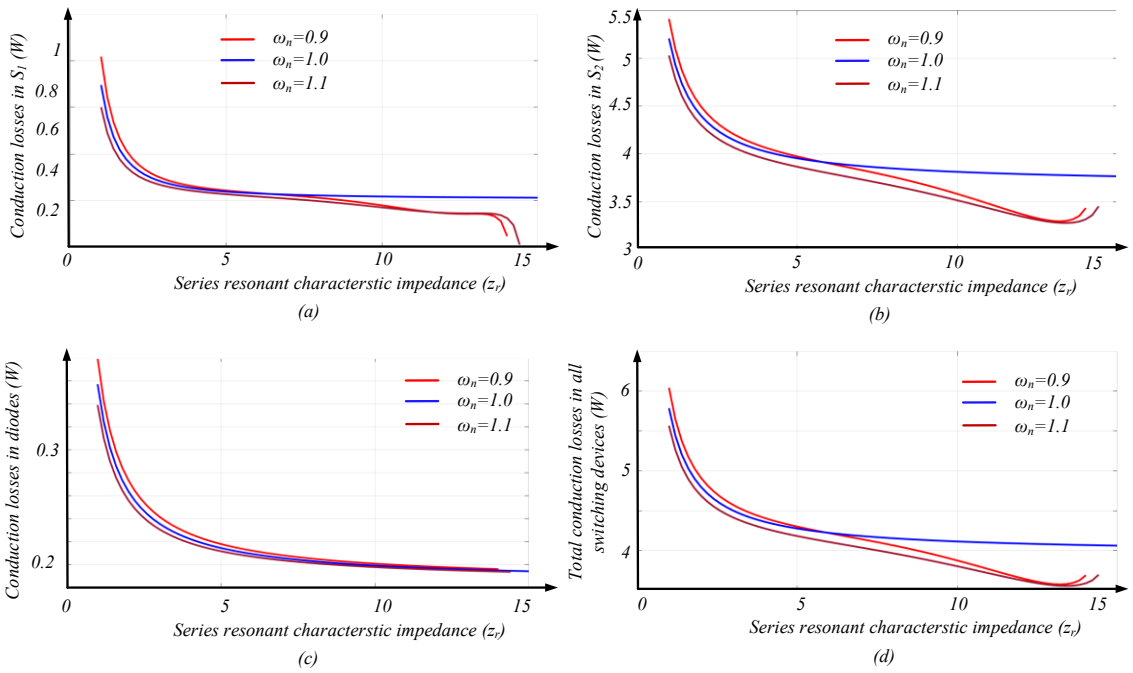


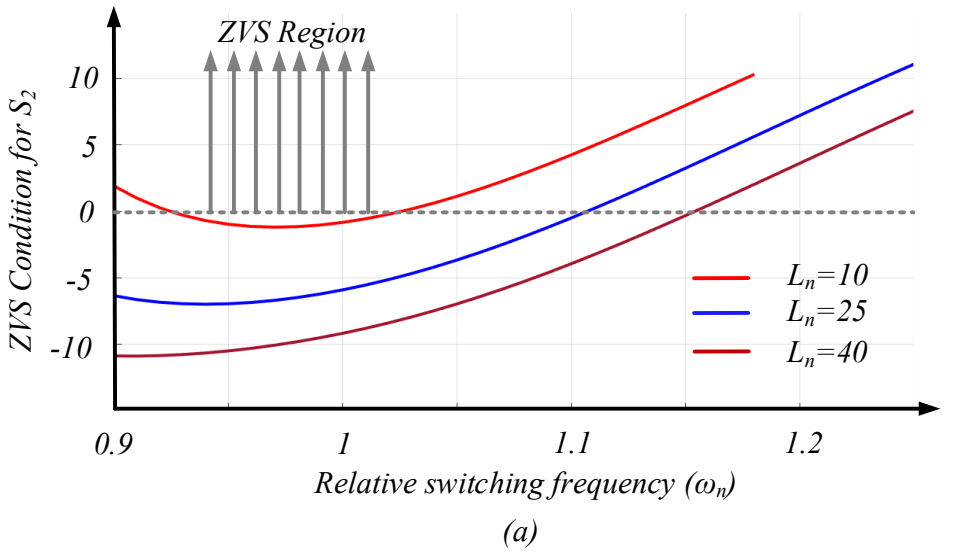
Fig. 6.13. Impact of selection of z_r on semiconductor devices power losses

From the above discussion, it is evident that the selection of turns ratio impact is indirectly seen in device power loss via current stress and voltage stress levels of semiconductor devices. Therefore, the variation in power losses in the semiconductor devices is studied under Fig. 6.9, to have a clear vision of the total losses in the converter. Power losses in the semiconductor devices show the same trend as their current stress. But combined power losses, as shown in Fig. 6.9 (d), conclude that bottom switch S_2 dominates total power losses. Therefore, operating converter above series resonant frequency with lower turns ratio helps to achieve minimum losses in the converter.

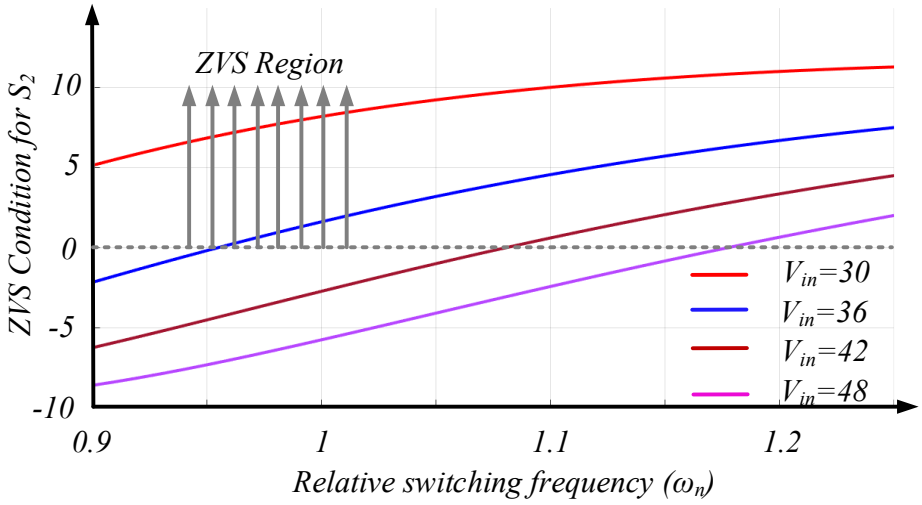
$$\frac{V_{in}}{z_r(1-d)}\sin\left(\frac{2\pi(1-d)}{\omega_n}\right)+\frac{\pi V_o}{4L_n\omega_n z_r n} > I_{in} \tag{6.26}$$

$$z_r < \frac{1}{I_{in}}\left[\frac{V_{in}}{z_r(1-d)}\sin\left(\frac{2\pi(1-d)}{\omega_n}\right)+\frac{\pi V_o}{4L_n\omega_n z_r n}\right] \tag{6.27}$$

$$z_r < \frac{1}{I_{in}}\left[\frac{V_{in}}{z_r(1-d)}\sin\left(\frac{2\pi(1-d)}{\omega_n}\right)\right] \tag{6.28}$$



(a)



(b)

Fig. 6.14. (a) Selection of Ln to maintain ZVS in converter (b) maximum input voltage variations can be sustained keeping ZVS of converter intact.

6.5.1.2 Impact on other components.

Turns ratio selection does not show a significant impact on some passive components such as input inductor and output capacitors as they are directly influenced by input and output conditions. But the selection of turns ratio has a significant impact on the DC link capacitors C_1 and C_2. Since C_1 and S_1 are connected in series, Fig. 6.8 (a) reveals the pattern of current stress on C_1. But Fig. 6.10 (a) shows that the capacitor C_2 would be suffering higher current stress unless the converter is operated with minimum turns ratio and above the series resonant frequency.

The influence of the impact of the turns ratio on all the components is summarized in a radar chart as shown in Fig. 6.11. This shows that the lower turns ratio imposes severe stress on MOSFETs while higher turns ratio subjects the MOSFETs to sever current stress. Therefore, a compromising value between high and low turns ratio such as 5.5 is selected to maintain acceptable current and voltage stress in the MOSFETs and other components. Further, operating converter above resonant

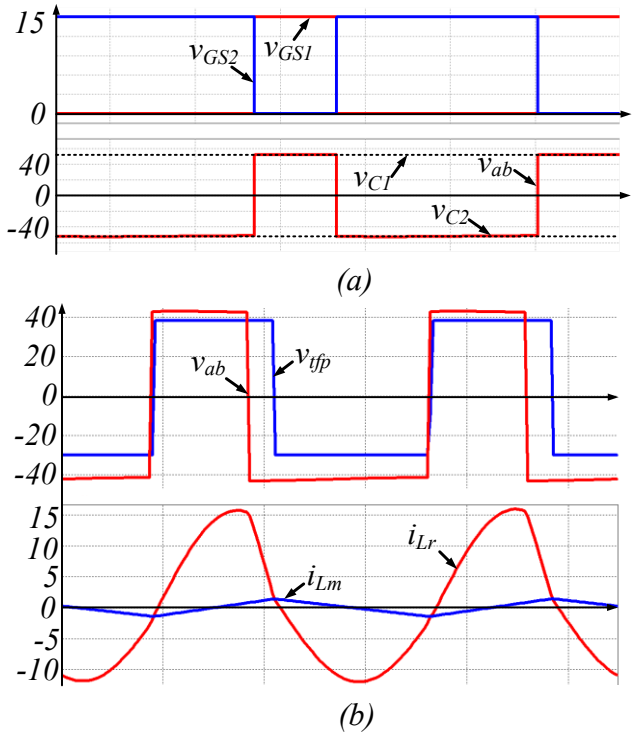


Fig. 6.15. (a) Switching gate pulses are resultant inverter output voltage (b) Resonant tank current generated as a result of inverter output voltage and transformer input voltage.

$$L_r = \frac{z_r}{\omega_n} \tag{6.29}$$

$$C_r = \frac{1}{z_r \omega_n} \tag{6.30}$$

$$L_p = L_n L_r \tag{6.31}$$

frequency offers minimum current stress on the MOSFETs. Therefore, relative switching frequency (ω_n) is selected as 1.1.

6.5.2 Selection of series resonant characteristic impedance (z_r)

The proposed converter employs a resonant tank based on the series resonance formed by the components L_r and C_r as shown in Fig. 6.2. An external parallel inductor (L_p) is included to extend the soft-switching range of the converter until the light load condition. The transformer turns ratio and the relative switching frequency is selected in the previous section, this section studies impact of the selection of z_r on converter components.

Characteristic impedance z_r decides the generated resonant current in the converter when the resonant tank is subjected to the alternating voltage provided by the capacitors C_1 and C_2 alternatively. It is evident from Fig 6.12 that higher values of z_r in the converter suppresses the resonant current. Since MOSFETs S_1 and S_2 carry a combination of the input and the resonant tank current, in order to maintain the current and the voltage stress, the effect of the characteristic impedance (z_r) on the MOSFETs and consequent power losses are presented in Fig. 6.13. Also, Fig 6.12 provides the relation between current stress on the DC link capacitor against z_r.

Fig. 6.12 (a), and (b) show that the current stress through the switches S_1 and S_2 is reduced with a higher value of z_r. This is so because, with the higher value of z_r, the resonant tank current reduces, as shown in Fig 6.12 (f), thus the switch currents through S_1, S_2 are also decreased. Consequently, the voltage stress across the switches increases as shown in Fig., 6.12 (d). Further, it is seen that from Fig 6.12, with the reduction in the resonant current, the current stress through the dc-link capacitor C_2, and secondary diodes are also reduced.

Observation from Fig 6.13 suggested an abstract idea about the selection of z_r, i.e., higher z_r supports minimum current stress in MOSFETs, diodes, and dc-link capacitors and minimum power loss in the semiconductor devices as shown in Fig.6.13. But a concrete conclusion on the selection of z_r is obtained by studying ZVS requirements of the converter.

The ZVS condition is given by (6.26), which on rearranging and approximating leads to the maximum limit on selection of z_r, by (6.27) and (6.28). Therefore, the selected value of z_r is concluded at z_r=9.

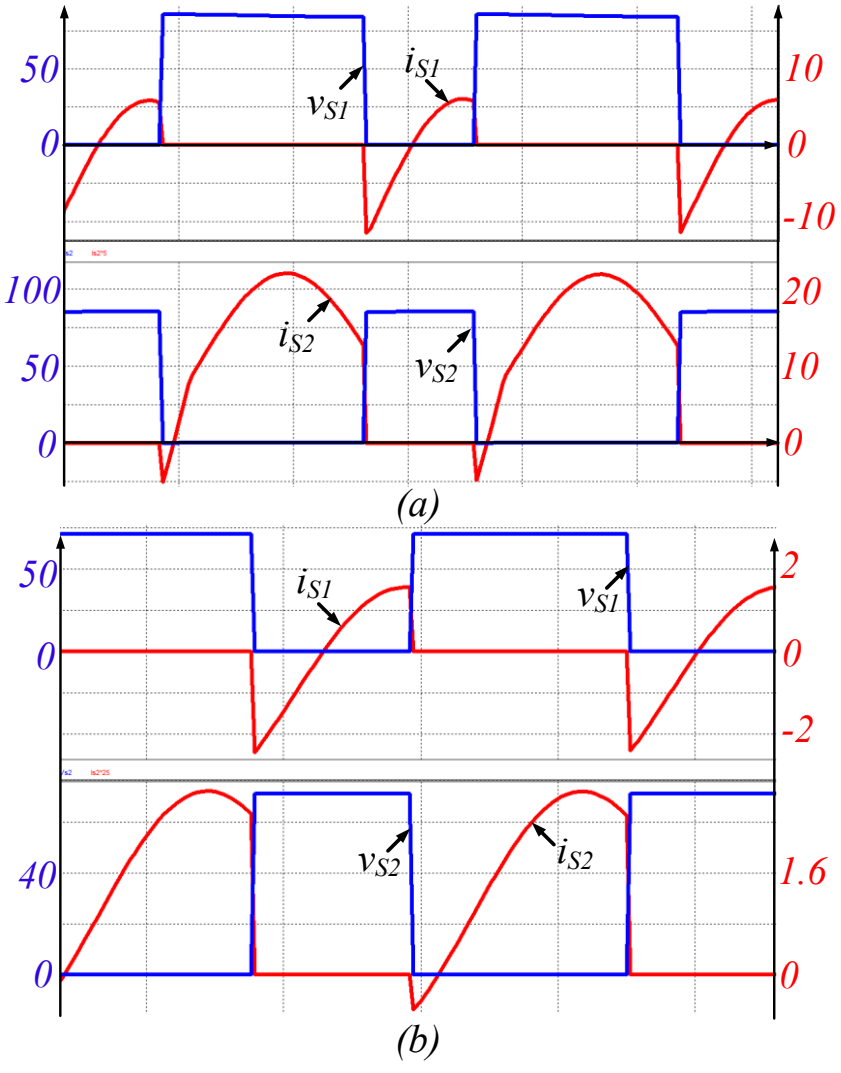


Fig. 6.16. Soft-switching of switches under (a) full load conditions and (b) light load conditions under minimum input voltage availability conditions.

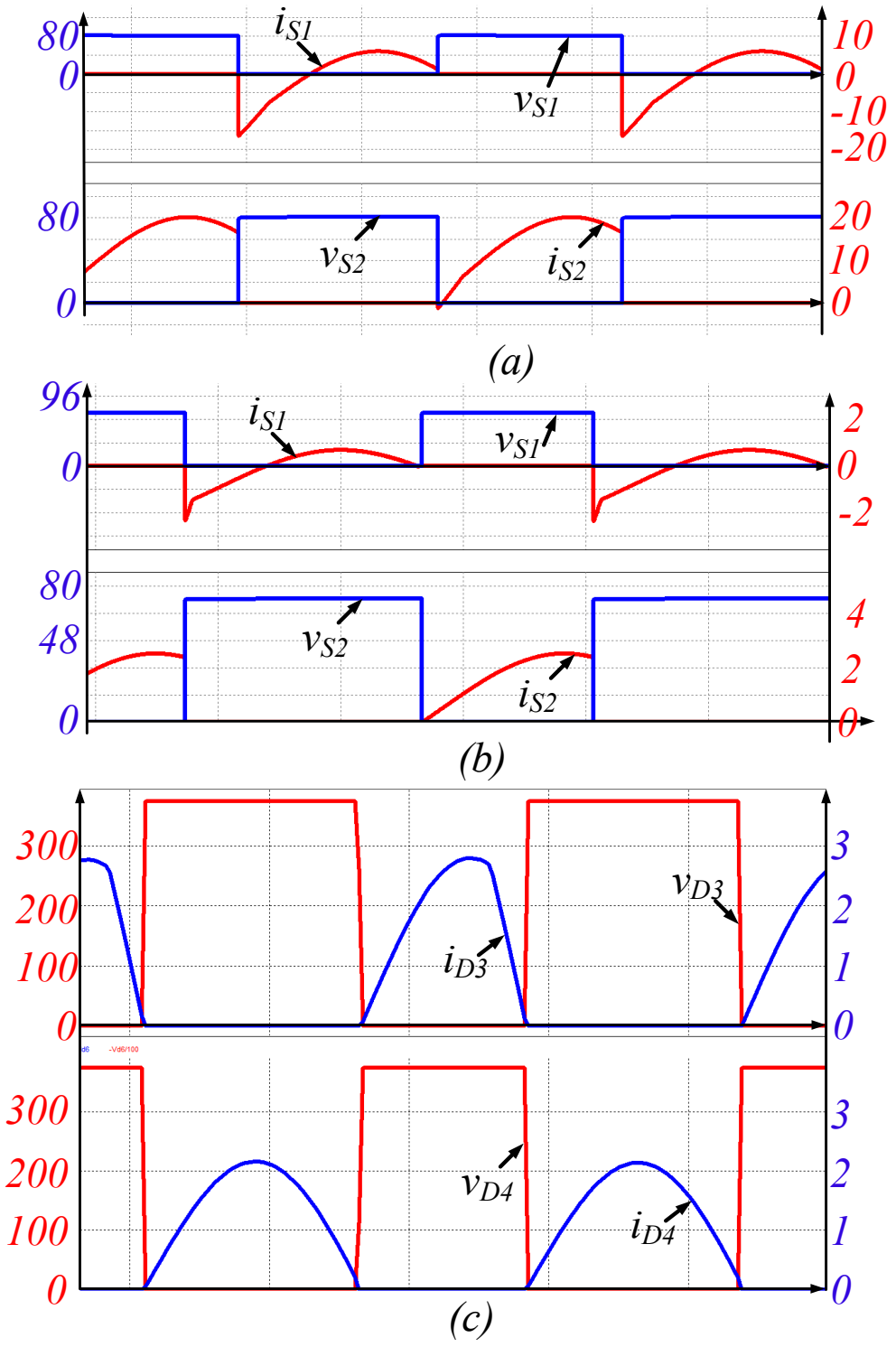


Fig. 6.17. Soft-switching of switches under (a) full load conditions and (b) light load conditions under maximum input voltage availability conditions. (c). soft-switching in secondary diodes due to rectification of resonant current.

6.5.3 Selection of Inductance ratio (L_n)

The inductance ratio is described as the ratio of the external parallel inductor to the series resonant inductor (L_n=L_p/L_r). Energy stored in the resonant tank is instrumental in operating switches S_1 and S_2 with the soft-switching. Energy stored in the resonant tank during full-load condition is enough for the soft-switching of S_1 and S_2 but not in the light-load conditions. Therefore, the external parallel inductor maintains extra energy in light load conditions to maintain soft-switching. Therefore, the soft-switching condition decides the value of required L_n in the converter to maintain soft-switching until light load. From Fig. 6.14(a), it can be decided that to achieve soft-switching till 10% of rated under input variations of 30V to 42V, L_n is selected as 10.

With the selection of parameters n, ω_n, z_r, L_n, resonant tank components are decided by (6.29), (6.30), and (6.31). Further design of other components is straight forward and already elaborated in Chapter 3, 4, and 5.

Table 6.1. List of components with part numbers used for prototype.

	Components	**Part number/Remarks**
1	Switches (S_1 and S_2)	200V, 64A, 17.5mΩ, IRFB4115PbF.
2	Diodes (D_1 and D_2)	600V, 8A, RFU10TF6S.
3	DC link capacitors	1uF, 400V film capacitors, 8 in parallel.
4	Output capacitors	680nF, 1kV, film capacitor.
5	Transformer	N 89 material, ferrite E core, primary 6 turns, secondary 33 turns. L_{lk}=1.5uH, L_m=13.5mH.
6	Resonant capacitors	10nF, 1kV, film capacitor
7	Gate driver	FOD3182

6.6 Simulation and experimental results

This section aims at verifying the proposed theory through simulation using PSIM 11.0 for maximum and minimum input conditions while serving load from rated load to 10% of rated load. Simulation results are presented in Fig. 6.15 to Fig. 6.17.

6.6.1 Simulation Results

High-frequency switching of S_1 and S_2, as verified and presented in Fig. 6.15(a), develops a constant voltage across C_1 and C_2. The resonant tank is fed with alternating voltage constituted with v_{C1} and v_{C2}. The Simulation results for minimum input voltage and full-load condition, as shown in Fig. 6.15 (b), also verifies this fact. Fig. 6.15(b) presents the resonant current based on resonant tank input voltage v_{ab} and resonant tank output voltage v_{tfp} under full load conditions and minimum input voltage. Sinusoidal resonant tank current justifies the adoption of the FHA technique for modeling of the converter. Further, as presented in Fig. 6.15 (b), current drawn by

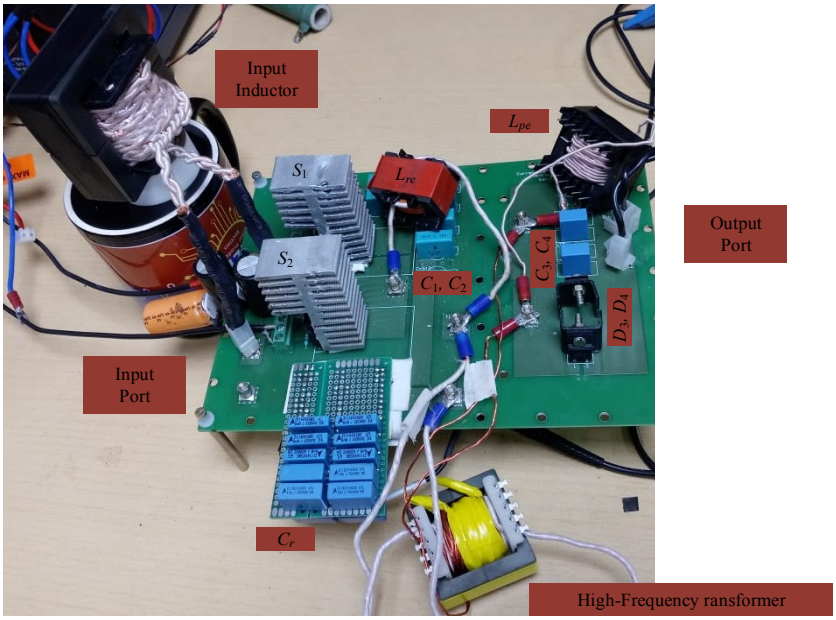


Fig. 6.18. Hardware prototype developed to test proposed converter.

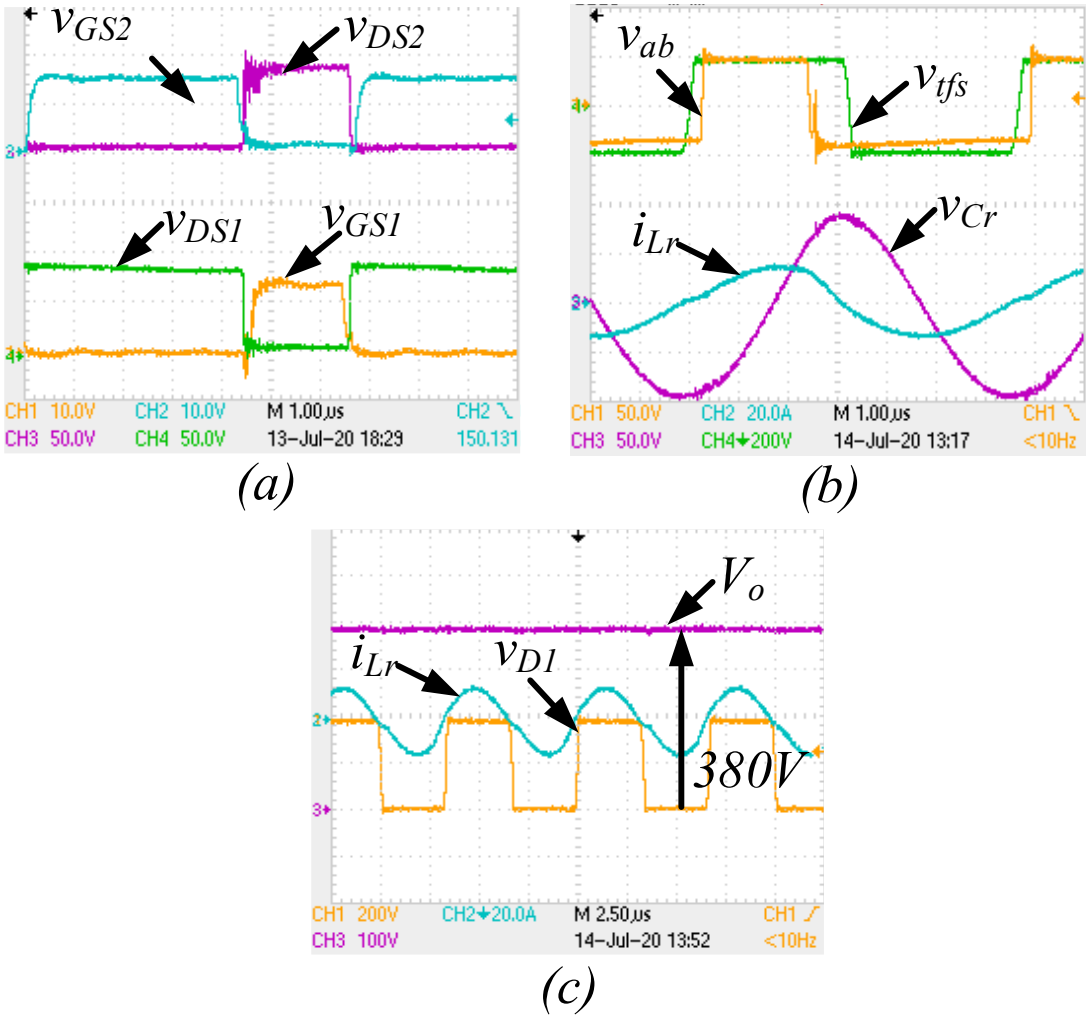


Fig. 6.19. Experimental results shown for V_{in}=30V, R_o=481.33Ω, V_o=380V. (a) Gate to source voltages and drain to source voltages of switches S_1, S_2. (b) Front end inverter output voltage (v_{ab}), transformer secondary voltage (v_{tfs}), resonant capacitor voltage (v_{Cr}), resonant tank current (i_{Lr}). (c) Output voltage (V_o), blocking voltage on voltage doubler diode (v_{D1}). Scales: v_{GS1}, v_{GS2} [10V/div]; v_{DS1}, v_{DS2}, v_{ab}, v_{Cr} [50V/div]; V_o [100V/div]; v_{tfs}, v_{D1} [200V/div]; i_{Lr} [20A/div].

the parallel inductor is negligible when compared to the resonant converter under minimum input and the rated load condition and justifies the approximation adopted in series resonant characteristic impedance design (6.28).

Fig. 6.16 (a) shows that the converter operation at minimum input voltage 30V and rated load condition maintaining ZVS switching to eliminate switching losses. Negative current during

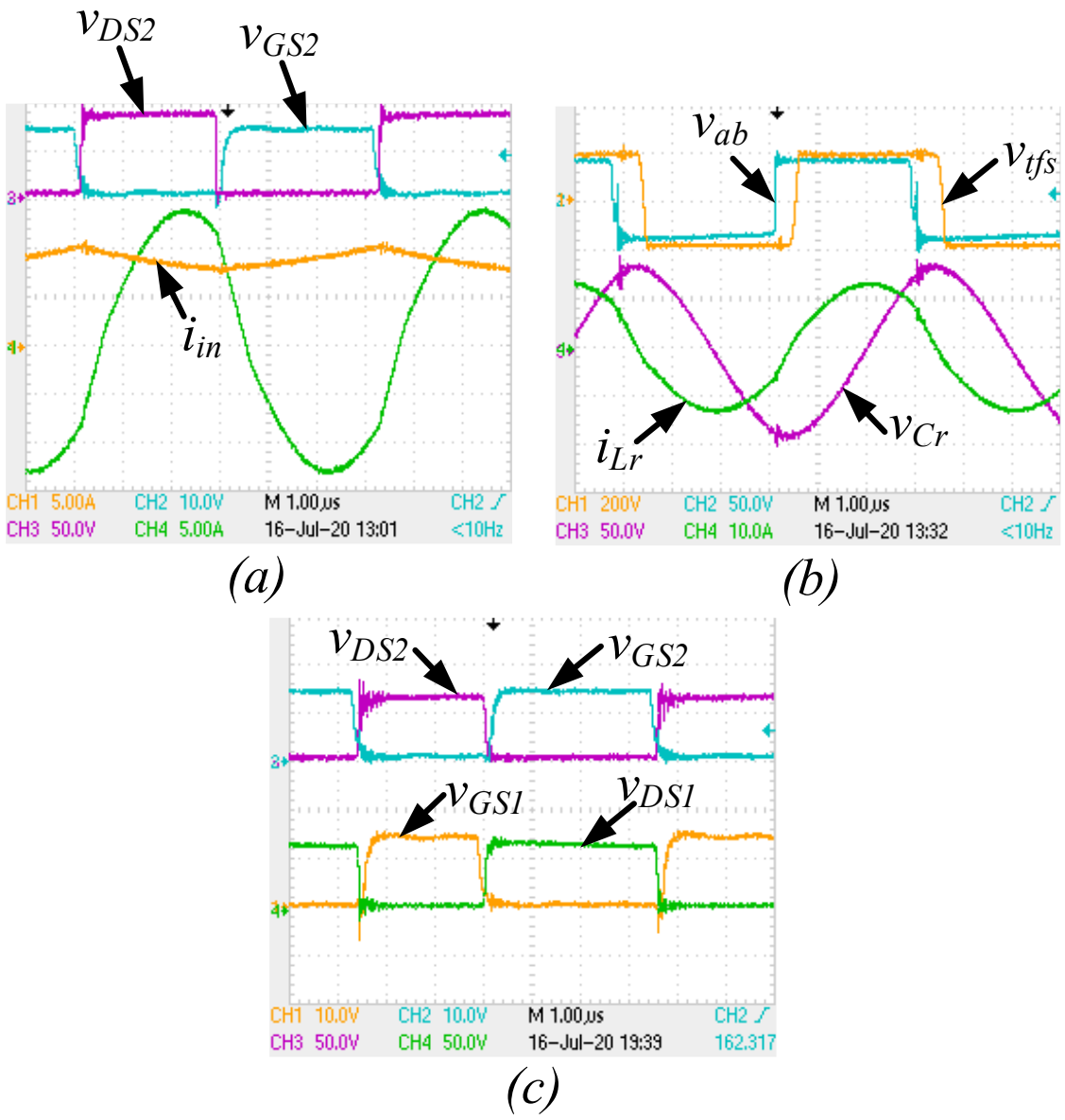


Fig. 6.20. Experimental results showing for (a), (b) Vin=42V, Ro=148.333Ω and Vo=380V and (c) Vin=30V, Ro=1483.33Ω and Vo=380V. Drain to source voltage of switches v_{DS1}, v_{DS2} [Scale:50V/div]; Gate to source voltage of switches v_{GS1}, v_{GS2}, [Scale:10V/div]; Front end inverter output voltage (v_{ab}), [Scale:50V/div]; transformer secondary voltage (v_{tfs}), [Scale:200V/div]; resonant capacitor voltage (v_{Cr}), [Scale:50V/div]; resonant tank current (i_{Lr}), [Scale:5A/div].

turn-on of the switches S_1 and S_2 from Fig. 6.16 (a) verifies this claim. Further, Fig. 6.16 (b) also verifies the fact that the proposed converter can maintain soft-switching till 10% of the rated load.

Similarly, Fig. 6.16 (a) and Fig. 6.16 (b) also confirms the fact that the proposed converter could maintain soft-switching irrespective of the variation in input voltage.

Fig. 6.14 (a) shows ZVS conditions for designed converter parameters, at minimum input voltage and rated load condition. The turn-on current for S_2 would be -5A to assure ZVS and design can sustain ZVS till 42V input voltage. The same is verified from Fig. 6.16 (a) when operating at 30V feeding rated load, with turn-on current of S_2 is -5A. This assures ZVS and it is maintained till 42V input. Near zero-current turn-on of S_2 in Fig. 6.17 (a) at 42V shows ZVS is lost beyond this voltage.

Fig 6.17 (c) shows currents carried by and voltages blocked by the voltage doubler diodes on the secondary side of the converter. It shows that the diodes conduct and commutate with ZCS. This soft-switching in diodes is due to the sinusoidal nature of resonant tank current, which is independent of load and input voltage fed, and so soft-switching of diodes.

6.6.2 Experimental Results

To validate the proposed analysis and design an experimental proof of concept hardware prototype has been developed in the laboratory. The hardware components are given in Table 6.1 and corresponding hardware setup is shown in Fig. 6.18.

6.6.2.1 Front-end inverter switches.

Voltage rating of switch is limited to 110V in proposed converter. Further, selecting a MOSFET with less conduction losses is conducive for maintaining possible higher efficiency. So IRFB4115PbF manufactured by Infenion is selected. Another major advantage is its brief turn off time which helps in minimizing turn-off losses at higher frequencies. Since proposed converter cannot provide soft-switching during turn off, this MOSFET is highly desirable.

6.6.2.2 Voltage doubler diodes.

Diodes in voltage doubler need to rectify current appeared on to secondary of transformer. This in turn appears as output voltage. Therefore, these diodes need to carry RMS current in proportion to load and block voltage equal to output voltage. In order to satisfy these requirements RFU10TF6S is selected. These diodes are rated for 600V, so can block 380V output voltage.

6.6.2.3 Split capacitor selection.

A 10uF, 160V electrolytic capacitor from shelf is taken for these capacitors. Care should be taken in current carrying capabilities of these capacitors as they are supposed to carry significant currents, especially lower split capacitor. Further, a high frequency film capacitor of 100nF, 400V is connected in parallel to each electrolytic capacitor.

6.6.2.4 Transformer

N 89 material ferrite E core is used to wind transformer with 1:5.5 turns ratio; primary 6 turns and secondary 33 turns. 1uH is obtained as leakage inductance. This can be part of required resonant inductance and remaining portion is obtained through an external series inductor with 6 turns.

Gate pulses required for driving the switches generated through TMS320F28335. Generated pulses are isolated and amplitude shifted to 15V peak through FOD3182 driver. Fig. 6.19 presents test results performed at input voltage 30V. The duty ratio and frequency of gate pulses are maintained at 0.69 and 150kHz to obtain an output voltage of 380V. Fig. 6.19(a) presents gate-to-source voltage and drain-to-source voltage of top and bottom switches (S_1, and S_2). Before the turn-on of the switches, i.e., during dead time, the drain-to-source voltage of the switches goes from blocking voltage to zero voltage to signify the fact that the negative turn-on current of the switch has discharged drain to the source capacitance. This forces the switch to maintain zero voltage across the drain-to-source terminals allowing it to turn on with ZVS. The same is observed for the upper switch of the converter. As the voltage across and the current through the switch are not overlapping, switching losses during turn-on are eliminated.

Fig. 6.19(b) shows the front end inverter output voltage and transformer secondary voltage reasonable to generate the resonant tank current. The corresponding voltage across the resonant capacitor is also presented in Fig. 6.19(b). It should be observed that the obtained results follow the simulation results closely as shown in Fig. 6.15(b). Further Fig. 6.19(c) shows the blocking voltage of the voltage doubler diodes. During zero voltage across diode, the resonant tank current is positive showing its conduction state. Further, it can be observed that the diode current at the beginning and commutating conduction instants is zero signifying ZCS turn on and ZCS turn-off in voltage doubler diodes. This is independent of load power and input voltage.

Also, Fig. 6.20(a) confirms the fact that the proposed converter maintains ZVS under maximum input voltage and full load condition. Fig. 6.20(b) shows the resonant current and corresponding voltage in the converter. Similarly, Fig. 6.20(c) verifies the fact that the proposed converter can maintain soft-switching till 10% of load demand.

6.6.3 Power loss analysis of the converter.

A comparison of power loss in the components is presented in Fig. 6.21 for the four cases i.e., LCL-SRC and (C)(L)(L)-SRC resonant converters serving rated load, 300W at an input voltage of 30V, and 42V, respectively. Fig. 6.21 reveals several interesting facts regarding the proposed converters. In all cases, power losses in secondary side diodes are same because diodes in all the cases carry load current, which is constant in all the four cases. This shows that power loss in the diodes is independent of the resonant tank employed and the value of input voltage.

The current required to maintain the desired output voltage while delivering demanded power is constant and is provided by the rectified resonant current. Therefore, the resonant current in all four cases is the same. However, the resonant current in (C)(L)(L)-SRC resonant converter is slightly lower than the LCL-SRC resonant converter. Therefore, power losses in (C)(L)(L) resonant tank are lower than the LCL resonant tank. However, this fact agrees with the principles of equivalence resonant tanks.

DC link capacitor C_2 carries input current (I_{in}) and resonant tank current (i_{Lr}) alternatively as S_1 and S_2 are switching with high frequency. Though i_{Lr} is the same at 30V and 42V, input

voltage reduces significantly at 42V conditions. Therefore, power loss in C_2 under minimum input voltage availability conditions. The same is the reason for S_2 to exhibit lower losses in case of maximum input voltage condition, though S_2 carries a combination of the input and the resonant currents during its conduction period. On the other hand, due to lower duty ratio at higher input voltage, the conduction time of the switch S_1 is significantly increases leading to higher RMS current through S_1 and higher power losses. Since dc-link capacitor C_1 and switch S_1 are connected in series, C_1 also observes a similar trend in power losses. Similarly, the input inductor observes a reduction in power loss with the increase in the input voltage, which relaxes the current stress in the converter to meet the desired power demand and output voltage.

6.6.4 The efficiency of the proposed converter

As seen from the above section, the components L_{in}, S_2, and C_2 turn out to be critical for power losses in the proposed converter and are dependent on the input voltage. At higher input voltage, the converter is operated with minimum power losses, therefore the converter exhibits higher efficiency for 42V cases in comparison to 30V cases. Further LCL-SRC resonant converter and (C)(L)(L)-SRC resonant converters exhibit nearly the same efficiency, as shown in Fig. 6.22, for a given available input voltage also agrees to equivalence resonance tank principles.

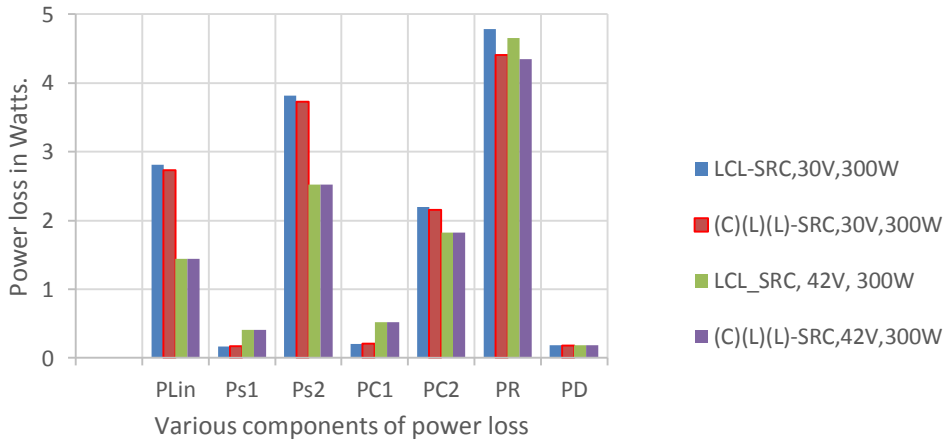


Fig. 6.21. Comparison of power loss in the proposed converter

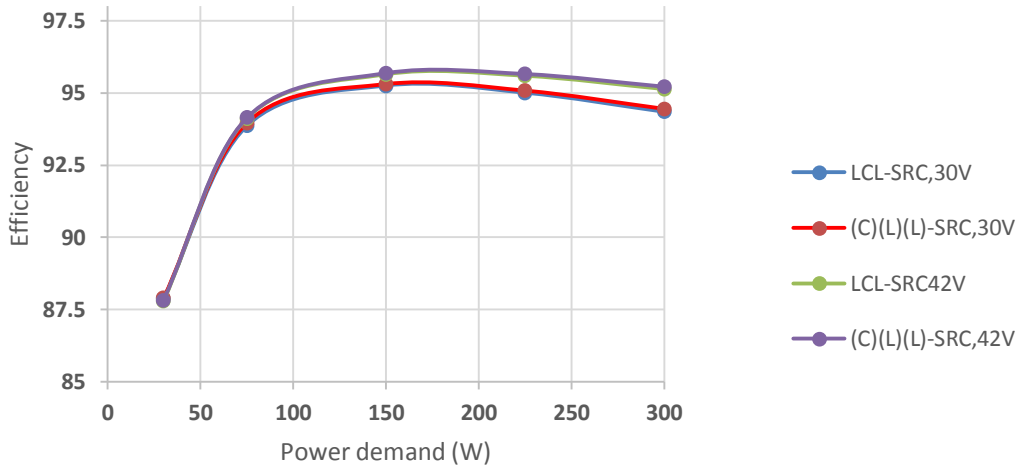


Fig. 6.22. The efficiency of LCL-SRC and (C)(L)(L)-SRC resonant converter.

Further, the peak efficiency of the converter is observed around half load but not at full load. This is a highly desirable characteristic because the majority power converters are operated below rated power for a significant amount in their lifetime but not always at full-load. This is also evident from weights laid by the California Energy Commission (CEC) to calculate the efficiency of a converter/inverter to quantify efficiency curves which are variable with power demand. Table. 6.2 and Table 6.3 show weights assigned by CEC commission and Euro commission, respectively according to the operating time of the converter for a given load during its lifetime. Weights in Table 6.2 and 6.3 reveals that the converter operates at full-load and extreme light load, for a small duration of time. On the other hand, loads between 20% and 80% received higher weights signifies a major operating portion for a converter during its lifetime.

A comparison of efficiency curves of the converters proposed against converters studied in previous chapters is also presented in Fig. 6.23 at minimum available input voltage and in Fig. 6.24 at maximum input voltage to study the impact of series resonance to achieve soft-switching. Fig. 6.23 shows a series resonant tank based high voltage gain dc/dc converter similar efficiency

Table 6.2. Weights approved for Euro efficiency calculation

Load percentage	100%	50%	30%	20%	10%	5%
Euro efficiency Weights.	0.2	0.48	0.1	0.13	0.06	0.03

Table 6.3. Weights approved for CEC efficiency calculation

Load percentage	100%	75%	50%	30%	20%	10%
CEC efficiency Weights.	0.05	0.53	0.21	0.12	0.05	0.04

at rated load condition but could not keep its efficiency up due to excess resonant tank current as explained in section I of this Chapter. Due to this reason efficiency of the LCC-T converter is relatively low irrespective of its operation in ZVS or ZCS mode. On the other hand, a series resonance can attenuate resonant current effectively under light load conditions to keep up the converter efficiency under light load conditions. For the same arguments mentioned, similar trend inefficiencies are observed even at maximum input voltage as shown in Fig. 6.24.

6.6.5 Comparison of the proposed converter

A comparison with the available converters is essential to bring out the unique features possessed by the proposed converter. For comparison of converters from various technologies such as 1) load resonant converter based on parallel resonance, as proposed in chapters 3, and 4 of this thesis, 2) load resonant converter based on series resonance, as proposed in Chapter 6 of this thesis, 3) Quasi resonant converter [] 4) LL type PWM based soft-switching converter. This converter brings out the soft-switching of the switches without using any resonance technique. A comparison among various techniques shows various advantages and setbacks in those technologies.

6.6.5.1 Converter ratings and modulation technique

A comparison is presented in Table. 6.4 and Table 6.5 shows the voltage and power ratings of the converters are almost equal, which forms a uniform base for comparison. All the contest converters are operated at high switching frequency maintaining a minimum of 100kHz to justify high switching frequency operation. LCC-T load resonant converter when operated in ZVS mode enters a switching frequency range of 200kHz due to its hybrid modulation. This is the major setback of this converter, making it complex to respond to the load and input disturbances. Input voltage in the range of 30V to 42V (140% of minimum input voltage) is considered for load

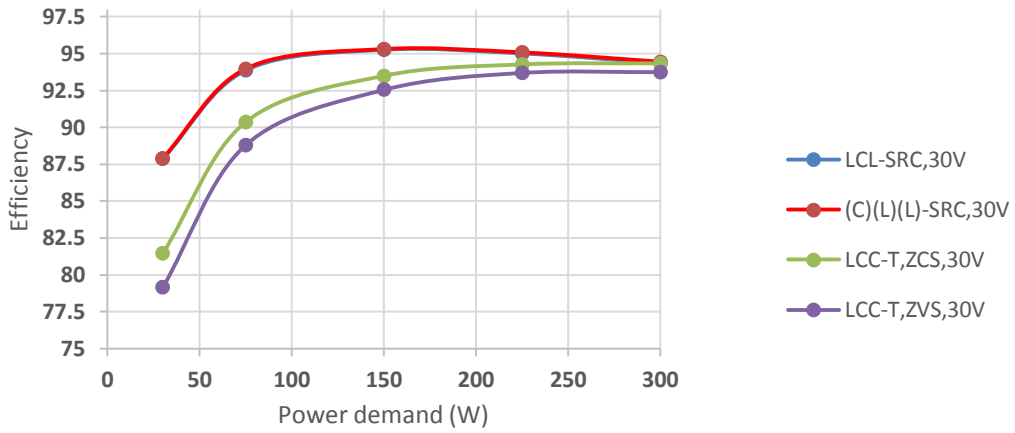


Fig. 6.23. Comparison of efficiencies among load resonant converter under minimum available input voltage conditions.

resonant converters while the input range possible for quasi-resonant converters is 30-34V (113% of minimum input voltage) which is very narrow. Interestingly, LL type PWM converter can hold soft-switching intact till 185% of its minimum input voltage, 22V to 41V. The load voltage for all converters is 380V, as it is the requirement for high voltage gain dc/dc converter feeding an inverter to generate 230V AC voltage.

6.6.5.2 Semiconductor devices

A major and comparable component in a power electronic converter is a semiconductor device. From Table 6.4, it is understood that the LL type PWM converter needs the highest number of main switches and auxiliary switches because it needs two boost converters in an interleaved fashion to achieve its schema of operation. This is a setback in this converter because it cannot implement its technique with a lower number of switches as possible in load resonant and quasi-resonant converters. Further, current stress and blocking voltage ratings are the two most important parameters, which are instrumental in finding a part number of switches and diodes because these ratings decide power losses, on-state resistance, and thermal stability of a switch under operation. Eventually, they influence efficiency, power density, and volume of the converter. Load and quasi-resonant converters are designed for the same rating, so they are closely comparable.

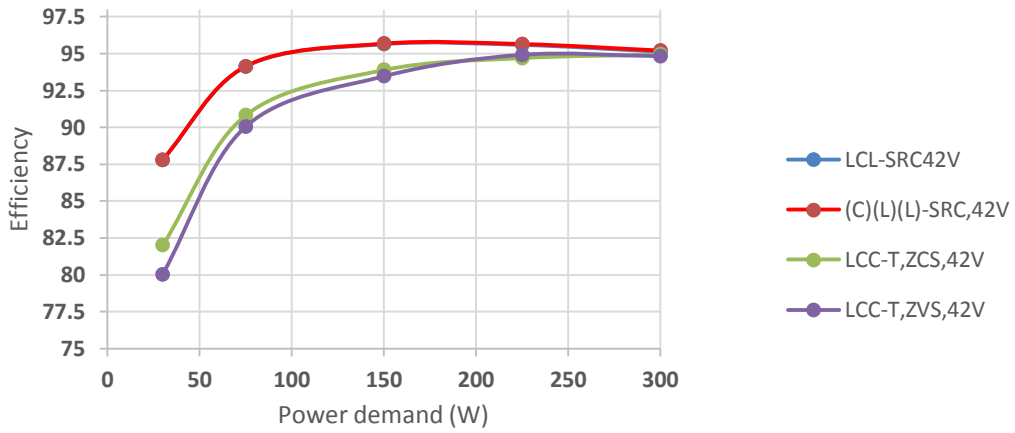


Fig. 6.24. Comparison of efficiencies among load resonant converter under maximum available input voltage conditions.

6.6.5.2.1 Diodes

It is observed that the secondary side diodes for the load resonant converters irrespective of the resonant tank observe similar voltage and current stress while in the quasi resonant converter the diodes face slightly higher stress. Though diode current stress on LL type PWM converter is slightly lower side than other converters, it uses a diode bridge rectifier with four diodes. Therefore, current stress is shared between two sets of diodes, thus looks smaller. But irrespective of voltage doubler or diode voltage rectifier each diode is supposed to block full load voltage. However, all diodes rectify a sinusoidal current so that they enjoy soft-turn on and soft turn off which helps to evade reverse recovery in them.

6.6.5.2.2 MOSFETs

MOSFETs in these converters are included for two functions, as the main switching element and the auxiliary switching element. The main switching element always processes the majority of the power and auxiliary switches only divert residual current during the blocking period of the main switch into a clamping capacitor till its next turn on. Therefore, main switches are subjected to higher current stress, while auxiliary switches are highly relaxed. On the other hand, the voltage stress on both types of switches is the same in a converter because both the

Table 6.4. Comparison of the proposed converter

		Load Resonance				Quasi	PWM
		Parallel Resonance		Series Resonance			
Parameter		**LCC-T ZVS**	**LCC-T ZCS**	**LCL SRC**	**(C)(L)(L) SRC**	**[54]**	**LL type**
Converter Ratings							
Output power		300W	300W	300W	300W	300W	200W
Output voltage		380V	380V	380V	380V	380V	350V
Input voltage range		30-42V	30-42V	30-42V	30-42V	30-34V	22-41V
Frequency of operation		175-210kHz	128kHz	150kHz	150kHz	100kHz	100kHz
Load compensation		Hybrid	PWM	PWM	PWM	PWM	PWM
Semiconductor ratings							
Diode	Avg. current	0.8A	0.8A	0.8A	0.8A	1.3A	0.66A
	Blocking Voltage	380V	380V	380V	380V	380V	350V
	Turn-on	ZVZCS	ZVZCS	ZCS	ZCS	ZCS	ZCS
	Turn-off	ZVZCS	ZVZSC	ZCS	ZCS	ZCS	ZCS
	Count	2	2	2	2	2	4
Main switch	RMS current	15.264A	14.4A	13.7A	13.69A	16.06A	6.1A
	Peak current	27A	26A	23.33A	23A	30A	15A
	Peak voltage	110V	110V	110V	110V	90V	110V
	Turn-on	ZVS	Hard	ZVS	ZVS	ZVS	ZVS
	Turn-off	Hard	ZCS	Hard	Hard	Hard	Hard
	Count	1	1	1	1	1	2
Auxiliary switch	RMS	1.67A	1.47A	2.89A	2.9A	4.25A	1.52A
	peak	2.8A	2.6A	6A	6A	10.5A	5.6A
	Peak voltage	110V	110V	110V	100V	90V	110V
	Turn on	ZVS	Hard	ZVS	ZVS	ZVS	ZVS
	Turn off	Hard	ZCS	Hard	Hard	Hard	Hard
	Count	1	1	1	1	1	2

Table 6.5. Comparison of the proposed converter continued.

	Load Resonance				**Quasi**	**PWM**
	Parallel Resonance		**Series Resonance**			
Parameter	**LCC-T ZVS**	**LCC-T ZCS**	**LCL SRC**	**(C)(L)(L) SRC**	**[54]**	**LL type**
Resonant tank						
L_r	10.69uH	9.26uH	10.504uH	11.5544uH	2uH	4uH
C_s	18.55nF	22nF	129.68nF	129.68nF	NA	NA
C_p	1.85uF	44nF	NA	NA	NA	NA
L_m	NA	NA	105.04uH	115.44uH	NA	1.61mH
Gain offered by tank	1.7	1.8	0.87	1.05	NA	NA
Resonant Current (RMS, full load)	10.89A	10.42A	9.78A	8.806A	12.93A	4A
Resonant Current (RMS, light load)	6.43A	5.4A	1.06A	0.886A	0.4A	
Transformer						
Transformer voltage rating (primary)	81.66V	81.72V	34.67V	37.83V	27.07V	61V
Transformer current rating (primary)	5.094A	4.77A	9.746A	8.8065A	12.93A	4A
Transformer VA rating	415.976VA	389.804VA	337.893VA	333.149VA	350VA	245.6VA
KVA/KW rating	1.39	1.3	1.263	1.11	1.16	1.166
TUF	72.12%	76.96%	88.78%	90.05%	85.73%	81.24%
Transformer turns ratio	1:2	1:2	1:5.5	1:5	1:7	1:4

switches are alternatively clamped with the same DC link capacitor during their off or blocking state.

It should be observed that the current stress in LL type PWM converter is significantly less than load and quasi-resonant converter as the total current stress in LL type PWM converter is shared between two main switches operated in an interleaved fashion. Even though peak current plays a minimum role in selecting a device, it is maximum in the case of the quasi-resonant converter. This eventually raises the RMS current of the switch higher, which plays a prominent role in switch selection. Among load resonant converters, (C)(L)(L)-SRC and LCL-SRC converters exhibit minimum switch RMS and peak currents. On the other hand, these converters exhibit higher peak currents and thus higher RMS currents in the auxiliary switch. However, power losses in auxiliary switches are negligible in comparison to the main switches. Also, the type of soft-switching in a converter is based on the design of the converter. It is to be observed that, unlike secondary diodes, it is not possible to achieve soft-switching on both transitions of a MOSFET. Therefore, all converters enjoy soft-switching either during turn-on or turn-off.

6.6.6 Resonant tank

Load and quasi-resonant converters employ a resonant tank while a LL type PWM converter is free of it. However, it needs an inductor like a resonant inductor in load resonant converters and is mandatory to achieve the soft-switching. In any case, the selection of the resonant tank components or inductor in the case of LL type PWM converter plays a very important role in the soft-switching range of the converter against input voltage variations and load disturbances. All contesting converters in Table 6.5 can exhibit the soft-switching through the entire operation of load, i.e., 10% of the rated load. But the challenge is to maintain the soft-switching against variations in input voltage. LL type PWM converter can offer soft witching in converter till 186% of minimum input voltage, while load resonant converters offer till 150% of the minimum input voltage. However, quasi-resonant converters suffer a major setback in maintaining the soft-switching against variations in input voltage.

Resonant currents through the resonant tank incur conduction losses, which are suppressed effectively under full and light load conditions in the case of LLC-SRC and CLC-SRC resonant converters. On the contrary, LCC-T resonant converter on operating with either ZCS or ZVS would contribute gain to overall converter gain, thus relaxing the burden on high-frequency

transformer turns ratio. However, LCL-SRC resonant converter attenuates the overall converter gain thus demands the transformer with a higher turns ratio. On the other hand, (C)(L)(L)-SRC resonant converter offers unity gain or slightly boosts up the overall converter gain, despite a variant of the series resonant converter. Therefore, this converter relaxes the transformer turns ratio. Finally, the resonant tank in a quasi-resonant converter does not contribute to overall converter gain, thus requiring the transformer with a higher turns ratio.

6.6.7 High-frequency transformer

The isolation element high-frequency transformer in power electronic converters for high voltage gain applications exacerbates its non-idealities due to large turns ratio and higher switching frequency. Fortunately, soft-switching techniques help to tame energy stored in non-idealities from turning into current and voltage spikes. Therefore, in all contesting converters, non-idealities are utilized properly for the soft-switching of the devices.

LCC-T resonant converter either with ZCS or ZVS, needs lower transformer turns ratio due to boosting nature of the resonant tank followed by the LL type PWM converter, LCL-SRC resonant converter, (C)(L)(L)-SRC resonant converter, and lastly quasi-resonant converter. The volt-ampere rating of the transformer decides the size of the transformer and is presented in Table 6.4. LCC-T resonant converter under ZVS mode has the highest volt-amperes rating of the transformer thus worse utilization of transformer is observed. On the other hand, the proposed (C)(L)(L)-SRC resonant converter exhibits the highest transformer utilization of 90% with 333.149VA, next to the LCL-SRC resonant converter with 88.78% TUF as given in Table 6.5.

Though LL type PWM converter and other contesting converters are compared with different power ratings, (C)(L)(L)-SRC converter exhibits superior transformer utilization over LL type PWM converter.

6.7 Conclusion

This Chapter evaluates the impact of the resonance circuit adopted in an isolated high voltage gain DC/DC converter to achieve soft-switching, wide-range input and load disturbance attenuation, modulation, high efficiency, high density, better transformer utilization, etc.,

1. As studied in Chapters 3, and 4 a parallel resonance (LCC-T tank) based high voltage gain DC/DC converter can offer soft-switching against input voltage range of 30-42V and load range till 10% of the rated load. This converter under ZCS mode needs simple modulation to control converter while in ZVS mode it adopts a complex hybrid modulation technique, a combination of duty and frequency control. However, this converter either in ZCS or ZVS modes unable to maintain better light load efficiency due to excess resonance current needed in the converter to charge and discharge the parallel capacitor. Therefore, compromised power density and TUF.
2. The proposed converter uses dual of parallel resonance i.e., series resonance-based resonance tank to counter setbacks in LCC-T resonant converter. Since a series resonance tank can offer only a maximum gain of unity, the transformer must compensate with a higher turns ratio than the LCC-T converter to achieve the desired gain.
3. Energy stored in the resonant tank is utilized for the soft-switching. The external inductor is connected in parallel to extend the soft-switching till 10% of the rated load. Inclusion of external inductance leads to 3 types of resonant tanks, LCL-SRC, (L)(LC)-SRC, and (C)(L)(L) -SRC resonant tanks. Among them, (L)(LC)-SRC is not suitable for adoption due to low-frequency resonance while LCL-SRC and (C)(L)(L)-SRC are equivalent based on the resonant tank equivalence principal. LCL-SRC converter is studied and modeled using FHA harmonic approach. Based on the equivalent circuit, the converter is designed.
4. Simulation results are shown to verify the proposed analysis. Results have verified the converter's ability to maintain the soft-switching for varying load conditions. Further, efficiency calculations have shown improvement in the converter's performance,

especially under light load conditions as the comparison to the LCC-T resonant converter.

5. A comparison table is provided to verify the fact that the converter offers a simple modulation technique, subject minimum currents and voltage stress on components, higher TUF over quasi-resonant converters, and LL type PWM type converter.

Next Chapter summarises and presents conclusions of the thesis.

Chapter 7 Conclusion and Future Work

This Chapter concludes the thesis. The summary of this thesis is presented in section 7.1, the contributions of this thesis are presented in section 7.2 followed by its scope and guidelines for future work in section 7.3.

7.1 Summary.

Technologies such as microgrids and ePTO systems have seen significant penetration on their way to integrate non-conventional energy sources such as PV/fuel cell/batteries into DC/AC grids. A high voltage gain DC/DC converter plays an important role in such integrations by matching its input port with intermittent availability of source and the output port with uncertain power demands of the load. Further, maintaining a high voltage gain, high efficiency to reduce the time of return, high power density to minimize the size of the converter is another side of the challenge.

To enhance the lifetime of low voltage PV/fuel cell/battery, current-source converters are widely studied in the literature over voltage-fed counterparts due to stiff input current, inherent voltage gain. Of them, resonant converters gained relatively limited attention on research over quasi-resonant converters. This research provides a detailed overview of clamped/unclamped isolated high-gain soft-switching resonant/quasi-resonant current-fed converters. A clamped quasi-resonant converter addresses the historical turn-off voltage spike issue in current-fed converters by incorporating an active-clamp circuit thereby complicating the converter and its driving needs. However, they offer simplicity in the modulation of the converter and dynamic regulation. On the other hand, an unclamped quasi-resonant converter inherently addresses the historical turn-off spike issue thereby offering simple converter and driving needs. However, it demands a complex modulation technique and dynamic regulation. Besides, light-load efficiency and the need for relatively small resonant components that are to be designed and manufactured

with high precision are inherent setbacks of quasi-resonant converter technology. Considering these drawbacks, this thesis presents the study on the adoption of resonant converters for the integration of PV/fuel cell/battery to DC bus in applications of microgrid and ePTO systems.

A high voltage gain DC/DC load resonant converter whose characteristics can be tuned with a given resonant tank is studied in Chapter 2. Key merits of it are 1) its current source feature to help to draw PV/fuel cell/battery-friendly current. 2) ZCS of the active switches if switching frequency is below resonant frequency or ZVS otherwise. 3) a simple PWM modulation at constant switching frequency if a suitable resonant tank and operating region point are selected. 4) ZCZVS turn off, of the diodes eliminating the need for the reverse recovery time. Therefore, rectifier grade diodes can be used. 5) No voltage and current spike on the switches to the transformer and device parasitic as they are integrated into the operation of the resonant tank of the converter.

Besides, the resonant frequency of the resonant tank is proposed closer to the switching frequency of the converter. To design the converter for higher switching frequency while offering practically realizable leakage inductance of the transformer and high-power density. This translates as higher power processing capabilities for current-fed soft-switching resonant converters. Further, the selection of a proper resonant tank can result in better light load efficiency and wider soft-switching range with source voltage. Higher energy storing capability in the resonant tank can push the power processing capability of the converter.

Simplified modeling of the resonant converters is a challenge due to numerous steady-state variables. Conventional time domain, state-space, and state plane approach, though accurate, are laborious and complicated thus resort to computer-aided techniques. Even though FHA can simplify the modeling of the resonant converters, it fails in the case of parallel and series-parallel resonant converters with capacitive filters. Existing FHA techniques allow a few approximations to simplify the modeling of such converters at the cost of inaccuracy and complexity. This thesis proposes a technique to restore the simplicity of FHA analysis for such circuits. This technique suggests modifications in the calculation of equivalent impedance, which in turn simplifies and improves the accuracy of the modeling. Accuracy and ability of the proposed equivalent linear sinusoidal (ELS) circuit to mimic actual series-parallel resonant converter with capacitive filter

are verified through simulation and experimental results. Further, the proposed technique is equally valid in the case of a parallel resonant converter with a capacitive filter.

Chapter 3 evaluates the characteristics of an LCC-T resonant converter operating below switching frequency. The gain characteristic of the LCC-T resonant tank is like a parallel resonance tank. Thus, it offers a load-independent gain characteristic below resonance. Since this gain is not vulnerable to load demand, the proposed converter is designed to operate in this region. This enabled the converter to operate at constant switching frequency with ZCS throughout the operating range. Soft switching of the semiconductor devices is maintained until 10% of rated load and till 150% of minimum input voltage variations. However, due to the parallel resonant capacitor, converter efficiency is compromised under the light load condition.

Chapter 4 studies and investigates the converter proposed in Chapter 3 in the above resonance mode to bring ZVS switching of the switches, which is more relevant in the case of MOSFETs. Due to the variable voltage gain of the resonant tank above resonance, the converter adopts a complex hybrid modulation technique. Though soft-switching of the converter is maintained until 10% of rated load and till 150% of minimum input voltage variations, the converter efficiency is highly compromised due to higher switching frequency operation.

Chapter 5 extends the converter proposed in Chapter 4 to its three-phase circuit to evaluate the converter for higher power rating. Like Chapter 4, the switches operate in ZVS mode, and the converter adopts a complex hybrid modulation technique. The converter can maintain soft-switching until 10% of the rated load. Further range of input voltage is also increased from 150% to 185% in comparison to the single-phase version. Simulation and experimental results are demonstrated for performance verification.

Chapter 6 proposed and investigated a series of resonance derived LCL-SRC resonant converter to counter setbacks of the LCC-T resonant converter. Though the transformer turns ratio is higher than the LCC-T resonant converter, the proposed converter can offer constant switching frequency operation, significantly improved light load efficiency, and ZVS of the MOSFETs, down to 10% of rated load and up to 150% of minimum input voltage variations.

A detailed comparison is provided in the table to verify the fact that the converter offers a simple modulation technique, exerts minimum currents and voltage stress on components, higher transfer utilization factor over clamped/unclamped quasi-resonant converters, and LL type PWM type converter.

Finally, the flat efficiency curve of the proposed converter allows to conserve maximum possible available energy. This increase in energy efficiency helps to reduce the carbon footprint. On average a US house hold can save a 10,972kWh energy accounts for $1450USD per year. From market study, it can be observed that a saving of 2500kWh electrical energy can supress 1.18million carbon emissions which is equivalent of 7.82million BTU savings [173], [174]. On the other hand, the increase in switching frequency capacity, power processing capability, input and load range and flat efficiency curve of the proposed converter opens up new medium and heavy duty applications like refrigerator trucks, long haul vehicles etc., as these applications need a power processing capability of tens of kilo watts for tens of hours which is otherwise not possible with available techniques intended that are intended for low power applications.

7.2 Contributions

The following are considerable contributions of the proposed thesis.

1. Traditionally, FHA analysis is adopted to mathematically model the load resonant converters except parallel resonant tank adopted capacitive ended converters. This thesis contributed to a simple FHA technique to ease the modeling of such converters. The proposed methodology is verified in theory and practice. Later, this method is proved instrumental in modeling several load resonant converter topologies proposed and analyzed in this thesis.
2. This thesis contributed to the analysis and design of a new parallel resonance LCC-T tank based current-fed high voltage gain topology for below and above resonance region. ZCS and ZVS operations of the devices are studied and experimentally verified. Two different modulation techniques are proposed to maintain soft-switching and high efficiency with wide source voltage and load current.

3. Besides, the thesis contributed to the analysis and design of a new three-phase topology of the proposed converter with an LCC-T resonance tank suitable for higher power capacity. It showed a significant improvement in input voltage and load current range for soft-switching and voltage regulation.
4. To overcome setbacks that appeared due to the parallel resonance tank, the thesis contributed to a series of resonance derived LCL-SRC resonant converter. This analysis revealed that the voltage stress on the components of this converters is lesser and the transformer utilization is significantly improved when compared to quasi-resonant converters. With an acceptable efficiency, this converter maintains soft switching for a wide range of input voltage and load current variations.

7.3 Scope of future work

With the experience gained during the compilation of this thesis, the following future work is recommended.

7.3.1 Robust closed loop control

Proposed high voltage gain DC/DC converters are intended for microgrids and automobile PTO systems. For such applications, PV panels cell are subjected to continuous fluctuations in load current and input voltage. Therefore, it is essential to develop robust controller to reject these fluctuations. This is achieved by developing a dynamic model of the topologies followed by designing a suitable controller to suppress the disturbance within a reasonably short response time.

7.3.2 Exploring other resonant tanks.

Converter characteristics can be further tuned by adopting other types of 2-elements resonant tanks and 4-elements resonant tanks to improve light-load efficiency, widen the soft-switching range against load disturbances and input voltage variations and improve voltage gain.

7.3.3 Scalability and operation.

Higher power processing scenarios involve in large quantities of current flowing through the devices. This dissipates significant power loss and high temperature rise leading to low efficiency and converter failure. In order to avoid this condition, an interleaved operation of the converter is recommended.

The interleaved operation of the proposed converter allows current sharing in the devices and other components to protect for higher power applications. On the other hand, a series connection of output terminals also allows its uses for higher output voltage applications, whose block diagram is shown in Fig. 7.1. Further, LCL-SRC resonant tank can be inherently achieved by using leakage inductance of the transformer, parasitic capacitance of the switch, and magnetizing inductance of the transformer.

The reduction of current in each device significantly reduces the power losses and thus temperature raise of the switches is within limits. This helps to improve efficiency of the converter.

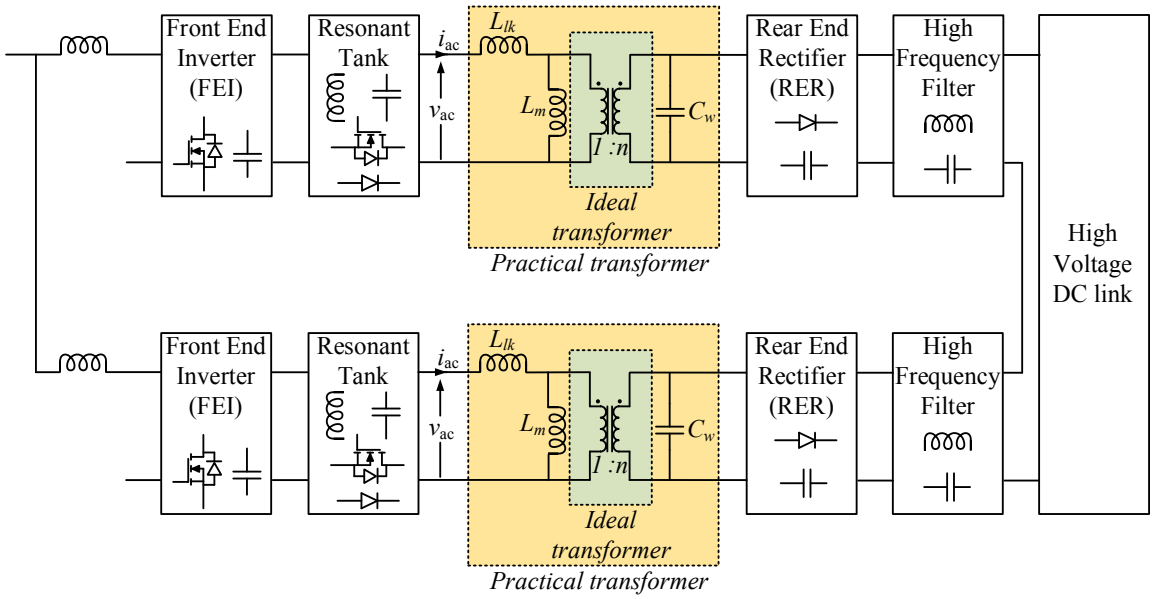


Fig. 7.1. Block diagram for interleaved current sharing at the input and series connected at the output for high power and high voltage DC link aplications.

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