© Universiti Tun Hussein Onn Malaysia Publisher's Office

IJIE

Journal homepage: http://penerbit.uthm.edu.my/ojs/index.php/ijie
ISSN : 2229-838X e-ISSN : 2600-7916

The International Journal of Integrated Engineering

Modular Multilevel DC-DC Boost Converter for High Voltage Gain Achievement with Reduction of Current and Voltage Stresses

M. N. A. Samat[1], Asmarashid Ponniran[1*], M. A. N. Kasiran[1], M. H. Yatim[1], M. K. R. Noor[1], J. N. Jumadril[1]

[1]Faculty of Electrical and Electronic Engineering,
Universiti Tun Hussein Onn Malaysia, Johor, 86400 MALAYSIA

*Corresponding Author

DOI: https://doi.org/10.30880/ijie.2021.13.02.005
Received 9 June 2020; Accepted 1 December 2020; Available online 28 February 2021

Abstract: This paper presents a modular multilevel DC-DC boost converter for high voltage gain achievement with reduction of current and voltage stresses. Normally, conventional DC-DC boost converter (CDBC) has low voltage gain capability, higher current and voltage stresses which lead to high conduction loss of the semiconductor devices due to the circuit structure limitation. Therefore, 4-level synchronous modular multilevel DC-DC converter (SMMC) with Marx topology adaptation is considered to improve the limitation circuit structure of CDBC. Besides, the 4-level SMMC have high voltage gain achievement, it also has lower current and voltage stresses features. A 145 W and 48 V input voltage of 4-level SMMC has been designed and experimentally verified where the result is compared with CDBC. The results show that the CDBC required 0.76 of duty cycle while 4-level SMMC only require 0.5 duty cycle to achieve 200 V output voltage, respectively. Additionally, the current stress decreases by 75% on input inductor and 50% reduction from voltage stress of switching as compared to the CDBC. Consequently, the selection rating for the components can be decreased and higher efficiency can be obtained for the 4-level SMMC as compared to the CDBC.

Keywords: Current stress, DC-DC boost converter, electric vehicle, Marx topology, multilevel converter, voltage stress

1. Introduction

The request for EV is growing fast as the demand for eco-friendly technologies increase. Conventional fossil fuels basis transportation system emits cumulative carbon particle to the atmosphere which lead to increasing of global warming issue [1], [2]. As fossil fuel extracted from earth and may come to an end, EV can replace the transportation system shortage of fuel in the future [3]. The call for growing demand on EV contributes to higher demand on the power converter system in which majorly consist of inverter and DC-DC converter. In the motor traction for EV propulsion of EV [4], [5], the ability to step up the storage of low voltage to higher rated usage is required and realized by considering DC-DC boost converter.

For EV power delivery from source (AC grid) to EV system load, the usage of power converter is highly important [6], [7]. Basically, DC-DC converters consist of a group of passive components. Various switching frequency may impact the improvisation of converter volume, weight and overall size [8]. Furthermore, when high switching frequency is considered for the DC-DC converter, it can decrease the converter performance due to switching device stress, high switching loss [7], and electromagnetic interference (EMI).

Today, the demand of DC-DC boost converter increases in line with the advance technology and development of converter arrangement for various application including EV. Moreover, the importance of DC-DC boost converter also

*Corresponding author: asmar@uthm.edu.my

exists in Datacenter/ Datacom system [9], transmission of HVDC system, and renewable energy industry [10], [11]. In EV, the boost converter is considered in order to step-up from low state at battery bank to higher voltage value which suitable for busbar supply of the EV system [12], [13]. Major criteria in converter design for EV are the converter efficiency and lower weight, lower volume, and small current ripple strained from battery [1], [14]. This requirement though does not achieve because of the drawback raised by the conventional boost converter [15].

Consequently, the 4-level SMMC configuration lead to a better topology to attain high voltage gain. With the converter structure implementation of multilevel and modular principle, the high voltage gain can be achieved. A number of modules are organized in a multilevel arrangement in order to generate a parallel scenario during capacitor charging mode. Then in discharging mode, the arrangement makes the capacitor discharge in series mode [12], [16], [17]. The controlling of the switches at the ON and OFF state lead to achieved the SMMC principle.

This study concentrates to design a multilevel modular converter which achieve high voltage gain with lower current stress and volt-age stress [18]. The comparison of both conventional converter (CDBC) and proposed multilevel modular DC-DC boost converter (SMMC) have done accordingly. Furthermore, both CDBC and 4-level SMMC circuit parameter design is also determined. In addition, the rated stresses of current are examined and compared at the converter input side.

2. Concept of High Voltage Gain Converter

There is variation of modular arrangements. The modular arrangement is also identified modular block or sub-module [7]. In general, a group of modules made the modular structure. Figure 1 illustrate high voltage gain converter by considering modular block to CDBC. In short, the modules can be defined as a combination of a few components that connected to each other. Whereas, modular is a combination of a few modules that is connected to each other. Each module can either be dissimilar from each other or can also be identical [16]–[18]. In the meantime, the relationship of CDBC duty cycle with output voltage and the relationship of SMMC duty cycle with output voltage are shown in Figure 2 respectively. It translates that at similar duty cycle, the output voltage generated by SMMC is higher as compared to the one generated by CDBC. Hence, the converter with voltage gain capability can conceivably reach based on this clarification.

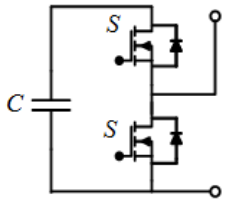


Fig. 1 - Marx topology modular block principle

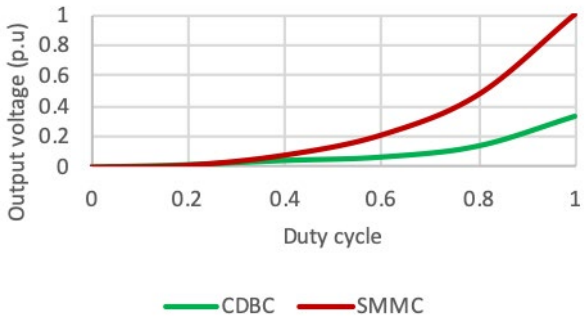


Fig. 2 - Relationship of duty cycle against output voltage (p.u.) for CDBC and SMMC

3. Principle of CDBC and 4-level SMMC

Basically, the CDBC circuit structure only comprise of an inductor, one capacitor, one diode and one switching device [13]. In the meantime, 4-level SMMC contains of five inductors, five capacitors, four diodes and eight switching devices. Conferring to [16], [19], the output voltage and input voltage have a relationship and can be stated as (1). Primarily, the rate of output voltage V_{out} of DC-DC boost converter is greater than the input voltage V_{in}.

$$\beta = \frac{V_{out}}{V_{in}} \tag{1}$$

Varying the converter duty cycle can step-up and step-down the output voltage of 4-level SMMC accordingly. The output voltage of DC-DC boost converter can further express with input voltage and duty cycle in a relationship as shown in (2).

$$V_{out} = \frac{V_{in}}{1-D} \tag{2}$$

3.1 Principle of CDBC

The general circuit arrangement and operation modes of Conventional DC-DC boost converter shown in Figure 3. From the figure, it displays the two operation modes of the CDBC. The operation mode is decisive for the charging and discharging stage towards the boost inductor component [1]. The energy being step-up will be transferred from input to the converter output sides. In order to operate the CDBC, a simple pulse width modulation (PWM) is required for the switch. As illustrated in Figure 4, the switching scheme of PWM by in view of a duty cycle swing at 0.5 and 0.76, respectively.

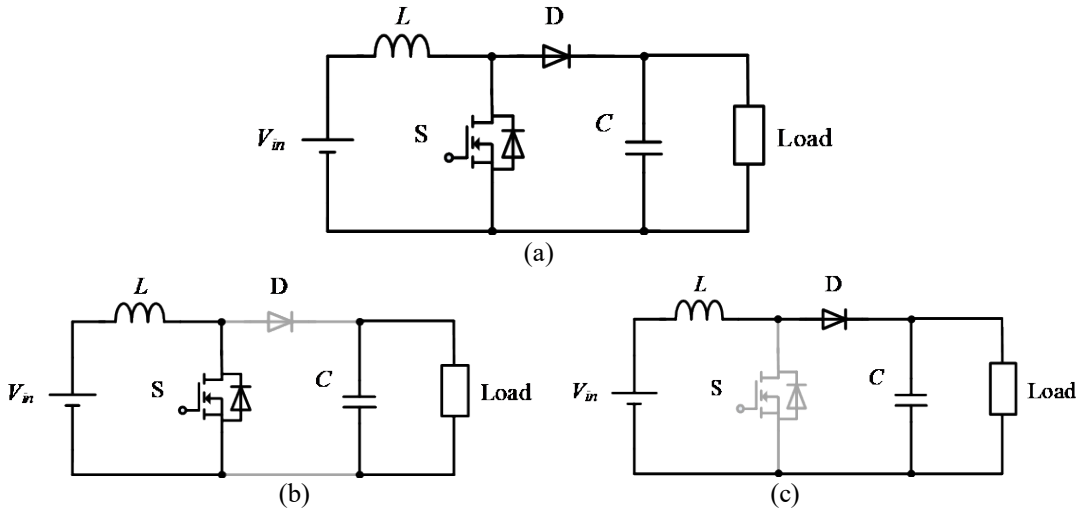


Fig. 3 - Circuit structure of CDBC (a) Main circuit structure (b) Operation mode 1 (c) Operation mode 2

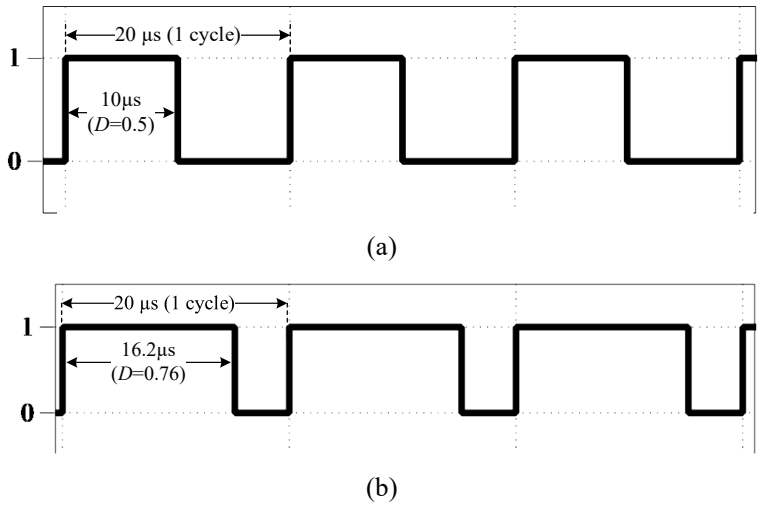


Fig. 4 - CDBC switching scheme for (a) 0.5 duty cycle (b) 0.76 duty cycle

3.2 4-level SMMC Principle

As shown in Figure 5, the main circuit arrangement of 4-level SMMC are stated. The circuit operation of 4-level SMMC can then separate into four operation modes. For high voltage gain achievement, the circuit arrangement intended the capacitor connect in parallel set-up in charging cycle, then abruptly change to series set-up during discharging mode [16], [19]. Consequently, the voltage of each charged output capacitors being added and sump up

before transferred to the load. This continuous and repeating process will provide the 4-level SMMC achieve the high voltage gain.

During operation mode 1, the switches is turn-OFF in every stage where the switches are Sc (S1c, S2c, S3c, and S4c). When the stage capacitor is in series connection, the voltage is rated at the load. Hence, the diodes operate in reverse biased thus virtually perform an open circuit scenario. Due to the open connection for input side and output side, the process of charging and discharging of inductor is occurred due to the current flow [16], [17]. For operation mode 2, the dead-time is set at the switching, whereas for operation mode 3, an additional time-delayed is set. To avoid a short circuit operation, those dead-time and time-delayed is required. Besides, the dead-time and time-delayed are also function to ensure the switches is fully turn-ON or turn-OFF. Furthermore, dead time and time-delayed also act as the safeguard to avoid scenario of surge voltage and short circuit [16], [20]. In operation mode 4, all switches Sa are turn-OFF. In this state, the current is flow to the output side due to the diodes are in forward bias. Hence, the energy from the inductor and capacitor can be transferred to the output side to realize the step-up voltage [16], [20], [21].

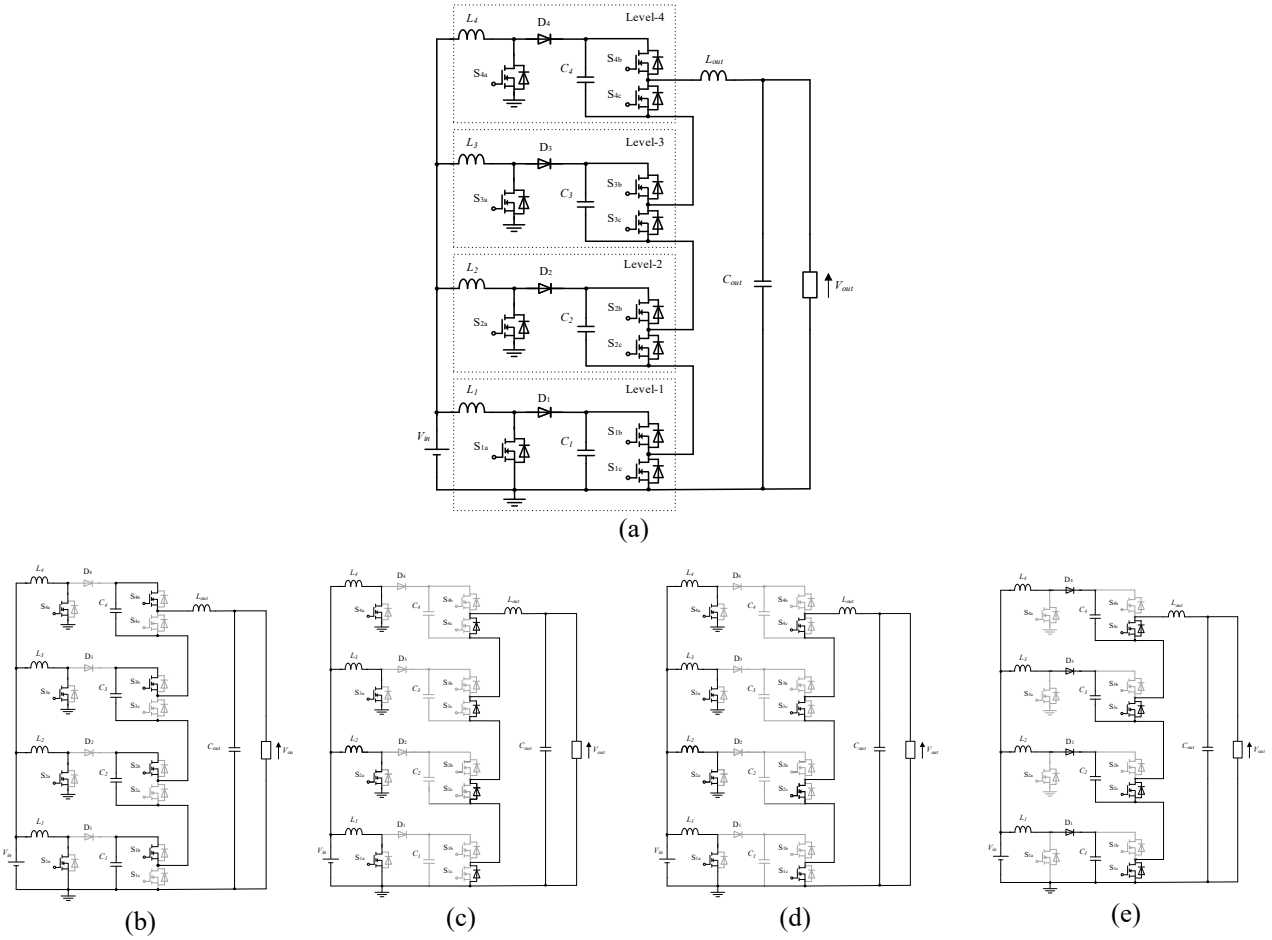


Fig. 5 - Circuit structure of 4-level SMMC (a) Main circuit structure (b) Mode 1: Capacitor discharging in series (c) Mode 2: Dead-time (d) Mode 3: Time-delayed (e) Mode 4: Capacitor charging in parallel

Figure 6 shows the switching pattern of the circuit that runs with three signals of PWM. Sa and Sb run in the same shape of PWM signals while Sc run at inverse pattern compared to Sa and Sb. Nonetheless, as the dead-time and additional time-delayed requirement, a slightly different of duty cycle (in the range of 0.01 duty cycle or 0.2μs) have been set, accordingly.

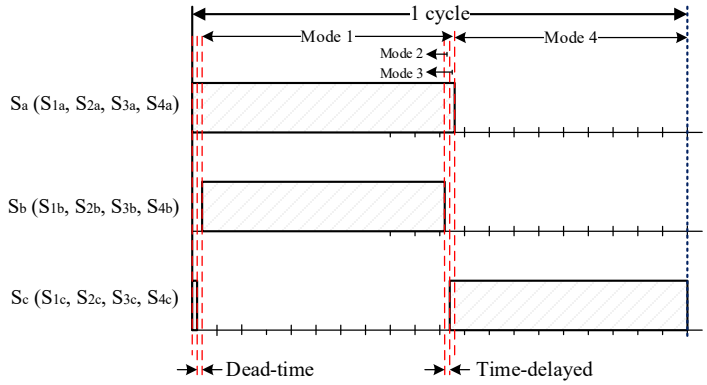


Fig. 6 - 4-level SMMC switching scheme

4. Parameters Design of CDBC and 4-level SMMC

Circuit parameters design is essential to comprehend the operation of converter circuit. Principally, inductor and capacitor are designed based on the current ripple and voltage ripple, respectively [7], [14]. Table 1 shows the parameter design of inductor and capacitor for CDBC. Meanwhile, Table 2 shows the parameter design of inductor and capacitor of 4-level SMMC. The design inductor and capacitor are different due to the unique circuit structure of 4-level SMMC with CDBC.

Table 1 - CDBC inductance and capacitance formulae

Parameter	Formula	
Inductor	$L = \frac{V_{in} D T_{sw}}{\Delta I_L}$	(1)
Input current	$I_{L(ave)} = \frac{V_{in}}{(1-D)^2 R}$	(2)
Minimum inductor	$L_{\min} = \frac{D(1-D)^2 R}{2 f_{sw}}$	(3)
Capacitor	$C = \frac{I_c D T_{sw}}{\Delta V_C}, I_c = I_{out}$	(4)

Table 2 - 4-level SMMC inductance and capacitance formulae

Parameter	Formula	
Input inductor	$L_{in(m)} > \frac{n(V_{in})^2 D}{2 P_{out} f_{sw}}$	(5)
Inductor current ripple	$\Delta I_{Lin(m)} = \frac{V_{in} D}{f_{sw} L_{in(m)}}$	(6)
Output inductor	$L_{out} = \frac{\left(n\frac{V_{in}}{1-D} - V_{out}\right)D}{f_{sw}\Delta I_{Lout}}$	(7)
Average inductor current on each stage	$I_{L(m)-ave} = \frac{P_{in}}{n V_{in}}$	(8)
Stage capacitor	$C_{(m)} = \frac{I_{L-ave(m)}(1-D)}{\Delta V_{C(m)} f_{sw}}$	(9)
	$C_{(m)} = \frac{P_{in}(1-D)}{n V_{in} \Delta V_{C(m)} f_{sw}}$	(10)
Maximum stage capacitor voltage	$V_{C(m)-\max} = V_{DS-\max}$	(11)
	$V_{C(m)-\max} = V_{in} + \frac{V_{out}}{n}$	(12)

4.1 Parameters Value of CDBC

Table 3 shows the parameters value for CDBC. The parameters value has been separated for both duty cycle of 0.5 and 0.76, respectively. For comparison, 0.5 of duty cycle is selected, while 0.76 of duty cycle is considered in order to achieve the desired output voltage.

Table 3 - Parameters design of the CDBC for V_{out} = 200 V

Parameter	Value	
	D = 0.5	D = 0.76
Output power, P_{out} (W)	145	
Input voltage, V_{in} (V)	48	
Output Voltage, V_{out} (V)	96	200
Voltage gain, β	2	4.17
Switching frequency, f_{sw} (kHz)	50	
Inductor, L (mH)	1	
Capacitor, C (μF)	470	

4.2 Parameters Value of 4-level SMMC

Table 4 illustrate the parameter design of 4-level SMMC. To achieve an output voltage of 200 V, 0.5 of duty cycle is considered regarding that, the input supply is 48 V.

Table 4 - Design parameters of the 4-level SMMC for V_{out} = 200 V

Parameter	Value
Output power, P_{out} (W)	145
Input voltage, V_{in} (V)	48
Output Voltage, V_{out} (V)	96
Voltage gain, β	2
Switching frequency, f_{sw} (kHz)	50
Inductor, L (mH)	1
Output inductor, L_{out} (mH)	8
Capacitor, C (μF)	470

5. Result and Analyses

In this research, the principle of the converter has been confirmed with simulation works and further confirmed with the experimental works, accordingly. The experimental works has been done for 145 W of CDBC and 4-level SMMC with input voltage of 48 V with a desired output rated of 200 V being set. Generally, there are three significant parameters are observed in 4-level SMMC which are the voltage gain, the stresses of voltage at capacitor, and the inductor current stress at input side.

5.1 High Voltage Gain Achievement

Simulation works has been performed for CDBC and 4-level SMMC converter circuit. Result from the simulation indicate that CDBC only produce 96 V when the duty cycle is set at 0.5. To achieve 200 V of output voltage, a higher duty cycle at 0.76 need to be implemented to the CDBC converter circuit. In contrast, 4-level SMMC can achieve 200 V at 0.5 duty cycle by considering same input voltage. Thus, the boost ratio of CDBC is 4.17. The result is experimentally confirmed with a prototype for CDBC and 4-level SMMC converter circuit. Figure 7(a) indicate the CDBC experimental result when operate at 0.5 duty cycle where the output experiment result rated at 96 V. Figure 7(b) further show the experimental result of CDBC circuit when operated at 0.76 duty cycle for desired 200 V output voltage realization.

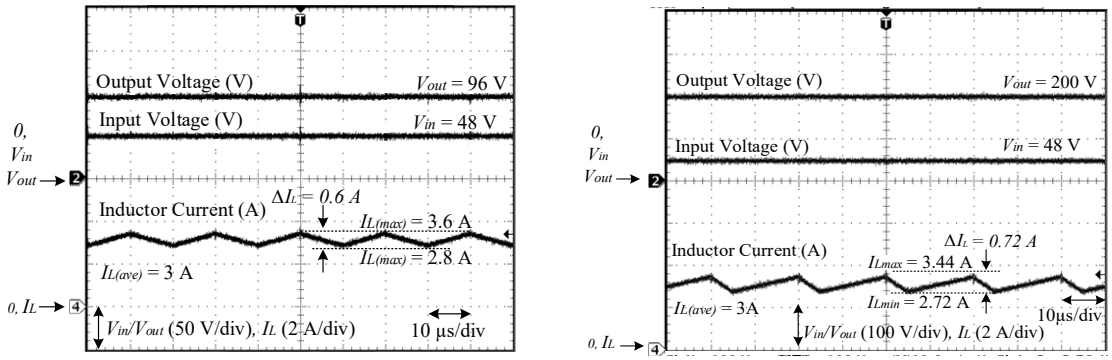


Fig. 7 - Experimental results of CDBC when (a) $D = 0.5$, and (b) $D = 0.76$

The experimental result for 4-level SMMC with input voltage at 48 V is shown in Figure 8. At 0.5 of duty cycle, 200 V of output volt-age can be obtained.

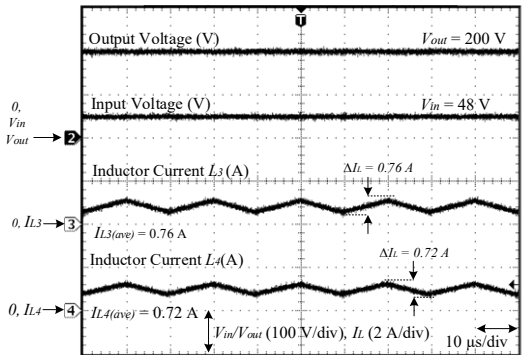


Fig. 8 - Experimental result of 4-level SMMC for $D = 0.5$

5.2 Input Inductor Current Stress Reduction

Principally, the current flow through input inductor and input cur-rent is similar. For the input inductor, the current stress is equal to the maximum value of current ripple generated at the input inductor. This is further verified with the simulation result and experimental work done to both CDBC and 4-level SMMC system. Simulation results of CDBC in Figure 9 shows the value of input inductor current flow at 3 A which is equal to the input current of the converter. In Figure 9 (a), the converter run at duty cycle of 0.5, the current stress at input inductor is equal to 3.36 A. In Figure 9 (b), when the CDBC converter run at duty cycle of 0.76, the stress of current at input inductor is 3.24 A. In another word, as the input current of the CDBC increase, the value of current stress at input inductor will also increase which lead to higher rating of inductor, and increase of the inductor sizing.

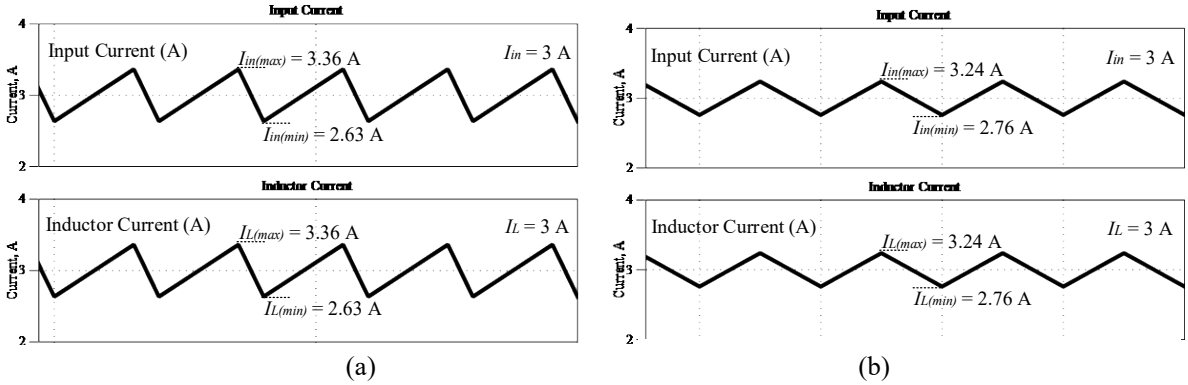


Fig. 9 - Simulation results of current stress on input inductor of CDBC at $L_{in} = 1$ mH for (a) at 0.5 duty cycle and (b) at 0.76 duty cycle.

The result from experiment for the current flow at input inductor of 4-level SMMC is shown in Figure 10. Due to limitation of component rating, the input current generated at 4 A. The current flow through each four of input inductor of the 4-level SMMC are around 1 A with the current stress for each level is around 1.3 A. Due to the parallel connection, the input inductor has smaller cur-rent stress as compared to the input current. With the current flow through input inductors decrease, the current stress is also reduced and smaller rating of inductor and lesser size of inductor can be implemented in the converter circuit.

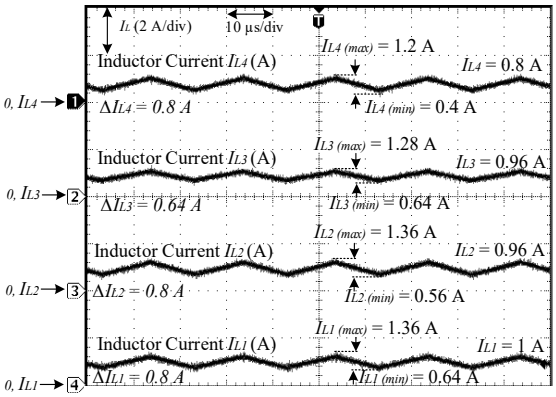
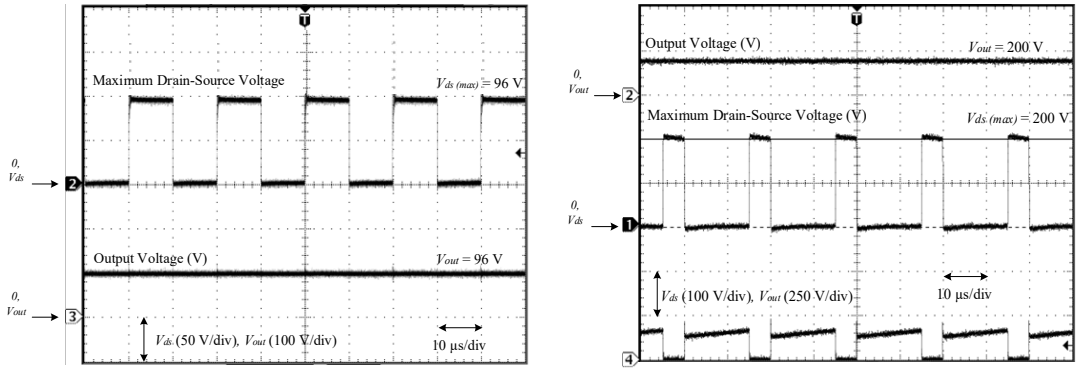


Fig. 10 - Experiment result for input inductor current stress of 4-level SMMC

5.3 Reduction of Voltage Stress at Converter Switch

Conventionally, the voltage stress on switching device similar with the output voltage due to the circuit structure limitation. Theoretically, the main contributor to switching device (ie: MOSFET) power loss occurs at the drain-source area. Higher voltage converter lead to higher drain-source voltage rating which increase the switching loss. Figure 11 shows experimental result of output voltage of CDBC when 0.5 and 0.76 of duty cycle are considered. The maxi-mum drain-source voltage are 96 V and 200 V when 0.5 and 0.76 of duty cycle are considered, respectively. Where the maximum drain-source voltage is similar with its output voltage.



(a) (b)

Fig. 11 - Experiment results of CDBC voltage stress with V_{in} =48V (a) at 0.5 duty cycle, V_{out} = 96 V (b) at 0.76 duty cycle, V_{out} = 200 V

Further experimental works is done to determine the voltage stress at 4-level SMMC as shown in Figure 12. Different location of switching devices have been considered to remark the voltage stress value. In this case, switches S4a, S1b and S2c have been selected. From the result at Figure 12, it shows that all of the MOSFET maximum drain-source voltage rated at 100V or in another words, two times lower than the CDBC MOSFET drain-source voltage for the same 200 V output voltage. With lower current stress achievement, MOSFET with smaller voltage rating can be used and smaller heat sink can be implemented to the converter system.

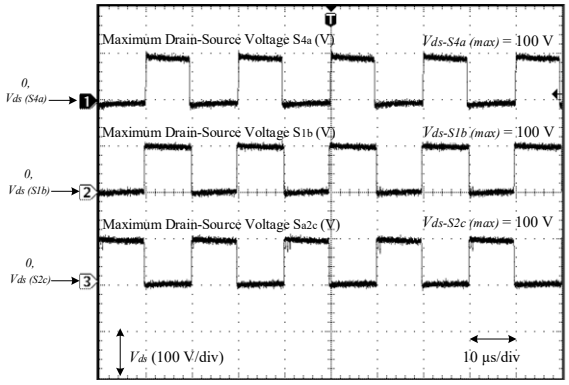


Fig. 12 - Experiment result of 4-level SMMC voltage stress at 0.5 duty cycle with V_{in} =48V

6. Conclusion

The author of this paper has discussed the achievement of high voltage gain in DC-DC boost converter when multilevel modular structure with Marx topology is considered. According to the simulation and experimental results, it has been confirmed that the pro-posed 4-level SMMC able to achieve high voltage gain due to the improvement of circuit structure. The difference percentage the output voltage of CDBC and 4-level SMMC for a same duty cycle is 67%. Besides, 4-level SMMC also having 75% smaller stress of current at input inductor and 50% less voltage stress at the converter switching device. Consequently, these will directly decrease the overall size of the inductor, decrease the size of heat sink and improve efficiency of the converter.

Acknowledgement

The authors would like to express their appreciation to the Universiti Tun Hussein Onn Malaysia. This research is funded by the Research Fund GPPS Vot H535.

References

[1] M. A. N. Kasiran, A. Ponniran, M. H. Yatim, and J. Itoh, "Evaluation of high power density achievement of optimum 4-level capacitor-clamped DC–DC boost converter with passive lossless snubber circuit by using Pareto-Front method," *IET Power Electron.*, 2019

[2] A. B. Ponniran and M. A. N. B. Kasiran, "Parameters design evaluation in 3-level flying capacitor boost converter," in *2017 IEEE Symposium on Computer Applications & Industrial Electronics (ISCAIE)*, 2017, pp. 195–199

[3] Y. Nozaki, "Development of higher-voltage direct current power feeding system for ICT equipment," *NTT Tech. Rev.*, vol. 7, no. 10, 2009

[4] M. K. R. Noor *et al.*, "Modified single-switch bridgeless PFC SEPIC structure by eliminating circulating current and power quality improvement," *IET Power Electron.*, vol. 12, no. 14, pp. 3792–3801, 2019

[5] J. Itoh and T. Fujii, "A new approach for high efficiency buck-boost DC/DC converters using series compensation," in *2008 IEEE Power Electronics Specialists Conference*, 2008, pp. 2109–2114

[6] S. M. Alagab, S. Tennakoon, and C. Gould, "Bidirectional marx DC–DC converter for offshore wind farm application," *J. Eng.*, vol. 2019, no. 17, pp. 3848–3854, 2019

[7] M. Taherian, M. Allahbakhshi, E. Farjah, and H. Givi, "A Modular Topology of Marx Generator Using Buck–Boost Converter," *IEEE Trans. Plasma Sci.*, vol. 47, no. 1, pp. 549–558, 2019

[8] V. A. K. Prabhala, P. Fajri, V. S. P. Gouribhatla, B. P. Baddipadiga, and M. Ferdowsi, "A DC–DC converter with high voltage gain and two input boost stages," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 4206–4215, 2015

[9] A. Ponniran, K. Orikawa, and J. Itoh, "Modular multi-stage Marx topology for high boost ratio DC/DC converter in HVDC," in *2015 IEEE International Telecommunications Energy Conference (INTELEC)*, 2015, pp. 1–6

[10] M. Muhammad, M. Armstrong, and M. A. Elgendy, "A nonisolated interleaved boost converter for high-voltage gain applications," *IEEE J. Emerg. Sel. Top. power Electron.*, vol. 4, no. 2, pp. 352–362, 2015

[11] M. K. Kazimierczuk and D. Czarkowski, *Resonant power converters*. John Wiley & Sons, 2012

[12] D. Anair and A. Mahmassani, "State of Charge: Electric Vehicles' Global Warming Emissions and Fuel-Cost Savings Across the United States; Union of Concerned Scientists: Cambridge, MA, 2012," *There is no Corresp. Rec. this Ref. Sch*

[13] Z. Lulić, E. Missoni, and R. Tomić, "The relevance of GHG emissions from motor vehicles," *Trans. FAMENA*, vol. 37, no. 2, pp. 39–56, 2013

[14] I. Alhamrouni, W. I. Hanis, M. Salem, F. M. Albatsh, and B. Ismail, "Application of DC-DC converter for EV battery charger using PWM technique and hybrid resonant," in *2016 IEEE International Conference on Power and Energy (PECon)*, 2016, pp. 133–138
[15] G. Hua and F. C. Lee, "Soft-switching techniques in PWM converters," *IEEE Trans. Ind. Electron.*, vol. 42, no. 6, pp. 595–603, 1995
[16] J.-M. Clairand, J. R. García, C. Á. Bel, and P. P. Sarmiento, "A tariff system for electric vehicle smart charging to increase renewable energy sources use," in *2017 IEEE PES Innovative Smart Grid Technologies Conference-Latin America (ISGT Latin America)*, 2017, pp. 1–6
[17] J. Dudrik and J. Oetter, "High-frequency soft-switching dc-dc converters for voltage and current dc power sources," *Acta Polytech. Hungarica*, vol. 4, no. 2, pp. 29–46, 2007
[18] T. Anandhi and S. PremKumar, "Application of DC-DC boost converter for solar powered traffic light with battery backup," *Indian J. Sci. Technol.*, vol. 8, no. 32, pp. 1–5, 2015
[19] C.-H. Shin, D.-Y. Kim, A.-Y. Ko, I.-K. Won, Y.-R. Kim, and C.-Y. Won, "The configuration of electric vehicle system using isolated DC-DC converter for a low-voltage and high-current type battery," in *2015 9th International Conference on Power Electronics and ECCE Asia (ICPE-ECCE Asia)*, 2015, pp. 2796–2801
[20] X. Li, P. Chen, and X. Wang, "Impacts of renewables and socioeconomic factors on electric vehicle demands–Panel data studies across 14 countries," *Energy Policy*, vol. 109, pp. 473–478, 2017
[21] A. Bin Ponniran, K. Orikawa, and J. Itoh, "Fundamental Operation of Marx Topology for High Boost Ratio DC-DC Converter," *IEEJ J. Ind. Appl.*, vol. 5, no. 4, pp. 329–338, 2016