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# Design of Extended Channel Ge-source TFET for Low Power Applications

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**Abstract**: In this paper, a novel design of a TFET structure using Ge-source and extending a part of the channel into the source is proposed. The DC performance is analyzed by evaluating the ON current, $I_{ON}/I_{OFF}$ ratio and subthreshold swing (*SS*). Moreover, the high-frequency performance is inspected in terms of transconductance ($g_m$) and unit-gain cutoff frequency ($f_T$). All simulations are performed utilizing 2D SILVACO TCAD. It is demonstrated that the ON current and the cut-off frequency can be simultaneously improved by appropriate design of the proposed structure.

**Keywords:** TFET, ambipolar current, Band-To-Band Tunneling (BTBT), transconductance, Subthreshold Swing (SS), cut-off frequency

## 1. Introduction

The continuous scaling down of the conventional MOSFET leads to a superior behavior regarding higher speed, improved high frequency (HF) performance and lower operational power [1, 2]. However, the miniaturization is obstructed by several unwanted effects that arose in the MOSFET as the device size goes on shrinking [3]. CMOS technology shows certain conditions as the device is scaled more and more in the nanometer regime, out of which power dissipation is an important issue. To overcome the issues regarding power dissipation, specific low power design techniques using CMOS are implemented [4]. Reduction of power dissipation could be achieved by reducing the supply voltage, but this has a disadvantage of increasing the delay.

New devices are being proposed in the literature to overcome the disadvantages resulted from miniaturization. One of the most promising devices in this regard is the tunneling FET (TFET). A TFET is a gated PiN diode that is turned on by applying a gate bias [5]. The gate voltage is used to modulate the width of the tunneling barrier, as the width is controlled by the electric field in the tunneling junction.

The current in conventional MOSFETs is based on the thermionic emission mechanism of charge carriers over a potential barrier. Consequently, keeping the power consumption within an acceptable boundary is one of the most severe difficulties for the conventional MOSFETs at advanced technology nodes. But TFETs avoid this issue by using the band-to-band tunneling (BTBT) mechanism rather than thermal injection to inject carriers into the channel of the device. The result of these mechanisms shows that the minimum subthreshold swing (*SS*) of the MOSFET is about 60

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mV/decade at room temperature. In comparison, the *SS* of TFETs is generally less than 60 mV/decade at room temperature [6].

Besides exhibiting *SS* lower than 60 mV/decade, TFETs also have the following advantages: reduced leakage current by using the BTBT mechanism and the similarity in the fabrication process compared with MOSFET [7]. However, TFETs have two critical drawbacks: low ON-current level and ambipolar behavior [8].

The coupling of the gate voltage with the channel potential has a profound impact on the $I_{ON}$ of the TFET. This has motivated researchers to design the transistor gate to improve $I_{ON}$ using some techniques like employing multiple gate structures [9, 10] or using a semiconductor heterojunction of different materials to have lower effective bandgap and hence higher $I_{ON}$ and lower subthreshold swing [11]. In this respect, low bandgap semiconductors, such as InAs [12] and $Mg_2Si$ [13], have been utilized. Such materials demonstrated higher tunneling rates than those in silicon because of their small bandgap, leading to a higher ON/OFF current ratio [14, 15].

One of the most attractive alternative materials used in TFETs is Germanium (Ge). Ge has attracted the attention of device engineers due to having a low bandgap ($E_g$ = 0.67 eV) and high carrier mobility. These characteristics result in a higher $I_{ON}$ [16, 17]. Some research works have considered the transfer characteristics and capacitance of Ge TFET but did not investigate the transconductance and the cutoff frequency of the device that are considered the main analog/RF parameters [18, 19].

In this paper, a new design of a TFET structure is proposed in which a part of the channel is extended into the source. The Ge material is used to serve as a source, while silicon is employed as the channel and drain material. By using the proposed structure, the ON current of Ge-source TFET is improved as well as the transconductance. The enhancement in transconductance boosts the cutoff frequency, as will be shown herein.

The paper is structured as follows. Following the introduction, section 2 presents the simulation methodology and device structure. The simulation results are discussed in section 3. Section 4 is devoted to the parametric analysis. The final section is devoted to the paper conclusion.

## 2. Simulation Methodology and Device Structure

All simulations, presented in this work, have been performed using SILVACO 2D ATLAS device simulator. The models used in the simulations are listed in Table 1. Firstly, the BTBT model is calibrated against the work in [20], Fig. 1 shows the calibration results. The electron and hole tunneling masses have been refined as $m_e$ = 0.11 and $m_h$ = 0.17, respectively. These values are adjusted to achieve best-fit between simulation and fully quantum simulation results in [20].

**Table 1 - Physical models used in the simulation**

| Physical Model | Description |
|---|---|
| Mobility | CVT: Enables transverse field, doping and temperature-dependent parts of mobility |
| Statistics | FERMI: To consider the highly doped regions, Fermi-Dirac statistics are adopted |
| Tunneling | BBT.NONLOCAL: The nonlocal BTBT model is used to consider the lateral tunneling through the channel. |
| Drift-Diffusion | Used for the transfer of holes and electrons |

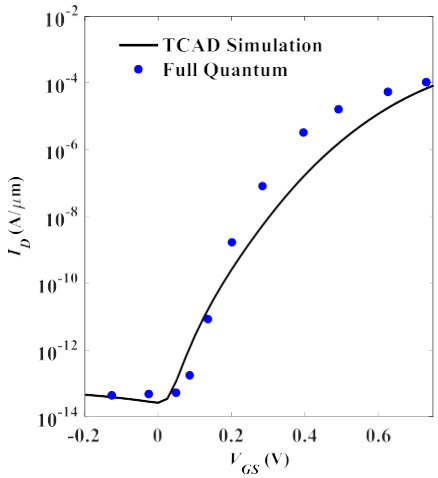
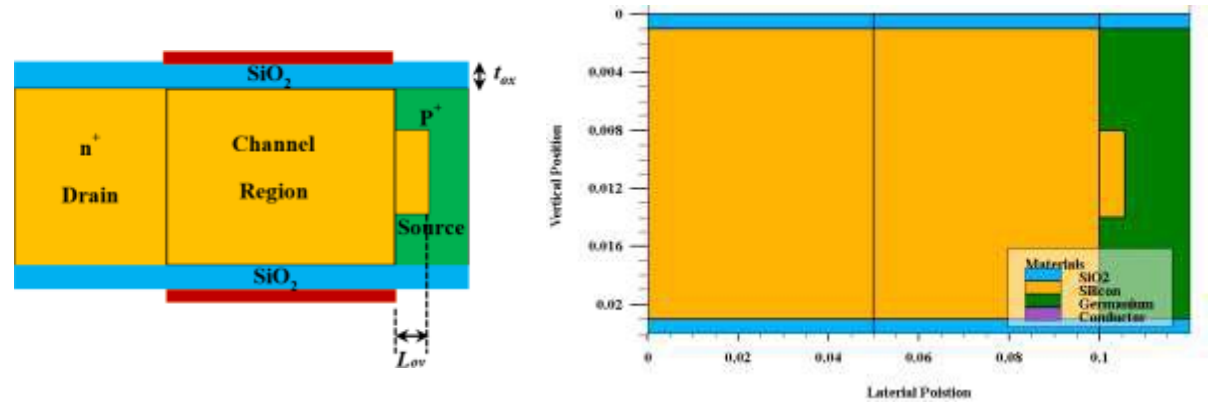



**Fig. 1 - TCAD model simulation calibrated vs the full quantum simulation in REF [20]**

A cross-sectional schematic of an n-type double gate (DG) TFET is shown in Fig. 2. The structure comprises a Ge $p^+$ source, Si intrinsic channel, and Si $n^+$ drain. All the junctions are assumed to be abrupt with uniform doping profiles. Further, in the proposed structure, the channel is extended into the source region with a length defined by $L_{ov}$. Fig. 2(a) presents the schematic diagram showing different regions and the design parameter $L_{ov}$. $L_{ov}$ affects the band bending at the interface between the source and channel regions and hence the tunneling rates. As a result, $L_{ov}$ has a direct influence on the electrical behavior of the transistor. Its value can be varied from 0 up to the source length. In the following simulation, $L_{ov}$ is varied from 0 (conventional case) to 16 nm.

The biasing conditions are $V_{DS}$ = 0.5V and $-0.2 < V_{GS} < 0.5$ V at $T$ = 300 K. The geometrical parameters and doping levels are listed in Table 2. A high doping concentration of $1\times10^{20}$ $cm^{-3}$ is adopted for the source region to enhance the tunneling current [21]. Meanwhile, the channel doping is low enough ($1\times10^{16}$ $cm^{-3}$) to produce a p-i-n configuration. Further, the drain doping is not so high to suppress the ambipolar current [22]. Its value is $1\times10^{18}$ $cm^{-3}$, which is relatively high, to ensure a drain electrode Ohmic contact [22]. The work function of the gate is taken to be 4.4 eV to ensure that the current starts to increase after $V_{GS}$ = 0 V [23]. Moreover, the gate oxide material used is $SiO_2$ (with dielectric constant = 3.9) whose thickness is $t_{ox}$ = 1 nm.




*a* *b*

**Fig. 2 - Proposed TFET device Structure (All dimensions are given in µm) (a) Schematic diagram showing different regions and the design parameter $L_{ov}$ and (b) Output structure from SILVACO device simulator**

**Table 2 - Main design parameters in device simulation**

| Parameter | Value |
|---|---|
| Source Length ($L_s$) | 20 nm |
| Channel Length ($L_{ch}$) | 50 nm |
| Drain Length ($L_d$) | 50 nm |
| Gate oxide thickness ($t_{ox}$) | 1 nm |
| Source doping (p-type) ($N_s$) | $1\times10^{20}$ $cm^{-3}$ |
| Drain doping (n-type) ($N_d$) | $1\times10^{18}$ $cm^{-3}$ |
| Channel doping (p-type) ($N_{ch}$) | $1\times10^{16}$ $cm^{-3}$ |
| Gate work function ($\Phi_g$) | 4.4 eV |

## 3. Simulation Results

In the following simulations, the overlap distance ($L_{ov}$) of the channel into the source is varied to inspect its influence on the device electrical behavior. Firstly, the nonlocal BTB tunneling rates are shown in Fig. 3 for two values of $L_{ov}$ (6 nm and 12 nm) compared to the conventional structure with no channel extension. It can be inferred that the proposed structure provides much higher rates than the conventional one (either for holes or electrons). These high tunneling rates indicate higher ON current when using the proposed structure.

Now, a comparison between the transfer characteristics of the conventional and proposed TFET for two values of $L_{ov}$ is shown in Fig. 4. It is observed that by increasing the overlap length, the ON current becomes higher. The ON current is doubled at $V_{GS}$ = 0.5 V and $L_{ov}$ = 12 nm. At the same time, the OFF current substantially remains constant, so the ON/OFF current ratio increases by the same factor when the overlapping increases. The results indicate that, at $L_{ov}$ = 12 nm, the ON current is about 2.5 of the conventional ON current at the ON state for which $V_{GS}$ = 0.5 V.

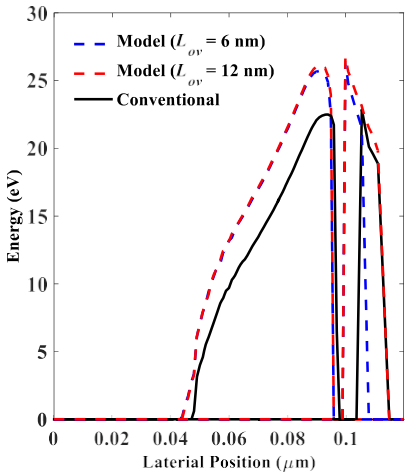



**Fig. 3 - BTB electron and hole tunneling rates for the proposed structure with different values of $L_{ov}$ (at $V_{DS}$ = 0.5 and $V_{GS}$ = 0.5 V)**

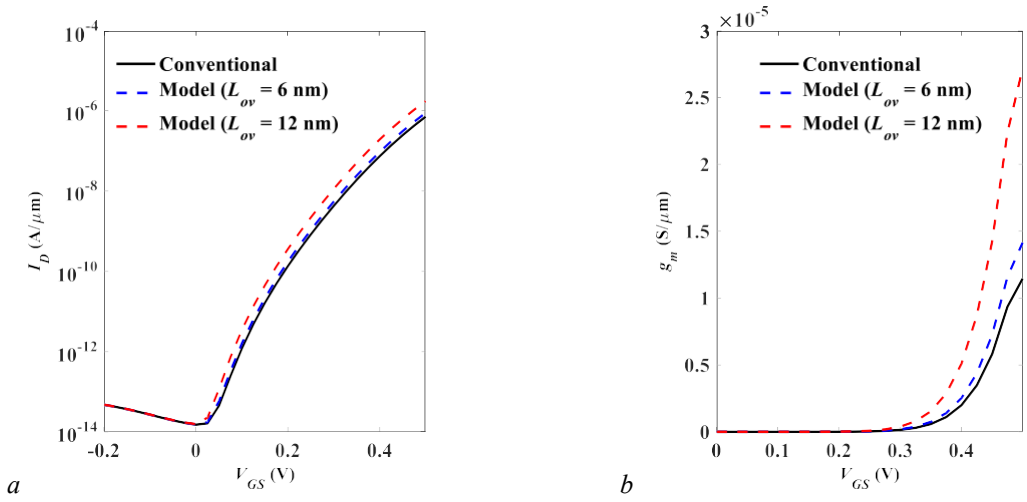



**Fig. 4 - Transfer characteristics of the conventional and proposed TFET structures with different overlap lengths at $V_{DS}$ = 0.5 V (a) log scale and (b) linear scale**

Next, the high-frequency parameters are inspected. The high-frequency performance is studied considering the transconductance ($g_m$) and gate capacitance ($C_{gg}$). Then, the unit gain cutoff frequency ($f_T$) is calculated based on the previous two parameters. Fig. 5(a) illustrates the variation of the intrinsic total gate capacitance ($C_{gg}$) of the proposed structure at $V_{DS}$ = 0.5 V. The result is compared with the gate capacitance of the conventional TFET structure. It is evident from the figure that $C_{gg}$ of the proposed structure is lowered with the increase of overlap length. When $L_{ov}$ = 12 nm, $C_{gg}$ is lowered by about 7% from its value for the conventional structure with no overlap (Given $V_{GS}$ = 0.5 V).

The transconductance is given by the rate of increase of the drain current with the gate-to-source voltage [24]. It can be formulated as,

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \tag{1}$$

The variation in transconductance is shown in Fig. 5(b). The proposed structure shows higher transconductance as compared to conventional TFET because of an increase in tunneling volume in the channel. Now, the cutoff frequency is approximated by the ratio of the transconductance to the total gate capacitance [25]. It can be given as,

$$f_T = \frac{g_m}{2\pi C_{gs}\sqrt{1+2C_{gd}/C_{gs}}} \approx \frac{g_m}{2\pi(C_{gd}+C_{gs})} = \frac{g_m}{2\pi C_{gg}} \quad (2)$$

Where $g_m$ is the transconductance and $C_{gg}$ is the overall gate capacitance. From the previous equation, $f_T$ is improved by increasing the transconductance and reducing the total gate capacitance [26, 27].

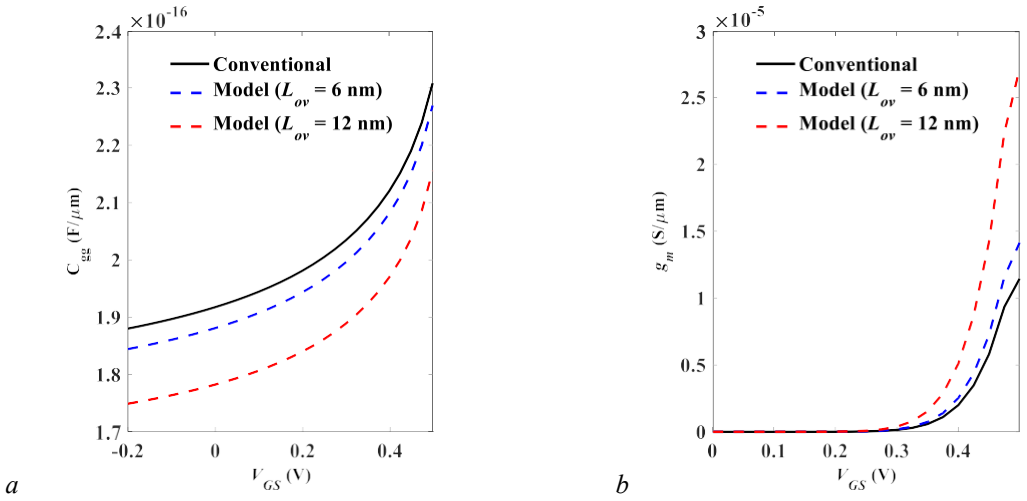



**Fig. 5 - (a) Variation of the intrinsic total gate capacitance and (b) transconductance as a function of gate voltage for the proposed structure (at $V_{DS}$ = 0.5 V)**

Fig. 6 shows the variation of the cutoff frequency of the proposed structure as a function of gate voltage at $V_{DS}$ = 0.5 V. The cutoff frequency of the proposed structure increases with the increase of $L_{ov}$. $f_T$ is increased by a factor of 2.7 at $V_{GS}$ = 0.5 V and $L_{ov}$ = 12 nm. This behavior is due to increasing the ratio of $g_m$ and $C_{gg}$ (as can be depicted from Fig. 5).

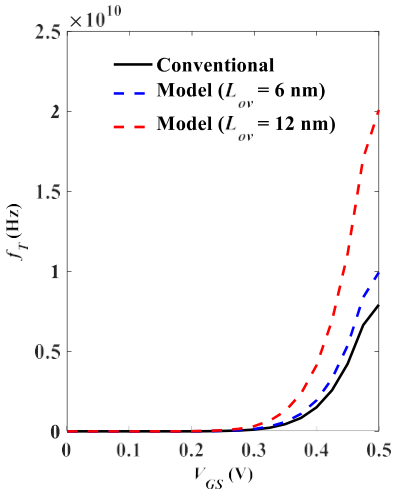



**Fig. 6 - Cutoff frequency variation vs gate voltage at $V_{DS}$ = 0.5 V**

## 4. Parametric Analysis

In order to design the proposed structure, we examine the variation of $L_{ov}$ from 6 nm to 16 nm to investigate the influence of the channel extension into the source. The main parameters studied to measure this impact are *SS*, $I_{ON}$ and $f_{Tmax}$. The *SS* can be defined as the gate voltage required to change the drain current by one decade. It can be determined as the inverse of the slope of the (log $I_D$) vs $V_{GS}$ curve in the subthreshold exponential region [28]. It can be formulated as,

$$SS = \frac{\partial V_{GS}}{\partial(\log I_D)} \tag{3}$$

Where the slope is determined by the partial differentiation of (log $I_D$) w.r.t. $V_{GS}$. Fig. 7(a) shows the *SS* variation with $L_{ov}$. As can be seen, *SS* decreases when increasing $L_{ov}$. So, there is an improvement in *SS* as a smaller *SS* leads to more improved dynamic performance. Moreover, Fig. 7(b) and Fig. 7(c) show an improvement in the ON current and the maximum cutoff frequency, $f_{Tmax}$, with increasing the overlapping length. By increasing the overlapping length from 6 nm to 16 nm, *SS* is decreased from 33 mV/decade to less than 30 mV/decade, $I_{ON}$ is increased from 1 µA/µm to 5 µA/µm and $f_{Tmax}$ is increased from 10 GHz to 65 GHz.

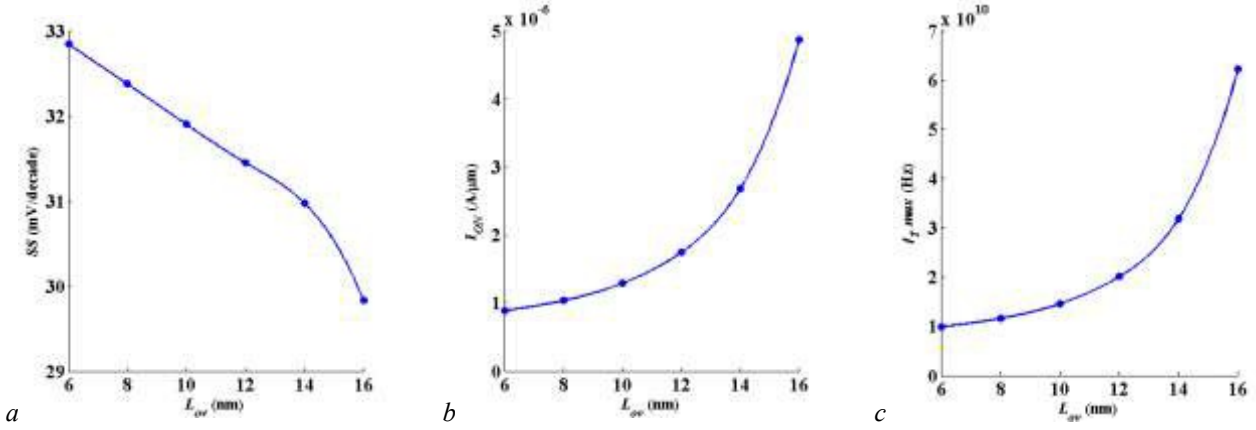



**Fig. 7 - Variation of performance parameters with $L_{ov}$ (at $V_{DS}$ = 0.5 V and $V_{GS}$ = 0.5 V): (a) sub-threshold swing, (b) ON current and (c) maximum cut-off frequency**

## 5. Conclusion

In this paper, by using 2D TCAD simulations, the impact of extending the channel into the Ge-source region of TFET has been studied to control the ON current while improving the high-frequency performance. It is demonstrated that by overlapping a part of the channel into the source region in a TFET, the ON current increases. In addition, the capacitance, transconductance and, in turn, the cutoff frequency are improved. By increasing the overlapping length, $L_{ov}$, from 6 nm to 16 nm, *SS* is decreased from 33 mV/decade to less than 30 mV/decade, $I_{ON}$ is increased by a factor of 5 and $f_{Tmax}$ is increased by a factor of 6.5. Based on this TCAD simulation study, the proposed structure could be used effectively for low power applications.

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