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Analysis of IG FINFET based N-Bit Barrel Shifter

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Abstract: This paper presents a new energy efficient N-bit barrel shifter using IG FinFET in 20 nm technology. The independent gate based FinFET device having more attractive features than standard CMOS technology. The proposed N-bit barrel shifter using independent gate FINFET device reduces the low power consumption over MOSFET and simulation results are performed using H spice software. In this work, it is presented the electrical analysis in terms of signal delay propagation and energy consumption of compacted barrel circuit for shifting operation.
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Keywords: FINFET, pass transistor, transmission gate, barrel shifter

1. Introduction

The independently connected gates control a channel act as circuit element and it is used for arithmetic systems. In general double gate device could be more scalable than the planar structures [1]. The standard FinFET used in integrated circuits is a double-gate or triple-gate structure, built over SOI or bulk substrates. The nature length of double gate device is shown in Equation (1)

$$\lambda = \sqrt{\frac{\epsilon_{si}}{2\epsilon_{ox}} t_{ox} t_{si}} \quad (1)$$

The physical dimensions are different from planar MOSFETs, because device width is proportional to silicon fin height [2].

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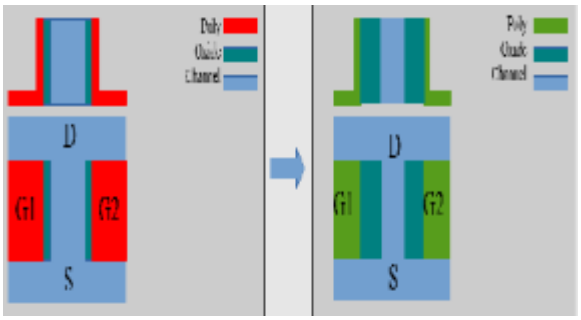

Fig. 1 - Independent Gate FinFET cross sections for Low V_{th} and High V_{th} transistors

Table 1 - Spice Parameters used for Electrical Simulation of IG FinFET [2]

Parameter	SPICE NAME	VALUE		DESCRIPTION
		Low V_{th}	High V_{th}	
$t_{ox\ 1,2}$	EOT 1, EOT 2	1 nm	2 nm	Effective oxide thickness
t_{si}	TSI	12 nm	8 nm	Silicon channel thickness
$\square_{ms\ 1,2}$	PHIG1,PHIG2	4.55 ev	4.85 ev	Gate Work Function
$L_{u\ D,S}$	LOVD	2 nm	5 nm	Gate/Drain Overlap
H_{FIN}	W	40 nm	40 nm	Fin Height
L	L	32 nm	32 nm	Gate Length

The Inv-Tx structure is more effective in terms of velocity saturation and process variability. The logical effort based delay model was derived using PTM model in H-spice [3]. The two different adiabatic logic families PFAL and PAL are incorporated in multiplexed based 4 bit barrel shifter [4]. The unique Vth modulation aspect of IG-FinFETs through selective gate bias is developed in this paper to enhance the barrel shifter performance while lowering the energy dissipation with minimum foot print of the chip [5]. The barrel shifter is combinational circuit and that is used in floating point adder and central processing unit [6].The barrel shifter is designed using CMOS logic. The high input impedance and load capacitances are disadvantages of CMOS logic. The pass transistor logic is introduced and it is used for area efficient n bit barrel shifter [7].The pass transistor network suffers from voltage swing and it is overcome by using level restorer and charge keeper circuits. The weak p-MOS it will act as restoring device [8]. The voltage degradation problem is overcome by using transmission gate for better noise margin. In transmission gate the number of active devices increases neither compared to PTL family. Transmission gate act as buffer and it is used for carbon nano tubes based VLSI interconnects [9]. In this work NOR based decoder using IG FINFET it is consider for N-it barrel shifter. The merit of NOR based decoder is used in microprocessor and it reduces the leakage power dissipation nearly 12% [10]. The leakage controlling transistor using FINFET technology saves 60 % at 14 nm technology node. The intermediate nodes are responsible for leakage control and it is further tested with four input NAND gate as bench mark circuit [11].The independent four terminal device is shown in figure 2.

Mode	N-Type	P-Type
Low V_{th} IG		
Low V_{th} SG		
High V_{th} IG		

Fig. 2 - Symbol Representation of FinFET

2. Conventional Barrel Shifter Circuit

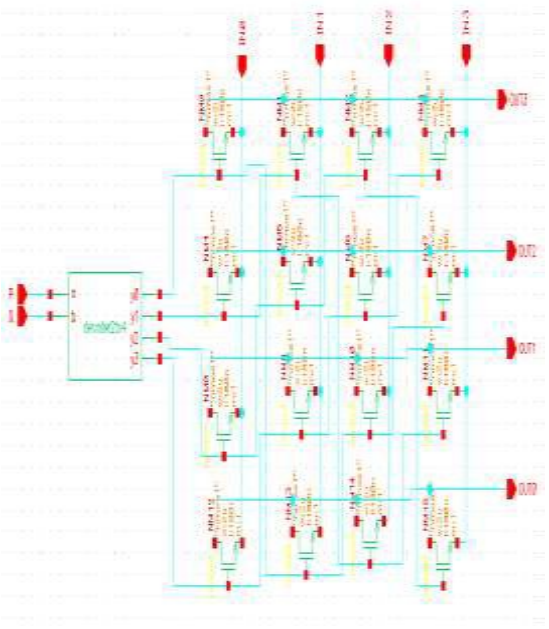

Fig. 3 - n-bit barrel shifter circuit using pass

The figure 3 shows the barrel shifter using pass transistor logic. The n bit barrel shifter consists of n bit decoder and switches. The n bit decoder is used for appropriate shifting based on the inputs to the output. The pass transistor network is affected from sneak path.

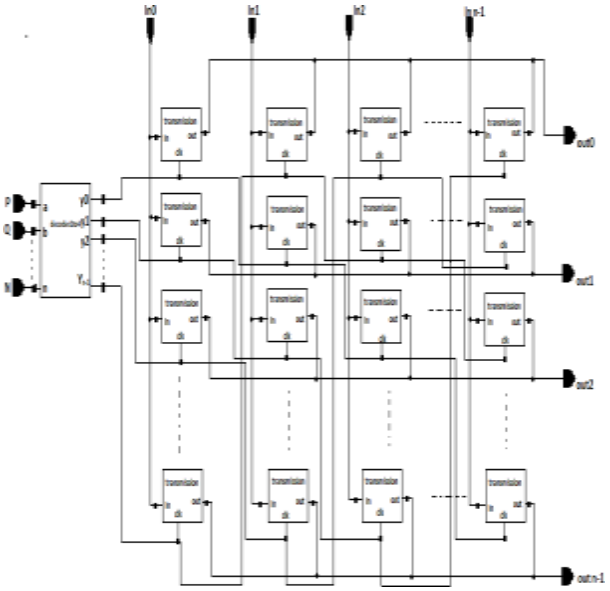

Fig. 4 - n-bit barrel shifter circuit using transmission gate

The figure 4 shows the transmission gate based n-bit barrel shifter circuit. The drawback of sneak path in pass transistor network is overcome by using transmission gate. The TG based rotator circuit increases the number of transistor compared to PTL based rotator circuit. The transmission gate is gives better noise immunity and it is used as driving stage of arithmetic systems.

3. Proposed N-Bit Barrel Shifter Circuit Using Finfet

The n bit barrel shifter circuit is constructed from NOR based decoder for high speed application. The NOR based decoder having better switching characteristics than NAND based decoder circuits. The figure 5 has shown the schematic of NOR based decoder.

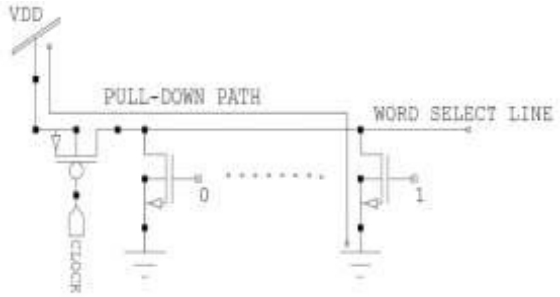

Fig. 5 - Schematic of NOR based decoder

The design of 3:8 decoder using IG FinFET is shown in figure 6.

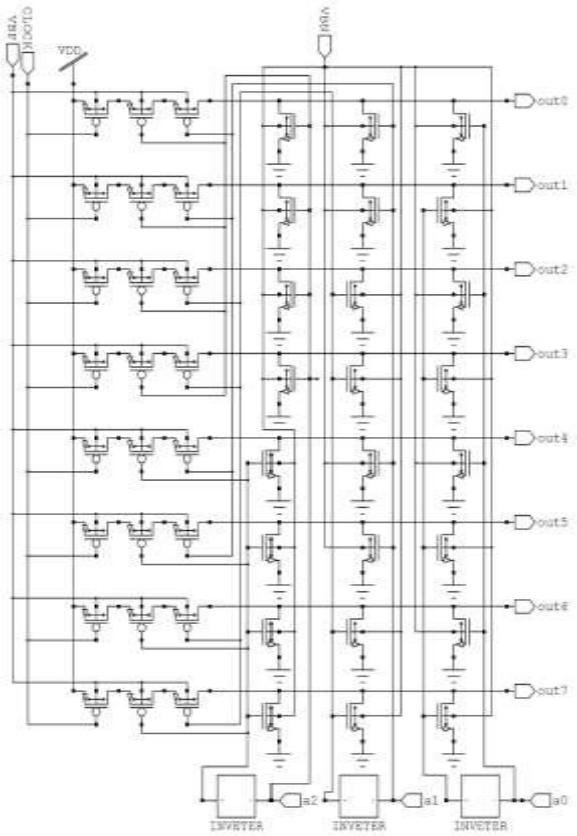

Fig. 6 - NOR based 3:8 decoder using IGFinFET [10]

The figure 7 shows the n bit barrel shifter circuit. The appropriate shifting is performed using IG FinFET based decoder. The decoder is used to select the minterms and the corresponding word line and bit line are asserted and remaining lines are disserted.

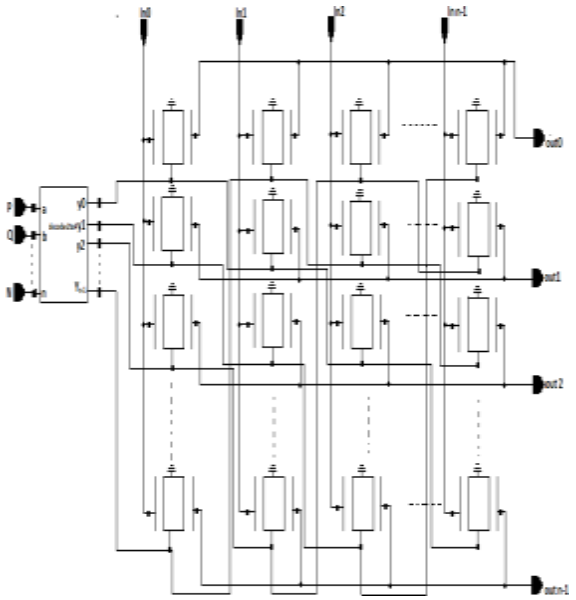

Fig. 7 - Proposed N-Bit Barrel Shifter using IG FinFET

4. Results and Discussion of Proposed System Using Ig Finfet

The variations in the temperature will also affect the performance of the circuit. This proposed system was designed under ambient conditions and mostly performed in the range of room temperature. Decoder is a circuit which converts n-bit binary data into m-level output lines. The pass transistors cells in a matrix with the use of decoder consume less amount of power and have a delay in Nano seconds. The transmission gate logic is used to solve the voltage drop problem in the pass transistor logic. The conventional method uses two designs and provides delay in Nano seconds and power is in micro watts.

Table 2 - Power delay product of proposed 2x4 decoder using IGFINFET system

Design	Power (Watts)	Delay (Sec)	Power delay product
2x4 decoder using conventional method	86.92×10^{-6}	1.59×10^{-9}	1.3820×10^{-13}
2x4 decoder using IGFINFET	**62.06×10^{-6}**	**0.96×10^{-9}**	**5.95776×10^{-14}**

Table 2 shows the comparision of simulation results of conventional 2 X 4 decoder with 2 X 4 decoder using IGFINFET. The proposed system results better power consumption than existing conventional techniques. The proposed system has utilizsed 28.6% less power, 39.6% less delay and shows efficiency of 99.5% in terms of power delay product.

Table 3 - Description of power delay product of 3x8 decoder using conventional method with proposed system

Design	Power (Watts)	Delay (Sec)	Power delay product
3x8 decoder using Conventional method	73.78×10^{-6}	13.287×10^{-9}	9.8031×10^{-13}
3x8 decoder using IGFINFET	**97.01×10^{-6}**	**10.249×10^{-9}**	**9.9425×10^{-13}**

Table 3 shows the comparision of simulation results of conventional 3 X 8 decoder with 3 X 8 decoder using IGFINFET. The proposed system results better power consumption than existing conventional techniques. The proposed system has utilizsed 31.4% more power, 22.86% less delay and shows efficiency of 89.69% in terms of power delay product. Well by comparing the 2x4 decoder IGFINFET simulation results with 3x8 decoder IGFINFET the power consumption and delay is less for 3x8 decoder.

Table 4 - Description of power delay product of 4x16 decoder using conventional method with proposed system

Design	Power (Watts)	Delay (Sec)	Power delay product
4x16 decoder using conventional method	105.7×10^{-6}	26.442×10^{-9}	2.7949×10^{-12}
4x16 decoder using IGFINFET	**82.63×10^{-6}**	**22.646×10^{-9}**	**1.8712×10^{-12}**

Table 4 shows the comparision of simulation results of conventional 4 X 16 decoder with 4 X 16 decoder using IGFINFET. The proposed system results better power consumption than existing conventional techniques. The proposed system has utilizsed 21.82% less power, 14.355% less delay and shows efficiency of 32.97% in terms of power delay product. When 2x4, 3x8 decoder simulation results are compared with 4x16 the delay is completely reduced and also power delay product provides high efficiency.

Table 5 - Power delay product proposed 4 bit barrel shifter using IGFINFET system

Design	Power (Watts)	Delay (Sec)	Power delay product
4 bit Barrel shifter using transmission gate	78.74×10^{-6}	26.05×10^{-12}	2.051×10^{-15}
4 bit Barrel shifter using pass transistor logic	35.87×10^{-6}	38.84×10^{-12}	1.393×10^{-15}
4 bit Barrel shifter using IGFINFET	**22.67×10^{-6}**	**14.65×10^{-12}**	**3.321155×10^{-16}**

Table 5 shows the comparision of simulation results of 4 bit barrel shifter using transmission gate, pass transistor logic with 4 bit Barrel shifter using IGFINFET. The proposed system results better power consumption than existing conventional techniques. The Barrel shifter using transmission gate simulation results are compared with IGFINFET Barrel shifter and this proposed system has utilizsed 71.22% less power, 43.761% less delay and shows efficiency of 83.80% in terms of power delay product. Next the 4 bit Barrel shifter with pass transistor logic is compared with IGFINFET Barrel shifter and this proposed system has utilizsed 36.79% less power, 62.28% less delay and shows efficiency of 76.166% in terms of power delay product. 4 bit Barrel shifter using IGFINFET has less delay in terms of transmission gate and pass transistor logic circuits.

Table 6 - Power delay product proposed 8 bit barrel shifter using IGFINFET system

Design	Power (Watts)	Delay (Sec)	Power delay product
8 bit Barrel shifter using transmission gate	93.21×10^{-6}	11.073×10^{-9}	1.0321×10^{-12}
8 bit Barrel shifter using pass transistor logic	49.17×10^{-6}	11.057×10^{-9}	5.436×10^{-13}
8 bit Barrel shifter using IGFINFET	**36.45×10^{-6}**	**9.013×10^{-9}**	**3.2852×10^{-13}**

Table 6 shows the comparision of simulation results of 8 bit barrel shifter using transmission gate, pass transistor logic with 8 bit Barrel shifter using IGFINFET. The proposed system results better power consumption than existing conventional techniques. The Barrel shifter using transmission gate simulation results are compared with IGFINFET Barrel shifter and this proposed system has utilizsed 60.89% less power, 18.60% less delay and shows efficiency of

68.16% in terms of power delay product. Next the 8 bit Barrel shifter with pass transistor logic is compared with IGFINFET Barrel shifter and this proposed system has utilizsed 25.86% less power, 18.45% less delay and shows efficiency of 93.966% in terms of power delay product. This proposed system has highest power delay product when compare to all decoder designs and also 4 bit Barrel shifter IGFINFET logic.

Table 7 - Power delay product proposed 16 bit barrel shifter using IGFINFET system

Design	Power (Watts)	Delay (Sec)	Power delay product
16 bit Barrel shifter using transmission gate	551×10^{-6}	23.63×10^{-9}	1.30230×10^{-11}
16 bit Barrel shifter using pass transistor logic	307×10^{-6}	17.009×10^{-9}	5.2217×10^{-12}
16 bit Barrel shifter using IGFINFET	**213×10^{-6}**	**15.66×10^{-9}**	**3.3355×10^{-12}**

Table 7 shows the comparison of simulation results of 16 bit barrel shifter using transmission gate, pass transistor logic with 16 bit Barrel shifter using IGFINFET. The proposed system results better power consumption than existing conventional techniques. The Barrel shifter using transmission gate simulation results are compared with IGFINFET Barrel shifter and this proposed system has utilized 61.34% less power, 33.728% less delay and shows efficiency of 74.27% in terms of power delay product. Next the 16 bit Barrel shifter with pass transistor logic is compared with IGFINFET Barrel shifter and this proposed system has utilized 30.61% less power, 7.93% less delay and shows efficiency of 36.122% in terms of power delay product. The 16 bit Barrel shifter IGFINFET has high efficiency of power delay product when compare to pass transistor logic, and transmission gate output simulation results. Figure 8 and 9 shows the simulation results of pass transistor and transmission gate. The input patterns are applied to stimuli to check the performance of the barrel shifter. By using transient analysis the full swing voltage is achieved.

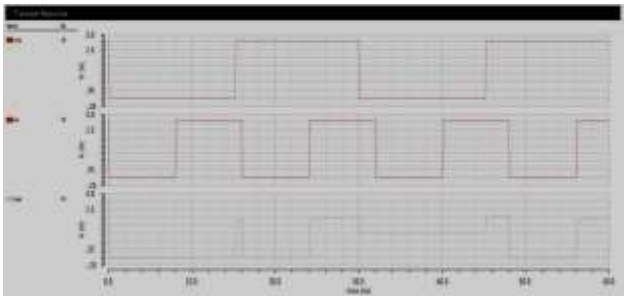

Fig. 8 - Simulation result of barrel shifter using pass transistor logic

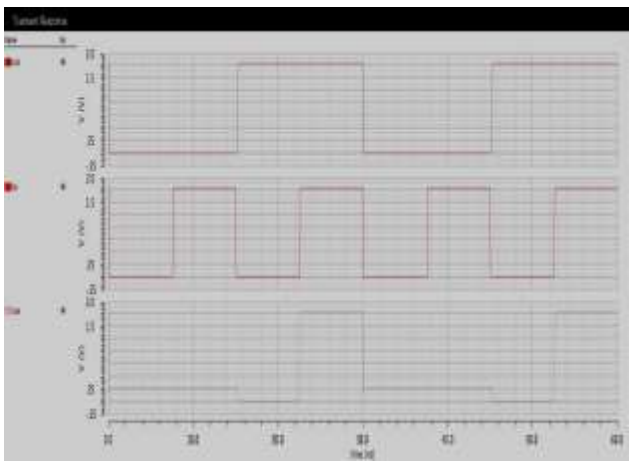

Fig. 9 - Simulation result of barrel shifter using transmission gate logic

5. Conclusions

In this paper, independent gate FinFET was explored, the variation of its low V_{th} in function of the back gate bias, which is meets the design aspects of low power circuits. The results are compared with the conventional methods with power delay product. The 2x4 decoder has 99.5%, whereas 3x8 decoder has 89.75%, 4x16 decoder has 32.97% power delay product efficiency using IGFINFET technology when compared to conventional method. The 4-bit, 8-bit, 16-bit Barrel shifter are designed using IGFINFET technology has efficiencies of 83.80%, 68.6%, 74.27% power delay products when compared to transmission gate barrel shifter logic. Similarly, the power delay efficiencies are 76.166%, 93.966%, 36.122% when compared to pass transistor logic.

References

[1] Hisamoto, D., Lee, W. C., Kedzierski, J., Takeuchi, H., Asano, K., Kuo, C.,... & Hu, C. (2000). FinFET-a self-aligned double-gate MOSFET scalable to 20 nm. IEEE Transactions on Electron Devices, 47(12), 2320-2325.

[2] Fossum, J. G., & Trivedi, V. P.(2013). Fundamentals of Ultra-thin-body MOSFETs and FinFETs. Cambridge University Press.

[3] Sharma, A., Alam, N., Chawla, R., & Anand, B.(2018) Modeling the effect of variability on the timing response of CMOS inverter-transmission gate structure. In 2018 International Symposium on Devices, Circuits and Systems (ISDCS), IEEE. 1-5.

[4] Anantharaman K., Manikandan A.V.M. (2018).Adiabatic Techniques for Energy-Efficient Barrel Shifter Design. In: Li J., Sankar A., Beulet P. (eds) VLSI Design: Circuits, Systems and Applications. Lecture Notes in Electrical Engineering, vol 469. Springer, Singapore .

[5] Raja, G. B., Madheswaran, M.(2013). Design and performance comparison of 6-T SRAM cell in 32nm CMOS, FinFET and CNTFET technologies. International Journal of Computer Applications.70 No 21.

[6] Nuriddin Safoev and Jun-Cheol Jeon.(2017). Area Efficient QCA Barrel Shifter. Advance and Science Technology Letters,144, 51-57.

[7] Mitra, S. K., & Chowdhury, A. R.(2015). Optimized logarithmic barrel shifter in reversible logic synthesis. In VLSI Design (VLSID), 2015 28th International Conference on 441-446, IEEE.

[8] Nehru, K., Shanmugam, A., & Thenmozhi, G. D.(2012). Design of low power ALU using 8T FA and PTL based MUX circuits. In Advances in Engineering, Science and Management (ICAESM), 2012 International Conference on 145-149, IEEE.

[9] Karthikeyan, A., & Mallick, P. S.(2018). Transmission Gate as Buffer for Carbon-Nanotube-Based VLSI Interconnects.IETE Journal of research, 64(2), 296-305.

[10] Chaturvedi, M., Bhadoria, A., Mahor, V., & Pattanaik, M.(2016). FinFET-Based Low Power Address Decoder under Process Variation. In Nanoelectronic and Information Systems (iNIS), 2016 IEEE International Symposium on 274-277, IEEE.

[11] Dadoria, A. K., Khare, K., Gupta, T. K., & Khare, N.(2017). Integrating sleep and pass transistor logic for leakage power reduction in FinFET circuits. Journal of Computational Electronics, 16(3), 867-874.