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Characterization of a 0.14 μm Submicron NMOS with Silvaco TCAD Simulator

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Abstract

A 0.14 μm NMOS was simulated using ATHENA and ATLAS modules from TCAD simulator. The electrical characteristics of the submicron device were studied. Constant field scaling was applied to the following parameters: the effective channel length, the density of the ion implantation for threshold voltage (VTH) adjustment, and the gate oxide thickness (TOX). Additional techniques implemented to avoid short channel effects in submicron devices were shallow trench isolation (STI), sidewall spacer deposition, lightly doped drain (LDD) implantation, and retrograde well implantation. The results show that retrograde well implantation allowed the highest density of the dopant to fall below the surface of the substrate. With the application of sidewall spacer and LDD implantation, a lighter doped region was created beyond the n+ drain/source junction. As the layers of metallization increases, it was observed that drain current (ID) increased as well. The important parameters for NMOS were measured and validated.

Keywords: sidewall spacer, LDD, retrograde well, metallization

1 INTRODUCTION

The density of a chip in MOS VLSI (Very Large Scale Integration) has been growing tremendously for the past few decades. One of the reasons is due mainly to size reduction of a transistor.

Starting off with 50 μm in the 1960s, the gate channel of a transistor has shrunk to less than 0.18 μm in 2000 (Hong Xiao 2001). In this paper, a 0.14 μm NMOS was simulated and studied. The device fabrication process was first simulated using the ATHENA module from the Silvaco Virtual Wafer Fab (VWF) TCAD tools. The electrical properties were then validated with the ATLAS module.

The performance of a 0.14 μm NMOS, which falls within the submicron regimes, may be severely affected by short channel effects. Thus, besides applying constant field scaling on the effective channel length (Lg), gate oxide thickness (TOX), and threshold voltage (VTH) adjust implantation, additional fabrication techniques have been implemented. Shallow Trench Isolation (STI), sidewall spacer deposition, Lightly Doped Drain (LDD) implantation, and retrograde well implantation were some of the techniques applied to ensure proper operation of the device (Slisher et al. 2006).

2 SIMULATION PROCESS WALKTHROUGH

The simulation process can be classified into 5 different phases. They are well formation, device isolation, transistor making, and interconnection (Hong Xiao 2001).

Initially, a p well is to be formed in the p-type single crystal silicon (Si) wafer. Screen oxide is grown on the surface of the substrate. This is followed by a high energy implantation. The wafer is tilted and rotated when the implantation process is performed.

The objective of growing a layer of screen oxide and tilting the wafer is to minimize channeling effect; whereas, rotating the wafer is to minimize shadowing effect. Soon after p well is formed, annealing and drive-in is performed to repair the lattice damage (Hong Xiao 2001).

Next, STI is employed to isolate neighbouring devices. A layer of pad oxide is first grown via dry oxidation. Silicon Nitride (Si3N4) is then deposited using Liquid Plasma Chemical Vapor Deposition (LPCVD). Pad oxide acts as a stress buffer which avoids cracks on Si3N4; whereas, Si3N4 acts as a mask for etching. Photoresist is deposited and photolithography is applied to define the active region of the device. Subsequently, Si3N4 and pad oxide are etched. After the photoresist is stripped, Reactive Ion Etching (RIE) is implemented to form trenches at the 2 sides of the active region. A thin layer of barrier oxide is grown in the trenches. The trenches are filled up with oxide using

Tetra-Ethyl-Oxy-Silane (TEOS) CVD process. The layer of barrier oxide prevents impurities from diffusing into the substrate during TEOS CVD process (Hong Xiao 2001). The oxide at the surface of the substrate is removed using Chemical Mechanical Polishing (CMP) process. STI is completed after annealing is performed and Si3N4 mask and pad oxide are etched.

Gate oxide is grown via dry oxidation. VTH adjust implantation is then performed, after which, the substrate undergoes annealing. Next, polysilicon gate is formed by depositing and etching a layer of polysilicon. The substrate is, again, annealed. LDD is then implanted to suppress hot electron effect (Hong Xiao 2001). Subsequently, Si3N4 is deposited via CVD process. Sidewall spacers are formed by etching the Si3N4 film. Source and drain junctions are implanted on the 2 sides of the active regions and annealing process is applied to activate the dopants. As soon as the basic structure of an NMOS is completed, a layer of titanium is deposited on the substrate surface. Rapid Thermal Annealing (RTA) is then employed to form silicide on the gate. A transistor is fabricated soon after the unreacted titanium is etched.

Interconnections in between transistors are to be performed with metallization. A layer of Boron Phosphor Silicate Glass (BPSG) is first deposited to form Premetal Dielectric (PMD). PMD acts as an insulator for multilevel interconnection (Quirk 2001). After annealing, BPSG is etched to form source/drain contacts. The first level of metallization is developed by depositing and etching aluminum (Al) on the contacts. An almost similar procedure is to be performed on the second level of interconnection. Another layer of BPSG, known as Intermetal Dielectric (IMD) (Quirk 2001) is deposited. The simulation process is completed when the redundant IMD is etched. A summary of the parameters used in NMOS fabrication is shown in Table 1.

3 SIMULATION RESULTS AND DISCUSSION

A. The 0.14 µm NMOS

Figure 1 shows the complete cross section of NMOS. As clearly shown by the dopant density distributions, retrograde well technique has resulted in the highest dopant density concentrated a certain depth below the surface of the substrate. It can also be observed that, LDD implantation formed a relatively lighter n doped region right beneath the sidewall spacers.

B. Retrograde Well

As compared to conventional well formation, in which, the highest dopant density lies at the surface of the substrate, retrograde wells use high energy implantation to place the highest dopant density at a certain desired substrate

depth. Figure 2 shows the boron concentration versus the substrate depth of the simulated 0.14 μm NMOS.

Table I Parameters in NMOS Fabrication.

Process Step	NMOS Parameters
Si substrate	• 7.0×10^{14} cm^{-3} Boron
	• <100> orientation
Retrograde well	• 0.02 μm screen oxide
	• 3.75×10^{12} cm^{-3} Boron
	• 100 keV implant energy
	• 7° tilt
	• 30 min, 900°C annealing
	• 36 min, 970°C drive-in
STI	• 0.01 μm pad oxide
	• 0.15 μm Silicon Nitride
	• 0.50 μm trench depth
	• 15 min, 900°C annealing
Gate oxide	• 0.034 μm gate oxide
V_{TH} adjust	• 12.45×10^{17} cm^{-3} Boron
	• 5 keV implant energy
Poly gate	• 0.25 μm polysilicon
	• 26 min, 850°C annealing
LDD	• 1×10^{13} cm^{-3} Phosphorous
	• 23 keV implant energy
	• 20 min, 800°C drive-in
Spacer	• 0.12 μm Silicon Nitride
Source/drain	• 1×10^{15} cm^{-3} Arsenic
	• 2×10^{15} cm^{-3} Phosphorous
	• 25 keV implant energy
	• 55 min, 800°C, 850°C, 900°C annealing
Silicide	• 0.12 μm Titanium
	• 0.02 min, 1100°C RTA
	• 0.1 min, 910°C annealing
PMD	• 0.30 μm BPSG
	• 20 min, 850°C annealing
Metal 1	• 0.10 μm Aluminum
IMD	• 0.30 μm BPSG
	• 15 min, 950°C annealing
Metal 2	• 0.30 μm Aluminum

As the channel length reduces, the depletion region encompasses the drain junction tends to extends farther towards the source. At a time, if the depletion regions of both drain and source junctions merge, a spurious current path is inevitably formed. The gate voltage will have lost its control over the current flow in between the 2 junctions. Such phenomenon is known as punch through (Sze 1988).

An increase of doping concentration in the substrate using retrograde well implantation allows the depletion regions drain/source junctions to be scaled down. Hence, punch through can be avoided when the depletion regions stay at a reasonable distance apart.

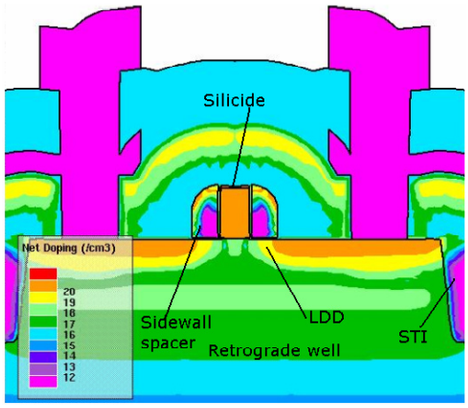

Figure 1. 0.14 µm NMOS.

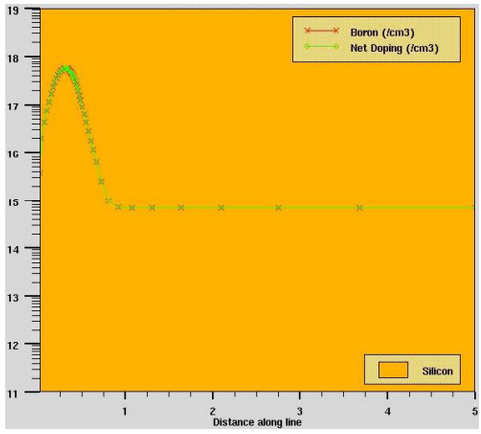

Figure 2. Boron density versus substrate depth of a 0.14 µm NMOS.

C. LDD Implantation

When the dimension of the device shrinks and the supply voltage remain constant, the electric field generated in the substrate will increase. As a result, the electrons along the channel might gain sufficient energy to be injected onto the gate oxide. The charging of the gate oxide causes long term degradation on the device. Such issue is known as "hot electron effect" (Sze 1988).

In order to avoid the electrons from gaining sufficient energy, the electric field along the drain region is to be reduced. One way of doing so is to implant a lighter n dopant surrounding the n+ drain/source implants. As shown in Figure 3, the net doping of LDD implantation beneath the sidewall spacers is relatively shallow compared to the drain/source implants.

D. NMOS Parameters

Important parameters such as VTH, TOX, and Lg are measured and extracted from the ATLAS module. The parameters are compared with the standard parameters published by International Technology Roadmap for Semiconductor (ITRS) and Berkeley Predictive Technology Model (BPTM) (Berkeley 2006). Since only the standard parameters for 70 nm, 0.10 µm, 0.13 µm, and 0.18 µm NMOS device were published in ITRS and BPTM, polynomial regression technique (using MATLAB tools) was applied to acquire the required parameters for a 0.14 µm NMOS. Table 2 shows a comparison between the parameters extracted from ATLAS and the standard parameters obtained using polynomial regression. It can be observed that the parameters extracted from the ATLAS module fall within the tolerance range of the standard parameters obtained through regression technique. Therefore, the simulation results are validated.

E. Electrical Characteristics

The ID-VD and ID-Vg electrical characteristics curves were plotted using ATLAS module.

Figure 4 and 5 shows the NMOS ID-VD relationships before and after metallization 2; whereas, Figure 6 and 7 shows the NMOS ID-Vg relationships before and after metallization 2. The differences in ID before and after second level interconnection were compared. The results are summarized in Table 3 and 4.

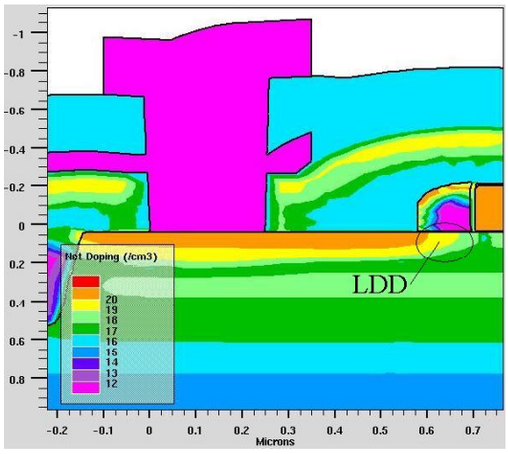

Figure 3. LDD Implantation.

Table 2 Comparison between Simulated Results and Standard Parameters for A 0.14 µM NMOS.

	Parameters	ATLAS Results	Standard Parameters
NMOS	V_{TH}	0.343138 V	0.3424 ± 12.7% V
	T_{OX}	3.46138 nm	3.2158 ± 4% nm
	L_g	0.133 µm	0.14 ± 15% µm

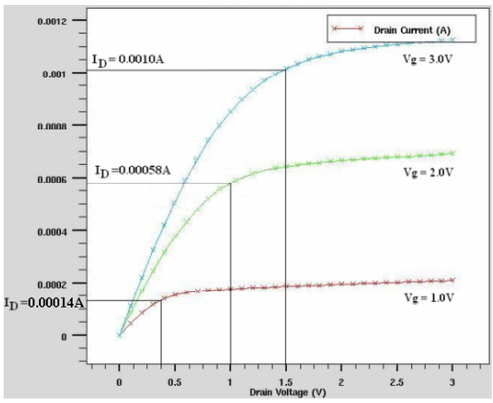

Figure 4. NMOS ID-VD relationship before metallization 2 is deposited.

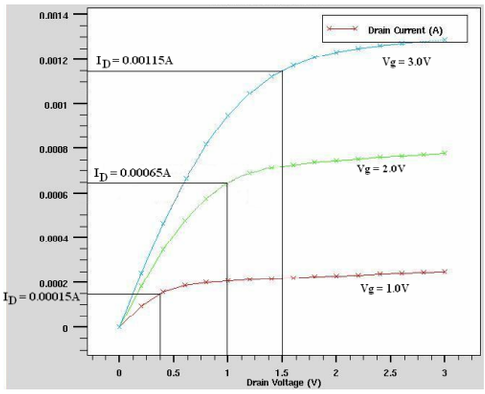

Figure 5. NMOS ID-VD relationship after metallization 2 is deposited.

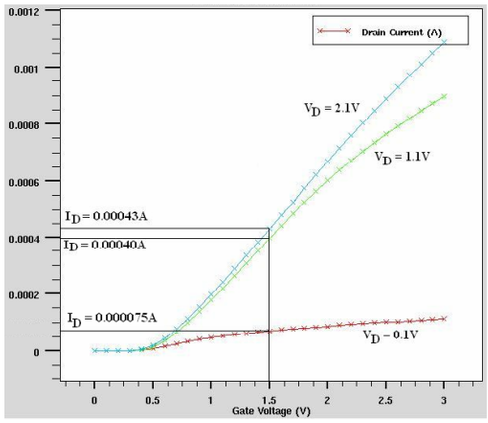

Figure 6. NMOS ID-Vg relationship before metallization 2 is deposited.

As can be seen from Figure 4 to Figure 7, the current- voltage characteristic curves remain unchanged even though a second layer of metallization has been deposited onto the device.

Nevertheless, ID increases after metallization 2. Since power consumption is directly proportional to ID, the simulation shows that by increasing the level of metallization, power consumption tend to increase as well.

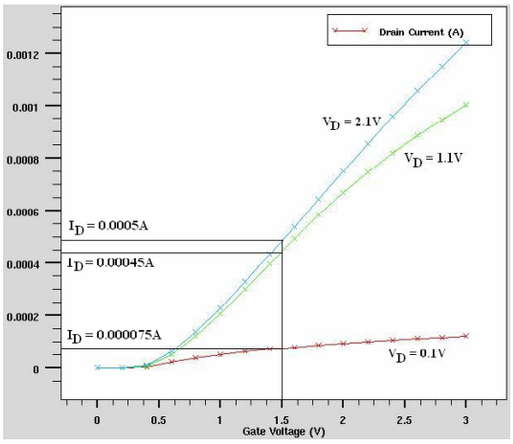

Figure 7. NMOS ID-Vg relationship after metallization 2 is deposited.

Table 3 Comparison of Id before and after Level 2 Metallization in Id-Vd NMOS Graph.

V_g	V_D	I_D before level 2 interconnection	I_D after level 2 interconnection	Rate of Increase in I_D
1.0 V	0.375 V	0.00014 A	0.00015 A	7.14%
2.0 V	1.0 V	0.00058 A	0.00065 A	12.07%
3.0 V	1.5 V	0.00100 A	0.00115 A	15.00%

Table 4 Comparison of Id before and after Level Metallization in Id-Vg NMOS Graph.

V_g	V_D	I_D before level 2 interconnection	I_D after level 2 interconnection	Rate of Increase in I_D
1.5 V	0.1 V	0.000075 A	0.000075 A	0%
1.5 V	1.1 V	0.000400 A	0.000450 A	12.50%
1.5 V	2.1 V	0.000430 A	0.000500 A	16.28%

4 CONCLUSION

A 0.14 µm submicron NMOS has been successfully simulated and validated. The result shows that retrograde well technique controls the highest concentration dopant at certain depth of the substrate; whereas, LDD implantation reduces the concentration of n dopant beneath the sidewall spacers. These techniques are effective in minimizing short channel effects. The current-voltage characteristic curves also show that as the level of interconnection increases, ID increases as well which should result in higher power consumption.

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