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To the Graduate Council:

I am submitting herewith a dissertation written by Ren Ren entitled "Modeling and Optimization Algorithm for SiC-based Three-phase Motor Drive System." I have examined the final electronic copy of this dissertation for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Doctor of Philosophy, with a major in Electrical Engineering.

Fred Wang, Major Professor

We have read this dissertation and recommend its acceptance:

Leon Tolbert, Daniel Costinett, Zheyu Zhang

Accepted for the Council:

Dixie L. Thompson

Vice Provost and Dean of the Graduate School

(Original signatures are on file with official student records.)

Modeling and Optimization Algorithm for SiC-based Three-phase Motor Drive System

A Dissertation Presented for the

Doctor of Philosophy

Degree

The University of Tennessee, Knoxville

Ren Ren

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Abstract

More electric aircraft (MEA) and electrified aircraft propulsion (EAP) becomes the important topics in the area of transportation electrifications, expecting remarkable environmental and economic benefits. However, they bring the urgent challenges for the power electronics design since the new power architecture in the electrified aircraft requires many benchmark designs and comparisons. Also, a large number of power electronics converter designs with different specifications and system-level configurations need to be conducted in MEA and EAP, which demands huge design efforts and costs. Moreover, the long debugging and testing process increases the time to market because of gaps between the paper design and implementation.

To address these issues, this dissertation covers the modeling and optimization algorithms for SiC-based three-phase motor drive systems in aviation applications. The improved models can help reduce the gaps between the paper design and implementation, and the implemented optimization algorithms can reduce the required execution time of the design program.

The models related to magnetic core based inductors, geometry layouts, switching behaviors, device loss, and cooling design have been explored and improved, and several modeling techniques like analytical, numerical, and curve-fitting methods are applied. With the developed models, more physics characteristics of power electronics components are incorporated, and the design accuracy can be improved.

To improve the design efficiency and to reduce the design time, optimization schemes for the filter design, device selection combined with cooling design, and system-level optimization are studied and implemented. For filter design, two optimization schemes including A_p based weight prediction and particle swarm optimization are adopted to reduce searching efforts. For device selection and related cooling design, a design iteration considering practical layouts and switching speed is proposed. For system-level optimization, the design algorithm enables the evaluation of different topologies, modulation schemes, switching frequencies, filter configurations, cooling methods, and paralleled converter structure. To reduce the execution time of system-level optimization, a switching function based simulation and waveform synthesis method are adopted.

Furthermore, combined with the concept of design automation, software integrated with the developed models, optimization algorithms, and simulations is developed to enable visualization of the design configurations, database management, and design results.

Table of Contents

Chapter One Introduction 1

1.1 Application Background 1

1.2 Research Motivations and Challenges 4

1.2.1 Modeling 8

1.2.2 Design Approach and Optimization 9

1.2.3 Design Automation 13

1.3 Proposed Model-Data-Optimization Framework for Power Electronics Design 13

1.4 Dissertation Layout 15

Chapter Two Literature Review 18

2.1 Power Semiconductors Modeling 18

2.1.1 Switching Behavior Model 19

2.1.2 Device Loss Model 22

2.1.3 Thermal Model for Power Devices 25

2.2 Passive Components Modeling in Power Electronics 27

2.2.1 Magnetics Core Inductor 28

2.2.2 Capacitor 37

2.2.3 Heatsink and Fan 40

2.2.4 Busbar and PCB Layout 41

2.3 Design Optimization in Power Electronics Design 43

2.3.1 Optimization Algorithm Review 44

2.3.2 Local Optimization for a Specific Trade-off Design Problem 49

2.3.3 Global Optimization of Whole Power Stage Design 51

2.4 Summary 59

Chapter Three Filter Design Optimization Considering Non-linear Physics Characteristics 62

3.1 Impacts of Current-bias Dependent Permeability on EMI filter Design 62

3.1.1 Investigation of Current-bias Dependent Permeability of DM Cores 63

3.1.2 Variable Inductor Model with Considering Current-bias Dependent Permeability 66

3.1.3 Study of Induced Unbalanced DM Impedance and Mixed-mode Noise 68

3.1.4 Design Algorithm with Consideration of Current-bias Dependent Permeability 71

3.1.5 Experimental Verification 72

3.2 Impedance-based CM Inductor Design Approach Considering Frequency-dependent and Imaginary Permeability 78

3.2.1 Characteristics of Frequency-dependent Permeability for CM Cores 79

3.2.2 Modeling of Frequency-Dependent Permeability and Derivation of Required Impedance of CM Inductor 80

3.2.3 Impedance-based CM Inductor Design Approach 84

3.2.4 Experimental Results 92

3.3 Maximum Magnetic Flux Density Model for CM Inductors 92

3.3.1 Limitation of Conventional Model 92

3.3.2 Proposed Common Mode Flux Density Model 95

3.3.3 Verification and Comparison 96

3.4 Leakage Model of Toroidal CM Inductor with Analogy of Reluctance and Capacitance 99

3.4.1 Rod Core Inductance Derivation with Analogy of Reluctance and Capacitance 99

3.4.2 Leakage Inductance of CM Choke Derivation 103

3.4.3 Verification of Proposed Leakage Model 109

3.5 Film Capacitor Model 112

3.5.1 Frequency-Dependent Ac Voltage Rating Model 113

3.5.2 ESL and ESR Model 114

3.6 Ac Dv/dt Filter Design Routine and Optimization with A_P prediction 116

3.6.1 Determination of Corner Frequency of *Dv/dt* Filter 116

3.6.2 Distribution of L and C with a Targeted Corner Frequency 118

3.7 PSO-based EMI Filter Routine and Optimization 122

3.7.1 Determination of Corner Frequency of EMI Filter 122

3.7.2 Design Iteration of EMI Filters 124

3.7.3 Design Optimization Algorithm Selection and Improvement 125

3.8 Summary 128

Chapter Four Device Selection Optimization Considering Switching Speed Limitation and Power-loop Layout 131

4.1 SiC MOSFETs Switching Behavior Model 132

4.1.1 Discrete-time Modeling of Switching Behavior 132

4.1.2 Switching Speed Prediction and Verification 136

4.2 Busbar Model 139

4.2.1 Thermal Model 139

4.2.2 Thickness Determination 141

4.3 Numerical Modeling of Power-loop Inductance with PEEC 142

4.3.1 Automated Creation of Busbar and Power-loop Layout 142

4.3.2 Numerical Techniques Comparison for Solving Field Problems 145

4.3.3 Parasitic Inductance Calculation with PEEC 147

4.4 Gate Resistance Selection with Switching Speed Optimization 155
 4.4.1 Gate Resistance General Selection Constraints 156
 4.4.2 Turn-off Gate Resistance Selection with di/dt constraint 157
 4.4.3 Turn-on Gate Resistance Selection with *dv/dt* constraint 158
 4.4.4 Complete Design Example for Gate Resistance Selection 160
4.5 Summary 164
Chapter Five Cooling Design Optimization with Multi-variable Device Loss Scaling 166
5.1 Cooling System Model 166
 5.1.1 Correction of Thermal Resistance of Extruded Heatsink 166
 5.1.2 Pressure Drop Model of Heatsinks and Fans 168
5.2 Switching Loss Scaling Method Considering Practical Parameters 170
 5.2.1 Proposed Scaling Method 170
 5.2.2 Verification of Proposed Scaling Method 174
5.3 Design Iteration Combined with Device Selection and Cooling Design 178
5.4 Summary 180
Chapter Six System-level Iteration and Optimization 182
6.1 Switching Function based Fast Simulation Scheme 182
6.2 Current Waveforms Synthesis for Components Design 189
6.3 THD Evaluation with Motor Model 191
6.4 System-level Optimization with Frequency and Modulation Selection 196
 6.4.1 System Iteration Scheme 196
 6.4.2 Case Study 198
6.5 Design Routine for Paralleled Converters 207

6.5.1 Design Strategies for Interleaving Angle and Coupled inductance 207

6.5.2 Case Study 210

6.6 Summary 213

Chapter Seven Development for Software 215

7.1 Model-view-controller (MVC) Architecture based UI framework 215

7.2 Design Configuration 216

7.3 Database Construction and Management 220

7.4 Design Results Visualization 221

7.5 Summary 224

Chapter Eight Conclusion and Future Work 225

8.1 Conclusion 225

8.2 Future Work 228

Reference 231

Vita 243

List of Tables

Table 3-1. Comparisons for different DM core materials 65

Table 3-2. Testing Condition and Specs of ANPC 74

Table 3-3. Specs of Two DM Inductors 75

Table 3-4. Specs of ANPC for EMI filter design 89

Table 3-5. Design results with two design approaches 90

Table 3-6. Comparison Results for Two Magnetic Flux Density Models 98

Table 4-1. Key parameter comparison between the predicted results and the testing results. ... 139

Table 4-2. Main futures of four numerical methods for field problems. 146

Table 4-3. Parameters of design example with C3M0065090J. 161

Table 4-4. Gate resistance selection constraints summary. 162

Table 5-1. Summary of Switching Loss Separation. 173

Table 5-2. Specs for switching loss comparison. 177

Table 5-3. Switching loss calculation comparison with two scaling methods. 178

Table 6-1. Motor Drive Controller Specification. 198

List of Figures

Fig. 1-1. Power consumption distribution for non-propulsive applications in conventional aircraft. 2

Fig. 1-2. Power consumption distribution for non-propulsive applications in the MEA 3

Fig. 1-3. The performance factors of power electronics converters in the MEA applications. 5

Fig. 1-4. A general view of design problem in power electronics in [11]. 10

Fig. 1-5. MOD framework for the development of the design tool for three-phase ac motor drive applications. 14

Fig. 2-1. Switching behavior model of Si MOSFET: (a) equivalent circuits model for saturation region [12, 13], (b) equivalent circuits model for ohmic region [13]. 20

Fig. 2-2. Switching behavior model of one phase-leg in [18]. 21

Fig. 2-3. Calculation of switching times and energies by double pulse testing [25]. 24

Fig. 2-4. Illustration of setup for calorimetric switching loss measurement in [29]. 24

Fig. 2-5. Steady-state thermal modeling for TO-type packages in [33]. 25

Fig. 2-6. Thermal flow of surface mount power devices through PCB in [34]. 26

Fig. 2-7. Steady-state thermal modeling for surface mount packages in [35]. 27

Fig. 2-8. Lumped circuits model of inductors in [10]. 31

Fig. 2-9. Illustration of thermal resistance network modeling for level 3 thermal design of inductors in [62]. 37

Fig. 2-10. Typical ESR curve with frequency in [65] 38

Fig. 2-11. Illustration of a cooling system with extruded heatsink and fan [69]. 40

Fig. 2-12. Illustration of dynamic fluid models on cooling design [69]. 41

Fig. 2-13. A general review of design problem in power electronics in [89]. 45

Fig. 2-14. Classification of optimization algorithms in two categories. 46

Fig. 2-15. Local optimization summary in power electronics design. 50

Fig. 2-16. The configuration of an industrial motor drive in [11]. 52

Fig. 2-17. Approach for system optimization for a motor drive in [11]. 53

Fig. 2-18. General concept for multi-objective optimization with Pareto-front curve in [101]. .. 53

Fig. 2-19. Higher-level system Pareto front could be identified by synthesizing sub-system Pareto fronts in [126]. 54

Fig. 2-20. Three layers of optimization structure in [126] for EV charger application. 55

Fig. 2-21. Pareto curve of the η-ρ performance space and the selected design point in [62]. 57

Fig. 2-22. Design variables arrangement comparison: centralized optimizer vs. distributed optimizers. 58

Fig. 3-1. Inductance curve with current-bias for ferrite and powder core [127]. 64

Fig. 3-2. Permeability percentage curves with current-bias for amorphous and powder core. 65

Fig. 3-3. Permeability percentage curve with current-bias for amorphous and powder core. 67

Fig. 3-4. Simulation waveforms for non-linear DM inductance. 69

Fig. 3-5. DM currents comparison with or without non-linear DM inductor model. 70

Fig. 3-6. Noise spectrum comparisons from simulation results. 70

Fig. 3-7. Flow chart of the design algorithm of EMI filter with consideration of current-bias dependent permeability. 73

Fig. 3-8. The prototype of ANPC for EMI testing setup. 74

Fig. 3-9. The prototype of two DM inductors 76

Fig. 3-10. Experimental waveforms and noise measurement for two inductors. 77

Fig. 3-11. EMI bare noise comparisons only with DM inductors. 77

Fig. 3-12. Corner frequency design of CM filter. 78

Fig. 3-13. Permeability curve for ferrite and nanocrystalline cores. 79

Fig. 3-14. Curve fitting results of the real and imaginary permeability of nanocrystalline material VITROPERM 500F. 81

Fig. 3-15. Equivalent common-mode circuits of a three-phase converter (a) without CM filter, (b) the CM filter. 83

Fig. 3-16. Real impedance curve of the traditional design approach. 85

Fig. 3-17. Design procedure to calculate the required turns number. 86

Fig. 3-18. Physical design procedure and iteration for CM inductors. 88

Fig. 3-19. The prototype of two CM inductors. 90

Fig. 3-20. Comparisons between measured results and design results. 91

Fig. 3-21. Noise spectrums comparison with two design inductors. 93

Fig. 3-22. CM inductor voltage and current waveforms. 97

Fig. 3-23. Derived magnetic flux density waveforms comparison for case II. 97

Fig. 3-24. The analogy between the electric field of plate capacitors and the magnetic field of rod core inductors. 101

Fig. 3-25. The duality between: (a). magnetic circuits, (b). electrical circuits. 101

Fig. 3-26. Leakage modeling comparison with two rod core inductance models. 103

Fig. 3-27. Magnetic fields of two-phase CM choke (hiding toroidal core). 104

Fig. 3-28. The analogy of magnetic fields and electric fields for a CM choke with a large turns number. 104

Fig. 3-29. Geometry equivalent transformation from curved faces to folded planes. 105

Fig. 3-30. Electric filed for non-parallel planes in polar coordinates. 106

Fig. 3-31. Comparison of leakage inductance models with FEM simulation results for magnetic core ZW43610TC. 110

Fig. 3-32. Comparison of leakage inductance models with FEM simulation results for magnetic core ZW44925TC. 111

Fig. 3-33. Limits for maximum ac RMS voltage with the operating frequency [139]. 113

Fig. 3-34. The typical ac voltage rating curves as a function of the frequency. 114

Fig. 3-35. The measured dissipation factor as a function of the frequency in [139]. 115

Fig. 3-36. The illustration of three cores bundled wires in [140]. 117

Fig. 3-37. Converter ac side output current with different LC combinations when the corner frequency of *dv/dt* filter is 166.7 kHz. 119

Fig. 3-38. Relationship between core weight and AP value. 120

Fig. 3-39. Output current prediction with phase PWM voltage: (a) PWM voltage of bridge output terminal, (b) predicted output current. 121

Fig. 3-40. One optimization example for dv/dt inductor. 121

Fig. 3-41. Two EMI configurations in this project. 123

Fig. 3-42. Corner frequency calculation based on bare noise, (a) dc side CM bare noise, (b) corner frequency determination based on required attenuation. 123

Fig. 3-43. Design iteration of dc side EMI filter design. 125

Fig. 3-44. Verification of PSO and GA algorithm with a strong non-linear function: (a) plot of the non-linear function with two variables, (b) contour plot of x-y plane, (c) iteration convergence with PSO, (d) iteration convergence with GA. 127

Fig. 3-45. Verification of the improved PSO algorithm. 127

Fig. 4-1. The illustration of *M* modes in one switching cycle for discrete-time modeling......... 133

Fig. 4-2. Automatic extraction of capacitance curves... 134

Fig. 4-3. Curve fitting results of transconductance as a function of junction temperature......... 134

Fig. 4-4. Curve fitting results of threshold voltage as a function of junction temperature. 135

Fig. 4-5. The characterization results of C_{gs} as a function of v_{gs}. 135

Fig. 4-6. Waveform comparison between the developed model and PSpice model.................. 136

Fig. 4-7. Prototype of DPT platform for SiC MOSFET C3M0065090J. 137

Fig. 4-8. Waveform comparison at the testing condition of 450 V and 20 A with different gate resistances. 138

Fig. 4-9. Design iteration for busbar thickness selection. 141

Fig. 4-10. One example of predefined two-level voltage source inverter layouts. 143

Fig. 4-11. Example of automatically created geometry with geometry description script language. 145

Fig. 4-12. Example of PEEC model for two volume cells. 149

Fig. 4-13. Discretization schemes for different geometries. 150

Fig. 4-14. Impedance matrix as a function of frequency with different discretization resolutions. 152

Fig. 4-15. Relative error as a function of frequency compared to 0.8 um discretization results. 152

Fig. 4-16. Extracted inductance value comparison of ANPC layout between FEM and PEEC. 154

Fig. 4-17. Extracted inductance value comparison of the laminated busbar between FEM and PEEC. 155

Fig. 4-18. Equivalent circuits for gate drive during turn-on transient. 156

Fig. 4-19. Diagram of the determination of turn-off gate resistance considering *di/dt*. 158

Fig. 4-20. Malfunction of gate drive due to high *dv/dt* event. 159

Fig. 4-21. Diagram of the determination of turn-on gate resistance considering *dv/dt*. 160

Fig. 4-22. Automatically created power loop layout for design example with C3M0065090J.. 161

Fig. 4-23. Switching waveforms and v_{gs} comparison with different gate resistances. 163

Fig. 4-24. Switching waveforms and v_{ds} comparison with different gate resistances. 164

Fig. 5-1. Length correction factor for the thermal resistance of extruded heatsinks. 167

Fig. 5-2. Temperature correction factor for the thermal resistance of extruded heatsinks. 167

Fig. 5-3. Forced air correction factor for the thermal resistance of extruded heatsinks. 168

Fig. 5-4. Pressure drop curves scaling with the law of fans. 169

Fig. 5-5. Operating condition determination with pressure drop curves of selected heatsink and fan. 170

Fig. 5-6. Loss related to the non-linear capacitance during charging and discharging. 172

Fig. 5-7. Switching loss scaling at different testing voltages. 174

Fig. 5-8. Switching loss scaling at different testing currents. 175

Fig. 5-9. Switching loss scaling at different gate resistances. 176

Fig. 5-10. Switching loss scaling at different junction temperatures. 176

Fig. 5-11. Flow chart of device selection and cooling design. 179

Fig. 6-1. One phase-leg for an ANPC converter. 183

Fig. 6-2. General equivalent circuits for ac outputs of three-phase converter systems. 184

Fig. 6-3. Dc input side equivalent circuits for ANPC converter. 185

Fig. 6-4. Two multi-level topologies for a three-phase converter system in [153]. 186

Fig. 6-5. General dc side equivalent circuits for multi-level converters. 187

Fig. 6-6. Simulation time comparison for three topologies. 189

Fig. 6-7. Phase voltage synthesis for multi-level converters. 190

Fig. 6-8. Switching cell in flying capacitor clamped topology. 191

Fig. 6-9. Open-loop scheme for starting a synchronous machine. 193

Fig. 6-10. Synchronous machine open-loop simulation waveforms. 193

Fig. 6-11. THD evaluation with steady-state operating waveforms in the open-loop simulation. 194

Fig. 6-12. Open-loop scheme for starting a permanent magnet synchronous machine. 195

Fig. 6-13. PMSM open-loop simulation waveforms. 195

Fig. 6-14. Design diagram for the whole converter. 197

Fig. 6-15. System-level iteration diagram. 197

Fig. 6-16. Power architecture of the motor drive controller. 198

Fig. 6-17. Waveforms of CM voltage and phase voltage with different modulations. 200

Fig. 6-18. Design results for three-level ANPC with SVM and single-stage EMI filter. 201

Fig. 6-19. Design results for three-level ANPC with DPWM and single-stage EMI filter. 202

Fig. 6-20. Design results for three-level ANPC with CMR and single-stage EMI filter. 202

Fig. 6-21. Design comparison for three-level ANPC with the single-stage EMI filter at 900 V. 203

Fig. 6-22. Design comparison for three-level ANPC with the two-stage EMI filters at 900 V. 204

Fig. 6-23. Design comparison for three-level ANPC with the two-stage EMI filters at 1500 V. 204

Fig. 6-24. Design comparison for three basic topologies at 900 V... 206

Fig. 6-25. All design results of three basic topologies.. 206

Fig. 6-26. The configuration of coupled inductors in two paralleled converters....................... 208

Fig. 6-27. Waveforms of phase voltage with different interleaving angles 209

Fig. 6-28. Waveforms of phase current with different current ratios. 210

Fig. 6-29. Design results of two paralleled ANPC converters with different interleaving angles and circulating current ratios. 212

Fig. 6-30. Design Comparison between the single converter and two paralleled converters. 213

Fig. 7-1. MVC architecture based software framework. 215

Fig. 7-2. Design configurations provided by the developed software. 217

Fig. 7-3. Load configurations in the developed software. 219

Fig. 7-4. Design parameters save and load function in the developed software....................... 219

Fig. 7-5. Database management in the developed software... 220

Fig. 7-6. Design visualization functions for the developed software. 222

Fig. 7-7. Weight breakdown for a single converter design result. 222

Fig. 7-8. Weight comparison at different switching frequencies. 223

Fig. 7-9. Detail design results and the selected component information. 223

Chapter One

Introduction

Transportation electrification becomes an irreversible trend to cope with the petroleum-based energy crisis and environmental pollution issues. Based on U.S. Energy Information Administration, transportation consumed energy is the second largest part, which is only lower than electric power consumption, and 93% of the consumed energy in transportation is from petroleum [1]. Hence, there is a huge and long-term opportunity while the transportation electrification revolution is underway, and there will be remarkable environmental and economic benefits for industry as well as new challenges and research topics for academia. In this context, the power electronics converter system, as an interface between the electrical power and power take-off unit (motor drives in most cases), will make major contributions to overcome the most urgent challenges in the process of transportation electrification.

In this chapter, the more electric aircraft (MEA), as the target application, is investigated to show requirements for the design of the power electronics converter system. The main target for the converter system in MEA is to achieve the lightest weight considering fuel economy. Furthermore, it is discussed what are the challenges and motivations for the design of power electronics converters at MEA applications. Eventually, a Model-Data-Optimization (MDO) framework is proposed to help develop such a design software to reduce the gap between the paper design and implementations and to improve the design efficiency.

1.1 Application Background

More electric aircraft (MEA) employ an increasing amount of electric power in the place of hydraulic, pneumatic, and mechanical power. The purpose of proposing the concept of MEA is to further improve the efficiency, to reduce the fuel-cost and CO_2 emissions [2], and to reduce the weight by replacing heavy hydraulic, pneumatic, and mechanical driven equipment. According to the report from military aircraft studies [3], MEA technologies will help realize a 5.4% increase in average flying time between failures and a 6.5% decrease in the total aircraft weight.

As shown in Fig. 1-1, the power created by turbines in conventional aircraft (e.g., A330) can be divided into a propulsive part and a non-propulsive part [4]. Electrical power only takes a very small portion of non-propulsive power for non-critical equipment and loads such as lights, cabin, and avionics. Most important functions like flight control and fuel pumping are realized by hydraulic and mechanical power from the main turbines. However, the hydraulic and mechanical drive equipment is typically heavy, inflexible, and requires regular maintenance [5]. Also, due to the requirement of the high reliability for aircraft, back-up hydraulic equipment for the flight control is installed in conventional aircraft. Hence, one main intention of the MEA concept is to replace the hydraulic actuators with motors [6].

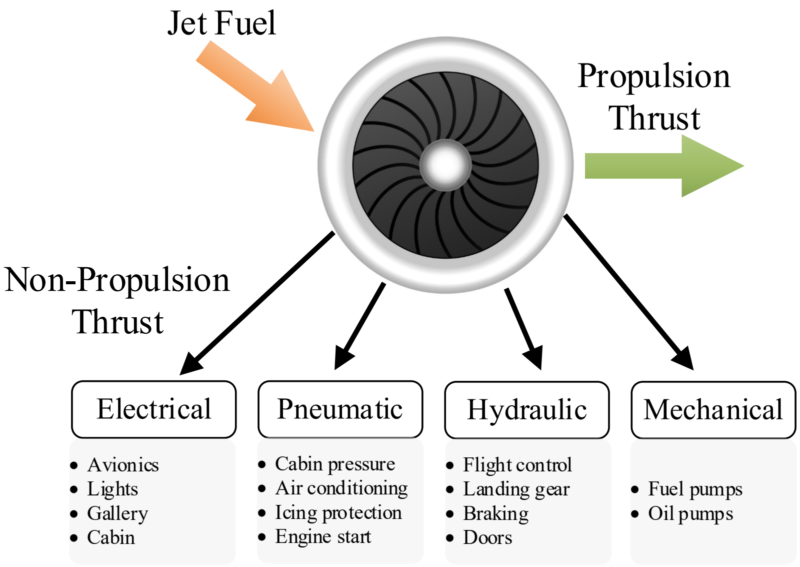

Jet Fuel
Propulsion Thrust
Non-Propulsion Thrust
Electrical
Pneumatic
Hydraulic
Mechanical
• Avionics
• Lights
• Gallery
• Cabin
• Cabin pressure
• Air conditioning
• Icing protection
• Engine start
• Flight control
• Landing gear
• Braking
• Doors
• Fuel pumps
• Oil pumps

Fig. 1-1. Power consumption distribution for non-propulsive applications in conventional aircraft.

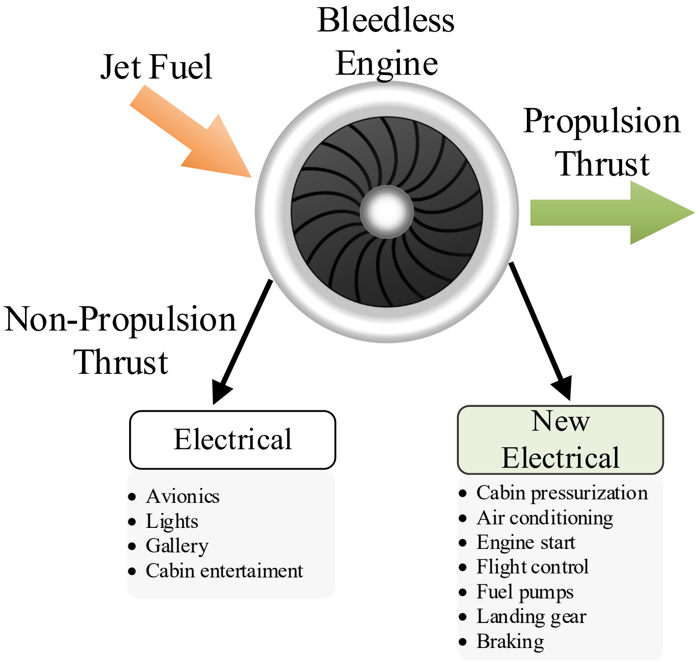

Bleedless Engine
Jet Fuel
Propulsion Thrust
Non-Propulsion Thrust
Electrical
Avionics
Lights
Gallery
Cabin entertaiment
New Electrical
Cabin pressurization
Air conditioning
Engine start
Flight control
Fuel pumps
Landing gear
Braking

Fig. 1-2. Power consumption distribution for non-propulsive applications in the MEA

To fully take advantage of the MEA concept, Fig. 1-2 shows a new mapping of non-propulsive power, and the most critical equipment is electrically powered. Moreover, to further improve the engine efficiency, a bleedless engine is applied instead of a bleed air engine [7]. Without bleed air, however, the aircraft requires a new environmental control system (ECS) for cabin pressurization, air conditioning, and icing protection. All these changes have led to significantly increased use of power converters and electric drives for this application, and power electronics converters design begins to play a key role in the design stage of MEA, and the high power density (weight based) of the converter system is the most desirable objective for fuel economy.

Moreover, power system architecture in MEA is still under development, and different schemes with different dc-link voltages and ac grid frequencies are proposed. The mechanical gearbox between turbines and generators are eliminated for high power generating efficiency. This, however, results in a varied line frequency (360 Hz – 800 Hz) compared with the constant main frequency of 400 Hz [8]. Also, many voltage levels exist in different aviation power architectures. For dc grid, 28 V, 270 V, 540 V, 900 V, 1000 V, 1500 V, 2400 V, and 7500 V are all considered as candidates while, for the ac grid, 115 V and 230 V from 360 Hz to 800 Hz are mainly considered [9]. As a result, to have a better understanding of how these parameters impact the system weight and performance, several benchmark design works need to be conducted for detailed comparisons.

On the other hand, since the power capacity in MEA is going to much higher (Airbus A330, 300 kVA; A380, 600 kVA; Boeing 787, 1 MVA), more and more power electronics converters will be applied, and the performance of power electronics converters becomes critical to the whole system. As shown in Fig. 1-3, weight, development costs, time to market and other performance factors must be considered and optimized carefully in the design stage.

However, owing to the high complexity of power electronics design which requires knowledge from multi-physics domains, no commercial power electronics design tool is available for an accurate converter performance evaluation. Generally, a comprehensive converter design incorporates several engineers from electric, thermal, and mechanical areas, and it can take 6 months to one year to evaluate and compare different topologies, modulations, and other technologies for only one specific application. Moreover, even though a complete design result has been finished in the paper design, it could still take a long time to debug converters due to the gaps between the paper design and the implementations.

1.2 Research Motivations and Challenges

Several factors contribute to the gaps between the paper design and implementations. First, the real performance of components diverges from the predicted performance due to inaccurate models. For example, the state-of-art core loss model IGSE is a curve-fitting model rather than an

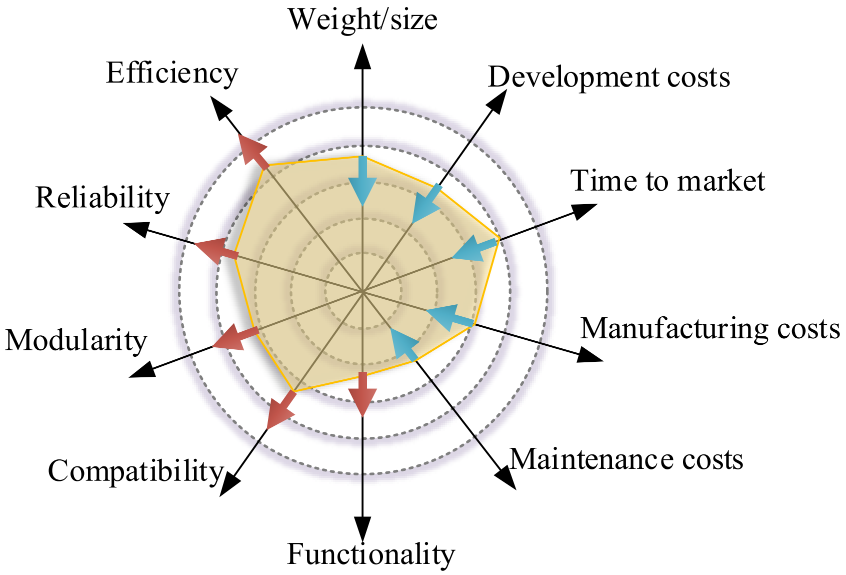

Weight/size
Development costs
Time to market
Manufacturing costs
Maintenance costs
Functionality
Compatibility
Modularity
Reliability
Efficiency

Fig. 1-3. The performance factors of power electronics converters in the MEA applications.

analytical model, and it cannot have a good estimation of core losses when a dc bias exists. Also, the current leakage inductance model for common-mode inductors in the literature still has 30% errors in some cases compared with testing results [10].

Second, the conventional design approach has not considered the non-linear physics characteristics of power electronics components. The EMI noise prediction highly depends on the impedance of magnetic core inductors. However, the impedance of magnetic core inductors can be varied with the operating frequency and current bias.

Third, the conventional design approach has experience-based assumption and margin selection rather than the scientific or optimized ones. For example, the current ripple is usually assumed as 10-20% of the peak current. However, the current ripple has impacts on the inductance value, inductor loss, device loss, cooling design and EMI noise spectrum. Such an experience-based rule to select inductance value is not scientific to get an overall optimal point for the whole converter system.

At last, the conventional design approach also is not capable of considering the interactions between the device switching behavior and the geometry of circuits, and a trial-and-error procedure is always required in the debugging stage. One example is how to select gate resistance which determines the switching speed. The switching speed affects both switching losses and switching frequency capabilities, and the faster switching speed is, the lower switching loss and higher switching frequency can be achieved. Moreover, the cooling design is also closely related to gate resistance selection due to its influence on the switches' loss. However, the gate resistance selection is generally decided by the allowed voltage spike during turn-off and is highly associated with the layout or geometry of PCB or busbar. As a result, it causes gaps between the paper design and testing results since the gate resistance selection is generally neglected in the paper design stage, and the impacts of these factors on the system-level converter performance are not included during the design. Hence, a trial-and-error procedure in the implementation step is carried out for debugging the converter. It is common to adjust gate resistance and redo the busbar or PCB layout in the debugging stage of the designed converter.

Furthermore, the power electronics converter design comprises numerous design variables and knowledge from several different fields such as electrical, thermal, mechanical, and magnetics, and it generally relies on the experience of engineers by fixing some design variables (like switching frequency, current ripple) and introducing some assumptions (e.g., constant inductance value and operating junction temperature). This traditional design procedure simplifies the design problem and provides a reasonable design point, but to verify, evaluate, and improve the converter performance with designed parameters, time-domain simulations need to be carried out for several design iterations. As a result, this experience and simulation-based design procedure will lead to a good but not the optimal design. The optimal design is closely related to the objective function, and it can be selected as the minimum loss, lowest cost, smallest size, or lightest weight based on the application requirement in power electronics design. Also, the multi-objective function can be applied to determine the optimal design to achieve the balance between two or several design objectives, e.g., efficiency and cost, power density and efficiency.

The purpose of the dissertation is to develop a comprehensive, scientific and automated design approach for SiC-based power electronics converters for three-phase ac motor drive in MEA applications that shrinks the gaps between the paper design and real performance of implemented converters, and also enables the weight optimization to determine the lightest converter system scheme. By utilizing advanced analytical modeling, numerical modeling and data-driven based modeling methods, the developed approach will fully consider non-linear physics characteristics of power electronics components neglected by the traditional design approach. Also, an optimization algorithm will be applied to reduce trial-and-error efforts in the switching frequency selection, LC filter value determination and other experience-based selection of design variables, providing a near-optimal design margin or design rule for components. Another feature of the proposed design approach is to cover the design coupling between the parasitics and layout geometries in real circuits, impacting the allowed switching speed and gate resistance selection. The partial element equivalent circuit (PEEC) method combined with advanced device models will be used to establish a link between the switching speed and layout geometries, affording a switching speed optimization considering busbar layout and EMI performance. It is also expected that the design approach will realize the capability of automated design without the integration of the expensive and computationally intensive FEM simulation software.

In the following, the challenges of this work have been separated into three aspects: modeling, design approach and optimization, design automation.

1.2.1 Modeling

The accurate models for power electronics components can effectively shrink the gaps between the paper design results and the implementation results. Also, with the advanced modeling, more non-linear physics characteristics and parasitics are considered in the paper design stage, further reducing the design gaps. The main challenges of modeling in power electronics design are:

1) Further to improve the accuracy of the modeling. Most models in power electronics have assumptions, and they can be applied only in some limited cases and ranges for acceptable errors, e.g., the leakage inductance model for toroidal common chokes and device loss model at different operating conditions.
2) Need to consider more non-linear physics characteristics of power electronics components. The inductance, capacitance and thermal resistance of heatsink are generally treated as constant values in power electronics design, but actually, they are not. For example, since the inductance highly depends on the current bias (magnetic field strength) and operating frequency, a time-varying inductor model should be developed considering the non-linear permeability model.
3) To solve the most difficult modeling problems by employing data-driven based modeling methods. The state-of-art core loss calculation method IGSE is still not accurate enough when the inductor has a dc-bias current. If a large amount of core loss data can be collected by measurements and simulations accurately, a data-driven based

method can be applied to train a multi-layer artificial neural network (ANN) based model.

4) To effectively and efficiently model the geometry-related parasitics. Nowadays FEM software is widely applied for the extraction of parasitics for the busbar and PCB layout. However, it requires users to draw or import the 3-D geometry manually and the parasitics only can be estimated at the end of the layout work. A lightweight tool or algorithm needs to be developed for parasitic extraction in the paper design stage before the implementation stage, and the tool can help create near-optimal layout automatically with the selected power switches and dc-link capacitors. Thus, the parasitics of the created layout can be quickly evaluated, then the switching speed can be further determined for the switching loss calculation and cooling design.

1.2.2 Design Approach and Optimization

Optimization methodology compels engineers to design in a structured way. Based on Fig. 1-4, the optimization problem in power electronics can be formulated in the following way:

Minimize or maximize:

$F(x)$ Objective function

Subject to:

$g(x) < 0$ inequality constraints

$h(x) = m$ equality constraints

$1 < x_i < N$ integer constraints

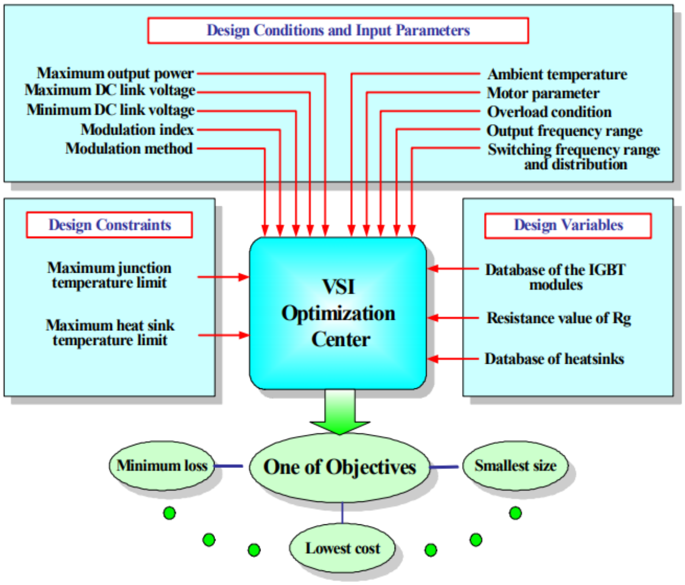

Design Conditions and Input Parameters
Maximum output power
Maximum DC link voltage
Minimum DC link voltage
Modulation index
Modulation method
Ambient temperature
Motor parameter
Overload condition
Output frequency range
Switching frequency range and distribution
Design Constraints
Maximum junction temperature limit
Maximum heat sink temperature limit
VSI Optimization Center
Design Variables
Database of the IGBT modules
Resistance value of Rg
Database of heatsinks
Minimum loss
One of Objectives
Smallest size
Lowest cost

Fig. 1-4. A general view of design problem in power electronics in [11].

where

$$\mathrm{x} = \left\{ \begin{matrix} x_1 \\ x_2 \\ \cdot \\ \cdot \\ x_n \end{matrix} \right\} \qquad \text{design variables}$$

Objective function: This function describes what the goal of optimization is, and what the designer’s requirement is. For power electronics, under global optimization, the objective function can be the lowest cost, lowest weight or highest efficiency. But under a partial optimization case, for a specific trade-off design, the objective function can also be the lowest harmonics, lowest CM voltage and so on.

One feature for objective function is that it can only have one target. If there is more than one objective, it is essential to assign a weight for each objective and sum up to one objective function by using weighting coefficients.

Constraints: The calculation of the objective function should be conducted under some given constraints. Usually, it includes three parts: inequality constraints, equality constraints and integer constraints. Inequality constraints and equality constraints are used to describe some design requirements. For example, one inequality constraint in power electronics design is that converter noise should be lower than the EMI standard while one equality constraint in power electronics design is that the working junction temperature of power devices is 150 ºC. Integer constraints is a physical limitation for some components, like turns number, and it must be an integer during the optimization procedure.

Design variable: This is the most straightforward part of one optimization procedure. In power electronics, if selecting the design variables from the bottom level, it will be hundreds of variables like turns number, core material, core shape, core dimensions, device type, capacitor type, etc. Another important remark is some design variables in power electronics are discrete variables rather than continuous variables, such as turns number or device type. Therefore, the optimization algorithms should be selected carefully to adapt to discrete variables.

However, most design approaches only focus on one function block of power electronics converters, such as the minimum harmonics, the minimum EMI filter volume, the minimum power switches' loss, the lightest heatsink design and so on, rather than the whole system-level performance. In this work, the objective of the design is to achieve the lightest weight design for the whole power electronics system including all function blocks in the motor drive applications. The efficiency of the converter system is also important, but it will not be added to the objective function. Instead, a minimum efficiency requirement will be applied in the design contains to exclude low-efficiency design cases. The main challenges of the design approach and optimization in this work are:

1) Try to avoid experience-oriented design rules and margin selections which helps to get a reasonable design but not an optimal design. For example, for a given corner frequency of one single-stage LC filter in EMI design, how to distribute L and C is a design trade-off. Usually, designers try to use the largest capacitance value and the smallest inductance value to achieve the minimum volume or weight. Nonetheless, the smallest inductance does not equal the minimum weight since the high current ripple can lead to a high core loss, which may increase the core size and weight. There should be a design optimization to solve design trade-offs more scientifically.
2) Consider additional impact factors on the realistic converter performance that previously have been neglected. In the conventional approach, to simplify the design, some assumptions are made for quick evaluation, but it indeed leads to a non-optimized design. For example, the pressure drops of heatsink and fan should be considered for the cooling design. The impact of the gate resistance selection on switching loss and voltage spike should also be considered.
3) How to accelerate the simulation speed for the design? Power electronics design requires many raw data of operating waveforms for the design of components. An investigation of the simplified and fast simulation scheme is necessary to improve the efficiency of the design tool.
4) How to formulate the power electronics design problems and to apply the optimization algorithms in the power electronics design? Brute force may not be efficient enough for the power electronics design.

1.2.3 Design Automation

Design automation is one of the most desirable features for a design tool, and it requires the incorporation of multiple software from different physics domains. To reduce manual interventions, the interfaces among multiple software need to be developed and tested. The main challenges of design automation in this work are:

1) Build databases for all power electronics components. The program can easily read and write the data in each database with a simple and friendly interface.
2) Establish the communication link among multiple software for the multi-physics design. However, another way is to apply self-developed lightweight algorithms or functions to replace large scale software that only part of functions is used for the design.
3) Develop a friendly user interface to do the configuration of design parameters, the management of design results and database.
4) Develop the visualization function to better display the design results.

1.3 Proposed Model-Data-Optimization Framework for Power Electronics Design

MDO based strategy is proposed to develop the design tool. As shown in Fig. 1-5, MDO stands for modeling, data, and optimization. MDO separates the design approach into three aspects: establishing models, acquiring data, applying optimization algorithm. All three aspects are combined to reduce the experience-based design procedure and unscientific design margins selection and to include unconsidered physics characteristics in the current design method.

Three modeling techniques are adopted for the modeling part. Analytical modeling and curve fitting modeling are applied for most models for fast calculation with acceptable error. Data-driven based modeling is used for the strong non-linear models like the core loss model and the leakage inductance model. Numerical modeling is adopted for the estimation of parasitics of the geometry-related structure of the busbar or the layout of the power loop. In this work, numerical modeling does not rely on the commercial FEM software like Ansys since it is so heavy and bulky with integrating too many functions, and only a few functions are really valuable for power electronics users. Instead, a lightweight partial element equivalent circuits (PEEC) based numerical modeling method is implemented to calculate the self and mutual inductance of different mechanical structures.

Data acquisition provides three functions in the design tool. First, through the data collection from datasheet provided by manufacturers, databases with all required parameters for power

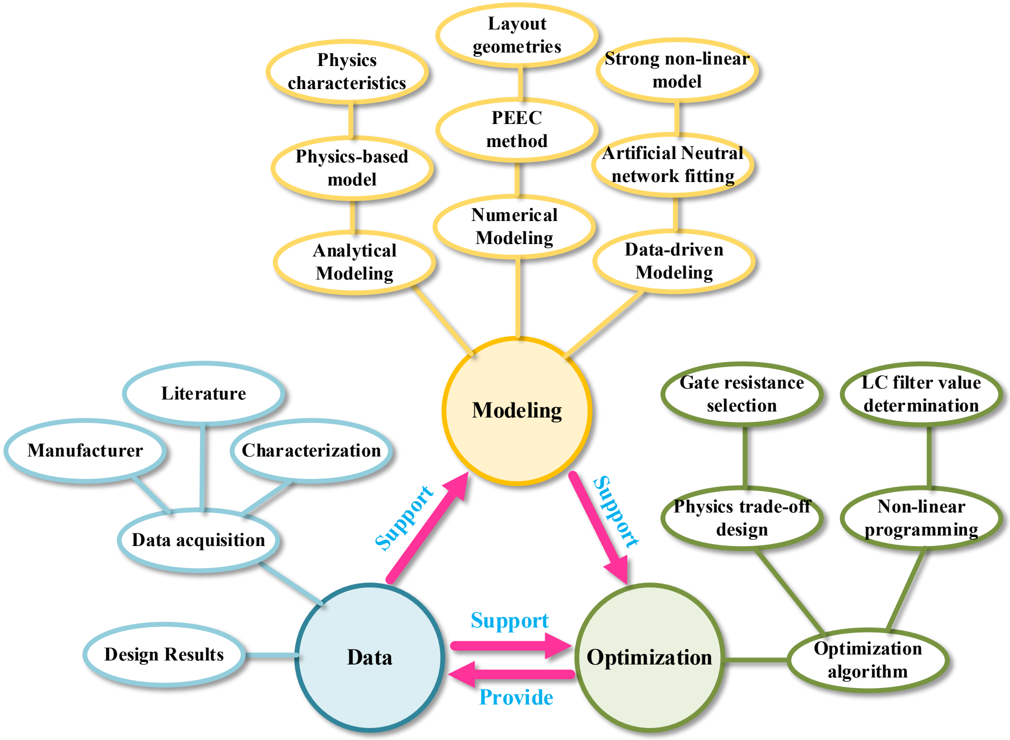

Layout geometries
Physics characteristics
Strong non-linear model
PEEC method
Physics-based model
Artificial Neutral network fitting
Numerical Modeling
Analytical Modeling
Data-driven Modeling
Modeling
Literature
Manufacturer
Characterization
Gate resistance selection
LC filter value determination
Support
Support
Data acquisition
Physics trade-off design
Non-linear programming
Support
Design Results
Data
Optimization
Optimization algorithm
Provide

Fig. 1-5. MOD framework for the development of the design tool for three-phase ac motor drive applications.

electronics components are established as the design inputs of the physical design of each component. Second, collecting the data from the characterization, measurements, simulations can be used for training ANN-based models to solve the most difficult and strong non-linear models in the power electronics area. Third, the design results can also be collected to create and train an expert system to predict the system performance without going through the detailed design procedure. Also, the created expert system could give design recommendations in terms of topologies, modulations, switching frequencies, and EMI filter structures only based on the specifications of converters.

Non-linear optimization algorithms and design strategies are applied for different kinds of trade-off problems in the power electronics design. Population-based searching algorithms like particle swarm optimization (PSO) and genetic algorithm (GA) are appropriate to discrete type design variables, non-linear and non-convex design problems in power electronics design.

1.4 Dissertation Layout

This dissertation is organized as follows:

The state-of-art research on the modeling and design optimizations of power electronics are reviewed in Chapter 2, and the research gaps are summarized.

Chapter 3 presents two filter design optimization schemes for different filters. For ac side *dv/dt* filters, a weight optimization with *Ap* prediction is applied. For EMI filters, a design optimization scheme combined with the modeling of non-linear characteristics of magnetic core inductors and the improved PSO algorithm is proposed. The frequency-dependent permeability of nanocrystalline cores and the current-bias-dependent permeability of powder cores are covered in the design, and their impacts on the filter performance are studied. Furthermore, a new perspective of the leakage inductor modeling through the analogy between reluctance and capacitance is applied to improve the accuracy of the leakage inductance modeling of toroidal cores.

Chapter 4 proposes a device selection scheme considering the practical layout and switching speed. A discrete-time switching behavior model is developed to predict the switching speed at different operating conditions and gate resistances, and an automatic geometry creation program is implemented with PEEC numerical modeling method to estimate the practical parasitic inductance of the busbar or PCB layout with the selected power devices. With the estimated parasitics, the gate resistance can be determined by the proper switching speed to avoid overvoltage and crosstalk issues.

Chapter 5 develops a cooling optimization scheme with more practical constraints. First, the pressure drops of heatsink and fans are modeled and considered to decide the airflow speed of the selected fan and the corresponding thermal resistance of the selected heatsink. Second, to obtain more accurate switching loss data, a multi-variable switching loss scaling method is proposed to incorporate more practical parameters including the gate resistance, the operating junction temperature. At last, a complete design iteration covering device selection optimization and cooling design is given.

Chapter 6 studies system-level iteration and optimization in terms of the selection of the switching frequency, modulation scheme, and topology. To accelerate the design iterations, a switching function based simulation scheme is presented for the three-phase inverter system, and current synthesis with switching functions is also given as inputs for the design of power electronics components. Moreover, the design algorithm for the paralleled converters is presented. Two extra design variables including the coupling inductance and interleaving angle are included to search the lowest system weight of two paralleled converters.

Chapter 7 presents the development of software that integrates all the design models and algorithms proposed in the dissertation. The developed software provides multiple functionalities covering the design configuration, database management, and design results visualization.

Chapter 8 summarizes the research work and contributions presented in this dissertation and discusses future work.

Chapter Two

Literature Review

Data acquisitions, components modeling, and design optimizations are three critical aspects of the power electronics design. Data acquisition provides raw data and detailed information for the power electronics components modeling and design either from manufacturers' datasheets or from characterization results. Component modeling covers all required models for the electrical and physical design of power electronics components by analytical, numerical or curve fitting models; Design optimization affords algorithms and iterations to solve trade-offs or search for optimal combinations in the power electronics design. In this chapter, the review of components modeling for electrical and physical design including both active and passive components is presented. Then the review for design approaches and optimization algorithms in power electronics applications is also given. Through the review, a comprehensive investigation and comparison of the state-of-art models and design algorithms in power electronics applications are conducted.

2.1 Power Semiconductors Modeling

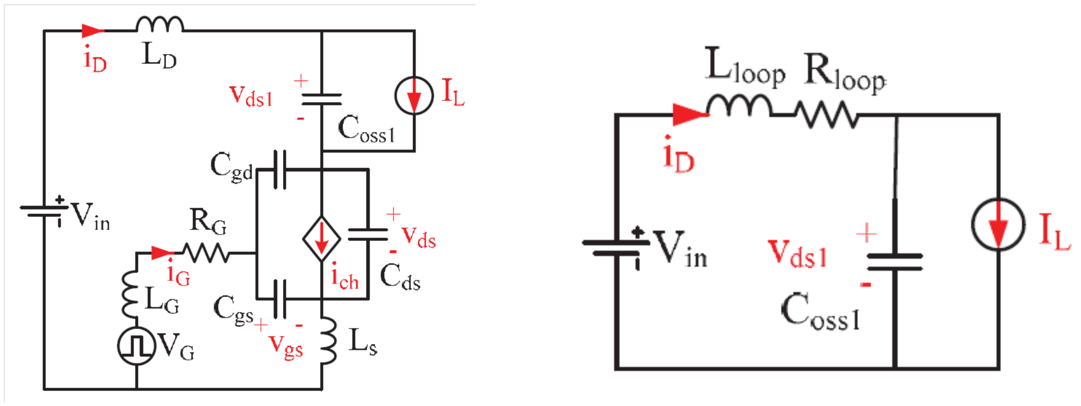
Power semiconductors play the key role in power electronics converters, realizing the waveforms modulation and power conversion. The many impacts of power semiconductors on power electronics design include EMI and power filter design, cooling design, busbar design, or power loop optimization in PCB design. Hence, the accuracy of power device modeling is critical to achieve a trusted and reliable overall converter design result.

Power device modeling generally covers the switching behavior model, loss model, and thermal model. The loss model and thermal model of power devices determine the cooling design of active components, while the switching behavior model is utilized to predict switching transient performance and waveforms at turn-on and turn-off. Furthermore, with the switching behavior model, the switching speed is predictable so that the maximum accepted power loop inductance can be calculated considering the maximum accepted voltage stress, providing a design guide to the power loop optimization.

This section will review the state of art power semiconductor models in the existing literature, how to apply device models into the design and the limitations of existing device models.

2.1.1 Switching Behavior Model

Ren [12] first presented a comprehensive analytical model of Si-MOSFETs considering the nonlinearity of the capacitors of the power devices and parasitic inductance in the power circuits. To derive switching waveforms of MOSFETs, Ren divided the turn-on and turn-off period into four phases, and each phase has different equivalent circuits. Then with equivalent circuits, the equations of key variables can be derived and solved at the frequency domain, and sinusoidal or exponential solutions are given by transferring back to the time domain. MOSFETs are equivalent to different components in different operation regions at four phases. In the saturation region, MOSFETs are treated as a voltage-controlled current source as shown in Fig. 2-1, and control gain is the transconductance of MOSFETs. In the ohmic region, MOSFETs are equivalent to resistance with the same value of channel resistance. With this model, the switching loss can be well predicted, and the estimated efficiency curve only has a maximum 1% error compared with the measured efficiency curve. Also, the switching waveforms obtained from this model can match the experimental waveforms very well even for 2 MHz oscillation.



(a) (b)

Fig. 2-1. Switching behavior model of Si MOSFET: (a) equivalent circuits model for saturation region [12, 13], (b) equivalent circuits model for ohmic region [13].

However, the difficult part of applying such an analytical model is how to extract parasitics of real circuits of converters accurately since the parasitics have a significant influence on the switching waveforms and switching loss results. Reference [14-16] further improves the model with the package parasitic inductance extraction and the passive components parasitics extraction. A comprehensive evaluation of switching loss caused by parasitics is given in [17] by using the analytical switching model, and it pointed out parasitic ringing induced switching loss is generally negligible even with a small gate resistance. However, the fast switching speed induced severe ringing with a small gate resistance could cause extra switching loss by cross-talk. To include the impacts of cross-talk on switching behavior, instead of the single device modeling, a phase-leg analytical model is proposed in [18, 19] as shown in Fig. 2-2. With the phase-leg configuration, the false turn-on and extra switching loss caused by cross-talk can be evaluated.

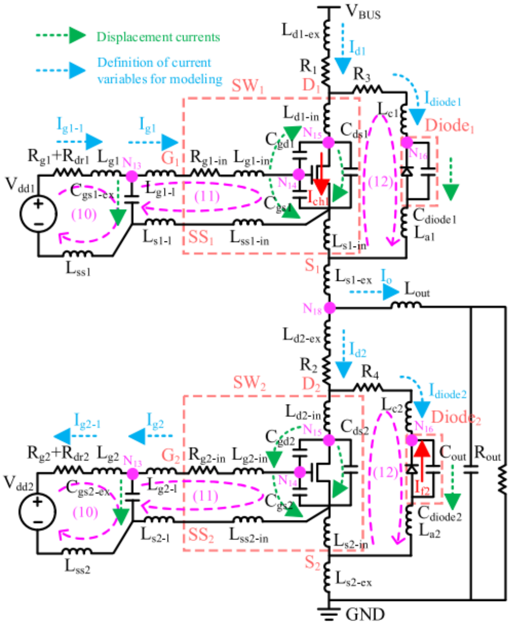

Displacement currents
Definition of current variables for modeling
V_BUS
L_d1-ex
I_d1
R_1
R_3
SW_1
D_1
I_diode1
L_d1-in
L_c1
Diode_1
I_g1-1
I_g1
C_gd1
N_15
C_ds1
R_g1+R_dr1
L_g1
N_13
G_1
R_g1-in
L_g1-in
N_16
V_dd1
C_gs1-ex
L_g1-l
(11)
N_14
(12)
C_gs1
I_ch1
(10)
C_diode1
L_a1
L_s1-l
SS_1
L_ss1-in
L_s1-in
L_ss1
S_1
L_s1-ex
I_o
L_out
N_18
L_d2-ex
I_d2
R_2
R_4
SW_2
D_2
I_diode2
L_d2-in
L_c2
Diode_2
I_g2-1
I_g2
C_gd2
N_15
C_ds2
N_16
R_g2+R_dr2
L_g2
N_13
G_2
R_g2-in
L_g2-in
C_out
R_out
V_dd2
C_gs2-ex
L_g2-l
(11)
N_14
(12)
C_gs2
I_f2
(10)
C_diode2
L_a2
L_s2-l
SS_2
L_ss2-in
L_s2-in
L_ss2
S_2
L_s2-ex
GND

Fig. 2-2. Switching behavior model of one phase-leg in [18].

Another weakness of the above analytical switch model is the inaccuracy or neglection of some strong nonlinearity of device parameters. E.g., transconductance is assumed as a fixed value in [12, 16], but actually, it is a function of the gate to source voltage v_{gs} and the drain current i_d, being considered in [20]. And, a nonlinear relationship between $C_{gs}(Q_g)$ and V_{gs} is used to further improve the accuracy of the switching model. With such efforts, a maximum 20 % error can be achieved for the prediction of the switching speed and switching loss over a wide load range. Furthermore, according to Xie [18, 19], the assumption of a controlled current source with a variable gain (transconductance) in the saturation region is still not sufficiently accurate, and I-V curve including both transfer and output characteristics in the saturation region should be modeled and utilized. To have better fitting results of I-V characteristics, the combination of a polynomial function, exponential function, Gaussian distribution function and inverse trigonometric function are applied to curve fitting the I-V curves for transfer and output characteristics. With such efforts, the channel current can be modeled more accurately compared with a simple controlled current source model, and the analytical waveforms can match the experimental waveforms better than the PSPICE model from the device manufacturer.

In addition, a lack of modeling of damping parasitic ringing is a common issue in the analytical switching model [21]. Even though the magnitude of the first resonant peak can be reproduced very accurately by the analytical switch model, the damping process of the parasitic ringing is difficult to match since the ac resistance of circuits is not considered. An exponential decay rate coefficient is added into the switch model during the turn-off in [21] to solve this issue.

2.1.2 Device Loss Model

The power switch loss model includes the switching loss model and the conduction loss model. Conduction loss calculation is relatively easy with on-resistance and channel current waveforms. At a known operating junction temperature, the corrected on-resistance of device channel is obtained from datasheet provided by the manufacturer, and the RMS value of device channel current can be derived in an analytical form or calculated from simulation results. With these inputs, the conduction loss can be calculated without obvious deviations.

For switching loss, the widely applied analytical model in [22] has a linear assumption on the switching waveforms. Then, with the assumption, the switching loss can be derived by calculating the overlap area of voltage and current waveforms during switching intervals. The classical one is given as follows at inductive load condition:

$$\begin{aligned} E_{sw} &= \frac{1}{2} v_{dc} i_L t_{sw} \\ t_{sw} &= \frac{Q_{gd}}{i_g} = \frac{Q_{gd} R_g}{V_{dr} - V_{miller}} \end{aligned} \tag{2.1}$$

where E_{sw} is the dissipated energy during switching transition, and v_{dc} and i_L are the voltage and current applied for the power switch, t_{sw} is the switching transition time, which can be estimated using the gate current and the gate-drain charge during miller plateau.

However, the analytical model with Eq. (2.1) cannot achieve a satisfying accuracy compared with experimental results since switching waveforms are varied with different types of power switches, and the model is also too simplified without considering the parasitics, layout, and device parameters. Some research [23], [20], [24] uses advanced switch behavior models to calculate the switching loss. The switching waveform can be derived analytically with the switch behavior model by considering the parasitics and device parameters, and the switching loss is calculated with the integral of the derived voltage and current waveforms. Such switch behavior models can achieve a much higher accuracy of switching loss calculation than the linear switching loss model, but the issue is the additional effort needed to extract the parasitics of layout and to obtain device parameters at different operating conditions from static characterizations.

Another way to estimate the switching loss is to use the loss data from a double pulse test (DPT) for the calculation. Fig. 2-3 in the literature [25] shows the typical testing waveforms and switching energy during turn-on and turn-off are calculated respectively. The layout of a DPT board must be similar to the one of the power stage PCB, achieving a closed power loop parasitic inductance for the switching loss evaluation. The delicate measuring procedures and careful selection of sensors for high accuracy are reported in the literature [26-28]. The switching energies at different voltage and current levels are measured for loss calculation and cooling design, and the measured data can help converter design achieve a high accurate switching loss calculation with the same gate drive design, same layout, and same gate resistance selection compared with real converter implementation. Nonetheless, the insertion of the current shunt adding extra power loop inductance may cause uncertainty of loss data. Also, the accuracy of DPT testing results highly depend on the skew of the probes, requiring a very careful post-processing procedure.

Recently, to achieve a more accurate switching data, Anderson [29] and Rothmund [30] presents an accurate calorimetric switching loss measurement. Fig. 2-4 shows the test setup of calorimetric measurement of switching loss by thermal measurements instead of electrical measurements, and the device under test (DUT) creates power loss with a continuous operation that eliminates measurements of electrical variables at the high frequency and fast switching speed. The issue of this experiment-oriented scheme is too time consuming and testing with all device candidates for the paper design can take a long time.

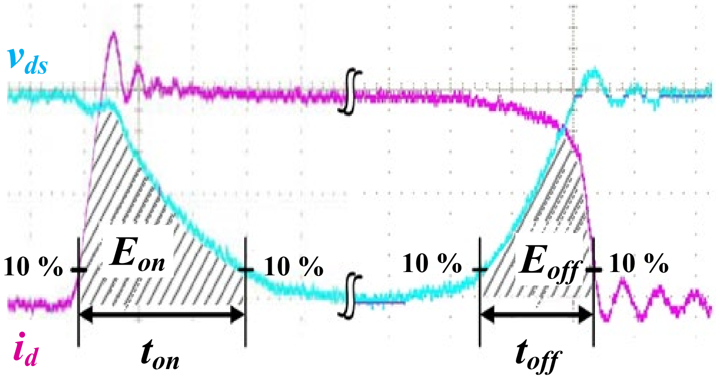


Fig. 2-3. Calculation of switching times and energies by double pulse testing [25].

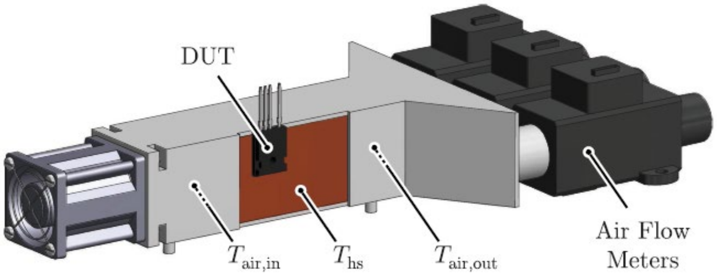


Fig. 2-4. Illustration of setup for calorimetric switching loss measurement in [29].

A compromised way of obtaining measured switching energy data is from datasheets of the selected device [31, 32], but the switching energy data from the datasheet is always for one specific testing voltage and current. Hence, a linear scaling method in [31] as Eq. (2.2) is used to calculate the switching loss at other applied voltages and currents.

$$P_{sw} = \sum_{t=t_1}^{t_{end}} \frac{V_{dc} i_{a\_ti}}{V_{test} I_{test}} (E_{on} + E_{off}) \tag{2.2}$$

where E_{on} and E_{off} are measured switching energy during turn-on and turn-off at a specific testing voltage V_{test} and current I_{test}, i_{a_ti} is the instantaneous phase current during turn-on and turn-off.

Since Eq. (2.2) does not consider non-linear characteristic of device parameters, e.g., C_{oss} variation with v_{ds}, and the gate resistance selection, so the loss estimation will not be accurate as of the loss calculation by measured data without scaling.

2.1.3 Thermal Model for Power Devices

Cooling design for power switches can be different in terms of different packages of power semiconductors categorized as TO-type packages (or other packages with a thermal pad directly attached to heatsinks) and surface mount packages.

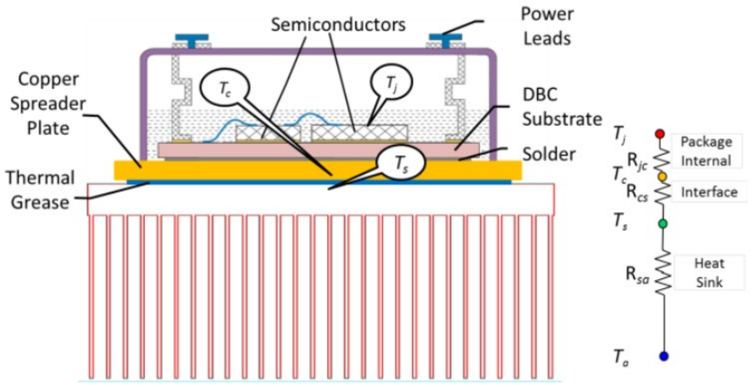

Semiconductors
Power Leads
Copper Spreader Plate
T_c
T_j
DBC Substrate
Solder
T_s
Thermal Grease
T_j
R_{jc}
Package Internal
T_c
R_{cs}
Interface
T_s
R_{sa}
Heat Sink
T_a

Fig. 2-5. Steady-state thermal modeling for TO-type packages in [33].

Steady-state thermal modeling for power devices with TO-type packages is illustrated in Fig. 2-5 in reference [33]. Generally, a thermal interface material is inserted between the case of power devices and the surface of heatsinks, and its thermal resistance can be calculated:

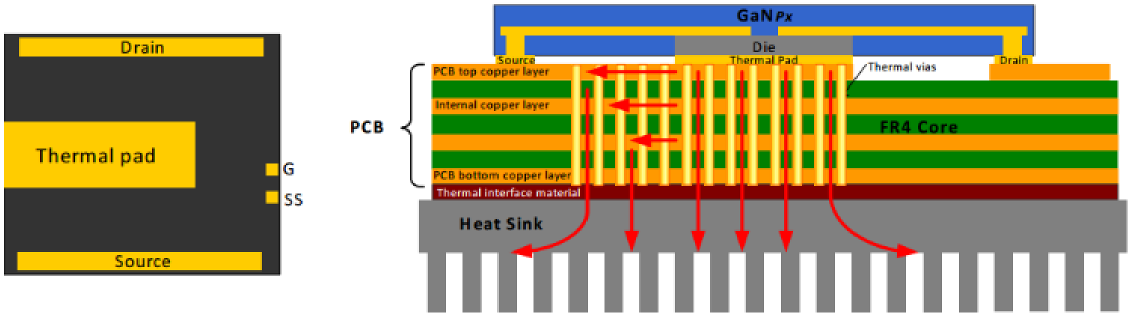
$$R_{thc-hs} = \frac{L}{kA} \tag{2.3}$$

where L is the thickness of the thermal interface material, A is 1.5 times of the device area and k is the thermal conductivity of the thermal interface material.

With the thermal resistance from the case of devices to the heatsink, the required thermal resistance from the heatsink to ambient can be calculated:

$$R_{th-hs} = \frac{T_j - T_{am} - P_h \cdot (R_{thc-hs} + R_{thj-c})}{P_{tol}} \tag{2.4}$$

where T_j is the desired junction temperature, T_{am} is the ambient temperature, P_h is the highest power loss of devices, P_{tol} is the total power loss of all devices.


Drain
Thermal pad
G
SS
Source
GaN Px
Die
Source
Thermal Pad
Drain
Thermal vias
PCB
PCB top copper layer
Internal copper layer
FR4 Core
PCB bottom copper layer
Thermal interface material
Heat Sink

GS66508P package area 79.5 mm^2

(a) Bottom view

(b) Cross section view of package thermal path using PCB cooling

Fig. 2-6. Thermal flow of surface mount power devices through PCB in [34].

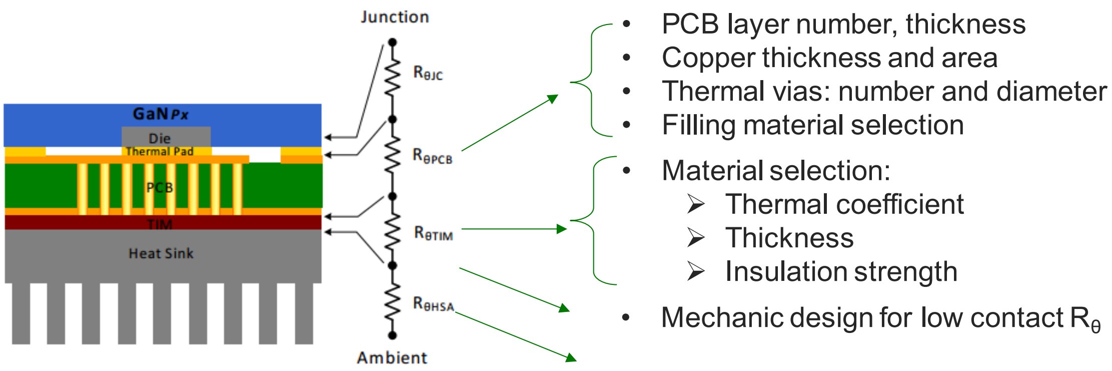

Junction
GaN Px
Die
Thermal Pad
PCB
TIM
Heat Sink
RθJC
RθPCB
RθTIM
RθHSA
Ambient
PCB layer number, thickness
Copper thickness and area
Thermal vias: number and diameter
Filling material selection
Material selection:
Thermal coefficient
Thickness
Insulation strength
Mechanic design for low contact Rθ

Fig. 2-7. Steady-state thermal modeling for surface mount packages in [35].

Compared with the cooling design in Fig. 2-5, the surface mount package shown in Fig. 2-6 cannot be directly attached to the surface of heatsinks while the thermal pad of such packages has to be soldered on the PCB. As a result, the thermal flow from power switches to heatsinks must go through thermal vias inside the PCB, and the additional thermal resistance of the PCB, determined by the PCB layer number, thickness, the number and diameter of thermal vias, is added to the total thermal resistance from the junction to the heatsink.

Steady-state thermal modeling for power devices with surface-mount packages is illustrated in Fig. 2-7 from the reference [35]. Since the additional PCB thermal resistance is added in the thermal flow, the required heatsink thermal resistance for a surface mount device is updated as:

$$R_{th-hs} = \frac{T_j - T_{am} - P_h \cdot (R_{thc-hs} + R_{thj-c} + R_{thPCB})}{P_{tol}} \tag{2.5}$$

2.2 Passive Components Modeling in Power Electronics

Passive components in power electronics converters include inductors, capacitors, busbars, and a cooling system. Inductors and capacitors are always applied for power filters, EMI filters and other auxiliary circuit blocks, e.g., ZVS realization tank and voltage snubber. Busbar is designed as connecting bridge between the dc-link voltage and devices, playing an important role to determine the switching behavior and loss. Cooling system helps transfer the dissipated power loss of the switches to the ambient, achieving a safe operating condition of power switches. All those components must be designed carefully with reasonable physical models, and the accurate model can shrink the gap between the design results and real operating performance of power electronics converters and reduce the trial-and-error efforts in the testing and implementation stage. This section will investigate the state-of-art models for the passive components in power electronics converters.

2.2.1 Magnetics Core Inductor

Once the inductance of the magnetic-core inductor is decided in the design procedure of the electrical design, the physical design of the magnetic-core inductor requires the inductance model, the loss model, and the thermal model to determine the core size, turn number, wire gauge, and temperature rise. The review in this section will cover three models required for the physical design in terms of inductance, loss and temperature rise calculations. Also, the parasitic capacitance model and leakage inductance model are investigated to better predict the performance of filters.

A. Impedance model

For conventional inductor design, with the selected magnetics material and core size, the turns number calculation is needed to determine the desired inductance or to prevent the saturation of magnetic cores [36].

For ferrite E-shape cores, since they generally do not have an air gap inside the core, the turns number is calculated based on the prevention of the saturation, and then the length of the centralized airgap is calculated to achieve the desired inductance [36]. The equation derivation of turns number in this case is given as follows with two basic formulae

$$\begin{cases} U=L\dfrac{di}{dt} \\ U=N\dfrac{d\phi}{dt} \end{cases} \Rightarrow N\frac{BA_e}{dt}=L\frac{di}{dt} \Rightarrow N=\frac{LI_{pk}}{B_{\max}A_e} \tag{2.6}$$

where N is the turns number, I_{pk} is the peak value of the inductor current, B_{max} is the maximum magnetic flux the magnetics core can operate, A_e is the cross-sectional area of cores. With the turns number, then the length of the centralized airgap is roughly estimated as

$$l_g \approx \frac{N^2}{\Re_g}=\frac{\mu_0 A_e N^2}{L} \tag{2.7}$$

where $\Re_g$ is the reluctance of the airgap, μ_0 is the vacuum permeability, and μ_r is the relative permeability. Eq. (2.7) is correct only when the assumption $\mu_r l_g/l_c \gg 1$ is made. In the implementation, the length of airgap is adjusted manually to achieve a desired inductance.

For powdered iron and amorphous alloys cores, a distributed air gap structure is usually adopted instead of the centralized airgap in ferrite cores [37]. Since the manufacturer adjusts the density of airgap and core size to obtain different properties of powder cores for different applications, no universal accurate analytical model can be developed to predict the inductance, especially for complex core shapes. Instead, a core inductance factor provided by manufacturers is used to estimate the required inductance. The core inductance factor is defined as the inductance per single turn squared

$$A_L=\frac{L}{N^2}=\frac{\mu_r\mu_0 A_e}{l_c}=\frac{1}{\Re}\ \left(\frac{H}{turn^2}\right) \tag{2.8}$$

A_L is a unique value for powder cores with different materials, shapes and sizes, and it can be found in the datasheet of powder cores from manufacturers. With A_L, the turn number is calculated by Eq. (2.8). Then the magnetic field strength H is calculated with $N*I$ to check whether the peak H exceeds the saturation of magnetic cores. If yes, a larger core is required to avoid saturation.

The above two inductance models are widely applied in the power filter design. With a specific operating frequency, they can provide a reasonable starting point to implement an inductor in power filters based on the parameters provided at the operating frequency. However, they do not incorporate the non-linear characteristics of permeability in the inductance model. Also, for EMI filter design, an impedance curve of inductors at the EMI measuring range needs to be known for better prediction of the attenuation of EMI filters.

To get more accurate models to predict the performance of inductors, a lumped model of one inductor is proposed in [10]. Fig. 2-8 gives the lumped circuits model of one inductor, and it includes the series inductance, the series resistance and the parallel parasitic winding capacitance. The inductance and resistance parts are frequency-dependent and varied with operating frequency. Therefore, the frequency-dependent permeability models are used for the calculation of inductance and core-loss equivalent resistance at one operating frequency. There are two models, Diffusion like model [38] and Nomura's model [39], that are developed from curve fitting for frequency-dependent permeability. According to [40], Nomura's model shows smaller errors at the whole frequency range compared with Diffusion like model, which is

$$\mu(f) = \frac{10^{a_2 \log_{10}(f) + b_2}}{1 + 10^{(a_2 - a_1)\log_{10}(f) + (b_2 - b_1)}} \tag{2.9}$$

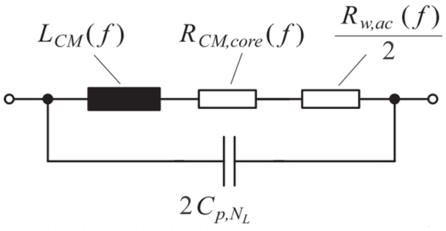


Fig. 2-8. Lumped circuits model of inductors in [10].

In addition, the winding-loss equivalent resistance is obtained from the winding loss calculation [41]. For the parasitic capacitance of the winding, comprehensive modeling of turn-to-turn capacitance and turn-to-core capacitance considering both air and insulation material is proposed in [42]. However, it assumes the arrangement of turns is compact, and no gap between the neighboring turns. Since this assumption cannot be always the situation for the inductors' winding structure, Kovacic [43] improved the model by considering the real arrangement of turns. With Kovacic's model, the error of turn-to-turn capacitance is only 13.8% compared with FEM simulations.

Except for the lumped circuits model of inductors, the per-turn model considering the self and mutual inductance of each turn is presented in [43]. Although it achieves higher accuracy theoretically, its derivation is highly dependent on the geometry of windings that may be validated for only one specific winding structure and core shape. Besides, some behavior models [44-46] are developed for accurate simulations, but they cannot be applied for the paper design stage since they require scattering parameters of inductors from the network analyzer, which is not preferable for the paper design.

The leakage model is also important for CM inductors design. By constructing an equivalent symmetrical geometry about the z-axis plane for toroidal cores, reference [47] developed a set of self and mutual impedance formulas directly from Maxwell's equation for coils on ferromagnetic cores in 2-D dimension. Although the model in paper [47] achieves an ultimate accuracy equivalent to a 2-D simulation with a FEM software, no closed-form solution is provided for simple use. Either Bessel functions or numerical method must be used to solve the equations with integrals, rendering them not applicable for engineering practice. Paper [48] further simplified the impedance derivation of toroidal structures with 1-D dimension assumption (magnetic fields only change with the thickness of windings), and it is very effective for toroidal transformers with the bifilar windings or no air gap structures to minimize the leakage flux in the air. However, it is not a common practice in the CM inductor design for EMI application, and separate winding structures are more popular due to the usage of leakage inductance as the DM inductance.

To obtain a more applicable model, Nave [49] proposed a leakage inductance model based on his finding that the magnetic fields of rod core and the leakage flux of toroidal CM core are quite similar. Then the leakage inductance model of toroidal CM cores was derived with the existing rod core model [49]. However, the error of Nave's model is up to 30% when the winding angle becomes larger with the increase of turns number. Heldwein [10] improved Nave's model by amending the effective leakage flux path length, but it only increases accuracy when the winding angle is smaller than 30° compared with Nave's model.

Zhou [50] developed a highly accurate model with Artificial Neutral Network fitting of FEM simulation results by sweeping the selected input variables, achieving only 2.4 % error. Nonetheless, the proposed method needs quite a lot of effort to obtain the training data with FEM simulations, and for different cores, it needs to redo the simulations to collect data for the model training.

B. Loss model

No complete physics model is developed for the magnetic core loss since the physical mechanisms of core loss involves hysteresis loss, eddy current losses, and residual losses (also called relaxation losses). Only is hysteresis loss physical model developed in [51], but the models are difficult to parameterize and the other two physical mechanisms-oriented losses are too complicated to model analytically. Steinmetz equation is developed for core loss calculation at a sinusoidal excitation

$$P = kf^{\alpha} B^{\beta} \tag{2.10}$$

where P is the core loss, f is the frequency of the sinusoidal waveform, B is the maximum magnetic flux density, α and β are the Steinmetz coefficients. In essence, Steinmetz equation is a curve-fitting function based on the loss measurement, so loss coefficients are valid only in one specific operating frequency and flux density range.

However, in power electronics applications, since the most current excitations of inductors are not sinusoidal waveforms and Flourier analysis cannot be applied for core loss calculations due to non-linearity of core loss equations, the utilization of Steinmetz equation is very limited. A modified Steinmetz equation (MSE) is proposed in 1996 [51, 52] based on physical motivation that domain wall motion loss depends on *dB/dt*. With this discovery, an equivalent frequency from a weighted average of *dB/dt* is derived

$$f_{eq} = \frac{2}{\Delta B^2 \pi^2} \int_0^T \left(\frac{dB}{dt} \right)^2 dt \tag{2.11}$$

Then Eq. (2.11) is substituted into the initial Steinmetz equation (2.10) to calculate the core loss. However, the error compared with the measured loss is still large in some cases since the averaging of equivalent frequency is too simplified to reflect all details of excitation waveforms.

To further improve the accuracy, an instantaneous core loss model is developed in [53], only depending on instantaneous *B*, *dB/dt*. With a combination of instantaneous core loss hypothesis and Steinmetz equation, a generalized Steinmetz equation (GSE) is proposed for arbitrary excitation waveforms, which is

$$P(t) = k_1 \left|\frac{dB}{dt}\right|^{\alpha} \left|B(t)\right|^{\beta\text{-}\alpha} \tag{2.12}$$

Nonetheless, testing results in [54] show GSE still is not accurate since core losses do not only dependent on *B(t)*, *dB/dt* but also the whole cycle. Hence, an improved GSE (iGSE) hypothesis is proposed in [55]. Compared with GSE, IGSE separated the excitation waveforms as minor loops and major loops, and each loop applies *ΔB* to replace instantaneous *B(t)* in Eq. (2.12), reflecting the detailed variations of the excitation of waveforms. The expression of IGSE is given as

$$P(t) = k_1 \left|\frac{dB}{dt}\right|^{\alpha} \left|\Delta B\right|^{\beta\text{-}\alpha} \tag{2.13}$$

The comparison results are given in [55], and IGSE shows much higher accuracy than GSE and MSE for arbitrary excitation waveforms. However, residual losses caused by the relaxation effect is still not included in IGSE. Mühlethaler [56] further improve IGSE and develop a new equation called as I^2GSE, considering the relaxation effect by adding extra terms into IGSE.

However, there are still two factors not included either in IGSE or I^2GSE. The first is dc bias not considered, and the equation cannot reflect core loss correctly when the excitation current has a dc component. The second is Steinmetz coefficients are valid only for a specific frequency, and different operating frequencies have different sets of Steinmetz coefficients. As a result, IGSE or I^2GSE may have larger errors when the excitation waveforms have abundant harmonics.

The winding loss includes two parts. One is dc loss and the other one is ac loss. For dc loss, it is determined by the copper dc resistance at the operating temperature. However, for ac loss, two factors including the proximity effect and skin effect affect the total ac loss, which is represented by the ac resistance under different operating frequencies and winding structures. Hence, the idea for calculating the copper loss is to derive the respective equivalent ac resistance for one specific winding structure at different operating frequencies. With the derived ac resistance at different frequencies, the total loss can be obtained by summing up the separated losses at different frequencies based on FFT analysis of the inductor current.

For ac resistance calculation for multi-layer windings, the most common methods are Larson method [57] shown Eq. (2.14) and Ferreira method [58] shown in Eq. (2.15), which are developed from Dowell method.

$$R_{ac-m} = R_{dc0} \cdot \frac{\xi}{2}[\frac{\sinh\xi + \sin\xi}{\cosh\xi - \cos\xi} + \frac{2}{3}(m-1)^2 \frac{\sinh\xi - \sin\xi}{\cosh\xi + \cos\xi}] \tag{2.14}$$

where R_{dc0} is the dc resistance, R_{ac-m} is the ac resistance of *m-th* layer in the winding, $\xi = d\sqrt{\pi}/2\delta$ is the thickness of the conductor foil normalized with respect to the skin depth $\delta = 1/\sqrt{\pi\mu_r\mu_o\sigma}$ and σ is the resistivity of the copper, m is the specific number of layers and d is the diameter of the round wire.

$$R_{ac-m} = R_{dc0} \cdot \frac{\xi(\eta)}{2}[\frac{\sinh\xi(\eta) + \sin\xi(\eta)}{\cosh\xi(\eta) - \cos\xi(\eta)} + \eta^2(2m-1)^2 \frac{\sinh\xi(\eta) - \sin\xi(\eta)}{\cosh\xi(\eta) + \cos\xi(\eta)}] \tag{2.15}$$

where $\eta=n*d/W$ is porosity factor (packing factor), n is the turns number and W is the width of the bobbin, $\xi(\eta) = d\sqrt{\pi}/2\delta(\eta)$ is the thickness of the conductor foil normalized with respect to the effective skin depth $\delta(\eta) = 1/\sqrt{\pi\mu_r\mu_o\sigma\eta}$, which is related to the geometrical arrangement of winding that is porosity factor.

For Larson method, it is derived under very closely packed windings and no relation with packing structure and it is only a 1-D dimensional calculation method. But Ferreira method tries to introduce some geometrical skin depth to modify the loss to reflect the loss influence caused by the geometry. However, for Ferreira's method, skin depth, on the other hand, is a physical material constant and cannot be dependent on geometry, so it causes some errors when the round wires are closely packed. The paper [59] also reports that the Larson method is most accurate for closely packed windings and Ferreira method is most accurate for loosely packed windings. When the porosity factor is lower than 0.8, Ferreira method is more accurate. Otherwise, Larson method is more accurate.

C. Thermal model

The thermal design of inductors is classified into three levels with different complexities [36]. Level 0 is a fast design approach with an empirical formula based on the testing results, provided by some handbooks of the inductor design [60]. The empirical formula only requires the estimated box volume of the inductor and airflow speed, and it is quite simple to calculate. However, it may be not accurate when the core shape and winding structure are changed compared with that for testing and fitting.

Level 1 thermal design is a single thermal resistance design, and the thermal resistance from the inductor to ambient is derived. The thermal model of inductors varied with different cooling methods. For passive cooling, the model is from reference [61] as follows:

$$\begin{aligned} T_{\text{choke}} &\approx R_{th}(P_{cu}+P_{fe}) \\ R_{th} &= [24(\frac{V_{eff}}{1cm^3})]^{-0.49} \end{aligned} \tag{2.16}$$

For forced convection cooling, the model from the reference [36] is given

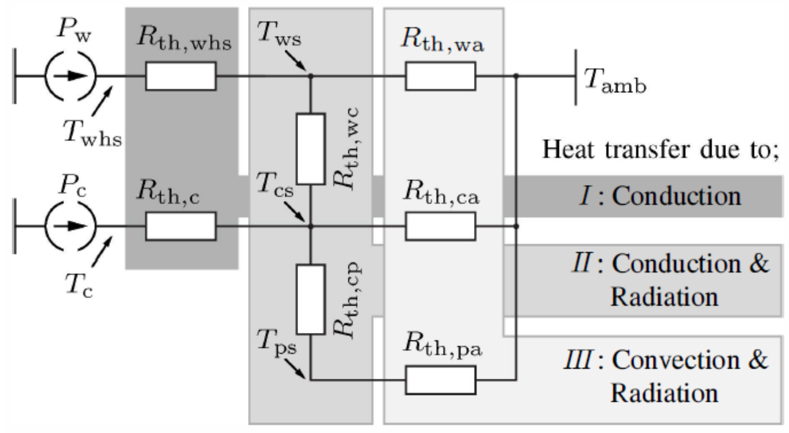

P_w
$R_{th,whs}$
T_{ws}
$R_{th,wa}$
T_{amb}
T_{whs}
$R_{th,wc}$
Heat transfer due to;
P_c
$R_{th,c}$
T_{cs}
$R_{th,ca}$
I : Conduction
T_c
II : Conduction & Radiation
$R_{th,cp}$
T_{ps}
$R_{th,pa}$
III : Convection & Radiation

Fig. 2-9. Illustration of thermal resistance network modeling for level 3 thermal design of inductors in [62].

$$\begin{aligned} h_c &\approx (3.33 + 4.8v^{0.8})L^{-0.288} \\ R_{th} &= \frac{1}{h_c S_L} \end{aligned} \tag{2.17}$$

where h_c is the heat transfer coefficient, v is the airflow speed, L is the length of a heatsink, S_L is the approximated box surface area.

Level 2 thermal design utilizes a resistance network [62] illustrated in Fig. 2-9. Thermal resistance from the core to the winding, the core to ambient, and the winding to ambient are considered. With such a detailed model, the temperature of different places of the inductor can be evaluated and the highest temperature point of the inductor can be identified.

2.2.2 Capacitor

Aluminum electrolytic capacitors, film capacitors, and ceramic capacitors are three most commonly applied capacitors in the power electronics applications, and all of them can be modeled by a series LRC circuit to represent the impedance [63], which is expressed as

$$Z_C = j\omega L_{ESL} + \frac{1}{j\omega C} + R_{ESR} \tag{2.18}$$

In Eq. (2.18), equivalent series inductance (ESL) L_{ESL} is calculated based on the self-resonant frequency of the impedance curve from the capacitor's datasheet, and self-resonant frequency is

$$f_{self-reson} = \frac{1}{2\pi\sqrt{L_{ESL}C}} \tag{2.19}$$

Equivalent series resistance (ESR) R_{ESR} is a frequency-dependent parameter determined by the material characteristic and connection series resistance [64]. As shown in Fig. 2-10, ESR at low frequencies is larger than one at medium to high frequencies since ESR is dominated by the dielectric losses in low frequency while resistive loss due to conduction determined ESR at medium to high frequencies. However, at very high frequency (>10 MHz), ESR will increase by $\sqrt{f}$ due to skin effect.

The capacitance varies with temperature for all three type capacitors, and especially for ceramic capacitors, its capacitance can change with applied voltage for X5R and X7R materials [64]. The above information usually can be obtained from manufacturers' datasheets, and an impedance curve in the datasheet is applied to derive the equivalent circuits.

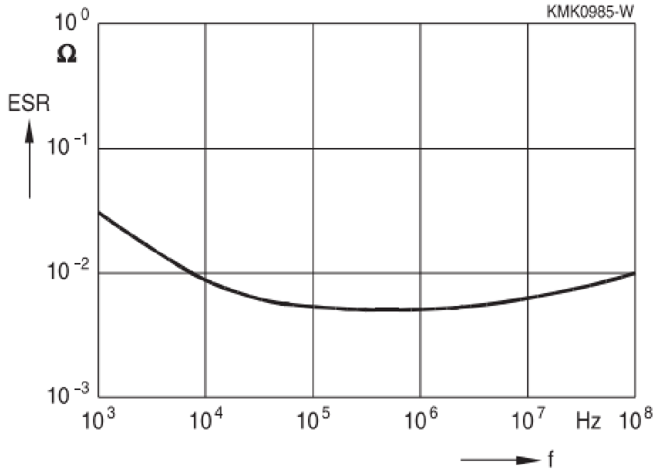


Fig. 2-10. Typical ESR curve with frequency in [65].

Except for some parameters in the impedance model, some electrical parameters are also frequency-dependent. Ac voltage rating of film capacitors highly depends on the frequency [65]. At the low frequency range, the ac voltage rating keeps fixed while it drops with a constant slope when the applied operating frequency increases.

Since some parameters in LRC equivalent circuits are frequency-varying, some behavior models with high order multi-stag LRC circuits are proposed in [66-68] to model the measured impedance curve for the whole frequency range. However, the high order models require many fitting efforts, and for each capacitor, a group of dedicated parameters must be used for the models.

The loss calculation of capacitors requires ESR value and RMS value of the capacitor current. Sometimes the datasheet gives dissipation factor (DF) at several frequencies instead of the impedance curve or ESR value, and DF is defined as

$$DF = \tan\delta = 2\pi f \cdot C \cdot ESR \tag{2.20}$$

Since ESR is a frequency-dependent value, the RMS current at each frequency is obtained by the FFT analysis of the capacitor current. Then, the capacitor loss is calculated as

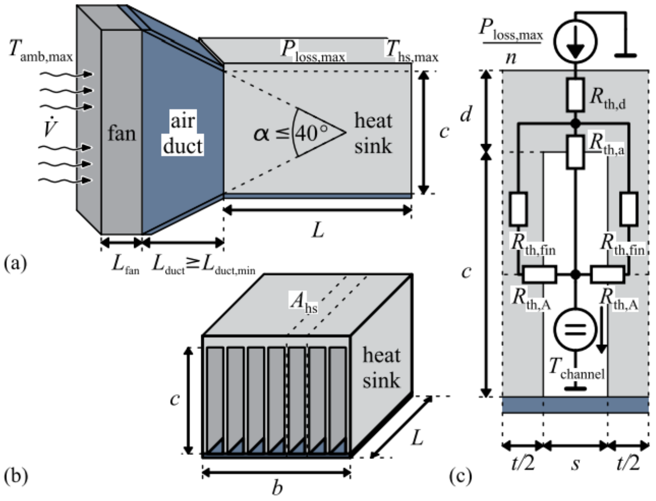
$$P_{total} = \sum_{f_{line}}^{Nf_{line}} I^2_{rms\_f} ESR_f \tag{2.21}$$

where P_{total} is the sum of the capacitor loss, I_{rms_f} is the RMS value of harmonics of the capacitor current, and ESR_f is the ESR value at different frequencies.

2.2.3 Heatsink and Fan

The most common cooling system in power electronics applications includes a fan, an air duct and an extruded heatsink [69] shown in Fig. 2-11. The thermal model of such a cooling system is developed in [70-72] involving the heat conduction and heat convection, but heat radiation is usually neglected due to its small impacts on the thermal resistance.

The thermal resistance of the heatsink is affected by the thickness and the number of fins, the length, the operating temperature, airflow speed. The design iteration of the cooling design is presented in [73-75]. Once the required thermal resistance is confirmed based on the thermal model given in Section 2.1.3, for a given airflow speed and operating temperature, the thickness and the number of fins, the dimensions of a heatsink are optimized to achieve the lowest weight or volume.



$T_{amb,max}$
$\dot{V}$
fan
air duct
$\alpha \leq 40°$
heat sink
$P_{loss,max}$
$T_{hs,max}$
c
L
L_{fan}
$L_{duct} \geq L_{duct,min}$
(a)
A_{hs}
heat sink
c
L
b
(b)
$\frac{P_{loss,max}}{n}$
$R_{th,d}$
d
$R_{th,a}$
c
$R_{th,fin}$
$R_{th,fin}$
$R_{th,A}$
$R_{th,A}$
$T_{channel}$
t/2
s
t/2
(c)

Fig. 2-11. Illustration of a cooling system with extruded heatsink and fan [69].

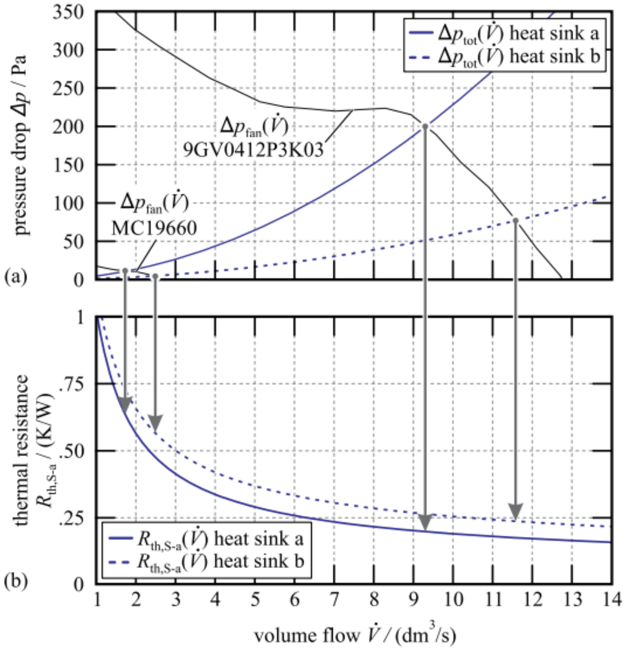


Fig. 2-12. Illustration of dynamic fluid models on cooling design [69].

However, the above design methods do not consider the dynamic fluid model of the fans and heatsinks. Ning [76] and Gammeter [69] further propose a new design procedure incorporated with the pressure drop models of fans and heatsinks. Fig. 2-12 shows how the pressure drop of fans and heatsinks impact the operating point of fan and the thermal resistance of heatsinks, and the volume flow of fans varied with different dimensions of heatsinks.

2.2.4 Busbar and PCB Layout

Power loop parasitic inductance has an influence on the switching loss and the voltage stress during the turn-off [77, 78]. Thus, power loops parasitic inductance minimization is a critical aspect of the design stage. Busbar and PCB are two general ways to connect power switches and dc-link capacitors in inverters. Busbar is more preferred in the high power application with power modules while PCB is more chosen for the low to medium power application with discrete power devices.

For the PCB layout, a general concept called the magnetic field cancellation is applied to reduce the power loop parasitic inductance [79]. With the help of the internal layer of power plane, a minimized vertical power loop area can be achieved for the parasitics inductance reduction. Also, some ceramic decoupling capacitors with very small ESL are suggested to be placed as close as possible to the power devices, helping to reduce the power loop area and relieve overvoltage issues during fast turn-off for wide bandgap devices [17].

The planar laminated busbar structure is effective and general design to realize the low stray inductance, achieving the voltage spike suppression and EMI noise containments. Reference [80, 81] first uses the impedance model by considering the self-inductance and mutual-inductance of each metal sheet to derive the equivalent stray inductance for a laminated busbar design. However, such a modeling method does not consider the number and shape of holes and apertures for a busbar design. To extract the stray inductance more accurately, numerical analysis methods are applied, such as finite element analysis (FEA) [82-84], and partial element equivalent circuit (PEEC) [78, 85]. FEA applies a differential form of MAXWELL's equations to solve the magnetic or electrical filed variables while PECC uses an integral form of MAXWELL's equations to solve the circuit-level variables. FEA software like Q3D from ANSYS is more widely applied in the extraction of the stray inductance of the busbar design than PEEC method, since the commercial available FEM tool is a perfect tool with integration with all required functions, e.g., field vector or intensity plot, the impedance matrix extraction, current density distribution and so on. For PEEC, it can directly calculate the inductance of a specific geometry of a busbar, however, the circuit variables like voltage and current needs to be solved with a circuit solver like PSPICE, and field variables require more post-processing calculations, but one of the advantages of PEEC compared with FEA is more time-efficient to only extract the stray inductance [86] instead of getting filed results.

The different arrangements for multi-layer laminated busbar for multi-level converters have been analyzed and compared in [77] with FEA simulations. The conclusion is the stacking order of different layers should be symmetrical to achieve the minimum stray inductance. Moreover, the busbar should also be designed with the shorter length and different layers should be placed as close as possible with satisfying the insulation and thermal limits.

Nonetheless, all design considerations for busbar design are at the implementation stage, and no link is established between the switching speed and the geometry design of the busbar in the paper design stage. The stray inductance of layout not only can determine the maximum switching speed considering the voltage stress but also can impact the switching loss and cooling design in terms of the gate resistance selection for the switching speed.

2.3 Design Optimization in Power Electronics Design

The power electronics converter design requires knowledge from different areas such as electrical, thermal, mechanical and magnetic [87-90], and some design variables have impacts on different parts of converters. For example, the gate resistance selection determines the switching speed, affecting EMI noise spectrum, cooling design of switches, voltage spike during turn-off. As a result, plenty of trade-off design problems exist in the power electronics design, and different design approaches and optimization schemes are applied to solve trade-off problems for the optimal design result. In this section, optimization algorithms in operation research have been reviewed, and applicable algorithms for the power electronics design are identified from the literature. Also, from the literature review, design optimizations in power electronics design are classified into two categories: local optimizations for a specific trade-off problem only focusing on one or two design variables and global optimizations for the whole converter design with considering all design variables. Both optimization schemes are investigated and reviewed in this section.

2.3.1 Optimization Algorithm Review

A general optimization problem involves three parts: design variables, constraints and objective function. The essence of an optimization problem is to find the best solution from all feasible solutions under certain design constraints [91]. Indeed, design problems in power electronics can be fitted into three parts very well and Fig. 2-13 from paper [89] displays fitting results in point of optimization view.

The optimization algorithms are generally divided into two categories: linear optimizations and non-linear optimizations [92]. In theory, a global optimal solution can be definitively obtained in a linear programming problem with certain algorithms such as simplex method, duality theory and interior point method [93]. However, for non-linear optimizations, only can local optimal results be achieved by different non-linear optimization methods such as gradient-based algorithms, penalty function-based algorithms, heuristic algorithms and the linear fractional programming [92]. Different initial sets of design input variables need to be set as many as possible for searching better local optima while global optima searching in the non-linear programming is NP (non-deterministic polynomial-time) hard problem [92]. The classification of different optimization algorithms is shown in Fig. 2-14.

As introduced in Chapter 1, the design problems in power electronics is a non-linear programming and non-convex problem, and the most difficult part in power electronics design is the formulation of the objective function for the whole converter performance, e.g., the converter efficiency and power density, involving hundreds of design input variables and plenty of trade-off design problems. In addition, most equations or models applied in power electronics design are strongly nonlinear, e.g., magnetic core loss, EMI corner frequency and so on, and the design input variables have both discrete (turns number) and continuous (inductance and capacitance) types. Therefore, no well-developed linear programming algorithm can be directly applied for power electronics design problems. In essence, the power electronics design for system-level optimization is a nonconvex optimization problem, and global optima searching in non-linear programming is an NP-hard problem. As a result, optimization methodologies have not been widely applied in the area of power electronics, especially for the whole power stage design. The brute-force algorithm with a small step and the well-defined design space is more popular in power electronics system-level design [62].

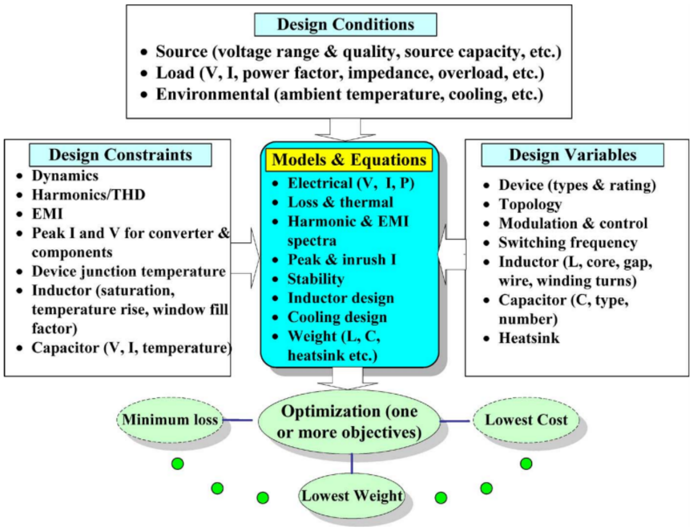
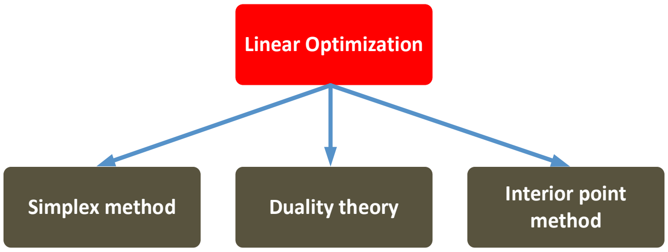
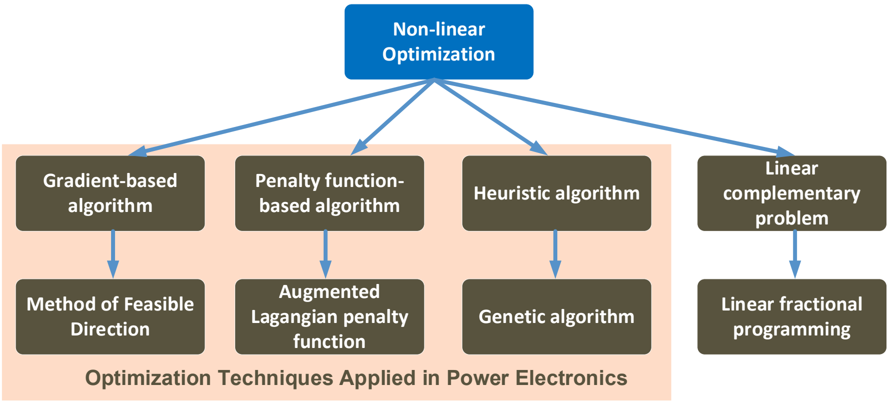

Design Conditions
• Source (voltage range & quality, source capacity, etc.)
• Load (V, I, power factor, impedance, overload, etc.)
• Environmental (ambient temperature, cooling, etc.)
Design Constraints
• Dynamics
• Harmonics/THD
• EMI
• Peak I and V for converter & components
• Device junction temperature
• Inductor (saturation, temperature rise, window fill factor)
• Capacitor (V, I, temperature)
Models & Equations
• Electrical (V, I, P)
• Loss & thermal
• Harmonic & EMI spectra
• Peak & inrush I
• Stability
• Inductor design
• Cooling design
• Weight (L, C, heatsink etc.)
Design Variables
• Device (types & rating)
• Topology
• Modulation & control
• Switching frequency
• Inductor (L, core, gap, wire, winding turns)
• Capacitor (C, type, number)
• Heatsink
Minimum loss
Optimization (one or more objectives)
Lowest Cost
Lowest Weight

Fig. 2-13. A general review of design problem in power electronics in [89].


Linear Optimization
Simplex method
Duality theory
Interior point method

(a) Linear optimization algorithms.


Non-linear Optimization
Gradient-based algorithm
Penalty function-based algorithm
Heuristic algorithm
Linear complementary problem
Method of Feasible Direction
Augmented Lagangian penalty function
Genetic algorithm
Linear fractional programming
Optimization Techniques Applied in Power Electronics

(b) Non-linear optimization algorithms.

Fig. 2-14. Classification of optimization algorithms in two categories.

However, in the meantime, a lot of trade-off design problems under specific applications have adopted optimization methodologies to realize a localized optimum design. As shown in Fig. 2-14, the non-linear programming algorithms like the gradient-based algorithm, penalty function-based algorithms, and heuristic algorithm have already been applied in the component-level optimization design.

For example, the method of feasible direction (MFD) is applied in [94] for the device loss minimization in three-phase voltage source inverters. The basic idea of this method is, from a feasible point and by searching along the descent direction, to find a new feasible point to decrease the value of the objective function. The key factor for this algorithm is how to select the searching direction and move steps for design variables.

The cost of single-phase boost PFC was optimized under different switching frequencies and current ripples [95] with penalty function-based algorithms. The augmented Lagrangian penalty optimization algorithm was adopted for searching the optimal design, which is also suitable for discrete design variables in power electronics Besides, in order to reduce the iteration times, the calculation of objective function was all based on the developed analytical models.

Ozpineci [96] applied genetic algorithms (GA) optimization technique to obtain the switching angles for a cascaded multilevel inverter. The objective function is the minimum 5th and 7th harmonics, and design variables are three switching angles in the converter control. Compared with the gradient-based algorithm in [94], GA has fewer constraints on the objective function and design variable type. Also, except for the global optimal, GA provides many near-optimal designs as well, which enables users to consider other trade-offs when deciding a final scheme.

PSO is another popular non-linear algorithm in power electronics design [97]. PSO and GA algorithms are compared in the following:

Similarity:

1. PSO and GA both belong to the evolutionary methods, and they can be applied to search the global optimal. However, no theoretical proof to guarantee two algorithms can obtain the global optimal.
2. Both algorithms adopt a stochastic optimization method to update the population and to search for the optimal.
3. Both algorithms have the inherent parallel ability, starting the search from a population instead of an individual value. As a result, they can decrease the possibility to trap in a local optimal.

4. Both algorithms are not restricted by the limitation of the objective function, e.g., continuity and differentiability of an objective function.
5. For complex constrained optimization problems, they always have premature convergence issues and poor convergence ability.

Difference:

1. PSO algorithm keeps the previous best individual result and information while GA does not have the previous memory and previous information may be destroyed by the change of the population.
2. GA has a heavier computation burden than PSO due to the coding, cross and mutation procedure of the individual information.
3. GA has better convergence ability than PSO in the research of previous literature [98, 99].
4. PSO has a faster convergence speed than GA. GA shares the information among the different individuals with the cross procedure, so the whole population will move to the optimal zone averagely. Nonetheless, PSO did not share the individual information, and it only uses the current optimal in the population to update the search and population. As a result, in most cases, PSO achieves a faster convergence speed than GA.
5. PSO is mainly applied for continuous variable problems while GA can be applied for both continuous and discrete variables problems.

Besides, the multi-objective function is also applied in the system-level design of power electronics to select a reasonable design case considering the trade-off between the power density and the efficiency of converters [100]. The traditional multi-objective function applied in [100] is based on the weighted sum method given as

$$\text{Minimize} \qquad F(x) = \sum_{i=1}^{m} \omega_i f_i(x) \tag{2.22}$$

where ω_i is the weighting coefficients of different objectives and $f_i(x)$ are different objective functions. However, in this method, weighting coefficients are selected based on practical requirements and experience in multi-objectives.

Another way to do the multi-objective optimization problem is to converter other objectives to one key objective. In PV application, the life cycle cost (LCC) function is derived in paper [101], converting the converter efficiency to the life cost function. With this method, the selection of weighting coefficients can be avoided.

2.3.2 Local Optimization for a Specific Trade-off Design Problem

Generally, owing to the design complexity of power electronics circuits, design optimization always only focuses on one specific trade-off design problem in the whole converter system. Therefore, local optimizations are most common cases in power electronics design. Some optimization work [102], [12, 103, 104] can directly get the analytical expression of the objective function, and the extreme value is obtained by solving the derivative of analytical objective equations. However, for some optimization design, the analytical model is hard to derive, and simulations are required for the design, so optimization methodologies are adopted for searching the optimal design case. Paper [12, 61, 94, 96, 97, 102-117] are typical research examples to realize the local optimal design for a given trade-off design problem, being summarized in Fig. 2-15.

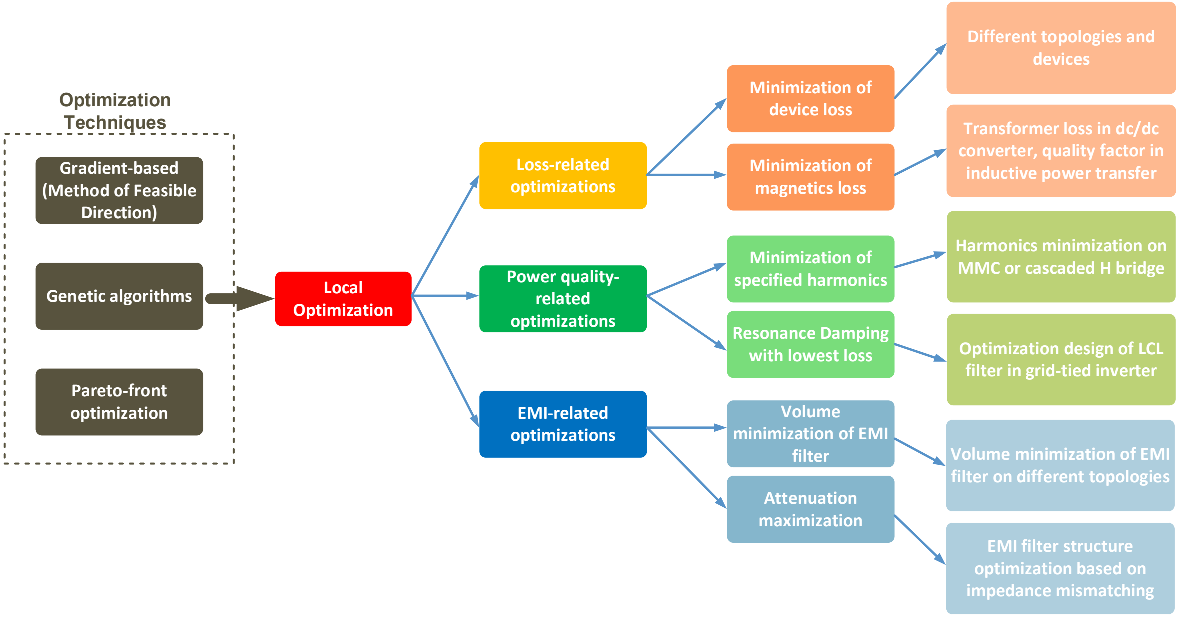

Optimization Techniques
Gradient-based (Method of Feasible Direction)
Genetic algorithms
Pareto-front optimization
Local Optimization
Loss-related optimizations
Power quality-related optimizations
EMI-related optimizations
Minimization of device loss
Minimization of magnetics loss
Minimization of specified harmonics
Resonance Damping with lowest loss
Volume minimization of EMI filter
Attenuation maximization
Different topologies and devices
Transformer loss in dc/dc converter, quality factor in inductive power transfer
Harmonics minimization on MMC or cascaded H bridge
Optimization design of LCL filter in grid-tied inverter
Volume minimization of EMI filter on different topologies
EMI filter structure optimization based on impedance mismatching

Fig. 2-15. Local optimization summary in power electronics design.

In paper [12, 94, 102-104, 107, 111, 112, 117], they all focus on the optimization of switching loss or conduction loss. For instance, Blaabjerg [94] proposed an analytical model based optimization design for total device losses. The objective is to realize minimum total device losses and design variables are gate resistance and gate voltage, affecting switching loss and conduction loss respectively. However, the gate resistance and gate voltage also influence the EMI noise because they can determine the switching speed for a given device. Hence, for the system-level design, this optimization may not obtain an optimum result in terms of the whole system efficiency or power density.

In paper [96, 108-110, 113, 115], power quality related local optimizations were conducted. One optimization example [96] shows a relationship between switching angles and harmonics in the design of multi-level converters. Moreover, a genetic algorithm optimization was applied to determine the switching angles which help to eliminate specified high order harmonics. Still, switching angles are optimized only based on THD while it may also affect other system-level performance (e.g., EMI noise spectrum).

In paper [61, 97, 105, 106, 114, 116], they concentrated on the optimizations of the converter interface like EMI. Boillat [61] tried to minimize EMI filter volume and proposed reasonable design constraints to confirm component values in EMI filters. The conclusion is that the remained free design variable is the inductance ratio between the CM inductance and DM inductance in one LC EMI filter, $k_L = L_{cm.1}/L_{dm.1}$, which has a significant influence on the filter volume. This is one example trying to decouple plenty of design variables and to locate the real design freedom, but it is still a localized optimization for EMI filter volume and it is also difficult to locate the real design freedoms in a system-level for the whole power stage design.

2.3.3 Global Optimization of Whole Power Stage Design

The global optimization of the whole power stage not only provides the optimal design point for an aimed objective function but also helps engineers have a comprehensive understanding of the relationships between design variables and the objective. There has been some literature discussing the global optimization design [11, 62, 95, 100, 101, 118-126]. They can be classified into two catalogs: distributed optimizers structure [11, 100, 101, 119-121, 124-126], which has paralleled optimizers for one system; centralized optimizer structure [62, 95, 118, 122, 123], which only has one optimizer for the whole system.

A distributed optimizer structure has more than one optimizer for one design problem. The key of this structure is how to separate the design problem into several relatively independent design problems and to search the optimal design for each individual optimizer. The system-level optimal design can be established by combining the local optimal design results and trade-offs among different optimizers.

Paper [11] developed an design tool for the power stage of the three-phase inverter system. Fig. 2-16 displays the general configuration of a motor drive system. To reduce the complexity of optimization design, paper separated design optimizers into three relatively independent subsystems: front-end diode rectifier, IGBT based inverter, and its thermal management system and EMI filter. Fig. 2-17 shows the three optimizers and their relationships. The benefit of this structure is that it can find the individual optimal design in each optimizer, and it could be further reused by other projects. Like the inverter stage and EMI optimizer, they all have universality and can be applied in most three-phase power electronics applications. Moreover, GA-based optimization techniques were used for fast searching for the optimal design. However, the interactions and trade-offs between those distributed optimizers also need to be recognized. Despite extra iterations for searching the system-level optimal design, it should be very careful to find out all the interactions and links among the different optimizers. Otherwise, it may be trapped in a local optimal design result with GA.

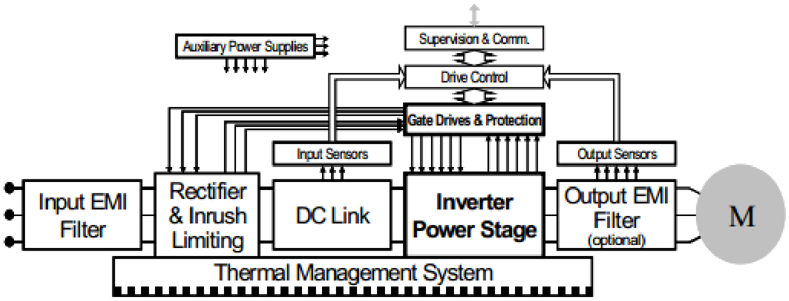

Auxiliary Power Supplies
Supervision & Comm.
Drive Control
Gate Drives & Protection
Input Sensors
Output Sensors
Input EMI Filter
Rectifier & Inrush Limiting
DC Link
Inverter Power Stage
Output EMI Filter (optional)
M
Thermal Management System

Fig. 2-16. The configuration of an industrial motor drive in [11].

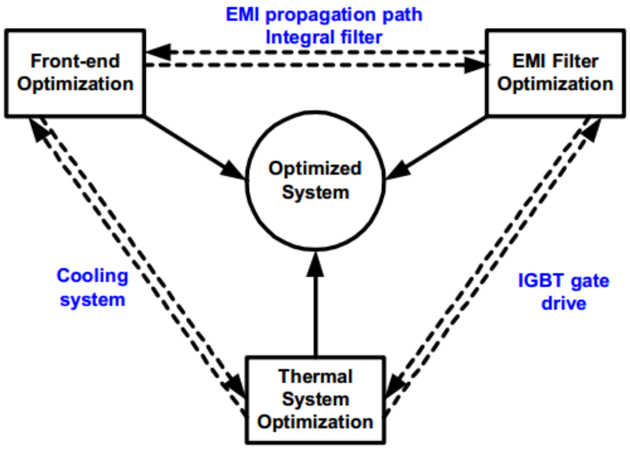

EMI propagation path
Integral filter
Front-end Optimization
EMI Filter Optimization
Optimized System
Cooling system
IGBT gate drive
Thermal System Optimization

Fig. 2-17. Approach for system optimization for a motor drive in [11].

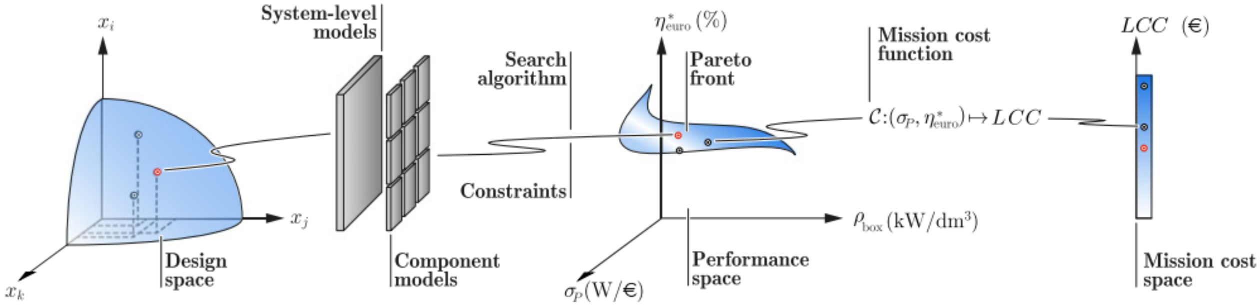

x_i
x_j
x_k
Design space
System-level models
Component models
Search algorithm
Constraints
η^*_{euro} (%)
Pareto front
ρ_{box} (kW/dm^3)
σ_P(W/€)
Performance space
Mission cost function
$\mathcal{C}:(\sigma_P, \eta^*_{\mathrm{euro}}) \mapsto LCC$
LCC (€)
Mission cost space

Fig. 2-18. General concept for multi-objective optimization with Pareto-front curve in [101].

To further improve system-level optimization with distributed optimizers, Pareto front was established in a two-stage structure [126], where an active front-end converter cascaded with a dc/dc converter. The concept of applications of Pareto front in power electronics design shown in Fig. 2-18 was first proposed in [90] in 2010, and further developments and improvements are in the literature [101, 119, 121, 124], [95, 118, 122, 123].

Fig. 2-19 shows the optimization scheme with distributed optimizer structure in system-level with Pareto fronts of subsystems [126]. According to paper [126], Pareto curves were plotted for three different design levels: the design of the dc-dc stage, the design of the active rectifier stage

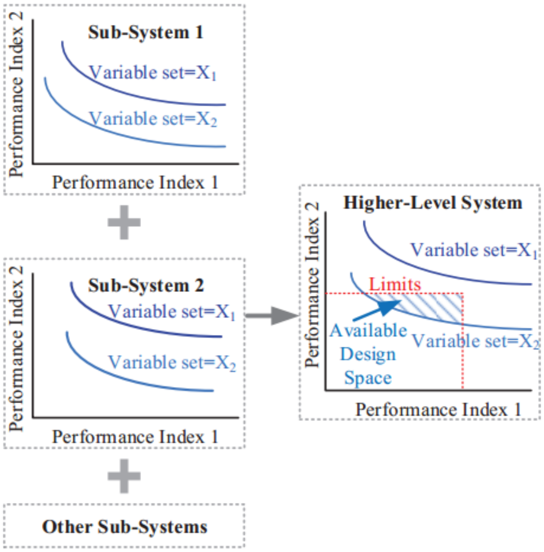

Sub-System 1
Variable set=X_1
Variable set=X_2
Performance Index 2
Performance Index 1
Sub-System 2
Variable set=X_1
Variable set=X_2
Performance Index 2
Performance Index 1
Other Sub-Systems
Higher-Level System
Variable set=X_1
Limits
Available Design Space
Variable set=X_2
Performance Index 2
Performance Index 1

Fig. 2-19. Higher-level system Pareto front could be identified by synthesizing sub-system Pareto fronts in [126].

and the design of the converter components. The system-level Pareto front can be obtained by summing up subsystem Pareto fronts.

A more detailed illustration of an optimization diagram is shown in Fig. 2-20 in [126]. The top-level optimization is a whole system-level optimization; medium-level optimization is a converter-level optimization and bottom-level optimization is a component-level optimization. To perform this concept, with pre-defined design variables from system-level optimization, each subsystem should be designed independently, calling for the well-defined design decomposition and links among different sub-systems. Moreover, the paper [126] does not apply any optimization algorithms for searching optimal design result compared with other schemes. It means the value of the objective function must be calculated for all combinations of design variables, introducing a heavy calculation burden. The general way to reduce iteration times in Pareto front is to have a design space for design variables. However, the essence of the design space is to reduce the combinations of design variables based on the human experience. In paper [126], the switching frequency is limited from 10 kHz to 150 kHz and dc bus voltage is limited from 340 V to 550 V because the authors thought that the optimal design would appear in this range of design variables.

Burkat [101] developed a better search algorithm for a Pareto front based design scheme. Compared with a mere brute-force search, it incorporated the additional heuristic searching method to reduce maximum design iterations by utilizing physical constraints and relationships of the applied models. The literature [101] gives two illustrations. First is in the cooling system, the thermal resistance will not further be reduced when the heatsink length has been increased to a certain value with the same fin geometry and fan because of the increased pressure drop. Hence, the heatsink with a longer length will not be explored if a certain length has arrived during optimization. The other example in magnetics design, when a core with a certain cross-section area exceeds B_{max} in the program, the core with the same material and smaller cross section will also be ignored safely.

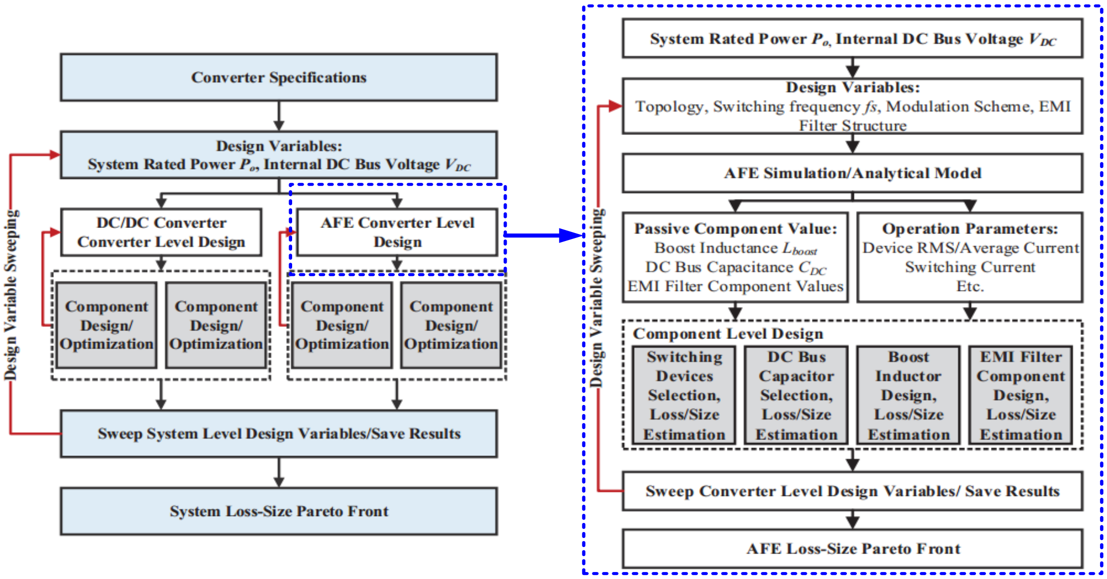

Converter Specifications
Design Variables:
System Rated Power P_o, Internal DC Bus Voltage V_{DC}
Design Variable Sweeping
DC/DC Converter Converter Level Design
AFE Converter Level Design
Component Design/ Optimization
Component Design/ Optimization
Component Design/ Optimization
Component Design/ Optimization
Sweep System Level Design Variables/Save Results
System Loss-Size Pareto Front
System Rated Power P_o, Internal DC Bus Voltage V_{DC}
Design Variables:
Topology, Switching frequency fs, Modulation Scheme, EMI Filter Structure
AFE Simulation/Analytical Model
Passive Component Value:
Boost Inductance L_{boost}
DC Bus Capacitance C_{DC}
EMI Filter Component Values
Operation Parameters:
Device RMS/Average Current
Switching Current
Etc.
Component Level Design
Switching Devices Selection, Loss/Size Estimation
DC Bus Capacitor Selection, Loss/Size Estimation
Boost Inductor Design, Loss/Size Estimation
EMI Filter Component Design, Loss/Size Estimation
Design Variable Sweeping
Sweep Converter Level Design Variables/ Save Results
AFE Loss-Size Pareto Front

Fig. 2-20. Three layers of optimization structure in [126] for EV charger application.

On the foundation of the above work, Mehrabadi [100] introduced a sensitive index in the distributed optimizer structure. This sensitive index is used to indicate the design quality in terms of converter robustness due to the tolerance of component values, which is also known as parametric uncertainty. Monte-Carlo (MC) analysis is adopted for evaluating system performance variation caused by parametric uncertainty. In addition, the Pareto front may obtain several similar optimal design results. With the help of the sensitive index, a better design result with the lower sensitive index can be selected from a reliability point.

Overall, the distributed optimizer scheme is a good candidate for system-level optimization. It reduces the complexity of optimization for the whole power stage and decouples the optimization problem into independent ones, which indirectly reduces the number of combinations of design variables and the number of design iterations. The issue for this structure is how to decompose one design problem into independent sub-systems and to recognize the links or design interfaces among different sub-systems, otherwise, only a local optimal design result would be obtained because of missing some relationships or trade-offs among different optimizers.

The centralized optimizer structure only has one optimizer in the design procedure. Compared with the distributed optimizer structure, the centralized optimizer does not decouple the design problem into relatively independent ones. It increases the number of combinations of design variables, which is more likely to find the global optimal design rather than the local optimal design.

Paper [62] proposed a system-level optimization procedure in a three-phase three-level T-type UPS system application. Even though the design includes two-stage converters, the optimizer directly chooses one subset of whole design variables for two stages and there is no interface or trade-off design variables between two stages design. In addition to the centralized optimizer, the Pareto front was adopted, and final design results are shown in performance space as displayed in

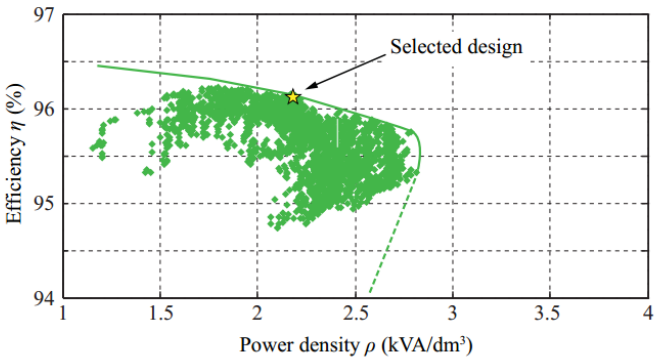


Fig. 2-21. Pareto curve of the η-ρ performance space and the selected design point in [62].

Fig. 2-21. The selected optimal design was chosen by a multi-objective function with two weighting coefficients for the power density and the efficiency of the whole converter system.

Paper [122] also adopted a centralized optimizer structure for minimizing the power density in the three-phase dc/ac converter design. However, in order to overcome the challenge (a great many combinations of design input variables) in the centralized structure, some design variables were assumed as fixed values based on the designer's experience where the modulation scheme was chosen for minimizing EMI noise and the current ripple of the boost converter was set for 20% of the peak inductor current. All those assumptions reduce the number of combinations and iterations, and it leads to a smaller design space, which may not enable to find the global optimal design.

Paper [95, 118, 123] implemented the centralized optimizer structure in some relatively simple applications successfully. In paper [95], the cost of single-phase boost PFC was optimized under different switching frequencies and current ripples. To reduce the iteration times, the calculation of objective function was all based on the developed analytical models. Besides, the augmented Lagrangian penalty algorithm was adopted for searching the optimal design, which is also suitable for discrete design variables in power electronics. Paper [95, 123] also applied a similar

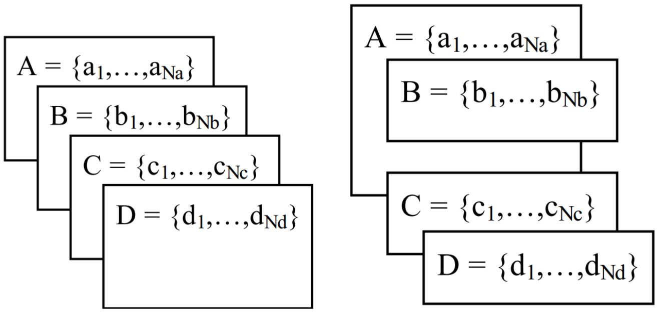


Fig. 2-22. Design variables arrangement comparison: centralized optimizer vs. distributed optimizers.

optimization scheme into the Flyback converter. The switching frequency and primary-side current ripple are two key input variables for the optimizer, and finally, the switching frequency and current ripple can be determined for the best performance under the pre-defined design conditions and constraints.

Overall, the centralized optimizer less depends on the human experience and is more likely to find the global optimal design. However, since there are a great many combinations for design variables, some experience-based assumptions are made to reduce the design space for optimization.

The core difference between the centralized optimizer and the distributed optimizer structures is the arrangement of design variables. For a large-scale system, there may be hundreds even thousands of design variables that require huge combinations of design variables and iteration times. Two optimizer structures introduce obvious differences in the numbers of iteration times. For example, if one system has 4 design variables shown in Fig. 2-22, what will be the difference in terms of iteration times? The left side structure in Fig. 2-22 shows the centralized optimizer, and the iteration likes a nested loop, having $N_a*N_b*N_c*N_d$ times of iterations. For the right side structure in Fig. 2-22, if B and C, D design variables are decoupled and A variable is assumed as the link between B and C, D variables, the iteration times can be only $N_a*(N_b+N_c*N_d)$, which will be dramatically reduced compared with the centralized optimizer. However, the distributed optimizer structure needs clearly define the design decomposition and links among optimizers, otherwise, it could take a huge risk to lose the global optimal design, and it relies more on human experience compared with the centralized optimizer structure.

2.4 Summary

This chapter reviews three areas that are closely related to the power electronics design.

First, power semiconductors related modeling is introduced and reviewed. Several switching behavior models based on the equivalent circuits were proposed in the literature to evaluate the switching performance, cross-talk phenomenon, and switching loss. To improve the accuracy of such behavior models, the non-linearity of parasitic capacitances, non-linear transfer parasitic characteristics and output characteristics are fitted by different kinds of mathematical functions. With the continuous improvement, the analytical waveforms predicted by the state-of-art switching behavior model can match the experimental waveforms better than the PSPICE model from the device manufacturer. However, the parasitic extractions and ac resistance estimation of the power loop are still the main barriers to apply the model. Moreover, different device loss models are surveyed. The analytical model with the switching waveform assumption and some parasitic capacitance parameters from the datasheet is the easiest way to estimate the switching loss, but the results may suffer a discrepancy with the measured loss data. Linear scaling of switching loss with the measured loss data is the most adopted approach to evaluate the switching loss, and DPT and calorimetric method can be used to characterize the switching loss. Nonetheless, the limitation of the linear scaling using the measured loss data is that the gate resistance selection, the junction temperature and non-linear parasitic capacitance induced loss are not considered. In the end, the lumped steady-state thermal resistance model, including device package, thermal resistance and heatsink, is reviewed for the cooling design. Compared with the TO-package, the PCB thermal resistance must be modeled and considered for the surface mount package of power devices.

Second, the modeling of passive components in power electronics is discussed, related to the magnetic core inductors, capacitor, heatsink and fan, and busbar and PCB layout.

For magnetics core inductors, the impedance model, loss model, and thermal model are respectively reviewed. The behavior model of the inductor impedance was established by fitting the frequency-dependent permeability, while the analytical per-turn model developed a set of self and mutual impedance formulas directly from Maxwell's equation for coils on ferromagnetic cores in 2-D dimension. One of the issues is the leakage inductance model for toroidal cores, and the current models cannot have a good prediction accuracy with the large turns-number since the assumption of magnetic field distribution is not correct in this case. The state-of-art core loss model IGSE or I^2GSE achieves relatively high accuracy for the arbitrary excitations with Steinmetz parameters. However, IGSE and I^2GSE still do not consider the impacts of dc bias on core loss, and also the Steinmetz parameters are only valid within a frequency range. Different levels of the thermal model of inductors are developed in the literature to exclude the bad design of inductors.

For capacitors, an equivalent circuits model is most commonly used for power electronics design. Disposition factor is an important parameter to determine the power loss and ESR in the model, and it is also a frequency-dependent variable whose characteristics are determined by the type of capacitors.

For heatsinks and fans, the thermal resistance of extruded heatsinks is well developed with the heat transfer theory. Also, to have a more accurate cooling design, the pressure drops of the heatsink and fan are modeled and applied to decide the operating condition of the fan and the real airflow speed provided by fans.

For busbars and PCB layouts, different techniques to achieve the low parasitic inductance are introduced, and the main principle is to realize the magnetic field cancellation. In addition, parasitic extraction methods are also summarized. However, all design considerations for geometry are at the implementation stage, and no link is established between the switching speed and the geometry design in the paper design stage, having the potential to cause the trial and error procedures in the converter testing.

Third, different optimization algorithms are summarized and classified as linear and non-linear programming. Since the power electronics designs are generally the strong non-linear problems, only can the non-linear programming be applied to solve the power electronics design problems, e.g., population-based optimization algorithms and gradient-based optimization algorithms. Besides, the state-of-art approaches for converter design are investigated. Currently, most design approaches only focus on one converter function like EMI filter, device loss or output harmonics. However, the impacts of design variables on the other converter functions or the whole converter are not carefully considered. Some recent works started to conduct global optimization of the whole power converter system, and the brute force searching and the genetic algorithm are applied to locate the optima of the design objective like the lowest weight or highest efficiency. Also, multi-objective optimizations with the Pareto curve are used to search the best trade-off design among several performance indexes. For highly complex converter system (multi-stage converter system), to avoid heavy searching efforts due to a large number of design variables, the design couplings can be identified to decouple the one design problem to two or more design problems, helping to much reduce the required iteration time for the brute-force searching.

Chapter Three

Filter Design Optimization Considering Non-linear Physics Characteristics

Filters in the 3-phase motor drive system may include the dc side EMI filter, ac side EMI filter or ac side *dv/dt* filter depending on the system specs and requirements. Since the strong non-linear physics characteristics of magnetic materials exist, the conventional inductor design always cannot accurately predict filter performance, and the conservative design margins and unscientific design criteria are applied to get an initial design results, leading to a trial-and-error procedure to adjust inductor design for good and reasonable design in the implementation stage. Especially for EMI filters, the main non-linear characteristics of magnetic materials are not incorporated in the conventional design, causing a performance discrepancy between the prediction results and testing results. Also, the corner frequency is always used as a performance index for EMI filter design. However, it is not guaranteed to obtain the optimal design result like the lowest weight with the highest corner frequency. The optimal design result is a trade-off between the inductance value and the volt-seconds of the designed inductor. Hence, a more scientific design approach with the optimization algorithm should be applied. In this chapter, the main non-linear characteristics of magnetic core materials are considered in the design, and the impacts of non-linear characteristics on filter design and noise prediction are carefully investigated and the leakage model of toroidal inductors is improved for the higher accuracy. Also, Particle Swarm Optimization (PSO) and *Ap* value-based weight prediction methods are used to search the lowest weight for the filter design.

3.1 Impacts of Current-bias Dependent Permeability on EMI filter Design

For medium to high power applications, due to the soft saturation and relatively higher saturation flux density, the powder and amorphous cores are commonly chosen for the DM inductors to achieve high power density in the EMI filter design. One of the issues of these materials is their permeability variation with operating current bias. Even for ac applications, the three-phase currents at different switching cycles during one line cycle vary greatly, which leads to a variable DM inductance at different time intervals during one line cycle. Since the three-phase system has the unequal instantaneous currents for three phases, current-bias dependent permeability will cause the unbalanced DM inductance/impedance which converts DM noise to CM noise, also called mixed-mode (MM) noise. In this paper, the characteristics of current-bias dependent permeability are investigated for several commonly adopted DM core materials. Moreover, a time-varying inductance model considering current-bias characteristics is developed and applied to evaluate its impacts on the CM noise and the CM filter design.

3.1.1 Investigation of Current-bias Dependent Permeability of DM Cores

Ferrite, powder core and amorphous are widely applied materials for DM inductors. Specifically, ferrite is more preferred for low power applications because of its lower power loss density at high frequency compared with the other two materials. However, since ferrite core needs a discrete gap structure to achieve a required inductance, it leads to a sharp saturation point and must be kept a safe distance away from the sudden roll-off. Also, the ferrite core is difficult to manufacture with a large core size for high power applications. Hence, the powder and amorphous cores with the distributed air gaps are more applicable in high power applications, especially for high inductor current cases. Fig. 3-1 from [127] illustrates the inductance curve with current-bias for ferrite and powder core (Kool Mu). From Fig. 3-1, powder core with distributed gap structure can withstand much higher maximum current-bias current or magnetic flux density compared to ferrite. However, the inductance of powder core and amorphous are more sensitive to the current

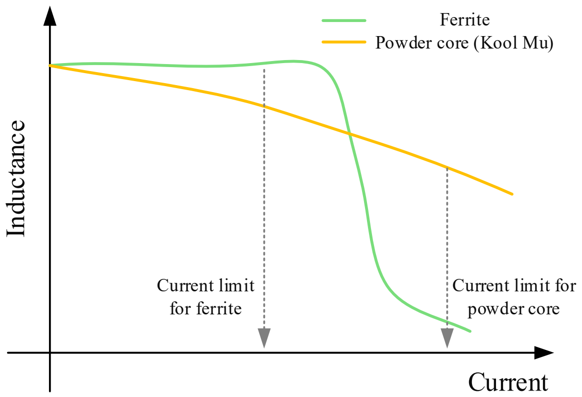


Fig. 3-1. Inductance curve with current-bias for ferrite and powder core [127].

bias and it varies by 20 % ~ 70 % to its initial inductance value based on different design principles. Therefore, this dissertation will mainly focus on DM inductors built with different kinds of powder cores from Magnetics and amorphous at medium to high power applications.

Fig. 3-2 shows the permeability percentage curve with dc bias for amorphous and powder cores. As it shows, the permeability of both amorphous and powder cores has an obvious trend to decrease when the magnetic field increases. Moreover, initial permeability has a significant influence on the permeability curve. The smaller initial permeability is, the wider the flat permeability range it achieves, e.g., for high flux powder core from Magnetics, the flat permeability range can be up to 30 A•T/cm with an initial permeability 26 u whereas the one with an initial permeability 125 u only is 9 A•T/cm. Also, different materials have different current-bias dependent permeability characteristics. With same initial permeability at 60 u, high flux powder core achieves similar current-bias performance with amorphous material 1 ($Fe_{82}Si_2B_{14}C_2$) [128], but KoolMu, MPP powder core material and amorphous material 2 ($Fe_{78}Si_9B_{13}$) [128] have a narrower flat permeability range and all curves shift to the left compared to high flux powder core material and amorphous material 1.

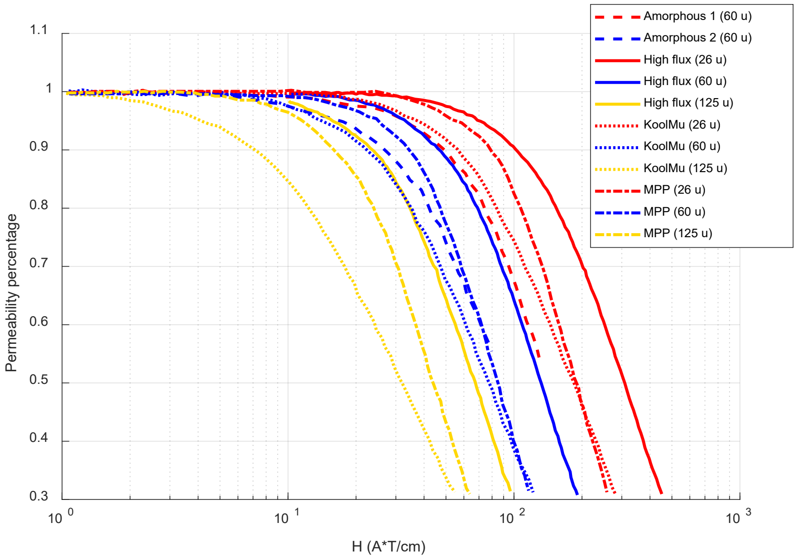


Fig. 3-2. Permeability percentage curves with current-bias for amorphous and powder core.

Table 3-1. Comparisons for different DM core materials

Material	**Alloy Composition**	**Core Loss**	**Dc Bias**	**Relative Cost**	**Saturation Flux Density (T)**	**Curie Temperature**	**60 u u flat to …**
Amorphous	Fe Si B	Low	Better	Medium	1.5	400 °C	2 MHz
High Flux	Fe Ni	Moderate	Best	Medium	1.5	500 °C	1 MHz
Kool Mu	Fe Si Al	Low	Good	Low	1.0	500 °C	900 kHz
MPP	Fe Ni Mo	Very low	Better	High	0.75	460 °C	2 MHz
XFlux	Fe Si	High	Best	Low	1.6	700 °C	500 kHz
Iron Powder	Fe	Highest	Good	Lowest	1.2-1.5	770 °C	500 kHz
Ferrite	Ceramic	Lowest	Poor	Lowest	0.45	100-250 °C	Variable

To summarize the current-bias and other characteristics of different DM core materials, Table 3-1 based on reference [129] is given for detailed comparisons.

With the above investigations, the current-bias dependent permeability of powder core and amorphous can contribute to a significantly unbalanced DM impedance in a three-phase converter system, which converts DM noise to non-intrinsic CM noise.

3.1.2 Variable Inductor Model with Considering Current-bias Dependent Permeability

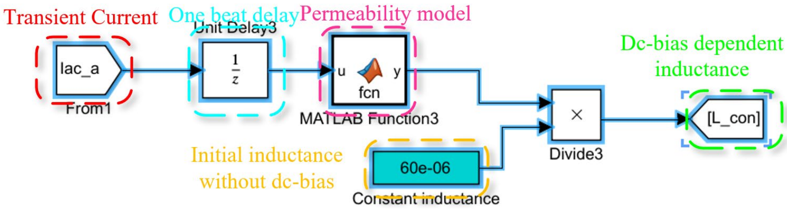
Magnetics gives a fitting model [130] of current-bias dependent permeability for different powder cores with corresponding coefficients. The fitting model can be applied to calculate the percentage of the initial permeability at one specific current bias condition.

$$\lambda = \frac{\mu_{real}}{\mu_{\text{intial}}} = \frac{1}{(a + bH^{c})} \quad \text{Units in A} \cdot T / cm \tag{3.1}$$

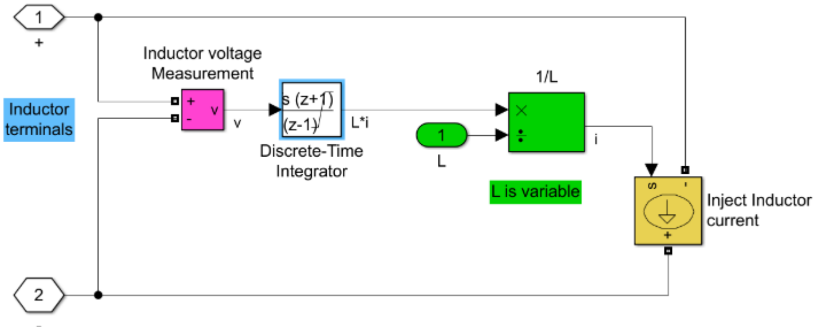
where λ is the percentage of the initial permeability, *a*, *b* and *c* are the fitting coefficients of one specific core material that are available in [130]. For amorphous core, this fitting model can be also applied, and fitting coefficients can be obtained by MATLAB curve fitting toolbox.

With the current-bias dependent permeability model, the inductor can be modeled as a current source. However, *v(t)*=L•*di/dt* in linear circuit system is not correct anymore for a non-linear inductance varying with current bias. The original form of Faraday's law must be adopted to model a time-varying inductance. The differential form of inductor voltage for a time-varying inductance is defined as

$$v(t) = \frac{d\phi_B}{dt} = \frac{d(L(t) \cdot i(t))}{dt} \tag{3.2}$$


Transient Current
One beat delay
Unit Delay3
Permeability model
Iac_a
From1
1
z
u
y
fcn
MATLAB Function3
Dc-bias dependent inductance
×
Divide3
[L_con]
Initial inductance without dc-bias
60e-06
Constant inductance

(a) Current-bias dependent inductance model.


1
+
2
-
Inductor terminals
Inductor voltage Measurement
v
v
s (z+1)
(z-1)
L*i
Discrete-Time Integrator
1/L
1
L
i
L is variable
Inject Inductor current

(b) Large signal model for time-varying inductance.

Fig. 3-3. Permeability percentage curve with current-bias for amorphous and powder core.

To implement the equation more conveniently in Simulink, Eq. (3.2) is rederived as an integral form, with current as of the output variable

$$i(t) = \frac{1}{L(t)} \int_{0}^{t} v(t)dt \tag{3.3}$$

Based on Eq. (3.3), the current-bias dependent inductance is modeled as a current source, whose output current is determined by the terminal voltage difference of inductor and time-varying inductance.

It needs two steps to implement the proposed model in Simulink. First, use an M function to calculate the permeability percentage under a specific current-bias condition, as shown in Fig. 3-3(a). A unit delay in *Z* domain is utilized to sample inductor current to calculate the instantaneous permeability with Eq. (3.1). Then the corresponding instantaneous inductance at a specific current is calculated.

Second, with the calculated inductance and the measured terminal voltage, the inductor current is derived with Eq. (3.3) by the integration of terminal voltage difference multiplying the instantaneous inductance value. The detailed function blocks are given in Fig. 3-3(b).

With the above model, DM inductors at three-phase are replaced with developed models with the chosen core material and fitting coefficients in Simulink.

3.1.3 Study of Induced Unbalanced DM Impedance and Mixed-mode Noise

A simulation of ANPC converter was built with developed DM inductor model in Simulink. Two simulations were conducted for comparing the effects of current-bias dependent permeability on unbalanced three-phase DM impedance and CM noise. One is with linear and constant inductance for DM inductance as a conventional design method, while the other one utilizes the current-bias dependent and time-varying inductance for DM inductance to achieve more accurate noise spectrum. The simulations were conducted for a 10 kW motor drive design, and the switching frequency is 100 kHz and the line frequency is 400 Hz. In addition to the leakage inductance of CM inductor, the required DM inductance is 200 μH based on the EMI design results. A high flux powder core from Magnetics is used based on physical design.

Fig. 3-4 shows the simulation results with the current-bias dependent permeability inductor model. As the duty cycle changes with time, three-phase currents also vary with time. Instantaneous inductances of three-phase DM inductor highly depend on the instantaneous phase currents. Also, as can be seen in Fig. 3-4, three-phase instantaneous DM inductances have unequal values that contribute to unbalanced DM impedance and convert DM noise to non-intrinsic CM noise. In this case, the DM inductance drops to around 55% at the phase current peak compared to the one at zero crossing point of phase current.

With time-varying DM inductance, the mechanism of DM current ripple is also changed. Fig. 3-5 gives the zoom-in phase current comparison between the constant and time-varying DM inductor models. From Fig. 3-5, near the zero-crossing point, the current ripples are quite close whereas the obvious difference is obtained at peak current point between the two models. Therefore, the time-varying inductance model with current-bias current does not only change CM noise but also alters DM noise significantly. Amplified DM noise with the time-varying inductance model further deteriorates CM noise. This is why, in a real application, DM inductance needs quite a large margin and overdesign if only using the constant DM inductance for design and simulations.

Fig. 3-6 further shows DM and CM noise spectrum comparisons between the two models. For DM noise, all the noise peaks at switching frequency harmonics of the non-linear model are higher than those of constant inductance model, since the inductance decreases with high current bias and the resulted lower inductance leads to a smaller DM impedance and higher DM current harmonics. For CM noise, owing to unbalanced DM impedance, some DM noise at switching frequency

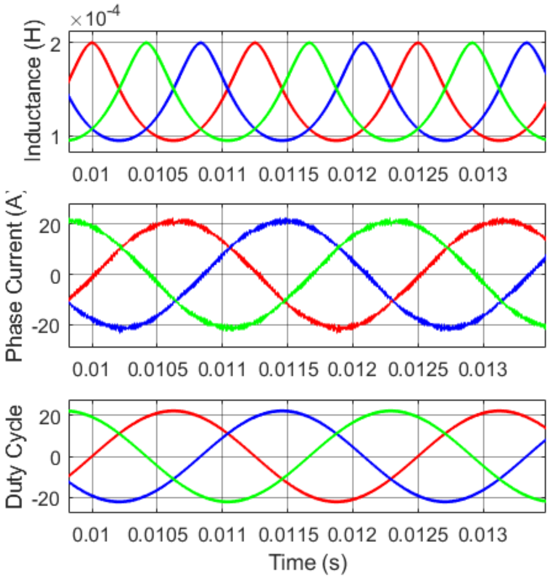


Fig. 3-4. Simulation waveforms for non-linear DM inductance.

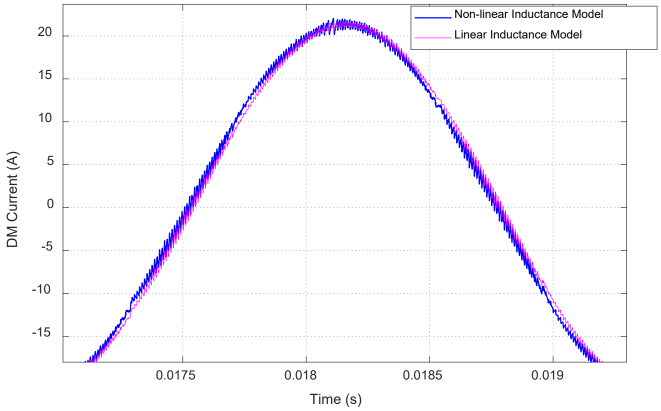
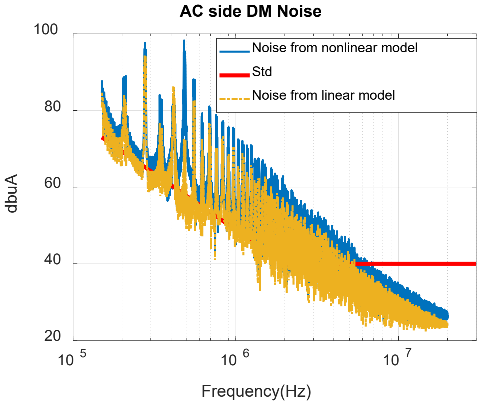
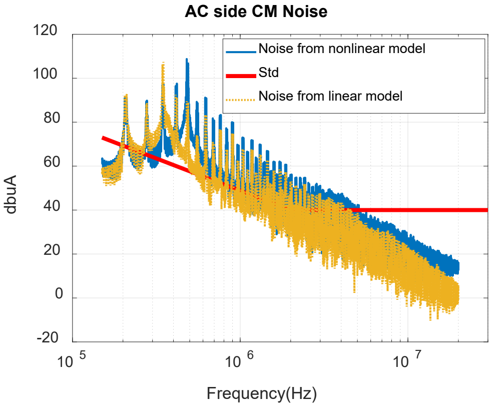


Fig. 3-5. DM currents comparison with or without non-linear DM inductor model.



(a). DM noise spectrum



(b). CM noise spectrum

Fig. 3-6. Noise spectrum comparisons from simulation results.

harmonics converts to CM noise, which makes CM noise peak of non-linear DM inductance model slightly higher than that with the constant inductance model. The more obvious difference is the CM noise spectrum of the non-linear model shifts to high frequency compared with the constant inductance model result.

Furthermore, for CM noise, although the low frequency range CM spectrum are very close due to the three-phase three-wire configuration, the medium to high frequency noise spectrums have obvious difference since the parasitic capacitance to the ground produces the low impedance branch for medium to high frequency displace currents.

Based on the above analysis, current-bias dependent permeability induced unbalanced DM impedances because of unequal three-phase instantaneous currents worsen both DM and CM noises.

3.1.4 Design Algorithm with Consideration of Current-bias Dependent Permeability

For the traditional design algorithm of EMI filters, generally for DM inductor design, it requires DM inductance cannot drop more than 40 % at peak current compared to the value at zero current [61]. However, the impacts of unbalanced DM impedance at switching transients on DM and CM noise are not considered. With the non-linear DM inductor model, the corner frequency of EMI filter for DM and CM noise would be changed due to the converted non-intrinsic CM noise and the varied DM noise.

The other issue of the traditional design algorithm is how to select inductance drop limitation, and 40 % may miss some possible solutions which have a lower weight, volume or cost. Furthermore, there is a design trade-off between the CM leakage inductance and DM inductance. CM leakage inductance can keep a stable inductance regardless of current bias, and DM inductance also plays as a part of CM inductance. Hence, a specific inductance drop limitation is replaced by an inductance ratio k (defined as DM inductance over CM inductance) in the proposed design algorithm. A larger CM leakage inductance is accompanied by the increase of CM inductance, which could reduce DM inductance. On the contrary, a larger DM inductance will help decrease the CM inductance.

The weight of EMI filters is chosen as the design objective. Fig. 3-7 shows the flow chart of the proposed design algorithm. Compared to the traditional EMI filter design, after finishing the physical design of DM inductors, the program will redo a simulation with non-linear DM inductors and the coefficients of the current-bias dependent permeability model based on the selected DM core material. With the updated noises, the corner frequency of DM and CM filter may be altered. Hence, the further step is to adjust DM capacitance and CM inductance/capacitance based on the new required corner frequency for noise attenuations if the EMI standard cannot be passed.

Moreover, in order to achieve semi-optimal design results, a design iteration is executed with different inductance ration k to brute-force search the lowest weight of EMI filter in whole design space. The range of inductance ratio here is assumed from 0-0.4, which is an experienced value based on the previous design results. Hence, with different initial CM inductance and inductance ratio k, the design algorithm can cover the most reasonable design space where the optimal design result may be located.

3.1.5 Experimental Verification

To validate the discovered phenomenon and the proposed model, a 10 kW ANPC converter with SiC MOSFETs was built for experiments. Fig. 3-8 shows the setup of the prototype for EMI noise measurement.

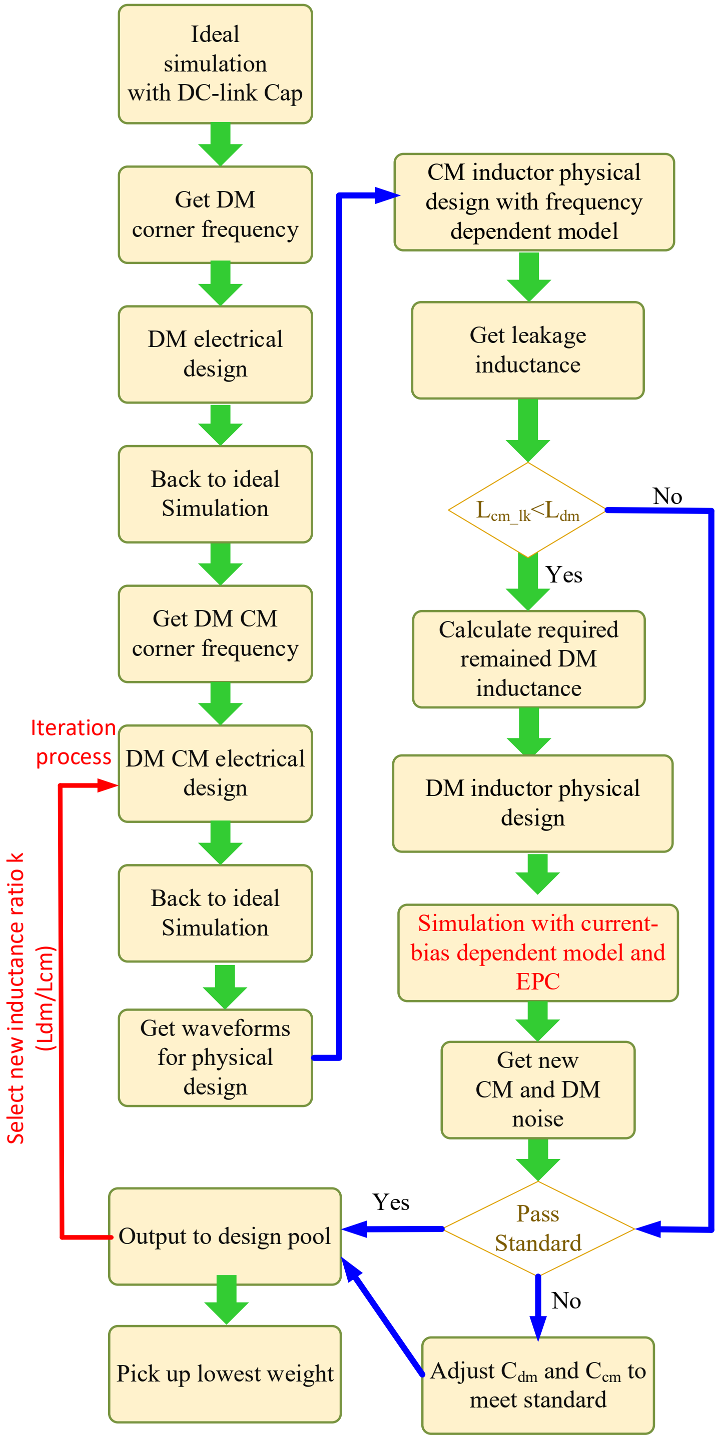

Ideal simulation with DC-link Cap
Get DM corner frequency
DM electrical design
Back to ideal Simulation
Get DM CM corner frequency
Iteration process
DM CM electrical design
Back to ideal Simulation
Get waveforms for physical design
Select new inductance ratio k (Ldm/Lcm)
CM inductor physical design with frequency dependent model
Get leakage inductance
$L_{cm\_lk}<L_{dm}$
No
Yes
Calculate required remained DM inductance
DM inductor physical design
Simulation with current-bias dependent model and EPC
Get new CM and DM noise
Pass Standard
Yes
No
Output to design pool
Pick up lowest weight
Adjust C_{dm} and C_{cm} to meet standard

Fig. 3-7. Flow chart of the design algorithm of EMI filter with consideration of current-bias dependent permeability.

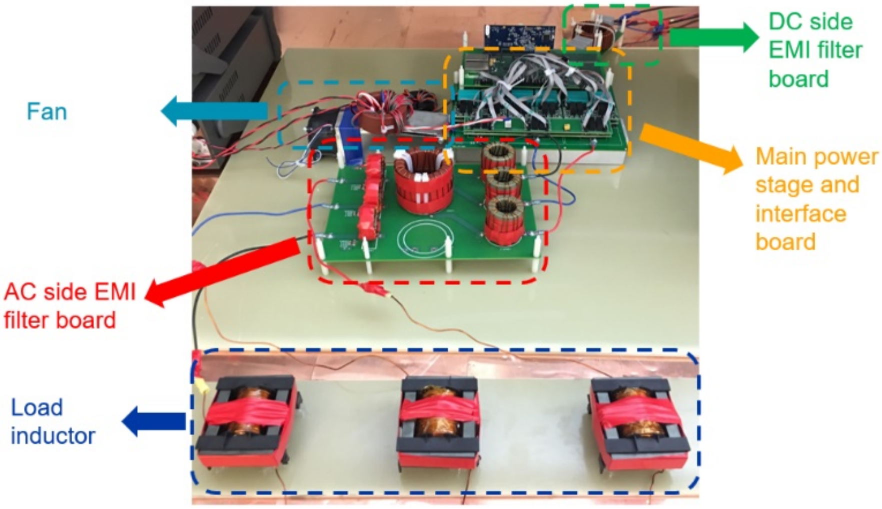

DC side EMI filter board
Fan
Main power stage and interface board
AC side EMI filter board
Load inductor

Fig. 3-8. The prototype of ANPC for EMI testing setup.

Table 3-2. Testing Condition and Specs of ANPC

Parameters	***Values***
Dc-link voltage, V_{dc}	400 V
Modulation index, M	1.1
Ac output peak current, I_{ac_pk}	20 A
Designed DM inductance, L_{DM}	220 µH
Switching frequency, f_{sw}	100 kHz

The testing condition and specs of the converter are given in Table 3-2.

A. Two DM Inductor Design

To verify the discovered phenomenon, two DM inductors are designed for comparison. Fig. 9 shows the construction of two inductors, and both inductors were built with KoolMu material. The difference is that the left-side inductor (labeled as inductor 1) is designed with following the general rule that the inductance drop is around 42% at ac peak current while the right-side inductor

Table 3-3. Specs of Two DM Inductors

Parameters	***Values (Inductor 1)***	***Values (Inductor 2)***
Company	Magnetics	Micro Metals
Part Number	0077439A7	FS-300060-2
A_L (nH/T^2)	135	68
Turns Number	35	56
Indutance drop at peak current	42% @ 20 A	12% @ 20 A

(labeled as inductor 2) is overdesigned as an almost ideal inductance that the inductance drop is only 12% at ac peak current. The detailed specs of two inductors are given in Table 3-3.

As Fig. 3-9 shows, the full utilization of saturation flux density of powder cores can help shrink the size and weight of inductors. However, high operating flux density design may cause unbalanced DM impedance and non-intrinsic CM noise.

B. Testing Results Analysis and Comparisons

To characterize the EMI noise with two different DM inductor designs, only DM inductors are applied in the EMI filter and the other parts of the EMI filter are removed for better illustration.

Fig. 3-10 shows the experimental waveforms and CM noise measuring results for an ANPC converter with two different DM inductor designs. Comparing Fig. 3-10(a) and Fig. 3-10(b), two differences can be observed. The first one is the current ripple at peak current: the phase current with inductor 1 design has a higher current ripple than the one with inductor 2 design since the DM inductance drops significantly at peak current for inductor 1 design. The second difference is the amplitude of the CM noise at the time domain. The CM noise with inductor 1 design has a higher peak amplitude than the one with the inductor 2 design. It demonstrates that the unbalanced DM inductance at transients can convert DM noise into the non-intrinsic CM noise.

Fig. 3-10(b) and Fig. 3-10(d) give the CM noise measuring results for two inductor design examples. A 10-dB attenuator is used to protect the spectrum analyzer. The noise peak and spectrum are also different, and detailed comparisons are replotted in Fig. 3-11. From Fig. 3-11(a), the DM noise peaks with 42% inductance variation are 2.7 dBuA and 5.1 dBuA higher than that with 12% inductance variation at 200 kHz and 300 kHz respectively. These higher DM noise peaks require a lower DM corner frequency of DM filters. Also, from Fig. 3-11(b), the CM noise peak with 42% inductance variation is 6.1 dBuA higher than the one with 12% inductance variation at 200 kHz. This higher CM noise peak also demands a lower CM corner frequency of CM filters.

A filter corner frequency design is conducted by using two measuring spectrums with different inductor designs. DO-160E standard is applied to determine the corner frequency and the design results are shown in Fig. 3-12. In this case, for inductor design 1, the corner frequency of the CM filter is 75.6 kHz, where the corner frequency of the CM filter is 54.1 kHz for inductor design 2. It demonstrates the current-bias dependent permeability of powder cores has an obvious impact on the CM filter design, which may need to further increase CM inductance value with a decreased corner frequency of CM filter.

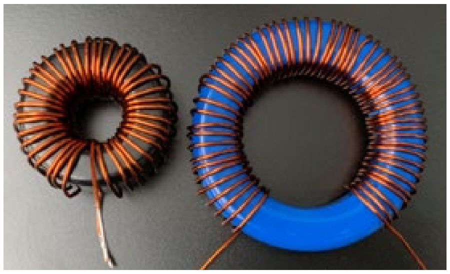
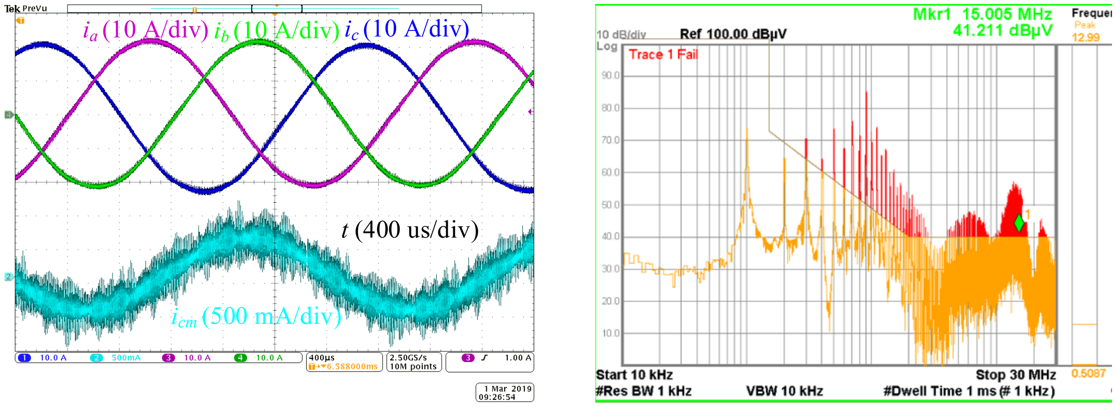
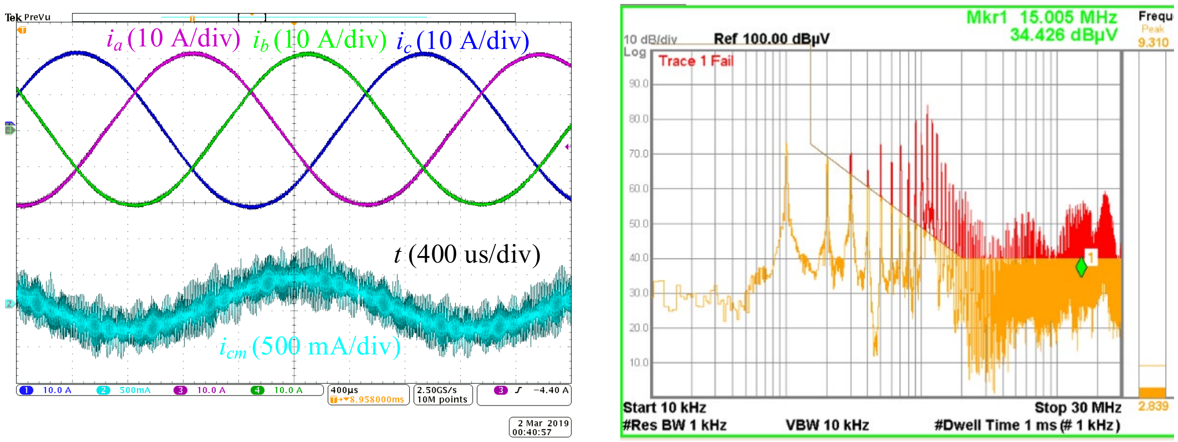


Fig. 3-9. The prototype of two DM inductors

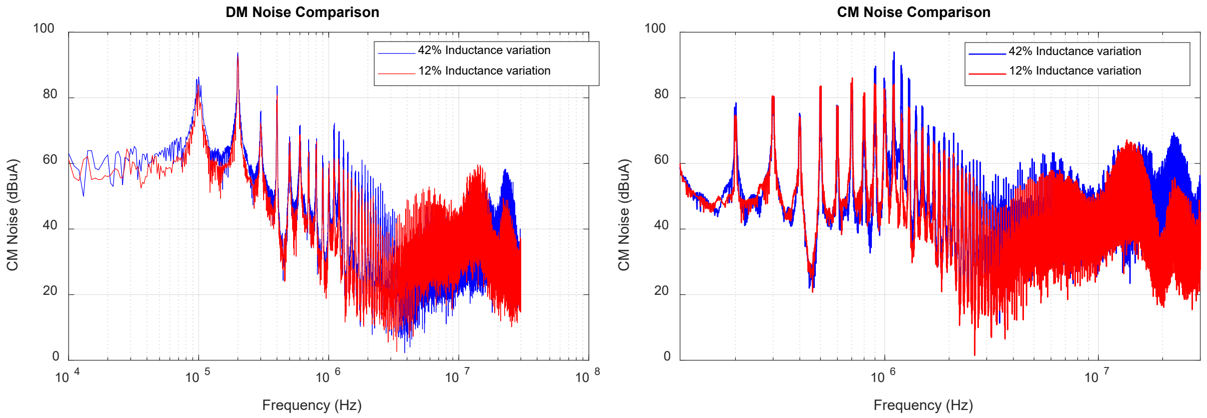


(a) The critical testing waveform in time domain with inductor 1 (b) CM bare noise with inductor 1



(c) The critical testing waveform in time domain with inductor 2 (d) CM bare noise with inductor 2

Fig. 3-10. Experimental waveforms and noise measurement for two inductors.



(a) DM noise comparison (b) CM noise comparison

Fig. 3-11. EMI bare noise comparisons only with DM inductors.

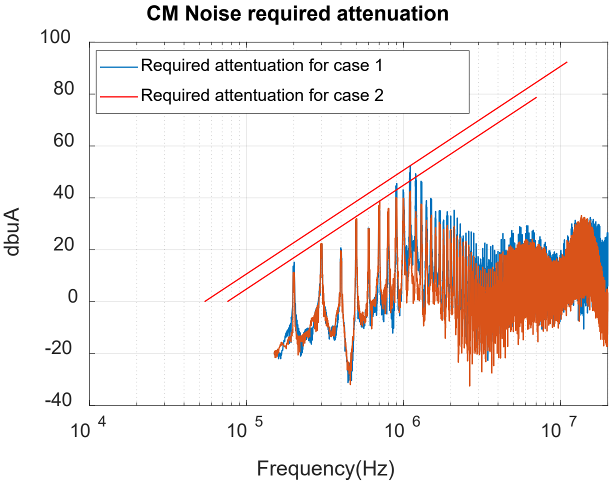


Fig. 3-12. Corner frequency design of CM filter.

3.2 Impedance-based CM Inductor Design Approach Considering Frequency-dependent and Imaginary Permeability

Due to the high saturation flux density and the high initial permeability, toroidal nanocrystalline cores are widely applied in the common-mode (CM) inductor design for high power applications. Compared with the flat permeability curve of ferrite cores up to several MHz, the permeability of nanocrystalline cores with a high initial value drops at only around 10 kHz. Furthermore, the imaginary permeability of nanocrystalline can provide a considerable impedance to achieve the noise attenuation compared with ferrite, being neglected in the inductance-oriented design approach. To achieve a more accurate design result, this dissertation proposes an impedance-based design approach with considering both frequency-dependent and imaginary permeability of nanocrystalline cores. The required impedance of a CM inductor is derived by the equivalent circuits at a specific frequency. Then, with the frequency-dependent permeability model, the turns number can be calculated by providing enough impedance using both the inductance produced by the real permeability and the resistance produced by the imaginary permeability. After sweeping the frequencies from 150 kHz to 2 MHz in the EMI range, the final turns number will be determined.

3.2.1 Characteristics of Frequency-dependent Permeability for CM Cores

Frequency-dependent and imaginary permeability are the nonlinear characteristics of magnetic cores, not paid much attention to by power electronics engineers, especially for nanocrystalline material [131]. Generally, nanocrystalline cores have a much higher initial permeability than ferrite cores, favoring the reduction of turns number. However, unlike the flat curve of the ferrite's permeability as shown in Fig. 3-13, the permeability of nanocrystalline quickly drops from around 20~30 kHz. Also, from Fig. 3-13, for ferrite cores, the real permeability dominates the magnitude of whole permeability below 1 MHz, while the real permeability only dominates the magnitude of whole permeability below 40 kHz for nanocrystalline cores. Hence, for nanocrystalline cores in EMI frequency range, starting from 150 kHz, not only the inductance produced by the real permeability but also the resistance produced by the imaginary permeability provides comparative impedances for the noise attenuation.

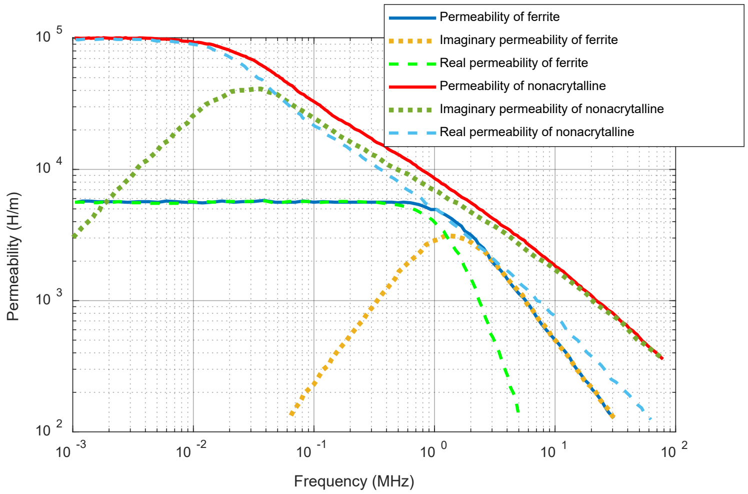


Fig. 3-13. Permeability curve for ferrite and nanocrystalline cores.

For the traditional inductor design of output filters for power electronics applications, the performance at the switching frequency is a major consideration [132, 133], and the permeability at the switching frequency is estimated by the linear interpolation. However, for EMI filters, the performance of filter components in the whole EMI testing frequency range is important. Frequency-dependent permeability can vary the inductance much at different frequencies, and CM inductance may not provide enough attenuation at high frequency due to the decreased permeability [39, 40]. Also, the equivalent resistance provided by core losses can be regarded as the part of impedance created by the imaginary permeability [39], which helps increase the impedance at high frequency. Papers [39, 40] use behavioral voltage sources to model the frequency-dependent resistive and inductive impedance of inductors, achieving an accurate spice model for simulations. However, they did not propose a practical design approach for the EMI filter design. Shen [41] proposes a comprehensive design approach of CM chokes at high frequency with considering all non-linear characteristics of cores and windings. Nonetheless, the resistance modeling of the imaginary part is based on Steinmetz formula, requiring different coefficients at different frequency ranges. Moreover, no detailed derivation of the required impedance of CM inductors is given for implementations.

3.2.2 Modeling of Frequency-Dependent Permeability and Derivation of Required Impedance of CM Inductor

According to the above analysis, for the traditional design approach, only considering the inductance and real permeability is not accurate enough to predict noise attenuation for CM inductor design. To improve the design approach, the first step should model the real and imaginary permeability of nanocrystalline cores. Nomura's model [131] is used in this paper through a curve fitting method to obtain the analytical permeability model of nanocrystalline material VITROPERM 500F [134] from VAC, and the detailed model is given in Eq. (3.4) for real permeability and Eq. (3.5) for imaginary permeability. Fig. 3-14 shows the curve fitting results, and the applied model achieves high accuracy both for real and imaginary permeability:

$$\mu_{re}(f) = \frac{10^{-0.8141\times\log_{10}(f)+8.513}}{1+10^{-1.0167\times\log_{10}(f)+4.111}} \tag{3.4}$$

$$\mu_{im}(f) = \frac{10^{-0.6242\times\log_{10}(f)+7.558}}{1+10^{-1.7782\times\log_{10}(f)+7.6515}} \tag{3.5}$$

To illustrate how to derive the required impedance of CM inductors with the permeability model, an ac-side CM inductor design for motor drive application complying with DO-160E standard is used as an example. Since DO-160E uses the current for the noise measurement, an insertion loss to satisfy the required attenuation is derived based on the CM equivalent circuits.

As shown in Fig. 3-15(a), it is the equivalent circuit for common-mode noises without the CM filter. The ac-side CM bare noise without the CM filter is derived as

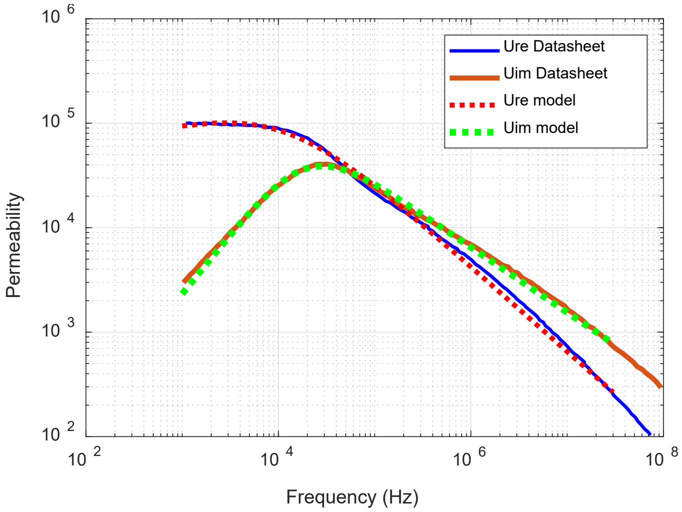


Fig. 3-14. Curve fitting results of the real and imaginary permeability of nanocrystalline material VITROPERM 500F.

$$\begin{cases} I_{cm\_bare} = \dfrac{v_{cm\_ac\_eq1}}{Z_{cm\_ac1}} \\ v_{cm\_ac\_eq1} = \dfrac{v_{cm}(Z_{Csc} \parallel Z_{cm\_ac1})}{Z_{cm\_dc} + (Z_{Csc} \parallel Z_{cm\_ac1})} \\ Z_{cm\_ac1} = Z_{Ldm\_ac} + \dfrac{Z_{motor} + Z_{cable}}{3} \end{cases} \tag{3.6}$$

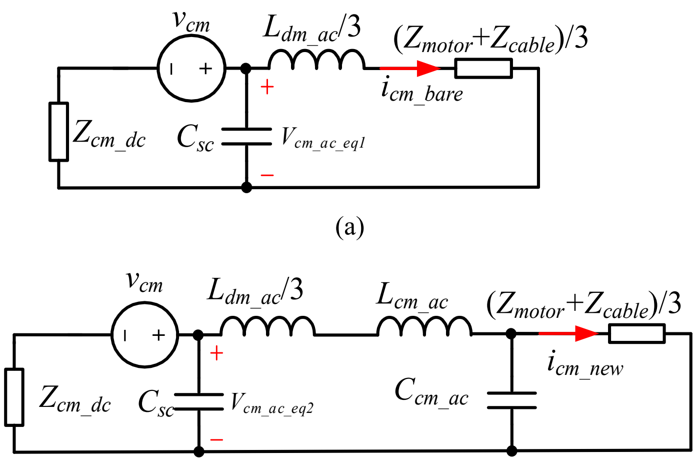
where v_{cm} is the CM voltage of a three-phase converter, $v_{cm\_ac\_eq1}$ is the equivalent CM voltage applied in ac-side without the CM filter, Z_{cm_ac1} is the ac-side CM impedance without the CM filter and Z_{cm_dc} is the dc-side CM impedance, and Z_{Csc} is the impedance of parasitic capacitance at ac-side.

With the insertion of the CM filter, shown in Fig. 3-15(b), the ac-side CM noise can be rederived as

$$\begin{cases} I_{cm\_new} = \dfrac{v_{cm\_ac\_eq2} Z_{Ccm\_ac}}{Z_{cm\_ac2}(Z_{Ccm\_ac} + Z_{load})} \\ v_{cm\_ac\_eq2} = \dfrac{v_{cm}(Z_{Csc} \parallel Z_{cm\_ac2})}{Z_{cm\_dc} + (Z_{Csc} \parallel Z_{cm\_ac2})} \\ Z_{cm\_ac2} = Z_{Ldm\_ac} + Z_{Lcm\_ac} + Z_{load} \parallel Z_{Ccm\_ac} \\ Z_{load} = \dfrac{Z_{motor} + Z_{cable}}{3} \end{cases} \tag{3.7}$$

where $v_{cm\_ac\_eq2}$ is the equivalent CM voltage applied in ac-side with the CM filter, Z_{cm_ac2} is the ac-side CM impedance with the CM filter and Z_{cm_dc} is the dc-side CM impedance, and Z_{load} is the impedance of the ac-side load.

To meet the EMI standard of DO-160E, the insertion loss, defined as i_{cm_bare} over i_{cm_new}, should be larger than the required attenuation Att_{req} calculated based on the noise magnitude difference between the bare noise and EMI standard. The above relationship is derived in Eq. (3.8),


v_{cm}
$L_{dm\_ac}/3$
$(Z_{motor}+Z_{cable})/3$
i_{cm_bare}
Z_{cm_dc}
C_{sc}
$V_{cm\_ac\_eq1}$
+
−
v_{cm}
$L_{dm\_ac}/3$
L_{cm_ac}
$(Z_{motor}+Z_{cable})/3$
i_{cm_new}
Z_{cm_dc}
C_{sc}
$V_{cm\_ac\_eq2}$
C_{cm_ac}
+
−

(a)

(b)

Fig. 3-15. Equivalent common-mode circuits of a three-phase converter (a) without CM filter, (b) the CM filter.

and it can be used to judge whether the CM inductor's impedance is large enough to provide the required attenuation at a specific frequency.

$$\begin{aligned}
& Att_{req} \le IL = 20\log\left|\frac{i_{cm\_bare}}{i_{cm\_new}}\right| \\
& \Rightarrow \left|Z_{cm\_ac2}\right| \ge \frac{10^{\frac{Att_{req}}{20}} v_{cm\_ac\_eq2}}{v_{cm\_ac\_eq1}} \cdot \frac{Z_{cm\_ac1} Z_{Ccm\_ac}}{(Z_{Ccm\_ac} + Z_{load})} \\
& \Rightarrow \left|Z_{Ldm\_ac} + Z_{Lcm\_ac} + \frac{Z_{load} Z_{Ccm\_ac}}{Z_{load} + Z_{Ccm\_ac}}\right| \\
& \quad \ge \frac{10^{\frac{Att_{req}}{20}} v_{cm\_ac\_eq2}}{v_{cm\_ac\_eq1}} \cdot \frac{Z_{cm\_ac1} Z_{Ccm\_ac}}{(Z_{Ccm\_ac} + Z_{load})}
\end{aligned} \tag{3.8}$$

The left issue is how to calculate the impedance of CM inductors at a specific frequency. For toroidal nanocrystalline cores, the datasheet usually provides A_L (H/N^2, inductance per square of turns number) at 100 kHz to calculate inductance. Hence, A_L is used to calculate the impedance of CM inductor at an arbitrary frequency, given in Eq. (3.9).

$$\begin{cases} Z_{Lcm\_ac}(f) = \omega_f A_{L\_100k} \dfrac{\mu_{im}(f)}{\mu_{re}(100k)} N^2 + j\omega_f A_{L\_100k} \dfrac{\mu_{re}(f)}{\mu_{re}(100k)} N^2 \\ \left| Z_{Lcm\_ac}(f) \right| = \omega_f A_{L\_100k} \dfrac{\sqrt{\mu_{re}(f)^2 + \mu_{im}(f)^2}}{\mu_{re}(100k)} N^2 \end{cases} \tag{3.9}$$

where ω_f is the angular frequency, and N is the turns number. With the corrected impedance of the CM inductor, the turns number can be determined by increasing to let Eq. (3.8) satisfied.

3.2.3 Impedance-based CM Inductor Design Approach

A. Electrical Design Approach

For the conventional CM inductor design approach, once the corner frequency is determined by only considering the first or second noise peak, the required CM inductance is calculated. However, the CM inductance designed with A_L value at low frequency may not afford enough impedance in the high frequency range because of the decreased permeability with the increase of frequency. As shown in Fig. 3-16, the CM inductance is calculated based on the first noise peak, and if assumed as an ideal inductor with the green impedance curve, the impedance of the CM inductor is larger than the required impedances in the whole EMI frequency range. Nonetheless, considering the frequency-dependent permeability, the real impedance curve of CM inductor is lower than the required impedances at several frequencies shown as the blue curve in Fig. 3-16. This example illustrates how important it is to consider the frequency-dependent permeability of the nanocrystalline core. Also, the imaginary permeability produced resistance can increase the impedance of CM inductors.

To achieve more accurate design results, an improved impedance-based design approach considering the frequency-dependent permeability and the imaginary permeability is proposed.

Fig. 3-17 shows the flowchart of the proposed electrical design approach to determine the turns number.

Based on the analysis in Section 3.1, the medium to high frequency EMI noise spectrum also highly depends on the permeability characteristics of DM cores. Since the three-phase system has the unequal instantaneous currents for three phases, the current-bias dependent permeability will cause the unbalanced DM inductance/impedance, converting DM noise to CM noise. To achieve a more accurate noise prediction result, a time-varying DM inductor is modeled in the simulation. The EMI spectrums from the simulation result are quite different when using the ideal linear inductor model and the time-varying inductor model, shown in Fig. 3-6.

After getting CM bare noise from the simulation with the time-varying DM inductor model, the design program will calculate the impedance of CM inductor with the selected nanocrystalline core and turns number N at the starting frequency of the EMI range. Then, the calculated impedance of the CM inductor is substituted into Eq. (3.8) to judge whether the impedance is large enough to provide the required attenuation. If not, the turns number will be continuously increased

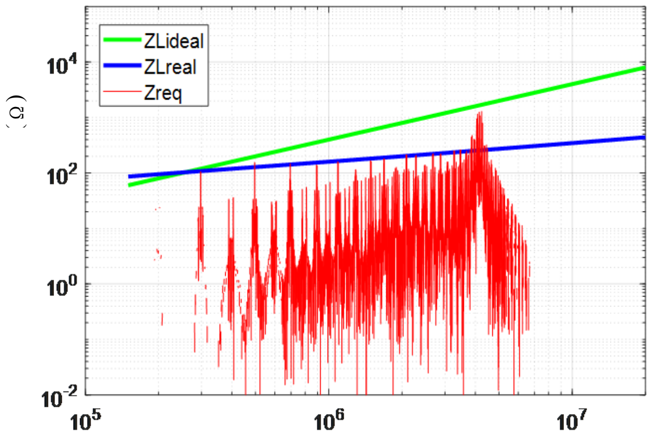


Fig. 3-16. Real impedance curve of the traditional design approach.

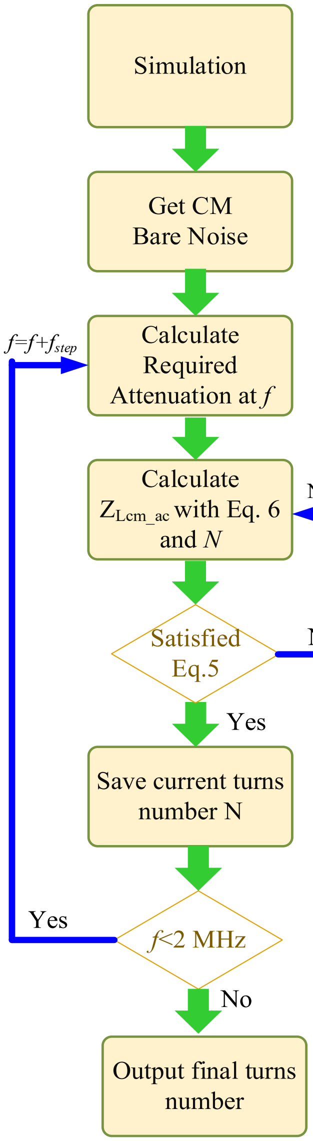

Simulation
Get CM Bare Noise
Calculate Required Attenuation at f
f=f+f_step
Calculate Z_Lcm_ac with Eq. 6 and N
N=N+1
Satisfied Eq.5
No
Yes
Save current turns number N
Yes
f<2 MHz
No
Output final turns number

Fig. 3-17. Design procedure to calculate the required turns number.

until the calculated impedance satisfies Eq. (3.8). With the same procedure, the impedance of the CM inductor is validated from 150 kHz to 2 MHz since the prediction of EMI noise for higher frequency range, dominated by coupling effects and parasitics, is not accurate. The final turns number will be finally obtained with the design iteration shown in Fig. 3-17.

B. Physical Design Iterations

The information of nanocrystalline cores from Vacuumschmeize is collected to build the database for the physical design of CM inductors. Fig. 3-18 gives the physical design iterations of CM inductors, and a suitable core will be selected based on the required turns number, windows area, saturation, and temperature rise.

The accuracy of the leakage inductance estimation is critical for the physical design of CM inductors. First, the maximum magnetic flux density calculation for CM inductors needs to include both DM and CM flux density, and DM flux density depends on the leakage inductance. Since the conventional maximum magnetic flux density model may not be accurate, a new estimation method considering frequency-dependent permeability is proposed in Section 3.3 and applied here.

Second, the DM flux induced core loss estimation in CM cores also highly depends on the accurate leakage inductance calculation. To achieve relatively high accuracy of the core loss estimation and the maximum flux density calculation, the improved leakage model, by the analogy between reluctances and capacitances, can be applied, which is presented in Section 3.3.

GSE is applied for the core loss. Since the magnetic flux is not uniformly distributed inside the magnetic core, the winding covered core volume has both DM and CM fluxes, while no winding covered core volume only has the CM flux. The core loss can be calculated as follows:

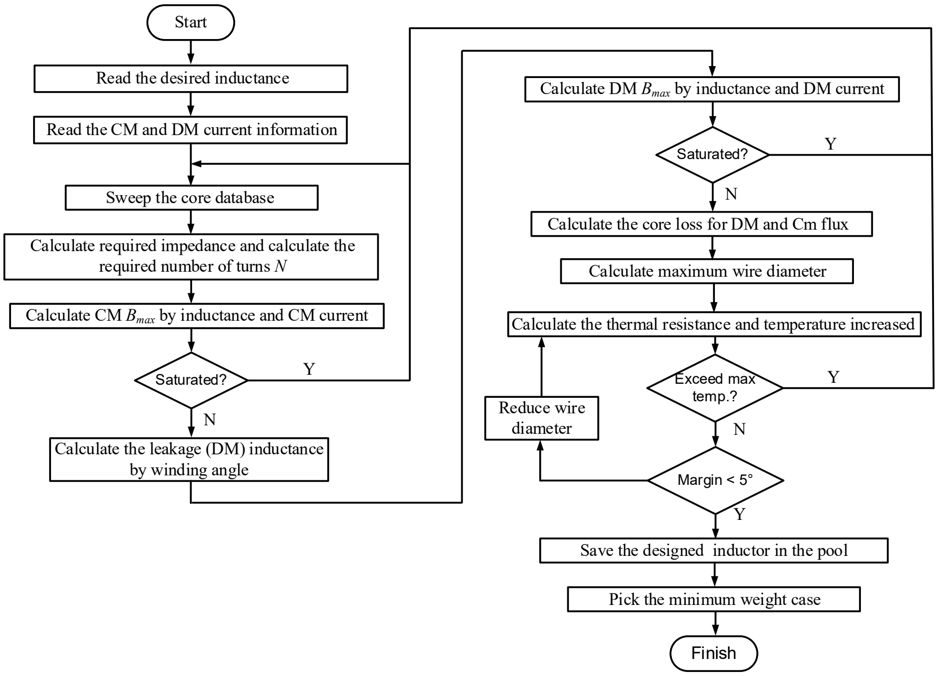

Start
Read the desired inductance
Read the CM and DM current information
Sweep the core database
Calculate required impedance and calculate the required number of turns N
Calculate CM Bmax by inductance and CM current
Saturated?
Y
N
Calculate the leakage (DM) inductance by winding angle
Calculate DM Bmax by inductance and DM current
Saturated?
Y
N
Calculate the core loss for DM and Cm flux
Calculate maximum wire diameter
Calculate the thermal resistance and temperature increased
Exceed max temp.?
Y
N
Reduce wire diameter
Margin < 5°
Y
Save the designed inductor in the pool
Pick the minimum weight case
Finish

Fig. 3-18. Physical design procedure and iteration for CM inductors.

$$\begin{cases} P_{wc} = \dfrac{1}{T}\displaystyle\int_0^T k_1 \left|\dfrac{dB_{DM}}{dt} + \dfrac{dB_{CM}}{dt}\right|^{\alpha} \left|B_{DM}(t) + B_{CM}(t)\right|^{\beta-\alpha} dt \cdot V_{core} \cdot \dfrac{3\theta_w}{2\pi} \\ P_{wuc} = \dfrac{1}{T}\displaystyle\int_0^T k_1 \left|\dfrac{dB_{CM}}{dt}\right|^{\alpha} \left|B_{CM}(t)\right|^{\beta-\alpha} dt \cdot V_{core} \cdot (1 - \dfrac{3\theta_w}{2\pi}) \\ k_1 = \dfrac{k}{(2\pi)^{\alpha-1}\displaystyle\int_0^{2\pi} |\cos\theta|^{\alpha} |\sin\theta|^{\beta} d\theta} \end{cases} \tag{3.10}$$

where P_{wc} and P_{wuc} are the core losses for the winding covered core volume and the winding uncovered core volume, V_{core} is the volume of the magnetic core, θ_w is the core angle covered by the one-phase winding, k, α and β are the Steinmetz parameters.

The total core loss of CM inductor can be calculated by summing up P_{wc} and P_{wuc}.

The thermal model varied with different cooling methods. In this design, two cooling methods are assumed, and they are passive cooling and air forced convection cooling. For passive cooling,

Table 3-4. Specs of ANPC for EMI filter design

Parameters	***Values***
Dc-link voltage, V_{dc}	400 V
Modulation index, M	0.9
Ac output peak current, I_{ac_pk}	24 A
Modulation Method	DPWM
Switching frequency, f_{sw}	100 kHz

the applied model is from reference [61] with Eq. (2.16). For air forced convection cooling, the model from the reference [36] with Eq. (2.17) is applied.

C. Design Example with Two Design Approaches

To verify the proposed approach, two CM inductors were designed for a 10 kW ANPC converter with the traditional inductance-based approach and the proposed impedance-based approach. Specs of ANPC converter for EMI filter design are given in Table 3-4 and DPWM is applied to reduce the switching loss. Two design approaches are compared for the CM filter design w/o considering the frequency-dependent permeability. Design approach #1 only considers the required inductance for the first noise peak attenuation by using the permeability at the switching frequency, while design approach #2 considers the required impedance for required attenuation from 150 kHz to 2 MHz by using the model of the frequency-dependent permeability.

Table 3-5 shows the design results with two design approaches.

Fig. 3-19 shows the prototypes of two built CM inductors with two design approaches. Since the nanocrystalline cores are selected from the existing cores in the laboratory, the core size may not be the most suitable and the windows area of the selected cores has some margins.

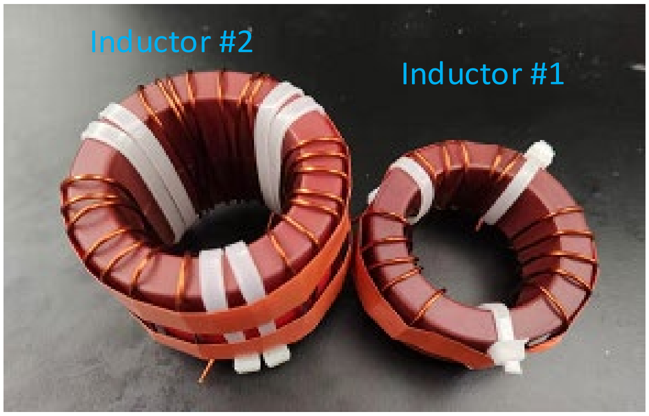
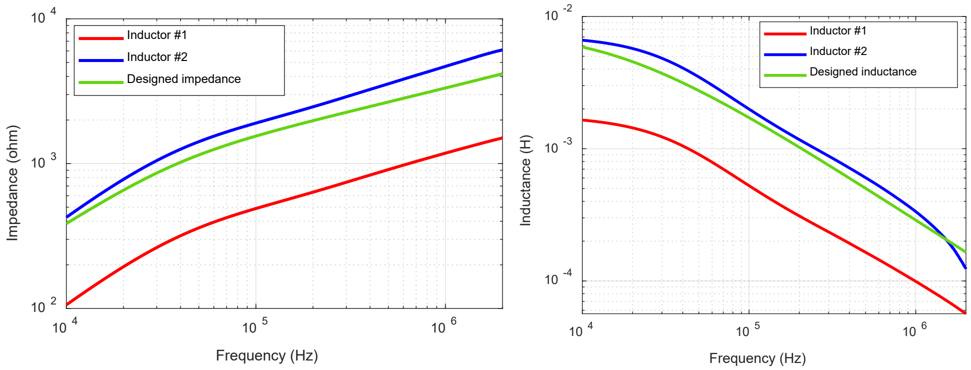


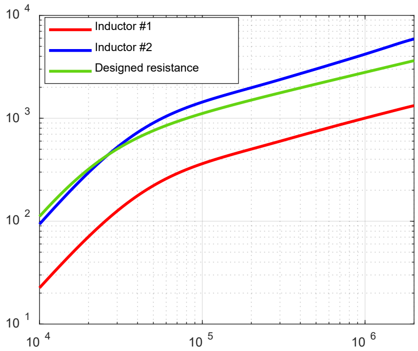
Fig. 3-19. The prototype of two CM inductors.

Table 3-5. Design results with two design approaches

Parameters	***Design Approach #1***	***Design Approach #2***
Selected Core	Vitroperm 500F T60004-L2100-W517	Vitroperm 500F T60004-L2100-W517
Core number	1	2
A_L, indutance per turn	17.5 uH @ 100 kHz	17.5 uH @ 100 kHz
Turns number	5	7
Required inductance	432 uH	N/A
Core loss calculation	18.9 W	32.1 W
Obtained CM inductance at the switching frequency	437.5 uH	857.5 uH *2
Obtained DM inductance	1.79 uH	4.6 uH * 2
AWG number	#15	# 15



(a) Impedance (b) Inductance



(c) Resistance

Fig. 3-20. Comparisons between measured results and design results.

Fig. 3-20 gives detailed comparisons between the measured data from the impedance analyzer and the design data. From Fig. 3-20, the impedance, resistance, and inductance of inductor #1 are closer to the desired values from 10 kHz to 2 MHz. Also, as shown in Fig. 3-20(b), the inductance of nanocrystalline cores varied much with the operating frequency, and the inductance decreases with the increasing of the operating frequency. However, from Fig. 3-20(c), the resistance at 2 MHz can be around 40 times of the one at 10 kHz, providing substantial impedance for the attenuation in the high frequency range. It demonstrates that the imaginary permeability induced impedance must be considered for the CM inductor design with nanocrystalline cores.

3.2.4 Experimental Results

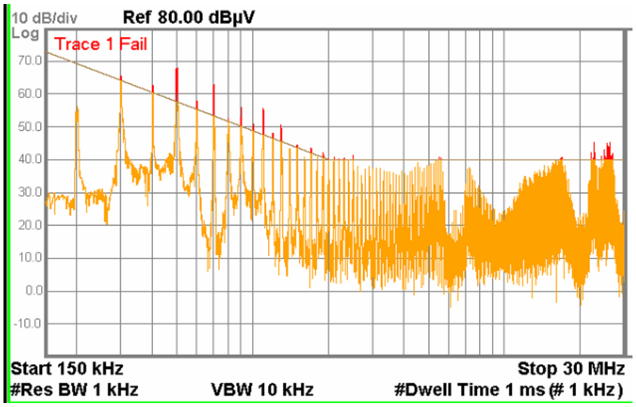
The prototype and EMI filter implementation are shown in Fig. 3-8, and the measured noise spectrums with two CM inductors are displayed in Fig. 3-21.

As shown in Fig. 3-21, the noise spectrum with the proposed design approach is a little bit lower than that with the traditional design approach at the first and second noise peaks and much lower at the higher frequency range. It illustrates that only considering the attenuation for the first noise peak and the second noise peak is not enough for the CM inductor design with nanocrystalline cores. From Fig. 3-21(b), with the impedance-based design scheme, CM noise at ac side from 150 kHz to 2 MHz are all below the EMI standard. However, for the ultra-high frequency range, from 10 MHz to 30 MHz, there are still noise peaks exceeding the EMI noise standard. The reason is the attenuation or insertion loss of the filter is mainly determined by the parasitics of filters and coupling effects at such a high frequency range. Hence, the noise behavior is very difficult to predict, and it highly depends on the layout and parasitics of filter components.

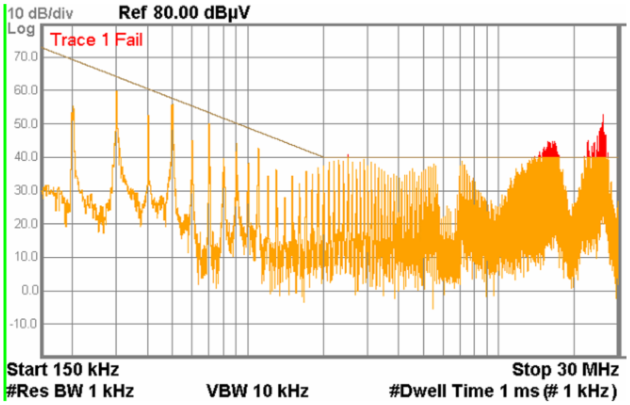
3.3 Maximum Magnetic Flux Density Model for CM Inductors

3.3.1 Limitation of Conventional Model

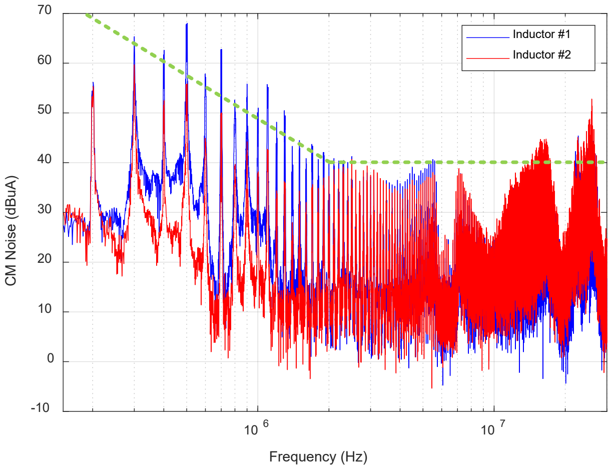
The maximum magnetic flux density calculation for CM inductors includes DM and CM flux density. The conventional model utilizes the maximum current and constant permeability to estimate the maximum common mode flux density, which is expressed as:



(a) CM noise spectrum with inductor #1



(b) CM noise spectrum with inductor #2



(c) CM noise spectrum comparison

Fig. 3-21. Noise spectrums comparison with two design inductors.

$$\begin{cases} B_{cm\_\max} = \dfrac{3L_{cm}I_{cm\_\max}}{NA_e} = \dfrac{3\mu_0\mu_r NI_{\max}}{l_e} \\ B_{dm\_\max} = \dfrac{L_{lk}I_{dm\_\max}}{NA_e} \\ B_{\max} = B_{cm\_\max} + B_{cm\_\max} \leq B_{sat} \end{cases} \tag{3.11}$$

where L_{lk} is the leakage inductance of the CM inductor, N is the turns number, A_e and l_e are the cross-sectional area of the core and the magnetic path length, I_{cm_max} and I_{dm_max} are the maximum currents of CM and DM components of output currents, B_{cm_max} and B_{dm_max} are the maximum CM and DM flux density, μ_0 and μ_r are vacuum permeability and the relative permeability of nanocrystalline materials.

One issue in Eq. (3.11) is how to select μ_r or L_{cm}, which are the frequency-dependent variables for nanocrystalline materials. If only picking the μ_r or L_{cm} at the switching frequency, it may cause either overestimation or underestimation for the maximum magnetic flux density calculation since the CM current may include rich harmonics including both high frequency and low frequency harmonics and the permeability varies much with frequency. E.g., the permeability at 10 kHz can be around 3 times the one at 100 kHz, and the difference of the maximum flux density can be huge with selecting different permeabilities at different frequencies. As a result, only using one frequency permeability and the maximum current to calculate the maximum flux density may not be accurate enough to evaluate saturation condition.

Another issue in Eq. (3.11) is how to select I_{max}. I_{max} is determined by the peak current in the time domain CM current waveform while the peak current is usually an impulse current caused by the switching actions. Based on the paper [41], the high frequency components of the impulse current are bypassed by the winding parasitic capacitance so that it only contributes to the limited amplitude of magnetic flux density. As a result, it may cause an overestimation by using the peak current value to estimate the maximum flux density. The experiment in the paper [41] also demonstrated that the sine excitation current can lead to a much higher operating flux density compared to the impulse excitation current with the same amplitude.

3.3.2 Proposed Common Mode Flux Density Model

To overcome the limitations of the conventional CM flux density model, a frequency domain calculation considering the amplitude of each harmonic and its corresponding permeability is applied to achieve a more reasonable estimation of the maximum CM magnetic flux density. CM current is converted into the frequency domain by FFT, then the magnetic flux density at each harmonic is calculated. At last, a reverse flourier transform is applied for magnetic flux density in the frequency domain to get the time domain solution:

$$\begin{cases} B_{cm}(t) = ifft\left(\dfrac{\mu_0 \mu_{r\_fi} N \sum_{n=-m}^{m} c_n e^{2\pi i(\frac{n}{T})x} I_{pk\_fi}}{l_e}\right) \\ fft(i_{cm}(t)) = \sum_{n=-m}^{m} c_n e^{2\pi i(\frac{n}{T})x} I_{pk\_fi} \end{cases} \tag{3.12}$$

where I_{pk_fi} is the amplitude of $\underline{i_{th}}$ harmonics, and μ_{r_fi} is the permeability for the $\underline{i_{th}}$ harmonics.

The CM maximum magnetic flux density calculation can be obtained by searching the maximum value of $B_{cm}(t)$ in Eq. (3.12), the saturation estimation can be more accurate with considering low frequency harmonics (3rd, 5th fundamental harmonics), and resonant current except for the switching frequency harmonics.

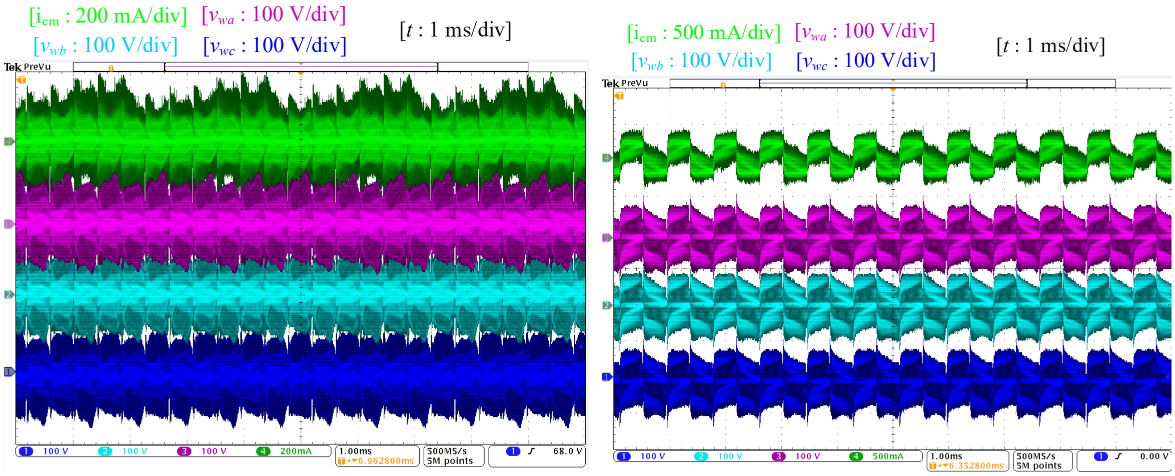
3.3.3 Verification and Comparison

To validate the proposed model, a measurement-based method is adopted to calculate the maximum flux density as the reference value. The adopted method requires to measure the voltage across the winding of the CM inductor. Then, using Eq. (3.13) to calculate flux density variation with the volt-seconds concept.

$$u = N\frac{d\varphi}{dt} \to d\varphi = \frac{udt}{N} \to dB = \frac{udt}{NA_e} \tag{3.13}$$

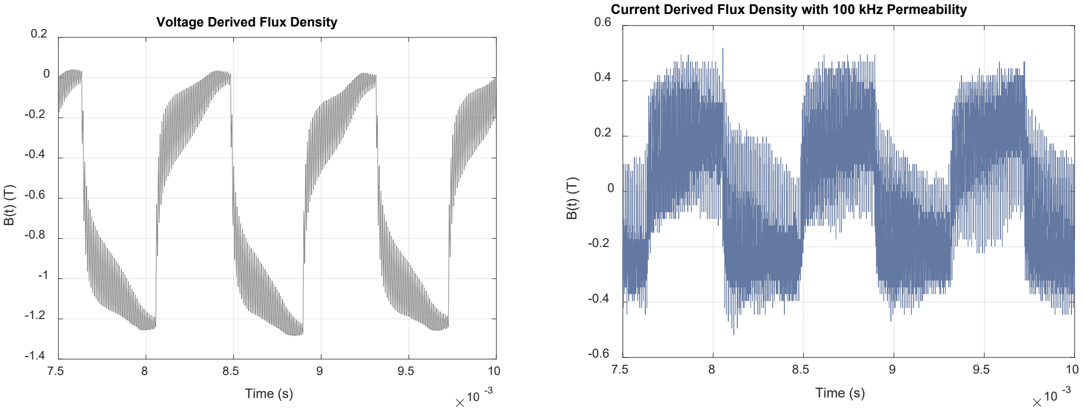
The voltage-based magnetic flux density calculation with Eq. (3.13) does not depend on any core characteristics. Hence, the results from this method can be used as a reference to evaluate the conventional and proposed current-based flux density models. Fig. 3-22 gives two cases for CM inductor winding voltage and current waveforms. In Fig. 3-22(a), the main component of CM current is the 100 kHz switching harmonics. In comparison, in Fig. 3-22(b), the main component of CM current includes both the 100 kHz switching harmonics and 1.2 kHz third fundamental harmonics.

As shown in Fig. 3-23, with the operating waveforms in the case II, the time domain magnetic flux density waveforms are derived based on the conventional and proposed models, respectively. From the comparison, the proposed model achieves much more accurate waveforms both in the amplitude of ΔB and waveform shape. Since the CM current has the third fundamental harmonics and the permeability at 1.2 kHz can be around 3 times the one at 100 kHz, the conventional model derived flux density waveform is not accurate enough by using a constant permeability at switching frequency 100 kHz.

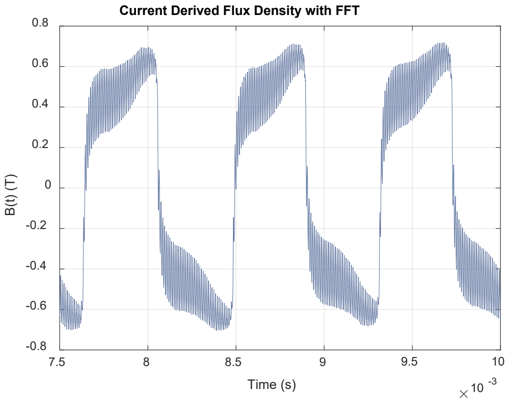


(a) Case I: low 3rd harmonics (b) Case II: high 3rd harmonics

Fig. 3-22. CM inductor voltage and current waveforms.



(a) Measured magnetic flux density (b) Convention method derived flux density



(c) Proposed method derived flux density

Fig. 3-23. Derived magnetic flux density waveforms comparison for case II.

Table 3-6. Comparison Results for Two Magnetic Flux Density Models

Case	**Voltage Derived ΔB (reference value)**	**Current Derived ΔB**				
		Peak value with constant permeability		Proposed model with FFT and frequency-dependent permeability	Peak value with filter and constant permeability	
		100 kHz	1.2 kHz	N/A	100 kHz	1.2 kHz
#1	0.3 T	0.94 T	N/A	0.27 T	0.36 T	N/A
#2	1.33 T	1.0 T	2.96 T	1.44 T	0.67 T	1.9 T

Furthermore, different methods are applied to estimate ΔB for comparison. The reference values for the two cases in Fig. 3-22 are from the voltage-based derivation. Then results with the conventional model with the constant permeability and the proposed model with FFT analysis and frequency-dependent permeability are summarized in Table 3-6. Also, for the conventional method, the peak current value selection applies two different ways. The first way of selecting the peak current is directed to use the peak current from the measured CM current waveform while the second is to implement a 5 MHz filter for the CM current waveform before selecting the peak current value. The purpose is to avoid the overestimation of the maximum flux density caused by the impulse currents which are bypassed by the winding capacitance.

For both cases I and II, the proposed model achieves the closest ΔB values compared with the reference values. For the case I, the conventional model has a much smaller difference with the reference value if choosing the peak current value with a 5 MHz filter. For the case II, due to the existence of harmonics at both low and high frequencies, the conventional model w/o filter cannot get a close estimation of ΔB compared with the reference values.

3.4 Leakage Model of Toroidal CM Inductor with Analogy of Reluctance and Capacitance

To reduce the volume and weight of differential-mode (DM) inductors, the leakage inductance of a toroidal common-mode (CM) choke is often used as partial DM inductance. However, the accurate prediction of the leakage inductance of CM chokes through an analytical model is difficult, making the determination of remaining DM inductance difficult. This dissertation proposes a modeling method with the analogy between reluctances and capacitances. The proposed method is verified by the leakage inductance comparison between the proposed model and simulation results for two CM cores with different turns numbers and wire gauges, and it demonstrated the proposed model can achieve the errors within 15% compared with simulation results for all cases.

3.4.1 Rod Core Inductance Derivation with Analogy of Reluctance and Capacitance

In this section, Navel's idea of using a rod core inductance model to calculate the leakage inductance of CM cores is still assumed correct, but the adopted rod core inductance model will be based on the conventional inductance calculation equation with equivalent DM permeability and effective path length of the leakage flux, which is not accurate enough.

In case the error of the leakage inductance is caused by the inaccuracy of the rod core inductance model in [49], this paper adopts Payne's model [135], having a maximum 1.5% error compared with measuring results, to improve the accuracy of the leakage inductance prediction. Payne's derivation of the rod core inductance provides a new perspective from the analogy between reluctances and capacitances. The idea is to obtain rod core inductance through the derivation of inductance ratio w/o the ferrite rod core, expressed as

$$
\begin{aligned}
L_f = L_{air}(L_f / L_{air}) &= \frac{R_{in\_air} + R_{out\_air}}{R_{in\_f} + R_{out\_f}} L_{air} \\
&= \frac{R_{in\_air} / R_{out\_air} + 1}{(R_{in\_air} / \mu_f) / R_{out\_air} + 1} L_{air}
\end{aligned}
\tag{3.14}
$$

where L_{air} is the air core inductance and L_f is the inductance with insertion of the rod ferrite core, R_{in_f} and R_{in_air} are the reluctance inside windings w/o the rod ferrite core, R_{out_f} and R_{out_air} are the reluctance outside winding w/o the rod ferrite core, and μ_f is the permeability of the ferrite core.

Since the space and material outside winding do not change without the insertion of the rod ferrite core, R_{out_air} and R_{out_f} can be assumed as the same value. However, the reluctance inside winding with rod ferrite core will decrease μ_f times than the one of the air-core inductor because of the high permeability of ferrite material. L_{air} is well studied with previous literature, so the only unknown term in Eq. (3.14) is the reluctance ratio between inside windings and outside windings for an air-core inductor. To derive the reluctance ratio, an analogy between reluctances and capacitances is applied. As shown in Fig. 3-24, the magnetic fields of rod core inductors and the electric fields of plate capacitors are quite similar. Also, based on the duality of reluctance and capacitance from Fig. 3-25 and Eq. (3.15), the reluctance can be analogized to the reciprocal of the capacitance. Hence, the reluctance ratio between inside and outside windings is converted to a derivation of the capacitance ratio between outside and inside plates, shown as Eq. (3.15).

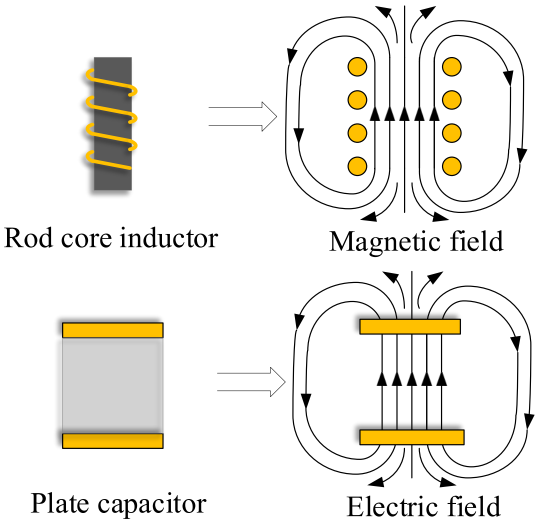
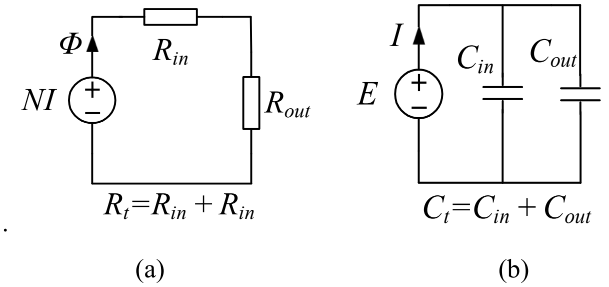

Rod core inductor
Magnetic field
Plate capacitor
Electric field

Fig. 3-24. The analogy between the electric field of plate capacitors and the magnetic field of rod core inductors.


Φ
R_{in}
NI
R_{out}
$R_t=R_{in}+R_{in}$
I
C_{in}
C_{out}
E
$C_t=C_{in}+C_{out}$

(a) (b)

Fig. 3-25. The duality between: (a). magnetic circuits, (b). electrical circuits.

$$\left.\begin{aligned} R &= \frac{1}{\mu_0 \mu_r}\frac{l}{A} \\ C &= \varepsilon_0 \varepsilon_r \frac{A}{l} \end{aligned}\right\} \Rightarrow R \sim \frac{1}{C} \Rightarrow \frac{R_{in\_air}}{R_{out\_air}} = \frac{C_{out}}{C_{in}} \tag{3.15}$$

The reason for using the analogy is the external magnetic fields outside winding is more complex and less well known, while the electric fields of such a structure in Fig. 3-24 is provided by Rappaport [136] for a monopole antenna. Then the reluctance ratio is obtained from the capacitance ratio in Eq. (3.16).

$$\begin{aligned} \frac{R_{in\_air}}{R_{out\_air}} &= \frac{C_{out}}{C_{in}} \approx \frac{l_c}{\pi r_c^2} / \frac{1}{3.49 r_c} \\ &= \frac{3.49 l_c}{\pi r_c} \approx 1.022 \frac{l_c}{r_c} \end{aligned} \tag{3.16}$$

where l_c is the length of the winding coil, and the r_c is the radius of the winding coil.

With the reluctance ratio, the final closed-form equation of the rod core inductance can refer to paper [135], and Payne [135] claims that the error of the proposed rod core inductance model is within 1.5%. To validate the effectiveness of using Payne's model to predict leakage inductance of CM choke, a ferrite toroidal core ZW435610TC from Magnetics was used to build CM chokes with different turns numbers. The comparison results with Nave's model and measuring results are shown in Fig. 3-26. As shown in Fig. 3-26, with few turns number, both Payne's model and Nave's model achieve high accuracy. Nonetheless, when turns number increases from 7 to 28, the error of Nave's model increases from 7.4% to 36.6% and the error of Payne's model also increases from 1.67% to 26.86%.

From the above analysis, although Payne's rod core inductance model achieves a smaller error compared to the Nave's leakage model, the error is still large when the winding has many turns.

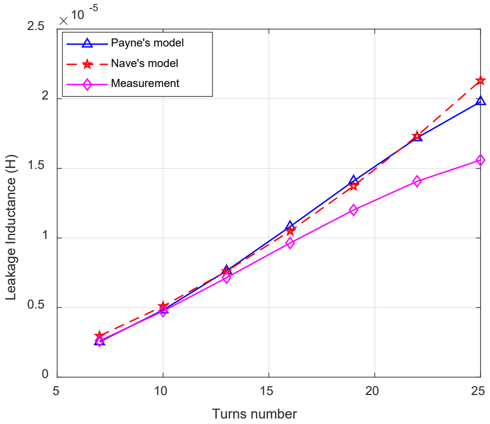
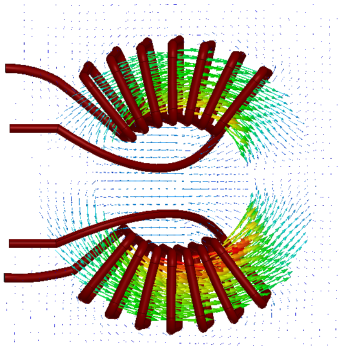


Fig. 3-26. Leakage modeling comparison with two rod core inductance models.

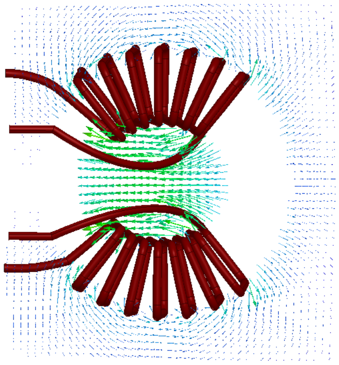
3.4.2 Leakage Inductance of CM Choke Derivation

Only using the rod core inductance model is not accurate enough for the leakage evaluation for the toroidal CM choke especially when the turns number is large. Fig. 3-27(a) illustrates the magnetic fields of a two-phase CM choke for both DM and CM flux and Fig. 3-27(b) displays only the leakage flux distribution. As can been seen, the leakage flux distribution in Fig. 3-27(b) is different from the magnetic fields of rod core inductor. For the upper winding, the fluxes outside winding are not symmetrical and the amplitude of fluxes in the lower side of the winding is larger than that in the upper side of winding. Hence, the assumption for Eq. (3.14) that R_{out_air} and R_{out_f} have the same value is not correct since the distribution of leakage flux with the large turns number has been changed. Eq. (3.14) for leakage inductance derivation must be corrected as

$$\begin{aligned} L_f &= L_{air}(L_f / L_{air}) = \frac{R_{in\_air} + R_{out\_air}}{R_{in\_f} + R_{out\_f}} L_{air} \\ &= \frac{R_{in\_air} / R_{out\_air} + 1}{(R_{in\_air} / \mu_f) / R_{out\_air} + R_{out\_f} / R_{out\_air}} L_{air} \end{aligned} \tag{3.17}$$

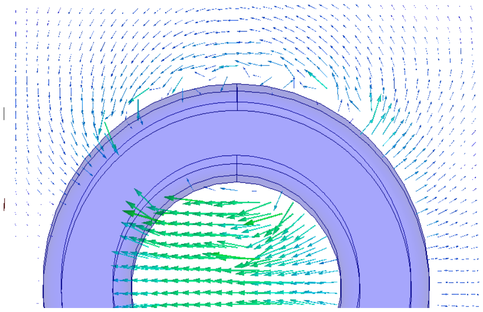


(a) Both CM and DM flux

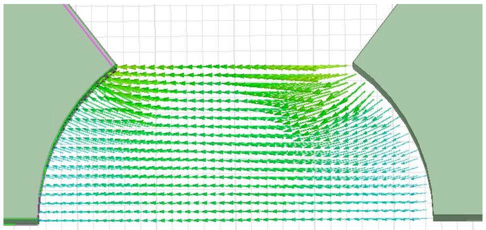


(b) Only DM (leakage) flux

Fig. 3-27. Magnetic fields of two-phase CM choke (hiding toroidal core).



(a) Leakage flux distribution



(b) Electric fields of two curved surfaces

Fig. 3-28. The analogy of magnetic fields and electric fields for a CM choke with a large turns number.

Compared with Eq. (3.14), Eq. (3.17) needs to derive R_{out_f} over R_{out_air}. The solution here is still to convert the derivation of the reluctance ratio to the derivation of the capacitance ratio. To construct the electric field analogy for the magnetic fields of leakage flux of the CM choke with a large turns number, a new geometry of metal sheet is given in Fig. 3-28(b). Comparing Fig. 3-28 (a) and (b), the leakage flux inside the toroidal core is close to the electric field of the two curved metal surfaces. With this the analogy assumption, the reluctance ratio of R_{out_f} over R_{out_air} can be derived as Eq. (3.18) by the calculation of the capacitance of two curved surfaces.

$$\frac{R_{out\_f}}{R_{out\_air}} = \frac{C_{out\_air}}{C_{curved} + C_{out\_air} / 2} \tag{3.18}$$

where C_{curved} is the capacitance of two curved surfaces.

To simplify the derivation of C_{curved}, two curved faces are regarded as two folded planes shown in Fig. 3-29 with the solid orange curves. With this equivalent geometry, the derivation of the capacitance of two curved faces is converted into the derivation of the capacitance of two non-parallel planes shown in Fig. 3-30.

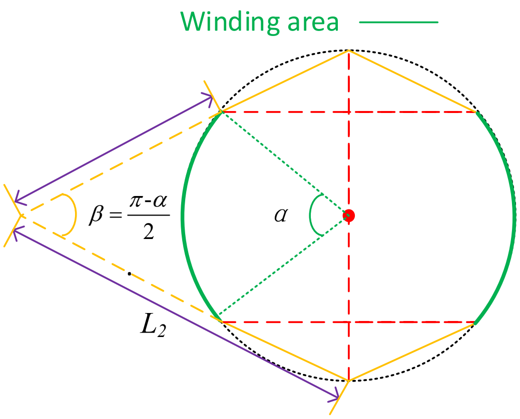


Fig. 3-29. Geometry equivalent transformation from curved faces to folded planes.

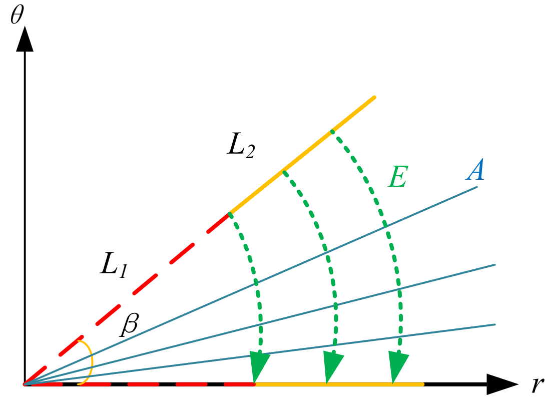


Fig. 3-30. Electric filed for non-parallel planes in polar coordinates.

Based on the symmetry, any plane including the origin point is the equipotential plane for the electric filed inside two non-parallel planes. As a result, the electric field intensity is only related to the distance r from the origin point and the direction of the electric field is perpendicular to equipotential planes. With this observation, electric filed intensity and electrical potential inside two planes are written as

$$\begin{aligned} E_{(r,\theta)} &= E_r e_\theta \\ U_{(r,\theta)} &= U_\theta \end{aligned} \tag{3.19}$$

Due to the continuity of potential, the electrical potential in polar coordinate can be analyzed as

$$\frac{\partial^2 U}{\partial^2 r} + \frac{1}{r}\frac{\partial U}{\partial r} + \frac{1}{r^2}\frac{\partial^2 U}{\partial^2 \theta} = 0 \tag{3.20}$$

From Eq. (3.19), the electrical potential is irrelevant to the distance r, so Eq. (3.20) is simplified as

$$\frac{1}{r^2}\frac{\partial^2 U}{\partial^2 \theta} = 0 \tag{3.21}$$

Eq. (3.21) can be solved with the general solution of a quadratic differential equation with the initial conditions:

$$\begin{aligned} &U{=}U_1-\frac{U_1-U_2}{\beta}\theta \\ &\text{where } \ \theta=0, U=U_1; \theta=\beta, U=U_2 \end{aligned} \tag{3.22}$$

Then, the electric field intensity and charge density can be derived as

$$\begin{cases} E=-\nabla U=\dfrac{U_1-U_2}{ra} \\ \sigma_r=\varepsilon_0 E=\dfrac{U_1-U_2}{ra}\varepsilon_0 \end{cases} \tag{3.23}$$

The capacitance of non-parallel planes finally is calculated based on the definition:

$$\begin{aligned} C&=\frac{Q}{\Delta U}=\frac{\int_{L_1}^{L_2}\sigma_r dS}{U_1-U_2} \\ &=\frac{H_t\varepsilon_0\dfrac{U_1-U_2}{\beta}\int_{L_1}^{L_2}\dfrac{1}{r}dr}{U_1-U_2}=\frac{H_t\varepsilon_0}{\beta}\ln\frac{L_2}{L_1} \end{aligned} \tag{3.24}$$

where L_1 and L_2 are labeled in Fig. 3-29, β is the angle between two non-parallel planes, α is the winding angle, H_t is the height of the core.

Substituting L_2 and L_1 by the calculations with the dimensions of the core, C_{curved} is obtained as

$$\begin{aligned} C_{curved}&=\frac{2H_t\varepsilon_0}{\beta}\ln\frac{r_{inner}/\sin(\beta/2)}{r_{inner}\cos(\beta)/\sin(\beta/2)} \\ &=\frac{2H_t\varepsilon_0}{\beta}\ln\frac{1}{\cos(\beta)} \end{aligned} \tag{3.25}$$

where r_{inner} is the radius of the inner side of the core.

The second approach to estimate the capacitance of two curved faces is to directly apply the equation for the capacitance of parallel plates since the electric field between two curved faces shown in Fig. 3-28(b) is very similar to the electric field of two parallel plates. The surface area is approximated by using the curved face's area, and the distance between two curved faces is averaged by the maximum and the minimum values. The final expression is:

$$\begin{aligned} C_{curved\_sc} &= \frac{\varepsilon_0(\pi-\alpha)H_t r_{inner}}{(2r_{inner}+2r_{inner}\cos(\beta))/2} \\ &= \frac{\varepsilon_0(\pi-\alpha)H_t}{1+\cos(\beta)} \end{aligned} \tag{3.26}$$

Combining Eq. (3.16), Eq. (3.17), and Eq. (3.25) or Eq. (3.26), the corrected leakage inductance can be calculated.

For the first proposed model, C_{curved} is derived by the equivalent geometry and the capacitance of non-parallel plates. The reluctance ratio of R_{out_f} over R_{out_air} is:

$$\left.\frac{R_{out\_f}}{R_{out\_air}}\right|_{first} = \frac{3.49r_c}{\frac{2H_t\varepsilon_0}{\beta}\ln\frac{1}{\cos(\beta)}+3.49r_c/2} \tag{3.27}$$

For the second proposed model, C_{curved} is derived by the approximation of curved faces as the two parallel plates. The reluctance ratio of R_{out_f} over R_{out_air} is:

$$\left.\frac{R_{out\_f}}{R_{out\_air}}\right|_{\sec ond} = \frac{3.49r_c}{\frac{\varepsilon_0(\pi-\alpha)H_t}{1+\cos(\beta)}+3.49r_c/2} \tag{3.28}$$

3.4.3 Verification of Proposed Leakage Model

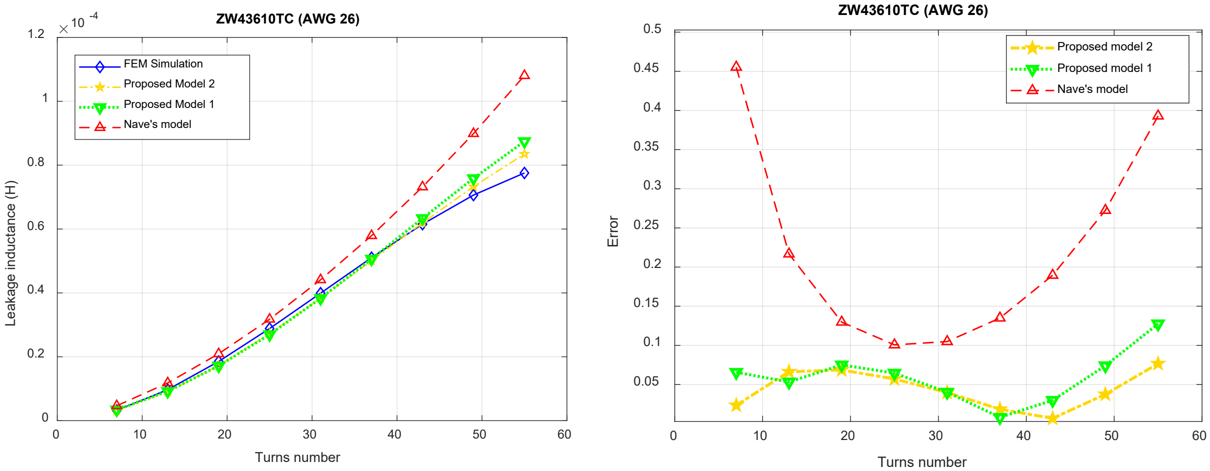
To verify the effectiveness of the proposed model, 3-D FEM simulations were conducted in COMSOL, and the simulation results were provided and verified by the paper [50] and have only a 1% error compared with the measuring results.

Fig. 3-31(a)-(d) gives the comparison results for the toroidal ferrite core ZW43610TC with AWG 26 wires and AWG 11wires. As it shows in Fig. 3-31(b), the errors of the proposed models drop from 40% to 10% compared with Nave's model when the turns number is 55. For different turns numbers, the errors of the proposed model 2 keep within 10%, and errors of proposed model 1 keep within 15%. The proposed model 2 achieves a little bit higher accuracy at 55 turns.

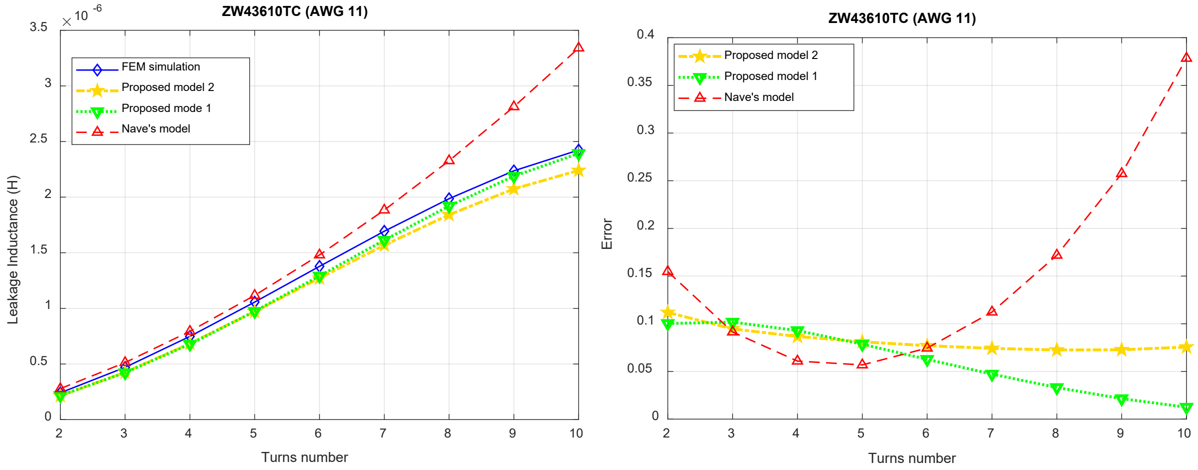
In Fig. 3-31(d), when the winding changes to AWG #11 wires, for different turns numbers, the errors of the proposed model 1 and 2 are both below 10%. However, the proposed model 1 can achieve 5% less error compared with the proposed model 2 at 10 turns.

Fig. 3-32(a)-(d) shows another example for the toroidal ferrite core ZW44825TC with AWG #20 wires and AWG #8 wires. When using AWG #20 wires, as same as the first case, the maximum error of the proposed model drops from 40% to 5% compared with Nave's model when the turns number is 20. However, in this case, when the turns number is 5, Nave's model shows better accuracy. For other turns number except 5, the proposed models show much better accuracy.

In Fig. 3-32(d), when the winding changes to AWG #8 wires, for different turns numbers, the errors of the proposed model 1 and 2 are both below 5%. In the whole turns number range, the proposed models show a much higher accuracy. Also, the proposed model 1 has 3% less error compared with the proposed model 2.

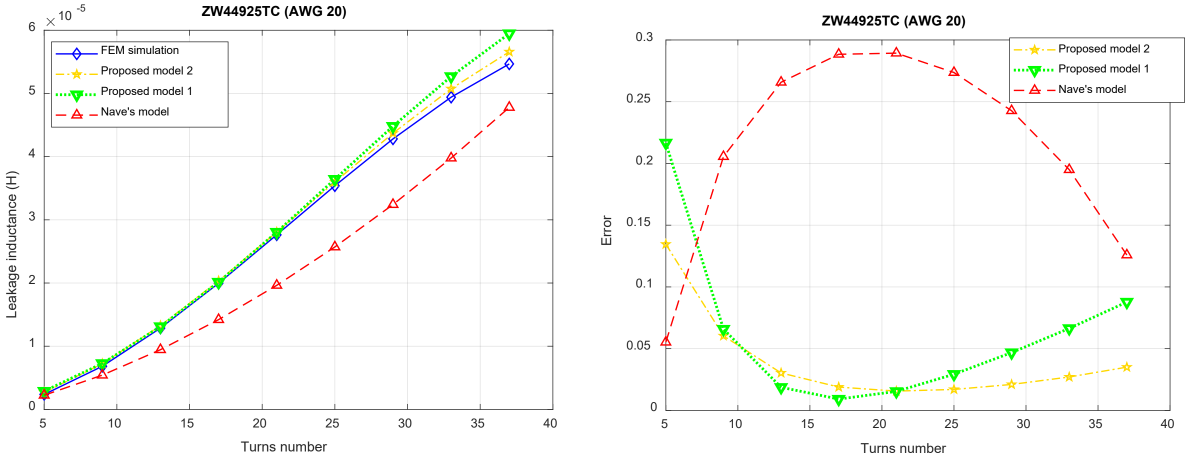


(a) Leakage inductance comparison with AWG #26 winding (b) Absolute error comparison with AWG # 26 winding

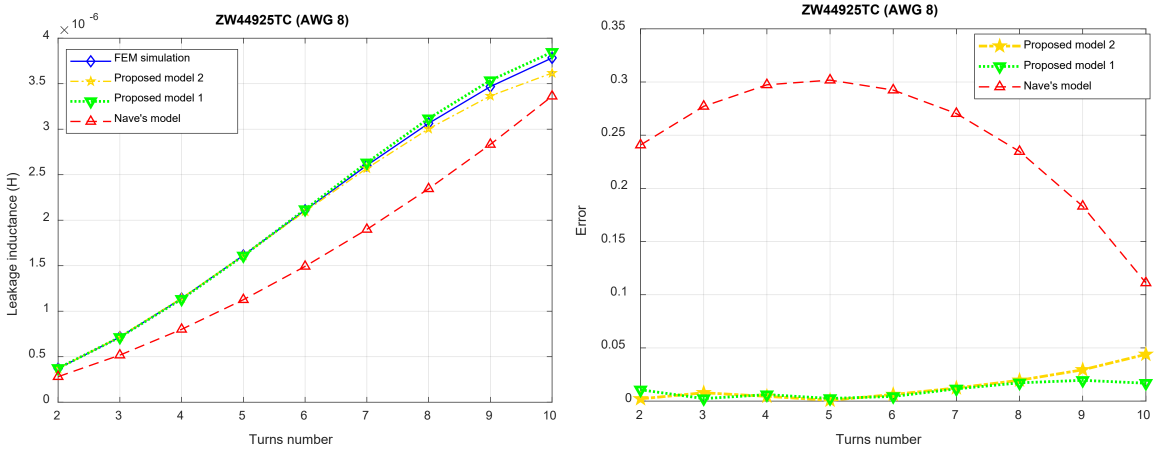


(c) Leakage inductance comparison with AWG #11 winding (d) Absolute error comparison with AWG # 11 winding

Fig. 3-31. Comparison of leakage inductance models with FEM simulation results for magnetic core ZW43610TC.



(a) Leakage inductance comparison with AWG #20 winding (b) Absolute error comparison with AWG # 20 winding



(c) Leakage inductance comparison with AWG #8 winding (d) Absolute error comparison with AWG # 8 winding

Fig. 3-32. Comparison of leakage inductance models with FEM simulation results for magnetic core ZW44925TC.

From comparisons, the proposed models show a much higher accuracy in most cases, especially for the large turns number. Only at two testing points with the low turns number, Nave's model has better accuracy, but the proposed models also have acceptable accuracy within 15% at those points. The proposed model 1 has better accuracy when using a larger wire diameter compared with the proposed model 2. For wires with smaller wire diameter, the proposed model 2 shows better accuracy than the proposed model 2. But in general, two proposed models both can achieve much higher accuracy compared with Nave's model, and the errors in different cases are lower than 15%.

3.5 Film Capacitor Model

Compared with film capacitors, the main advantage of aluminum electrolytic capacitors is the energy density can be ten times higher than that of film capacitors [137]. However, two factors hinder the application of aluminum electrolytic capacitors in aviation applications. First, aluminum electrolytic capacitors only have a one-fifth lifetime of film capacitors and much less ripple current capability [138]. Second, aluminum electrolytic capacitors are more sensitive to the temperature. The capacitance varies around 30% for the whole operating temperature range [138]. Also, the dissipation factor can be changed around 10% for the whole operating temperature range [138]. Hence, in this dissertation, film capacitors are selected for EMI filters design and dc-link capacitors in terms of lifetime and temperature-dependent characteristics for aviation applications.

To have a more accurate design results, frequency-dependent ac voltage rating and ESR are modeled in this section.

3.5.1 Frequency-Dependent Ac Voltage Rating Model

One of the characteristics of film capacitors is the frequency-dependent ac voltage rating. In the aviation power system, the main frequency varies from 360 Hz to 800 Hz. As a result, the ac RMS voltage rating at this frequency should be paid attention to for the safety consideration.

As Fig. 3-33 shows, three different factors contributing to determine the ability of a film capacitor to withstand the ac voltage at different operating frequency ranges [139]. In frequency range *a*, the voltage rating is limited by corona discharge, degrading the film metallization. In frequency range b, above the frequency f_1, the ac voltage rating is determined by the thermal power dissipation. In even higher frequency range c, the ac voltage rating is limited by the allowed current through the contacts, avoiding causing overheat.

Generally, only the frequency range a and b are the technical interesting range in power electronics. Fig. 3-34 illustrates how the ac RMS voltage rating of one film capacitor varies with operating frequency. Below the corner frequency f_c, shown in Fig. 3-34, the ac RMS voltage rating keeps fixed while it drops with a falling slope when the frequency is higher than f_c.

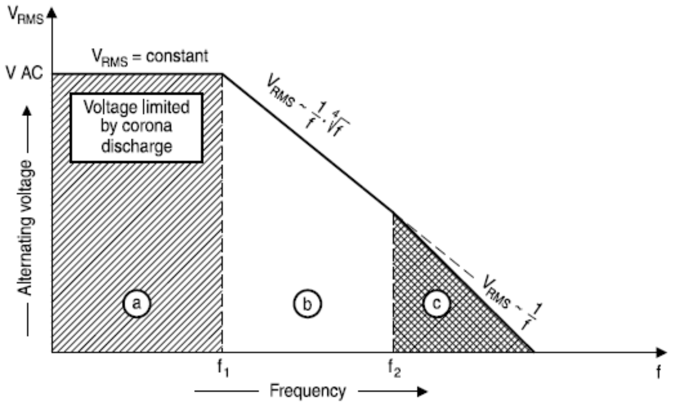

V_{RMS}
V AC
V_{RMS} = constant
Voltage limited by corona discharge
Alternating voltage
$V_{RMS} \sim \frac{1}{f \cdot \sqrt[4]{f}}$
$V_{RMS} \sim \frac{1}{f}$
a
b
c
f_1
f_2
f
Frequency

Fig. 3-33. Limits for maximum ac RMS voltage with the operating frequency [139].

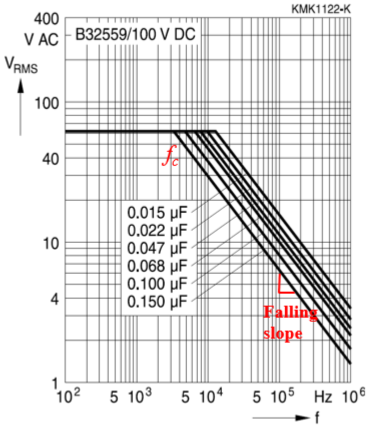


Fig. 3-34. The typical ac voltage rating curves as a function of the frequency.

Based on this characteristic, three key parameters from this curve are collected in the database of film capacitors, which are the voltage rating at low frequency V_{AC}, the corner frequency f_c, and the falling slope of the curve -*k*. With those parameters, the ac RMS voltage rating higher than corner frequency can be expressed as

$$\log(V_{RMS}(f)) = \log(V_{AC}) - k[\log(f) - \log(f_c)] \tag{3.29}$$

With Eq. (3.29), the ac RMS voltage above the corner frequency can be derived as

$$V_{RMS}(f) = V_{AC}(\frac{f}{f_c})^k \tag{3.30}$$

3.5.2 ESL and ESR Model

In main power circuits, ESL of a dc-link film capacitor can contribute to the parasitic inductance of the power loop, impacting the switching behavior and overvoltage. For EMI filters, ESL of a film capacitor influences the insertion loss of the whole EMI filter at the high frequency range. ESL of a film capacitor can be easily obtained from impedance curves in the datasheet. With getting the corner frequency of an impedance curve, the ESL is derived from Eq. (2.19)

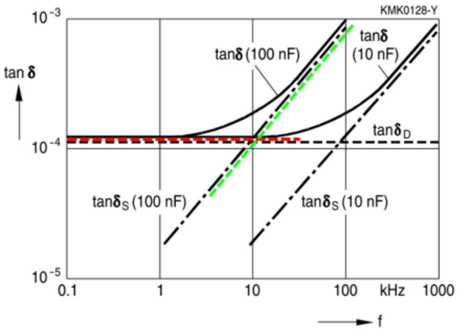


Fig. 3-35. The measured dissipation factor as a function of the frequency in [139].

$$L_{ESL} = \frac{1}{4\pi^2 {f_{self-reson}}^2 C} \tag{3.31}$$

ESR is also a frequency-dependent variable like ac RMS voltage rating for film capacitors, determined by the dissipation factor. However, the frequency-dependent ESR is not given in the datasheet, and usually only are dissipation factor at 1 kHz and 100 kHz given. To obtain the ESR in the technical interesting frequency range, the characteristic of the dissipation factor must be analyzed from 100 Hz to 1 MHz.

One example of the measured dissipation factor curve is given in Fig. 3-35. In the low frequency range from 10 Hz to 1 kHz, the dissipation factor is fixed value since the loss is determined by the energy consumed to polarize and depolarize the dielectric materials. However, based on Eq. (2.20), the ESR varied with frequency for a fixed DF. The ESR at this frequency range can be calculated with the dissipation factor at 1 kHz

$$R_{ESR} = \frac{\tan\delta}{2\pi f C} \tag{3.32}$$

Once the frequency is higher than 1 kHz, the ESR is determined by the series resistance, which is a constant value. This ESR can be calculated with DF data at 100 kHz from the capacitor's datasheet.

3.6 Ac Dv/dt Filter Design Routine and Optimization with A_P prediction

High *dv/dt* can lead to damage and premature failure of the motor winding insulation by high voltage spike caused by reflected waveform through long cables of motor drives. In this section, a weight-oriented ac *dv/dt* filter design approach with A_p value prediction is presented.

3.6.1 Determination of Corner Frequency of *Dv/dt* Filter

The corner frequency of a *dv/dt* filter is decided by the targeted *dv/dt* value related to cable length and the insulation requirement. If the length of the motor drive output cable is short, the required *dv/dt* limit based on the reflected voltage is much higher than some standards. To have a conservative design to keep the safe operation of motors, 0.5 V/ns as a design target is selected based on NEMA MG1-PART 30 for general motors with an output voltage higher than 600 V.

If the length of the output cables is long, the overvoltage will be the main consideration to decide the *dv/dt* limit. For 3-phase motor drives, instead of the single-core wire, three core bundled wires are adopted for ac outputs shown in Fig. 3-36 to consider the coupling effects among three bundled wires. To extract parasitics of three core bundled wires, Hafner [141] developed a sequence impedance model considering the coupling and the interconnection of sheaths. However, the analytical model in [141] is too complicated to use with the Bessel function. To simplify the model, a lumped parasitic model from ABB documents [140] is applied, but it is only validated for the positive sequence excitation, which are normal operating conditions for a balanced 3-phase system. The model is given as follows:

$$\begin{cases} L_{\mathrm{c}} = 0.05 + 0.2\ln\left(\dfrac{K \cdot s}{r_c}\right) \ \ [\mathrm{mH/km}] \\ C_c = \dfrac{\varepsilon_r}{18\ln\dfrac{r_0}{r_i}} \ \ [\mu\mathrm{F/km}] \end{cases} \tag{3.33}$$

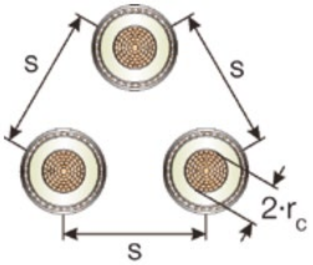


Fig. 3-36. The illustration of three cores bundled wires in [140].

where K=1 for the trefoil formation and K=1.26 for flat or single formation, s is the distance between conductor axes and r_c is the conductor radius in mm illustrated in Fig. 3-36, r_o is the external radius of the insulation and r_i is the radius of a conductor including a screen in mm, ε_r is the relative permittivity of the insulation material, which is 2.5 from IEC 60287 for cross-linked polyethylene(XLPE).

With the cable model, the time t_t for the inverter output pulse to travel from the inverter terminals to the motor terminals can be derived as:

$$\begin{cases} t_t = \dfrac{l_c}{v} \\ v = \dfrac{1}{\sqrt{L_c C_c}} \end{cases} \tag{3.34}$$

where l_c is the cable length, L_c is the cable inductance per unit length, C_c is the capacitance per unit length.

Based on the literature [142], when the traveling time t_t is shorter than one-third of the PWM pulse rise time t_r, the peak voltage of the cable considering PWM pulse rise time is given as

$$V_{pk} = \frac{3 l_c V_{dc} \Gamma_L}{v t_r} + V_{dc} \quad for\ t_t < \frac{t_r}{3} \tag{3.35}$$

where Γ_L is the voltage reflection coefficient, and it is generally between 0.9 and 1 when the cable impedance is much smaller than the load impedance.

Assuming the allowed maximum overvoltage is 1.2 times of the dc-link voltage, the desired PWM pulse rise time called the critical rise time t_{cr} is derived as:

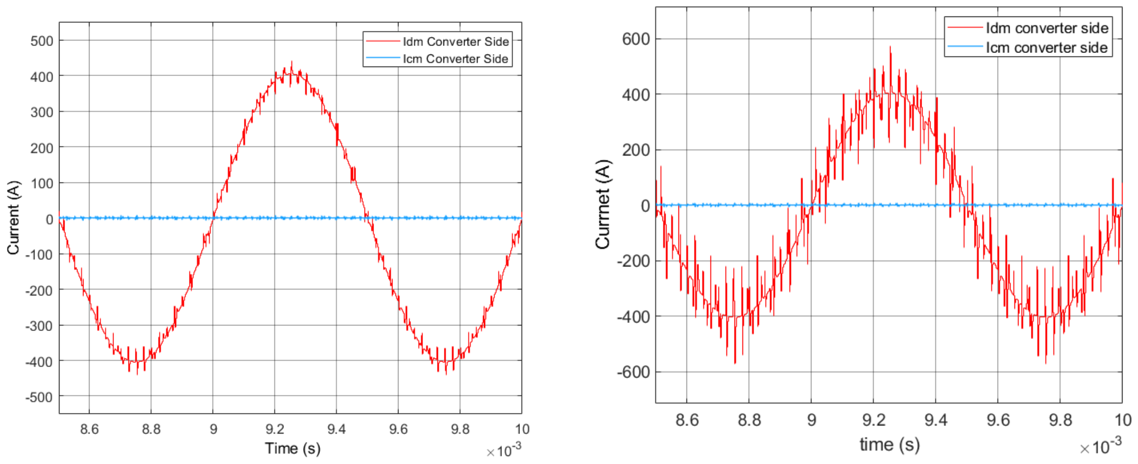
$$\frac{3l_c\Gamma_L}{vt_{cr}} \simeq 0.2 \Rightarrow t_{cr} = \frac{3l_c\Gamma_L}{0.2v} \tag{3.36}$$

With desired *dv/dt* value (when the cable length is short) or the critical rise time t_{cr} (when the cable length is long), the corner frequency of *dv/dt* filter can be determined as

$$\begin{cases} T_r = 2t_{cr} = \dfrac{2V_{dc}}{Dvdt_{\lim}} \\ f_{c\_dvdt} = \dfrac{1}{2t_{cr}} \end{cases} \tag{3.37}$$

3.6.2 Distribution of L and C with a Targeted Corner Frequency

With the derived corner frequency of *dv/dt* filter, there is still an issue on how to distribute L and C values at a fixed corner frequency. Fig. 3-37 gives the waveforms with different LC combinations, and as can be seen, the output phase current in Fig. 3-37(b) shows a much higher current ripple compared with that in Fig. 3-37(a). As a result, even though the inductance of Fig. 3-37(b) is smaller than the one in Fig. 3-37(a), the weight of the inductor of *dv/dt* filter of Fig. 3-37(b) still can be heavier since the high current ripple caused saturation can lead to a large core size compared with the small current ripple in Fig. 3-37(a).



(a). $L_f = 10\ \mu H$, $C_f = 91\ nF$, $R_f = 20.9\ \Omega$ (b). $L_f = 2\ \mu H$, $C_f = 460\ nF$, $R_f = 4.18\ \Omega$

Fig. 3-37. Converter ac side output current with different LC combinations when the corner frequency of *dv/dt* filter is 166.7 kHz.

Manually trial-and-error could be a good solution to find reasonable design, but it may also miss better design results, and there is a trade-off design between the inductance selection and current ripple amplitude in terms of weight optimization. Here an A_P-based weight optimization algorithm is proposed to search the best LC combination. A_P is defined as a multiplication of the required core cross-sectional area and the core windows area for winding, indicating the required power of an inductor. Eq. (3.38) shows the derivation of A_P, which used as a weight indicator in the inductor design. A plot between magnetics core weight and A_P value is made from the collected core database for this design in Fig. 3-38, further illustrating a higher A_P value will indicate a heavier magnetics core.

$$\left.\begin{array}{l} \left.\begin{array}{l} U = N\dfrac{d\phi}{dt} \\ U = L\dfrac{dI}{dt} \\ d\phi = \Delta B A_e \end{array}\right\} \Rightarrow A_e = \dfrac{L\Delta I}{N\Delta B} \\ \\ A_w = \dfrac{N I_{rms}}{J} \end{array}\right\} \Rightarrow A_p = A_e \cdot A_w = \frac{L I_{\text{peak}} I_{rms}}{J B_{\max}} \tag{3.38}$$

where N is the turns number of inductors, L is the inductance, I_{peak} is the peak inductor current, I_{rms} is the RMS of the inductor current, J is the inductor current density, B_{max} is the allowed maximum operating magnetic flux density.

With the weight indicator A_P, a prediction of the peak and RMS value of the output phase current is required for the A_P calculation. Getting the data from the simulation is one option but it is far away from efficient, and the simulation needs to be run so many times once the LC value is changed. Hence, an analytical approach is adopted here. First, the PWM voltage is obtained from a one-time simulation. Then, the PWM terminal voltage shown in Fig. 3-39(a) can be transferred into the frequency domain with double side Fourier analysis. Second, with selected LC value for *dv/dt* filter, in the frequency domain, each harmonics current can be calculated with equivalent circuits in the ac side. Then, the output current in the time domain shown in Fig. 3-39(b) can be synthesized with the amplitude and phase information in the frequency domain. With such information, A_P will be calculated with the peak current and RMS of the synthesized current waveform.

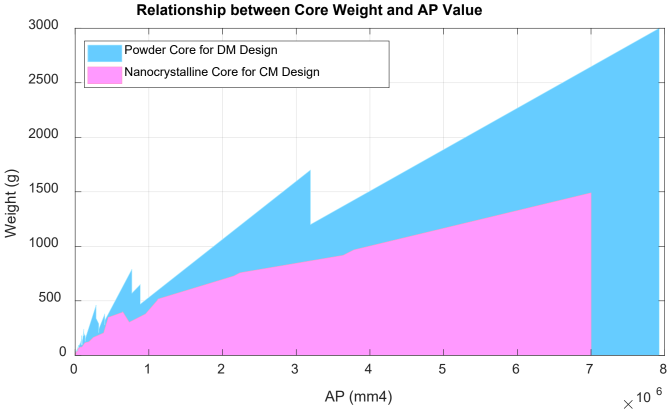
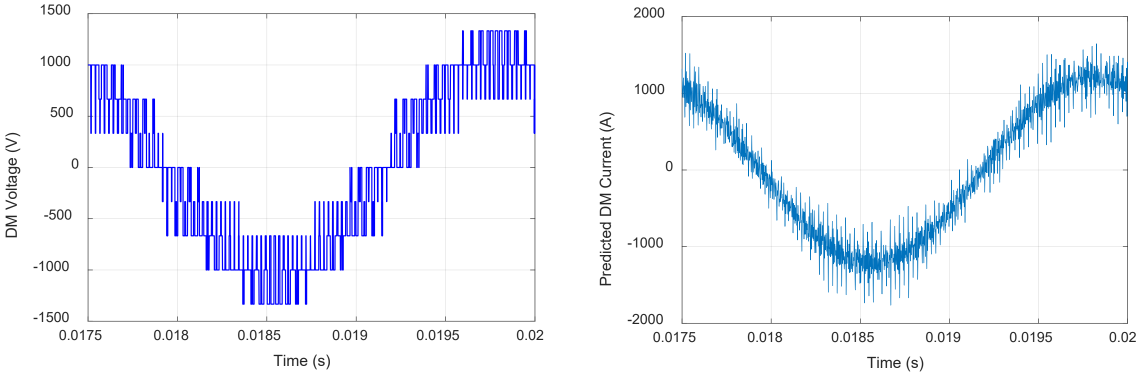


Fig. 3-38. Relationship between core weight and AP value.

Fig. 3-40 gives one example to illustrate the design iteration of LC value determination for *dv/dt* filter. For a fixed frequency, a small capacitance value as 10 nF is selected as C_{base}. The capacitance of *dv/dt* filter is decided by using a factor *N* to multiply the C_{base}. As *N* increases, the capacitance of *dv/dt* filter rises while the inductance of *dv/dt* filter drops. At a specific *N*, an A_P value is calculated with the analytical model. After sweeping N from 1 to 100, an A_P curve like Fig. 3-40 can be obtained to choose the LC value by *N* for the minimum A_P value.



(a) (b)

Fig. 3-39. Output current prediction with phase PWM voltage: (a) PWM voltage of bridge output terminal, (b) predicted output current.

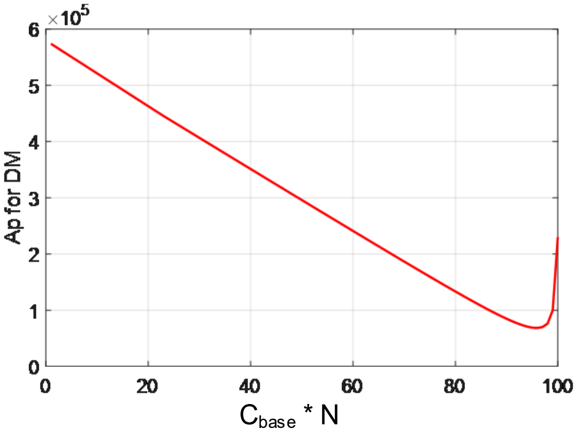


Fig. 3-40. One optimization example for dv/dt inductor.

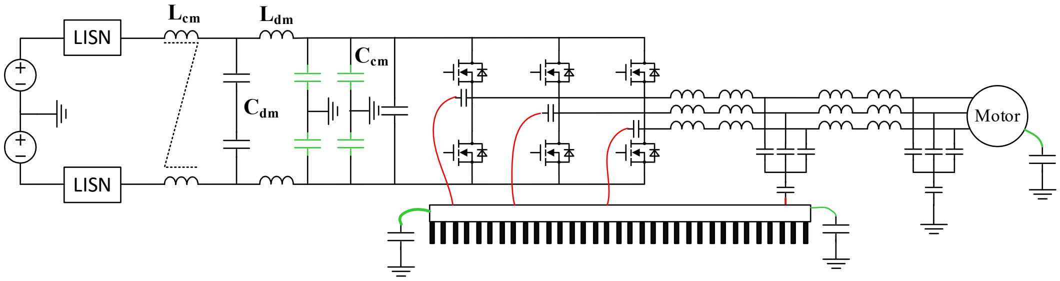
3.7 PSO-based EMI Filter Routine and Optimization

Two EMI configurations are adopted in the project as shown in Fig. 3-41. EMI configuration in Fig. 3-41(a) is a normal EMI configuration in dc side with two-phase common-mode (CM) inductors. For the EMI configuration in Fig. 3-41(b), a three-phase CM inductor is used since the neutral wire of dc input is connected to the middle point of the dc-link of the converter to achieve the voltage balancing of the middle point of dc-link voltage. In addition, for a motor drive system, the ac side EMI filters are not necessarily required. Depending on the different applications and the cable length, either *dv/dt* filters or EMI filters can be applied in the ac outputs for the 3-phase motor drive system.

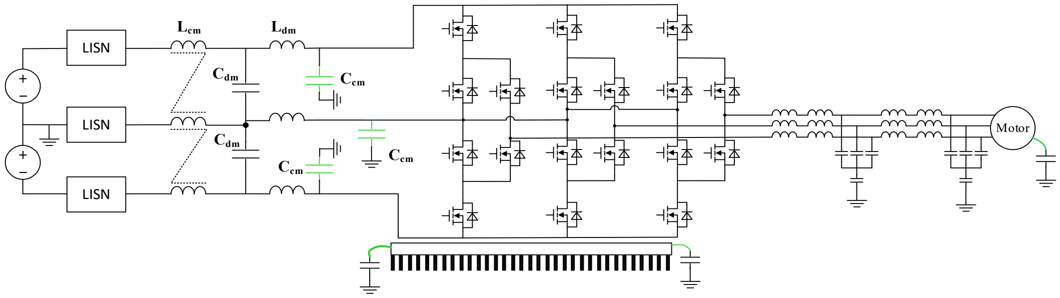
3.7.1 Determination of Corner Frequency of EMI Filter

Based on the principle of the impedance mismatch, the proper filter structure can be selected to achieve near ideal attenuation. A fixed noise attenuation 40 dBuA/dec for first-order LC filters or 80 dBuA/dec for second-order LC filters can be applied to get the corner frequency of EMI filter from simulation results. Fig. 3-42(a) gives one CM bare noise example without the insertion of EMI filter in the simulation, and the corner frequency at this case is calculated with an attenuation slope of 40 dBuA/dec based on the required attenuation in Fig. 3-42(b).

There is a sequence for getting corner frequencies for the DM and CM EMI filters. The first step is to get DM bare noise only with dc-link capacitors in simulation, then to calculate the corner frequency of DM filter. With the insertion of DM filter in the simulation, CM bare noise is obtained to further calculate the corner frequency of the CM filter.

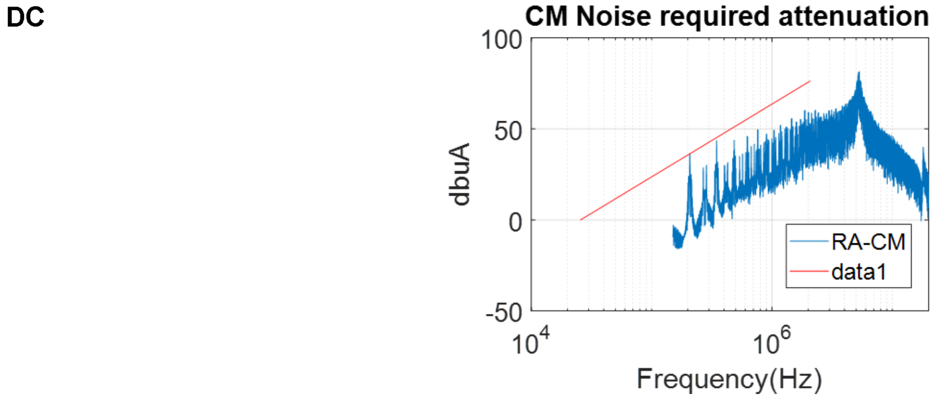

LISN
LISN
L_{cm}
L_{dm}
C_{cm}
C_{dm}
Motor

(a) EMI filter configuration in two-level VSC


LISN
LISN
LISN
L_{cm}
L_{dm}
C_{dm}
C_{cm}
C_{dm}
C_{cm}
C_{cm}
Motor

(b) EMI filter configuration in three-level VSC

Fig. 3-41. Two EMI configurations in this project.



(a) (b)

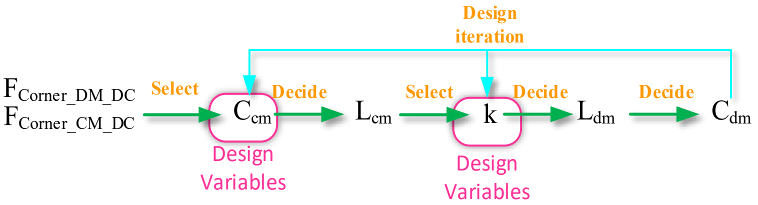
Fig. 3-42. Corner frequency calculation based on bare noise, (a) dc side CM bare noise, (b) corner frequency determination based on required attenuation.

3.7.2 Design Iteration of EMI Filters

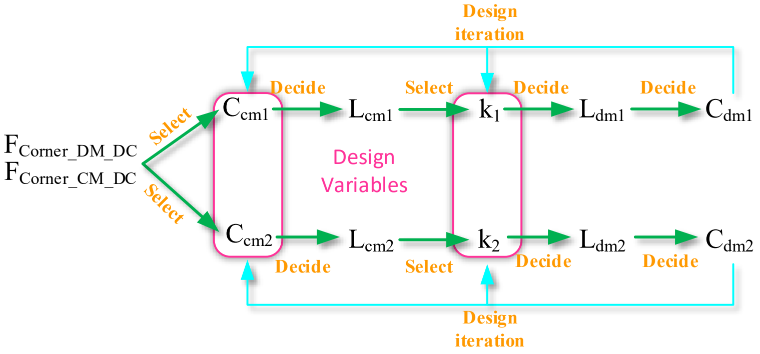
Like *dv/dt* filter, after getting the corner frequencies of DM and CM EMI filters, it is usually to select LC values with some experience-based trial and error procedure, which is neither scientific nor efficient. Also, a design coupling exists between the selection of CM inductance and DM inductance. Larger CM inductance also creates a larger leakage inductance, helping to reduce the required DM inductance or even to eliminate DM inductors. Vice versa, larger DM inductance can also help reduce the required CM inductance. In addition, similar to *dv/dt* filter, for a fixed corner frequency, the distribution L and C can lead to different amplitudes of inductor current ripples, introducing the other trade-off between the inductance value and the amplitude of the inductor current ripple for the inductor weight optimization.

To get an optimal design for the design coupling and LC value determination, a new design variable defined as the inductance ratio k between DM inductance and CM inductance is introduced. Then, with DM and CM corner frequencies, only two free design variables can be manipulated to achieve the lowest weight for the single-stage EMI filter while four free design variables are used for the two-stage EMI filter. As shown in Fig. 3-43(a), C_{cm} and k are two free design variables in the single-stage EMI filter design, and once these two variables are selected, the left variables in EMI filter design are confirmed with the known corner frequencies of EMI filters. For the two-stage EMI filter design, from Fig. 3-43(b), C_{cm1}, C_{cm2}, k_1 and k_2 are four free design variables to determine the remaining parameters.

The searching space or design space of design variables C_{cm} and k must be confined to exclude infeasible solutions and to limit the searching efforts. The maximum value of C_{cm} is set based on the leakage current limitation or reasonable value, and the maximum value of C_{dm} is set based on the reactive power limitation. Then k can be defined with a selected C_{cm_select}:


Design
iteration
F_Corner_DM_DC
F_Corner_CM_DC
Select
Ccm
Decide
Lcm
Select
k
Decide
Ldm
Decide
Cdm
Design
Variables
Design
Variables

(a) Single stage EMI filter iteration and decision variables


Design
iteration
F_Corner_DM_DC
F_Corner_CM_DC
Select
Select
Ccm1
Decide
Lcm1
Select
k1
Decide
Ldm1
Decide
Cdm1
Design
Variables
Ccm2
Decide
Lcm2
Select
k2
Decide
Ldm2
Decide
Cdm2
Design
iteration

(b) Two stage EMI filter iteration and decision variables

Fig. 3-43. Design iteration of dc side EMI filter design.

$$k = N_{\min} + N_{scale} = \frac{L_{dm\_\min}}{L_{cm}} + N_{scale} = \frac{1/(4\pi^2 C_{dm\_\max} f_{dm})}{1/(4\pi^2 C_{cm\_select} f_{cm})} + N_{scale} \tag{3.39}$$

where N_{min} is the minimum inductance ratio, which is calculated by a division of the minimum DM inductance over the CM inductance with the selected C_{cm_select}. N_{scale} is scaling factor is defined from 0 to 100 used for varying the DM inductance.

3.7.3 Design Optimization Algorithm Selection and Improvement

With the defined design space, in order to improve the searching efficiency, some possible optimization algorithms can be applied. For this case, since the calculation of the inductor weight (objective) involves a group of strong non-linear and nondifferentiable equations, gradient-based or Lagrange multiplier based methods cannot be used while evolutionary algorithms are considered in this dissertation, including PSO and GA algorithm.

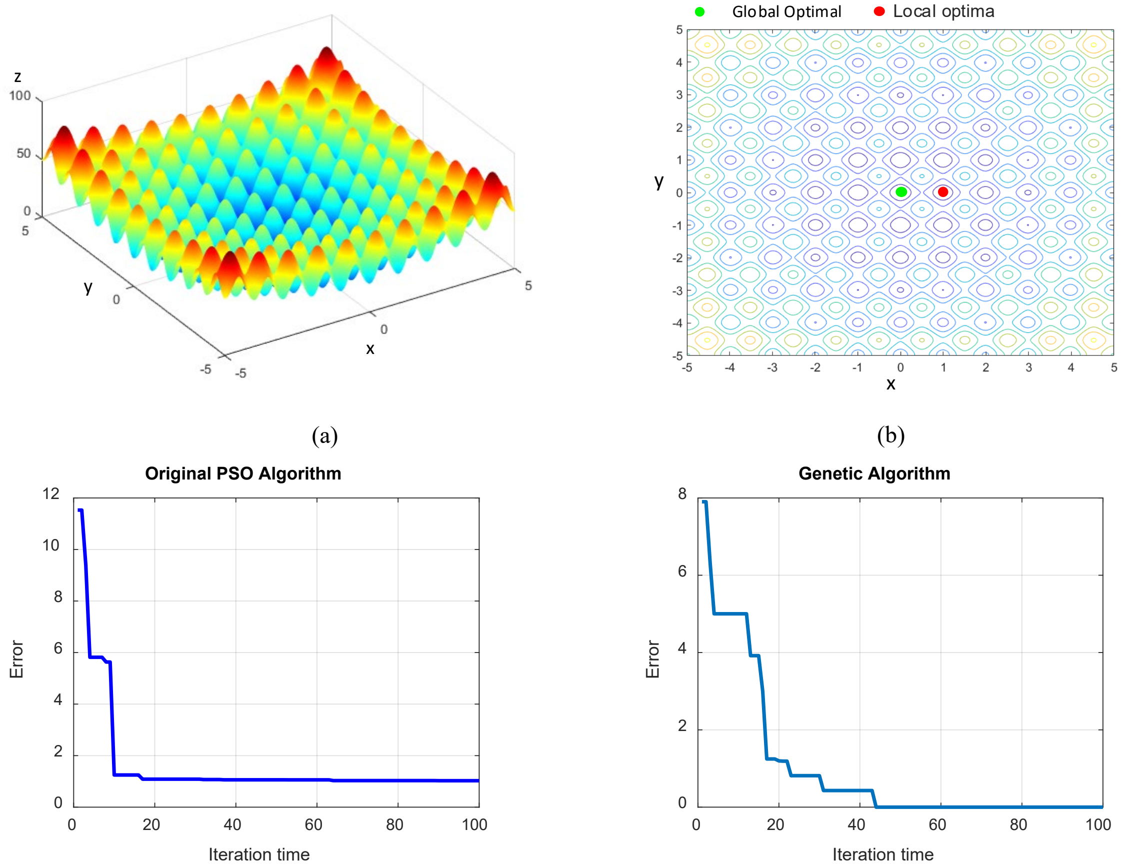
The convergence speed and global searching performance of PSO and GA are discussed in section 2.3.1. To further validate and compare the optimization algorithms, two algorithms are tested with Rastrigin function with a strong non-linearity.

The following gives the Rastrigin function:

$$\mathrm{y} = 20 + x_1^2 + x_2^2 - 10(\cos 2\pi x_1 + \cos 2\pi x_2) \tag{3.40}$$

The 3-D plot of Eq. (3.40) is given in Fig. 3-44(a), showing the strong non-linearity which could be similar to the filter weight function with design variables. Fig. 3-44(b) further gives a contour plot in the x-y plane. For population-based algorithms, one issue is the selection of initial group values, which can affect optimization results greatly. Fig. 3-44(c) shows one optimization iteration process with PSO, the searching is trapped in a sub-optimal point showing as a red point in Fig. 3-44(b). Fig. 3-44(d) shows the same optimization iteration process with the same initial group values but with GA, and the algorithm gets out of the trapped point to arrive at the global optimal point. However, PSO has a much faster convergence speed than GA, which is also very important since the one complete iteration for the EMI filter design with the simulations, complicated models, and physical design calculations are long. It can cost 6 minutes for one iteration in this case.

In order to have both fast convergence speed in PSO and good convergence ability in GA, an improved PSO algorithm with the mutation terms based on [143] and constriction factor based on [144] is applied. The mutation terms are the same as the procedure in GA, expanding the diversity of the populations and avoiding trapping in a local optimal. Moreover, based on Clerc's research [145], the use of a constriction factor could be necessary to ensure the convergence of PSO. Combined with two techniques in the literature, the improved PSO is also tested with



(a) (b)

(c) (d)

Fig. 3-44. Verification of PSO and GA algorithm with a strong non-linear function: (a) plot of the non-linear function with two variables, (b) contour plot of x-y plane, (c) iteration convergence with PSO, (d) iteration convergence with GA.

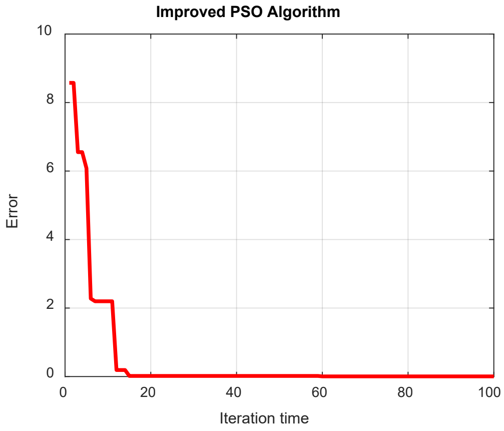


Fig. 3-45. Verification of the improved PSO algorithm.

Rastrigin function. The performance of the algorithm is shown in Fig. 3-45. Compared with the results in Fig. 3-44(c-d), the improved PSO algorithm has a faster convergence speed than GA but with the same convergence ability.

The improved PSO algorithm consists of the velocity and position iteration:

$$\begin{aligned} v_i(k+1) &= v_i\left(k\right) + c_1\gamma_{1i}(p_i - x_i(k)) + c_2\gamma_{2i}(G - x_i(k)) \\ x_i(k+1) &= x_i(k) + c_3 v_i(k+1) \end{aligned} \tag{3.41}$$

where i is the particle index, k is the discrete time index, v is the velocity of i_{th} particle and x is the position of i_{th} particle, p_i is the best position found by i_{th} particle, which is also called personal best, and G is the best position found by the swarm, which is also called global best. γ_{1i} and γ_{2i} are the random numbers on the interval 0 from 1 applied to i_{th} particle, c_1 and c_2 are the learning factors, c_3 is the constriction factor.

Compared with the original PSO, the improved PSO has an extra constriction factor c_3 and no weighting factor in $v_i(k)$ term. Also, a mutation mechanism is added to diverse the population as:

$$\begin{aligned} & p, q = rand(1) \\ & if\ \ p > 0.8\ \&\&\ q > 0.8 \\ & m = rani([1, sizepop]) \\ & x_1(m) = rand(1) \times 0.4 \\ & x_2(m) = rand(1) \times 0.85 + 10 \end{aligned} \tag{3.42}$$

where p and q are the random numbers between 0 and 1, m is a random integer between 1 and the size of the population, $x_i(m)$ is the i_{th} variable value of the m_{th} individual.

3.8 Summary

Two non-linear physics characteristics of magnetic core inductors are identified. First, for powder and amorphous cores, the current-bias dependent permeability can cause time-varying instantaneous inductance at different current levels. As a result, for an ac 3-phase system, the DM inductors at different phases leads to the different instantaneous DM inductances, introducing the unbalanced DM impedance and converting some DM noise to non-intrinsic CM noise at high frequency range. To predict CM and DM noise more accurately for EMI filters design, a time-varying inductor model is proposed and the impacts of unbalanced DM impedance on noise behavior are also studied. Second, for nanocrystalline cores, the impacts of the frequency-dependent permeability are investigated. The real permeability of nanocrystalline cores drops quickly starting from 40 kHz while the imaginary permeability becomes dominant at high frequency to provide the impedance for the high frequency noise attenuation. An impedance-based design approach considering both real permeability and imaginary permeability below 2 MHz to obtain a more accurate design result.

The conventional maximum magnetic flux density model for CM inductors by using the peak current and constant permeability is not accurate enough compared with the voltage derived flux density from experiments, especially for the CM current including rich harmonics. To improve the accuracy, a new model with FFT analysis considering each harmonic and its corresponding permeability from the frequency-dependent permeability model is proposed. Based on the testing results, the proposed model can reduce the error of the maximum magnetic flux density estimation from 24.8% to 8.3%.

The leakage inductance model is critical for the core loss calculation and core saturation estimation. However, the conventional leakage inductance model cannot achieve high accuracy with the relatively high turns number since the assumption of the leakage magnetic field is not correct at the high turns number. To solve this issue, a new leakage model is proposed based on the analogy between the reluctance and capacitance, and the proposed model can much reduce the error at the high turns number case. The 3D FEM simulation verifies the proposed model can reduce 25%~30% errors compared with Nave's model at large turns number.

Except for modeling improvements in the design of filters, two optimization approaches are proposed. In order to solve the inductor weight trade-off between the inductance and current ripple peak value, the A_p prediction for filters weight is applied for the ac side *dv/dt* filter design. In addition, to solve the design trade-off between DM and CM inductance, an inductance ratio between DM and CM inductance is introduced as the design variable in EMI filters design. PSO and GA are compared and tested in terms of convergence speed and convergence ability. At final, an improved PSO with the mutation terms and constriction factor is adopted to help search the global optimal for EMI filters design more efficiently.

Chapter Four

Device Selection Optimization Considering Switching Speed Limitation and Power-loop Layout

In the conventional power electronics design, the selection of power semiconductors mainly considers the power loss, operation frequency capability, and the impacts on cooling design. However, in the paper design stage, the switching speed is not carefully considered or optimized since no power-loop layout or busbar design would be conducted in the paper design stage. The most common design procedure is to finalize PCB design or busbar design when the paper design is finished. Then, with the implemented hardware, the gate resistance (switching speed) will be adjusted with a way of trial-and-error based on the overvoltage suppression and cooling performance. In such a design method, it always exists a gap between the predicted performance and the real converter performance.

To shrink the gap between the design and implementations, a new device selection optimization considering switching speed limitation and power-loop layout is proposed in this chapter. The discrete-time modeling of switching behavior is applied to predict the switching behavior and switching speed. An automatic layout creation with the selected device package is proposed with an open source geometry description scripting language, and the parasitic inductance of the power loop can be numerically modeled and extracted with partial element equivalent circuits (PEEC) method. With these advanced models, design automation incorporated with the device database is presented in the paper design stage to determine the power semiconductor and the optimized gate resistance (switching speed) to realize both the lowest weight and the overvoltage containment.

4.1 SiC MOSFETs Switching Behavior Model

4.1.1 Discrete-time Modeling of Switching Behavior

The switching behavior model of power semiconductors is well studied in previous research. Here, a discrete-time modeling method with state-space matrices are applied, which is similar to the work in the literature [13, 18]. The turn-on and turn-off processes are divided into four intervals with the corresponding state-transition matrix [13]. If the state-transition matrix at each subinterval can be inverted, the basic equation for discrete-time modeling method is given as:

$$x_{(n+1)} = \left(\prod_{i=1}^{M} e^{A_i t_i} \right) x_{(n)} + \sum_{i=1}^{M} \left(\left(\prod_{j=1}^{M} e^{A_j t_j} \right) (e^{A_i t_i} - I) A_i^{-1} B_i \right) \tag{4.1}$$

where t_i is the duration time for i_{th} interval shown in Fig. 4-1, A_i and B_i are the state-transition and input matrix for i_{th} interval, $x_{(n+1)}$ is the state vector in $(n+1)_{th}$ discrete time step, and $x_{(n)}$ is the state vector in n_{th} discrete time step.

Fig. 4-1 shows the illustration of the discrete-time modeling procedure, and device switching behavior can be split into several modes, and, in each mode, the power semiconductor is modeled with an equivalent circuit. The detailed mode analysis and state-transition matrices derivation can be found in the literature [13].

Compared with previous modeling work, this dissertation tries to incorporate more non-linear parameters of devices with less fitting efforts. For non-linear parasitic capacitances, a Python-based automatic curve extraction tool is developed with an open-source computer vision library (OpenCV) and optical character recognition library Python-tesseract. As shown in Fig. 4-2, the

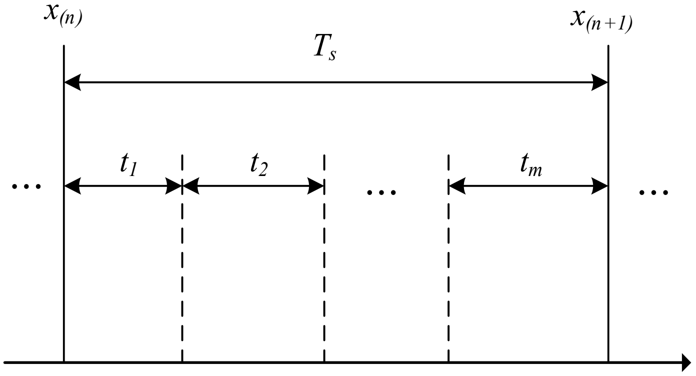
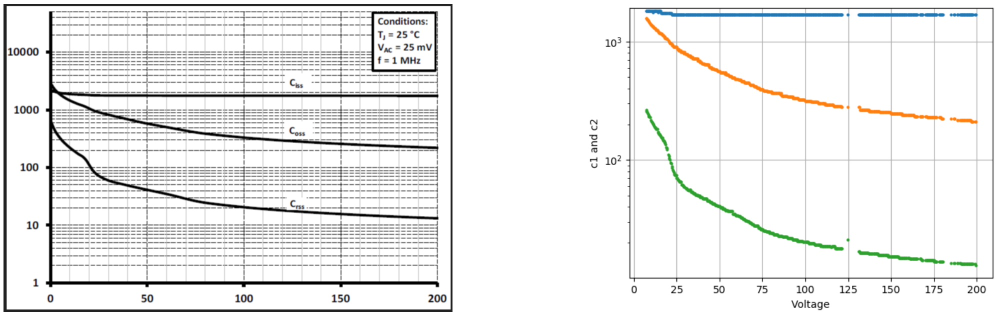


Fig. 4-1. The illustration of M modes in one switching cycle for discrete-time modeling

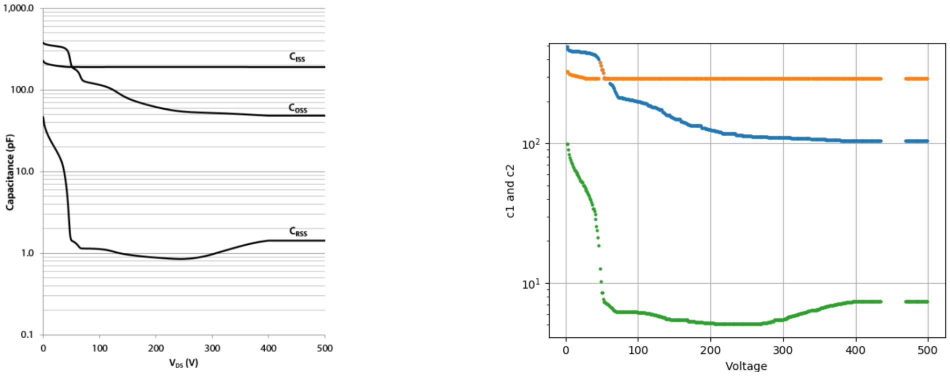
developed tool can automatically extract all black curves from the figure in the datasheet, helping reduce many manual efforts to obtain the raw data from the datasheet. Also, the extracted data is stored as the matrix form in a .txt file, which can be easily read by MATLAB and the linear interpretation is used to establish the fitting function in MATLAB.

Furthermore, the impacts of junction temperature on the switching behavior are considered. First, the transconductance g_m is a function of the junction temperature T_j and the voltage difference (v_{gs}-V_{th}), and the transconductance curves can be obtained from the transfer characteristic curves in Fig. 4-3(a), and the fourth-order polynomial equation is used to fit the transconductance curves as a function of the junction temperature and the voltage difference. The fitting results are shown in Fig. 4-3(b). Second, the threshold voltage V_{th} is also a function of the junction temperature which impacts the switching behavior. A linear interpretation method is used for curve fitting shown in Fig. 4-4. With those fitting functions, the variations of transconductance and threshold voltage with temperature are added to the discrete-time modeling for higher accuracy.



(a) Capacitance curves example #1

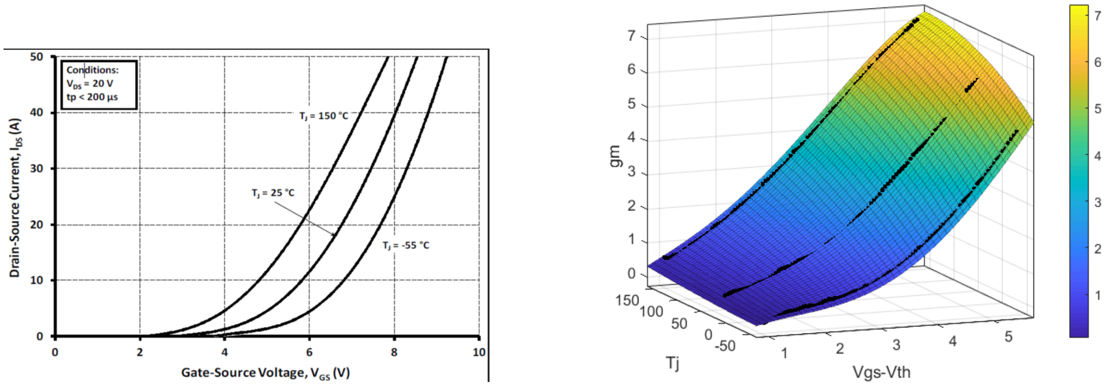
(b) Extracted curves for example #1



(c) Capacitance curves example #2

(d) Extracted curves for example #2

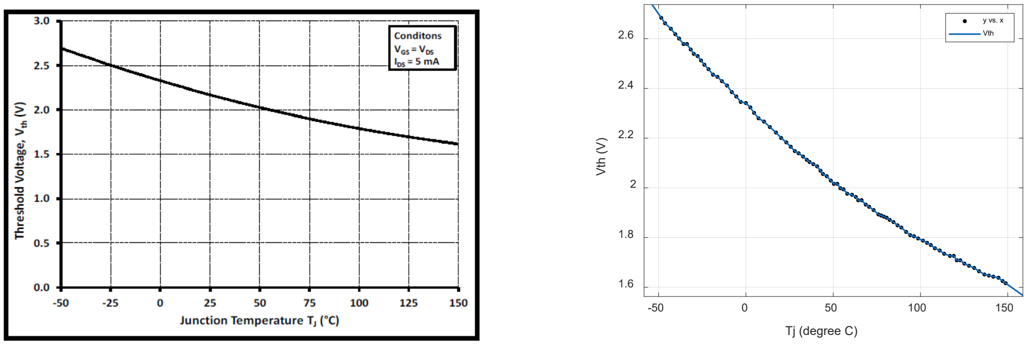
Fig. 4-2. Automatic extraction of capacitance curves.



(a) Example of transfer characteristics at different temperatures

(b) Curve fitting of transconductance

Fig. 4-3. Curve fitting results of transconductance as a function of junction temperature



(a) Example of threshold voltage at different temperatures (b) Curve fitting of threshold voltage

Fig. 4-4. Curve fitting results of threshold voltage as a function of junction temperature.

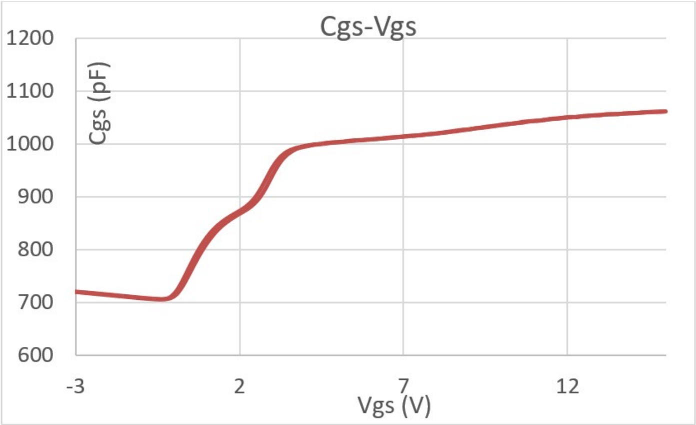


Fig. 4-5. The characterization results of C_{gs} as a function of v_{gs}.

Moreover, based on the literature [19], the non-linear characteristic of C_{gs} as a function of v_{gs} should also be considered. However, generally, the characteristic of C_{gs} with v_{gs} is not given in the datasheet, requiring extra efforts to characterize C_{gs} curve with a curve tracer. Fig. 4-5 shows one measuring example through the curve tracer, and the fitting function is established for the discrete-time modeling.

4.1.2 Switching Speed Prediction and Verification

First, to validate the developed model, a Saber MOSFET model with the built-in curve fitting tool is applied and compared. A switching waveform comparison between the developed model and Saber model is compared in Fig. 4-6. Since the Saber model did not cover the C_{gs}-v_{gs} characteristics shown in Fig. 4-5, the developed model also excluded the C_{gs}-v_{gs} characteristics for a fair comparison. As shown in Fig. 4-6, with the same parameters of the gate drive and circuits parasitics, the developed model shows a good consistency compared with the simulation model, validating the correctness of the developed model.

Second, in order to compare the developed model with real switching behavior performance, a DPT is conducted with the SiC MOSFET C3M0065090J with a D^{2}park package, and the prototype is shown in Fig. 4-7. With testing results, two cases with the different gate resistances are used for the comparison and study. For a fair comparison, the developed switching model applies the same parasitics of the DPT board and the same gate drive parameters.

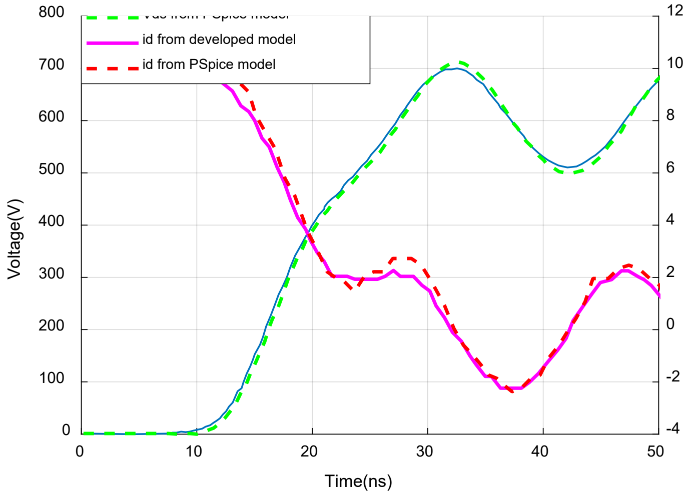


Fig. 4-6. Waveform comparison between the developed model and PSpice model.

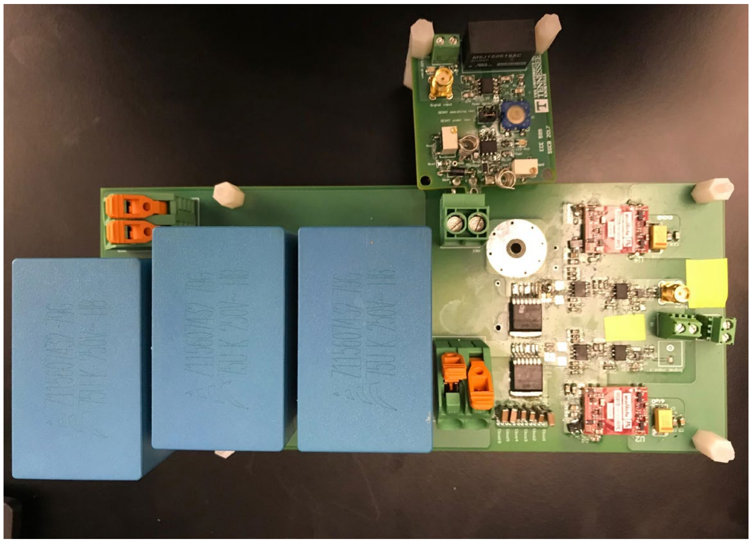
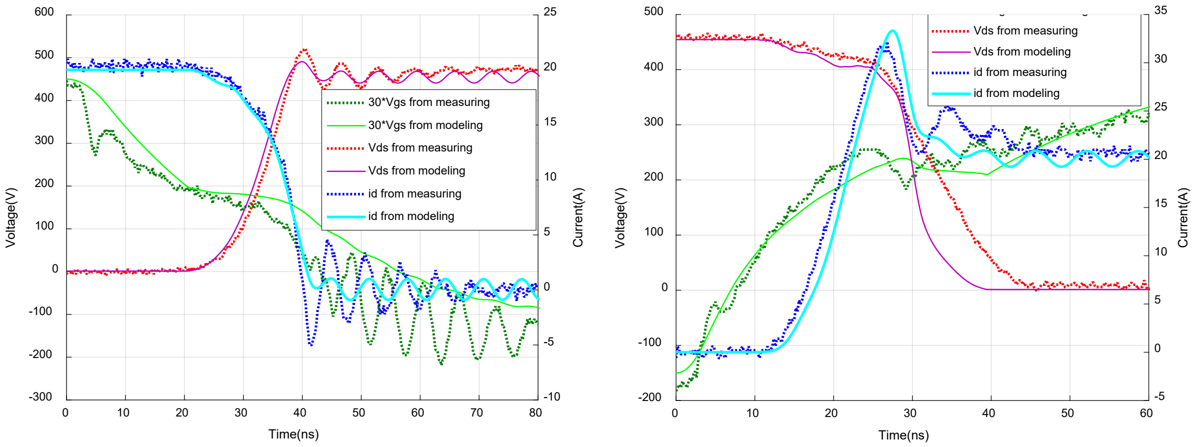
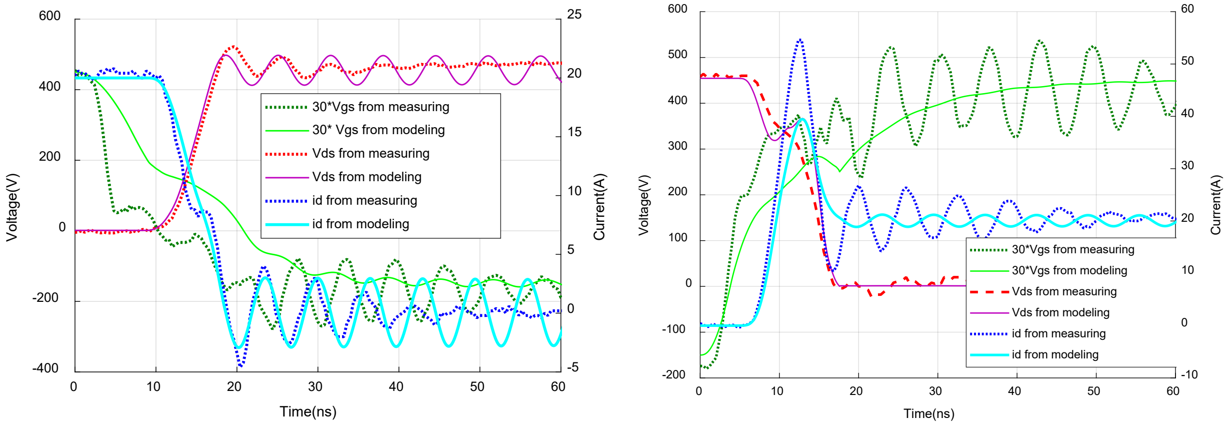


Fig. 4-7. Prototype of DPT platform for SiC MOSFET C3M0065090J.

Thus, a waveform comparison was conducted at the testing condition of 450 V dc-link and 20 A load current. In Fig. 4-8, turn-on and turn-off waveforms are compared when the gate resistances are 20 Ω and 2.5 Ω respectively. For turn-off waveforms comparison, from Fig. 4-8(a) and (c), the waveforms of v_{ds} and i_d from the developed model match the testing waveforms well no matter what the gate resistance is used, but the v_{gs} modeling waveforms have some discrepancies compared with testing waveforms. The possible reason is the measured v_{gs} waveform is not a real v_{gs} waveform due to the parasitics of interconnection and wire bonding compared with the developed model. For turn-on waveforms comparison, from Fig. 4-8(b), the i_d waveforms are close but the v_{ds} waveforms have the obvious discrepancy when the gate resistance is 20 Ω. However, when the gate resistance changes to 2.5 Ω, the discrepancy of v_{ds} waveforms becomes smaller but the resonant amplitudes of i_d waveforms have an obvious difference. The possible reason is the gate drive of the high-side switch is not modeled, and the switch current contributing by the cross-talk is not modeled and included.



(a) Turn-off waveforms comparison @ *Rg*=20 Ω (b) Turn-on waveforms comparison @ R_g=20 Ω



(c) Turn-off waveforms comparison @ *Rg*=2.5 Ω (d) Turn-on waveforms comparison @ *Rg*=2.5 Ω

Fig. 4-8. Waveform comparison at the testing condition of 450 V and 20 A with different gate resistances.

Table 4-1 further gives some key parameter comparison between the predicted results and the testing results. In terms of switching speed prediction, the errors of predicted results are acceptable to evaluate the overvoltage or *dv/dt*, *di/dt* value. The overvoltage estimation error is within 5%, and the error of *dv/dt* and *di/dt* is below 15%. However, for the switching loss estimation, especially for turn-on with a 20 Ω gate resistance, the error can be up to 25.3%.

Table 4-1. Key parameter comparison between the predicted results and the testing results.

Parameters	***2.5* Ω**		***20* Ω**	
	Measured	Predicted	Measured	Predicted
Dv/dt during turn-on	115 V/ns	134.1 V/ns	68.1 V/ns	85.4 V/ns
Di/dt during turn-off	3.89 A/ns	3.66 A/ns	2.62 A/ns	2.48 A/ns
V_{dsmax}	522 V	497.6 V	512 V	487.3 V
E_{off}	13.4 uJ	14.83 uJ	39 uJ	41.7 uJ
E_{on}	80.7 uJ	72.8 uJ	165.5 uJ	122.7 uJ

Since the switching speed and overvoltage prediction are the main objectives here, even though the developed model cannot achieve very high accuracy of the switching loss prediction, it is still good enough to use the developed model to estimate the switching speed and select the proper gate resistance.

4.2 Busbar Model

For high power applications, the busbar is more common to adopt as the connecting bridge for in and out cables, dc-link capacitors and power semiconductors instead of PCB. In this section, the thermal model and thickness determination procedure of the busbar are developed.

4.2.1 Thermal Model

Busbar can be modeled as an isothermal plate with natural convection. The effects of thermal radiation are neglected in the derivation of the thermal resistance of the busbar. Based on heat transfer theory, a relationship between the heat transfer coefficient and the power loss is established as:

$$P_{loss} = h_c A_{eff} T_{diff} \tag{4.2}$$

where h_c is the heat transfer coefficient of the busbar, A_{eff} is the effective area for natural convection, T_{diff} is the temperature difference between the ambient and busbar.

Heat transfer coefficient of natural convection can be calculated as:

$$h_c = \frac{Nu \cdot \lambda_{air}}{L} \tag{4.3}$$

where Nu is the Nusselt number, λ_{air} is the thermal conductivity of air, L is the length of the isothermal plate.

Since busbar is modeled as an isothermal plate, the Nusselt number can be found from:

$$\begin{cases} Nu = 0.54 Ra^{1/4} \\ Ra = Gr\,\mathrm{Pr} = \dfrac{g\beta T_{diff}\delta^3}{v^2}\mathrm{Pr} \\ \beta = 3.25\times10^{-3}\ \mathrm{K}^{-1} \\ v = 16.5\times10^{-6}\ \mathrm{m}^2/s \\ g = 9.8\ \mathrm{m}/s^2 \\ \mathrm{Pr} = 0.7 \end{cases} \tag{4.4}$$

where g is the gravitational acceleration, β is the coefficient of volume expansion, δ is the characteristic length of the geometry, v is the kinematic viscosity of a fluid, Gr is Grashof number and Pr is Prandtl number.

Combined with Eq. 2.12 to Eq. 2.14, the thermal resistance of busbar at natural convection is derived as:

$$R_{b-air} = \frac{T_{diff}}{P_{loss}} = \frac{1}{h_c A_{eff}} = \frac{L}{(\frac{g\beta T_{diff}\delta^3}{v^2}\mathrm{Pr})^{\frac{1}{4}} \lambda_{air} A_{eff}} \tag{4.5}$$

4.2.2 Thickness Determination

Compared with the conventional design procedure for power electronics converters, the geometry of a busbar or power loop layout will be automatically created based on the topology and the device package in this dissertation, which will be presented in Section 4.3. Here, it is assumed that the geometry is confirmed in the design iteration, and the remaining task is how to determine the optimal thickness to achieve the lowest weight within the limited temperature rise. Also, the material of the busbar is assumed as aluminum whose weight density is 2.7 g/cm^3.

The thickness of a busbar is determined by the temperature rise. With the thermal resistance of a busbar, the allowed power loss can be calculated. Assuming that the ac components of the dc-link current are provided by the dc-link capacitor bank, an FFT analysis is conducted and the skin depth at each harmonic is calculated. Thus, the loss can be obtained by summing up the loss induced by each harmonic.

In addition, the electric conductivity of aluminum is corrected considering the temperature impact. The whole design iteration of the busbar thickness is shown in Fig. 4-9. The thickness of a busbar is adjusted based on the temperature rise, and the minimum thickness is obtained when the temperature rise falls into the targeted range.

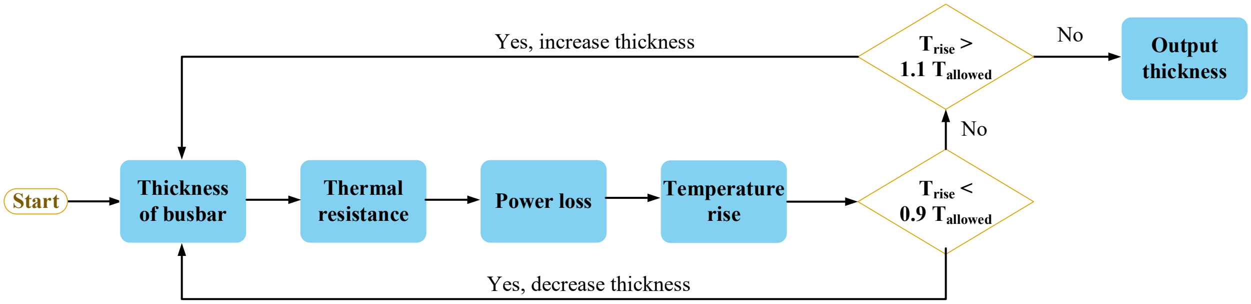

Yes, increase thickness
$T_{rise} >$ 1.1 $T_{allowed}$
No
Output thickness
No
Start
Thickness of busbar
Thermal resistance
Power loss
Temperature rise
$T_{rise} <$ 0.9 $T_{allowed}$
Yes, decrease thickness

Fig. 4-9. Design iteration for busbar thickness selection.

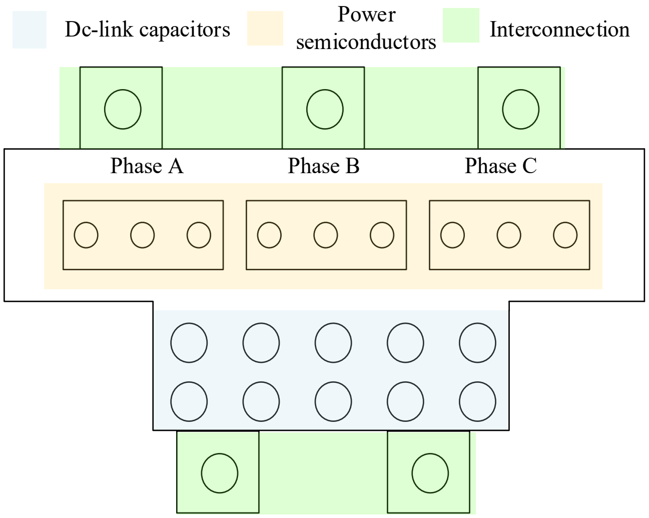
4.3 Numerical Modeling of Power-loop Inductance with PEEC

Generally, the detailed geometry of a busbar is designed and implemented after the selection of power devices. However, it may cause a trial-and-error process in the testing since the gate resistance or switching speed is not selected and considered based on the geometry limitation. To improve the design procedure and reduce the trial-and-error, automatic creation of the geometry based on the topology and the device package is developed during the device selection iterations. Also, the PEEC algorithm is applied to extract the parasitic inductance for the automatically created geometry for busbars or power loop layouts.

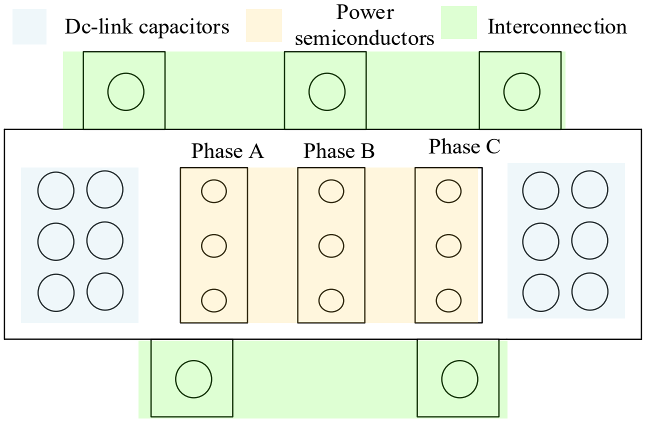
4.3.1 Automated Creation of Busbar and Power-loop Layout

Since the device selection iteration includes plenty of power devices in the device database, it is very time-consuming and unrealistic to manually draw the layouts and the busbar structures based on the topology and the device package. To realize the design automation, automated creation of the geometry for busbars and power-loop layouts is proposed.

In most cases, geometry structures in busbar design and PCB layout are not complex. They are made of traces, holes, and planes. Moreover, a general rule of magnetic field cancellation is followed to design the busbar structure and PCB layout. Specifically, for a busbar, a laminated structure with the overlap of the positive and negative busbar is applied. For PCB layouts, a vertical power loop in two adjacent layers is adopted to reduce the parasitic inductance. Also, to decrease the commutation loop area, the dc-link capacitors or the decoupling capacitors should be placed close to the power semiconductors. With such rules, the basic geometry of busbars and PCB layouts and components arrangement for different topologies can be predefined, and the dc-link capacitors and power devices will be fitted into the geometry design based on the dimensions and


Dc-link capacitors
Power semiconductors
Interconnection
Phase A
Phase B
Phase C

(a) Layout scheme #1


Dc-link capacitors
Power semiconductors
Interconnection
Phase A
Phase B
Phase C

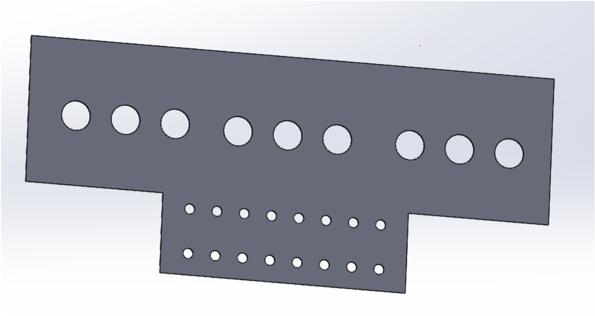
(b) Layout scheme #2

Fig. 4-10. One example of predefined two-level voltage source inverter layouts.

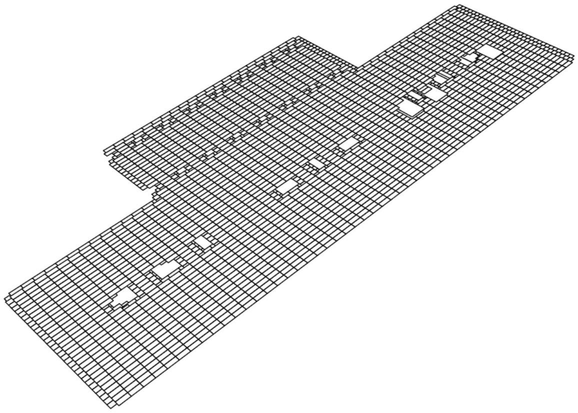
the packages. One example of the predefined geometry of a two-level converter is given in Fig. 4-10, and two layout schemes are available for the selection considering the device and capacitors dimensions and packages.

Also, in order to automatically create the predefined geometries with the selected devices and capacitors, an open-source geometry description scripting language originally developed by Mattan Kamon at M.I.T. is chosen [146]. It was developed for describing the geometries in interconnect problems for IC package design. In this scripting language, all geometries are defined in an x-y-z coordinate and it can easily define holes, traces and planes, which is good enough to describe the geometries in power electronics design. Moreover, an automatic script generation function is developed in MATLAB to create the geometry script file for the parasitics extraction. The required inputs of the automatic script generation are the dimension information of the selected power device and dc-link capacitor, operating frequency, the thickness of the busbar and insulation material thickness.

One automatic geometry creation example of the two-level VSC is given in Fig. 4-11 with the SiC power module CAS120M12BM2 from Wolfspeed and dc-link B25620B1197K983 from EPCOS. The busbar design with manual drawing in SolidWorks based on the predefined structure in Fig. 4-10(a) is shown in Fig. 4-11(a) while the automatically created geometry with the geometry description scripting language is given in Fig. 4-11(b). The holes in Fig. 4-11(b) have low display resolution because of the low number of segments, and the developed visualization program cannot handle the display with a large number of segments due to heavy memory utilization. However, it will not be an issue for the parasitics extractions since no visualization is needed during the calculation of the PEEC algorithm.



(a) Manually draw by SolidWorks



(b) Same geometry created by the automated function

Fig. 4-11. Example of automatically created geometry with geometry description script language.

4.3.2 Numerical Techniques Comparison for Solving Field Problems

Finite element methods (FEM), the method of moments (MoM), PEEC, finite difference methods (FDM) are the most popular numerical techniques to solve the field problems. The main difference is four numerical methods apply different mathematical approaches to solve Maxwell's equations, and hence, render one numerical method preferable for a specific problem compared with others. From the point of the formulation of Maxwell's equations, the above numerical methods can be classified by using the differential form and integral form to numerically solve the field problems.

Table 4-2. Main futures of four numerical methods for field problems.

Method	**FEM**	**MOM**	**FDM**	**PEEC**
Formulation	Differential	Integral	Differential	Integral
Solution variables	Field	Circuit	Field	Circuit
Cell geometries	Nonorthogonal	Nonorthogonal	Orthogonal	Nonorthogonal
Solution domain	All can be applied for frequency and time domains			

The numerical methods with the differential formulation required to discretize the whole geometry structure including the air while the numerical methods with the integral formulation only need to discretize the materials. It implies that the differential approaches demand a larger number of cells and heavier computation burden compared with the integral formulation based approaches. Also, the solution variables from the differential formulation based approaches and integral formulation based approaches are different. The field variables like $\vec{E}$ and $\vec{B}$ can be obtained for the numerical methods with the differential formulation, but the circuit variables like currents and voltages need post-processing. Nonetheless, the circuits variables like currents and voltages can be delivered for the numerical methods with the integral formulation, but field variables need post-processing. Furthermore, Table 4-2 gives the main features of the most popular numerical methods for field problems based on the literature [147].

In this dissertation, the objective is to estimate the parasitic inductance of a specific busbar design or power loop layout. Hence, it is not necessary to know the magnetic or electric field distribution. The inductance calculation in FEM and FDM needs extra post-processing efforts either by energy or flux linkage calculations. Also, most commercially available FEM software is very heavy and bulky including too many features and functions not needed for this application and an extra interface is required for communication between the MATLAB and FEM software. PEEC is a perfect numerical modeling method for this application since fewer computation efforts without the discretization of air and post-processing are required. Also, a well-developed open source PEEC algorithm [148] enabling modifications and customizations is available to adaptive to this application.

4.3.3 Parasitic Inductance Calculation with PEEC

A. Principle of PEEC

Based on Maxwell's equations, the total electric field in free space can be expressed as:

$$\vec{E}^t(\vec{r},t) = \vec{E}^i(\vec{r},t) - \frac{\partial \vec{A}(\vec{r},t)}{\partial t} - \nabla \phi(\vec{r},t) \tag{4.6}$$

where $\overrightarrow{E^i}$ is the electric potential from an external electric field, $\vec{A}$ and ϕ are the magnetic vector potential and the electric scalar potential.

Based on the Gauss's law in Maxwell's equations, the derivation of $\overrightarrow{E^t}$ is:

$$\vec{E}^t(\vec{r},t) = \frac{\vec{J}(\vec{r},t)}{\sigma} \tag{4.7}$$

where $\vec{J}$ is the current density in a conductor and σ is the conductivity of the material.

Substituting Eq. (4.7) into Eq. (4.6), then a formula of the external applied electric potation is obtained as:

$$\vec{E}^i(\vec{r},t) = \frac{\vec{J}(\vec{r},t)}{\sigma} + \frac{\partial \vec{A}(\vec{r},t)}{\partial t} + \nabla \phi(\vec{r},t) \tag{4.8}$$

Applying with free space Green's function defined in [149], the form of electric field integral equation (EFIE) is derived as:

$$\begin{aligned}\hat{n}\times\vec{E}^{i}(\vec{r},t) &= \hat{n}\times\frac{\vec{J}(\vec{r},t)}{\sigma}\\ &+\hat{n}\times\left[\sum_{k=1}^{K}\mu\int_{v_k}G(\vec{r},\vec{r}')\frac{\partial\vec{J}(\vec{r}',t_d)}{\partial t}dv_k\right]\\ &+\hat{n}\times\left[\sum_{k=1}^{K}\mu\int_{v_k}G(\vec{r},\vec{r}')q(\vec{r}',t_d)dv_k\right]\end{aligned} \tag{4.9}$$

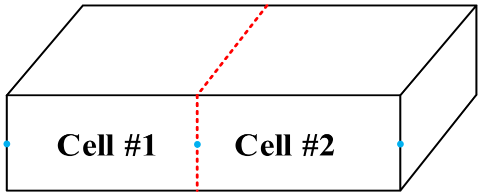
where v_k is the k_{th} volume cell, where $\vec{r}$ and $\vec{r'}$ are the observation and source point, the G is the green function, $\hat{n}$ is the surface normal to the body surfaces, t_d is the delay time the light travels from the observation point to the source point.

The interesting place is Eq. (4.9) can be interpreted as the KVL equation in the circuits theory, which is:

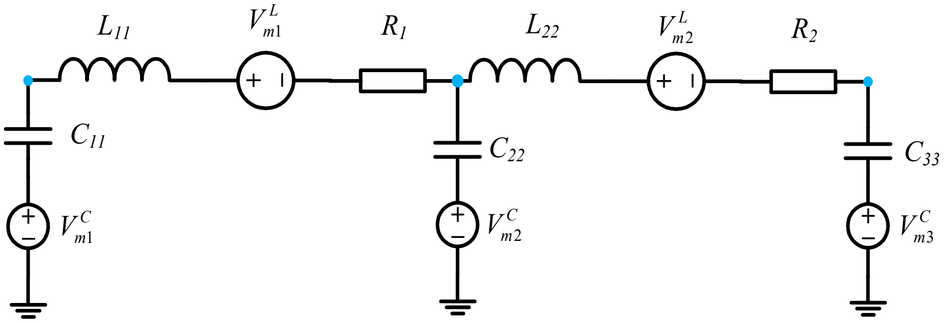
$$V_i = Ri + sLi + \frac{Q}{C} \tag{4.10}$$

where V_i is the externally applied voltage, R, L, C is the resistor, inductor and capacitor in the circuit, Q is the total charge of a capacitor in the circuit.

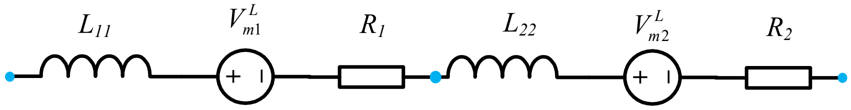
With such an analogy, the EFIE of Eq. (4.9) also can be interpreted as an equivalent circuit for a discretized volume cell, and one example is shown in Fig. 4-12 with two volumes cells for one conductor. Fig. 4-12(b) shows the full LCR PEEC model corresponding to three terms in Eq. (4.9), and V_{m1}^{L} and V_{m1}^{C} are the magnetic and capacitive coupling induced voltage drops from all other cells. In this application, the parasitic capacitance is not a concern, so the third term in Eq. (4.9) is neglected to reduce the computation burden. As a result, the PEEC model is simplified as the circuits shown in Fig. 4-12(c).



(a) Two volume cells example



(b) Full LCR PEEC model



(c) Simplified LR PEEC model

Fig. 4-12. Example of PEEC model for two volume cells.

Since the practical implementation of PEEC is not the focus of this dissertation, no detailed instructions will be given. The literature [149] and open-source code of PEEC [146] are a good reference for the practical implementations.

B. Impacts of Discretization on Modeling Accuracy

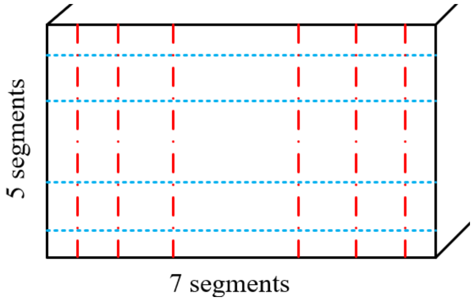
The precision and strategy of the discretization for geometries influence the accuracy of inductance calculations. In order to model non-uniform current distribution because of skin and proximity effects, two different strategies are used for the discretization of geometries. For traces, to consider edge effects due to the charge density distribution, an asymmetrical discretization method is applied for the height and width directions. As shown in Fig. 4-13(a), 5 and 7 segments are created in the height and width directions. Also, each segment has a different discretization precision and the ratio of discretization length between two adjacent segments is 2.

For planes, since the main non-uniform current distribution is in the thickness direction, the same asymmetrical discretization method is applied in the thickness direction. However, for width and length directions, the symmetrical discretization method is used as shown in Fig. 4-13(b) since the current distribution is more uniform than one in the thickness direction.

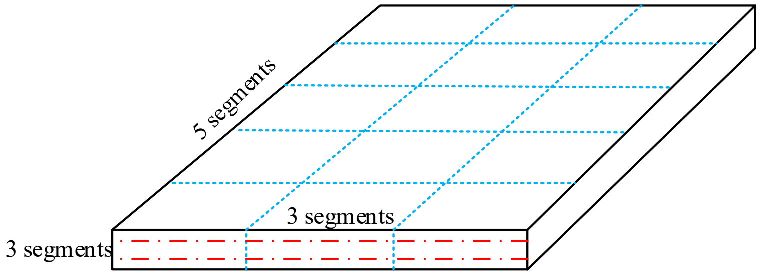
The resolution of the discretization with symmetrical and asymmetrical methods can be derived. For the symmetrical method, the resolution is easy to calculate as:

$$R_{sym} = \frac{L}{N_{Seg}} \tag{4.11}$$

where L is the length of one edge, N_{seg} is the number of segments.



(a) Discretization for traces



(b) Discretization for planes

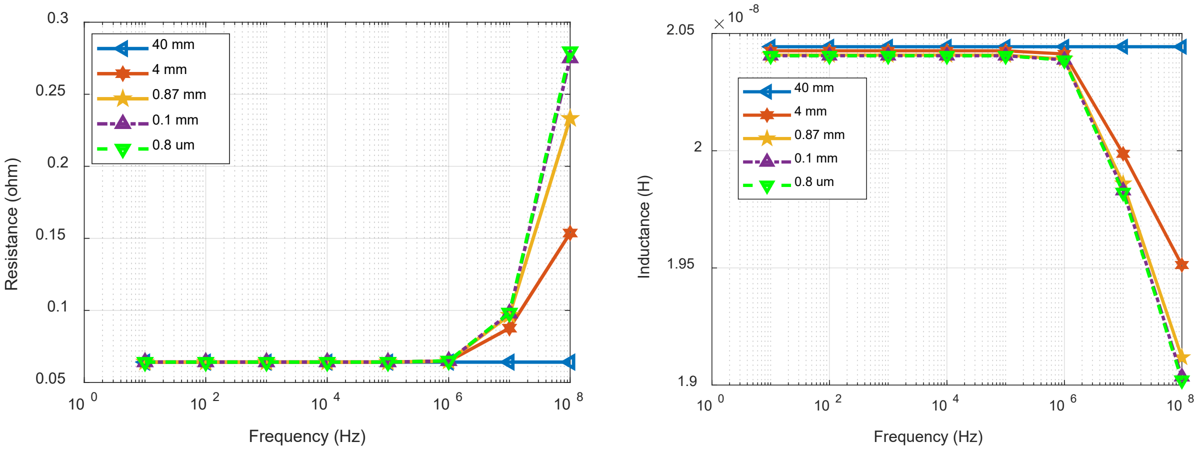
Fig. 4-13. Discretization schemes for different geometries.

For the asymmetrical method, the resolution is derived as:

$$R_{asy} = \frac{L}{\left(2^{\frac{N_{seg}-1}{2}} - 1\right) + \left(2^{\frac{N_{seg}-1}{2}-1} - 1\right)} = \frac{L}{2^{\frac{N_{seg}-1}{2}} + 2^{\frac{N_{seg}-3}{2}} - 2} \tag{4.12}$$

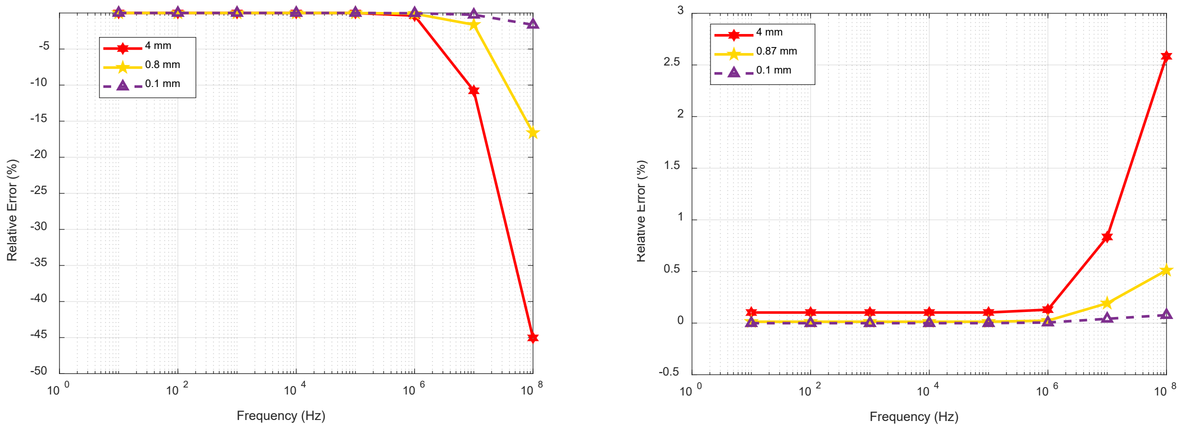
Compared with Eq. (4.11) and Eq. (4.12), with the same number of segments, the asymmetrical discretization method can achieve a much finer resolution than the symmetrical discretization method.

To investigate how the resolution of discretization impacts PEEC modeling accuracy, a case study for a copper trace ($L \times W \times H$: 40×8×3 mm) is carried out to calculate the resistance and inductance. Fig. 4-14 gives the calculation results of the resistance and inductance values as a function of frequency with different discretization resolutions. Since 0.8 μm is around one-tenth of the skin depth at 100 MHz, the results with 0.8 μm resolution are used as the referenced values for comparisons. From Fig. 4-14(a), the discretization resolution has an obvious impact on the accuracy of the resistance calculations, especially at high frequency range. As shown in Fig. 4-15(a), the relative errors can be up to 45% when the discretization resolution is 4 mm, and the reason is the discretization is not precise enough to reflect skin effects for the resistance modeling. The interesting part is the inductance modeling results. From Fig. 4-14(b), even though the discretization resolution varies from 0.8 μm to 40 mm, the final inductance values at different frequencies are still quite close. Based on Fig. 4-15(b), the maximum error is only 2.5 % even when the discretization resolution is 4 mm. This comparison implies the low discretization resolution can be applied if the accuracy of the resistance is not important, helping reduce the calculation time dramatically.



(a) Resistance value as a function of frequency (b) Inductance value as a function of frequency

Fig. 4-14. Impedance matrix as a function of frequency with different discretization resolutions.



(a) Resistance relative errors as a function of frequency (b) Inductance relative errors as a function of frequency

Fig. 4-15. Relative error as a function of frequency compared to 0.8 um discretization results.

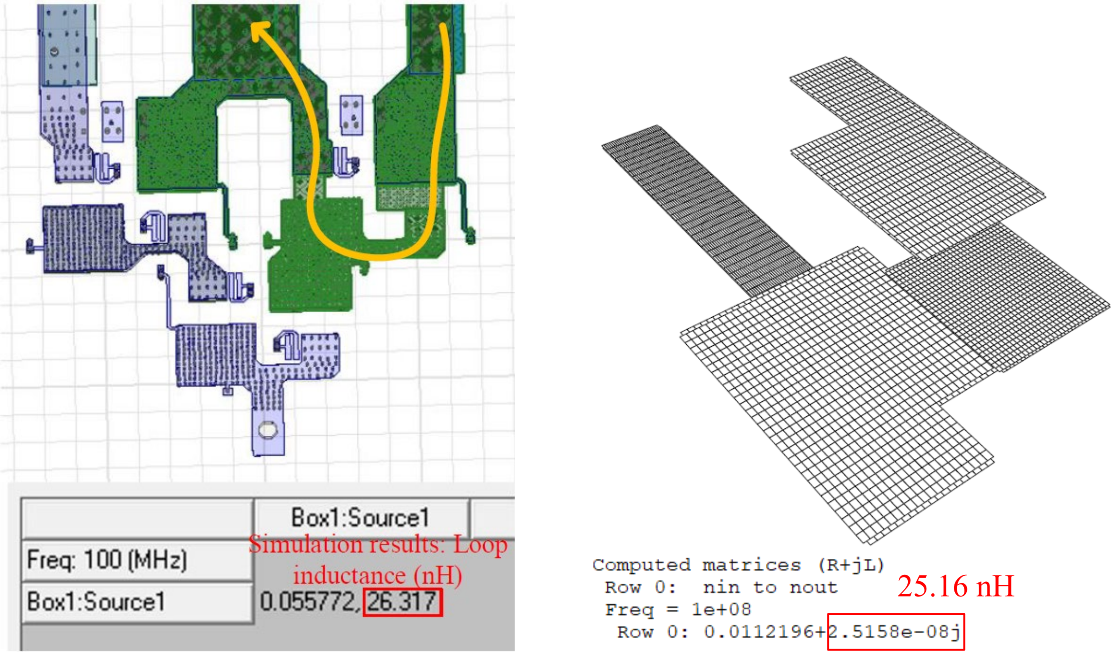
C. Design Example and Verification

In order to verify the effectiveness of the implemented PEEC method, three geometry examples are used for parasitic inductance extractions through FEM software Q3D and PEEC algorithm.

The first two examples are from the practical PCB layout of one 10 kW ANPC converter shown in Fig. 4-16. For the PEEC method, planes are used to model the power loop layout while, for the FEM method by Q3D, PCB layout in Altium Designer can be directly imported into the software for the simulation. Also, the thickness of the cooper is set as 2oz. Fig. 4-16(a) and (b) gives the parasitic inductance results for the short commutation loop in the ANPC converter with FEM and PEEC methods, and the difference is 4.45 %. Furthermore, Fig. 4-16(c) and (d) gives the parasitic inductance results for the long commutation loop in the ANPC converter with FEM and PEEC methods, and the difference is 2.3%. This comparison demonstrates that the PEEC method can achieve similar accuracy of parasitic inductance calculation compared with the FEM method.

Another geometry example is created automatically for a busbar design for a two-level converter. As Fig. 4-17 shows, the inductance values from FEM and PEEC are also very close, and the difference is 6.17%.

By comparing the calculated inductance values for the same geometries with FEM and PEEC methods, it demonstrated the PEEC method can achieve a comparable accuracy in terms of parasitic inductance extraction.



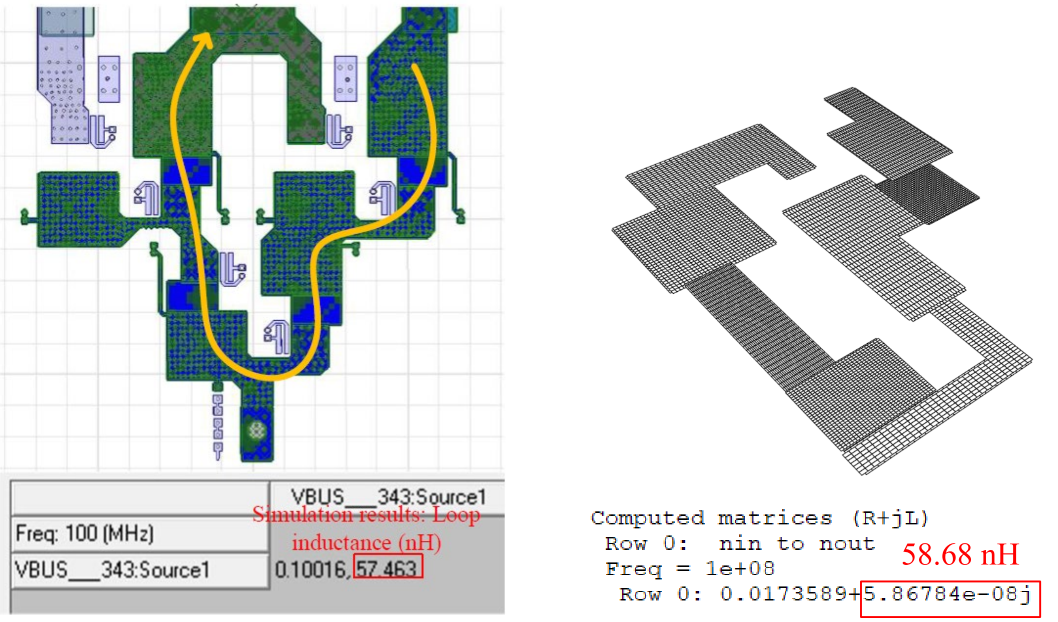
	Box1:Source1
Freq: 100 (MHz)	
Box1:Source1	0.055772, 26.317

Simulation results: Loop inductance (nH)

```
Computed matrices (R+jL)
 Row 0:  nin to nout
 Freq = 1e+08
  Row 0: 0.0112196+2.5158e-08j
```

25.16 nH

(a) FEM result for short commutation loop (b) PEEC result for short commutation loop



	VBUS___343:Source1
Freq: 100 (MHz)	
VBUS___343:Source1	0.10016, 57.463

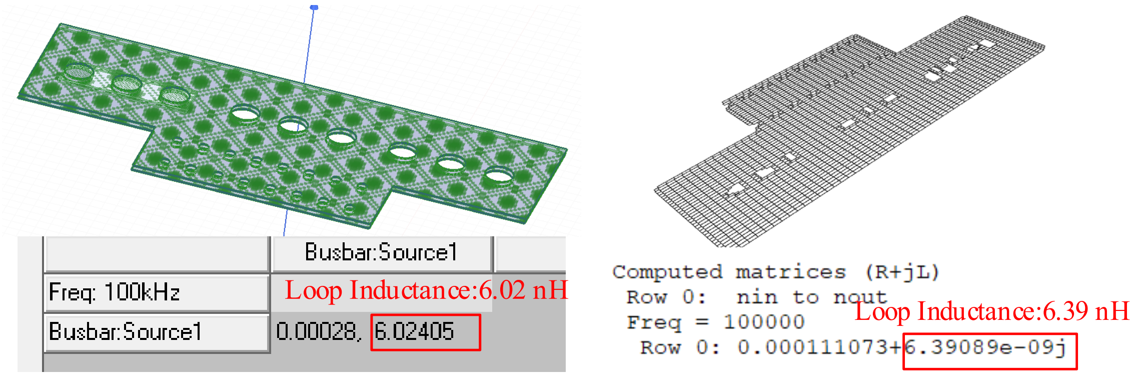
Simulation results: Loop inductance (nH)

```
Computed matrices (R+jL)
 Row 0:  nin to nout
 Freq = 1e+08
  Row 0: 0.0173589+5.86784e-08j
```

58.68 nH

(c) FEM result for long commutation loop (d) PEEC result for long commutation loop

Fig. 4-16. Extracted inductance value comparison of ANPC layout between FEM and PEEC.



	Busbar:Source1
Freq: 100kHz	Loop Inductance:6.02 nH
Busbar:Source1	0.00028, 6.02405

```
Computed matrices (R+jL)
 Row 0:  nin to nout
 Freq = 100000
  Row 0: 0.000111073+6.39089e-09j
```

Loop Inductance:6.39 nH

(a) FEM result (b) PEEC result

Fig. 4-17. Extracted inductance value comparison of the laminated busbar between FEM and PEEC.

4.4 Gate Resistance Selection with Switching Speed Optimization

The relation between the gate resistance selection and switching speed usually is not considered in the paper stage, and some research work only tries to optimize gate resistance selection in terms of the trade-off between the switching loss and the switching frequency. However, in the testing stage, it always needs to change the gate resistance since power devices suffer drain-source voltage oscillations with a high overvoltage spike or cooling system is not capable of the heat caused by devices' power losses. Once the gate resistance is changed to fix issues, the cooling and noise performance change accordingly, which may induce a trial-and-error procedure for the converter testing. To reduce this gap between the paper design and the practical implementation, the gate resistance selection is carefully considered in paper design in this dissertation by the switching speed prediction with the developed discrete-time switching behavior model and the parasitic inductance extraction with the developed automated geometry creation and PEEC numerical modeling method.

4.4.1 Gate Resistance General Selection Constraints

Before giving the gate resistance constraints limited by the switching speed, some general gate resistance selection criteria are given in this subsection. For gate drive circuits during turn-on and turn-off transients, as shown in Fig. 4-18, it was formed of an LCR resonant circuit, which is a classical second-order system. To avoid the oscillations of the gate voltage and current, it was necessary to avoid the system as an underdamped state. The damping ratio of such a circuit can be easily derived as:

$$\xi=\frac{1}{2}(R_G+R_{pull-up})\sqrt{\frac{C_{GS}}{L_G}} \tag{4.13}$$

where R_G is the gate resistance including the internal and external gate resistance, $R_{pull\text{-}up}$ is the pull-up (or pull-down for turn-off) gate resistance inside the gate drive IC. C_{GS} and L_G are the parasitic gate to source capacitance and gate loop parasitic inductance.

If the damping ratio is larger than 1, the oscillation of the gate voltage and current can be avoided, which gives a gate resistance lower limit as:

$$R_G \geq 2\sqrt{\frac{L_G}{C_{Gs}}} \tag{4.14}$$

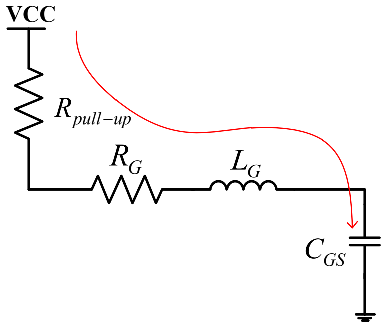


Fig. 4-18. Equivalent circuits for gate drive during turn-on transient.

The second constraint is to select the proper gate resistance to limit the initial gate current not to exceed the maximum source and sink current. The purpose of this is to make the totem pole circuit inside the gate drive IC not to work in the saturation region. Also, the developed discrete-time switching behavior model does not cover the modeling of the gate drive, so it is better to keep the gate drive working at the ohmic region for the higher modeling accuracy. With this constraint, a low limit constraint is given as:

$$R_G \geq \frac{V_{cc} - V_{ee}}{I_{g\max}} \tag{4.15}$$

where V_{cc} and V_{ee} are the steady-state gate voltages for turn-on and turn-off, I_{gmax} is the maximum gate current determined by the peak sink and source current capability of gate drive IC.

4.4.2 Turn-off Gate Resistance Selection with *di/dt* constraint

Combined with Eq.(4.14) and Eq. (4.15), an initial gate resistance can be decided. Nonetheless, this initial gate resistance generally has a very low value to cause an unaccepted voltage spike due to the drain-source voltage oscillation. The diagram of the determination of the turn-off gate resistance to avoid the overvoltage issue is given in Fig. 4-19.

First, a SiC device is chosen from the device database, also providing the package information for the geometry creation and the device characteristics information for the analytical device switching behavior model. Second, the busbar geometry or PCB layout is created depending on the device type (power module or discrete device) and the topology. Third, the parasitic inductance of the created geometry can be extracted by the numerical modeling method through the PEEC method, and the *di/dt* value can be obtained by the discrete-time switching behavior model with the initial turn-off gate resistance. Finally, a design iteration is conducted to increase the initial

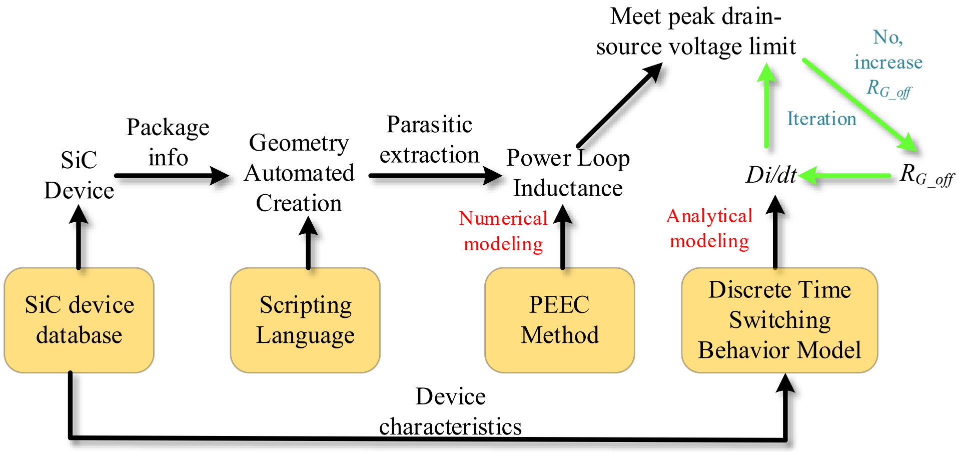

Meet peak drain-source voltage limit
No, increase R_{G_off}
Iteration
Package info
SiC Device
Geometry Automated Creation
Parasitic extraction
Power Loop Inductance
Di/dt
R_{G_off}
Numerical modeling
Analytical modeling
SiC device database
Scripting Language
PEEC Method
Discrete Time Switching Behavior Model
Device characteristics

Fig. 4-19. Diagram of the determination of turn-off gate resistance considering *di/dt*.

turn-off resistance until the calculated peak drain-source voltage is within the design margin. Since the applied numerical model and analytical model can reflect the practical implementations more precisely, the voltage margin can be reduced from the conventional 50% to 20% for the lower switching losses.

4.4.3 Turn-on Gate Resistance Selection with *dv/dt* constraint

For the turn-on gate resistance selection, the lower limit can be determined by the Eq. (4.14) and Eq. (4.15) and another lower limit can be decided to prevent the malfunction of gate drive at off-state during the high *dv/dt* event created by the complementary switch, which is shown in Fig. 4-20. The voltage across the gate to source during *dv/dt* cannot exceed the threshold voltage V_{th} for preventing the switch from false turn-on. The expression of v_{gs} during dv/dt can be derived as:

$$C_{gd}\cdot\frac{dv}{dt}\cdot\left(R_{G\_off}+R_{sink}\right)\cdot\left(1-e^{-\frac{\Delta t}{\left(R_{G\_off}+R_{sink}\right)\left(C_{gd}+C_{gs}\right)}}\right)\le 0.8V_{th} \tag{4.16}$$

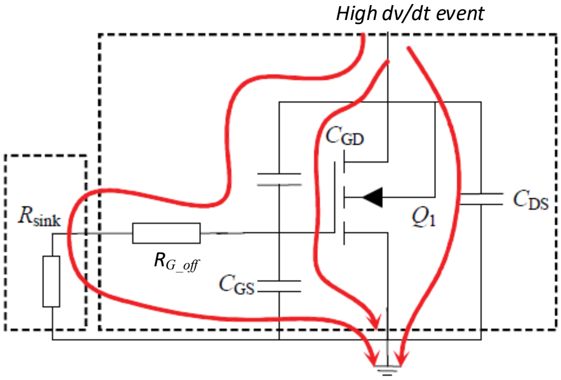


Fig. 4-20. Malfunction of gate drive due to high *dv/dt* event.

where *dv/dt* value and the turn-on time Δ*t* are determined by R_{G_on} of the complementary switch. A 20% margin is given for the threshold voltage judgment.

To satisfy Eq. (4.16) with a proper R_{G_on}, the diagram shown in Fig. 4-21 is applied. The initial turn-on gate resistance is set as 0 Ω and the turn-off gate resistance has already been determined by the iteration shown in Fig. 4-19, and a design iteration is conducted to increase the initial turn-on resistance until the Eq. (4.16) is satisfied. The obtained R_{G_on} from the diagram is also a lower limit of turn-on resistance and, combined with the lower limit decided in Section 4.4.1, the minimum R_{G_on} can be determined. Based on the study of impacts of the switching edges on the EMI noise spectrum in [150], the sharp and high slew rate switching edges of wide bandgap (WBG) devices only affect the EMI noise higher than 20 MHz, so the fast switching speed is good for EMI noise spectrum. Based on the author's experience, the disadvantage of ultra-fast switching is the most ICs in the markets do not have enough high CM noise transient immunity (CMTI) to withstand high *dv/dt* and common mode pulse noise, introducing many difficulties in control and sampling circuits design. However, IC designers and manufacturers start to improve the CMTI capability aiming for WBG devices and some research has been done for the control and sampling

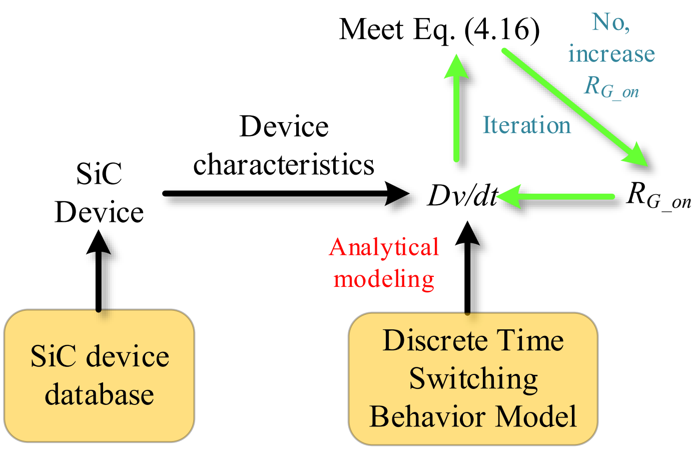

Meet Eq. (4.16)
No, increase R_{G_on}
Iteration
Device characteristics
SiC Device
Dv/dt
R_{G_on}
Analytical modeling
SiC device database
Discrete Time Switching Behavior Model

Fig. 4-21. Diagram of the determination of turn-on gate resistance considering *dv/dt*.

circuits design at the high switching speed [151]. Hence, the minimum R_{G_on} is selected as the final turn-on gate resistance for the lighter cooling system and EMI filter design.

4.4.4 Complete Design Example for Gate Resistance Selection

SiC MOSFET C3M0065090J is used for a two-level VSC as a design example and four film capacitors MKP1848712924Y5 from Vishay are chosen as the dc-link capacitors. The corresponding layout has been created given in Fig. 4-22 and the parasitic inductance is calculated as 9.1 nH considering the power loop and parasitic inductance of the dc-link capacitors, and other parameters and parasitics are summarized at Table 4-3.

With the parameters in Table 4-3 and the discrete-time switching behavior model, the gate resistance selection constraints in Section 4.4.1 and the design iteration results in Section 4.4.2 and 4.4.3 are obtained and summarized in Table 4-4.

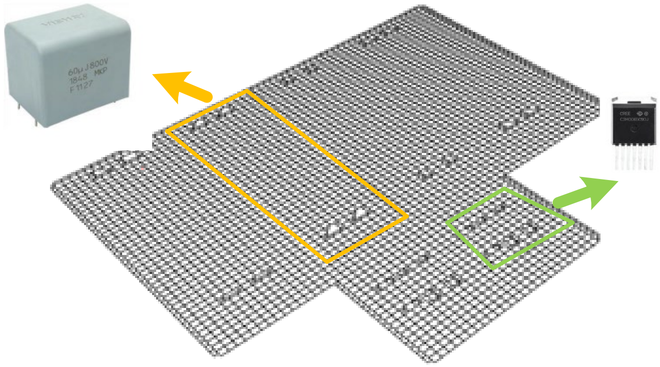


Fig. 4-22. Automatically created power loop layout for design example with C3M0065090J.

Table 4-3. Parameters of design example with C3M0065090J.

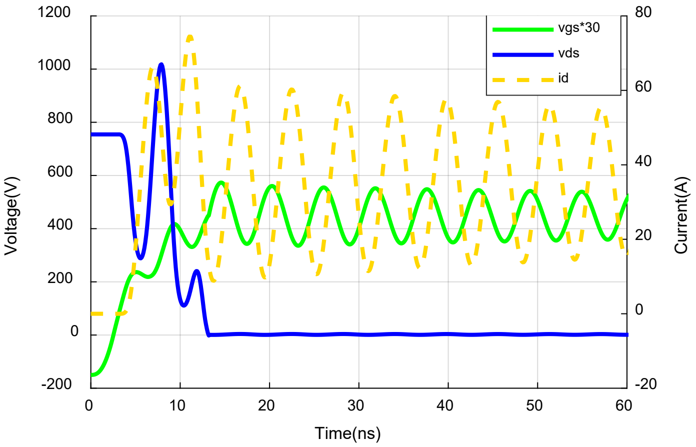
Parameters	***Values***
Dc-link voltage: V_{dc}	750 V
Maximum load current: I_{acmax}	35 A
Power loop inductance: L_d	7.9 nH
Parasitic capacitance: C_{gs}	980 pF
Gate drive voltage: V_{dr}	15 V/ -5 V
Required maximum V_{ds}: V_{dsmax}	862 V (750*1.15)
Gate loop inductance: L_g	2 nH
Common source inductance: L_{ss}	0.5 nH

Table 4-4. Gate resistance selection constraints summary.

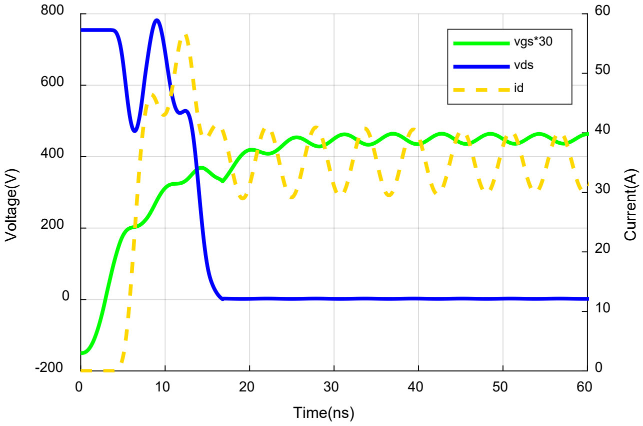
Parameters	***Values***
Gate voltage damping: Eq. (4.14)	>= 5.6 Ω
Gate drive current limitation: Eq. (4.15)	>= 3.3 Ω
Design iteration for R_{G_off} to suppress peak voltage	>= 7.7 Ω
Design iteration for R_{G_on} to avoid cross-talk	>= 5.8 Ω

Based on Eq. (4.14), the gate resistance should be higher than 5.6 Ω to damp the gate voltage oscillation for a second-order system, and Fig. 4-23 gives the v_{gs} waveforms comparison with different gate resistances. From Fig. 4-23(a) and (b), it is clear to see that v_{gs} waveforms are at under damped state during the turn-on when the gate resistance is lower than 5.6 Ω. Once the gate resistance is increased to 5.6 Ω as shown in Fig. 4-23(c), the v_{gs} waveform is well damped without oscillations. Gate drive IC current limitation determined the lower boundary of the gate resistance given in Table 4-4 is 3.3 Ω, which is surpassed by the gate voltage damping constraint.

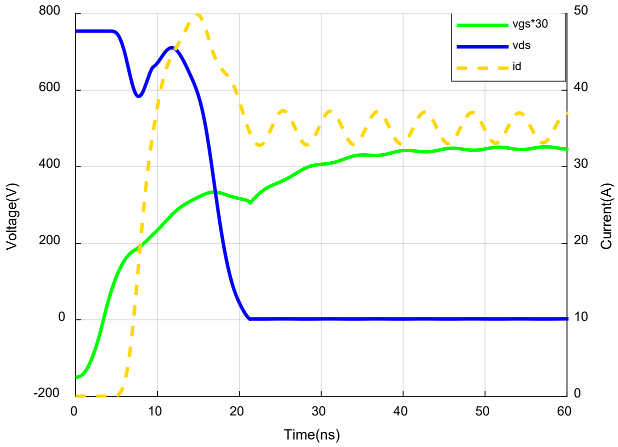
5.6 Ω is set as an R_{G_off} for the v_{ds} overvoltage suppression iteration, and 0.1 Ω is selected as the step change for each iteration. After the iterations are finished, 7.7 Ω is the final obtained value to achieve the overvoltage target given in Table 4-3. Fig. 4-24 further gives the v_{ds} waveforms comparison when the gate resistance is 5.6 Ω or 7.7 Ω. Fig. 4-24(b) shows the peak voltage with 7.7 Ω turn-off gate resistance is 863.2 V while Fig. 4-24(a) shows the peak voltage with 5.6 Ω turn-off gate resistance is 887.7 V.



(a) R_{G_on}=2 Ω

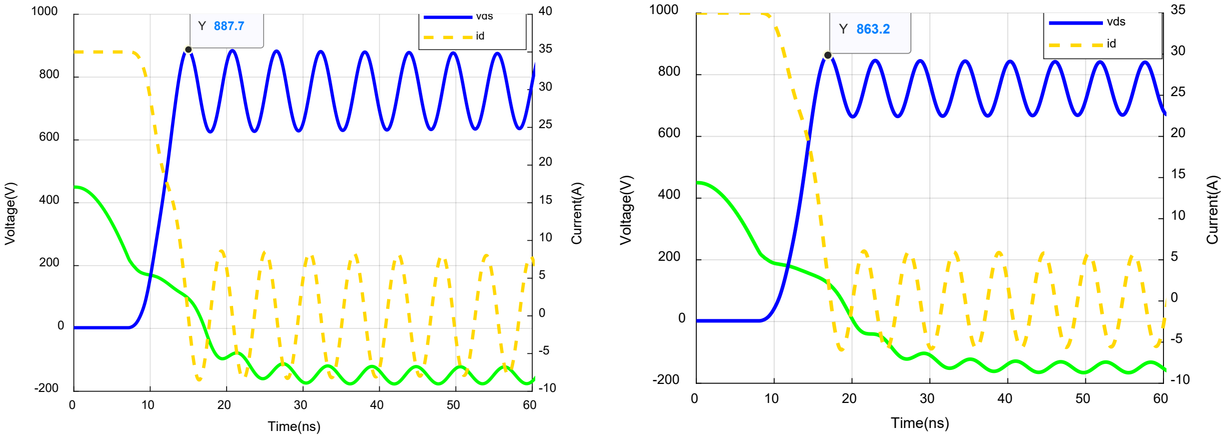


(b) R_{G_on}=4 Ω



(c) R_{G_on}=5.6 Ω

Fig. 4-23. Switching waveforms and v_{gs} comparison with different gate resistances.



(a) R_{G_off}=5.6 Ω (b) R_{G_off}=7.7 Ω

Fig. 4-24. Switching waveforms and v_{ds} comparison with different gate resistances.

In addition, 5.6 Ω is set as an initial R_{G_on} for the iteration to avoid malfunction of the gate drive, and 0.1 Ω is selected as the step change for each iteration. After the iterations are finished, 5.8 Ω is achieved.

In summary, with the design iterations of the gate resistance selection considering switching speed, the turn-on resistance is selected as 5.8 Ω and the turn-off resistance is selected as 7.7 Ω for this design example.

4.5 Summary

A discrete-time switching model is developed to predict the switching speed and peak voltage spike with different gate resistances. Compared with the existing literature, the developed discrete-time switching model incorporates the temperature-related characteristics, such as temperature-dependent transconductance, temperature-dependent threshold voltage. Also, C_{gs} nonlinear characteristic as a function of v_{gs} is included in the model for better prediction accuracy.

Since the conventional power electronics design cannot evaluate the switching speed and overvoltage during the device selection due to the absence of the geometries for the busbar or PCB layout in the paper design stage, an automatic geometry creation tool using the open-source geometry description scripting language is developed. A simplified geometry only for power loop following the magnetic field cancellation can be created based on the topology, device package and dc-link capacitor dimension information. Also, the thickness of a busbar can be determined by the developed thermal model and weight optimization iteration. Once the geometry is confirmed, through the PEEC numerical modeling method, the parasitic inductance can be calculated as the input for the discrete-time switching behavior model.

With the switching behavior model and PEEC numerical modeling, the design iterations are proposed to determine the suitable turn-on and turn-off gate resistances. For the turn-off gate resistance, it is mainly determined by the *dv/dt* and corresponding power loop inductance to maintain a reasonable voltage spike. For the turn-on gate resistance, it is decided to avoid the malfunction of gate drives.

With such improvements, the device selection iteration can be more scientific to avoid the trial-and-error in the implementation stage, and gate resistances are preselected based on the switching speed and overvoltage limitations. Moreover, the cooling design can be also more scientific considering the switching speed and applied gate resistances, and this part will be presented in the next Chapter.

Chapter Five

Cooling Design Optimization with Multi-variable Device Loss Scaling

Cooling design plays an important role in the power electronics design to keep the power semiconductors working at a safe junction temperature. To have a more accurate cooling design, the pressure drop of heatsinks and fans must be considered to determine the airflow speed and the corresponding thermal resistance of the heatsink. The power device loss calculation is also critical to achieve a highly accurate cooling design. In this chapter, a multi-variable device loss scaling method is presented considering the junction temperature and gate resistance selection. The general way of the loss calculation is to use the loss data from the datasheet with the linear scaling based on the operating current and voltage. However, some manufacturers only provide one switching loss data at one specific testing condition and gate resistance, and the linear scaling of the only switching loss data may not be accurate enough at some applications. A discrete switching behavior model developed in Chapter IV is applied to scale the switching loss data with the selected gate resistance and the assumed operating junction temperature.

With the developed thermal model of heatsinks and fan, and loss scaling method, a complete design iteration is proposed to search the lowest weight of the combination of devices and heatsinks.

5.1 Cooling System Model

5.1.1 Correction of Thermal Resistance of Extruded Heatsink

In this design, all passive heatsinks are selected with extruded fins, and the thermal resistance of extruded heatsinks is related to the length of heatsinks, the temperature of heatsinks, and airflow speed. Therefore, three correction factors in terms of those variables for extruded heatsinks are given in reference [152] from manufacturer AAVID. Fig. 5-1, Fig. 5-2, and Fig. 5-3 are given to illustrate the relationship of three correction factors and thermal resistance.

Usually, the natural convection thermal resistance for a three-inch length of extrusion heatsinks is given in the manufacturers' datasheet. With the above correction factors, all the heatsinks collected in the database can be adjusted to have different lengths, operating temperatures and airflow speed to satisfy the requirement of thermal resistance of heatsinks.

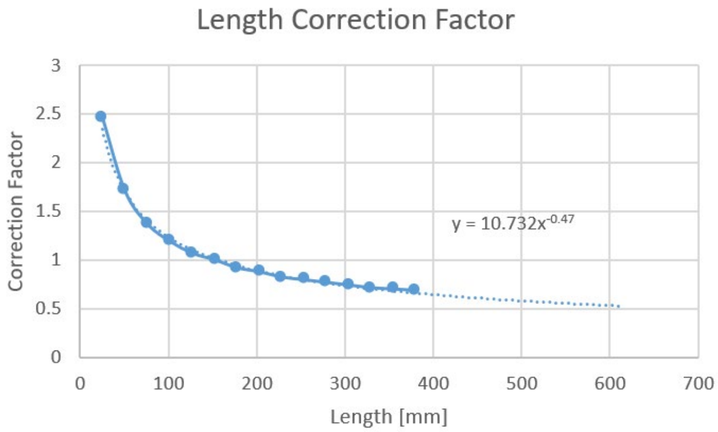


Fig. 5-1. Length correction factor for the thermal resistance of extruded heatsinks.

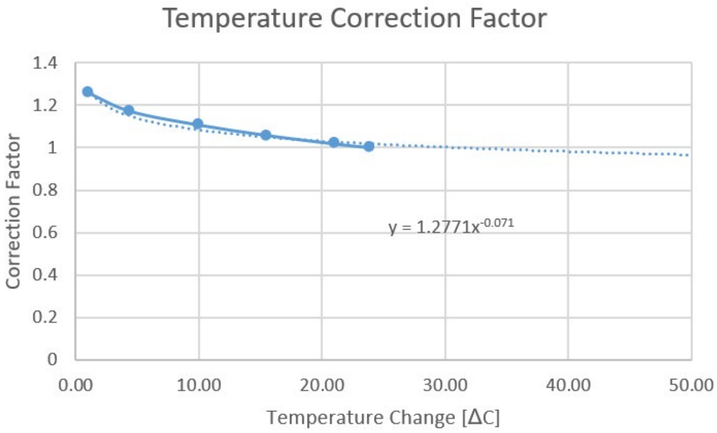


Fig. 5-2. Temperature correction factor for the thermal resistance of extruded heatsinks.

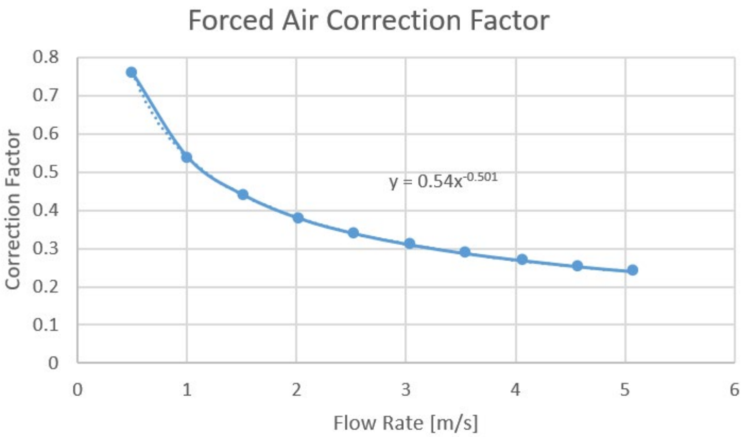


Fig. 5-3. Forced air correction factor for the thermal resistance of extruded heatsinks.

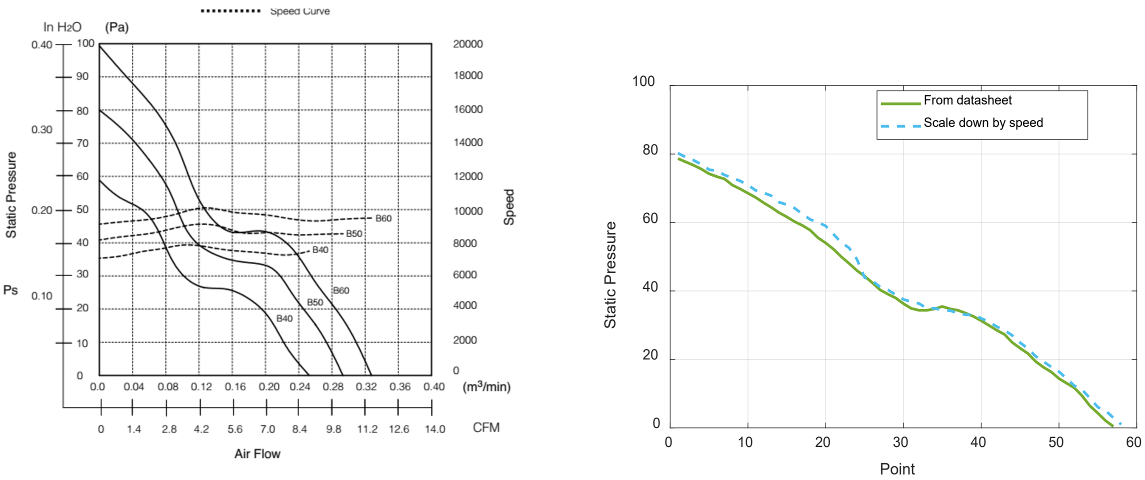
5.1.2 Pressure Drop Model of Heatsinks and Fans

The pressure drop model of extruded heatsinks is developed in reference [69, 76]. The friction caused pressure drop caused by the duct and fins of the heatsink, and the fluid acceleration caused pressure drop are considered in the model, which is expressed as:

$$p_{dr\_tol} = \Delta p_{hs} + \Delta p_{duct} + \Delta p_{acc} \tag{5.1}$$

where p_{dr_tol} is the total pressure drop of the heatsink, Δp_{hs} is the pressure drop caused by the airflow friction of fins and Δp_{hs} is the pressure drop caused by the airflow friction of the duct, Δp_{acc} is the pressure drop caused by the airflow acceleration. The full expanded expression of Eq. (5.1) can be found in the literature [69].

The pressure drop model of fans is obtained through curve fitting based on the datasheet from manufacturer NMB. Only is one pressure drop needed for one series of fans, and the other pressure drop curves at different fan sizes in one series can be scaled by the law of fans related to the RPM, diameter of fans, and fluid density, which is expressed as



(a) Pressure drop curves for 1608VL series (b) Scaling result comparison

Fig. 5-4. Pressure drop curves scaling with the law of fans.

$$P_2 = P_1 \times \left(\frac{n_2}{n_1}\right)^2 \times \left(\frac{d_2}{d_1}\right)^2 \times \left(\frac{\rho_2}{\rho_1}\right)^1 \tag{5.2}$$

where n is the rotation speed of fans per minute, d is the diameter of fans, and ρ is the air density at different altitudes.

With such a scheme, the fitting efforts of different fans are much reduced. Fig. 5-4(a) gives one scaling result for the 1608VL-04W series from NMB company. The pressure drop curve of 1608VL-04W-B40 whose speed is 7500 RPM at zero pressure drop is obtained by curve fitting method. Then, 1608VL-04W-B50 whose speed is 8500 RPM at zero pressure drop is scaled from the pressure curve of 1608VL-04W-B40 based on Eq. (5.2), which is shown in Fig. 5-4(b). Compared with the curve given in Fig. 5-4(a), the obtained curve through the scaling method has very good accuracy.

With the pressure drop models for heatsinks and fans, the operating condition can be determined by the intersection point of two pressure curves of the selected heatsink and fan. Fig. 5-5 gives one example of the pressure drop curves of the selected heatsink and fan, the intersection point is

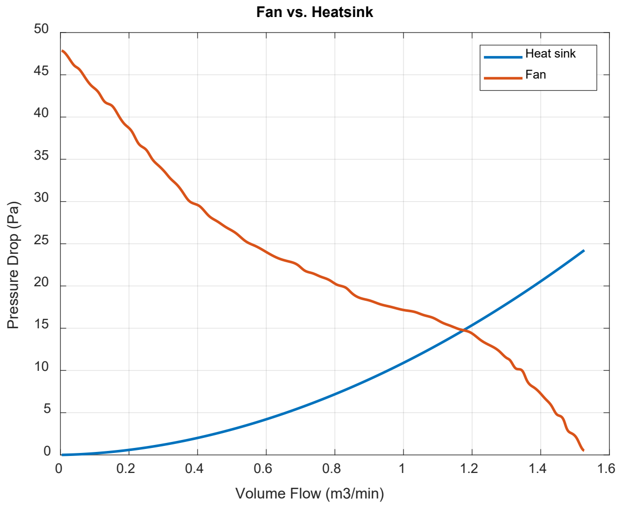


Fig. 5-5. Operating condition determination with pressure drop curves of selected heatsink and fan.

located when the volume flow of the fan equals 1.19 m^3/min. If the pressure drops are not considered in the design, the initial volume flow at zero pressure drop is 1.53 m^3/min, introducing a 28.6% error for the estimation of the operating airflow speed. As a result, the thermal resistance of the heatsink will also have a remarkable error, leading to an underestimate thermal resistance and a trial-and-error process.

5.2 Switching Loss Scaling Method Considering Practical Parameters

5.2.1 Proposed Scaling Method

The most convenient way to calculate the switching loss is to utilize the switching loss data from the official datasheet. However, most of the datasheets did not provide comprehensive switching loss data at different operating voltages, currents, and applied gate resistances. The compromise way is to use the linear scaling method to calculate the switching loss at arbitrary current and voltage levels. The disadvantages of the linear scaling method are listed as follows:

1. The switching loss includes the non-linear part associated with the non-linear junction capacitance as a function with v_{ds}. Only using the linear scaling method will cause relatively large errors at the low current level and high switching frequency.
2. The switching loss calculation does not reflect the selected or practical gate resistance in the linear scaling method. The switching loss data given by the datasheet is always measured with a typical gate resistance 10 Ω. However, the gate resistance can be varied much based on the power loop parasitic inductance and other switching speed constraints presented in Section 4.4. Hence, the switching loss must be also scaled with the selected gate resistance.
3. The impacts of temperature on the transconductance and threshold voltage are not included in the linear scaling method. The transconductance and threshold voltage are varied with the operating temperature, affecting the switching speed of the power devices.

To overcome those disadvantages and improve the switching loss calculation accuracy, a multi-variable switching loss scaling method based on the developed discrete-time switching behavior model is proposed. Compared with the linear scaling method, except the operating voltage and current, the selected gate resistance R_G and the operating junction temperature T_j are also required as the input variables for the loss scaling. Also, the separation of the non-linear loss related to the junction capacitance and the overlap loss during switching transients has been conducted for higher accuracy.

The non-linear part switching loss is caused by charging or discharging of the junction capacitance, and two losses are associated with this process. As shown in Fig. 5-6, during the charging process of a non-linear junction capacitance, E_{oss} represents the energy stored in the junction capacitance and E_r represents the energy consumed by the resistive component in the circuits. Because of the existence of non-linear junction capacitance, E_{oss} and E_r are not equal like the linear capacitance, and the expression of each part can be expressed as:

$$E_{oss}(V) = \int_0^V C_{oss}(v_c) v_c dv \tag{5.3}$$

$$E_r(V) = Q(V)V - E_{oss} = \int_0^V V C_{oss}(v_c) dv_c - \int_0^V C_{oss}(v_c) v_c dv \tag{5.4}$$

The separation of the switching loss has been summarized in Table 5-1. The loss distributions of DPT measured data and theoretical data are different since the current sensor cannot directly measure the channel current of power devices. The function E_{oss} and E_r at any voltages can be calculated with C_{oss} fitting function got in Section 4.1.1, and the overlap loss E_{VIon} and E_{VIoff} are obtained by using the E_{on} and E_{off} in the datasheet based on the loss distribution in Table 5-1. Then, the overlap loss E_{VIon} and E_{VIoff} part will be scaled with the discrete-time switching behavior model by the applied gate resistance R_G, the assumed junction temperature T_j, and the operating voltage and current.

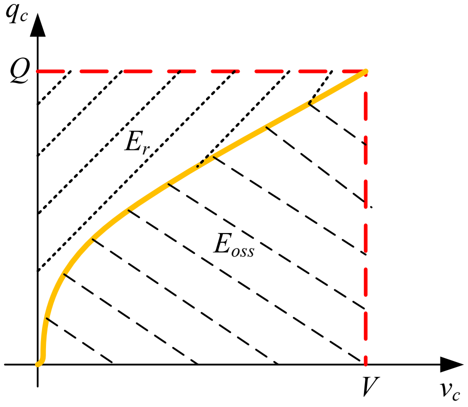


Fig. 5-6. Loss related to the non-linear capacitance during charging and discharging.

Table 5-1. Summary of Switching Loss Separation.

Switching loss	***Loss distribution***	
	DPT Measured	Theoretical
Turn-on loss E_{on}	$E_{VIon} + E_r$	$E_{VIon} + E_r + E_{oss}$
Turn-off loss E_{off}	$E_{VIoff} + E_{oss}$	E_{VIoff}

First, the scaling ratio is obtained by using the discrete-time switching behavior model to calculate the overlap loss ratios between the required operating condition and the reference operating condition in the datasheet:

$$\begin{cases} r_{loss\_on} = \dfrac{E_{VIon\_cal}(R_G, T_j, V, I)}{E_{VIon\_cal}(R_{G\_ref}, T_{j\_ref}, V_{ref}, I_{ref})} \\ r_{loss\_off} = \dfrac{E_{VIoff\_cal}(R_G, T_j, V, I)}{E_{VIoff\_cal}(R_{G\_ref}, T_{j\_ref}, V_{ref}, I_{ref})} \end{cases} \tag{5.5}$$

where E_{VIon_cal} and E_{VIoff_cal} are the calculated values with the discrete-time switching behavior model, R_G, T_j, V and I are the real operating condition in the paper design, and R_{G_ref}, T_{j_ref}, $V_{ref,}$ and I_{ref} are the reference operating condition for the measured switching loss data.

Second, the reference turn-on and turn-off energy loss E_{on_ref} and E_{off_ref} from the datasheet are used to get the updated E_{on_upd} and E_{off_upd} with the overlap loss ratios:

$$\begin{cases} E_{on\_upd} = r_{loss\_on} \cdot E_{VIon\_ref} + E_r(V) \\ \qquad\quad = r_{loss\_on} \cdot \left(E_{on\_ref} - E_r(V)\right) + E_r(V) \\ E_{off\_upd} = r_{loss\_off} \cdot E_{VIoff\_ref} + E_{oss}(V) \\ \qquad\quad = r_{loss\_on} \cdot \left(E_{off\_ref} - E_{oss}(V)\right) + E_{oss}(V) \end{cases} \tag{5.6}$$

5.2.2 Verification of Proposed Scaling Method

In order to verify the effectiveness of the proposed switching loss scaling method, DPT testing set up for SiC MOSFET C3M0065090J shown in Fig. 4-7 is used to measure the switching loss data at different gate resistances, testing voltages and currents.

First, a group of measured data with the same testing current and gate resistance but at different testing voltages is used for study and comparison. The loss data at 150 V and 35 A is used as the reference values, and both the linear scaling method and the proposed scaling scheme are applied to get the switching loss data at 300 V and 450 V. Fig. 5-7 gives the scaling results with two methods, and it shows that the scaling results of E_{on} with the linear scaling method diverge greatly from the measured results of E_{on}. Although the results with the proposed scheme have a maximum error of 12.1%, they are much more accurate than the results with the linear scaling method for E_{on}. For E_{off} scaling, two methods achieve similar accuracy, but the linear scaling method shows a little bit better result at 450 V cases compared with one with the proposed scheme. Overall, the proposed scaling scheme shows the higher accuracy of the total switching loss over the linear scaling method in terms of the voltage variable scaling.

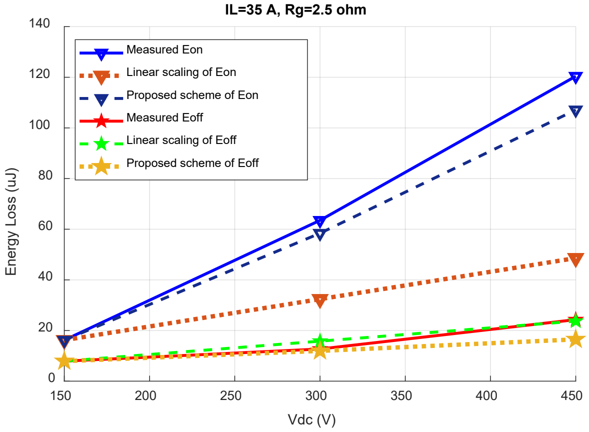


Fig. 5-7. Switching loss scaling at different testing voltages.

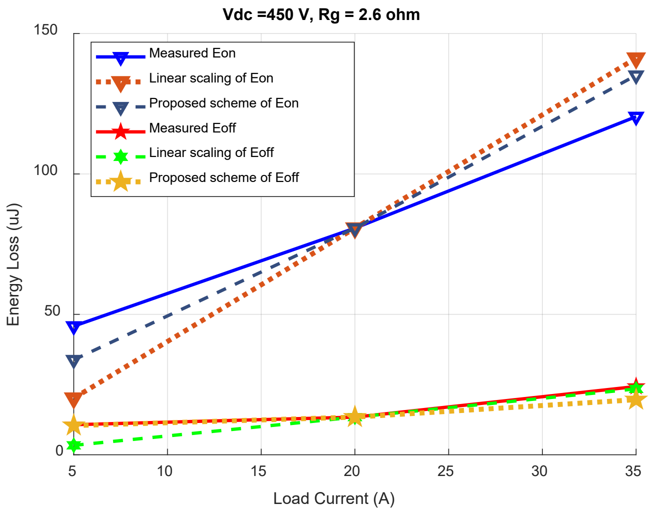


Fig. 5-8. Switching loss scaling at different testing currents.

Second, a group of measured data with the same testing voltage and gate resistance but at different testing currents is used for study and comparison. The loss data at 450 V and 20 A is used as the reference values, and both the linear scaling method and the proposed scaling scheme are applied to get the switching loss data at 5 A and 35 A. As shown in Fig. 5-8, unlike the voltage variable scaling, the results of E_{on} from the linear scaling method does not diverge from the measured data that much. Nonetheless, the results of E_{on} from the proposed scheme still achieve a smaller error than the ones of the linear scaling method. The maximum error of E_{on} with the proposed scheme is 26.2 % at 5 A. For E_{off} scaling, since E_{off} is much smaller than E_{on}, the error of two methods are both within an accepted range, not introducing an obvious error to the total switching losses calculation. In a summary, two methods are both effective to scale the switching losses for the current variable scaling with acceptable errors, but the proposed scaling scheme shows a little bit higher accuracy than the linear scaling method.

Third, the measured switching loss data with the same testing current and voltage but different gate resistance is used for study and comparison. The loss data at 450 V, 30 A and 2.5 Ω is used as the reference values. From Fig. 5-9, the scaled E_{on} for the 20 Ω gate resistance has a 20.9% error compared with the measured data with 20 Ω gate resistance, but it is still better than only using one switching loss data to calculate the switching loss for different gate resistances.

Fourth, a group of switching data at different junction temperatures from the datasheet of SiC MOSFET C3M0065090J is used for study and comparison. The loss data at 400 V, 20 A and 2.5 Ω is used as the reference values, and the scaled switching loss data at different temperatures are obtained shown in Fig. 5-10. The maximum error of the scaled results is 15.25 % compared with the measured data. The variation of the scaled switching loss data as a function of operating temperatures is smaller than one of the measured loss data. The difference of E_{on} between 25 °C and 150 °C is 3.7 μJ for the scaled switching loss data so that it may not have an obvious difference if not considering the temperature impacts, but the proposed method still improves the accuracy a little bit by considering the junction temperature influences.

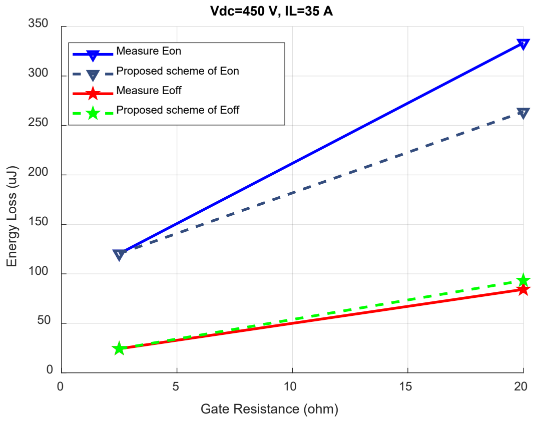


Fig. 5-9. Switching loss scaling at different gate resistances.

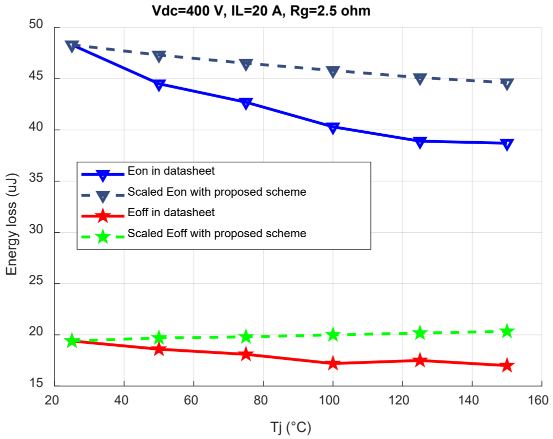


Fig. 5-10. Switching loss scaling at different junction temperatures.

At final, a switching loss calculation comparison with two scaling methods are conducted for a two-level VSC and the detailed specifications of the converter are given in Table 5-2. The loss breakdown of the total device losses with two scaling methods are given in Table 5-3, and the main difference part is the turn-on power loss, which is up to 7.5 W. For turn-off power loss, the difference is 0.9 W since the turn-off power loss itself is small. The conduction losses from two methods are the same because it is only determined by the channel on-resistance at different junction temperatures. Overall, the total power loss difference is 8.41 W, which is around 12 % of the total power loss with the linear scaling method.

Table 5-2. Specs for switching loss comparison.

Parameters	***Values***
V_{dc}	750 V
Output power	10 kW
Switching frequency	100 kHz
Operating junction temperature	120 °C
Turn-on resistance	5.6 Ω
Turn-off resistance	7.7 Ω
Reference E_{on}	39 uJ @ 400 V/20 A/7.2 Ω
Reference E_{off}	17 uJ @ 400 V/20 A/7.2 Ω

Table 5-3. Switching loss calculation comparison with two scaling methods.

Switching loss	***Loss Comparison***	
	Linear Scaling	Proposed Scaling method
Turn-on power loss P_{on}	*26.74 W*	*34.25 W*
Turn-off power loss P_{off}	*8.16 W*	*9.06 W*
Conduction loss P_{con}	*37.57 W*	*37.57 W*
Total device power loss P_{tol}	*72.47W*	*80.88 W*

5.3 Design Iteration Combined with Device Selection and Cooling Design

A design iteration combined with the device selection and cooling design is given in Fig. 5-11. A commercially available SiC MOSFET, heatsink and fan databases are prebuilt for the design iterations. As shown in Fig. 5-11, after the initialization of the device database, each device will go through the device selection iteration. To exclude some infeasible devices, a preliminary judgment on the voltage rating and current rating is applied as:

$$\begin{array}{l}\text{Voltage rating: } 1.2V_{stress} \le V_{rated} \le 2V_{stress} \\ \text{Current rating: } I_{rated} \le I_{rms}\end{array} \tag{5.7}$$

where V_{rated} and I_{rated} are the rated voltage and current for the continuous running in the datasheet, V_{rated} is the voltage stress during the turn-off in the steady state, I_{rms} is the maximum current RMS value of one switch for one line cycle.

After passing the preliminary judgment, a gate resistance determination considering switching speed and geometry limitation based on Chapter IV is conducted. Then, with the proposed loss scaling method, the required E_{on} and E_{off} are obtained at the selected gate resistances, operating junction temperatures, and voltage and current levels. With calculating the power

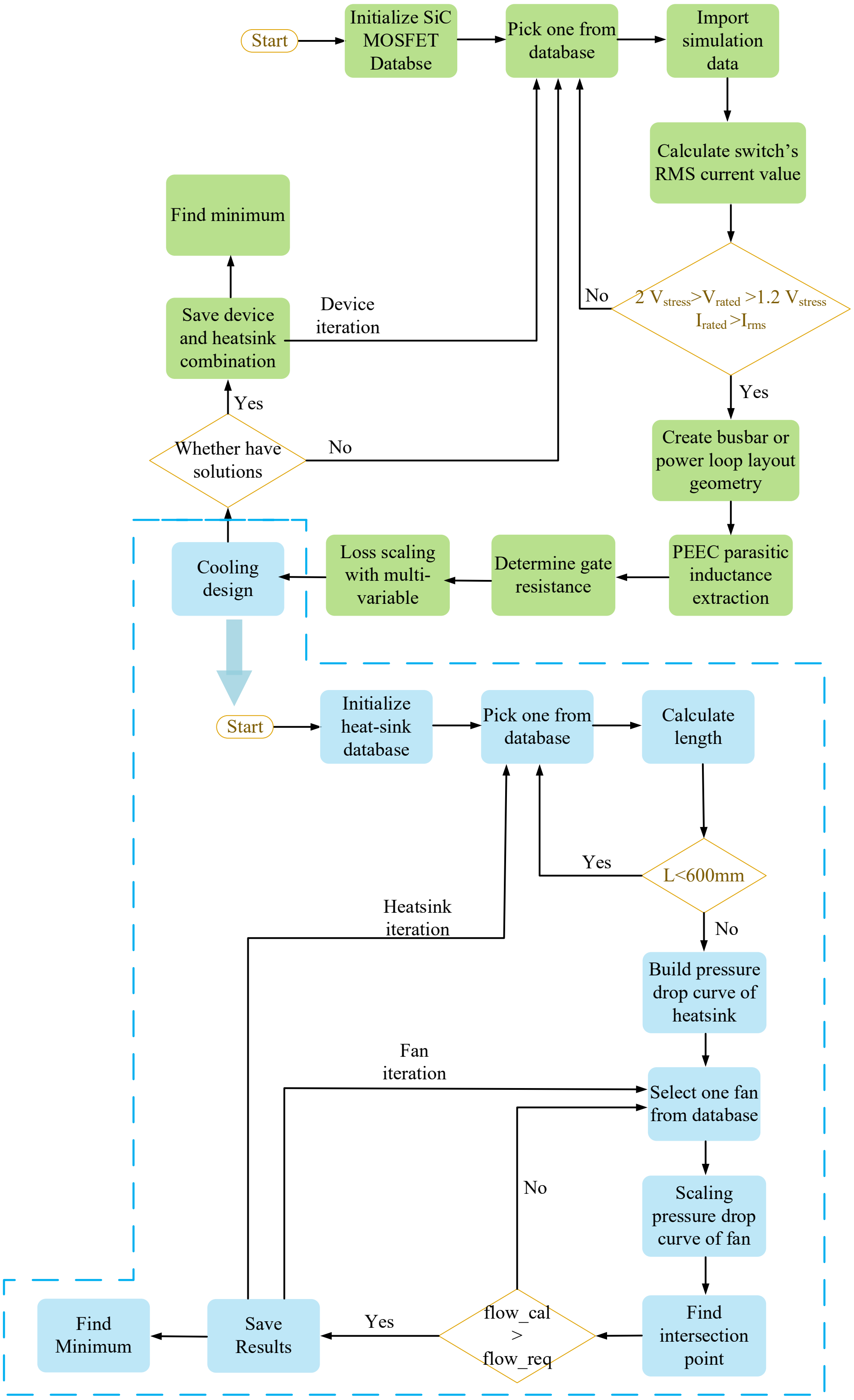

Start
Initialize SiC MOSFET Databse
Pick one from database
Import simulation data
Calculate switch's RMS current value
2 V_stress>V_rated >1.2 V_stress
I_rated >I_rms
No
Yes
Create busbar or power loop layout geometry
PEEC parasitic inductance extraction
Determine gate resistance
Loss scaling with multi-variable
Cooling design
Whether have solutions
No
Yes
Save device and heatsink combination
Device iteration
Find minimum
Start
Initialize heat-sink database
Pick one from database
Calculate length
L<600mm
Yes
No
Build pressure drop curve of heatsink
Select one fan from database
Scaling pressure drop curve of fan
Find intersection point
flow_cal > flow_req
No
Yes
Save Results
Find Minimum
Heatsink iteration
Fan iteration

Fig. 5-11. Flow chart of device selection and cooling design.

semiconductors' losses, the required thermal resistance is derived. A comprehensive cooling design iteration is conducted in the lower flow chart shown in Fig. 5-11. With the selected fan and heatsink from the database, their pressure drop curves are established by the analytical model and fitting results. The intersection point can be found for the operating condition for a fan, determining the airflow speed the fan can be capable of. The lowest weight of the feasible solutions in the cooling design will be adopted for the selected device, but if no cooling solution is found, this device will be dropped, and a new device candidate will be selected for the iteration.

After the finish of all design iterations, the lowest weight of combinations of power devices and the cooling system is selected from the design results pool.

5.4 Summary

To have a more accurate cooling design to shrink the gaps between the paper design and hardware implementations, the pressure drop model of extrusion heatsinks and fans are developed to determine the operating condition of the fan. Thus, a more practical flow volume (or flow speed) is obtained to correct the thermal resistance of the selected extrusion heatsink.

In addition, the accuracy of the switching loss is also critical to have an accurate cooling design. The conventional linear scaling method with provided E_{on} and E_{off} from datasheets cannot accurately reflect the impacts of the operating junction temperatures and the selected gate resistance. In order to improve the linear scaling method, the discrete-time switching behavior model developed in Section IV is applied to scale the switching loss considering different operating conditions with multiple input variables: the operating voltage, the operating current, the operating temperature, and the gate resistance. Also, separation of the overlap loss and non-linear junction capacitance induced loss is conducted, and only is the overlap loss scaled by a loss ratio obtained by the discrete-time switching behavior model. Through comparison with the measured data, the proposed scaling method can achieve a higher accuracy either in voltage variable scaling or current variable scaling. Moreover, the proposed scaling method enables the switching loss to be scaled with the operating temperature and the selected gate resistance, which is not possible for the linear scaling method. Since the proposed scaling method still uses the loss data from the datasheet rather than the one from the analytical model itself, the demand for the high accuracy of the switching behavior model is relatively weakened.

At last, a comprehensive design iteration combined with the device selection optimization presented in Section IV considering the switching speed and the cooling design optimization with a multi-variable scaling method is proposed. The minimum weight solution can be found in the feasible solutions pool.

Chapter Six

System-level Iteration and Optimization

Except for the design of function blocks inside power converters, how to decide the system-level parameters and configurations are also critical to achieve the lowest converter system weight. The selection of the topology, switching frequency, and the corresponding modulation can affect the system performance greatly, and paralleling converters with different interleaving angles can be another option to improve the system performance. Hence, all those system-level parameters and configurations should be investigated carefully to search the optimal solutions to realize the optimal design goal or target.

Also, the iterations of converter design require many simulations to provide the raw data for the models and calculations. If applying the conventional switch-based simulation model, long execution time is demanded for the whole design iteration, which can be up to several days. To improve the time efficiency of the whole design iteration, switching function based simulations are adopted to reduce the simulation times and required design times.

6.1 Switching Function based Fast Simulation Scheme

For the loss calculation and filter design, the PWM voltages with detailed switching transients are not required especially for WBG switches. Due to the fast switching speed of WBG switches, based on the literature [150], the equivalent frequency of the sharp switching edges of PWM voltage is beyond 20 MHz, causing very limited impacts on the ac output current and dc input current in the simulation. Therefore, to simplify the simulation and to reduce the simulation time, all power switch models in the simulation are replaced with the switching function controlled voltage source. PWM voltage at each phase-leg is synthesized as a function of modulation signals (gate signals) and the dc-link voltage.

Here an ANPC converter is used as an example to illustrate how to synthesize the switching function for the controlled voltage source. As shown in Fig. 6-1, the PWM terminal voltage v_{aN} in phase a can be expressed as:

$$v_{\mathrm{a}N} = (s_1 \times 1 + s_p \times 0)s_2 \frac{V_{dc}}{2} + [s_4 \times (-1) + s_{\mathrm{n}} \times 0]s_3 \frac{V_{dc}}{2} \tag{6.1}$$

where s_i is the corresponding gate drive signal for the switch S_i, and the Boolean variable is used for those signals:

$$s_i = \begin{cases} 1 & \text{switch is on} \\ 0 & \text{switch is off} \end{cases} \tag{6.2}$$

The phase b and c PWM voltages can also be derived like Eq. (6.1), and with three-phase PWM terminal voltages, the CM and DM voltages of each phase are expressed as:

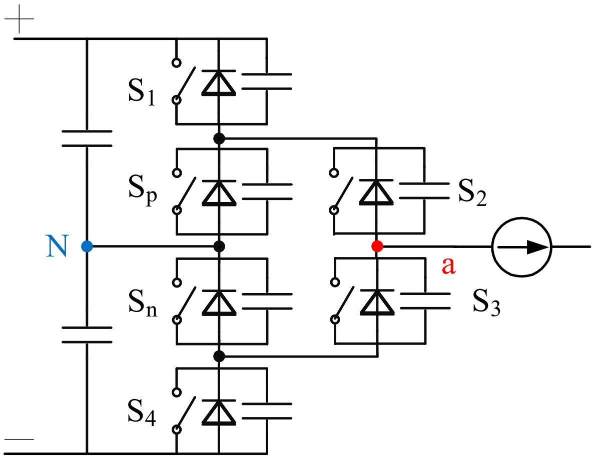


Fig. 6-1. One phase-leg for an ANPC converter.

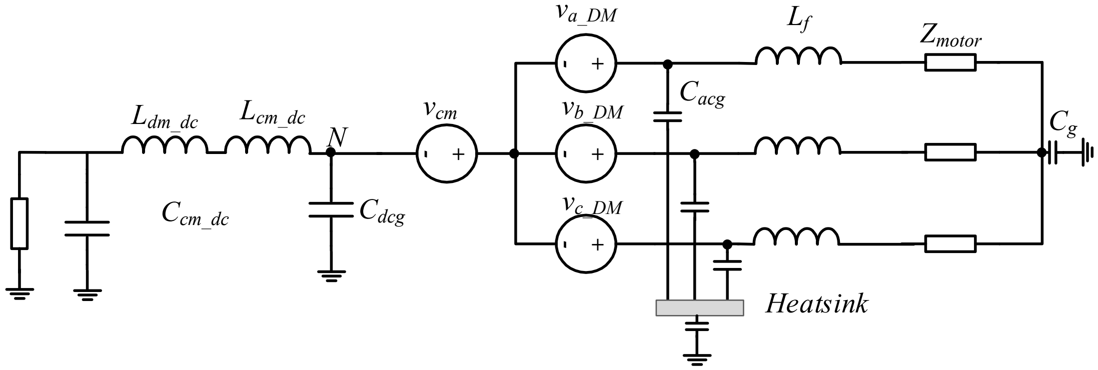


Fig. 6-2. General equivalent circuits for ac outputs of three-phase converter systems.

$$\begin{cases} v_{CM} = \left(v_{aN} + v_{bN} + v_{cN}\right)/3 \\ v_{a\_DM} = v_{aN} - v_{CM} \\ v_{b\_DM} = v_{bN} - v_{CM} \\ v_{c\_DM} = v_{cN} - v_{CM} \end{cases} \tag{6.3}$$

With synthesized switching functions, a general ac side equivalent circuit is given in Fig. 6-2. The general equivalent circuits shown in Fig. 6-2 are not only validated for the ANPC converter but are also effective for all other three-phase inverter topologies. The controlled voltage sources are used to represent the CM and DM voltage with the synthesized functions, and both DM and CM currents on the ac side are acquired, but only the CM current can be obtained on the dc side.

The equivalent circuits in Fig. 6-2 cannot solve the dc side DM current. To further get DM current in the dc side for the three-phase inverter system, an extra equivalent circuit must be built to get the dc side input current. For the ANPC converter, dc side input currents have two free variables, positive bus current i_{dc1} and neutral wire current i_{dc2}, and the negative bus current can be derived using i_{dc1} and i_{dc2}. Hence, the dc input side can be modeled as two controlled current sources as shown in Fig. 6-3, and i_{dc1} and i_{dc2} can be expressed with the switching function as:

$$\begin{cases} i_{dc1} = \left(s_{a1}s_{a2}i_a + s_{b1}s_{b2}i_b + s_{c1}s_{c2}i_c\right) \\ i_{dc2} = \left(s_{a2}s_{ap} + s_{a3}s_{an}\right)i_a + \left(s_{b2}s_{bp} + s_{b3}s_{bn}\right)i_b + \left(s_{c2}s_{cp} + s_{c3}s_{cn}\right)i_c \end{cases} \tag{6.4}$$

where i_a, i_b and i_c are the ac side output currents for three phases.

For two-level VSC, the dc input side can be modeled by only using one current source due to no existence of the neutral wire. To extend the general form of dc input side equivalent circuits, as shown in Fig. 6-4, two common topologies in motor drive applications, flying capacitor clamped and diode clamped multi-level converters, are considered. For ac side, they both can be modeled by using the equivalent circuits in Fig. 6-2. For dc-side, the dc input current of flying capacitor clamped multi-level converter is only determined by the switching actions of the top switch at each phase, and its equivalent circuits are as same as the two-level VSC shown in Fig. 6-5(a). As a result, the expression of i_{dc} in Fig. 6-5(a) is generalized as:

$$i_{dc} = \sum_{i=a,b,c} i_i s_{i\_top} \tag{6.5}$$

where s_{i_top} is the modulation signal of the top switch at phase i.

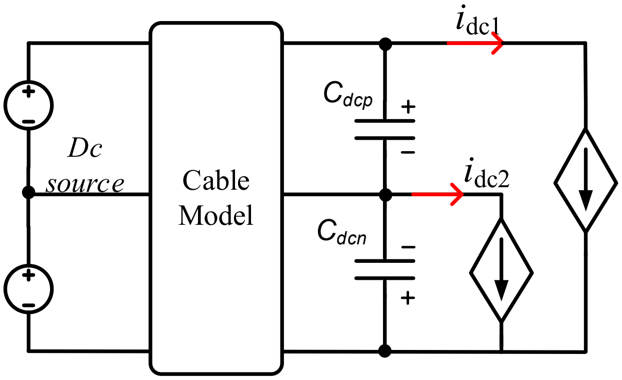
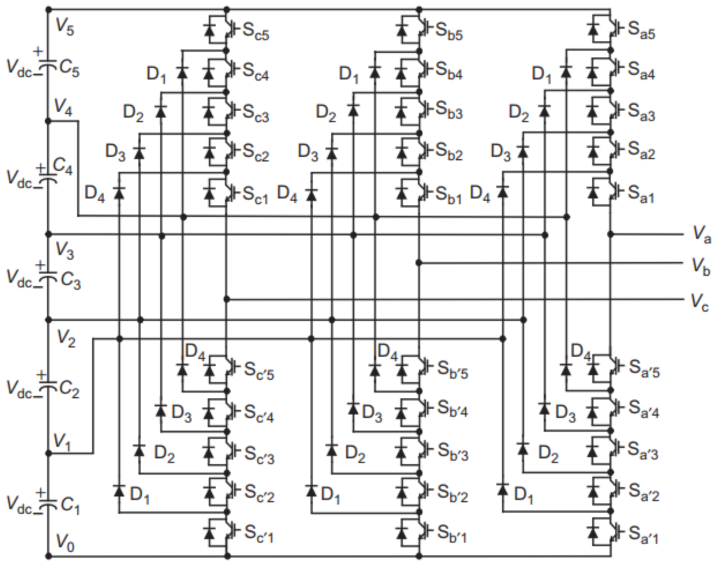
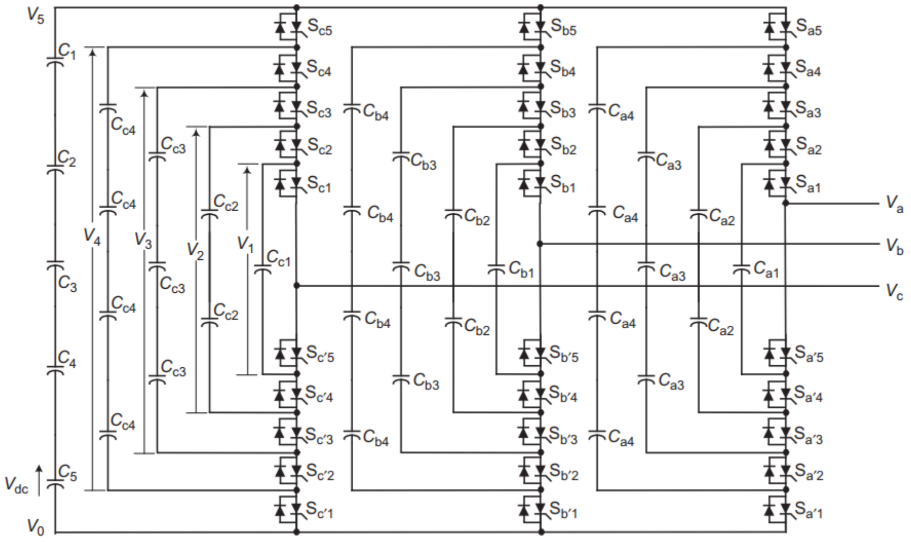


Fig. 6-3. Dc input side equivalent circuits for ANPC converter.

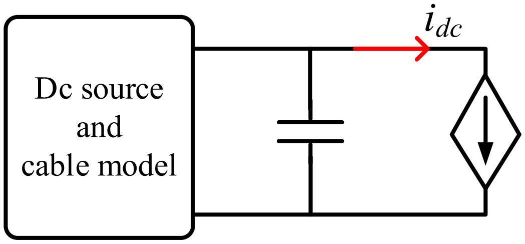

V5
Vdc
C5
V4
Vdc
C4
V3
Vdc
C3
V2
Vdc
C2
V1
Vdc
C1
V0
D1
D2
D3
D4
Sc5
Sc4
Sc3
Sc2
Sc1
Sb5
Sb4
Sb3
Sb2
Sb1
Sa5
Sa4
Sa3
Sa2
Sa1
Va
Vb
Vc
Sc'5
Sc'4
Sc'3
Sc'2
Sc'1
Sb'5
Sb'4
Sb'3
Sb'2
Sb'1
Sa'5
Sa'4
Sa'3
Sa'2
Sa'1

(a) Diode clamped multi-level converter

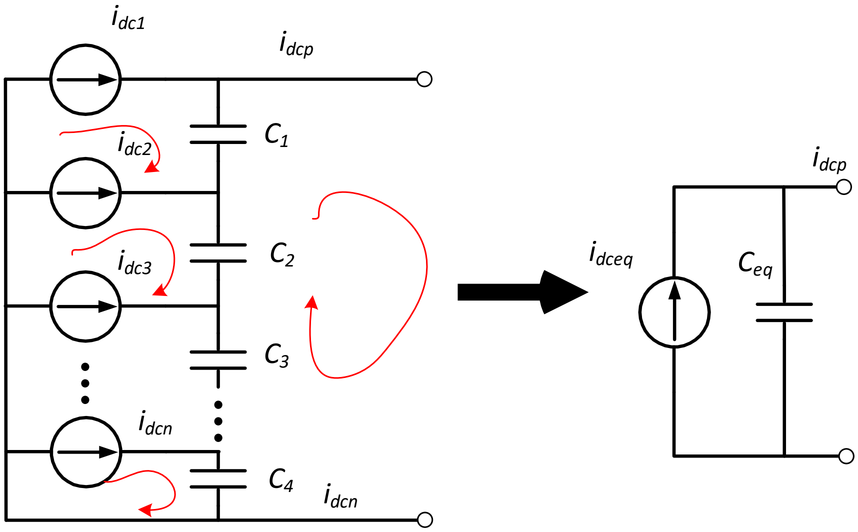

V5
C1
C2
C3
C4
Vdc
C5
V0
V4
V3
V2
V1
Cc4
Cc3
Cc2
Cc1
Cb4
Cb3
Cb2
Cb1
Ca4
Ca3
Ca2
Ca1
Sc5
Sc4
Sc3
Sc2
Sc1
Sb5
Sb4
Sb3
Sb2
Sb1
Sa5
Sa4
Sa3
Sa2
Sa1
Va
Vb
Vc
Sc'5
Sc'4
Sc'3
Sc'2
Sc'1
Sb'5
Sb'4
Sb'3
Sb'2
Sb'1
Sa'5
Sa'4
Sa'3
Sa'2
Sa'1

(b) Flying capacitor clamped multi-level converter

Fig. 6-4. Two multi-level topologies for a three-phase converter system in [153].



(a) Dc side equivalent circuits for flying capacitor clamped converter



(b) Dc side equivalent circuits for diode clamped converter

Fig. 6-5. General dc side equivalent circuits for multi-level converters.

It is difficult to model the dc input current of diode clamped converters with the switching function controlled current sources shown in Fig. 6-4(b) since the required number of controlled current sources varies with the number of voltage levels. It needs to manually change the simulation circuits when the voltage level changes. To avoid a laborious change of simulation circuits, a further simplified equivalent circuit similar to the two-level VSC is proposed. By applying Norton's theorem, the complicated equivalent circuits involving multiple controlled current sources are simplified as one current source with an internal impedance as shown in Fig. 6-5(b).

When shorting the two terminals in Fig. 6-5(b), the equivalent current i_{dceq} and capacitance C_{eq} with the Loop Current Method is derived as:

$$\begin{cases} i_{dceq} = i_{dc1} + \dfrac{n-1}{n} i_{dc2} + \dfrac{n-2}{n} i_{dc3} + \ldots + \dfrac{1}{n} i_{dcn} \\ i_{dcn} = \begin{cases} \sum\limits_{i=a,b,c} [s_{i\_n+1} - s_{i\_n}] i_i \quad when\ i_{phase} > 0 \\ \sum\limits_{i=a,b,c} [s_{i\_n} - s_{i\_n+1}] i_i \quad when\ i_{phase} < 0 \end{cases} \\ C_{eq} = C_{fly} / n \end{cases} \tag{6.6}$$

where n is the number of voltage levels, i_{dcn} is the current value of the *nth* current source, C_{fly} is the capacitance value of the flying capacitor.

To demonstrate the simulation time reduction of the switching function based simulations, a comparison study is conducted in the Simulink with switches based simulations and switching function based simulations. The simulation time is measured with “tic” and “toc” functions in the MATLAB, and the time step for Power GUI inside Simulink is set as 2e-8 for Simscape electrical specialized power system models in terms of EMI noise prediction while the global simulation is set as variable time step and the maximum time step is 1e-6 for remaining control and signal function blocks. The simulation time is six line cycles, and ode23tb is selected as the solver for differential equations.

The simulation time comparisons for three topologies are given in Fig. 6-6. Specifically, switching function based simulation can reduce the execution time by 38.72% for the three-level ANPC case compared with switches based simulation. Moreover, more switches involved in the simulation, more execution time can be decreased.

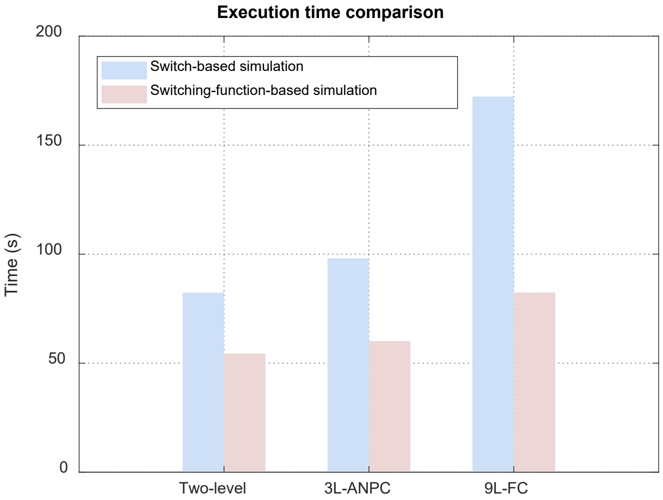


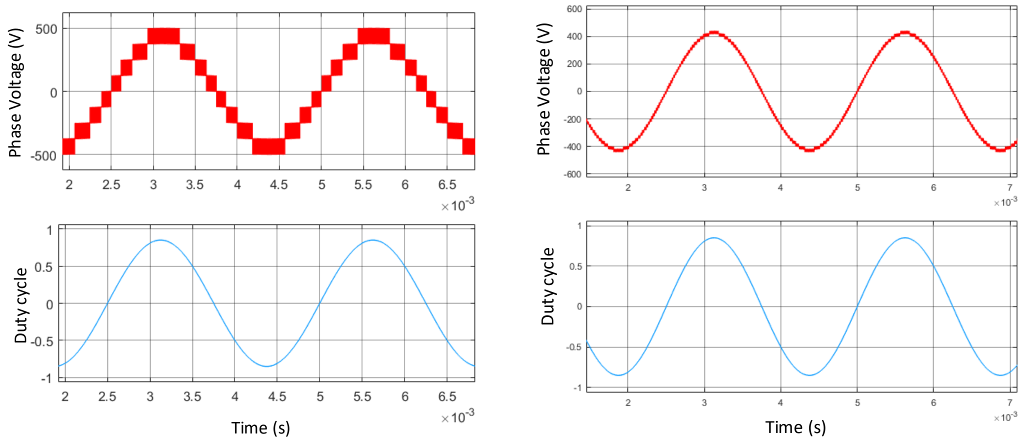
Fig. 6-6. Simulation time comparison for three topologies.

6.2 Current Waveforms Synthesis for Components Design

As examples shown in Fig. 6-7, for multi-level topologies, the phase voltage can be synthesized for the arbitrary voltage levels with switching functions. However, owing to the nonexistence of real circuits and related components in the simulation, switching function based simulations cannot provide current waveforms of passive components or switches for the electrical and physical design.

To get current waveforms for components design, the analytical solutions combined with switching functions and phase currents are derived. In this section, by using the flying capacitor clamped topology as an example, current waveforms synthesis for flying capacitance design and device loss calculation are illustrated with the proposed solution.

For the flying capacitance design, the typical switching cell in flying capacitor clamped topology is given in Fig. 6-8. The current of flying capacitor C_{fly_n} is determined by the switching signals of neighboring four switches. s_{u_n-1} and s_{l_n-1} are the upper and low side switch for the *(n-*



(a). 9 voltage levels (b). 51 voltage levels

Fig. 6-7. Phase voltage synthesis for multi-level converters.

$1)_{th}$ switching cell, and s_{u_n} and s_{l_n} are the upper and low side switch for the n_{th} switching cell. The flying capacitor current i_{fly_n} can be expressed as:

$$i_{fly\_n} = (s_{u\_n-1} \cdot s_{l\_n} - s_{l\_n-1} \cdot s_{u\_n}) \cdot i_{ph} \tag{6.7}$$

where i_{ph} is the phase current.

With the derived i_{fly_n}, the time domain voltage of the flying capacitor is further obtained by Eq. (6.8). Assuming a reasonable voltage ripple constraint, the desirable flying capacitance can be calculated.

$$u_{fly\_n}(t) = \frac{1}{C_{fly\_n}} \int_0^t i_{fly\_n}(t)dt \tag{6.8}$$

For the device loss calculation, the current for one switch s_{u_n} can be derived as:

$$i_{su\_n} = s_{u\_n} i_{ph} \tag{6.9}$$

With the derived switch's current, the conduction loss and switching loss can be calculated based on the definition. For the switching loss calculation, the phase current direction should be

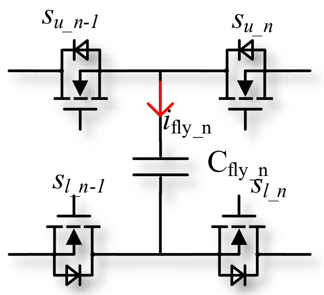


Fig. 6-8. Switching cell in flying capacitor clamped topology.

paid attention to. For the upper side devices in one phase-leg, the turn-on and turn-off losses are zero if the phase current is from the load side to the phase-leg mid-point due to zero-voltage switching. Similarly, for the lower side devices in one phase-leg, the turn-on and turn-off losses are zero if the phase current is from phase-leg mid-point to the load side.

6.3 THD Evaluation with Motor Model

Power quality is one concern in motor drive applications, and total harmonics distortion (THD) is adopted to evaluate the power quality. Depending on requirements for different types of motors, a sine wave filter may be required to suppress current harmonics. Hence, how to evaluate THD accurately with the motor load is critical.

The most convenient way is to use an LR equivalent circuits plus a back electromotive force (back EMF) for a simplified motor model. However, such a simplified model cannot reflect the current harmonics for some specific types of motors. E.g., synchronous machines with the salient pole rotor structure have varying self-phase inductances during one line cycle instead of a fixed phase inductance. Also, the damper winding can contribute to current harmonics. Therefore, high-order dynamic models for different types of motors in the Simulink library are applied for the evaluation.

To avoid the implementation of complex motor control and the design of control parameters, open-loop schemes are adopted to start a motor to achieve the steady-state operating waveforms. For different types of motors, the open-loop schemes for starting a machine are different. Here open-loop schemes for synchronous machines and permanent magnet synchronous machines are illustrated.

For a synchronous machine, the open-loop scheme is given in Fig. 6-9. After starting the synchronous machine, the excitation voltage will not be applied to the field winding and the mechanical power is set to zero. The motor is operated in the way like an induction machine with currents induced in the damper and field windings. To suppress the induced voltage across the field winding and field current, the field current multiplying a gain are applied in the field winding to represent a resistor across the field winding. Then when rotor speed reaches a threshold value near the synchronous speed, the nominal excitation voltage will be applied in the field winding and the rotor will synchronize with the line frequency. In the meantime, the full mechanical power is also enabled with a ramp signal from zero. The whole starting waveforms are given in Fig. 6-10, and the steady-state waveforms near the end of the simulation are used for THD calculation.

Fig. 6-11 shows the steady-state waveforms and FFT analysis results. In this case, the line frequency is 167 Hz and the switching frequency is 16.7 kHz. From the FFT analysis shown in Fig. 6-11(b), the current harmonics at switching frequency and sideband harmonics contribute main THD, and THD is 3.41%.

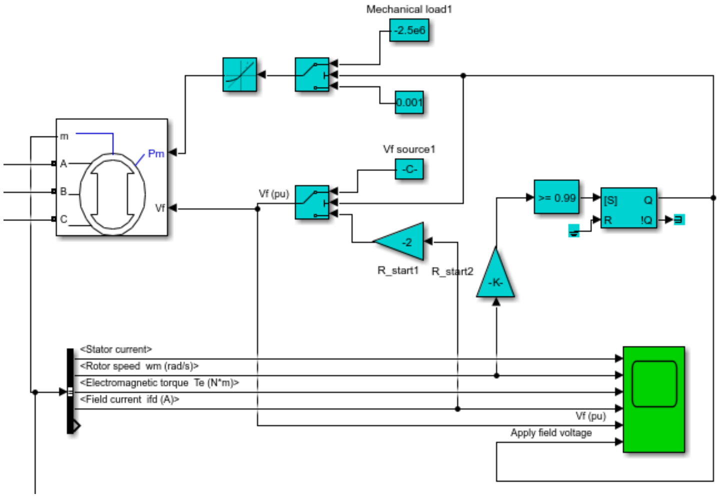

Mechanical load1
-2.5e6
0.001
m
A
B
C
Pm
Vf
Vf source1
-C-
Vf (pu)
>= 0.99
[S]
R
Q
!Q
-2
R_start1
R_start2
-K-
<Stator current>
<Rotor speed wm (rad/s)>
<Electromagnetic torque Te (N*m)>
<Field current ifd (A)>
Vf (pu)
Apply field voltage

Fig. 6-9. Open-loop scheme for starting a synchronous machine.

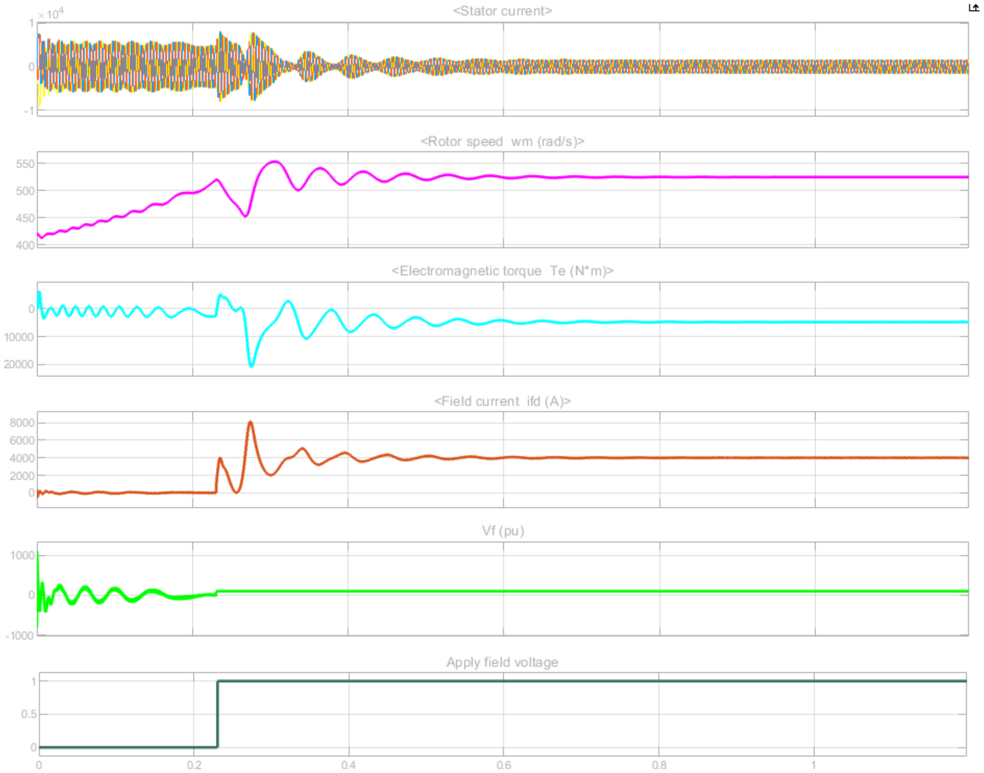
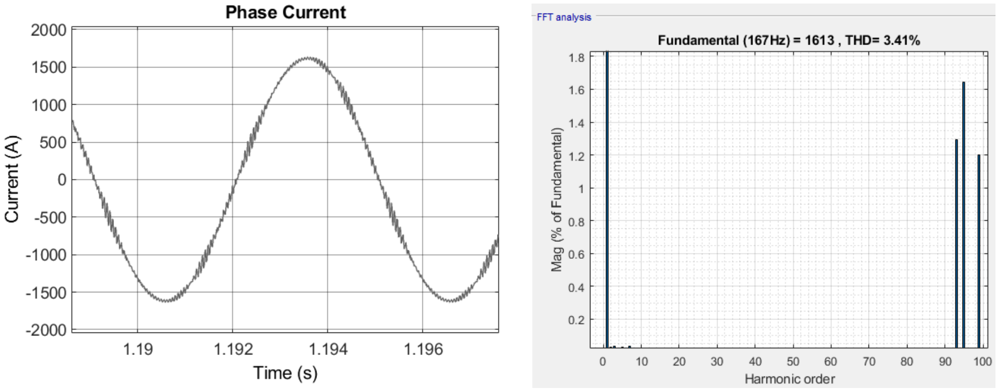


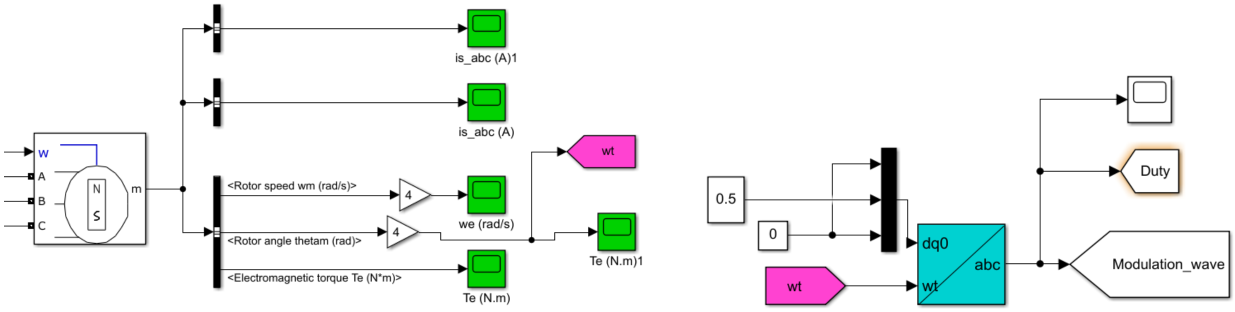
Fig. 6-10. Synchronous machine open-loop simulation waveforms.



(a). Steady-state waveforms (b). FFT analysis

Fig. 6-11. THD evaluation with steady-state operating waveforms in the open-loop simulation.

Fig. 6-12 gives the open-loop scheme for the permanent magnet synchronous machine (PMSM). The main difference compared with SM is field flux cannot be controlled and PMSM cannot work in the induction machine mode during start-up, so the rotor electrical angle is measured and fed back to duty cycle reference. Also, the load for the motor is changed from a mechanical power load to a constant speed load. As a result, the system synchronization between the stator and the rotor is realized by the feedback of the rotor electrical angle. Then, as shown in Fig. 6-12(b), the duty cycle reference is created in dq-axis rotor synchronous frame with the rotor electrical angle. To achieve an approximate zero d axis current control performance, the d axis duty cycle is set to zero, and q axis duty cycle is set to control the output power and phase voltage amplitude. Fig. 6-13 gives the simulation waveforms for the open-loop simulations of PMSM, and the steady-state current waveforms can be used for THD calculation.


is_abc (A)1
is_abc (A)
w
A
B
C
N
S
m
<Rotor speed wm (rad/s)>
4
we (rad/s)
<Rotor angle thetam (rad)>
4
<Electromagnetic torque Te (N*m)>
Te (N.m)
wt
Te (N.m)1
0.5
0
wt
dq0
abc
wt
Duty
Modulation_wave

(a). Motor model (b). Duty cycle reference

Fig. 6-12. Open-loop scheme for starting a permanent magnet synchronous machine.

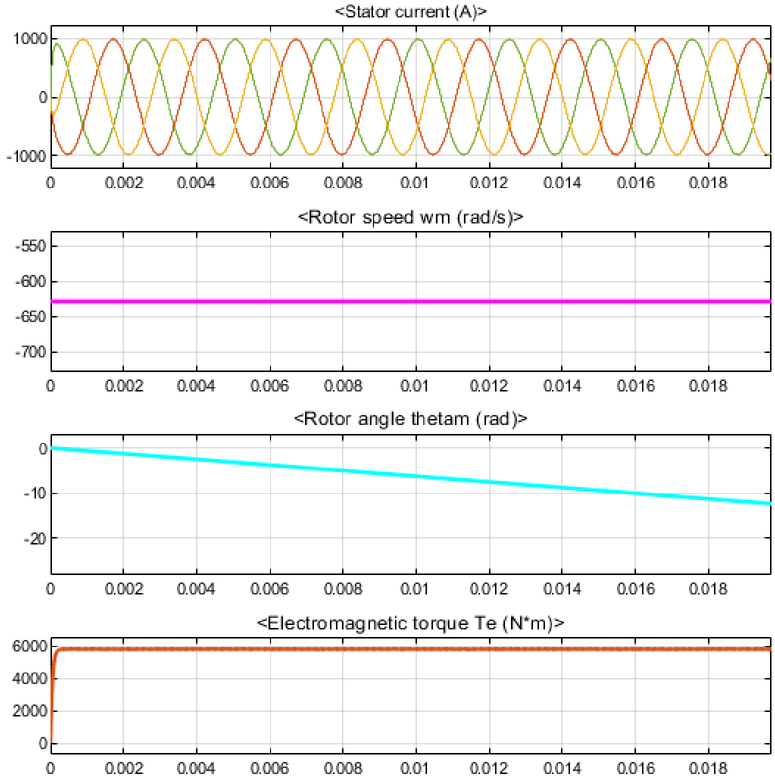


Fig. 6-13. PMSM open-loop simulation waveforms.

6.4 System-level Optimization with Frequency and Modulation Selection

6.4.1 System Iteration Scheme

Fig. 6-14 gives a design diagram for a converter-level design that includes simulation, model and algorithm, and database. Through the simulation, the required raw data and waveforms are obtained for the electrical design and physical design of power electronics components. Models are separated into two blocks. The left block covers the active power switches selection and corresponding cooling design iterations considering the practical power loop layout and switching speed. The right block mainly focuses on passive components design. Also, for each function block, the selected optimization algorithm or iteration loop is applied to search the optimal for the objective. Several databases are built to support the design and provide the discrete commercial components as the inputs of the physical design.

Fig. 6-15 further shows the system-level iteration diagram. In the system level, the design specs, topology, modulation scheme, switching frequency, filter configuration, and converter structure can be treated as design variables. The main purpose of system-level iterations is to search the optimal combination of those system-level design variables. After one converter design is finished, the related design results will be saved in the design pool. With sweeping all switching frequencies, modulation schemes, dc-link voltages, and other system-level variables, the best design results can be found from the design pool including all the design cases.

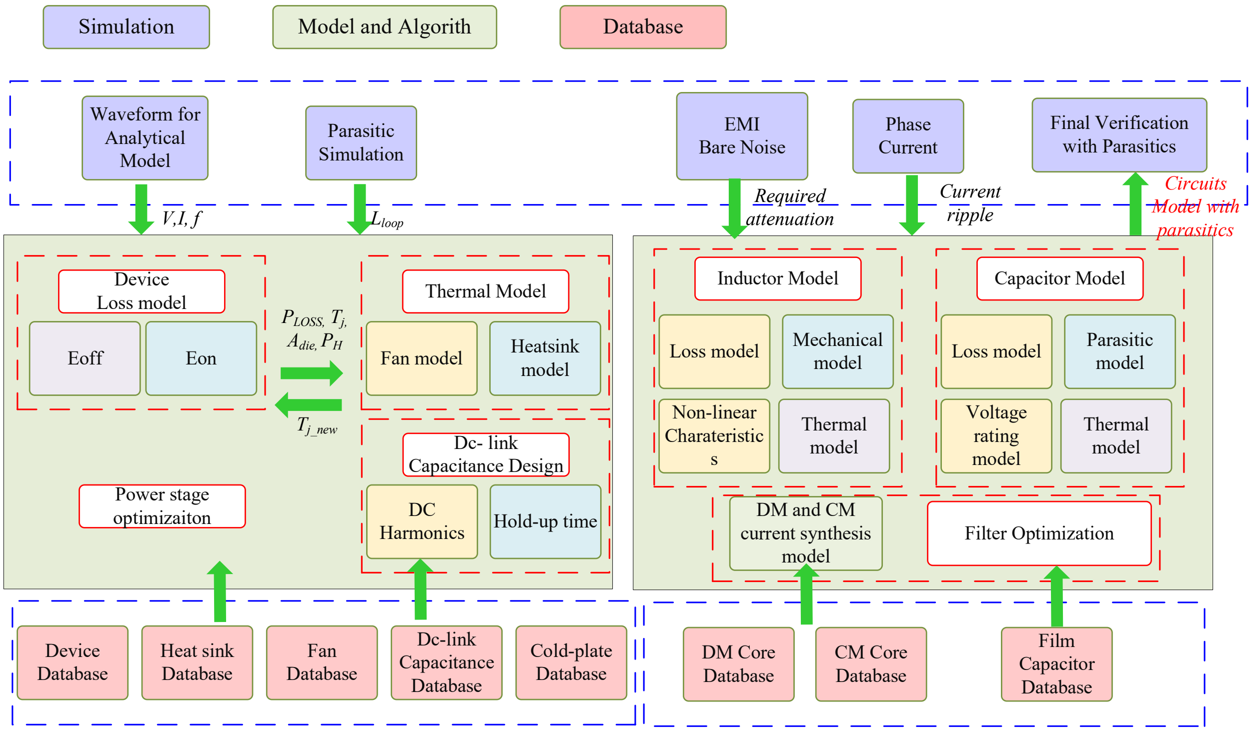

Simulation
Model and Algorith
Database
Waveform for Analytical Model
Parasitic Simulation
EMI Bare Noise
Phase Current
Final Verification with Parasitics
V,I, f
L_{loop}
Required attenuation
Current ripple
Circuits Model with parasitics
Device Loss model
Eoff
Eon
P_{LOSS}, T_j, A_{die}, P_H
T_{j_new}
Thermal Model
Fan model
Heatsink model
Dc- link Capacitance Design
DC Harmonics
Hold-up time
Power stage optimizaiton
Inductor Model
Loss model
Mechanical model
Non-linear Charateristic s
Thermal model
Capacitor Model
Loss model
Parasitic model
Voltage rating model
Thermal model
DM and CM current synthesis model
Filter Optimization
Device Database
Heat sink Database
Fan Database
Dc-link Capacitance Database
Cold-plate Database
DM Core Database
CM Core Database
Film Capacitor Database

Fig. 6-14. Design diagram for the whole converter.

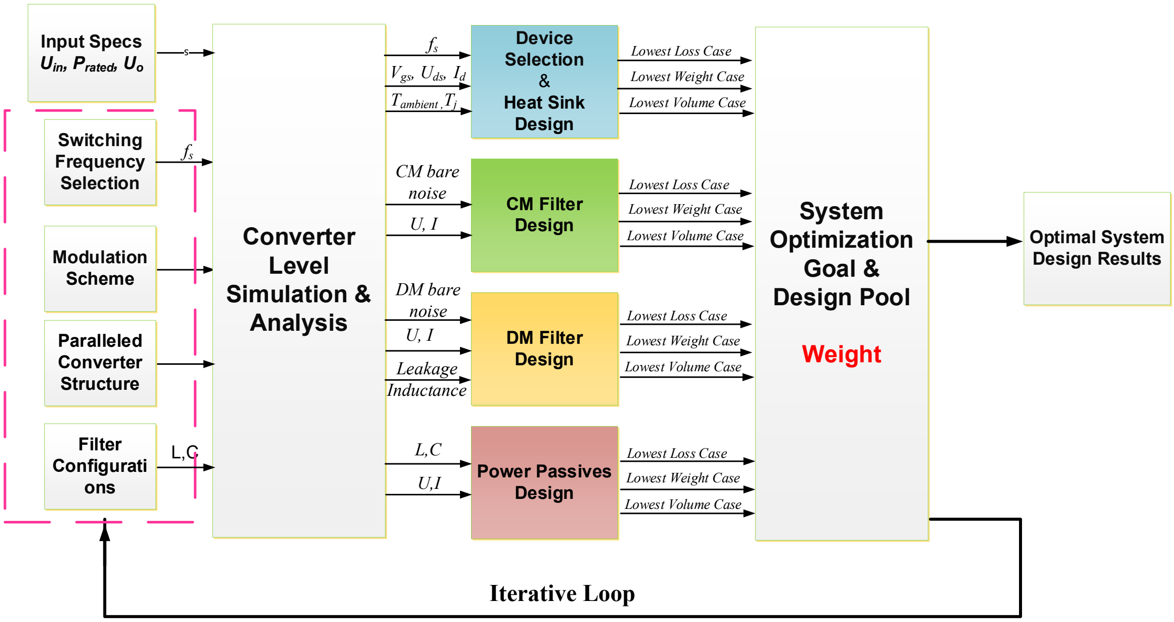

Input Specs U_{in}, P_{rated}, U_o
Switching Frequency Selection
Modulation Scheme
Paralleled Converter Structure
Filter Configurati ons
f_s
L,C
Converter Level Simulation & Analysis
f_s
V_{gs}, U_{ds}, I_d
$T_{ambient}$, T_j
CM bare noise
U, I
DM bare noise
U, I
Leakage Inductance
L,C
U,I
Device Selection & Heat Sink Design
CM Filter Design
DM Filter Design
Power Passives Design
Lowest Loss Case
Lowest Weight Case
Lowest Volume Case
System Optimization Goal & Design Pool
Weight
Optimal System Design Results
Iterative Loop

Fig. 6-15. System-level iteration diagram.

6.4.2 Case Study

One case study with target specs and desired features are listed in Table 6-1. The key requirements are specific power density higher than 10 kW/lb, power efficiency higher than 98%.

The converter structure is given in Fig. 6-16, and three topologies including ANPC, T-type, and two-level voltage source converters are considered. Also, three dc-link voltages including 540 V, 900 V, and 1500 V are adopted for the design for the system weight comparison. In the following, ANPC converter design results will be given first to illustrate how to evaluate the one topology at the system-level with different switching frequencies, dc-link voltages, and modulation methods. Then, a design summary and comparison of the three topologies are given.

Table 6-1. Motor Drive Controller Specification.

System& Environmental	Target density: > 10 kW/lb Target efficiency: >98% Liquid cooling with Propylene Glycol and Water Mixture
Electrical & Functional	Power: 500 kW High Voltage DC Power Input: 540 V, 900 V, 1500 V AC output: 3-phase AC power (modulation index 1.1) AC frequency: 1 kHz Meet EMI requirement (DO-160) in dc side, no EMI filter in ac side Requirement of dv/dt limitation: 0.5 V/ns Control, sensor and protection included
Desired Features	Use SiC MOSFET Robust and reliable for use at a high vibration and high altitude environment

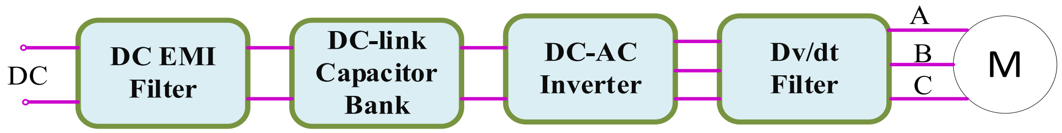


Fig. 6-16. Power architecture of the motor drive controller.

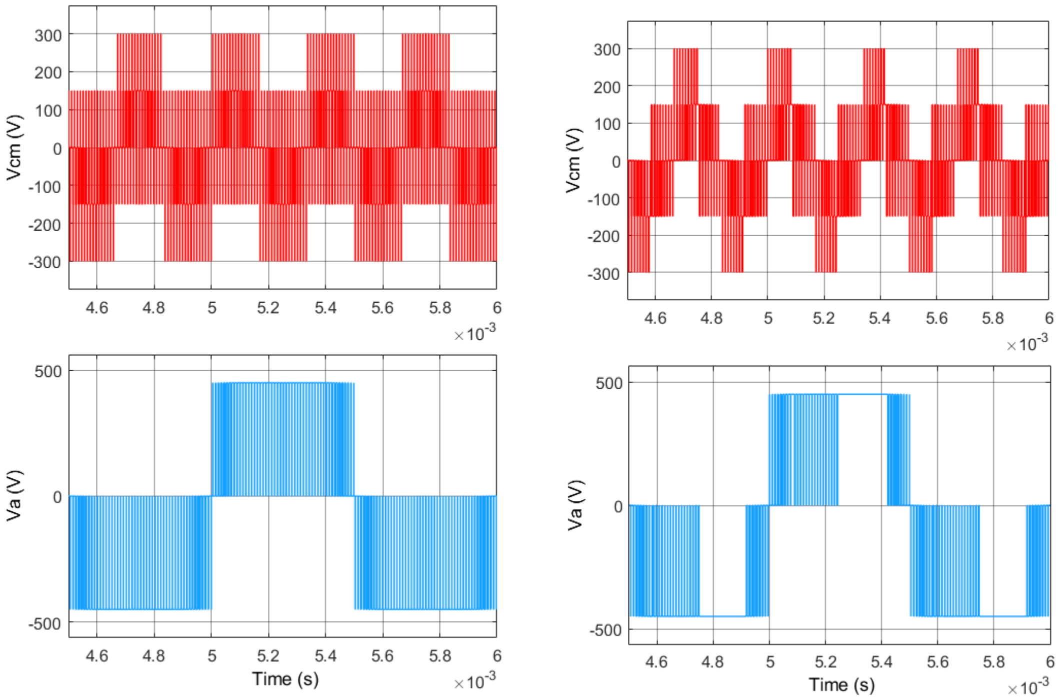
A. ANPC Converter Design Results

SVM, DPWM, CMR are chosen for the ANPC converter design. Fig. 6-17 shows the waveforms of CM voltage and phase voltage with three different modulation schemes. From Fig. 6-17(b) and (c), both DPWM and CMR modulation can help reduce the switching actions and loss compared with SVM modulation shown in Fig. 6-17(a). Also, CMR can reduce the peak amplitude of CM voltage from 300 V to 150 V shown in Fig. 6-17(c) compared with DPWM and SVM.

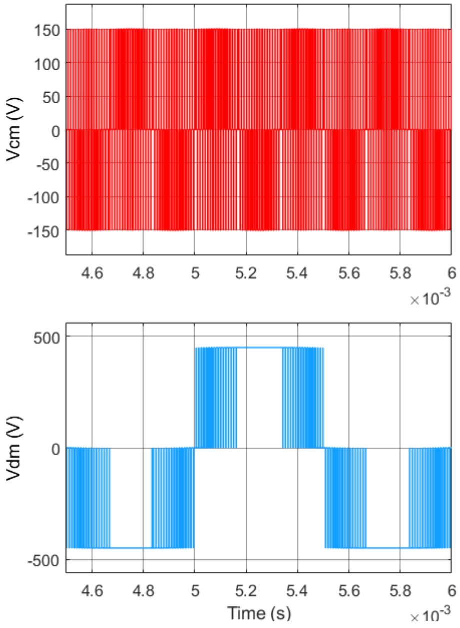
The voltage rating of power devices applied in APNC is the half of dc-link voltage, and the required voltage rating of devices in 540 V dc-link is only 270 V, which far blows the minimum voltage rating of SiC MOSFETs (650 V – 900 V). Hence, 540 V will not be used for the design of ANPC converters, and only 900 V and 1500 V are used as the dc-link voltages for the design.

Fig. 6-18, Fig. 6-19, and Fig. 6-20 shows the design results of ANPC with different modulation methods. For each switching frequency, from left to right, the bar charts give the weight breakdown information for 900 V and 1500 V respectively. For all modulation schemes, the design results of ANPC at 900 V shows a lower total converter weight than one at 1500 V for most switching frequencies. The reason is that 900 V dc-link voltage can enable the use of the state-of-art 900 V SiC power module for high current application with ultra-low on resistance, while, for 1500 V dc-link, 1.2 kV and 1.7 kV power devices have to be paralleled for such a high power application leading to heavier device and heatsink weight. Also, CM noise becomes higher in 1500 V compared with one in 900 V, leading to a heavier CM filter design.

The weight of dc-link capacitors is mainly decided by the dc-link voltage. The higher dc-link voltage is, the lighter the weight of dc-link capacitors is. This is because the dc-link capacitance is determined by the energy requirement during load change to support the dc-link. The higher dc-



(a) SVM (b) DPWM



(c) CMR

Fig. 6-17. Waveforms of CM voltage and phase voltage with different modulations.

link voltage can reduce the requirement of the dc-link capacitance since the energy of capacitors is quadratic with the voltage applied in capacitors but linear with the capacitance.

High switching frequency did not show any benefits to reduce the weight of *dv/dt* filter since the corner frequency of *dv/dt* filter is around 200 kHz, which is beyond switching frequency. On the contrary, the high switching frequency current ripple may increase the core loss and winding loss, leading to a larger core size and heavier weight.

Fig. 6-21 gives weight comparisons with different modulations at 900 V dc-link. The weight of EMI filter weight with CMR or DPWM is lower than that with SVM, and it demonstrated that CMR can help reduce CM noise and the weight of CM filters. Also, both CMR and DPWM have fewer switching actions and less power loss, resulting in a lighter cooling system compared with one with SVM modulation.

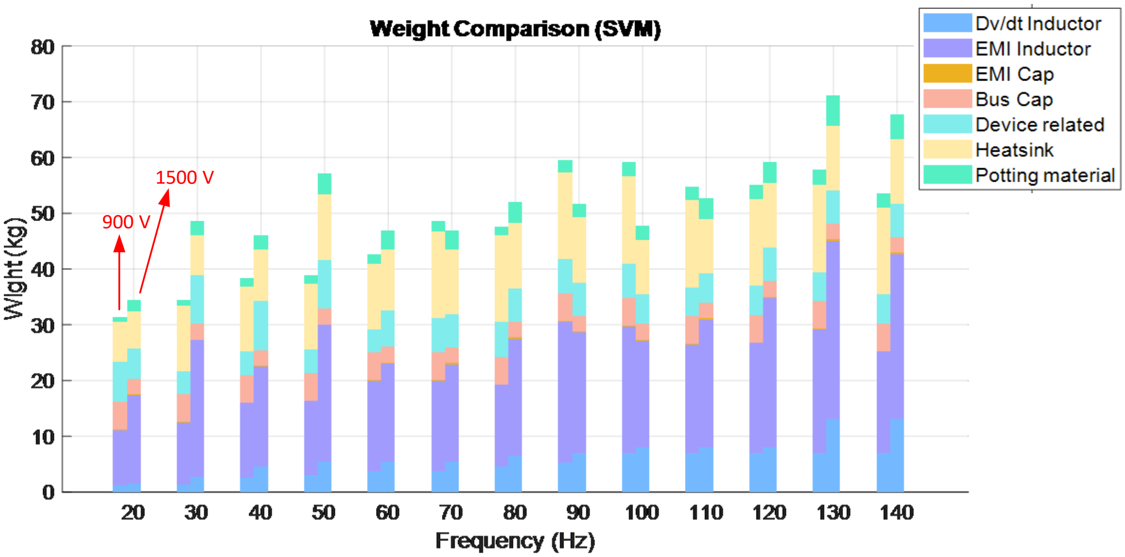


Fig. 6-18. Design results for three-level ANPC with SVM and single-stage EMI filter.

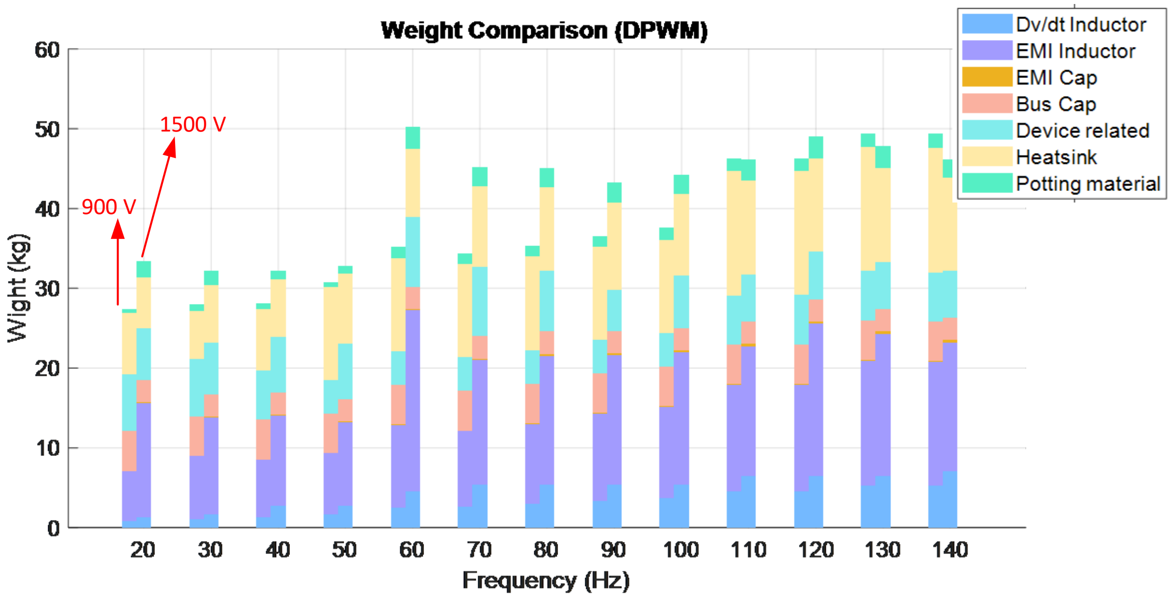


Fig. 6-19. Design results for three-level ANPC with DPWM and single-stage EMI filter.

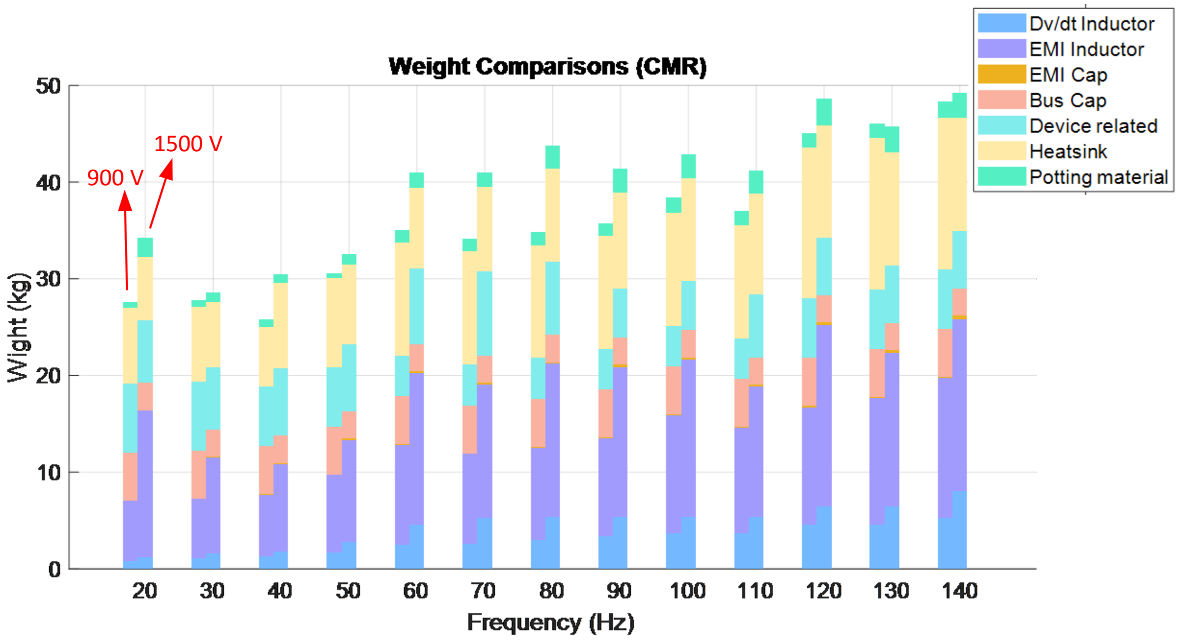


Fig. 6-20. Design results for three-level ANPC with CMR and single-stage EMI filter.

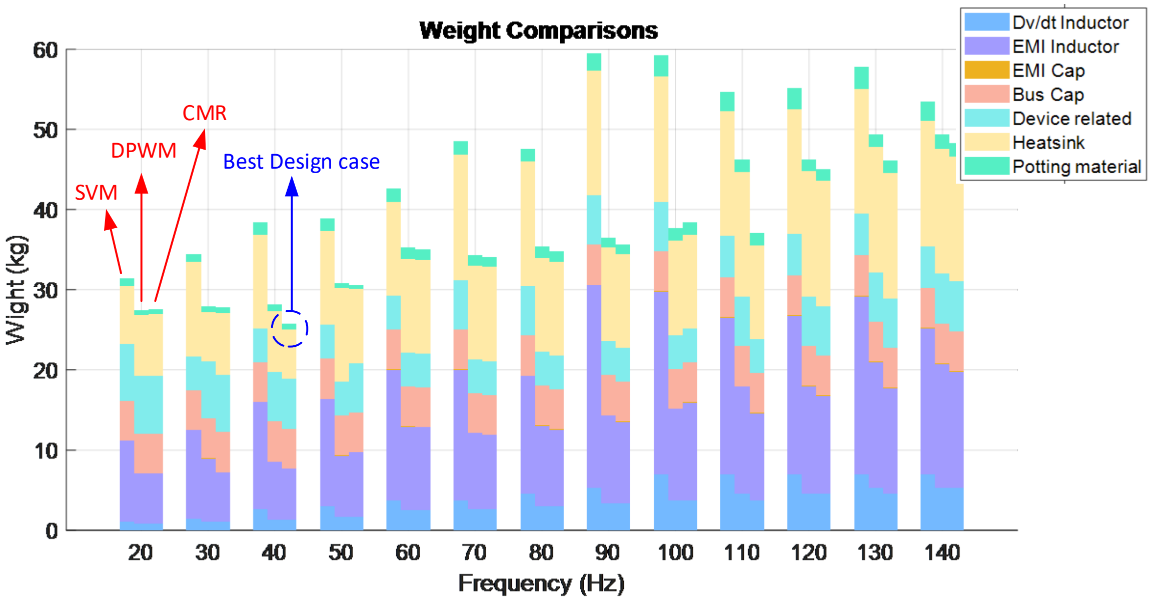


Fig. 6-21. Design comparison for three-level ANPC with the single-stage EMI filter at 900 V.

Fig. 6-22 and Fig. 6-23 further gives the design results with two-stage EMI configurations. From the weight comparisons, the two-stage EMI filter configuration did not show a weight reduction trend compared with a single-stage EMI filter configuration. The main reason is that the minimum core size is mainly determined by the window area of cores in the high inductor current case. For this design at 500 kW, the average current of the dc side is from 350 A – 930 A for different dc-link voltages. Hence, the large diameter of wires limits the selection of core sizes even though the inductance in two-stage EMI filter configuration is smaller than that in single-stage EMI filter configuration.

For all design results, the best design case of three-level ANPC is 40 kHz, CMR modulation with a single-stage EMI filter configuration.

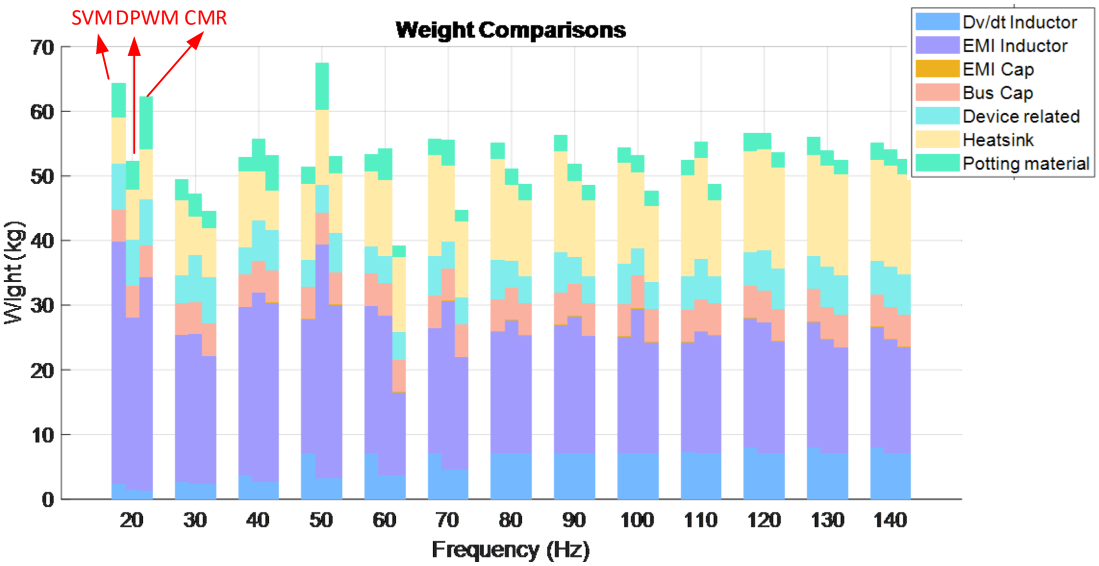


Fig. 6-22. Design comparison for three-level ANPC with the two-stage EMI filters at 900 V.

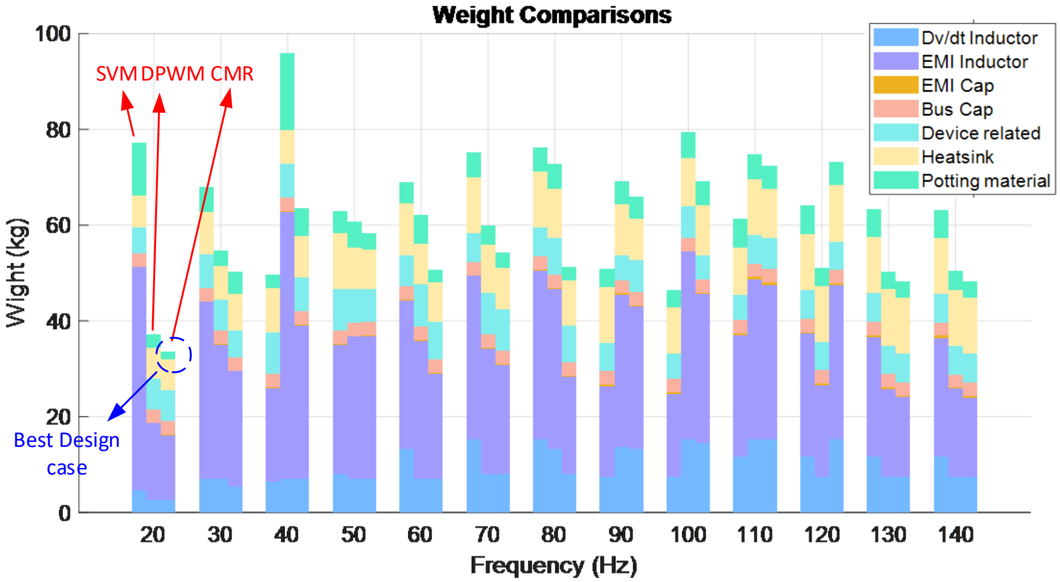


Fig. 6-23. Design comparison for three-level ANPC with the two-stage EMI filters at 1500 V.

B. Design Comparison of Three Topologies

Design comparisons of three basic topologies at 900 V dc-link with individual best modulation scheme is shown in Fig. 6-24. From the comparison, three-level topologies design results including ANPC and T-type achieve the lower total converter weight than that of two-level VSC design results, and main weight reduction is in the EMI filter and *dv/dt* filter part. More control freedom is realized with the help of spare reductant zero vectors in the modulation of three-level converters. In this design, CMR is chosen as the best modulation due to both switching loss reduction and CM mode voltage reduction, helping decrease the weight of the cooling system and EMI filter weight.

To compare with ANPC and T-type, they have similar weight at low switching frequency range. However, if looking at the weight breakdown of bar charts, the weight distribution is not the same. The weight of the dc-link capacitor and EMI filters are the same, while the individual weight of the device and heatsink is quite different. ANPC requires more power switches than T-type, so the device weight of the ANPC converter is heavier than that of the T-type converter. Since T-type needs two dc-link voltage rated power devices whereas ANPC not, the high switching loss with higher voltage rating devices results in a heavier weight of the heatsink in T-type converter compared with one in ANPC.

Fig. 6-25 is given to compare all design results in terms of the trade-off between the total weight and efficiency. Although ANPC and T-type converter can achieve similar total weight, the design results of the ANPC converter have higher efficiency compared with that of the T-type converter. As a result, the best design result of the ANPC converter is selected as the most promising candidate for this application.

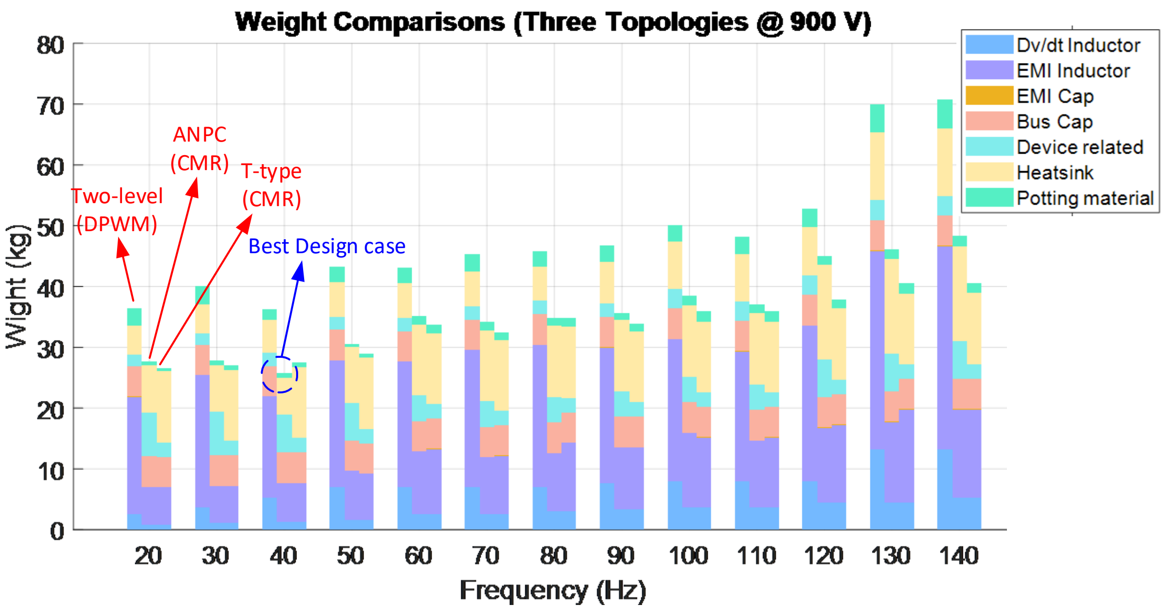


Fig. 6-24. Design comparison for three basic topologies at 900 V.

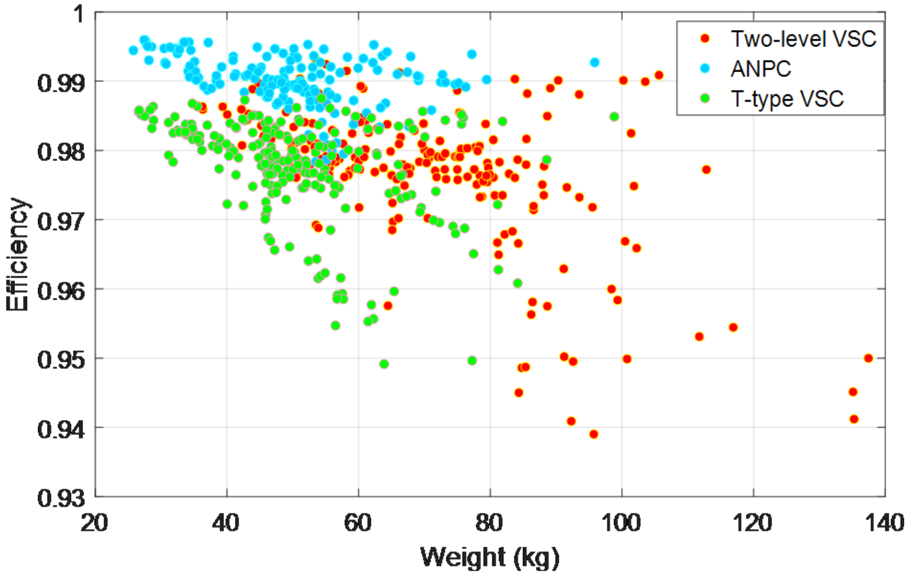


Fig. 6-25. All design results of three basic topologies.

6.5 Design Routine for Paralleled Converters

Converters in parallel is a potential option to reduce the total converter system weight in high power applications since the interleaving scheme can be applied to reduce the weight of passive components. However, it requires additional coupled inductors to suppress the high frequency circulating current between paralleled converters. Hence, there are trade-offs for the selection of the interleaving angle and the coupled inductance. In this section, design strategies for paralleled converters are presented and a case study for two converters in parallel is given for comparing with the best single converter design in Section 6.4.2.

6.5.1 Design Strategies for Interleaving Angle and Coupled inductance

Compared with the single converter design, converters in parallel enable more design freedoms with the interleaving scheme. The first one is the interleaving angle between two paralleled converters, and a phase shift is applied for two carrier waveforms of two paralleled converters. The interleaving angle of the phase shift can be varied from 0° to 180°, leading to different phase voltages and circulating current. There is a trade-off of interleaving angle selection between the harmonics (or noise cancellation) and circulating current. The large interleaving angle like 180° can achieve the minimum harmonics and switching noise but results in high switching frequency circulating current due to the volt-seconds difference between phase legs in different converters.

To relieve this issue, coupled inductors are inserted between the same phases to suppress circulating current shown in Fig. 6-26. Therefore, the second design freedom is the current ripple ratio of the peak-peak circulating current ripple over the peak phase current, leading to the different required coupled inductance. The small current ripple ratio requires a large coupled inductance while the conduction and switching loss of switches in phase legs could be reduced. On the contrary, the high current ripple ratio can lead to a small coupled inductance but higher switching loss and conduction loss for power switches.

Three different interleaving angles are illustrated in Fig. 6-27, which are 20°, 60°, and 180°. In Fig. 6-27, v_{a1} and v_{a2} are phase voltages of phase *a* in two paralleled converters before coupled inductors while v_a represents the final phase voltage after coupled inductors. As can be seen, the larger interleaving angle is, the more voltage levels can be achieved in the phase voltage v_a. As a result, 180° interleaving angle can achieve the minimum THD of the phase voltage, which is 23.56%, while THD of the phase voltage with 20° and 60° interleaving angles are 32.04% and 39.89%, respectively.

Different circulating current ripple ratios are illustrated in Fig. 6-28. Similar to the voltage definitions in Fig. 6-27, i_{a1} and i_{a2} are phase currents of phase *a* in two paralleled converters before coupled inductors while i_a represents the total phase current after coupled inductors. As shown in Fig. 6-28, under one specific interleaving angle, the coupled inductance can be designed to achieve different circulating current ripple amplitudes, and the larger coupled inductance leads to a lower amplitude of circulating current ripple.

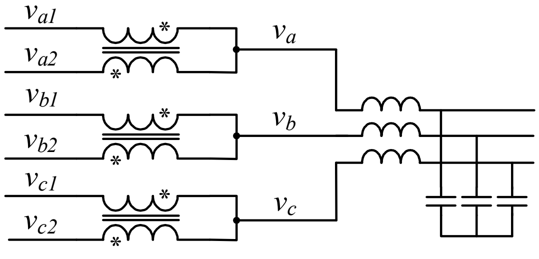
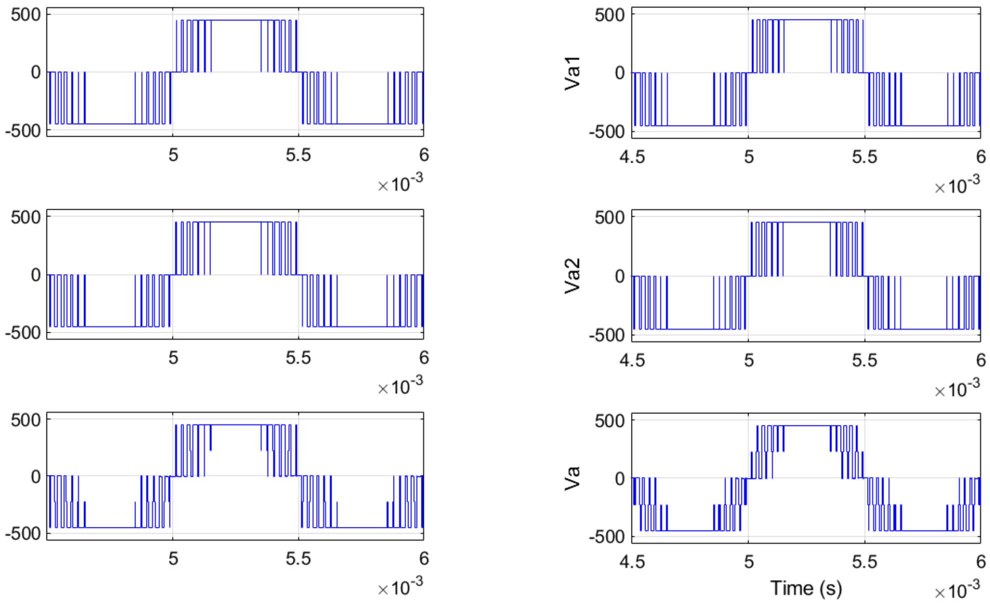
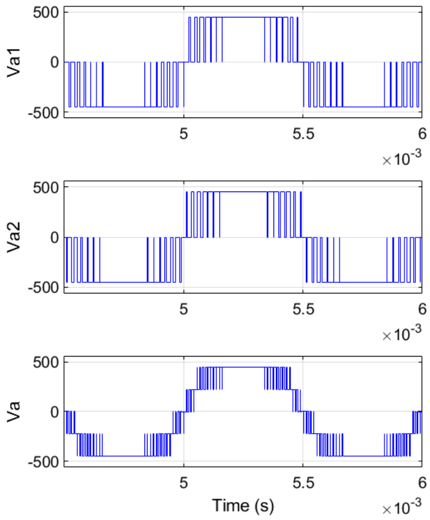


Fig. 6-26. The configuration of coupled inductors in two paralleled converters.

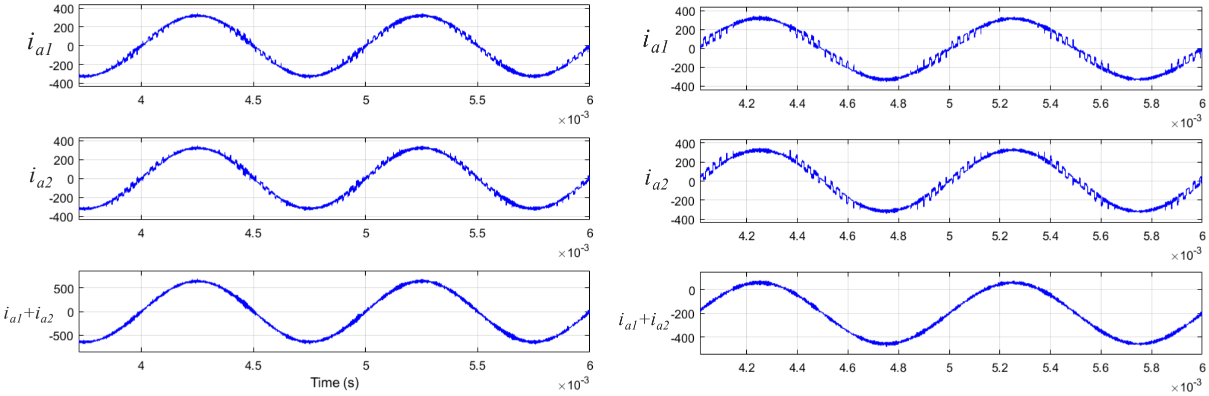


(a) 20° (b) 60°

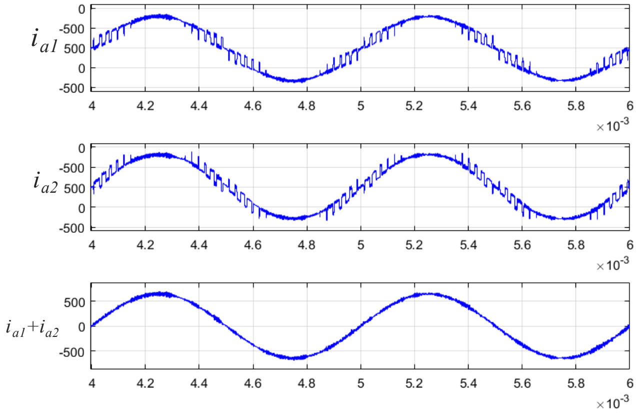


(c) 180°

Fig. 6-27. Waveforms of phase voltage with different interleaving angles



(a) 0.1 (b) 0.2



(c) 0.3

Fig. 6-28. Waveforms of phase current with different current ratios.

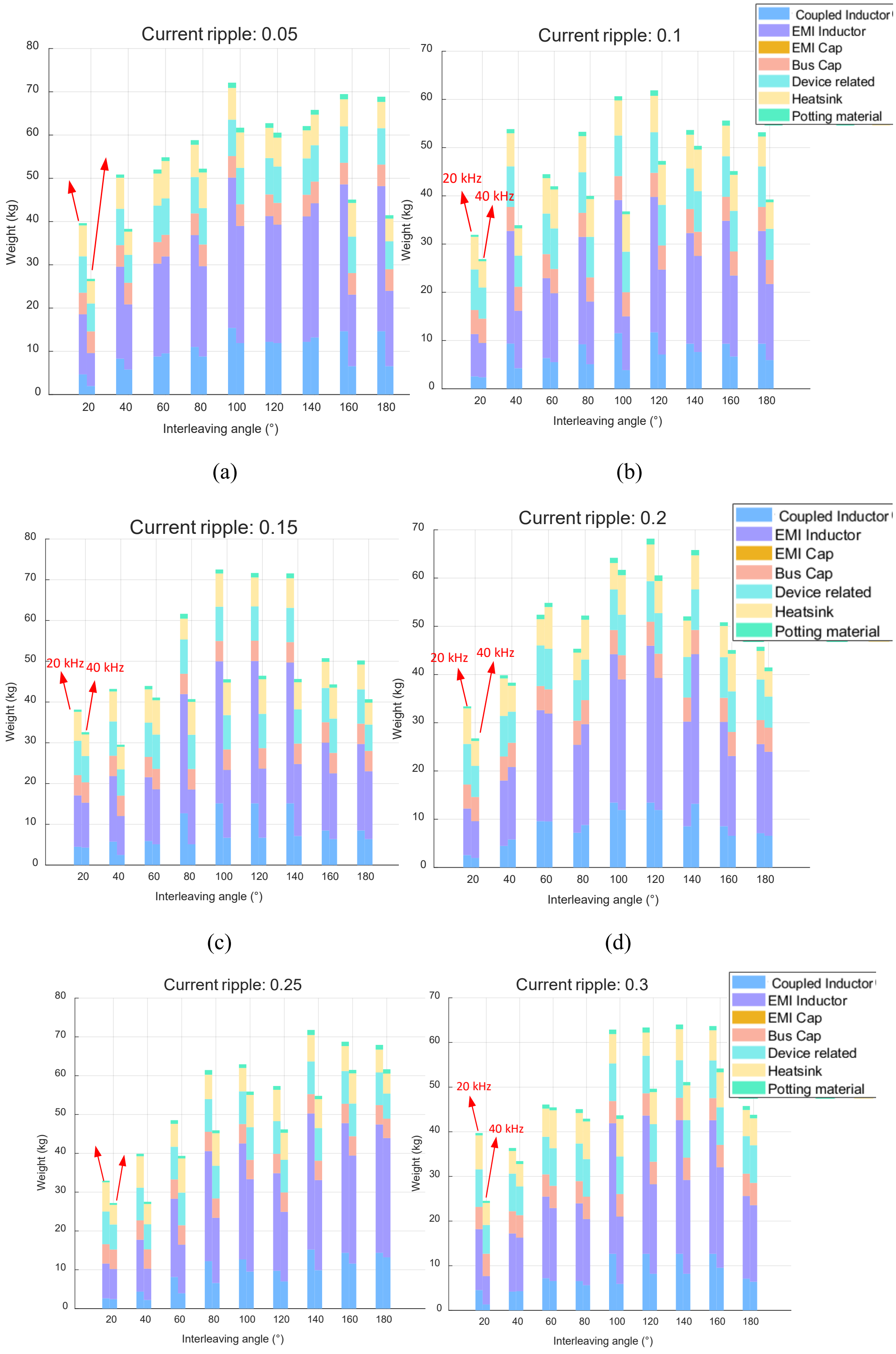
The design strategy here is to explore different interleaving angles and circulating current ripple ratios to achieve the lowest system weight. The design space of the interleaving angle including 9 cases is from 0° to 180°, and 20° per step. Similarly, the design space of circulating current ripple ratio including 6 cases is from 0.05 to 0.3, and 0.05 per step.

6.5.2 Case Study

The design specs and requirements in Section 6.4.2 are still applied here, but two paralleled converters are adopted instead of a single converter. Design results of two paralleled ANPC converters at 20 kHz and 40 kHz with different circulating current ratios and interleaving angles are given in Fig. 6-29. 20 kHz and 40 kHz are the preferable switching frequencies to achieve the low system weight based on the design comparison in Section 6.4.2, so they are applied for the paralleled converters design.

Based on the design results from Fig. 6-29, the design results of 40 kHz generally get lower the total system weight compared with one of 20 kHz. The larger circulating current ratios like 0.25 or 0.3 can achieve the lower total system weight than that with small circulating current ratios since the large current ratios only require the smaller coupled inductance and almost does not increase the weight of the cooling system. For the interleaving angle, 20°, 40°, 160°, and 180° are better than other interleaving angles in terms of total system weight. One interesting result is 180° is not worst to have the heaviest coupled inductor as the expectation while 100° ~ 140° are the worst interleaving angles having heaviest coupled inductor. It illustrates that the weight of coupled inductors is not only determined by the required inductance but also the volt-seconds applied in the inductor.

Two best design cases of two paralleled ANPC converters are compared with a single ANPC converter shown in Fig. 6-30. From this comparison, the conclusion is that two paralleled converters cannot help reduce the total system weight. First, since there is no ac side EMI filter, new added coupled inductors will increase ac side filters' weight. Second, dc-link capacitance is determined by the load change, so interleaving did not favor the reduction of dc-link capacitance. Third, the weight of the dc side DM filter is very light, and interleaving did not improve CM noise obviously, so the interleaving scheme cannot reduce DC EMI filters' weight much.



(a) (b)

(c) (d)

(e) (f)

Fig. 6-29. Design results of two paralleled ANPC converters with different interleaving angles and circulating current ratios.

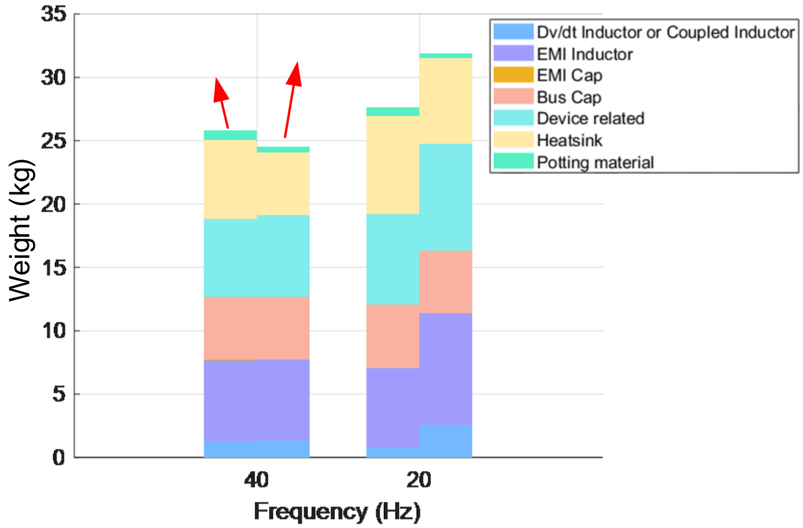


Fig. 6-30. Design Comparison between the single converter and two paralleled converters.

6.6 Summary

In the converter system level, dc-link voltage, modulation scheme, and topology can be treated as the design variables. To search the lowest converter system weight, different system-level design variables need to be evaluated through multiple design iterations, demanding a very long time to run simulations for providing the raw data and waveforms. The switching function based simulations are developed instead of switch-based simulations to reduce the execution time for the design iterations.

However, the drawback of switching function based simulations is that the waveforms of the components in the main power stage cannot be obtained, e.g., current waveforms of switches and current waveforms of flying capacitors in multi-level converters. In the post-processing for the semiconductor loss calculation and passive components design, the required waveforms can be synthesized with switching functions combined with modulation signals and phase currents. Two detailed examples are given to illustrate how to synthesize the waveforms for the device loss calculation and flying capacitance design in flying capacitor clamped multi-level topology.

Also, the system structure of the converter design consisting of databases of components, simulations and analytical models is presented for the system performance evaluations. A 500 kW motor drive in the aircraft application is used as a case study to demonstrate how the system-level optimization and iteration are conducted to search the lowest system weight. Through the system-level design iterations, three promising topologies with different modulation methods and switching frequencies are designed and compared to locate the best system performance. Moreover, three dc-link voltages are applied for the design to study how the dc-link voltage selection impacts the system weight.

Converters in parallel is another potential option to further improve the power density. A design strategy considering the trade-offs of the selections of the interleaving angle and coupled inductance is proposed. A case study is conducted for two paralleled converters to search the best combination of the interleaving angle and coupled inductance for the lowest system weight. Also, the best design results of paralleled converter structure are compared with the best design results of the single converter structure.

Chapter Seven

Development for Software

To enable more people to use the developed models and design algorithms for the converter design and optimization, a software integrating all design functions and models is further developed in MATLAB App Designer with a friendly UI. With the developed software, the design specifications configuration, database management and design results visualization are enabled. Also, the software supports five topologies including two-level, three-level ANPC, three-level T-type, multi-level flying capacitor clamped, and multi-level diode clamped voltage source converters.

7.1 Model-view-controller (MVC) Architecture based UI framework

MVC architecture is adopted to develop the software for the motor drive design. As shown in Fig. 7-1, the software development is separated by three parts: UI controller, design algorithm and model, and results visualization. The purpose of this architecture is to modify, upgrade and maintain three parts of programs separately without cross-correlations.

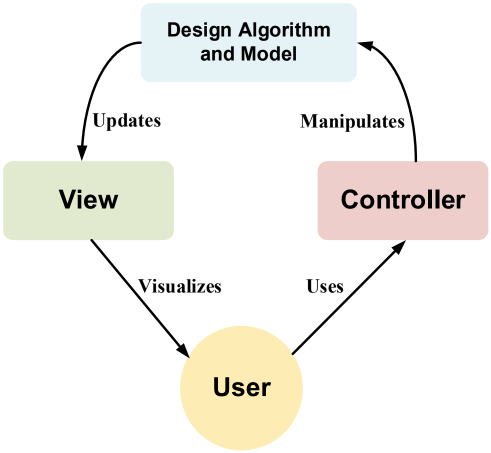


Fig. 7-1. MVC architecture based software framework.

The UI controller is developed by MATLAB App Designer, and all the design parameters and constraints can be configurated in the UI controller. Accordingly, those design parameters and constraints will be applied as the required inputs for models and design algorithms. Design algorithm and analytical models are implemented with M-File functions in an M-script, and circuit simulation models adopt Simulink. The execution of the selected models and design algorithm will provide final design results. Then, data visualization is realized by plotting functions in MATLAB, and the obtained design results are displayed as independent figures or displayed within the user interface of the software.

7.2 Design Configuration

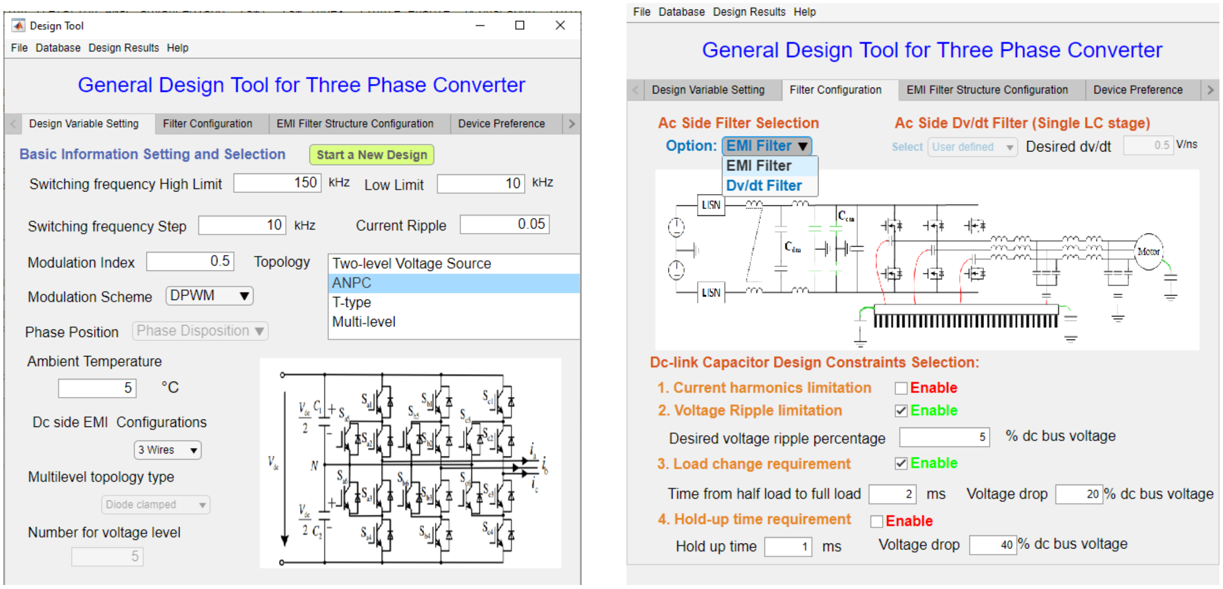
The developed software provides fruitful functionalities to configure a three-phase motor drive design for different specifications and requirements. Fig. 7-2 gives all configuration options for the converter design.

Specifically, Fig. 7-2(a) shows the basic configurations of converters provided by the developed software. Through this tab, five topologies and their possible modulation schemes can be selected. For multi-level topologies, the arbitrary voltage level is available for the configuration with the help of the switching-function based simulation scheme and design approach. Also, the switching frequency design range, ambient temperature, and duty cycle can be set in this tab.

Fig. 7-2(b) gives the configuration tab for the ac side filter and dc-link capacitors. Based on the practical requirement, the ac side filter is configured as either an EMI filter or *dv/dt* filter. For the *dv/dt* filter, the corner frequency can be determined by either the desired *dv/dt* value or the reflected voltage spike. Also, design constraints for dc-link capacitors can be selected in four aspects including the current harmonics limitation, voltage ripple limitation, load change requirement and hold-up time requirement.

As shown in Fig. 7-2(c), the detailed EMI filter structure and design configurations are given, and both the stage number and filter structure can be configured. In terms of the inductor design, three cooling methods are available for the selection and related analytical models are implemented. Also, the winding wire can be chosen from the general AWG cable and Litz wire with the equivalent AWG.

Fig. 7-2(d) and (e) show the device selection and cooling design configurations respectively. The power semiconductor and heatsink candidates are loaded from the database and are displayed in two tabs. The final configuration for the power rating, output RMS voltage, and dc-link voltage are given in the tab shown in Fig. 7-2(f).


Design Tool
File
Database
Design Results
Help
General Design Tool for Three Phase Converter
Design Variable Setting
Filter Configuration
EMI Filter Structure Configuration
Device Preference
Basic Information Setting and Selection
Start a New Design
V_{dc}
$\frac{V_{dc}}{2}$
C_1
C_2
N
S_{a1}
S_{a2}
S_{a3}
S_{a4}
S_{a5}
S_{a6}
S_{b1}
S_{b2}
S_{b3}
S_{b4}
S_{b5}
S_{b6}
S_{c1}
S_{c2}
S_{c3}
S_{c4}
S_{c5}
S_{c6}
i_a
i_b
i_c

Switching frequency High Limit 150 kHz Low Limit 10 kHz

Switching frequency Step 10 kHz Current Ripple 0.05

Modulation Index 0.5

Topology: Two-level Voltage Source / ANPC (selected) / T-type / Multi-level

Modulation Scheme DPWM

Phase Position Phase Disposition

Ambient Temperature 5 °C

Dc side EMI Configurations 3 Wires

Multilevel topology type Diode clamped

Number for voltage level 5

File
Database
Design Results
Help
General Design Tool for Three Phase Converter
Design Variable Setting
Filter Configuration
EMI Filter Structure Configuration
Device Preference
EMI Filter
Dv/dt Filter
LISN
LISN
C_{cm}
C_{dm}
Motor

Ac Side Filter Selection

Option: EMI Filter

Ac Side Dv/dt Filter (Single LC stage)

Select User defined Desired dv/dt 0.5 V/ns

Dc-link Capacitor Design Constraints Selection:

1. Current harmonics limitation ☐ Enable

2. Voltage Ripple limitation ☑ Enable

Desired voltage ripple percentage 5 % dc bus voltage

3. Load change requirement ☑ Enable

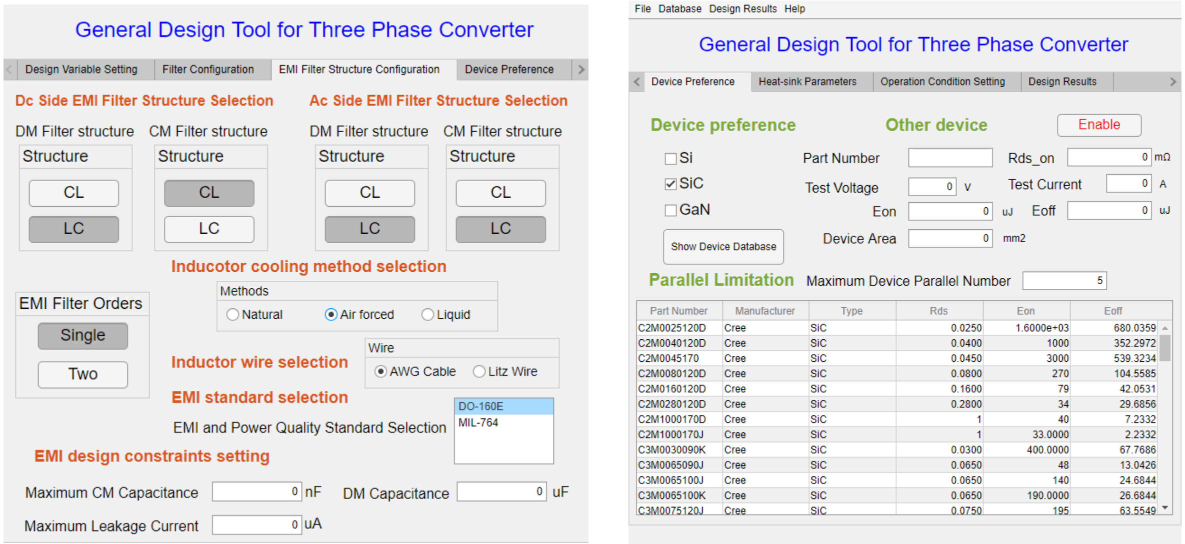
Time from half load to full load 2 ms Voltage drop 20 % dc bus voltage

4. Hold-up time requirement ☐ Enable

Hold up time 1 ms Voltage drop 40 % dc bus voltage

(a). Topology and modulation selection (b). Ac side filter configuration

Fig. 7-2. Design configurations provided by the developed software.


General Design Tool for Three Phase Converter
Design Variable Setting
Filter Configuration
EMI Filter Structure Configuration
Device Preference
Dc Side EMI Filter Structure Selection
Ac Side EMI Filter Structure Selection
DM Filter structure
CM Filter structure
DM Filter structure
CM Filter structure
Structure
CL
LC
Inducotor cooling method selection
EMI Filter Orders
Single
Two
Inductor wire selection
EMI standard selection
EMI design constraints setting
File Database Design Results Help
General Design Tool for Three Phase Converter
Device Preference
Heat-sink Parameters
Operation Condition Setting
Design Results
Device preference
Other device
Enable
Show Device Database
Parallel Limitation

Methods: ○ Natural ● Air forced ○ Liquid

Wire: ● AWG Cable ○ Litz Wire

EMI and Power Quality Standard Selection: DO-160E, MIL-764

Maximum CM Capacitance 0 nF

DM Capacitance 0 uF

Maximum Leakage Current 0 uA

☐ Si

☑ SiC

☐ GaN

Part Number

Rds_on 0 mΩ

Test Voltage 0 V

Test Current 0 A

Eon 0 uJ

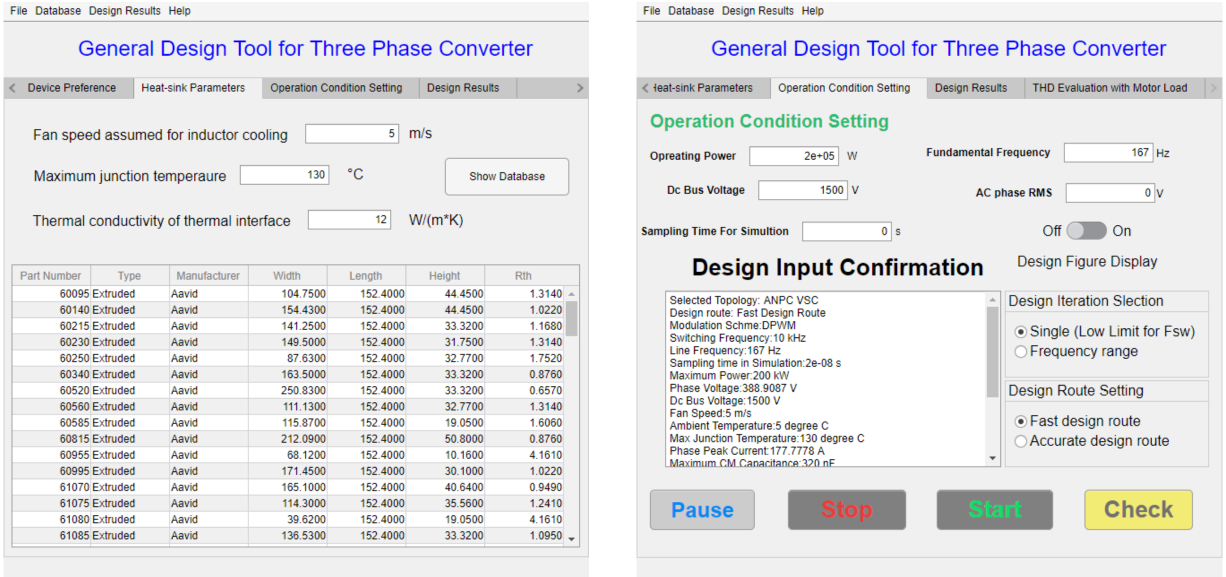
Eoff 0 uJ

Device Area 0 mm2

Maximum Device Parallel Number 5

Part Number	Manufacturer	Type	Rds	Eon	Eoff
C2M0025120D	Cree	SiC	0.0250	1.6000e+03	680.0359
C2M0040120D	Cree	SiC	0.0400	1000	352.2972
C2M0045170	Cree	SiC	0.0450	3000	539.3234
C2M0080120D	Cree	SiC	0.0800	270	104.5585
C2M0160120D	Cree	SiC	0.1600	79	42.0531
C2M0280120D	Cree	SiC	0.2800	34	29.6856
C2M1000170D	Cree	SiC	1	40	7.2332
C2M1000170J	Cree	SiC	1	33.0000	2.2332
C3M0030090K	Cree	SiC	0.0300	400.0000	67.7686
C3M0065090J	Cree	SiC	0.0650	48	13.0426
C3M0065100J	Cree	SiC	0.0650	140	24.6844
C3M0065100K	Cree	SiC	0.0650	190.0000	26.6844
C3M0075120J	Cree	SiC	0.0750	195	63.5549

(c). Filter structure and design configuration (d). Device selection configuration


File Database Design Results Help
General Design Tool for Three Phase Converter
Device Preference
Heat-sink Parameters
Operation Condition Setting
Design Results
Show Database
File Database Design Results Help
General Design Tool for Three Phase Converter
Heat-sink Parameters
Operation Condition Setting
Design Results
THD Evaluation with Motor Load
Operation Condition Setting
Design Input Confirmation
Pause
Stop
Start
Check

Fan speed assumed for inductor cooling 5 m/s

Maximum junction temperaure 130 °C

Thermal conductivity of thermal interface 12 W/(m*K)

Part Number	Type	Manufacturer	Width	Length	Height	Rth
60095	Extruded	Aavid	104.7500	152.4000	44.4500	1.3140
60140	Extruded	Aavid	154.4300	152.4000	44.4500	1.0220
60215	Extruded	Aavid	141.2500	152.4000	33.3200	1.1680
60230	Extruded	Aavid	149.5000	152.4000	31.7500	1.3140
60250	Extruded	Aavid	87.6300	152.4000	32.7700	1.7520
60340	Extruded	Aavid	163.5000	152.4000	33.3200	0.8760
60520	Extruded	Aavid	250.8300	152.4000	33.3200	0.6570
60560	Extruded	Aavid	111.1300	152.4000	32.7700	1.3140
60585	Extruded	Aavid	115.8700	152.4000	19.0500	1.6060
60815	Extruded	Aavid	212.0900	152.4000	50.8000	0.8760
60955	Extruded	Aavid	68.1200	152.4000	10.1600	4.1610
60995	Extruded	Aavid	171.4500	152.4000	30.1000	1.0220
61070	Extruded	Aavid	165.1000	152.4000	40.6400	0.9490
61075	Extruded	Aavid	114.3000	152.4000	35.5600	1.2410
61080	Extruded	Aavid	39.6200	152.4000	19.0500	4.1610
61085	Extruded	Aavid	136.5300	152.4000	33.3200	1.0950

Opreating Power 2e+05 W

Fundamental Frequency 167 Hz

Dc Bus Voltage 1500 V

AC phase RMS 0 V

Sampling Time For Simultion 0 s

Off On Design Figure Display

```
Selected Topology: ANPC VSC
Design route: Fast Design Route
Modulation Schme:DPWM
Switching Frequency:10 kHz
Line Frequency:167 Hz
Sampling time in Simulation:2e-08 s
Maximum Power:200 kW
Phase Voltage:388.9087 V
Dc Bus Voltage:1500 V
Fan Speed:5 m/s
Ambient Temperature:5 degree C
Max Junction Temperature:130 degree C
Phase Peak Current:177.7778 A
Maximum CM Capacitance:320 nF
```

Design Iteration Slection: ● Single (Low Limit for Fsw) ○ Frequency range

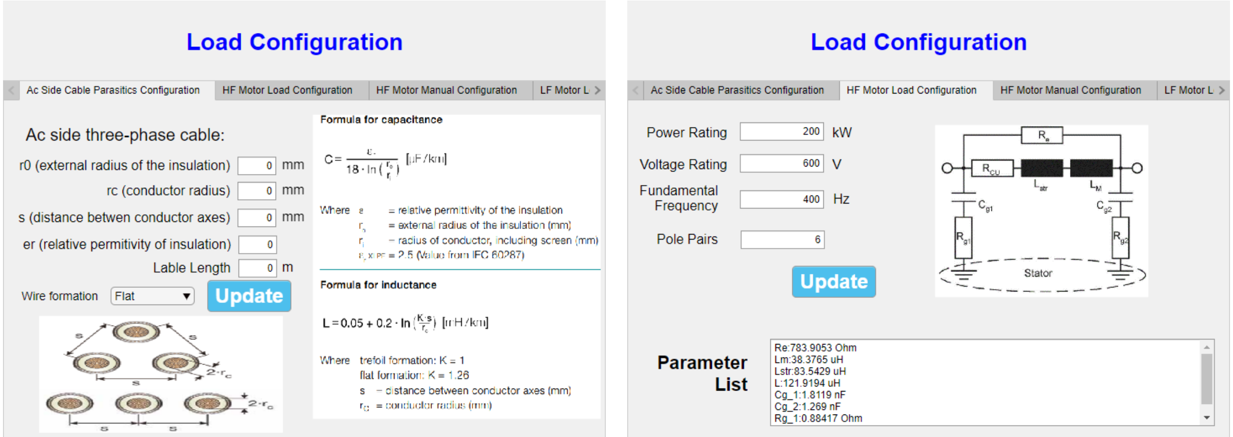
Design Route Setting: ● Fast design route ○ Accurate design route

(e). Cooling design configuration (f). System-level specs configuration

Fig. 7-2. continued.

Fig. 7-3 further shows the load configurations in the developed software. The parasitics of the ac side cable are updated in the simulation based on the inputs of parameters of the applied cables. Except for the ac side cable, three load types including the high frequency motor model, low frequency motor model and RLC model are provided for the simulation. The high frequency motor model is applied for the EMI noise evaluation and filter design while the low frequency motor model is applied for THD simulation. In addition, the RLC load is provided as the general load model for other potential applications.

Another useful function is shown in Fig. 7-4. Since many efforts are required to configure the details and the configuration of one design case may be time-consuming, the developed software can save the current design configurations as a MAT file in MATLAB. To recover the previous design configuration quickly, the software can load the saved configuration files to save time.


Load Configuration
Ac Side Cable Parasitics Configuration
HF Motor Load Configuration
HF Motor Manual Configuration
LF Motor L
Update
s
2·r_c
Load Configuration
Ac Side Cable Parasitics Configuration
HF Motor Load Configuration
HF Motor Manual Configuration
LF Motor L
Update
R_e
R_CU
L_str
L_M
C_g1
C_g2
R_g1
R_g2
Stator

Ac side three-phase cable:
r0 (external radius of the insulation) 0 mm
rc (conductor radius) 0 mm
s (distance betwen conductor axes) 0 mm
er (relative permitivity of insulation) 0
Lable Length 0 m
Wire formation Flat

Formula for capacitance

$$C = \frac{\varepsilon_r}{18 \cdot \ln\left(\frac{r_o}{r_i}\right)} \; [\mu F/km]$$

Where ε = relative permittivity of the insulation
r_o = external radius of the insulation (mm)
r_i = radius of conductor, including screen (mm)
ε_r XLPE = 2.5 (Value from IEC 60287)

Formula for inductance

$$L = 0.05 + 0.2 \cdot \ln\left(\frac{K \cdot s}{r_c}\right) \; [mH/km]$$

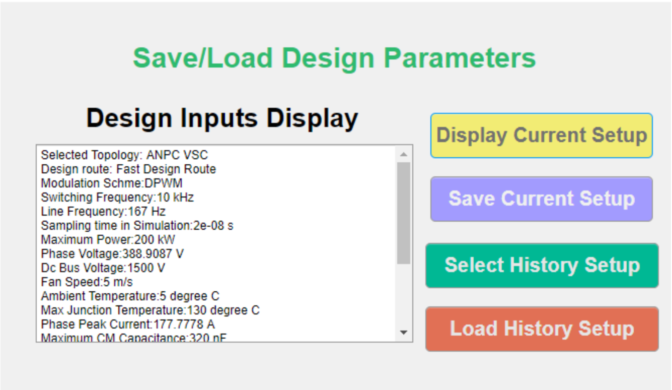
Where trefoil formation: K = 1
flat formation: K = 1.26
s = distance between conductor axes (mm)
r_c = conductor radius (mm)

Power Rating 200 kW
Voltage Rating 600 V
Fundamental Frequency 400 Hz
Pole Pairs 6

Parameter List
Re:783.9053 Ohm
Lm:38.3765 uH
Lstr:83.5429 uH
L:121.9194 uH
Cg_1:1.8119 nF
Cg_2:1.269 nF
Rg_1:0.88417 Ohm

(a). Cable model configuration (b). High frequency motor model configuration

Fig. 7-3. Load configurations in the developed software.


Save/Load Design Parameters
Display Current Setup
Save Current Setup
Select History Setup
Load History Setup

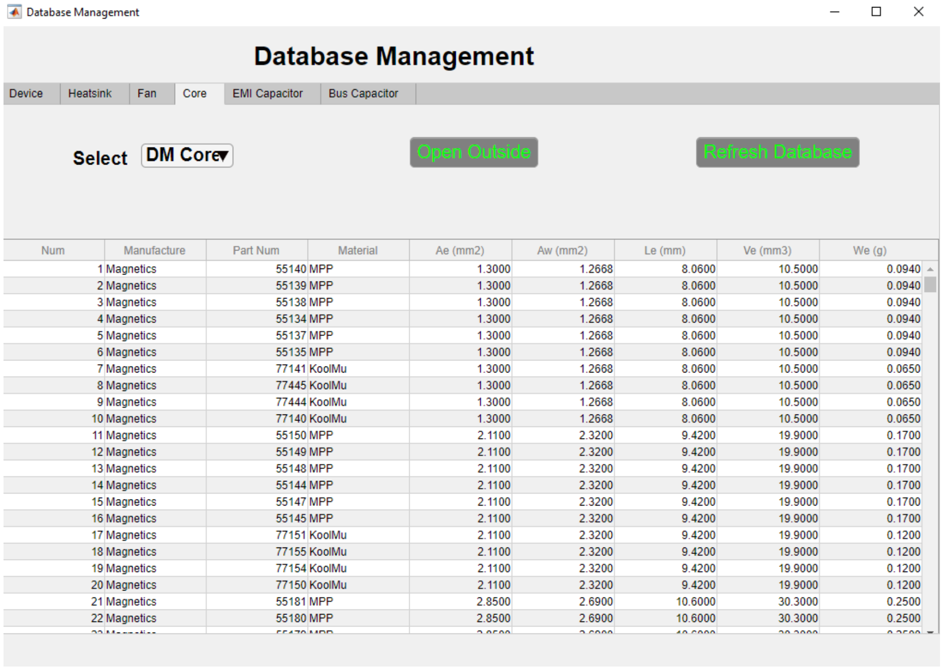
Design Inputs Display
Selected Topology: ANPC VSC
Design route: Fast Design Route
Modulation Schme:DPWM
Switching Frequency:10 kHz
Line Frequency:167 Hz
Sampling time in Simulation:2e-08 s
Maximum Power:200 kW
Phase Voltage:388.9087 V
Dc Bus Voltage:1500 V
Fan Speed:5 m/s
Ambient Temperature:5 degree C
Max Junction Temperature:130 degree C
Phase Peak Current:177.7778 A
Maximum CM Capacitance:320 nF

Fig. 7-4. Design parameters save and load function in the developed software.

7.3 Database Construction and Management

The strategy of the design approach is to use commercial components as candidates to estimate the converter weight, which leads to more practical design results in terms of weight estimation. Eight databases are built with Excel covering device, heatsink, fan, DM core, CM core, DM capacitor, CM capacitor, and bus capacitor. The user interface to manage the database is shown in Fig. 7-5, and the detailed information for each component is displayed in the table for convenient look-up.

To add a new item or delete an existing item in the database, the software provides a function to open the excel file outside. Then all the items in the opened database can be edited easily with Microsoft Excel.



Num	Manufacture	Part Num	Material	Ae (mm2)	Aw (mm2)	Le (mm)	Ve (mm3)	We (g)
1	Magnetics	55140	MPP	1.3000	1.2668	8.0600	10.5000	0.0940
2	Magnetics	55139	MPP	1.3000	1.2668	8.0600	10.5000	0.0940
3	Magnetics	55138	MPP	1.3000	1.2668	8.0600	10.5000	0.0940
4	Magnetics	55134	MPP	1.3000	1.2668	8.0600	10.5000	0.0940
5	Magnetics	55137	MPP	1.3000	1.2668	8.0600	10.5000	0.0940
6	Magnetics	55135	MPP	1.3000	1.2668	8.0600	10.5000	0.0940
7	Magnetics	77141	KoolMu	1.3000	1.2668	8.0600	10.5000	0.0650
8	Magnetics	77445	KoolMu	1.3000	1.2668	8.0600	10.5000	0.0650
9	Magnetics	77444	KoolMu	1.3000	1.2668	8.0600	10.5000	0.0650
10	Magnetics	77140	KoolMu	1.3000	1.2668	8.0600	10.5000	0.0650
11	Magnetics	55150	MPP	2.1100	2.3200	9.4200	19.9000	0.1700
12	Magnetics	55149	MPP	2.1100	2.3200	9.4200	19.9000	0.1700
13	Magnetics	55148	MPP	2.1100	2.3200	9.4200	19.9000	0.1700
14	Magnetics	55144	MPP	2.1100	2.3200	9.4200	19.9000	0.1700
15	Magnetics	55147	MPP	2.1100	2.3200	9.4200	19.9000	0.1700
16	Magnetics	55145	MPP	2.1100	2.3200	9.4200	19.9000	0.1700
17	Magnetics	77151	KoolMu	2.1100	2.3200	9.4200	19.9000	0.1200
18	Magnetics	77155	KoolMu	2.1100	2.3200	9.4200	19.9000	0.1200
19	Magnetics	77154	KoolMu	2.1100	2.3200	9.4200	19.9000	0.1200
20	Magnetics	77150	KoolMu	2.1100	2.3200	9.4200	19.9000	0.1200
21	Magnetics	55181	MPP	2.8500	2.6900	10.6000	30.3000	0.2500
22	Magnetics	55180	MPP	2.8500	2.6900	10.6000	30.3000	0.2500

Fig. 7-5. Database management in the developed software.

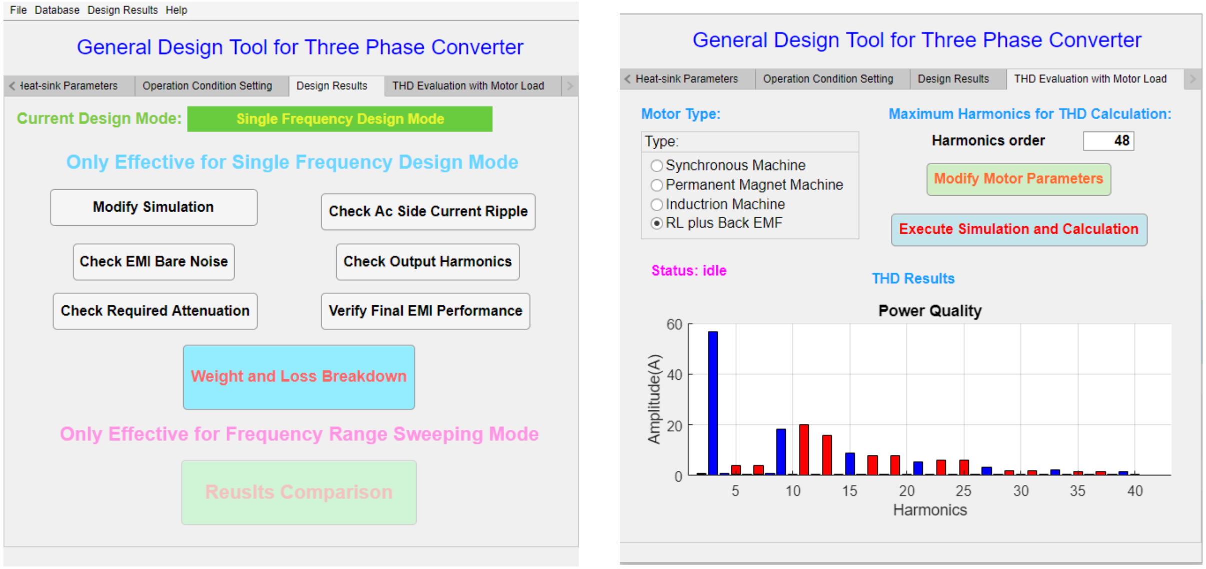
7.4 Design Results Visualization

The developed software provides visualization functions for EMI noise spectrum, ac side current ripple, output current harmonics and THD result, weight and loss breakdown for the single converter, and weight comparison with sweeping switching frequencies.

Fig. 7-6(a) shows the design results display function tab. In this tab, the design results at the single frequency design mode and sweeping frequency design mode can be visualized with pie and bar charts. E.g., Fig. 7-7 gives the weight breakdown displays for the flying-clamped multi-level converter and two-level voltage source converter. The program can identify the selected topology in the file of design results and display the weight of the required components accordingly. Compared with Fig. 7-7(a) and (b), Fig. 7-7(a) has one extra item for the weight of flying capacitors due to the topology selection.

Similarly, the program can plot different figures of design results comparison with switching frequency based on the selected topology and configurations. Fig. 7-8 shows two figures for different ac side EMI configurations and the selected topologies. Fig. 7-8(a) shows the weight of flying capacitors while Fig. 7-8(b) did not because of the difference in selected topologies. Also, Fig. 7-8(b) shows the weight of *dv/dt* inductors while Fig. 7-8(a) did not due to the difference in ac side filter configurations.

Except for graphical visualizations, an information query program is developed to look up the detailed information for design results. As Fig. 7-9 shows, the weight and loss numbers for different parts can be checked in the “Weight and Loss” tab. Also, the physical design results and component selection results can be reviewed. For example., for the inductor design, the number of cores in the stack, turns number, wire gauge, temperature rise, and total weight and loss are displayed in the “Inductor Infor” tab.


File
Database
Design Results
Help
General Design Tool for Three Phase Converter
Heat-sink Parameters
Operation Condition Setting
Design Results
THD Evaluation with Motor Load
Only Effective for Single Frequency Design Mode
Modify Simulation
Check Ac Side Current Ripple
Check EMI Bare Noise
Check Output Harmonics
Check Required Attenuation
Verify Final EMI Performance
Weight and Loss Breakdown
Only Effective for Frequency Range Sweeping Mode
Reusults Comparison
General Design Tool for Three Phase Converter
Heat-sink Parameters
Operation Condition Setting
Design Results
THD Evaluation with Motor Load
Motor Type:
Maximum Harmonics for THD Calculation:
Modify Motor Parameters
Execute Simulation and Calculation
THD Results
Power Quality
Amplitude(A)
Harmonics
0
20
40
60
5
10
15
20
25
30
35
40

Current Design Mode: Single Frequency Design Mode

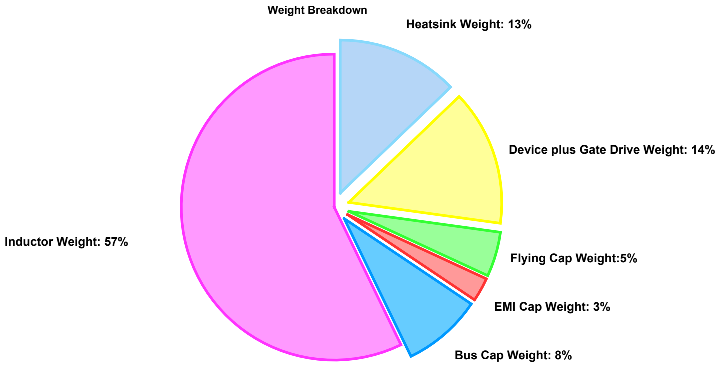
Type:
○ Synchronous Machine
○ Permanent Magnet Machine
○ Inductrion Machine
● RL plus Back EMF

Harmonics order 48

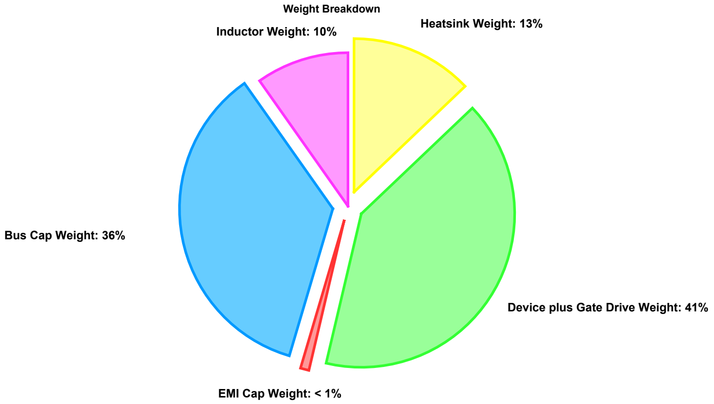
Status: idle

(a). Weight breakdown and comparison display (b). THD results display

Fig. 7-6. Design visualization functions for the developed software.

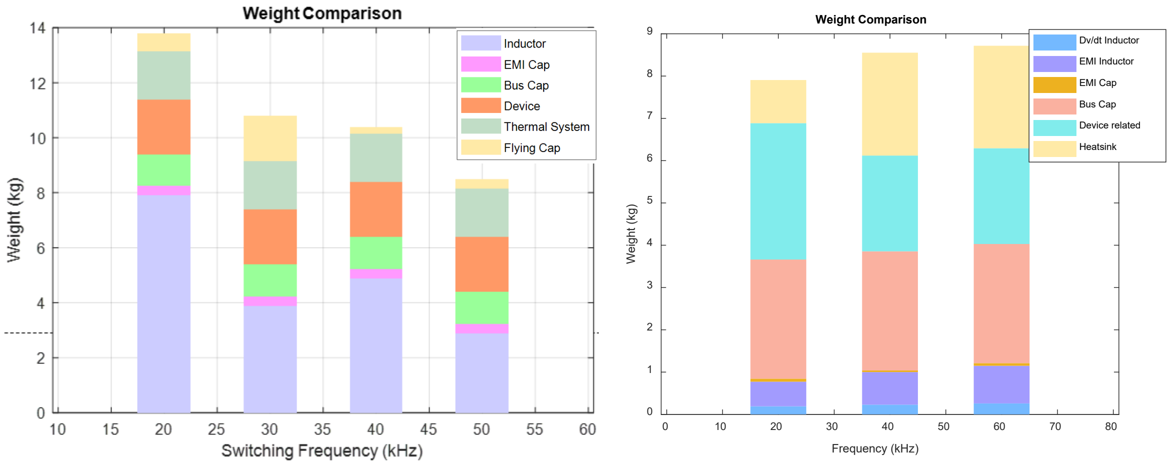


(a). Flying capacitor clamped multi-level converter weight breakdown display



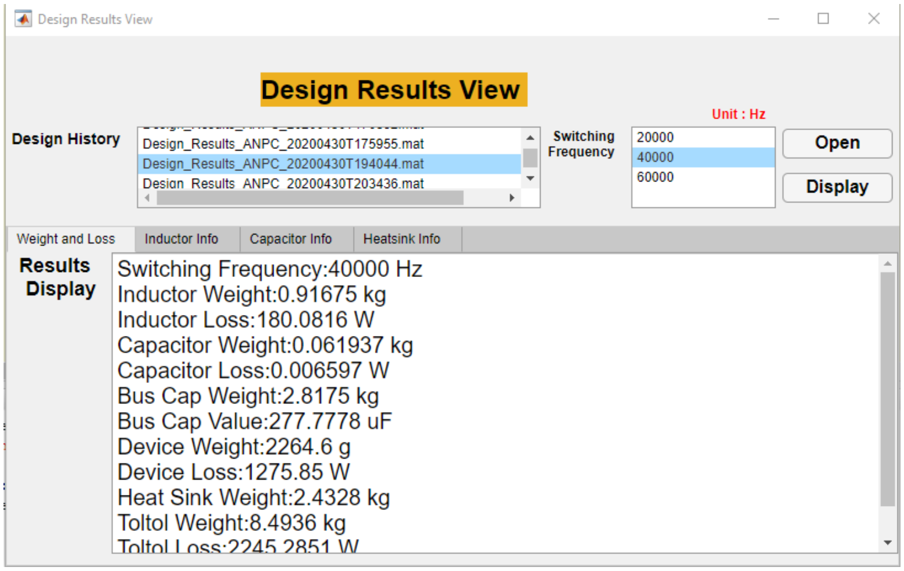
(b). Two-level VSC weight breakdown display

Fig. 7-7. Weight breakdown for a single converter design result.



(a). Multi-level converter with ac side EMI filter (b). ANPC converter with ac side *dv/dt* filter

Fig. 7-8. Weight comparison at different switching frequencies.


Design Results View
Design Results View
Unit : Hz
Design History
Design_Results_ANPC_20200430T175955.mat
Design_Results_ANPC_20200430T194044.mat
Design_Results_ANPC_20200430T203436.mat
Switching Frequency
20000
40000
60000
Open
Display
Weight and Loss
Inductor Info
Capacitor Info
Heatsink Info
Results Display

```
Switching Frequency:40000 Hz
Inductor Weight:0.91675 kg
Inductor Loss:180.0816 W
Capacitor Weight:0.061937 kg
Capacitor Loss:0.006597 W
Bus Cap Weight:2.8175 kg
Bus Cap Value:277.7778 uF
Device Weight:2264.6 g
Device Loss:1275.85 W
Heat Sink Weight:2.4328 kg
Toltol Weight:8.4936 kg
Toltol Loss:2245.2851 W
```

Fig. 7-9. Detail design results and the selected component information.

7.5 Summary

Software integrated with design algorithms and models is developed for the general motor drive design. In order to achieve easy maintenance and upgrade, the MVC concept is adopted to separate the software into three modules, and each module can be developed with fewer relations with other modules.

The developed software provides complete converter design configurations that include not only the converter related parameters like the topology and modulation selection, switching frequency, and cooling method but also load related parameters like load type and cable parasitics. Also, eight databases for power electronics components are built with commercially available products, and a database management program is developed to add or modify items in the database easily. Moreover, graphic and literal version design results visualization programs are developed. The weight and loss breakdowns at one switching frequency are given by pie charts while the weight comparison results at different switching frequencies are given by bar charts, and the EMI noise spectrum and current harmonics for THD calculation can be also given with figures. To review more detailed design results, all the numbers and component selections results are displayed in a separately developed subprogram.

Chapter Eight

Conclusion and Future Work

This chapter summarizes the work that has been done and proposes the potential future work which can further push forward this research topic.

8.1 Conclusion

In this dissertation, the modeling and optimization schemes in the three-phase motor drive system have been investigated and studied to shrink the gaps between the paper design and implementation. For the modeling part, the conclusions are drawn as follows.

- The time-varying inductance model for powder core inductors considering the current-bias dependent permeability is developed to study the impacts of unbalanced DM impedance in a three-phase ac system on EMI filter design. From simulation and experimental results, it demonstrates that the unbalanced DM impedance can convert partial DM noise into non-intrinsic CM noise in the high frequency range, leading to a lower corner frequency of CM filter design compared with the result without considering the unbalanced DM impedance.
- The impedance-based CM inductor design scheme is proposed that incorporates the frequency-dependent permeability and imaginary permeability model for nanocrystalline core inductors. Instead of only using the corner frequency to determine the required CM inductance, the proposed scheme derives the required CM impedance based on the required noise attenuation. Then, the turns number can be determined by providing enough CM impedance from 150 kHz to 2 MHz.

- An improved maximum magnetic flux density model for CM inductor is proposed with current FFT analysis and the frequency-dependent permeability model. With the proposed model, the error for B_{max} estimation is reduced from 24.8% to 8.27% compared with the peak current based B_{max} model.
- From the perspective of the analogy between the reluctance and capacitance, the errors of the proposed leakage inductance model for a toroidal core inductor is reduced 25%~30% at large turns number compared with models in the previous literature.
- An automatic geometry creation program is developed to form the corresponding power loop layout and busbar design for the selected device and dc-link capacitors. PEEC numerical modeling method is adopted to extract parasitic inductance from the created geometries.
- A discrete-time switching behavior model is developed combined with the extracted parasitic inductance to determine the gate resistance selection based on the overvoltage constraint.
- A multi-variable loss scaling method with the discrete-time switching behavior model is proposed to reflect the impacts of the gate resistance and junction temperature on switching energies. In an ANPC converter loss calculation example, the total device loss obtained from the proposed multi-variable scheme is 11.6% higher than the conventional linear loss scaling method.

For the design optimization schemes part, the conclusions are drawn as follows.

- Two optimization schemes are developed to achieve the minimum weight of filters. A_p based weight indicator is used to predict the weight of *dv/dt* filters, and the improved PSO algorithm is applied to search the optimal EMI filter design. Through testing with the Rastrigin function, the improved PSO algorithm can achieve both fast convergence speed of PSO and the global searching capability of GA.

- A device selection iteration is developed to determine the turn-on and turn-off gate resistance considering multiple constraints like the avoidance of underdamped state of gate drive voltage, the current limitation of gate drive IC, overvoltage issue and malfunction of gate drive. The design results show the turn-on gate resistance is mainly determined by *di/dt* to avoid the malfunction of gate drive (cross-talk), and the turn-off gate resistance is mainly determined by *dv/dt* to avoid the voltage breakdown during the turn-off.
- A complete design iteration including device selection and cooling design is proposed. Compared with the conventional paper design method, the proposed scheme can cover the impacts of geometry related design factors and gate resistance selections.
- A system-level converter design optimization is applied. The impacts of different topologies, modulation methods, switching frequencies, paralleled converter structure and filter configurations on the converter system weight can be evaluated.

Finally, to reduce the learning cost and design time, UI-based design software is developed to enable more people to conduct converter designs with the models and design algorithms presented in this dissertation. With the developed software, the multiple functionalities are provided as follows.

1. Design configurations: converter, load, filter, and output specifications configurations are provided. For the target specifications, the different combinations of topologies, modulation schemes, cooling methods, switching frequencies, and converter paralleling structure can be evaluated to determine the lowest converter system weight.

2. Database management: eight databases are built with Excel, covering all common applied power electronics components. The users can edit, add, or delete items in each database.
3. Design results visualization: both graphical and literal design results visualization programs are developed. The loss and weight breakdown for a single converter and weight comparison for multiple variables can be displayed.

8.2 Future Work

- Modeling accuracy improvement

In this dissertation, some models for the physical design are empirical formula or curve-fitting based functions, which are only effective or validated in a limited operating range. To improve design accuracy, it is necessary to further verify those models at different operating conditions.

1. Thermal models of busbars and inductors at the high output power and current application. The adopted thermal model of inductors in [36] is an empirical formula based on testing results at low-medium power applications while the high power and high output current are common design cases in a motor drive application. As a result, the adopted thermal model may not be accurate enough for the high output current. The extra verification and improvement of thermal models need to be done in terms of high output current.
2. Conduction loss model does not incorporate the impacts of junction temperature. For ac output currents, the instantaneous junction temperature varies during one line cycle. Thus, the on-resistance also varies with junction temperature during one line cycle so that the conduction loss calculation is not accurate by only assuming a constant

junction temperature. The device dynamic thermal model should be considered to predict the instantaneous junction temperature and corresponding on-resistance.

3. The state of art core loss model IGSE or I^2GSE did not include the loss impacts of dc-bias. Also, Steinmetz parameters depend on the operation frequency range, and the selection of Steinmetz parameters at one testing frequency may not be scientific for the ac side output currents with rich high frequency harmonics.

- Automatic layout optimization

The geometry related design factors have been incorporated for the main power commutation loop in this dissertation. However, the layouts of the main power commutation loop are limited by predefined experience-based geometries for different topologies. One promising improvement is to develop an automatic layout program to optimize the commutation loop based on the selected topology, dimensions of dc-link capacitors, and power semiconductors. This can further help paper design results achieve more accurate parasitic inductance estimation.

Another layout optimization should be considered in EMI filter design since the layout and position of capacitors and inductors in EMI filters are critical to the attenuation performance. Also, layouts and positions of filter components impact near-field magnetic and capacitive coupling effects, causing different insertion losses or transfer gains of EMI filters. Therefore, an automatic layout optimization program for the EMI filter is worth exploring to predict EMI filter attenuation more accurately.

- Utilization of existing design results to give performance indication and suggestion for the future design

With the developed software, a large number of design results will be produced through different design specifications and requirements, and those design results can be treated as “big data” in the power electronics area. Furthermore, it is possible to train an “expert system” with the existing design results by the knowledge of computer science like deep learning to predict the converter performance and promising schemes for a new application or design requirements.

- Consideration of components’ tolerance

In reality, no manufacturer can guarantee the same parameters for all the produced components, and a tolerance data is normally provided in the datasheet and user’s guide, e.g., film capacitors have a 20% tolerance for the capacitance value and magnetic cores have a 10% tolerance for the permeability. Consequently, how the tolerance of components impact the power electronics design and how to consider the tolerance in the design is important.

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