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Design of an adaptive cable equalizer using 0.5 [mu]m [i.e. micrometer] CMOS process

Mohammad Abdul Ahad
University of Tennessee

To the Graduate Council:

I am submitting herewith a thesis written by Mohammad Abdul Ahad entitled "Design of an adaptive cable equalizer using 0.5 [mu]m [i.e. micrometer] CMOS process." I have examined the final electronic copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

Syed K. Islam, Major Professor

We have read this thesis and recommend its acceptance:

Marshall O. Pace, M. Mostofa Hawlader

Accepted for the Council:
Carolyn R. Hodges

Vice Provost and Dean of the Graduate School

(Original signatures are on file with official student records.)

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DESIGN OF AN ADAPTIVE CABLE EQUALIZER USING 0.5 μm CMOS PROCESS

A Thesis
Presented for the
Master of Science Degree
The University of Tennessee, Knoxville

Mohammad Abdul Ahad

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ABSTRACT

Data transmitted over a long length of cable at high rates must be equalized in order to compensate for the loss and phase dispersion of the cable. The more the cable length, the more the loss is in it. As the data transfer rate is increasing, more bandwidth is needed and the data communication industries are demanding an equalizer system with more bandwidth. A pole-zero model for the coax cable- equalizer is developed which shows that the poles and zeros of the cable transfer function decrease linearly with the increase of the cable length. Thus an adaptive equalizer system has been designed where the length of the cable will be estimated through the peak detector circuitry and the equalizer filter will be tuned automatically according to the estimated cable length using this linearity. All the circuits of the system have been designed using AMI 0.5μm CMOS technology and simulated on Cadence's Spectre tools.

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CHAPTER 1

Introduction

Data transmitted over a long length of cable at high rates must be equalized in order to compensate for the loss and phase dispersion of the cable [1]. This loss is proportionate to the root of the frequency ($\sqrt{f}$) of the data transmitted. As the data communication industry is always eager to increase the rate of data transfer to higher level, it is essential that the cable should be equalized. Again, loss in the cable increases with the increase of the length of the cable for a particular frequency of operation. Any data transmission through the cable is bandwidth limited. The more the bandwidth, the more is the rate of data transfer through cable. For data transmission over standard telephone lines, the channel bandwidth is typically a few kilohertz over a few miles. Transmission over unshielded-twisted-pair wire is bandwidth limited to a few tens of megahertz over 300 feet and transmission over high-quality coaxial cable is limited to the hundreds of megahertz range over a few hundreds feet. The extent to which the equalizer is able to match the inverse of the cable loss characteristic determines the extent to which inter-

symbol interference induced jitter is eliminated. In application where the cable length may vary the equalizer must adapt its transfer function accordingly.

The current trend in CMOS VLSI is to perform information processing more and more in the digital domain [2]. However, the interface between the analog outside world and the digital processor will remain analog in nature. As the technology forges ahead, the performance/cost potential of the complete system cannot be fully realized until integrated circuits with analog input and output can be implemented. The main challenge in implementing a high-speed data-communications transceiver in a standard CMOS process is in the analog parts of the system. These parts include the equalizer and the clock-recovery circuit. If the analog components can be successfully integrated, then it may be possible to integrate the complete transceiver onto a single chip. The complete transceiver may include a data scrambler and de-scrambler, analog-to-digital and digital-to-analog converters for multi-level signaling, and feed-forward as well as decision-feedback equalizers as described in [3].

The main work of this thesis project involved the design of an adaptive analog cable equalizer implemented in AMI 0.5μm CMOS process. The system is designed such a way that it will estimate the length of cable to its input automatically and accordingly tune the filter. The system is designed based on a MATLAB program, which modeled the pole-zero variation of the cable transfer function with the length of the cable. The interesting result of this model is that poles and zeros of the cable transfer function

decrease linearly as the cable length increases. The equalizer filter is designed as a cascade of three band-pass filters where tuning capability has been introduced when the length of the cable changes. Moreover, the filter is selected to give a single pole and single zero with a gain factor of one.

1.1 Losses in Cable

There are two types of losses occur in the cable made of copper, namely skin effect loss and the dielectric loss. The skin effect arises when electro-magnetic waves are incident upon, or are guided by, conducting surfaces. The electric fields set up currents in the surface and hence the fields only penetrate for a finite distance. This in turn means that the currents only exist near the surface. In practice, in a thick conductor, the current level falls exponentially with the depth below the metal surface. The result is that the currents on conductors associated with a guided field only make use of a finite metal thickness. Hence the resistance experienced by the currents (which leads to dissipation losses) is influenced by this thickness as well as the material's resistivity. The magnitude of the currents falls exponentially with a 1/e scale depth, given by the approximate expression,

$$d \approx \frac{1}{2*10^{-3}*\sqrt{f.\sigma}} \qquad 1.1$$

where,

f = frequency of operation and

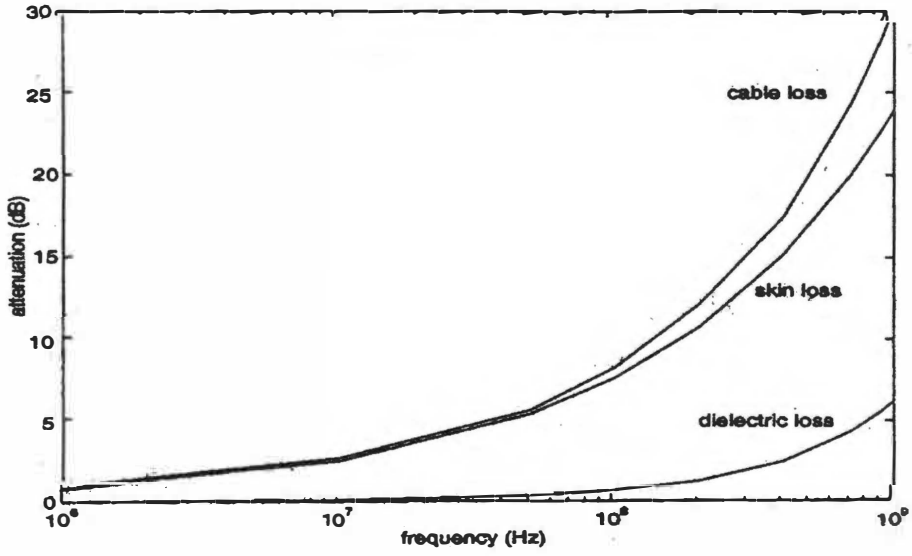

Figure 1.1: Cable attenuation showing both the skin loss and the dielectric loss

σ = conductivity of the metal

This frequency dependence affects both the signal velocity causing dispersion distortions and preferentially attenuates high frequencies causing a change of the amplitude spectrum.

Another kind of loss that occurs in cable is dielectric loss. This loss is prominent at very high frequencies. Dielectric loss occurs due to the molecular movement at higher frequencies and results in loss as heat. Figure 1.1 shows the two types of losses that occur in the cable. From figure 1.1, it is evident that, skin loss is the most prominent part of the cable loss and frequency up to 100MHz, dielectric loss has little contribution on the overall cable loss.

1.2 Data Communication Through Wire

There are many applications that use wire as a medium to transfer data. Few of them are reviewed here. Cable is the medium that ordinarily connects network devices. Cable's ability to transmit encoded signals enables it to carry data from one place to another. These signals may be electrical as in copper cable or light pulses as in fiber-optic cable.

1.2.1 Ethernet

Ethernet is a well-known and widely used network technology [4] that employs bus topology. Ethernet was invented at Xerox Corporation in early 1970s as a 10Mbps (Megabits per second) networking protocol, very fast for its day, operating over a heavy coax cable. Digital Equipment Corporation, Intel Corporation and Xerox later cooperated to devise a production standard, which is informally called DIX Ethernet for the initials of the three companies. IEEE now controls Ethernet standards. Conceptually, an Ethernet LAN consists of a single coaxial cable, called the ether, to which multiple computers connect. A given Ethernet is limited to 500 meters in length, and the standard requires a minimum separation of 3 meters for each pair of connections. Ethernet hardware operates at a bandwidth of 10 Megabits per second. A newer version known as *fast Ethernet* operates at 100Mbps. Because it uses a bus topology, Ethernet requires multiple computers to share access to a single medium. A sender transmits a modulated carrier wave, which propagates from the sender toward both ends of the cable.

The main Ethernet standards for transmitting 100Mbps over copper are 100Base-T4, 100Base-TX and 100Base-T2. Each specifies information rates of 100Mbps. However they use different number of cable pairs, and different coding scheme.

100Base-T4 uses four pairs of CAT4 cable and is useful for installations where upgrading to CAT5 is impractical.

100Base-TX uses two pairs of CAT5 cable with each pair supporting 50Mbps. 4B5B coding is used to increase the transition density to make clock synchronization easier and to remove DC bias.

100Base-T2 works with two pairs of CAT3 cable, each supporting 50Mbps. Gigabit Ethernet is an emerging standard with information capacity of 1000Mbps over four pairs of CAT5 cable up to 100 meter in length.

1.2.2 Digital Television

Broadband technologies can be classified as either one-way or two-way. One-way technologies send digital information to the end user at very high speeds, but rely on some other means (usually an analog modem and a phone line) to receive information from the end user. One-way broadband technologies include digital television (DTV) and satellite. Two-way broadband technologies, such as cable and digital subscriber lines (DSL) send and receive digital information at very high speeds over the same medium. Two-way broadband technologies usually require a wired infrastructure. Broadband transmission uses the same principles as cable TV and runs on coax. Broadband and

cable TV take advantage of coax cable's ability to transmit many signals at the same time. Each signal is called a channel. Each channel travels along at a different frequency, so it does not interfere with other channels. Again television studios use digital video transmission from the video cameras to the editing equipment and monitors. The video signal in a video camera has three component signal for each red, green and blue. Alternatively, these three signals may be luminance, Y, and the color difference signals, Y-R and Y-B. These signals are analog in nature but for editing purposes, these signals are converted to digital. When converting to digital, the luminance channel is sampled at 13.5 MHz, while the color difference channels are sampled at half that rate, The end result of sampling each with 10 bit resolution and multiplexing the three lines into one, is a 270 Mbps serial digital signal as specified in SMPTE Standard 259M [5]. Other bit rates covered by this standard are 143 Mbps for 10-bit sampling of NTSC, and 177 Mbps for 10-bit sampling of PAL. There are other standard bit rates of 360Mbps, 400Mbps. SMPTE Standard 344M uses serial data rate of 540Mbps. SMPTE Standard 292M, which is used for High- Definition-Television (HDTV) defines a bit-serial interface for component video at data rates in the range of 1.485Gbps. Application of this standard requires the use of cables which have loss proportional to the square root of frequency. Also, the cable attenuation should not exceed 20dB at half the bit rate.

1.2.3 ATM

Asynchronous transfer mode (ATM) is a high-performance, cell-oriented switching and

multiplexing technology that utilizes fixed-length packets to carry different types of traffic [6]. ATM is a technology that will enable carriers to capitalize on a number of revenue opportunities through multiple ATM classes of services, high-speed local-area network (LAN) interconnection, voice, video, and future multimedia applications in business markets in the short term, and in community and residential markets in the longer term. Asynchronous transfer mode (ATM) is a technology that has its history in the development of broadband ISDN in the 1970s and 1980s. Technically, it can be viewed as an evolution of packet switching. Like packet switching for data (e.g., X.25, frame relay, transmission control protocol [TCP]/Internet protocol [IP]), ATM integrates the multiplexing and switching functions, is well suited for bursty traffic (in contrast to circuit switching), and allows communications between devices that operate at different speeds. Unlike packet switching, ATM is designed for high-performance multimedia networking. ATM technology has been implemented in a very broad range of networking devices. The ATM cells consist of a 48 byte information load, a five byte address load, and may be transmitted at many standard rates. ATM user network interface (ATM UNI) standards specify how a user connects to the ATM network to access these services. A number of standards have been defined for T1/E1 (25Mbps), T3/E3, OC–3 (155Mbps) and OC–12 with OC–48 (2.4Gbps) in the works. OC–3 interfaces have been specified for use over single-mode fiber (for wide-area applications) and over unshielded twisted pair or multimode fiber for lower-cost, in-building applications.

1.3 Problems of Data Communication Through Lossy Cable

Due to the skin effect that was described earlier, any electrical signal suffers loss when transmitted through it. This loss is frequency dependent and the more the frequency, the more the loss is. For this attenuation, any step response through a length of cable will have a finite transition time. So inter-symbol interference may occur if the time between consecutive data signal edges is less than the transition time of the signal from the cable. The inter-symbol interference caused in this manner can lead to errors in the received signal as it passes to the next stage. Again, bit error rate is directly related to jitter which may cause distortion to output wave shape. Phase dispersion may also occur.

1.4 Thesis Outline

The first chapter describes the background and the motivation for this thesis work. It also provides some applications of cable for high-speed data communication and problems of data communication thorough cable.

A pole-zero model for the cable equalizer, which unveils the relationship between the cable length and the poles and zeros of the corresponding cable transfer function, has

been presented in chapter two. Using that model a new adaptive cable equalizer system topology has been introduced.

Chapter three provides all designs and complete description of the circuit blocks for the overall adaptive equalizer system which were done in AMI 0.5μm CMOS process. Simulation results are also provided here for each block.

The overall system simulation results and their conformity with the ideal responses have been described in chapter four.

Chapter five gives the conclusion of the work and remark on future work that can be done on this project.

Appendix A gives a brief description on the present adaptive cable equalizer ICs.

CHAPTER 2

System Design

In this chapter, a theoretical basis of the frequency dependent losses on co-axial cable is derived. Using these equations, a pole-zero model for the cable-equalizer that is, the pole-zero variation of the cable transfer function with its length is developed using MATLAB curve-fitting routine. An adaptive analog equalizer system to correct those frequency dependent losses has been proposed and the system topology has been presented.

2.1 General Equalizer System Topology

An equalizer with a transfer function that is the inverse of the channel response is called a zero forcing linear equalizer [7]. One possible method of implementing frequency-domain equalizer [8] is through the use of an array of bandpass filters, Bi(s), each followed by a gain control stage, Gi(s), as shown in Figure 2.1, so that the weighting of

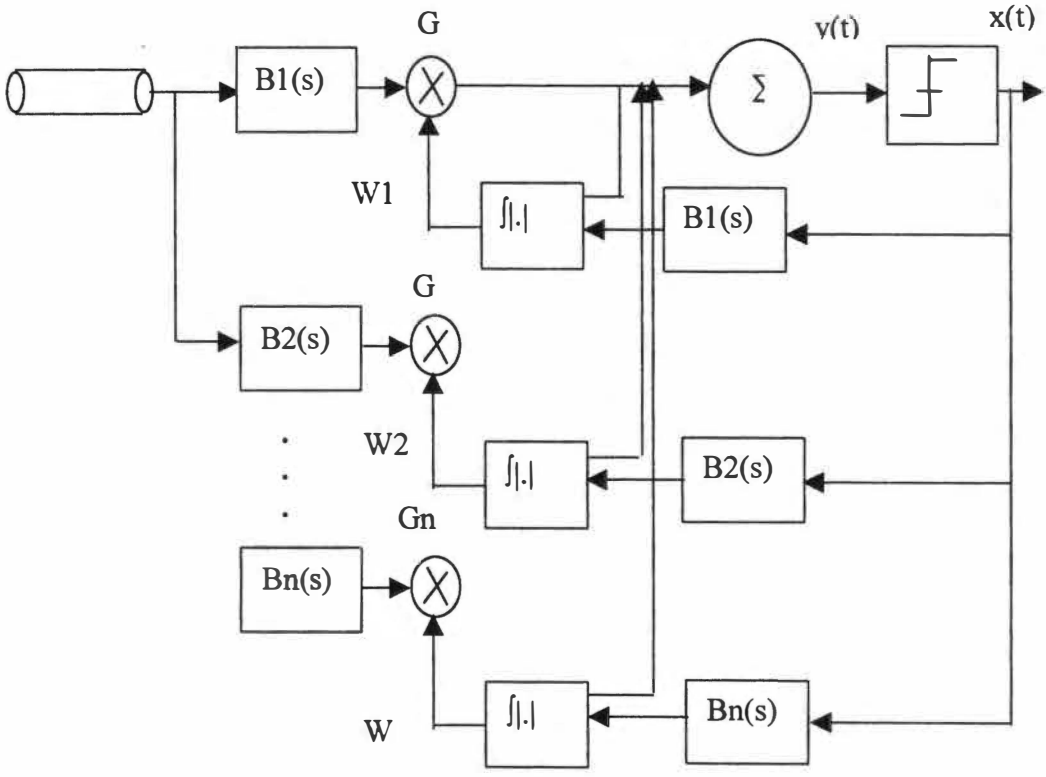

Figure 2.1: General Equalizer block diagram

each of the spectral bands can be independently controlled. The bands must be narrow enough so that the applied weighting is appropriate for all frequency components within the band. Then, it should be possible to re-assemble the transmitted signal, s(t), by summing the weighted spectral components to produce y(t)

But, a new system can be developed if the cable transfer function can be modeled by keeping its gain factor as unity. In that case the cable transfer function may redefined like below,

$$C(x) = 1.\ \frac{(s-z1)(s-z2)(s-z3)}{(s-p1)(s-p2)(s-p3)} \qquad 2.1$$

So no gain control block is needed and instead of using the filter blocks in summation, those blocks can be used in cascade and each filter block will have the appropriate pole and zero with a capability of automatic tuning of its pole and zero.

2.2 Cable Characterization:

Transmission line equations can be derived starting with the per-unit-length model as in [8] and shown in Figure 2.2. The elements r, l, c and g are all per-unit-length values. The two fundamental differential equations [9] for transmission line are,

$$\frac{d}{dx}V(x) = -(r + j\omega l).I(x) \qquad 2.2$$

and the current shunted between the lines in each section is,

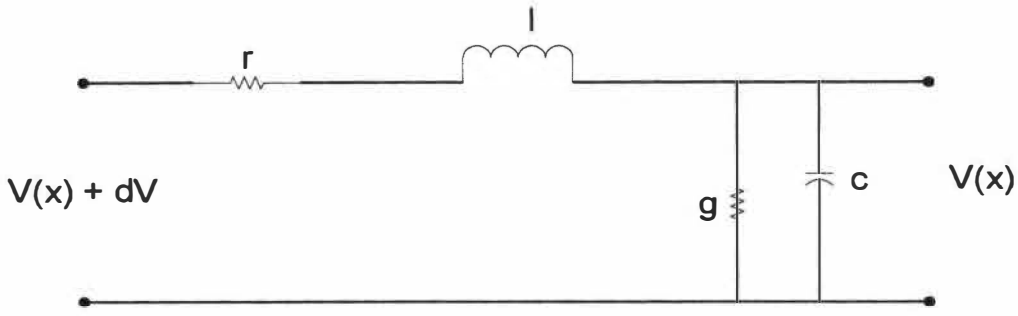

Figure 2.2: Modeling of transmission line

$$\frac{d}{dx} I(x) = (g + j\omega c).V(x) \qquad 2.3$$

Taking the derivative of equation 2.2 and using equation 2.3 gives,

$$\frac{d^2V}{dx^2} = (r + j\omega l) \,.\, (g + j\omega c) \,.\, V(x) \qquad 2.4$$

solving,

$$V(x) = V_A e^{-\gamma x} + V_B e^{\gamma x} \qquad 2.5$$

where γ is the propagation constant and V_A, V_B are the amplitude of the forward and reverse traveling signals respectively. In a properly terminated transmission line, the reverse traveling signal is zero so that the transfer characteristic is given by,

$$C(s) = e^{\gamma L} \qquad 2.6$$

where L is the length of the line. γ is called the propagation constant. Now the series impedance elements can be written as,

$$Zs = (r + j\omega l) \tag{2.7}$$

And the parallel admittance can be written as,

$$Yp = (g + j\omega c) = \frac{1}{Zp} \tag{2.8}$$

So, if Z_T is the characteristic impedance then the total impedance is,

$$Zin = Zs + \frac{ZpZ_T}{Zp + Z_T} = Z_T \tag{2.9}$$

Now, solving for Z_T, we get,

$$Z_T = \sqrt{ZsZp} = \sqrt{\frac{r + j\omega l}{g + j\omega c}} \tag{2.10}$$

It is shown in [9] that per unit propagation constant γ can be written as,

$$\gamma = \sqrt{ZsYp} = \sqrt{(r + j\omega l)(g + j\omega c)} \tag{2.11}$$

$$= \sqrt{rg - \omega^2 lc + j\omega(gl + rc)} \tag{2.12}$$

$$= \sqrt{\{\omega^2 lc[\frac{rg}{\omega^2 lc} - 1 + \frac{j\omega}{\omega^2 lc}(gl + rc)]\}} \tag{2.13}$$

$$= \sqrt{-\omega^2 lc}\{1 - [\frac{rg}{\omega^2 lc} + j\omega(\frac{g}{\omega^2 c} + \frac{r}{\omega^2 l})]\}^{1/2} \tag{2.14}$$

It is assumed that the losses are small but not necessarily negligible, which implies that $r << \omega l$ and $g << \omega c$. Then equation 2.14 can be written as,

$$\gamma = \sqrt{-\omega^2 lc} * \sqrt{1 - v} \tag{2.15}$$

where $v << 1$. Using the identity of $(1 + x)^{1/2}$, the equation 2.15 can be simplified to the form of ,

$$\gamma = \frac{r}{2\sqrt{l/c}} + \frac{g}{2}\sqrt{\frac{l}{c}} + j\omega\sqrt{lc}\left(1 + \frac{r}{8\omega^2 l^2} + \frac{g^2}{8\omega^2 c^2} - \frac{rg}{4\omega^2 lc}\right) \qquad 2.16$$

The resistance, r, is a frequency-dependant resistor with equal real and imaginary parts. The real part of the propagation constant is known as the attenuation constant and is given by,

$$\alpha = \frac{r}{2\sqrt{l/c}} + \frac{g}{2}\sqrt{\frac{l}{c}} \qquad 2.17$$

This can be written as,

$$\alpha = \frac{r}{2Z_o} + \frac{g}{2Y_o} \qquad 2.18$$

where $Z_o = \frac{1}{Y_o}$ is the characteristic impedance of the line and $Z_o = \sqrt{\frac{l}{c}}$. Thus, the real part of the series impedance, and the real part of the AC shunt admittance, contribute to the cable attenuation. The imaginary part of the propagation constant is the phase constant, given by,

$$\beta = \omega\sqrt{lc}\left(1 + \frac{r^2}{8\omega^2 l^2} + \frac{g^2}{8\omega^2 c^2} - \frac{rg}{4\omega^2 lc}\right) \qquad 2.19$$

Then we have,

$$\gamma = \alpha + j\beta \qquad 2.20$$

The velocity of propagation is $v = \frac{\omega}{\beta}$. At low frequencies, when the condition $r << \omega l$ is no longer true, the velocity of propagation is reduced. This dispersion effect can cause the

high-frequency signal components to pass along the cable faster than the low-frequency components. However, for high-speed data transmission, the frequency content of the signal is high enough that the low frequency dispersion effect is not evident.

To find the frequency dependence of attenuation, it is important to take into account the increase in series resistance at higher frequencies due to skin effect. The series resistance per unit length is given by,

$$r = \frac{1}{\sigma A} \tag{2.21}$$

where σ is the conductivity of the wire and A is the cross-sectional area containing the current. At low frequency the conduction area is πr^2_w where r_w is the wire radius. When the frequency of signals on the cable is high enough that conduction occurs near the surface of the conductor, the series resistance (r), can increase significantly. At high frequencies, the skin effect causes the current to conduct only to skin depth, δ, given by [10],

$$\delta = \sqrt{\frac{1}{\pi f \mu \sigma}} \tag{2.22}$$

where μ is the conductor relative permeability. Then the cross-sectional area containing the current is $2\pi r_w \delta$, causing the series resistance to be frequency dependent according to [8],

$$r_{ac} = \frac{1}{\pi r_w} \sqrt{\frac{\mu}{8\sigma}} \sqrt{\omega}(1+j) \tag{2.23}$$

Using the real part of r_{ac} in place of r in equation 2.18 results in

$$\alpha = k_1\sqrt{\omega} + k_2\omega \qquad 2.24$$

where k_1 and k_2 are independent of frequency.

To get an idea of the relative contribution of the dielectric losses, it can be shown that the dielectric losses and skin effect contribute equally to the attenuation at 15GHz. At this frequency, each term contributes 92dB to the attenuation. Since this frequency is beyond the usable range, another figure of merit at a lower frequency will be useful. This is the frequency where the dielectric loss term contributes 3dB to the attenuation, and is found to be 487MHz. Since this frequency is still very high, the second term in equation 2.24 can be ignored. So equation 2.24 will become,

$$\alpha = k_1\sqrt{\omega} \qquad 2.25$$

So the cable transfer function can be written as

$$C(x) = \exp(-(L.\, k_1.\sqrt{\omega})) \qquad 2.26$$

Note that the linear phase term due to β has been neglected since it is simply a delay for all frequency components and does not contribute to distortion. The phase term introduced by the $j\omega$-term is accurate in modeling the imaginary part of the resistance variation due to skin effect.

2.3 Cable Transfer Function Design

The cable transfer function in equation can be written in terms of cable attenuation as follows,

Table 2.1: Cable attenuation in dB for different length of cable in different frequencies

Frequency MHz	450 feet of cable	900 feet of cable	1800 feet of cable
11	-3.72dB	-7.58dB	-14.32dB
22.4	-5.32dB	-10.81dB	-21.04dB
33.3	-6.42dB	-12.62dB	-25.82dB
44.6	-7.64dB	-15.61dB	-30.17dB

$$C(x) = \exp(-L.a.(1+j).\sqrt{\omega}) \quad 2.27$$

$$\text{where, } a = \text{abs}\left[\frac{\log(attenuation)}{L.\sqrt{\omega}}\right] \quad 2.28$$

$$\text{And, attenuation} = 10^{(\text{attenuation in dB})/20} \quad 2.29$$

The attenuations in dB for the Belden 728A coax cable are tabulated in Table 2.1 for few frequencies. From the above table, it is evident that for a particular frequency, the cable attenuation in dB is linearly proportional to its length. Figure 2.3 is showing the linear relationship between cable attenuation in dB and its length for the frequency of 25 MHz. Using this linear relationship and using the equations 2.27, 2.28 and 2.29 a set of

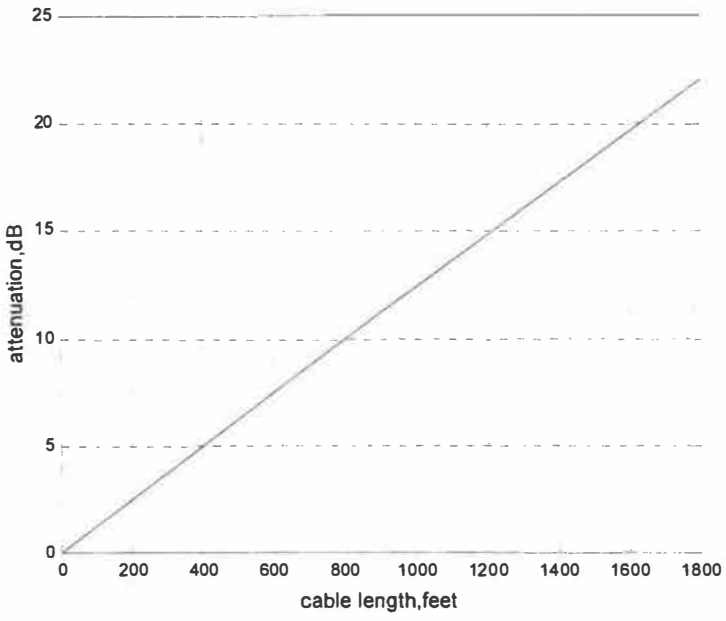

Figure 2.3: Linear relation between cable attenuation and length

attenuation curves for 100 feet to 900 feet of cable are drawn for frequency range of 10KHz tol00MHz. The curves are shown in Figure 2.4. The bottom curve in the figure 2.3 is for 900 feet and so on with 100 feet of decrement.

A MATLAB [12] curve fitting routine program has been used to fit those curves assuming a cable transfer function as equation 2.1 which is written below again.

$$C(x) = 1.\ \frac{(s-z1)(s-z2)(s-z3)}{(s-p1)(s-p2)(s-p3)} \qquad 2.30$$

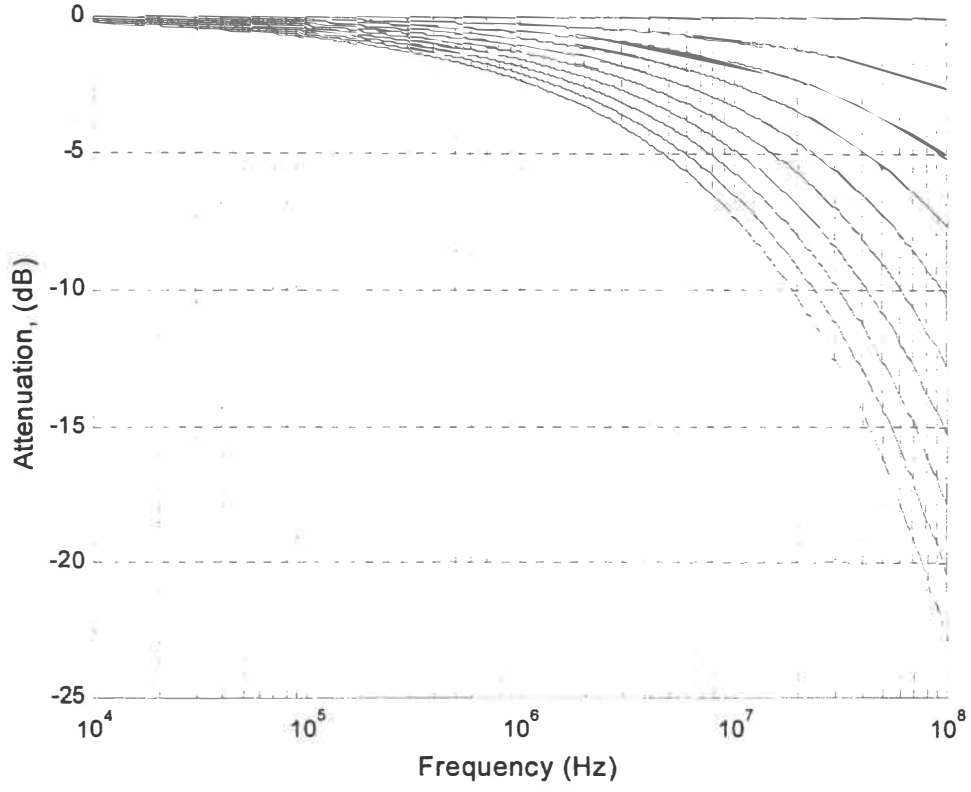

Figure 2.4: Ideal attenuation curves for 100- 900 feet of cable

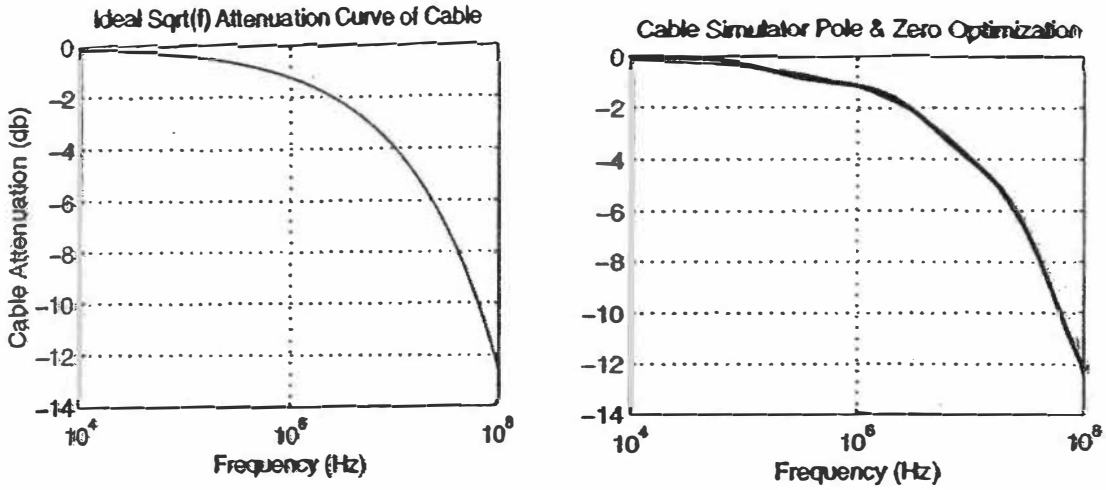

Figure 2.5: Ideal curve versus fitted curve

where the gain factor K is set to 1. So this technique will give us a unique feature to design a filter stage using only the poles and zeros without any gain stage to control K.

In the MATLAB program, initial guess of three sets of poles and zeros are taken as input for a particular length of cable-transfer function curve and the curve fitting routine fits that curve using those initial guess and when the fitting is done, program gives three sets of poles and zeros which are the best possible results of poles and zeros for that curve. Figure 2.5 is showing the ideal curve and the fitted curve. There is some error in fitting which is less than ±0.5dB.

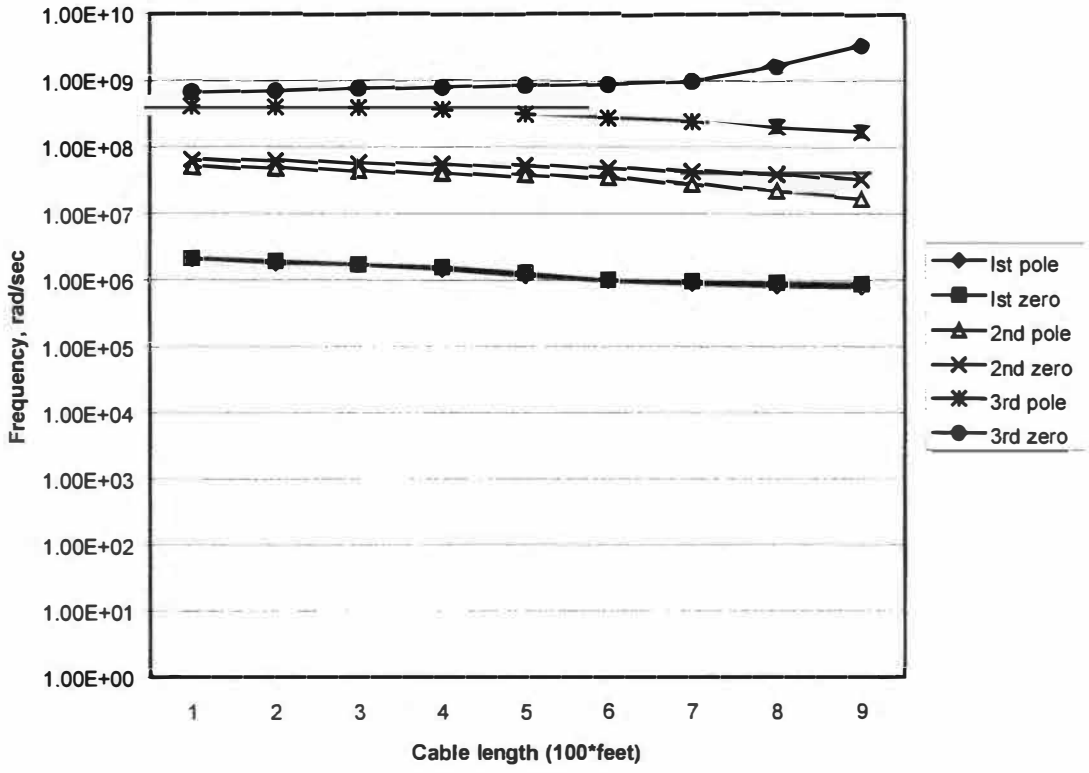

Figure 2.6: Pole zero variation of cable transfer function with cable length

Figure 2.6 shows the pole-zero variation with the cable length. This figure is important, as it shows that, except the third zero, all poles and zeros are decreasing almost linearly with increasing cable length. So using this linearity, an adaptive cable equalizer system is possible, which can estimate the length of cable in its input and accordingly change the equalizer-filter poles and zeros. The equalizer poles and zeros are the zeros and poles of the cable respectively as the equalizer transfer function is the inverse of the cable transfer function which is given by,

$$E(x) = 1.\ \frac{(s-p1)(s-p2)(s-p3)}{(s-z1)(s-z2)(s-z3)} \qquad 2.31$$

2.4 Proposed System Diagram

The system block diagram is shown below in Figure 2.7. The output signal from the cable is fed to a voltage to current converter (OTA) as well as to a Gm-C filter. The output of the OTA is rectified by a rectifier, which is compared with a reference voltage to estimate the cable length. The rectified voltage for the zero cable length is set equal the comparator reference voltage, but for all other length of cable, the rectified output voltages will be less than reference voltage and the comparator output will be proportional to this difference of the voltages. The comparator output will be divided into three different voltages to be used to tune the three stages of the Gm-C filter to provide appropriate pole and zero for each stage.

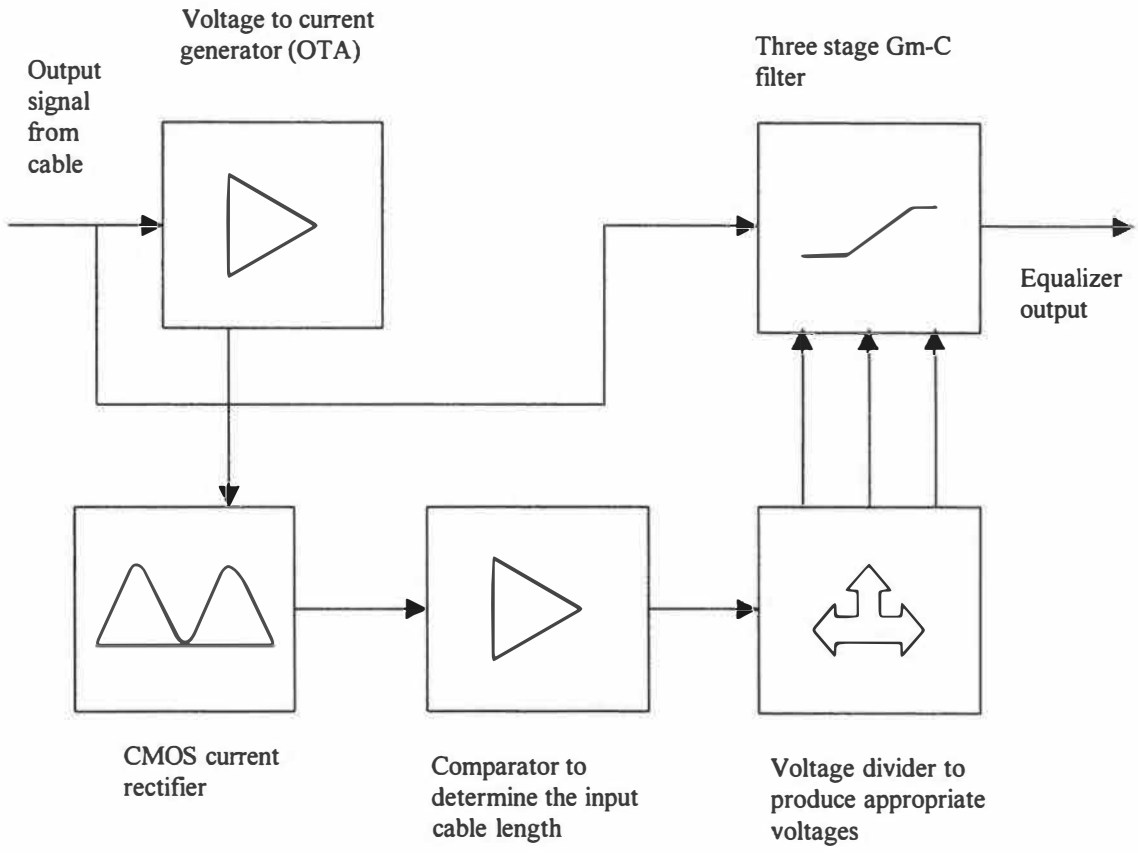

Figure 2.7: Equalizer system block diagram

The peak detector, which consists of the OTA, rectifier and comparator, works on the basis that the attenuation for different cable length at a particular frequency is known. The following Table 2.2 shows the output voltages for 200mV (peak) input voltage at different length of cable at a frequency of 25MHz. Here, the OTA, rectifier, comparator and the voltage divider are designed to be linear, so is possible to use the linearity of the pole-zero variation of the equalizer transfer function in the filter stage. A cascaded three-stage filter is used to get the desired pole-zero and thus the desired transfer function as Figure 2.8.

Table 2.2: Output signal levels of 200mV peak input signal for different length of cable

Length of cable (feet)	Attenuation (dB)	Output signal of cable (mV)
500	6	100
600	7.2	87.3
700	8.4	76
800	9.6	66
900	10.8	57
1000	12	49

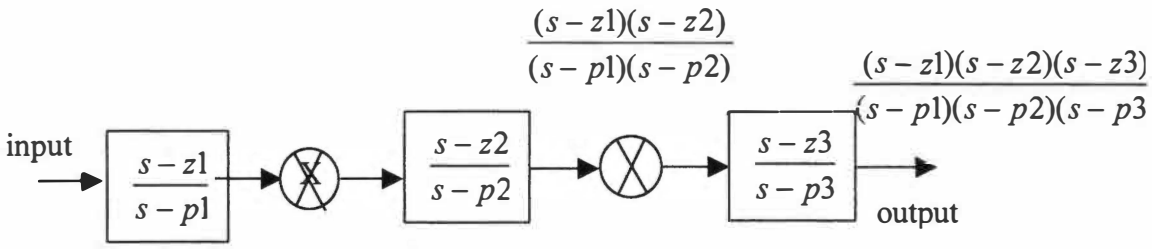

Figure 2.8: Three cascaded filter stages with their appropriate poles and zeros

As the gain factor (k) in the cable transfer function is 1, the equalizer transfer function response will be inverse of that of the cable transfer function. Figure 2.9 is showing the ideal equalizer response needed for the equalizer system. So the designed adaptive equalizer should be able to produce response as close as those of ideal ones.

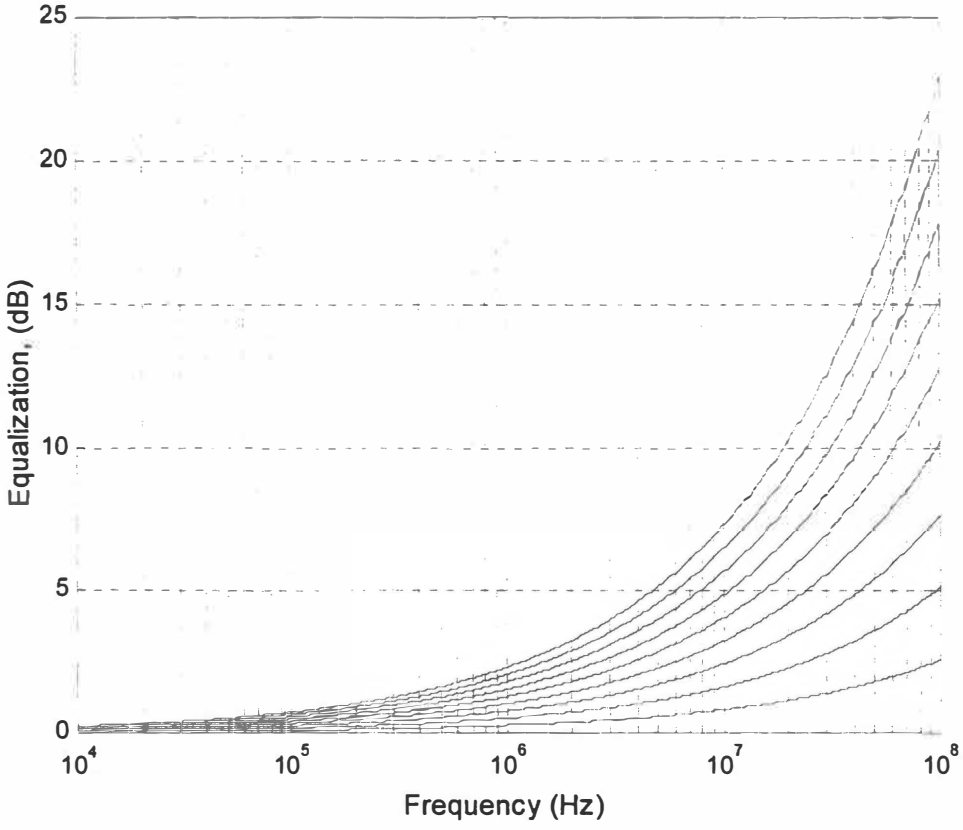

Figure 2.9: Ideal response of the equalizer for 100- 900 feet of cable

CHAPTER 3

Circuit Design

This chapter describes all the circuits needed for the equalizer system that was describes in Chapter two.

3.1 Bias Circuit Design

A good and reliable current generator is crucial in any analog circuit design. A CMOS version of a self-biasing Widler current source [8] is chosen in this design. This consists of MOS transistors of N1, N2, P1, P2 and a resistor Rbias. Cascode devices are used to improve the output impedance [12]. The bottom devices are designed with minimum allowable channel length (.6μm). Cascode devices, with slightly larger channel length (.8μm), are used in order to provide higher output impedance than a single device could provide. For example, a 100μA current source has a low frequency output impedance of 20KΩ if generated from a single transistor of minimum length. This value increases to 4MΩ when a cascode device with slightly larger than minimum length is added. Figure 3.1 shows the bias circuit and the startup circuit, which will be described later. The n-

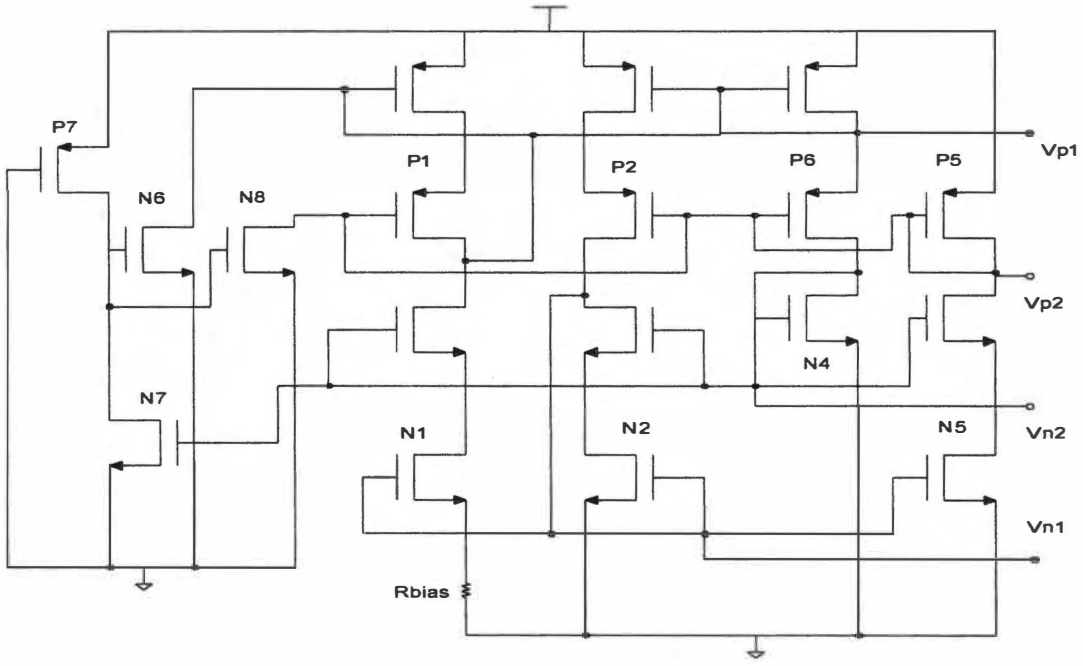

Figure 3.1: Constant transconductance bias current generator

channel cascode devices have a gate voltage generated by diode-connected NMOS transistor N4. This reference level is chosen high enough so that the gate-source voltage of the top device of N2 causes the bottom device N2 to be operated in saturation just beyond the triode region. This allows the cascode current-mirror output to operate within a few hundred millivolts of the supply voltage. Similarly, the p-channel cascode devices have a gate reference voltage generated by diode-connected PMOS transistor P5. Then, the voltage on current mirrors biased from this reference circuit can be as low as the sum of the saturation voltages of the two-stacked devices.

The significance of this bias-circuit arrangement is that it generates a current, which causes the devices to have a transconductance determined by the conductance of the resistor, Rbias. Then any device in the circuit, which uses a current generated by the reference voltages of this bias circuit, will also have a transconductance determined by Rbias. A first order analysis shows that the transconductance of device N2, in Figure 3.1, will be exactly equal to the conductance of Rbias. Furthermore, this transconductance is significantly independent of supply voltage, temperature, and process variations. A second-order analysis shows that mobility degradation, finite output impedance, and body effect, alter the result of the first-order analysis. The effects of mobility degradation and finite output impedance are only a few percent, but the body effect causes the transconductance of N2 to be only three quarters of the conductance of Rbias. The body effect is the main reason for the transconductance to be dependent on the process and temperature. However, the device transconductance is still proportional to the conductance of Rbias.

3.1.1 Startup Circuit

There is always a possibility that the bias current may be zero at the startup of the circuit in all self-biased circuits. The startup circuit, which is shown in Figure 3.1 ensures that the bias circuit does not latch into a zero-bias current mode on power up. When the supply voltage is high enough to turn on P7, V_{p1} and V_{p2} will be pulled low by N6 and N8 until V_{n2} is high enough to turn on N7. Then the bias circuit will operate in the desired mode.

3.1.2 First-Order Analysis

Since the drain currents of N1 and N2 are forced to be equal by the P1, P2 current mirror, [8] we can write,

$$\frac{\mu_n Cox}{2}(W/L)_1 V^2_{eff1} = \frac{\mu_n Cox}{2}(W/L)_2 V^2_{eff2} \qquad 3.1$$

Summing voltages gives

$$I\,Rbias + V_{eff1} = V_{eff2} \qquad 3.2$$

Since, $V_{gsi} = V_t + V_{effi}$

Also, the transconductance of N2 is $g_{m2} = \frac{\partial I_2}{\partial Vgs_2}$ or

$$g_{m2} = \frac{2I_2}{V_{eff2}} \qquad 3.3$$

Substituting V_{eff1} from equation 3.1 into equation 3.2, and then $I_1 = I_2$ from equation 3.2 into equation 3.3, results in

$$g_{m2} = \frac{2\left(1 - \sqrt{\frac{(W/L)_2}{(W/L)_1}}\right)}{Rbias} \qquad 3.4$$

If $(W/L)_1$ is chosen four times larger than $(W/L)_2$ the result simplifies to

$$g_{m2} = \frac{1}{Rbias} \qquad 3.5$$

Thus the transconductance of N2 depends only on the value of resistor, Rbias.

3.1.3 Error due to Body Effect

The body effect causes the threshold voltage of a device to change if the device source node is at a different potential than that of the device body. For an n-channel device in a p-type substrate, the threshold voltage increases when the source voltage is higher than the substrate voltage. In the bias circuit of Figure 3.1, device N2 does not suffer from the body effect, but N1 does.

The main division from the first order analysis is due to the body effect on N1. The standard method of eliminating the body effect on a device is to connect the device bulk to the device source. In a standard n-substrate process, this can be done with the n-channel devices. However, with the more common p-substrate process, the n-channel device is not available in a well and cannot have its bulk connected to its source. Then the body effect can be eliminated by connecting the bias resistor between V_{DD} and the source of a p-channel device. Then the p-channel devices in the circuit will have their transconductance determined by the bias resistor. The n-channel devices will have a transconductance related to the p-channel transconductance according to [8],

$$g_{mn} = \sqrt{\frac{\mu_n (W/L)_n}{\mu_p (W/L)_p}}\, g_{mp} \qquad 3.6$$

If the p-channel devices are now process and temperature independent, the n-channel devices will have a residual dependence proportional to the square root of the ratio of mobility.

The disadvantage of the constant-transconductance bias circuit is that the bias current, and device saturation voltage can change significantly for the given variations. For example, the bias current, and hence the chip power will increase by fifty percent for an eighty degree temperature rise. An increase in device saturation voltage can reduce the signal voltage headroom.

In the implementation of this bias circuit, the resistance is chosen to be 3.57 K Ω for Rbias with 200 Ω on-chip and the remainder off-chip. The on-chip resistor is used to improve the stability margin of the N1, N2, P1 and P2 feedback loop. Most of the resistance is placed off-chip so that a surface-mount resistor, with its better accuracy and temperature characteristics, can be used.

3.2 Input Cable length detection

A peak-detector circuitry, which consists of a voltage to current generator, a rectifier and a comparator, is used to estimate the input cable length of the equalizer. The amplitude is detected by converting the input voltage to current, rectifying the current, and integrating it on a capacitor. Figure 3.2 shows the basic principle of amplitude detection. Linearity is important in the peak detection. So a linear voltage to current converter is needed. A current rectifier topology is also selected.

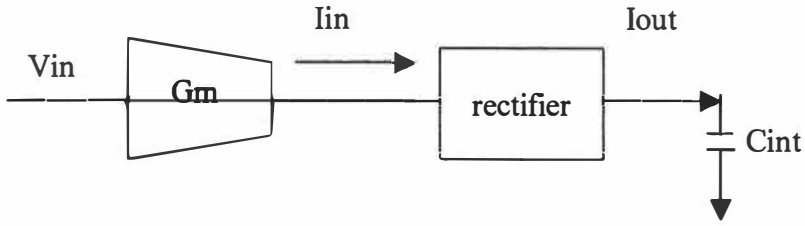

Figure 3.2: Block diagram for the peak detection technique

3.3 OTA Design

A voltage to current converter (OTA) [13] is selected so that it can produce linear current with the input voltage. The OTA circuit is shown in Figure 3.3. As the output of the OTA is the input of the rectifier, the circuit is designed in such a way that the loading effect is minimum.

3.4 Rectifier Design

The current rectifier topology used in this project is shown in Figure 3.41 [4]. Here two half wave rectifiers (N1,N3 and N2,N4) are driven by the opposite output phases of an

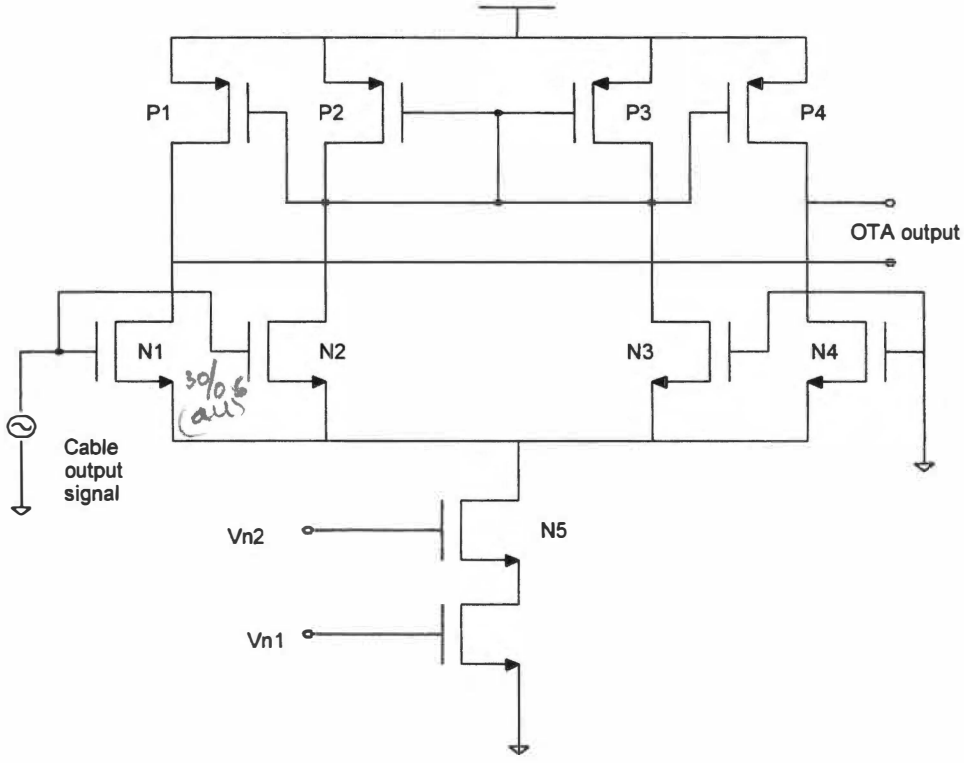

Figure 3.3: Linear OTA circuit

OTA with a differential output. Their outputs are summed. When one output of the OTA drives positive current into one halfwave rectifier, the other output will draw negative current from the other half wave rectifier. There will always be one halfwave rectifier drawing current from the output. Therefore, the OTA and the two half wave rectifiers make up a full wave current rectifier. The advantage of this strategy is that there is no inherent source of non-linearity anywhere in the rectifier. A bias current (P1a, P1b and Na, Nb) is introduced to decrease the voltage swing at the input of the rectifier. In that case the input transistors do not completely switch off during the zero crossing of the input current. One of the transistors of a half wave rectifier will only switch off when the other one, conducting the current during that half period is completely on. The bias current adds extra current to the output current of the rectifier. This creates an error on the integrated output voltage because extra current will be integrated as long as the non-conducting transistor in each halfwave rectifier is not completely off. The OTA is designed to be linear and the output current of the OTA is rectified and this extra bias current is added every time with the rectified current. So the total current, which will be integrated in a capacitor, is considered to be the rectified current plus the extra current for any OTA output current and thus this extra current is a non-issue in this design. The bias current can be decreased until the transistors operate in the weak inversion region. In this design, the bias current is set to be 3.5μA. A reference level is created by source follower N5, along with current source N9a and N9b, to set the allowable input voltage to be compatible with the voltage level that the OTA output can provide.

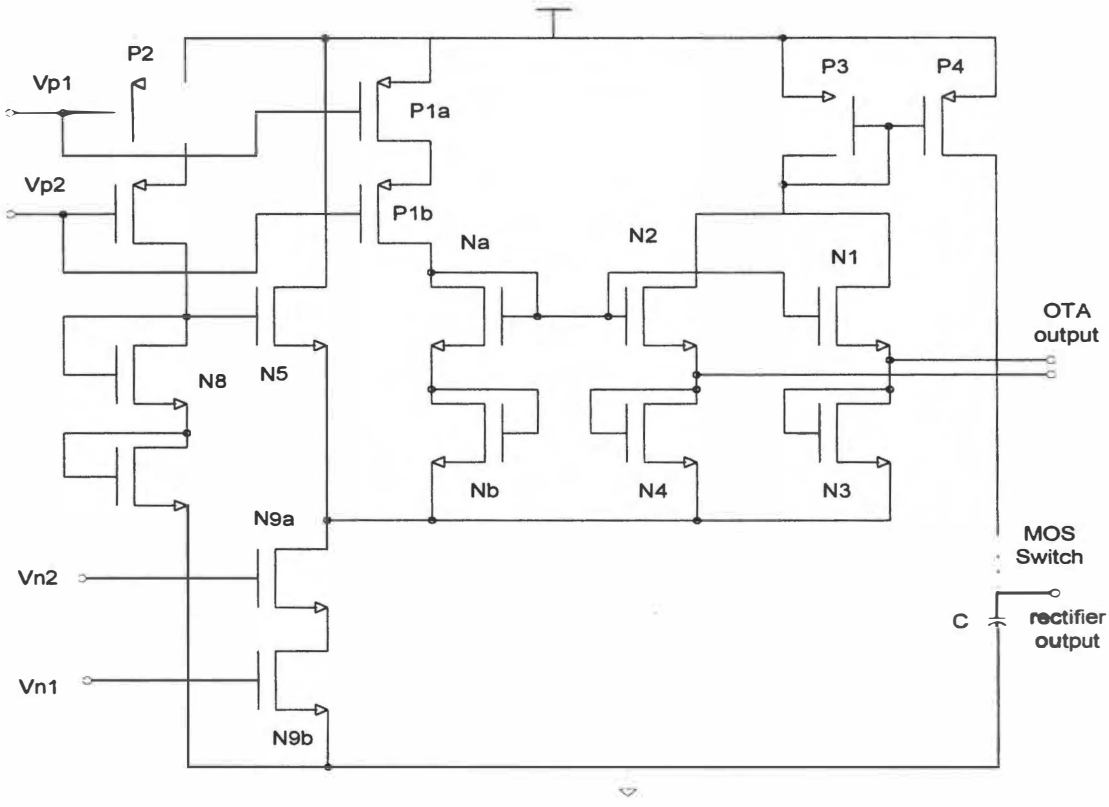

Figure 3.4: Rectifier circuit with lifted input bias voltage

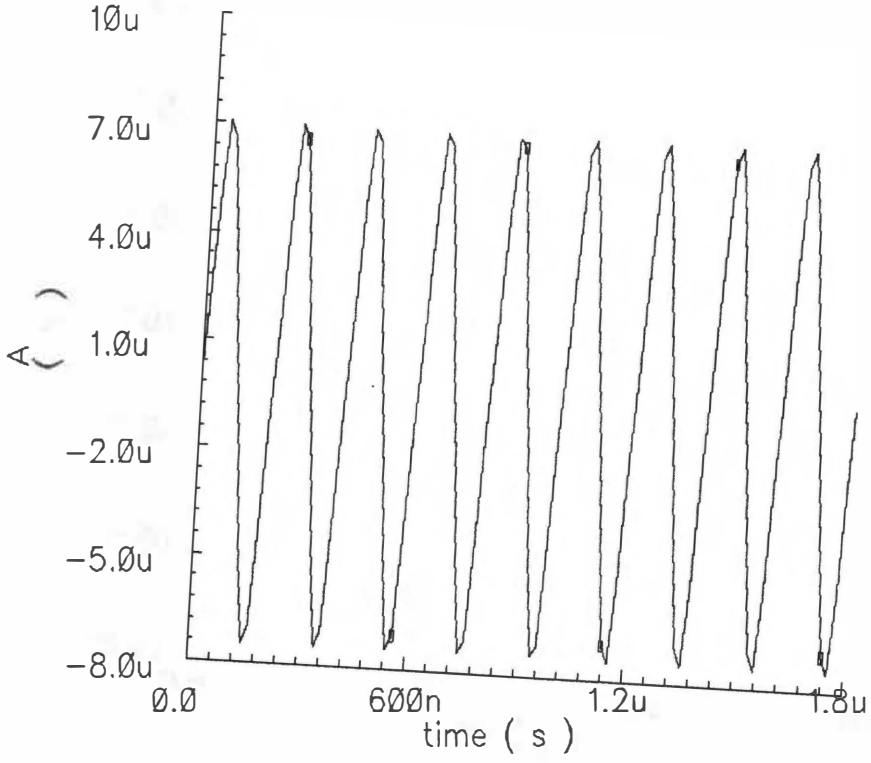

Figure 3.5: Input signal to the rectifier (output signal from the OTA)

To integrate the current on the capacitor a current mirror is used. The integrated output voltage is given by

$$V_{out} = \frac{1}{C}\int_0^{NT} I_{rect}\sin(\frac{2\pi}{T}t)dt \qquad 3.7$$

where T is the period of the input signal, N is the number of integrated periods, and I_{rect} is the amplitude of the rectified current.

The mirror, P4 is designed such a way that the rectified current to the integrating capacitor is large enough and will be comparable to the reference voltage that will be

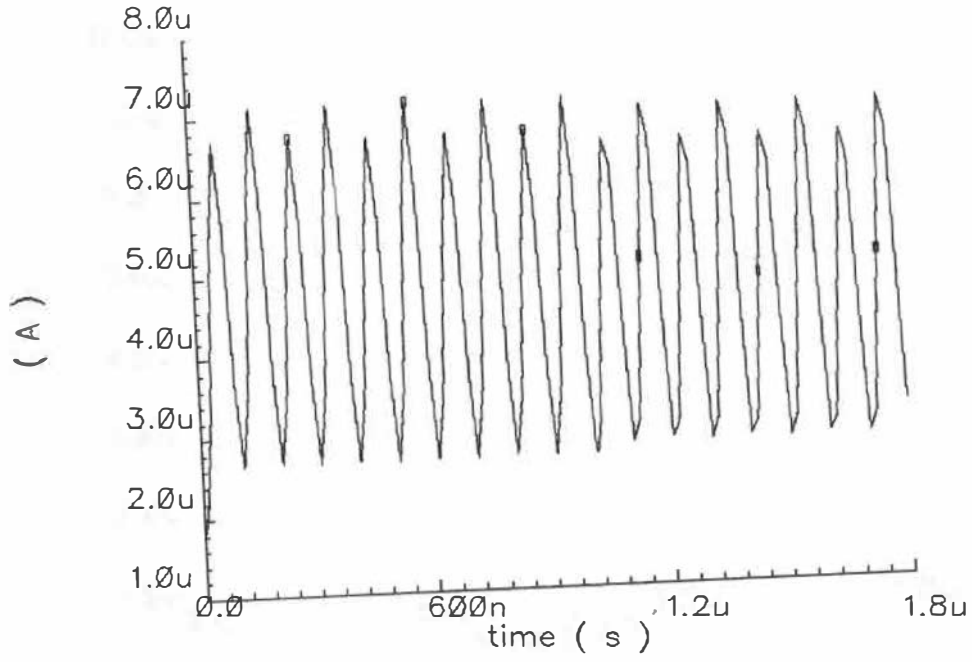

Figure 3.6: Output current after rectification

used in the comparator and will be described in the later sections. The input and output current of the rectifier is shown in Figure 3.5 and Figure 3.6. From the Figure 3.6, it is evident that, 6μA, 1Mhz input current into the rectifier is rectified on 2.5μA bias current through N9a. This bias current cannot be avoided and has no effect on the overall rectified voltage. Again output current is less than input current because the bias current through P1a, b is deducted from the output current.

From equation 3.7, it is clear that rectifier output voltage can be controlled by changing the value of the capacitor, or changing the I_{rect} or taking different number of the input current cycles. In this design, the reference voltage in the comparator is set to be 842mV.

So the value of the I_{rect}, capacitor and the number of the input current periods are set such a way that, 400mV(p-p), 25Mhz input signal to the equalizer will produce 842mV output voltage to the rectifier. The reason of doing this is that, the 25MHz input carrier to the cable is 400mV(p-p) and thus if the cable output is also 400mV(p-p) then it means that there is no loss in the cable, which is possible only when the cable length is negligible. But for any other length of cable, there will be some loss and the 400mV(p-p) signal will be attenuated. As the rectifier is designed to give output voltage linearly with the input voltage or current to the OTA, the rectifier voltage will be linear with the attenuated cable signal voltage.

Table 3.1: The rectified output voltages of different input peak voltages

Input peak voltage to the OTA or cable output voltage (mV)	Rectifier Output voltage (mV)
200	842
175	816
150	790
125	762
100	735
75	708
50	680

The Table 3.1 is showing the output rectified voltages for different attenuated cable input voltages. From the table, it is evident that, the output rectified voltage is linear with the cable output voltage. A switch is connected to the capacitor to set the number of cycles to be integrated on the capacitor. Here a clock signal with a pulse width of 1.3μs is given to turn off the switch. So the capacitor will be charged within 1.3μs and hold the voltage constant. This is the output rectified voltage. A typical NMOS switch can be used, but it has charge injection [15] and clock feed-through problems. So a T-switch can be used to counteract these problems. The problem of using a switch is that, first 1.3μs, the cable output data will be un-equalized. Figure 3.7 is showing the output voltage of the rectifier when the switch is off after 1.3μs.

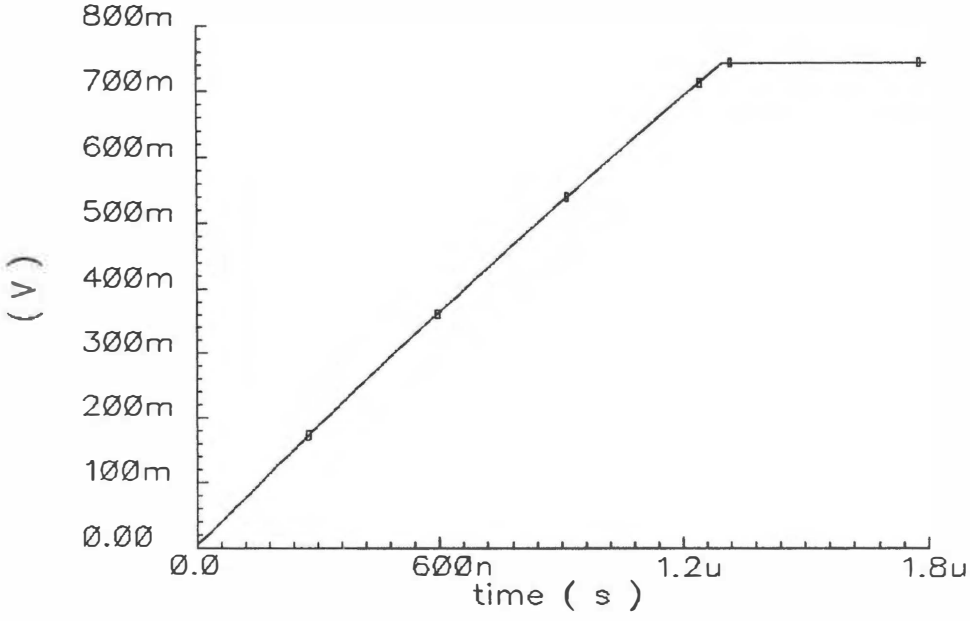

Figure 3.7: Constant capacitor voltage after the switch is off at 1.3us

3.5 Comparator Design

A source coupled pair differntial amplifier with PMOS current load [16] is used to design the simple comparator. This is shown in Figure 3.8. This circuit has excellent CMRR since any common mode currents in M1 and M2 drains tend to be cancelled by the active load at the output node. A capacitor is used to hold the output voltage of the comparator. A reference voltage of 842 mV is applied to one of the input device. The choice of this voltage is that, the bias current generator that was described earlier, will produce a reference voltage of 842mV and thus no separate reference voltage generator is needed. Again, this magnitude of voltage is big enough to drive the input device into saturation all the time. On the other input of the comparator, the rectifier output voltage is fed. As described in the previous section, this rectified voltage will be proportional to the output cable signal and for negligible cable length this voltage will be exactly 842mV. But with the increase of the cable length, this voltage will be decreasing linearly. So difference in the two input voltages of the comparator will be amplified and the capacitor that is connected to the output of the comparator will be charged with the output voltage of the comparator. For a difference voltage of V_{id} to the comparator will produce a difference of current ΔI_d, which is,

$$\Delta I_d = \mu_n \frac{C_{ox}W}{2L} V_{id} \sqrt{\frac{2I_{ss}}{\mu_n(C_{ox}W/2L)} - (V_{id})^2} \qquad 3.8$$

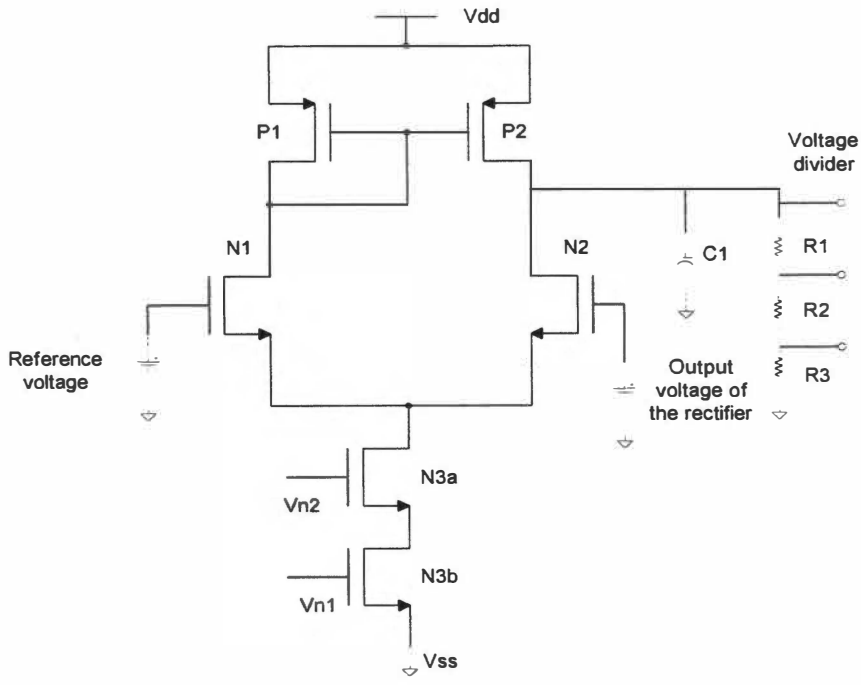

Figure 3.8: Comparator circuit with three- resistor voltage divider

So the difference in the output current will be linear with the difference of input voltage V_{id}. The expression is valid when both transistors are in the saturation mode of operation, which is true if,

$$|V_{id}| \leq \sqrt{\frac{I_{ss}}{\mu_n(C_{ox}W/2L)}} \qquad 3.9$$

So, for the MOSFET pairs, the range of V_{id} for which both devices are active is a function of device dimensions and bias current. It can be shown that the differential input voltage required to just turn off one of the transistors in the pair is $\sqrt{2}\,|V_{GS} - V_t|$ or $\sqrt{2}\,\Delta V_{GSQ}$ where,

$$\Delta V_{GSQ} = \sqrt{\frac{2I_D}{\mu_n C_{ox} W / L}} \qquad 3.10$$

For this design, the rectifier output voltage will be 690mV for the maximum cable length of 900ft. So the comparator NMOS transistors are sized and bias current are set, so that those two input NMOS can remain in active region when the maximum difference voltage to the input is 152mV (842mV – 690mV).

3.6 Filter Design

The most critical part of the equalizer design is to get the proper filter, which will give the desired transfer function. The transfer function of the desired equalizer while modeled in MATLAB was set as $1.\frac{(s-z1)(s-z2)(s-z3)}{(s-p1)(s-p2)(s-p3)}$, that is the gain factor K was set to be 1. So, a band-pass filter with a transfer function of $\frac{(s-z)}{(s-p)}$ with no gain term is needed.

Then using three stage cascaded band pass filter will give the desired transfer function. There are two main techniques for realizing integrated analog filters. One technique is the use of switched-capacitor circuits and the other is continuous time filtering. Switched-capacitor (SC) techniques are relatively difficult to implement in the higher ranges of operation for the following reasons [2]. (1) Sampling of signals occurs at many points inside the SC filter. Although the signal that is fed into the SC filter is band-limited, the noise that gets added to the signal internally often is not. These noise components get aliased into the baseband of the filter. (2) Switch feedthrough problems are severe at

higher clock rates. (3) High-frequency effects caused by improper amplifier settling, switch resistance, etc. are difficult to model and simulate for an SC realization. As no sampling is required, continuous time filters have a significant speed advantage over their switched-capacitor counterparts [17]. The filter co-efficients of the continuous time filter are determined by the product of two dissimilar elements, such as capacitance and the resistor (transconductor) values. Although continuous time filter has relatively poor linearity and noise performance, it does not create that much problem in the applications such as data communication and video circuits where distortion and noise performances are not too demanding.

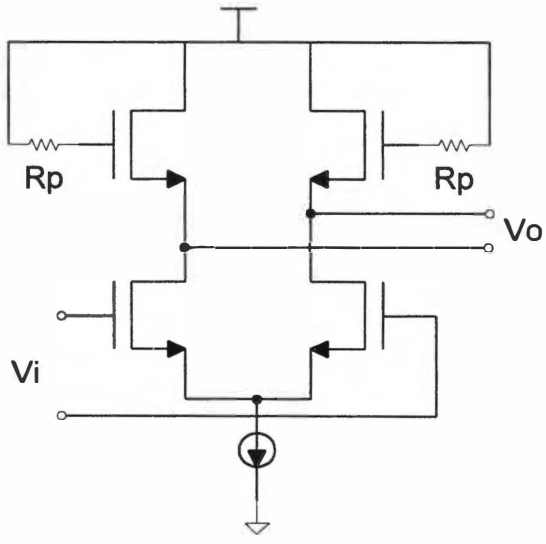

Figure 3.9: Gm-C filter topology selected for this design

For the equalizer filter design, few [18], [19] filter topologies have been investigated. The filter topology, that has been selected, is shown in Figure 3.9. This is source-coupled pair with enhancement-mode load [16]. This is essentially just a resistively loaded stage using another diode connected NMOS to form a nonlinear resistive load. This is often used in wideband amplifiers where low gain can be tolerated and the low resistance of the load results in large bandwidth for the stage. A resistor Rp is added between Vdd and the gate of the NMOS load device. This resistor along with the gate-source capacitance of the NMOS load device will provide the tuning capability for the filter. Figure 3.10 is showing the small signal model of the half circuit of the Figure 3.9. The model is simplified by neglecting the body effect parameter g_{mb}. The gate to source capacitance of the driver NMOS is neglected as the cable input has very small resistance of 75Ω for impedance matching. Summing the currents at the output node, we have,

$$g_{m2}V_o - \frac{Vo}{r_{o2}} - \frac{V_o}{Rp + Xc_{gs2}} - g_{m1}Vi - \frac{V_o}{r_{o1}} = 0 \qquad 3.11$$

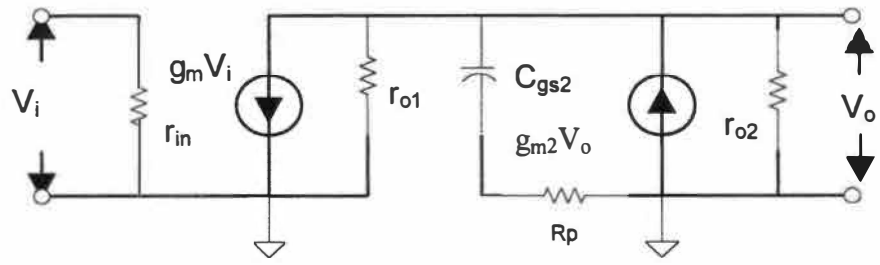

Figure 3.10: Small signal model derived for the half circuit of the filter topology

Solving, we obtain,

$$\text{Av} = \frac{Vo}{Vi} = \frac{-g_{m1}}{g_{m2} + \frac{1}{r_{o1}} + \frac{1}{r_{o2}} + \frac{1}{Rp + Xc_{gs2}}} \qquad 3.12$$

As r_{o1} and r_{o2} are large, neglecting $1/ r_{o1}$ and $1/ r_{o2}$. Again setting g_{m1} and g_{m2} equal, we get,

$$\text{Av} = \frac{1 + jwC_{gs2}Rp}{1 + jwC_{gs2}(\frac{1}{g_m} - Rp)} \qquad 3.13$$

So, the pole and the zero of the single filter stage is,

$$\text{Zero,} \qquad Z = \frac{-1}{C_{gs2}Rp} \qquad 3.14$$

$$\text{And pole,} \qquad P = \frac{-1}{C_{gs2}(\frac{1}{g_m} - Rp)} \qquad 3.15$$

Keeping C_{gs2} constant and changing Rp and g_m, we can obtain desired pole and zero. The complete filter stage is shown in Figure 3.11. Here three filter stages similar to Figure 3.9 are cascaded. The equalizer output is taken out from the third filter stage as a differential output. The gate resistances attached with the enhancement-mode load are shown as variable resistances. PMOS devices in triode region will be used in place of these resistors. Each filter stage will act as a band pass filter stage with band limited by their gate capacitance.

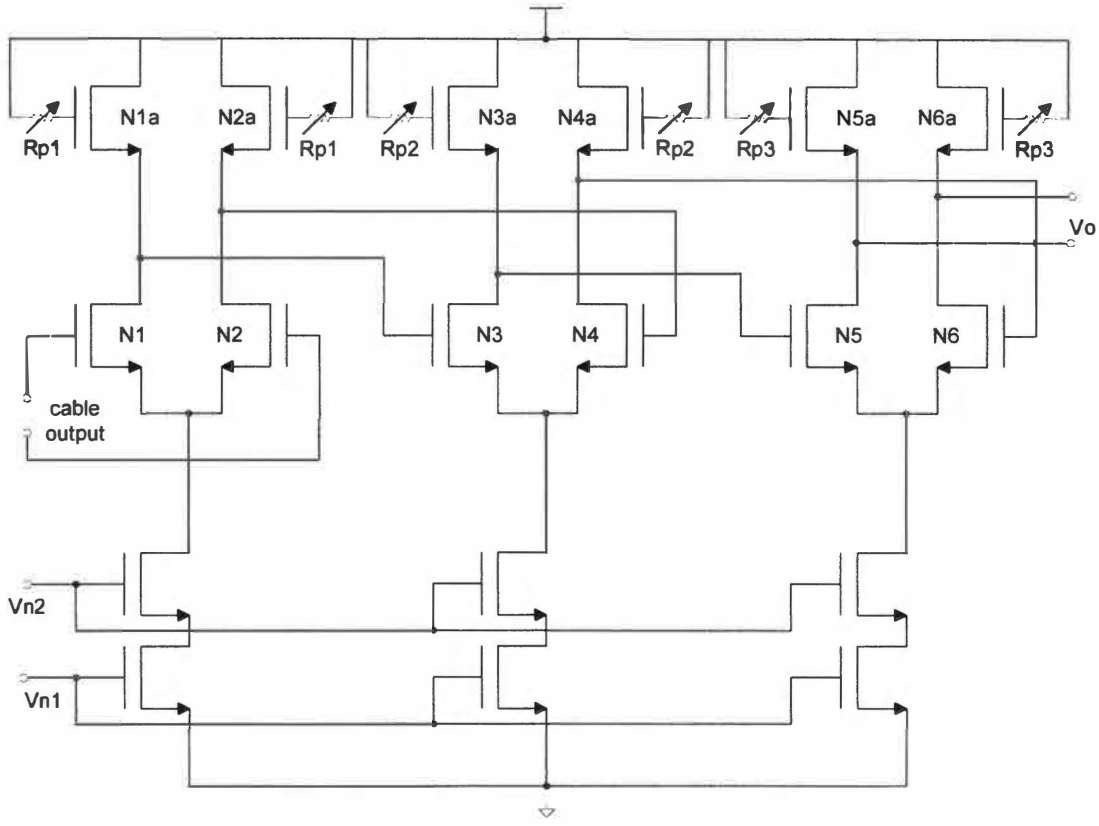

Figure 3.11: Complete filter circuit with Rp shown as variable resistance

From equation 3.14 and 3.15, we see that the zero is set by Rp alone and the pole is set by Rp as well as by g_m. Equation 3.15 can be written as

$$P = \frac{-1}{(\frac{C_{gs2}}{g_m} + C_{gs2}Rp)} \qquad 3.15$$

But, in the design, g_m is kept smaller than Rp so that first term in the denominator of equation 3.15 is smaller than second term. In that case, both zero and pole will be set by Rp alone. In fact, from Chapter Two, Figure 2.6, we can see that both pole and zero for 1st and 2nd sets of pole-zero are almost equal except for the third pole-zero. As third pole-zero are in higher frequency range, so their effect is small in the overall transfer function. So in first and second stage the value of g_m is set such a way that for a value of Rp which is derived for a specific zero, the corresponding pole value will be approximated to close enough to the exact value of the pole. Although the third pole-zero are splitting apart with the increase of the cable length, those are kept equal in this design. As described earlier, these higher frequency pole-zero will not effect that much to the equalizer transfer function. In Figure 3.12, three pass bands of the three stages make the transfer function for 900 feet of cable for bandwidth of 100Mhz.

3.7 MOS version of the variable resistors

A MOS device in triode region acts as a resistive device. A PMOS device is used in this

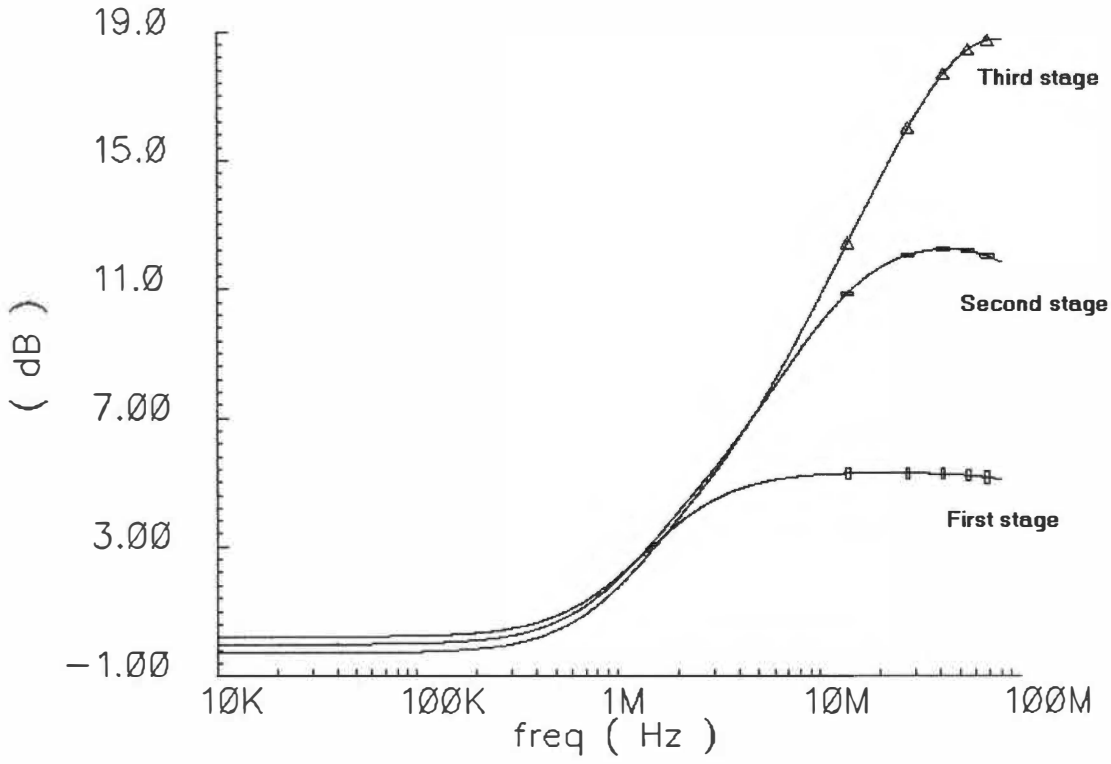

Figure 3.12: Output response of the three cascaded filter stages

A MOS device in triode region acts as a resistive device. A PMOS device is used in this design. A PMOS device is in triode region if,

$$V_{sg} \geq V_{thp} \text{ and } V_{sd} \leq V_{sg} - V_{thp}$$

The PMOS connection into the filter stage enhancement-mode load device is shown in Figure 3.13. From the figure above, it is evident that PMOS is always in triode region as there is no gate current in N3 so to P1. As no current is flowing through P1, so its V_{ds} is also zero, which ensures that this device is always in triode region. The on-resistance of this triode connected PMOS device is,

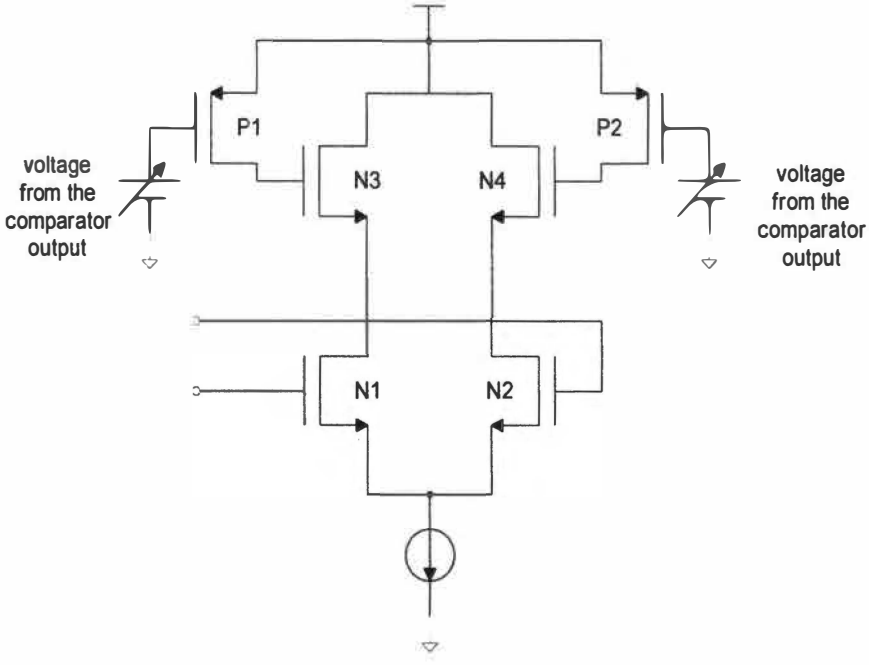

Figure 3.13: Variable resistance implementation by triode connected PMOS

$$Ron \approx \frac{1}{\beta_p(V_{sg} - V_{thp})} \qquad 3.16$$

where,β_p = Kp. W/L,

For a fixed W/L this Ron can be changed by changing V_{sg}. As source of P1 is always in V_{DD}, so applying a gate voltage to it (of course V_{sg} should be greater than V_{thp}) will change the on-resistance of PMOS transistor.

3.8 Resistor Voltage divider

Three off-chip resistors are used to divide the comparator output voltage. Figure 3.8 is showing the three resistors used to divide the output of the comparator. These three resistors will provide three different voltages to the gate of the triode connected PMOS devices in the filter circuit. From Chapter Two Figure 2.6 and equation 3.13 and 3.14 we know that, for every 100 feet of cable length, the values of the filter stage resistors increase 20KΩ, 12KΩ and 6KΩ for the 1st, 2nd and the 3rd stage respectively. Again, rectifier output voltage changes 10mV for every 100 feet cable. So the values of the resistors are set such a way that for every 10mV differential input voltage to the comparator, the three divider voltages are incremented enough to be capable of changing the resistance of the PMOS triode connected devices to the desired values. Simulation results show that using 3.5KΩ resistors will provide desired voltages to the triode connected PMOS devices in the filter stages. Table 3.2 shows the three divider voltages for every 10mV differential input increment.

Table 3.2: Voltage divider's output for every 10mV input voltage difference in the comparator

ΔV (mV)	R1 (Volt)	R2 (Volt)	R3 (Volt)
100	2.99	1.99	0.999
110	3.07	2.03	1.02
120	3.15	2.07	1.05
130	3.24	2.12	1.08
140	3.33	2.16	1.10
150	3.41	2.21	1.13

CHAPTER 4

Simulation Results

The circuit simulations of each stage were done using Spectre simulation tools [26] of CADENCE and HSPICE was used to verify the results of pole-zero model developed by MATLAB. The AMI 0.5μm CMOS process [20] was used to design all the circuit blocks. This non-silicided CMOS process has 3 metal layers and 2 poly layers, and a high resistance layer. The process is for 5volt applications. The minimum channel length of this process is 0.6μm and the minimum width is 1.95μm. This process uses SPICE level-11 model parameters. The resistors and the capacitors values used in this design are tabulated in Table 4.1 and the W/L values and drain currents of all the devices of each block are shown in Table 4.2.

Figure 4.1 is showing the frequency response of the equalizer filter output for cable length of 400 to 900 feet. In this figure, the top curve is for the 900 feet and the bottom one is for 400 feet of cable. For each 100 feet increase of cable length, the equalizer response increases about 2dB at 100MHz.

Table 4.1: Resistor and the capacitor values used in this design

Circuit Block	Device Name	Values
Bias Circuit generator	R1	3.57KΩ
Rectifier	C1	3nF
Comparator/Voltage Divider	R1	3KΩ
	R2	3KΩ
	R3	3KΩ
	C1	1pF

From frequency 10K to few hundred KHz there is attenuation of 0.273dB for all of the curves. This is due to the body effect of the driver MOSs of the filter stages. The attenuation is originally 3dB if g_m of both the driver and the enhancement-mode load is kept equal. But in the design, g_m of the driver is designed to be higher than g_m of the load devices to cancel out the lower frequency attenuation as much as possible. In fact, in the ideal response of the equalizer, there is very small gain in the lower frequencies. This simulated deviation from the ideal response in the small frequency range is less than 0.5 dB. The target cable length to be equalized was 100 to 900 feet, but from simulation result, it is evident that at 400 feet of cable or below, the curves loose its proper shape. The reason is that, the voltage divider output voltages are designed to be able to increase

Table 4.2: W/L and the drain currents of the devices used in each block of the design

Circuit Block	Device	W/L values	Drain Current
Bias generator	N1	40/0.6µ	44.4µA
	N2	10/0.6µ	48.77µA
	N4	6/1.95µ	48.04µA
	N5	10/0.6µ	49.35µA
OTA	N1, N4	30/0.6µ	102µA
	N2, N3	30/0.6µ	70.62µA
Rectifier	N1, N2	9/0.6µ	0.9µA
	P3	1.95/0.6µ	1.84µA
	P4	252/0.6µ	-----
	Na, Nb	4.95/0.6µ	3.8µA
Comparator	N1, N2	120/0.6µ	-----
Filter	N1, N2	250/0.6µ	586µA
	N3, N4	150/0.6µ	151µA
	N5, N6	120/0.6µ	80µA

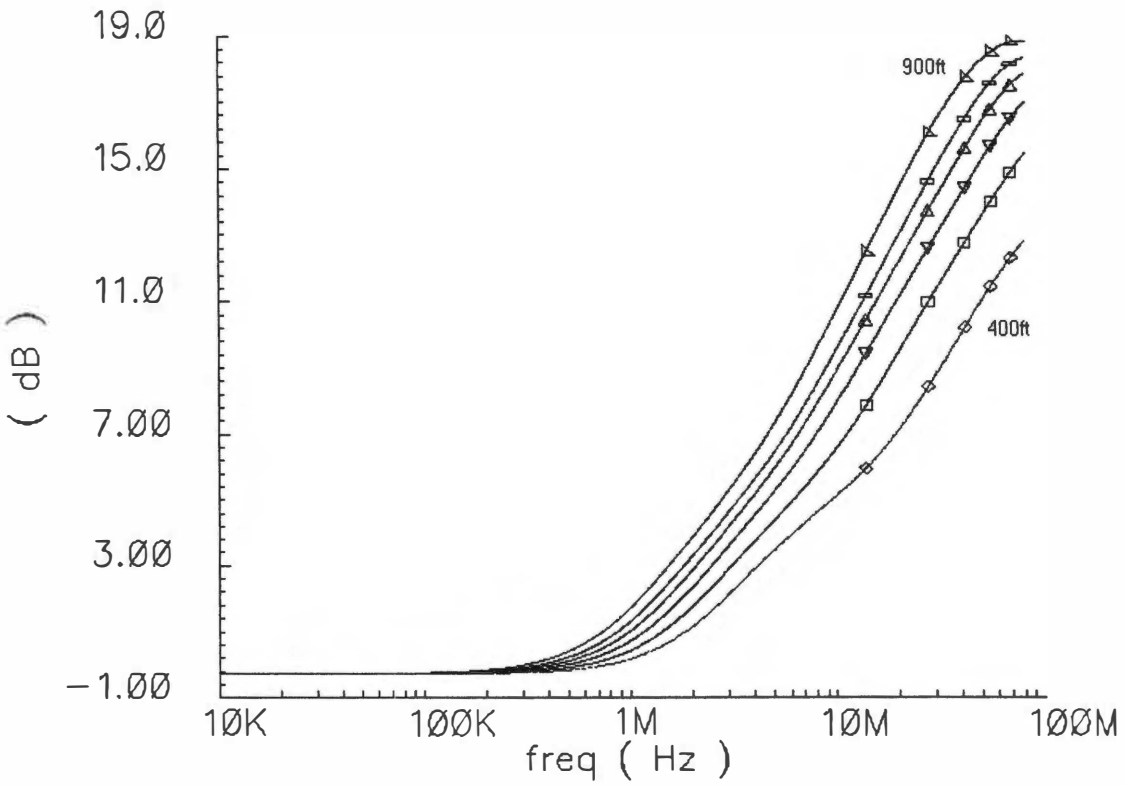

Figure 4.1: Equalizer output frequency response for 400-900 feet of cable

the on-chip resistors (triode-connected MOS) by 20 KΩ, 15 KΩ, and 10 KΩ respectively for the first, second and the third stage of the filter. But, in the range of 100- 400 feet of cable, the poles and zeros for these sets of curves are very close to each other and resistor values for these sets of curves do not require to be varied by 20 KΩ, 15 KΩ and 5 KΩ as it is required for the curve sets of 400-900 feet of cable.

Figure 4.2 is showing the input attenuated signal of 200mV (p-p) to the equalizer at 25 MHz and Figure 4.3 is showing the gain of 9dB attained at that particular frequency. Table 4.3 shows the deviation between the ideal response and the simulated response of 400 feet ideal equalizer curve and the simulated curve for different frequencies. As all

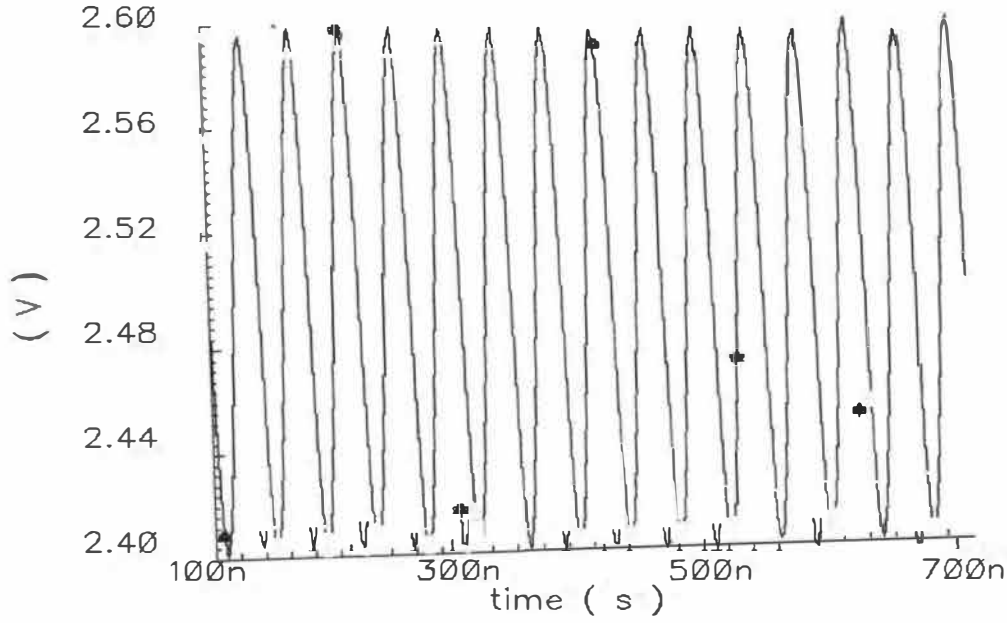

Figure 4.2: Input signal of 200mV (p-p) to the equalizer

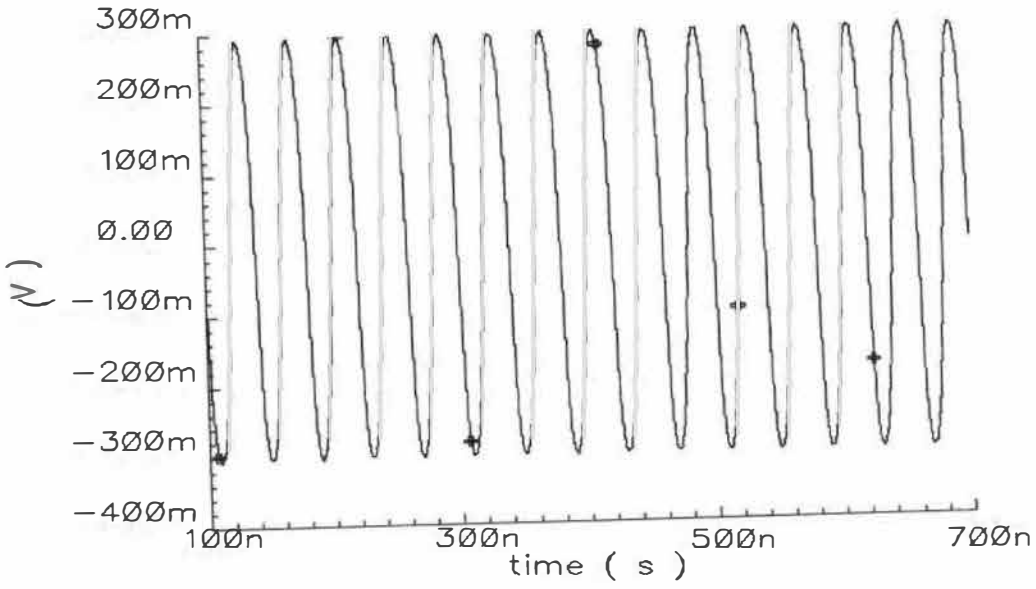

Figure 4.3: Equalizer output signal of 600mV (p-p) at 25 MHz

the curves are symmetrical, these results of deviation are also applicable for any other length of cable.

4.1 Off-chip Input and Output stage

The Belden coax 728A cable has a characteristic impedance of 75Ω. So for impedance matching, a 75Ω resistor will be used. Again, the input from cable is single ended but it will be applied differentially to the input of the filter.

The output buffer is used to drive off-chip load resistor. The choice of off-chip resistor value depends on the desired output amplitude, A and bandwidth, BW, which is given by

Table 4.3: Error between ideal response and the simulated response

Frequency of operation (MHz)	Ideal response (dB)	Simulated response (dB)	Error (dB)
1	1	0.5	0.5
25	5	6.5	1.5
75	8.5	9.5	1.0
100	10.2	11.8	1.6

[8],

$$R = \frac{1}{2\pi C.BW} \qquad 4.1$$

where R is the off-chip load resistor and C is the output-node parasitic capacitance.

CHAPTER 5

Discussion and Recommendation

A cable pole-zero model has been developed which shows that, poles and zeros of the cable transfer function decrease linearly with the increase of cable length. This important result helps to realize an adaptive cable equalizer where the poles and zeros for the equalizer filter can be changed linearly with the change of the cable length. Again, this linear relationship requires that all the building blocks in the equalizer system should be linear in behavior. Most of the building blocks for the overall equalizer system have been designed. CMOS process has been chosen to implement this equalizer system as CMOS process allows low-power, high density circuits to be used cost effectively. As the equalizer system is a part of the high-speed data communication transceiver, and most of the part of this transceiver is digital in function and they are all can be easily implemented in CMOS process, so if the analog part of this transceiver like equalizer is implemented in CMOS process, then the whole transceiver can be implemented in a single chip. While the pole-zero model for the cable-equalizer had been developed, the gain constant (k) for the cable transfer function was assumed to be one. So, the main

challenging part of the equalizer design is to design a filter which has a transfer function with gain constant one, so that, no gain controller (usually automatic gain controller) is needed. For this, few of the filter blocks have been investigated and the one which is described in section 3.7 of chapter three has been developed which gives only one pole and one zero without any gain term in its transfer function and thus help to realize the equalizer system without any gain controller which is predominantly used in today's equalizer systems. So, the system consists of an OTA, a rectifier and a comparator to detect the input cable length of the equalizer, a three-stage filter and a voltage divider to generate voltages to tune the poles and zeros of the filters. The circuit, which is not designed here, is the output stage. An output stage capable of driving the equalized data signal off-chip may be needed. It allows the equalizer circuit to operate as a stand-alone chip. If the equalizer drives a decoder and clock recovery circuit, which is on the same chip as the equalizer, then an output driver is not needed.

5.1 Future Work

The pole-zero model for the cable-equalizer was developed using 3 poles and 3 zeros. The first thing that can be done, is to investigate the pole-zero model using more than 3 poles and 3 zeros It is evident that, the more the poles and zeros the better the curve fitting is on MATLAB.

This equalizer system is developed for a single carrier frequency, which is known and can be detected. Using that frequency, the input cable length has been estimated. The

system can also be designed where multiple channel frequencies can be detected and these can be used to estimate the input cable length.

In the design of the rectifier, a switch is used to facilitate the capacitor to be charged for a certain time. For this time, the output data of the cable will remain un-equalized. So other system topology or circuit can be developed to avoid this problem.

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APPENDICES

APPENDIX A

Integrated Adaptive Cable Equalizers

Because of it's demand in data communication, integrated circuit (IC) for adaptive cable equalizer is widely developed by many companies for long time. Here is a brief description of few of those that are widely used.

National Semiconductor's CLC014 adaptive cable equalizer is a low-cost monolithic solution for equalizing data transmitted over cable (or any media with similar dispersive loss characteristics). The CLC014 simplifies the task of high-speed data recovery with a one-chip solution and a minimal number of external components. The equalizer automatically adapts to equalize any cable length from zero meters to lengths that attenuate the signal by 40dB at 200MHz. This corresponds to 300 meters of Belden 8281 or 120 meters of Category 5 UTP (unshielded twisted pair). The equalizer operates over a wide range of data rates from less than 50Mbps to rates in excess of 650Mbps. [21]. Application of this equalizer includes SMPTE 259M serial digital interfaces, serial digital video routing and distribution, serial digital data equalization and reception, data recovery equalization ATM, CAD networks, medical, set top terminals, industrial video networks.

Maxim Integrated Products builds upon its industry-leading adaptive equalizer portfolio with the introduction of the MAX3802 quad adaptive equalizer [22]. Maxim adaptive equalization algorithm, already proven in the MAX3800 and MAX3801 equalizers, enables low-cost copper system interconnections up to 3.2Gbps and effectively extends the usable length of coaxial and twin-axial copper cable in point-to-point communications applications. The MAX3802 contains four independent 3.3V adaptive cable equalizers and four independent cable drivers on a single chip. It automatically adjusts to attenuation caused by skin-effect levels of up to 30dB at 1.6GHz, making inexpensive 30m cables viable interconnect solutions. Applications include high-Speed Links in communications and data systems, Back-plane and Twin-Axial Cable Interconnects, Category 5 UTP-Based systems, digital video systems.

A cable equalizer product of the Gennum corporation is GS9064 [23]. This is a second generation high-speed bipolar integrated circuit designed to equalize and restore 270Mbps signals received over 75Ω coax cable. The GS9064 is designed to support both SMPTE 259-M-C and DVB-ASI 270Mbps. Their another product GS1524, equalize and restore signals to the coax cable at data rates from 143Mbps up to 1.485Gbps. The GS1524 is designed to support SMPTE 292M, SMPTE 344M, and SMPTE 259M.

Sony Corporation's [24] CXB1454R cable equalizer, which is a part of the chip set for serial transmission of 24 bit full-color VGA, SVGA and XGA digital image data, can adaptively equalize up to 10 meter of cable.

TDK Semiconductor Corporation [25] produces the TSC 78Q2250 which is a high-speed line transceiver integrated circuit, intended for use in ATM applications at 155.52Mbps. It is used at the interface to 100 meters or less Category 5 UTP cabling and is connected to the line via isolation transformers. The receiver provides adaptive equalization for accurate clock and data recovery. A similar product is the TSC 78Q2120 transceiver for 100Base-TX Ethernet which can equalize MLT-3 data over 110 meters CAT5 cable.

VITA

Mohammad Abdul Ahad was born on the 1st of November of 1973 in Chittagong, Bangladesh. He had his Primary education from Saint Mary's School and high schooling from the Collegiate School, Chittagong. He stood 13th in the combined merit list of 20 in the Secondary School Certificate Examination under the Comilla Board and obtained 17th position in the combined merit list of 20 in the Higher Secondary School Certificate Examination from Chittagong College under the same board. Cherished to become an Electrical Engineer, he joined the renowned engineering university of Bangladesh, The Bangladesh University of Engineering and Technology (BUET), Dhaka in 1993 from where he graduated with a Bachelor of Science in Electrical and Electronic Engineering in 1998. He obtained position in the Dean's List in few undergraduate semesters while studying in BUET. In fall, 1999 he joined in the University of Tennessee, Knoxville in the Master's program of Electrical and Computer Engineering. Since then, he has been working as a Teaching Assistant in that department and at the same time working with Dr. Syed K. Islam towards his Master's thesis. In summer, 2001 he had internship experience with Transwitch Corporation, Raleigh, NC where he developed the pole-zero model for the cable equalizer. He is now planning to go for Ph.D.