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Modeling, Measurement and Mitigation of Fast Switching Issues in Voltage Source Inverters

Wen Zhang
University of Tennessee, Knoxville, wzhang53@vols.utk.edu

To the Graduate Council:

I am submitting herewith a dissertation written by Wen Zhang entitled "Modeling, Measurement and Mitigation of Fast Switching Issues in Voltage Source Inverters." I have examined the final electronic copy of this dissertation for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Doctor of Philosophy, with a major in Electrical Engineering.

Fred Wang, Major Professor

We have read this dissertation and recommend its acceptance:

Leon M. Tolbert, Daniel J. Costinett, Zheyu Zhang

Accepted for the Council:

Dixie L. Thompson

Vice Provost and Dean of the Graduate School

(Original signatures are on file with official student records.)

Modeling, Measurement and Mitigation of Fast Switching Issues in Voltage Source Inverters

A Dissertation Presented for the

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To my wife

Acknowledgments

Doctorate degree is a journey both arduous and pleasant. My deepest gratitude goes to my advisor, Dr. Fred Wang, without whom the journey would be impossible. Besides the technical knowledge, his inspiration leads me to a broader perspective, even beyond the power electronics field. I must also thank for the level of freedom he gave me throughout the years, to explore different disciplines and dream about what is possible.

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Finally, I must thank the support and encouragement from my wife, Ying Liu, which fueled me towards graduation. Without her reminders, I would have forgotten there is an end to this journey.

Abstract

Wide-bandgap devices are enjoying wider adoption across the power electronics industry for their superior properties and the resulting opportunities for higher efficiency and power density. However, various issues arise due to the faster switching speed, including switching transient voltage overshoot, unstable oscillation, gate driving and evaluation difficulty, measurement and monitoring challenge, and potential load insulation degradation. This dissertation first sets out to model and understand the switching transient voltage overshoots. Unique oscillation patterns and features of the turn-on and turn-off overvoltage are discovered and analyzed, which provides new insights into the switching transient. During the experimental characterization, a new unstable oscillation pattern is found during the trench MOSFET's turn-off transient. The MOSFET channel may be falsely turned back on, resulting in severe oscillation and possible loss of control. Time-domain and large-signal analytical models are established, which reveals the negative impact of common-source inductances and unconventional capacitance curve of trench MOSFET. Besides the devices themselves, another determining part in their switching transient behavior is the gate driver. A programmable gate driver platform is proposed to readily adapt to different power semiconductors and driving schemes, which can greatly facilitate the evaluation and comparison of different

devices and driving schemes. The faster switching speed of wide-bandgap devices also requires more demanding measurement and monitoring solutions. A novel combinational Rogowski coil concept is proposed, which leverages the self-integrating feature to further increase the bandwidth. Prototypes achieved more than 300 MHz bandwidth, while keeping the cross-sectional area less than 2.5 mm^2. Finally, the very high voltage slew rate of wide-bandgap devices may negatively impact the motor load insulation. Attempting to fully utilize the higher switching frequency capability, sinewave and dv/dt filters are compared. It is shown that sinewave filters can achieve higher efficiency and power density than dv/dt filters, especially for high frequency applications.

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Chapter 1

Introduction

1.1 Semiconductor Material and Devices

Wide-bandgap semiconductor materials including silicon carbide (SiC) and gallium nitride (GaN) demonstrate superior physical properties compared to the traditional silicon (Si) material, as shown in Fig. 1.1 [1]. The higher breakdown field translates into thinner junction size for the same blocking voltage. The higher thermal conductivity leads to better thermal dissipation and opportunities for higher operating temperature. Finally, the dielectric constant in SiC and GaN is smaller, resulting in smaller parasitic capacitances, further translating into faster switching speed and lower switching loss. As a result, wide-bandgap power semiconductors are receiving wider adoption across the power electronics industry for these unprecedented capabilities and opportunities.

Many different power semiconductor designs have been reported and commercially available. A few samples are shown in Fig. 1.2. SiC Schottky diodes are among the first devices available and have demonstrated better static and dynamic characteristics than Si PiN diodes [2].

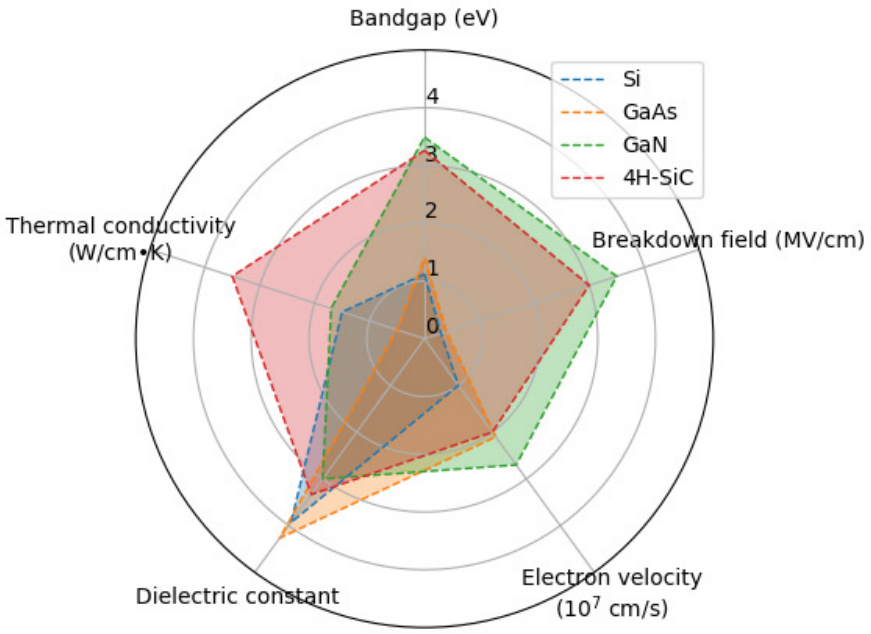


Figure 1.1: Wide-bandgap semiconductor material properties comparison with Si.

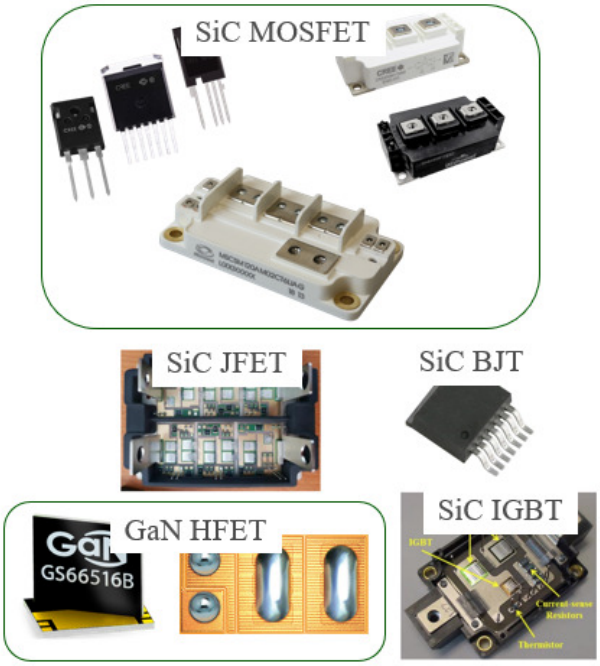


Figure 1.2: Wide-bandgap power semiconductor device examples.

Active devices including junction-field-effect-transistors (JFET) or cascode devices have also been demonstrated with either SiC or GaN [3]–[6]. Because of the difference in material properties, it is also feasible to fabricate high-voltage high-current bipolar-junction-transistor (BJT) with SiC [7]–[10]. However, because of the easy voltage-driven nature of metal-oxide-semiconductor field-effect-transistors (MOSFET), they are still the most popular choice. High-voltage and high-current power SiC MOSFET modules or discrete device have been reported [11]–[13]. With GaN material, enhancement-mode high-electron-mobility-transistors (HEMT) or hetero-junction-field-effect-transistors (HFET) have also been evaluated and applied in power electronics converters [14]–[17]. To achieve even higher blocking voltage, SiC insulated-gate-bipolar-transistors (IGBT) have been demonstrated for medium voltage applications [18], [19].

1.2 Background and Motivation

The superior properties of wide-bandgap semiconductors enable improvements across a wide range of applications, including solar inverters, uninterrupted power supplies, railway traction inverters, electric vehicle battery chargers and traction drives, induction heating and medium- to high-voltage grid applications [20]. The general two-level three-phase voltage source converter, as shown in Fig. 1.3, can represent the circuit topology in many of the previous applications. The DC voltage source V_d is connected with three parallel phase-leg branches, which is then connected to the three-phase load Z_{ABC}. The three-phase load Z_{ABC} may come from the utility grid interface or electric machine, with or without additional filters. The basic principle of power electronics converter mandates that the load impedance must

be dominantly inductive to avoid excessive current in the switches S_1–S_6.

As the switching speed increases, a plethora of issues arise and numerous literature have reported on them. The high switching speed characteristic means the devices may be susceptible to excessive amount of overvoltage during the switching transient [21]–[23]. Even though the switching transient of MOSFETs has been extensively studied [24]–[30], it is necessary to reexamine some of the assumptions as they may no longer hold true for the much faster SiC MOSFETs. In [24], [25], the overvoltage during the turn-off transient is calculated by considering the MOSFET channel as a linearly decreasing current source. While very intuitive, the switching time information is required, and the MOSFET channel current behavior is more complex than the assumption. In other literature [26]–[30], the switching transient is solved in a stage-by-stage fashion, examining the equivalent circuit of the MOSFET and diode in each stage and then solving the circuit explicitly using initial conditions from the previous stage. The stage transitions are assumed to happen in a fixed sequence. Because the switching transient circuit is a high-order nonlinear system, assumptions are required to obtain a closed-form solution. References [26], [28] assumes a plateau region for the gate-source voltage. Reference [27] makes the assumption that the drain current and its derivative are zero in some of the transition stages. When the MOSFET is in saturation region, [29] assumes the current flowing though its parasitic capacitances is negligible. Reference [30] assumes the drain-source voltage and drain current change linearly during the switching transient. Because the aforementioned assumptions may not always hold true for SiC MOSFETs, attempts have been made with numerical methods to solve the switching transient circuit. The semiconductor models are usually created by curve fitting against behavioral equations [30]–[34].

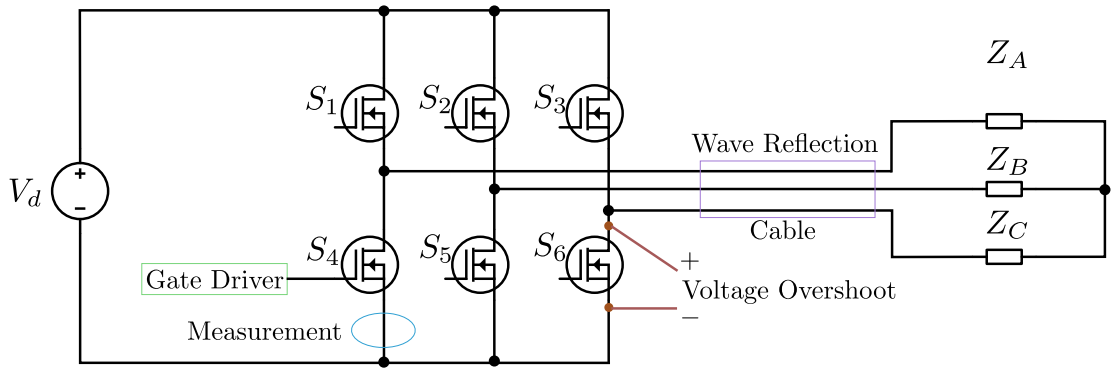


Figure 1.3: Simplified schematic of two-level three-phase voltage source converter and fast switching issues discussed.

The faster switching speed presents challenges in undesirable ringing and oscillation during the switching transient. Besides the power loop oscillation, excessive amount of gate loop inductance may also result in destructive gate-source overvoltage [17]. In addition to the normal oscillations, abnormal oscillation phenomena have also been reported. An example is the crosstalk phenomenon which happens when the synchronous device is falsely turned on during the active device's turn-on transient [35], [36]. The root cause is found to be the synchronous device's gate-drain capacitance C_{gd} charging its gate-source votlage V_{gs} above the threshold due to high voltage slew rate in the power loop. Another type of abnormal oscillation phenomenon is reported in [37], [38] where sustained oscillations with SiC JFET and SiC MOSFET are observed in the turn-off transient. The phenomena were partly due to pronounced amount of parasitic elements. Reference [39] reported a simulation phenomenon where a SiC MOSFET channel is temporarily turned on during the turn-off transient when the source inductance is very large. Unstable oscillation is also reported in [40] with parallel MOSFETs in solid-state circuit breaker applications. Gallium nitride (GaN) HFETs abnormal oscillation has also been investigated. In [5], continuous ringing is observed in short circuit condition, and the cause is due to insufficient gate resistance damping. In [41], instability due to the GaN HFET's unique reverse conduction behavior and common source inductance is presented and analyzed.

With the advent of wide-bandgap semiconductors, a wide range of devices have been reported and commercially available, including SiC junction-field-effect-transistor (JFET) [42] and GaN heterojunction-field-effect-transistor (HFET) [43]. Current driven devices such as SiC bipolar-junction-transistor (BJT) have also been actively investigated [8], [9], [44]. These drastically different devices have very diverse gate/base driving requirements, in terms

of on-state or off-state voltage and continuous or transient gate current magnitude. Numerous works have also been conducted on advanced gate driving strategies. As an extension to the simplest two-level voltage source driving, three or four level driving have been demonstrated and are capable of achieving better transient performance [10], [45]. Instead of simple turn-on or turn-off gate resistors, more complex impedance network with series or parallel RLC networks have also been investigated [10], [46], [47]. Current source or resonant gate drivers are another group of driving schemes which enable the direct control of gate current during switching transients and the recovery of gating energy for high frequency applications [48]–[51]. Unlike the voltage source drivers, the device gate is directly charged or discharged by an inductor current, and the driving voltage is clamped with active switches or diodes. The current source driving concept has also been utilized for SiC BJTs to effectively reduce the base driving loss [8].

In addition to the device itself and its gate driver, the measurement and monitoring technique is also being challenged the faster switching speed of wide-bandgap devices. Several high-bandwidth current measurement techniques are available [52]. Resistive current shunts can achieve very high bandwidth up to several GHz but are limited to non-continuous pulse operation due to heat dissipation [53], [54]. Current transformers can achieve up to 250 MHz measurement bandwidth but the cross-sectional area is quite large due to the magnetic material saturation limitation [55]. The resulting extra power loop area when routing the power loop conductor around the current transformer is therefore also large. Rogowski coils are another widely used type of current sensor based on the Faraday's induction law [56]. The helix coil directly measures the derivative of the current, which is then reconstructed by a passive or active integrating circuit [57]. The state-of-the-art commercial Rogowski coil has a

small circular cross-sectional area with a diameter of 3.5 mm but the measurement bandwidth is limited to 50 MHz [58]. A Rogowski coil with up to 225 MHz bandwidth is demonstrated in [59], but numerical integration with oscilloscope is required and the sensitivity is quite low due to the low number of turns. Reference [60] proposed an integrated Rogowski coil for a GaN power stage, but the measurement bandwidth is not explicitly given.

Regarding the load, the faster switching speed and resulting higher voltage slew rate may damage the motor load insulation [61]. Numerous solutions to these issues have been developed and evaluated over the years. The simplest solution is putting a line termination network consisting of a simple RC filter at the motor terminal to match the cable impedance [62]. While the wave reflection problem is alleviated, the voltage slew rate at the motor terminal is still pretty high and the termination capacitor may result in excessive power loss. An active terminator using diodes to clamp the motor terminal voltage is proposed in [63]. Likewise, although the wave reflection issue is gone, the sharp voltage edge is still present at the motor terminal. A more popular solution, the dv/dt filter has been widely investigated [64]–[71]. Reference [64] integrates the filter inductor into the converter bus bar and connection cable. Reference [65] put the branch of filter capacitor and resistor in parallel with the filter inductor to reduce the power loss. Reference [66] introduces diode clamping circuit to further limit the voltage overshoot. In addition to diode clamping, [67] put a RC circuit in the diode clamping circuit to help with the EMI. Reference [68] proposes to connect the middle point of the filter capacitors back to the middle point of the DC link to improve EMI. Reference [69] integrates the common mode inductor with the dv/dt filter. Reference [71] combines both the common mode inductor and connects the neutral point back to the middle point of DC link. Reference [70] investigates the effectiveness of using two dv/dt

filters in series. On the other hand, another filter solution, the sinewave filter has long been considered more expensive, costly and lossy [72]. However, with the high switching frequency capabilities from wide-bandgap devices, they are now being evaluated again. Reference [73] compares the system efficiency of GaN HFET and Si MOSFET motor drive. Reference [74] demonstrates a sinewave filter in GaN HFET motor drive while damping the sinewave filter with both analog and digital filters.

Given the relatively immaturity of wide-bandgap semiconductors, there are several other fast switching related issues. The capability to switch faster comes from the smaller semiconductor size. However, the smaller die size translates into worse temperature hike during the short-circuit event and therefore lower tolerance against shoot-through conditions. The traditional "desaturation" protection method has been investigated and improved to accommodate the faster switching speed [83], [84]. Using the parasitic inductance in the power loop, the switching transient current may be reconstructed and protection action may be triggered [85]. The gate charge characteristic has also been used for protection purpose [86]. Direct current measurement has also been utilized for protection although it is only limited to pulse operation [79].

In order to fully utilize the semiconductor devices, the parasitic elements must be minimized to enable the fastest possible switching speed. A number of packaging techniques have been proposed and evaluated to the wide-bandgap semiconductors [87]–[90]. Sub-nH packaging has been demonstrated with flexible printed circuit board approach [91]. Other issues may also arise or become worse with the wide-bandgap devices, including electromagnetic interference and thermal management.

In summary, to limited the scope of discussion, the issues that will be focused in this

dissertation are listed below.

1. The high switching speed characteristic means the devices may be susceptible to excessive amount of overvoltage during the switching transient [21]–[23]. With the faster switching transient of SiC MOSFETs, the switching transient voltage overshoot models need reexamination in order to better utilize the devices.

2. The parasitic elements may also bring about abnormal oscillatory behaviors to the switching transient [37], [38], [75]. The higher switching speed means semiconductor devices are even more sensitive to the parasitic elements.

3. With the advent of wide-bandgap devices, numerous conventional and unconventional power semiconductor devices have been available. The gate driver is a critical component regulating the devices' performance. In order to quickly evaluate different semiconductor devices and tune the switching performance, there is a need for a "universal" and programmable gate driver [76]–[78].

4. The higher switching speed and oscillation frequency means more stringent current sensor requirement, in terms of bandwidth and electrical footprint[53], [79], [80]. Existing sensor technologies can not meet the requirement to continuously measure and monitor the switching transient current.

5. The converter output voltage slew rate is greatly increased because of the faster switching speed. However, the high slew rate may present insulation issues for motor loads, especially those with long cables [61], [81], [82]. The dv/dt filter is typically preferred over the sinewave filter with Si-based converters. Given SiC MOSFET's

higher switching frequency capability, there may be opportunities for sinewave filters to achieve better efficiency and power density.

1.3 Chapter Layout

Each chapter is devoted to one of the five listed issues. A literature review is carried out first and the research background is introduced. The theoretical analysis or design methodology is then laid out before presenting the experimental demonstration and verification. Finally, a short summary section and some potential future work are appended at the end of each chapter.

Chapter 2 focuses on the normal switching transient overvoltage, in both the turn-off and turn-on transients. A hypothetical ideal switching transient is first analyzed, and interesting observations on the two different overvoltage mechanisms are made. Analysis on the non-ideal switching transient is then presented and similarities between the ideal and non-ideal cases are noticed, which are then experimentally verified. The turn-off transient is highly sensitive to oscillation stage transitions. The turn-off overvoltage may exhibit non-monotonic behavior, where the overvoltage may be larger with smaller power loop inductance or slower switching speed. The turn-on transient, on the other hand, is largely independent of the load current. To predict the overvoltage and guide device selection and converter layout, numeric modeling with neural-net behavioral models is carried out and it is shown the approach can accurately model the switching transient overvoltage.

Instead of normal oscillation, **Chapter 3** focuses on the abnormal oscillation during switching transient. A novel abnormal oscillation pattern, "self-turn-on" is found when

characterizing a trench MOSFET. The MOSFET is falsely turned on during the turn-off transient. SPICE and large-signal models are established to understand the phenomena. The root cause is found to be the rapid changing nonlinear capacitance curve and the common source inductance. Especially with large-signal models, it is found that the MOSFET's nonlinear voltage-capacitance curve contributes directly to the instability. Although the phenomena are observed with Si CoolMOS, the understanding can also be applied towards SiC devices and help future semiconductor device development.

Gate drivers play an critical role governing the devices' switching transient behavior. In practice, however, there are various types of power semiconductors with very different driving requirements. There are a plethora of gate driving schemes, including voltage source and current source driving. **Chapter 4** proposes a programmable and universal gate driving platform, which can drive most of the common power semiconductors and adapt to different driving schemes. The platform significantly lowers the effort to characterize different power semiconductors and evaluate different driving schemes.

Another technical challenge related to the fast switching speed is the switching transient current measurement. Existing current sensors suffer from either insufficient measurement bandwidth, large insertion inductance, or noncontinuous operation. A novel combinational Rogowski coil current sensor is proposed in **Chapter 5**. Compared to existing Rogowski coil sensors, it utilizes both the differentiating and self-integrating feature of a shielded coil. Experimental prototypes demonstrate up to 300 MHz measurement bandwidth, around 5 times higher than existing state-of-the-art. The design methodology and practical considerations are discussed in detail. The concept here greatly enhances the capabilities of Rogowski coils, and can serve as a great tool for online semiconductor switching transient monitoring.

Because of the fast switching speed, voltage source inverters suffer from very high output voltage slew rate, which poses a severe threat to the motor winding insulation, especially those connected with a long cable. **Chapter 6** compares two basic filter topologies, sinewave and dv/dt filters, to tackle the high voltage slew rate. Traditionally, dv/dt filters are favored against sinewave filters because of the smaller physical size and lower power loss. However, because of the much higher switching frequency capability and lower switching loss of SiC MOSFETs, it is shown in that it is possible to achieve on-par or even better system-level performance with the sinewave filters in SiC-based drives. The comparison and filter optimization strategy provide an invaluable guideline for motor drive filter selections.

The last **Chapter 7** summarizes the previous chapters and concludes the whole dissertation. Relevant possible future work are also pointed out.

Chapter 2

Switching Transient Overvoltage Modeling and Characterization

2.1 Introduction

Wide-bandgap devices offer transforming opportunities for power electronics converters towards higher power density and efficiency. The switching speed is much faster, but the overvoltage stress during the switching transient is also likely more severe than the Si counterparts. The switching transient voltage overshoot is a crucial factor in selecting device voltage rating. Too much voltage rating margin translates into extra cost, while too little voltage margin risks converter safety and may mandate slowing down the switching speed. Thanks to the higher bandgap energy, SiC devices are more robust against single-event-burnout [92], [93], making it more tempting to fully utilize its voltage rating. Therefore, the understanding and modeling of the switching transient overvoltage is essential to better utilize the SiC devices and optimize power converters' performance.

Even though the switching transient of MOSFETs has been extensively studied [24]–[30], it is necessary to reexamine some of the assumptions as they may no longer hold true for the much faster SiC MOSFETs. In [24], [25], the overvoltage during the turn-off transient is calculated by considering the MOSFET channel as a linearly decreasing current source. While very intuitive, the switching time information is required, and the MOSFET channel current behavior is more complex than the assumption. In other literature [26]–[30], the switching transient is solved in a stage-by-stage fashion, examining the equivalent circuit of the MOSFET and diode in each stage and then solving the circuit explicitly using initial conditions from the previous stage. The stage transitions are assumed to happen in a fixed sequence. Because the switching transient circuit is a high-order nonlinear system, assumptions are required to obtain a closed-form solution. References [26], [28] assumes a plateau region for the gate-source voltage. Reference [27] makes the assumption that the drain current and its derivative are zero in some of the transition stages. When the MOSFET is in saturation region, [29] assumes the current flowing though its parasitic capacitances is negligible. Reference [30] assumes the drain-source voltage and drain current change linearly during the switching transient. Because the aforementioned assumptions may not always hold true for SiC MOSFETs, attempts have been made with numerical methods to solve the switching transient circuit. The semiconductor models are usually created by curve fitting against behavioral equations [30]–[34].

The simplified equivalent circuit of the switching transient is shown in Fig. 2.1. Note that in addition to the overvoltage across the MOSFET M in the turn-off transient, there is another overvoltage mechanism, which is across the inactive switch when the active switch is turned on. This is named "turn-on overvoltage" in this paper. In Fig. 2.1, the turn-on

overvoltage occurs across the diode D when the lower active MOSFET M is turned on and the diode D is passively turned off. Similar to the turn-off overvoltage, it has been studied in a similar stage-by-stage fashion [94], [95].

The two overvoltage mechanisms are examined here to understand their different characteristics. Ideal analysis is presented first to highlight the possible complex oscillation pattern transitions during the switching transient. The ideal analysis also provides a baseline for studying the non-ideal practical switching transient. Turn-off transients are very sensitive to load current while turn-on transients are not. The turn-off overvoltage also may exhibit a nonlinear relationship with the switching speed or power loop inductance. Experimental characterization is then performed to further understand and verify the analytical result. Finally, numerical modeling with SPICE is demonstrated which is capable of accurately predicting the switching transient overvoltage. The SPICE model also further confirms the unconventional stage transitions for fast switching transients.

2.2 Hypothetical Ideal Switching Transient

Before analyzing the practical switching transients with more accurate MOSFET and diode models, a hypothetical case is discussed where the MOSFET channel is considered as an ideal switch. This means the gate driver can instantly toggle the MOSFET channel to completely on or off, as shown in Fig. 2.2. This is of course impossible because in practice all gate driver buffers have limited driving capabilities and the gate parasitic elements limit how fast the gate-source voltage v_{gs} can change. The diode is also assumed ideal with zero on-state voltage drop. Nevertheless, the simplified hypothetical ideal analysis will offer an

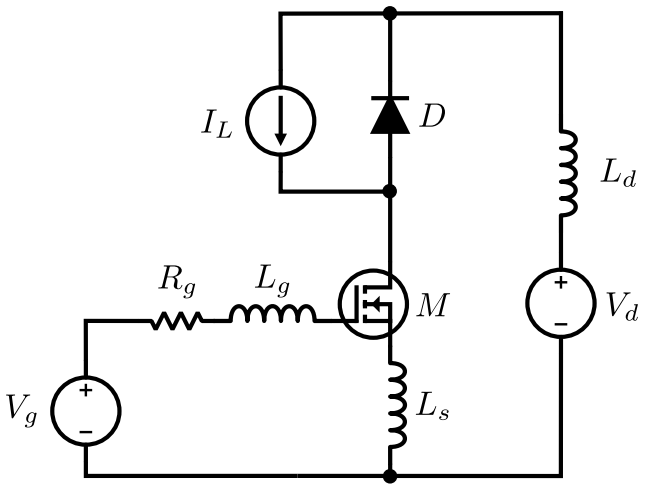


Figure 2.1: MOSFET and diode phase-leg switching transient simplified circuit schematic.

interesting perspective and a useful foundation for the later non-ideal switching transient analysis.

2.2.1 Ideal turn-off transient

The junction capacitances C_j for the diode and MOSFET are assumed linear and the same. In the turn-off transient, the MOSFET channel current is immediately shut off. The equivalent circuit after the MOSFET channel shuts off is shown in Fig. 2.3. The DC link voltage is denoted as V_d and the load current is denoted as I_L. At the beginning of the turn-off transient, the diode is still in blocking state and $v_H(t=0)=0$ and $v_L(t=0)=V_d$. The current flowing through the power loop inductance is still $i_d(t=0)=I_L$. The circuit is essentially an oscillation between the power loop inductance L_d and the two parasitic capacitances C_j, with two excitation sources I_L and V_d. The upper diode voltage v_H and lower MOSFET voltage v_L can be solved by superposition,

$$v_L(t) = \frac{I_L}{2}\sqrt{\frac{L_d}{2C_j}} \cdot \sin\sqrt{\frac{2}{L_d C_j}}t + \frac{I_L}{2C_j}t, \tag{2.1}$$

$$v_H(t) = \frac{I_L}{2}\sqrt{\frac{L_d}{2C_j}} \cdot \sin\sqrt{\frac{2}{L_d C_j}}t - \frac{I_L}{2C_j}t + V_d. \tag{2.2}$$

The current flowing through the parasitic inductance L_d is given by

$$i_d = \frac{I_L}{2} + \frac{I_L}{2} \cdot \cos\sqrt{\frac{2}{L_d C_j}}t. \tag{2.3}$$

Again assuming the diode is ideal, the diode starts conducting after v_H drops to zero.

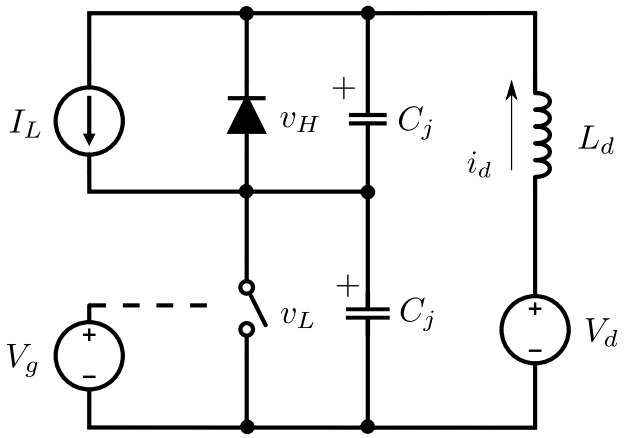


Figure 2.2: Hypothetical ideal switching transient circuit model where the MOSFET channel can be instantaneously turned on or off.

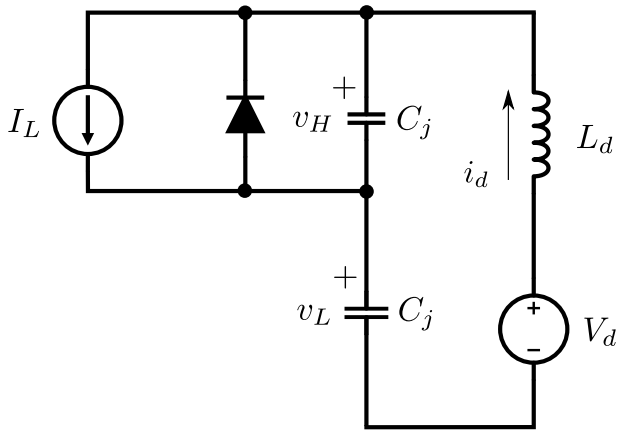


Figure 2.3: Hypothetical ideal turn-off switching transient circuit model where the MOSFET channel is turned off instantly.

Denoting the time when the diode starts conducting as t_1,

$$v_H(t_1) = \frac{I_L}{2}\sqrt{\frac{L_d}{2C_j}} \cdot \sin\sqrt{\frac{2}{L_d C_j}}t_1 - \frac{I_L}{2C_j}t_1 + V_d = 0. \tag{2.4}$$

Equation (2.4) is a transcendental equation, so there is no closed-form solution. However, if further denote the phase angle associated with the oscillation as $\sqrt{\frac{2}{L_d C_j}}t_1 = \alpha$, then

$$v_L(t_1) = V_d + I_L\sqrt{\frac{L_d}{2C_j}}\sin\alpha, \tag{2.5}$$

$$i_d(t_1) = \frac{I_L}{2}(1+\cos\alpha) \geq 0. \tag{2.6}$$

After the diode starts conducting, the diode shorts the load current I_L and now the circuit oscillates between only the lower capacitance C_j and the power loop inductance L_d. The initial conditions for this simple oscillation are given in (2.5) and (2.6). The oscillation dies down gradually due to the resistance in the power loop. In the ideal case here where the resistance is neglected, it is trivial to find the lower voltage v_L after t_1 to be,

$$v_L(t > t_1) = V_d + I_L\sqrt{\frac{L_d}{2C_j}}\sin\alpha\cos\frac{t}{\sqrt{L_d C_j}} + \frac{I_L}{2}\sqrt{\frac{L_d}{C_j}}(1+\cos\alpha)\sin\frac{t}{\sqrt{L_d C_j}}. \tag{2.7}$$

The turn-off overvoltage in the ideal turn-off transient is found by taking the maximum of the expression above,

$$v_{L,max} = V_d + \frac{I_L}{2}\sqrt{\frac{L_d}{C_j}} \cdot \sqrt{3 + 2\cos\alpha - \cos^2\alpha} \in \left[V_d, V_d + I_L\sqrt{\frac{L_d}{C_j}}\right]. \tag{2.8}$$

The upper boundary of the turn-off voltage stress is $V_d + I_L\sqrt{\frac{L_d}{C_j}}$. This means the energy

stored in the parasitic inductor L_d at the beginning of the turn-off transient is completely transferred into the lower parasitic capacitance. On the other hand, the lower boundary is only V_d, meaning the maximum voltage stress on the lower device is just the DC link voltage. This means the energy stored in the parasitic inductance L_d at the beginning of the turn-off transient is completely dissipated in the oscillation before the diode starts conduction.

From (2.8), the turn-off overvoltage depends greatly on the phase angle α. In fact, for $\alpha = (2k+1)\pi, k \in \mathbb{N}$, the turn-off voltage stress is only the DC link voltage V_d. This means the overvoltage may be minimal even for heavy load conditions. It is more evident in a numerical example. Suppose the junction capacitance $C_j = 100$ pF, and the DC link voltage $V_d = 600$ V, the turn-off overvoltage under different load current I_L is shown in Fig. 2.4. The power loop inductance L_d is either 20 nH or 40 nH. The turn-off overvoltage takes its minimum value of V_d in a somewhat periodical fashion. The overvoltage does not increase linearly and monotonically with the load current I_L. Because of the diode conduction timing t_1 determined by (2.4), higher load current sometimes ends up with lower overvoltage. Comparing the different power loop inductances, higher L_d does not necessarily translate into higher overvoltage given the same load current. Due to the complex oscillation transitions, higher power loop inductance may end up with lower overvoltage.

2.2.2 Ideal turn-on transient

On the other hand, the ideal turn-on transient is a lot simpler. It is assumed that the MOSFET channel is turned on so fast that its parasitic capacitance is instantly discharged to zero and $v_L = 0$. The equivalent circuit is shown Fig. 2.5. At the moment the MOSFET

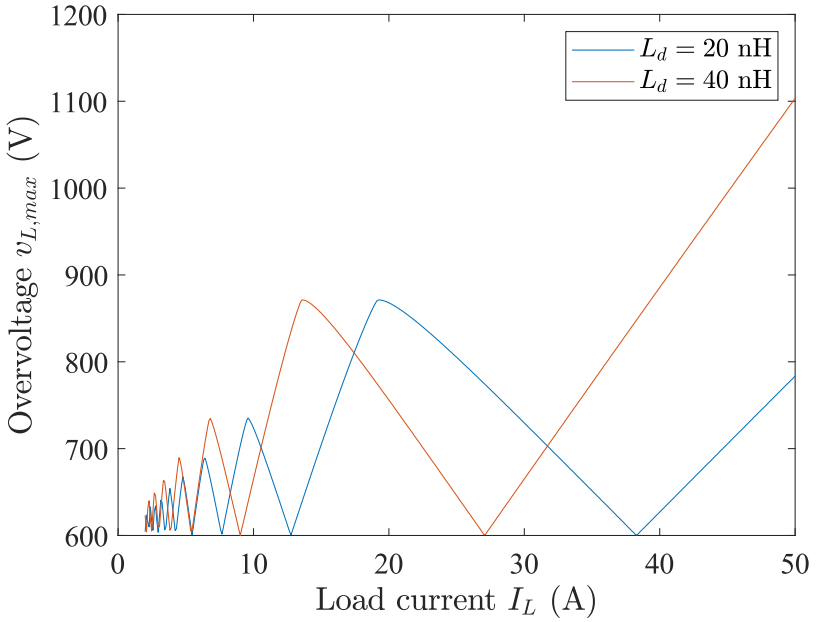


Figure 2.4: Example relationship between the ideal turn-off transient voltage stress $v_{L,max}$, parasitic inductance L_d and load current I_L.

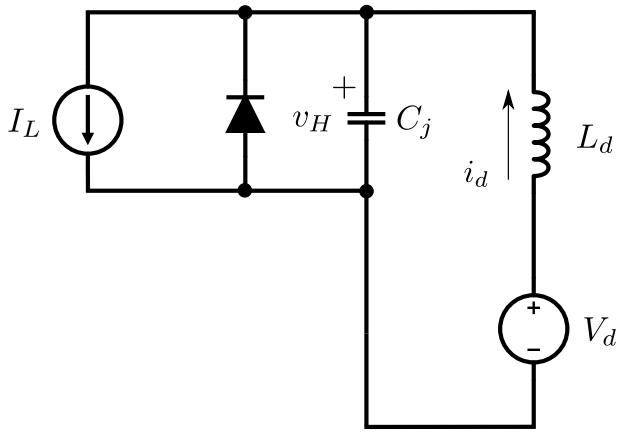


Figure 2.5: Hypothetical ideal turn-on switching transient equivalent circuit where the MOSFET channel is turned on instantly.

channel is turned on, the initial conditions are $i_d(t=0)=0$ and $v_H(t=0)=V_d$. The diode is still in conduction state. This is essentially a shoot-through state and the parasitic inductor L_d is linearly charged by the DC source voltage V_d,

$$i_d(t)=\frac{V_d}{L_d}t. \tag{2.9}$$

At $t=t_2$, the parasitic inductor current reaches the load current $i_d(t=t_2)=I_L$, and the diode starts blocking. The circuit oscillates between the high side parasitic capacitance C_j and the power loop inductance L_d. The high side voltage v_H can be easily found,

$$v_H(t>t_2)=V_d\left(1-\cos\frac{t}{\sqrt{L_dC_j}}\right). \tag{2.10}$$

It is trivial to see that the ideal turn-on overvoltage is independent of the load current I_L. The maximum voltage stress is always $2V_d$ and happens at $t=t_2+\pi\sqrt{L_dC_j}$.

In summary, if the gate driver has infinite driving capability and the MOSFET channel can be instantly turned on or off, the turn-on and turn-off overvoltage exhibit very different behaviors. When assuming the parasitic capacitances C_j are constant, in the ideal turn-on transient, the overvoltage is independent of the load current I_L and is always $2V_d$. In the turn-off transient, the overvoltage is dependent on the load current I_L but not in a simple linear way. It greatly depends on the phase angle α or the diode conduction time t_1. The voltage stress may be only the DC link voltage V_d. In the worst case, however, the turn-off overvoltage can reach $V_d+I_L\sqrt{\frac{L_d}{C_j}}$ and may be higher than $2V_d$.

2.3 Practical Non-ideal Switching Transient

The previous hypothetical ideal analysis assumes the MOSFET channel can be instantly turned on or off, which is unlikely in practice. On the other hand, the actual switching transient circuit is a high-order nonlinear system, and is difficult to obtain a closed-form solution. To focus on the possible stage transitions, the gate inductance L_g, power loop damping resistance R_d and common source inductance L_s are omitted. The simplified equivalent circuit is shown in Fig. 2.6. Also to facilitate the analysis, the MOSFET channel current in the saturation region is modeled as a simple linear voltage controlled current source,

$$i_M = g_{fs}\left(v_{gs} - V_{th}\right), \tag{2.11}$$

where g_{fs} is the transconductance and V_{th} is the threshold voltage of the MOSFET. Furthermore, the diode forward voltage drop and reverse recovery are omitted. Instead of obtaining a solution to the overvoltage, the objective here is to use more amenable equations to provide some qualitative understandings of the switching transients. The switching transient circuit stage transition, i.e. the diode conduction and MOSFET stage transition, will be focused and compared against the previous hypothetical ideal case.

2.3.1 Turn-off transient

The turn-off transient starts when the gate driver output voltage V_g drops from on-state driving voltage V_c to the off-state driving voltage V_e. Before the gate-source voltage v_{gs} drops below the Miller plateau voltage $V_m = V_{th} + \frac{I_L}{g_{fs}}$, the MOSFET remains in ohmic region and there is no change in the power loop current or voltage. The transition can be described as a

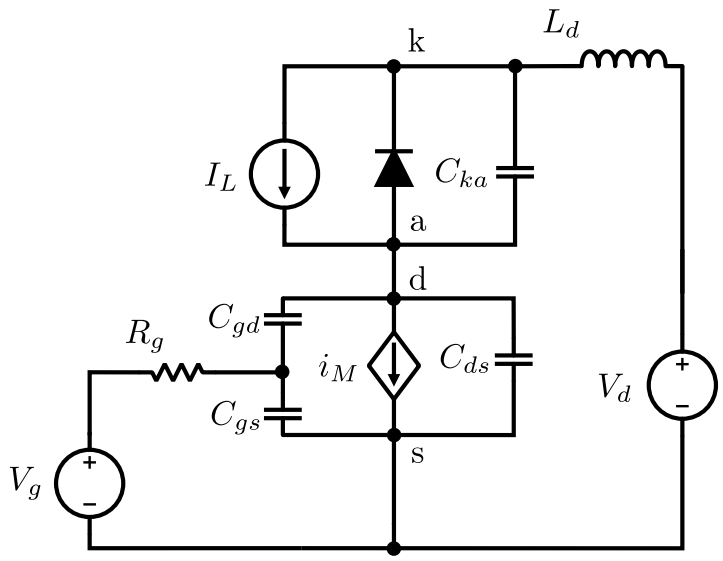


Figure 2.6: Simplified switching transient equivalent circuit model with MOSFET channel as a voltage controlled current source.

simple RC discharging process,

$$v_{gs} = V_e + (V_c - V_e) \exp\left[-\frac{t}{R_g(C_{gs} + C_{gd})}\right]. \tag{2.12}$$

Once the gate-source voltage v_{gs} drops down to the Miller plateau voltage V_m, the MOSFET goes into saturation region. The diode is still in blocking state. Compared to the ideal case, the MOSFET channel acts as a varying damping resistance. Nevertheless, the power loop oscillation still happens between the upper diode capacitance C_{ka}, the lower MOSFET capacitance C_{ds} and the power loop inductance L_d, as shown in Fig. 2.6. Note that the circuit is at least still a 4th-order system, whose closed-form solution is intractable.

Following this period, the next switching transient period depends on whether the diode voltage v_{ka} drops down to zero first and the diode starts conduction, or the gate-source voltage v_{gs} drops below the threshold voltage V_{th} first and the MOSFET goes into cut-off region. Assuming the diode starts conduction before the MOSFET goes into cut-off region, the equivalent circuit is shown in Fig. 2.7. The power loop is essentially a damped LC resonance between the MOSFET parasitic capacitance C_{ds} and the power loop inductance L_d, with the MOSFET channel being the damping resistance. Afterwards, the MOSFET then goes into cut-off region, and the system becomes a simple LC resonance between the MOSFET parasitic capacitance C_{ds} and the power loop inductance L_d.

However, if the MOSFET is turned off so fast and goes into cut-off region first before the diode starts conduction, the equivalent circuit is shown in Fig. 2.8. This in the power loop is essentially the same circuit as in the ideal case in Fig. 2.3. The circuit is an undamped oscillation between the diode capacitance C_{ka}, MOSFET parasitic capacitance C_{ds} and the

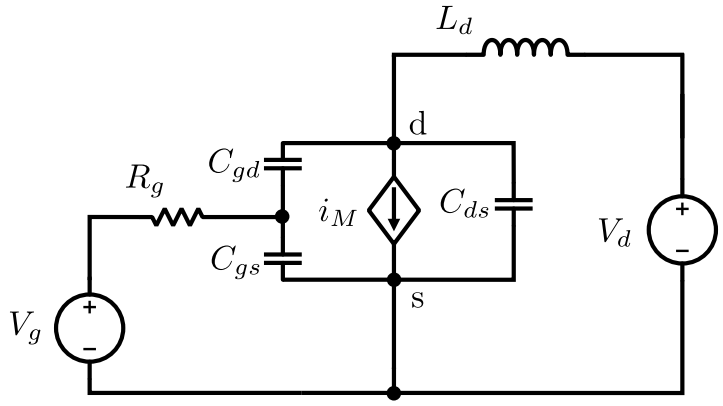


Figure 2.7: Equivalent switching transient circuit when the diode is conducting.

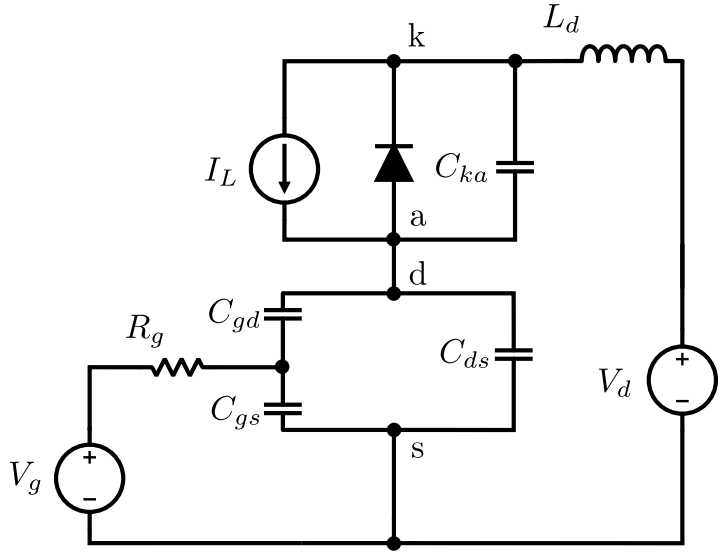


Figure 2.8: Equivalent switching transient circuit when the MOSFET goes into cut-off region.

power loop inductance L_d. Afterwards, similarly, the diode starts conducting and the circuit becomes a simple oscillation between the MOSFET capacitance C_{ds} and the power loop inductance L_d.

As a summary and comparison to the ideal turn-off transient, the oscillation patterns during the turn-off switching transient are the same. The oscillation first happens between both the diode and MOSFET capacitance and the power loop inductance, with the MOSFET channel being a varying damping resistor. If the diode starts conduction first, the circuit then becomes the oscillation between the MOSFET capacitance C_{ds} and the power loop inductance L_d, with the MOSFET channel still being a varying damping resistor. If the MOSFET goes into cut-off region first, the circuit then becomes almost exactly the same as the ideal turn-off.

In conclusion, it is evident that the practical turn-off transient is governed again by the two different oscillation patterns, although with the varying MOSFET channel resistance bringing more complexity. It is reasonable to infer that if the MOSFET switching speed is fast, we could observe similar properties as in the ideal case, including non-monotonic load current dependence and lower overvoltage with higher power loop inductance.

2.3.2 Turn-on transient

The turn-on transient starts when the gate voltage swings from the off-state voltage V_e to the on-state voltage V_c. Like the turn-off transient, at the beginning, the gate-source voltage

v_{gs} is charged above the threshold voltage V_{th},

$$v_{gs} = V_c + (V_e - V_c) \exp\left[-\frac{t}{R_g(C_{gs} + C_{gd})}\right]. \tag{2.13}$$

Once the gate-source voltage v_{gs} exceeds the threshold voltage V_{th}, the MOSFET goes into saturation region. Since the diode is still conducting, the equivalent circuit is the same as in Fig. 2.7 and can be described by

$$V_c = v_{gs} + R_g C_{gs}\left(\frac{dv_{gs}}{dt} + \frac{dv_{gd}}{dt}\right), \tag{2.14}$$

$$V_d = L_d \frac{di_d}{dt} + v_{ds}, \tag{2.15}$$

$$i_d = g_{fs}\left(v_{gs} - V_{th}\right) + C_{ds}\frac{dv_{ds}}{dt} - C_{gd}\frac{dv_{gd}}{dt}, \tag{2.16}$$

$$v_{gs} = v_{gd} + v_{ds}. \tag{2.17}$$

Again, it is difficult to directly solve the equations, but it is possible to make some speculations. It is trivial to that there is no load current I_L term in the equations. Naturally the solution to this stage is independent of the load current I_L. This is obvious in the circuit level since the load current is shorted by the diode at this stage. After this period, similar to the turn-off transient, there are two possibilities, depending on whether the MOSFET goes into ohmic region first or the diode starts blocking first.

Assuming the diode starts blocking first and the MOSFET remains in saturation region, the condition for the diode starts blocking is the power loop current i_d rises to the load

current I_L. Therefore, the circuit can be described by

$$V_c = v_{gs} + R_g C_{gs} \left(\frac{dv_{gs}}{dt} + \frac{dv_{gd}}{dt} \right), \tag{2.18}$$

$$V_d = L_d \frac{di_d}{dt} + v_{ka} + v_{ds}, \tag{2.19}$$

$$I_L = i_d - C_{ka} \frac{dv_{ka}}{dt}, \tag{2.20}$$

$$i_d = g_{fs} \left(v_{gs} - V_{th} \right) + C_{ds} \frac{dv_{ds}}{dt} - C_{gd} \frac{dv_{gd}}{dt}, \tag{2.21}$$

$$v_{gs} = v_{gd} + v_{ds}. \tag{2.22}$$

It is possible here to further simplify the equations and make some further speculations. Because the overvoltage across the diode is of interest here, the diode voltage v_{ka} is kept,

$$\begin{aligned} &\frac{L_d R_g C_{gs} C_{ds} C_{ka}}{g_{fs}} \cdot \frac{d^4 v_{ka}}{dt^4} + \\ L_d C_{ka} &\left(\frac{C_{ds}}{g_{fs}} + R_g C_{gd} \right) \cdot \frac{d^3 v_{ka}}{dt^3} + \\ &\frac{R_g C_{gs} (C_{ka} + C_{ds})}{g_{fs}} \cdot \frac{d^2 v_{ka}}{dt^2} + \\ &\left(R_g C_{gd} + \frac{C_{ka} + C_{ds}}{g_{fs}} \right) \cdot \frac{dv_{ka}}{dt} = V_c - V_{th} - \frac{I_L}{g_{fs}}. \end{aligned} \tag{2.23}$$

Note (2.23) is 4th-order and it is mathematically intractable to solve. Also note that the load current I_L is only present on the right-hand side of the equation. If the transconductance g_{fs} is large, the right-hand side value changes little with different load current I_L, meaning the solution to this period has little dependence on the load current I_L. Take the MOSFET C3M0065090J used in later experiments for example, its on-state driving voltage $V_c = 15.0$ V, threshold voltage $V_{th} = 2.1$ V and transconductance $g_{fs} = 13.6$ S. This means when the load

current I_L changes from no load $I_L = 0$ A to full load $I_L = 35$ A, the right-hand side value only changes from 12.9 V to 10.7 V. The relatively small change on the right hand side means the change in the specific solution to this differential equation is also relatively small, while the general solution remains the same.

On the other hand, if the MOSFET is so fast and goes into ohmic region before the diode starts blocking, the diode is still in conduction state and equivalently a shoot-through condition is created. Like the ideal case, the current in the power loop i_d rises linearly,

$$i_d = i_{d,0} + \frac{V_d}{L_d} t, \tag{2.24}$$

where $i_{d,0}$ is the initial power loop current condition determined by the previous stage.

Once the current in the power loop reaches the load current $i_d = I_L$, the equivalent circuit is again a simple LC resonance between the power loop inductance L_d and the diode parasitic capacitance C_{ka}. The initial conditions are $i_d = I_L$ and $v_{ka} = 0$, which are identical to the ideal turn-on case. Therefore, the solution of this stage is also the same as (2.10). The turn-on voltage stress in this case will also be $2V_d$ if the diode parasitic capacitance C_{ka} is constant. However, typically the diode parasitic capacitance C_{ka} is nonlinear and decrease with bias voltage. Therefore, the turn-on maximum voltage stress in this case will be higher than $2V_d$.

In conclusion, for the non-ideal turn-on transient, similarities with the ideal case can also be found. Especially if the gate driver is fast enough to drive the MOSFET into ohmic region before the diode starts blocking, the overvoltage oscillation pattern is the same as the ideal case. On the other hand, if the gate driver is not fast enough and diode starts

blocking first, the overvoltage is the result of a complex fourth-order system. In this case, if the transconductance g_{fs} is large enough, the turn-on overvoltage is also independent of the load current I_L.

2.4 Experimental Switching Transient Overvoltage

The experimental characterization setup to verify the previous analysis is shown in Fig. 2.9. The various components and measurement probes are listed in Table 2.1. The MOSFET and diode are soldered underneath the PCB. For turn-off overvoltage characterization, the MOSFET is soldered as the lower device; for turn-on overvoltage, the diode is soldered as the lower device. This is to enable measurement with the passive voltage probes. Note the gate resistance R_g below here means the external gate resistance, while the MOSFET C3M0065090J has an internal gate resistance $R_{g,int} = 4.7\ \Omega$. The experimental waveforms are captured at room temperature. Another thing to note is that the drain current I_d sensor may have an inconsistent measurement bandwidth and is compensated as in [96].

2.4.1 Turn-off overvoltage

The turn-off overvoltage sweep with different gate resistance R_g is shown in Fig. 2.10, and the sweep with different extra drain inductance L_d is shown in Fig. 2.11. The drain inductance variation is achieved by soldering a short wire perpendicularly into the PCB. The value of extra power loop inductance ΔL_d is determined by measuring this short wire inductance directly. In the gate resistance R_g sweep, the extra drain inductance ΔL_d is kept at minimal. In the drain inductance ΔL_d sweeps, the gate resistance is kept at $R_g = 0\ \Omega$.

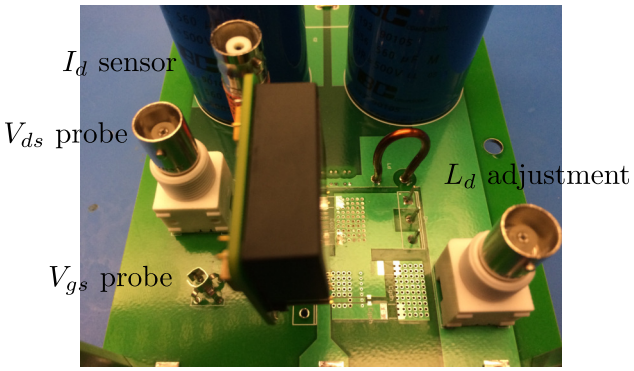
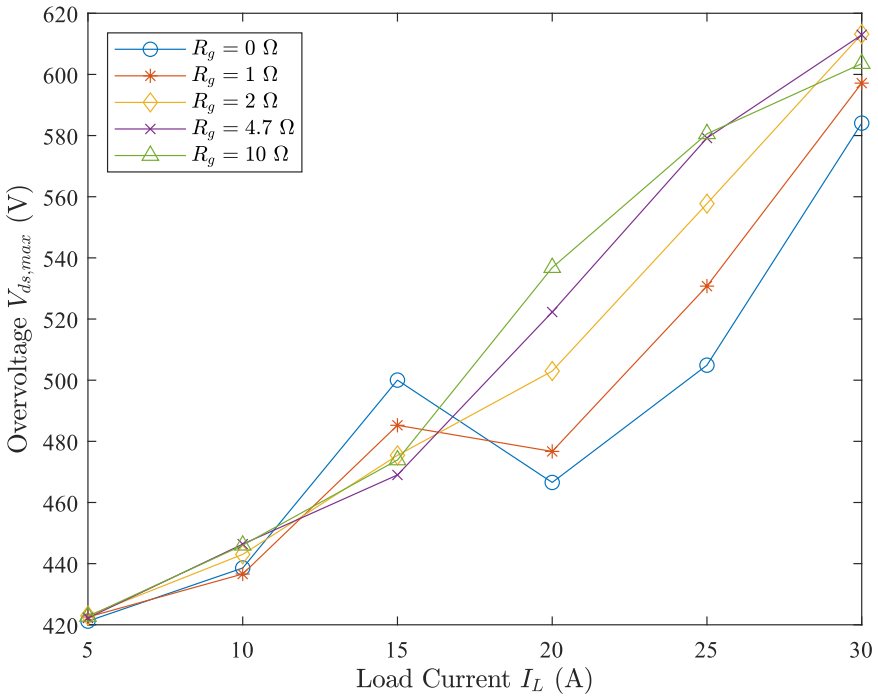


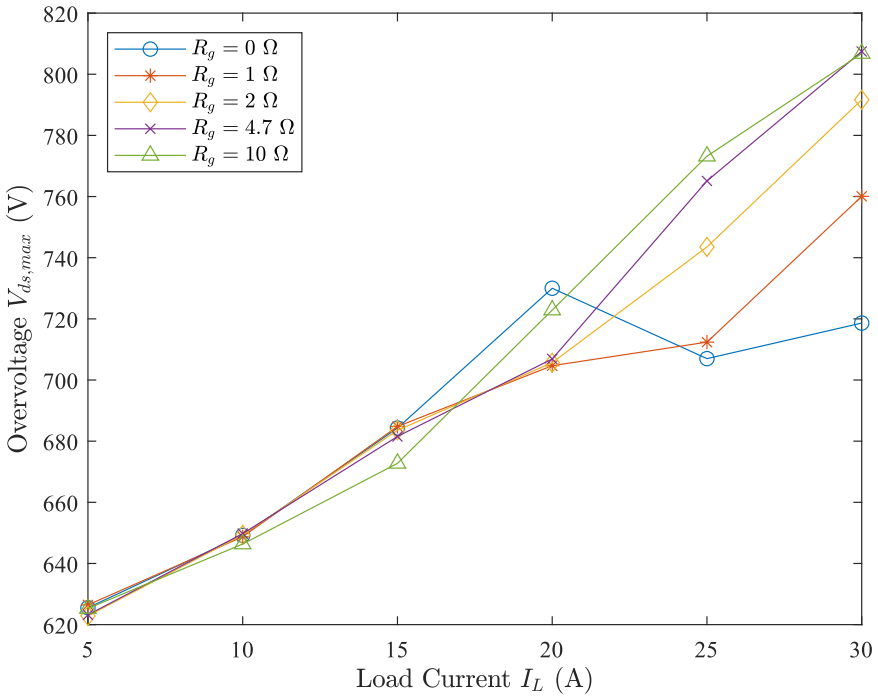
Figure 2.9: Switching transient overvotlage experimental characterization setup.

Table 2.1: Switching transient overvoltage experimental setup components

Item	**Part Number**	**Note**
MOSFET	C3M0065090J	900 V/35 A, TO-263-7
Diode	C4D20120D	1200 V/33 A, TO-247-3
Driver buffer	IXDN609SI	9 A source/sink current
V_{gs} probe	TPP1000	1000 MHz
V_{ds} probe	TPP0850	800 MHz
I_d sensor	SSDN-414-01	2000 MHz*

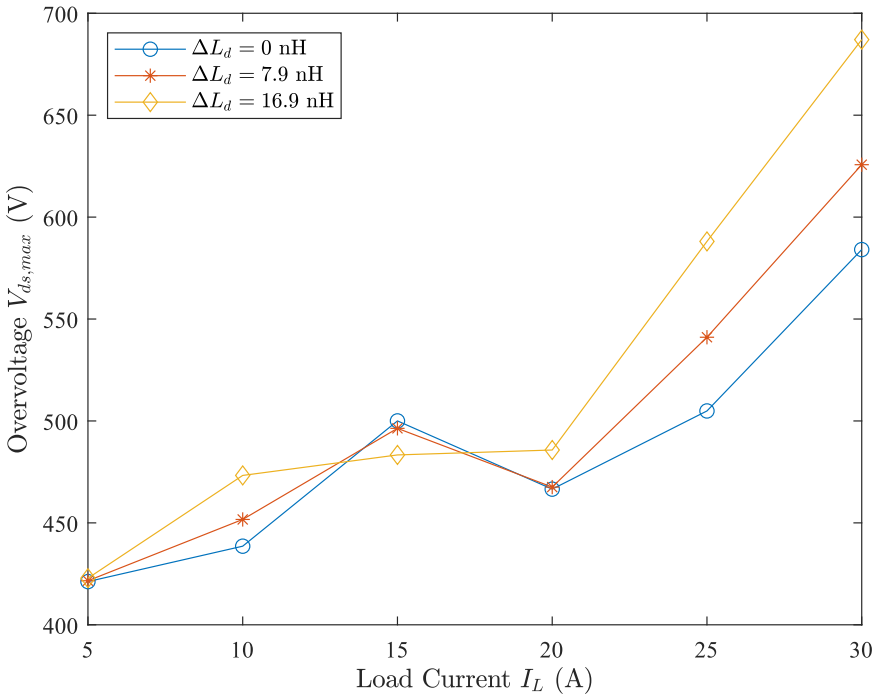


(a)

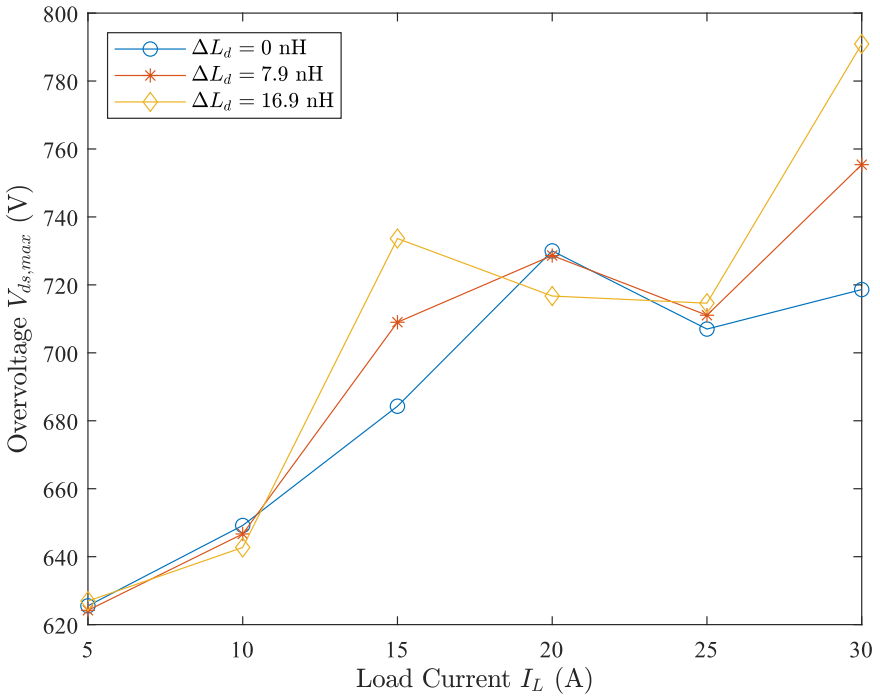


(b)

Figure 2.10: Experimental turn-off maximum voltage stress with different gate resistances at different DC source voltage: (a) $V_d = 400$ V; (b) $V_d = 600$ V.



(a)



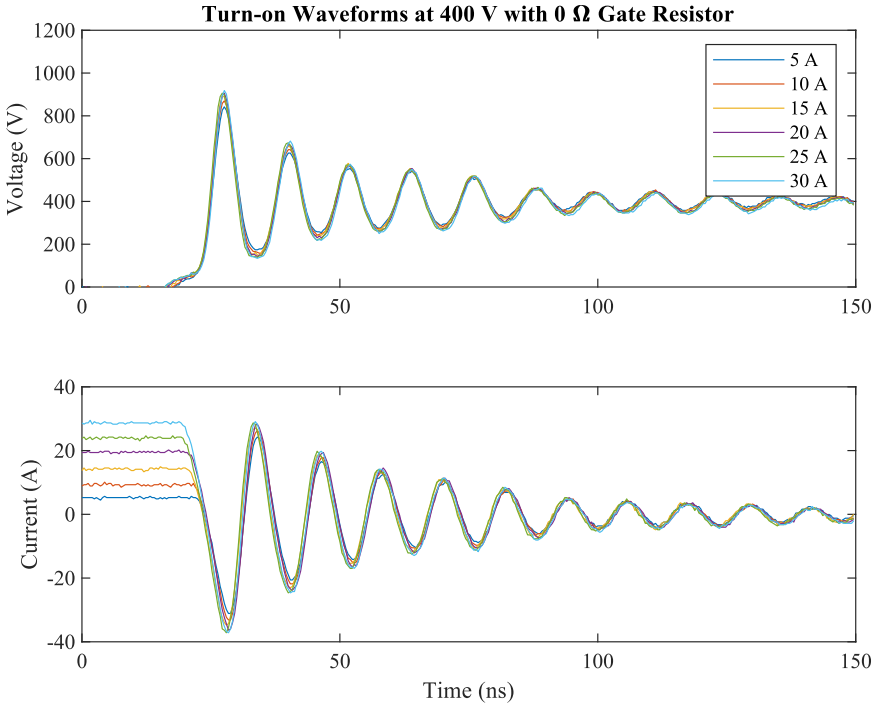
(b)

Figure 2.11: Experimental turn-off maximum voltage stress with different extra drain inductance: (a) $V_d = 400$ V; (b) $V_d = 600$ V.

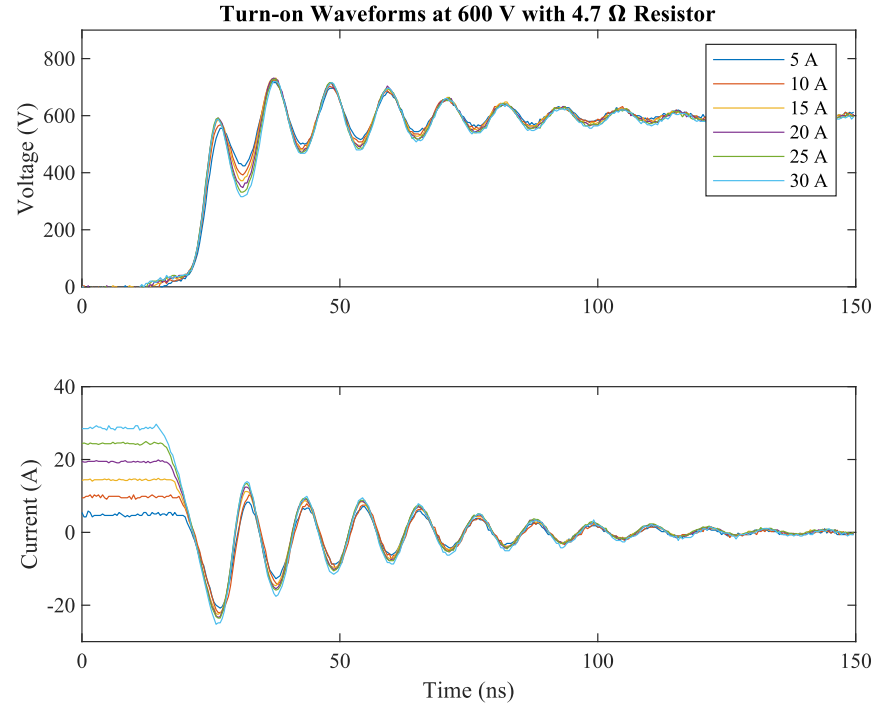
The drain-source voltage probe directly measures between the drain tab and the Kelvin-source connection. Therefore, the turn-off overvoltage measurement here minimizes the external package inductance influence and should reflect the actual overvoltage across the MOSFET. In Fig. 2.10a, it is clearly shown that the impact of load current and gate resistance on turn-off overvoltage is nonlinear. At $I_L = 15$ A, the overvoltage is worst when the switching speed is the fastest $R_g = 0\ \Omega$. However, at $I_L = 20$ A, the overvoltage is worst when the switching speed is the slowest $R_g = 10\ \Omega$. Likewise, when $R_g = 0\ \Omega$, the overvoltage at $I_L = 15$ A is higher than that from $I_L = 20$ A. Similarly, in the drain inductance sweep in Fig. 2.11a, at 15 A load current, the largest extra power loop inductance of $\Delta L_d = 16.9$ nH surprisingly results in the lowest overvoltage. Although not as extreme as in the ideal case in Fig. 2.4, the nonlinear relationship between the turn-off overvoltage and switching speed and parasitic inductance is obvious.

2.4.2 Turn-on overvoltage

The experimental waveforms of the diode voltage and current during the MOSFET's turn-on transient are shown in Fig. 2.12. Note that because the diode C4D20120D is in TO-247 package, the measurement of its voltage includes inductive voltage drop due to the lead and packaging inductance. So the "real" voltage across the diode cathode and anode will be higher than the captured waveforms. Still, from Fig. 2.12 the turn-on overvoltage is almost independent of the load current. The switching transient waveforms nearly overlap with each other under different load current conditions. Similarly, given the same DC source voltage V_d and gate resistance R_g, the turn-on transient overvoltage is also nearly identical.



(a)



(b)

Figure 2.12: Experimental turn-on transient diode voltage v_{ka} and current i_{ak} waveforms: (a) $V_d = 400$ V, $R_g = 0$ Ω; (b) $V_d = 600$ V, $R_g = 4.7$ Ω.

Also note in Fig. 2.12a, the waveform during the oscillation looks sinusoidal but is clearly affected by the nonlinearity of the capacitance C_{ka}.

It is also trivial to see that the turn-on overvoltage decreases with slower switching speed, in contrast to the turn-off overvoltage. Likewise, the relationship between the turn-on overvoltage and the extra parasitic loop inductance is shown in Fig. 2.13. The overvoltage increases monotonically with the extra parasitic inductance.

In summary, the experimental results confirms the previous ideal and non-ideal analysis results. The turn-off overvoltage is highly nonlinear and may exhibit lower value under faster switching speed or larger power loop inductance. The turn-on overvoltage, on the other hand, has little dependence on the load current.

2.5 Numerical Modeling and Analysis Verification

As shown earlier, predicting the turn-on overvoltage requires solving a high-order nonlinear system, which is more attainable with numerical solvers. This then naturally leads to the use of SPICE simulators, which allow easy and detailed semiconductor device modeling and faster calculation speed.

2.5.1 Semiconductor output characteristics

The first step in modeling the switching transient behavior is obtaining an accurate device model. Wolfspeed provides SPICE models for their devices online [97]. However, there is a large discrepancy between the provided model for C3M0065090J and its actual output characteristics captured on a curve tracer, as shown in Fig. 2.14. The difference is most

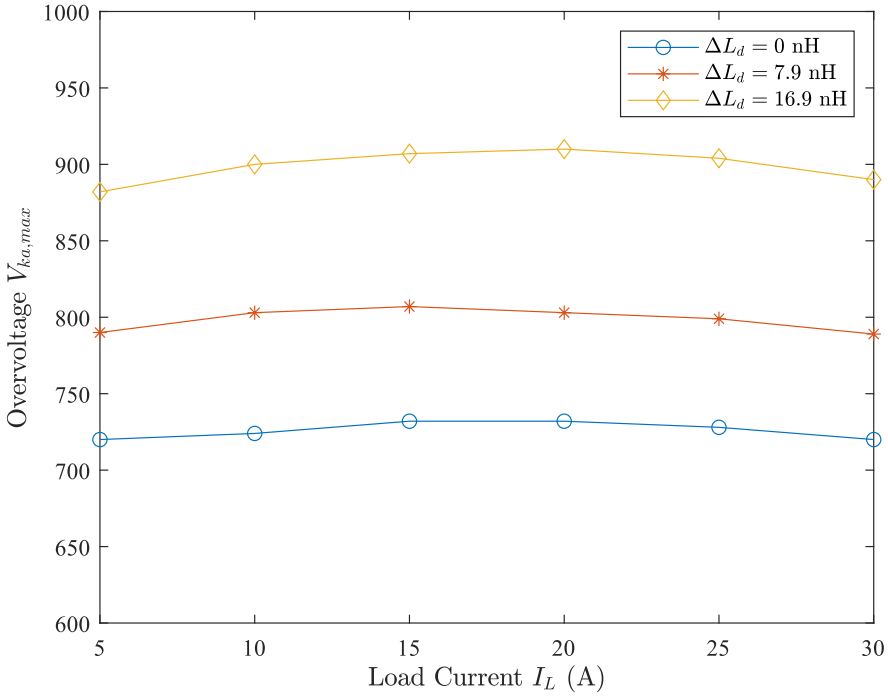


Figure 2.13: Relationship between parasitic inductance and turn-on maximum voltage stress.

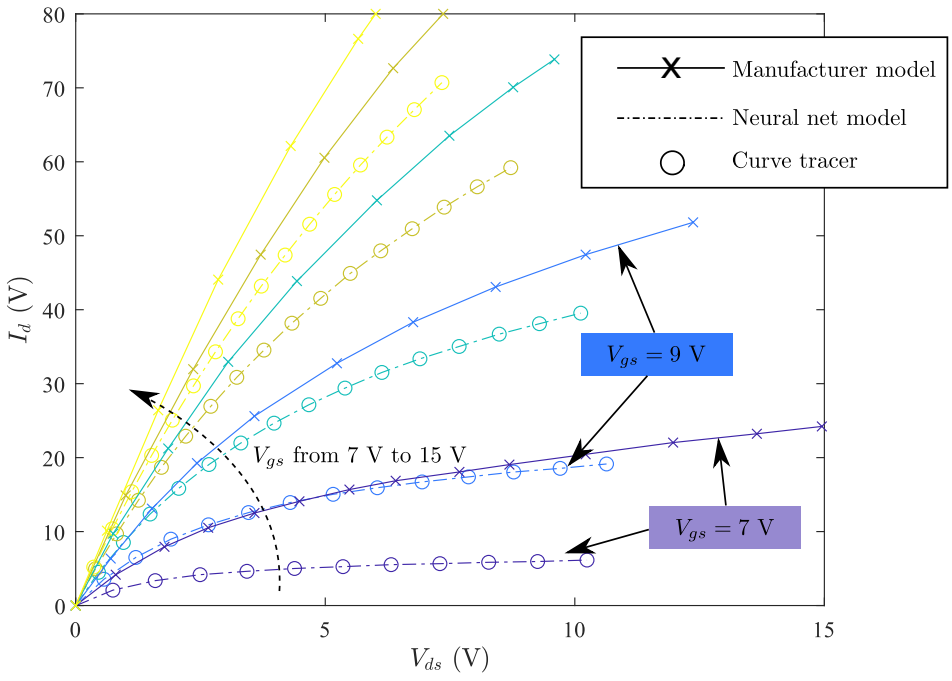


Figure 2.14: Output characteristics comparison between provided model and actual curve tracer capture.

severe in the low gate driving range, where V_{gs} is around 9.0 V. For example, at $V_{gs} = 9.0$ V and $V_{ds} = 8.0$ V, the manufacturer model predicts the drain current to be around 40 A, but the curve tracer capture shows the drain current is only around 15 A.

To represent the actual device more truthfully, the output characteristics are modeled directly with the curve tracer data. A trivial way to do this is using the lookup table built in SPICE. However, in practice, it is found that convergence issues may arise due to the "choppiness" in the lookup table. The more common way is to curve fit the output characteristics to some behavioral functions. However, the functions are usually quite complicated and it may be tedious and time-consuming to tune the parameters. On the other hand, artificial neural networks are widely used as a data regression tool. Given just one hidden layer and ten neurons, the accuracy is extremely good, as shown in the comparison between the artificial neural network model and the curve tracer data in Fig. 2.14. Note though, due to nature of the statistical nature of neural network, it can only predict the range of data it has been trained. Therefore, to guarantee a reasonable model in switching transients, the experimental output characteristics data must cover the entire operating range of the device.

2.5.2 Turn-off comparison

The simulation model in LTSpice is shown in Fig. 2.15. The gate-source capacitance C_{gs} is assumed constant. The various circuit parasitic element values are shown in Table 2.2. Also note that in addition to the MOSFET internal gate resistance $R_{g,int}$, the gate driver IC also has internal source or sink resistance during the switching transient. In either turn-on or

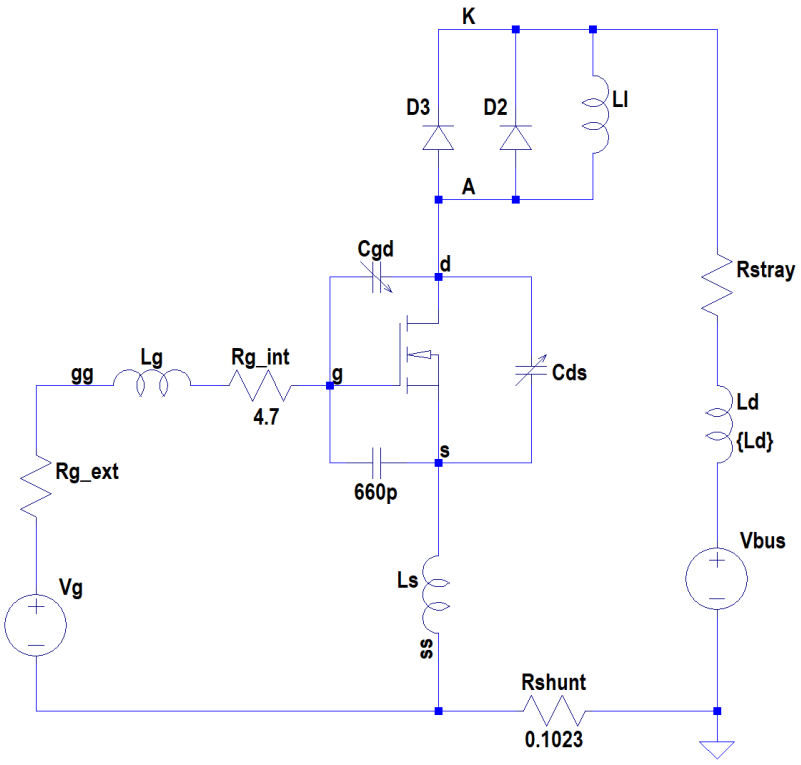


Figure 2.15: Simulation model for turn-on and turn-off transient in LTSpice.

Table 2.2: Switching transient overvoltage simulation parameters

Parameter	Value
Gate inductance L_g	10 nH
Common source inductance L_s	0.8 nH
Power loop inductance L_d	43 nH
Stray resistance R_d	200 mΩ
Internal gate resistance $R_{g,int}$	4.7 Ω
Gate driver source resistance R_{source}	2.0 Ω
Gate driver sink resistance R_{sink}	1.5 Ω

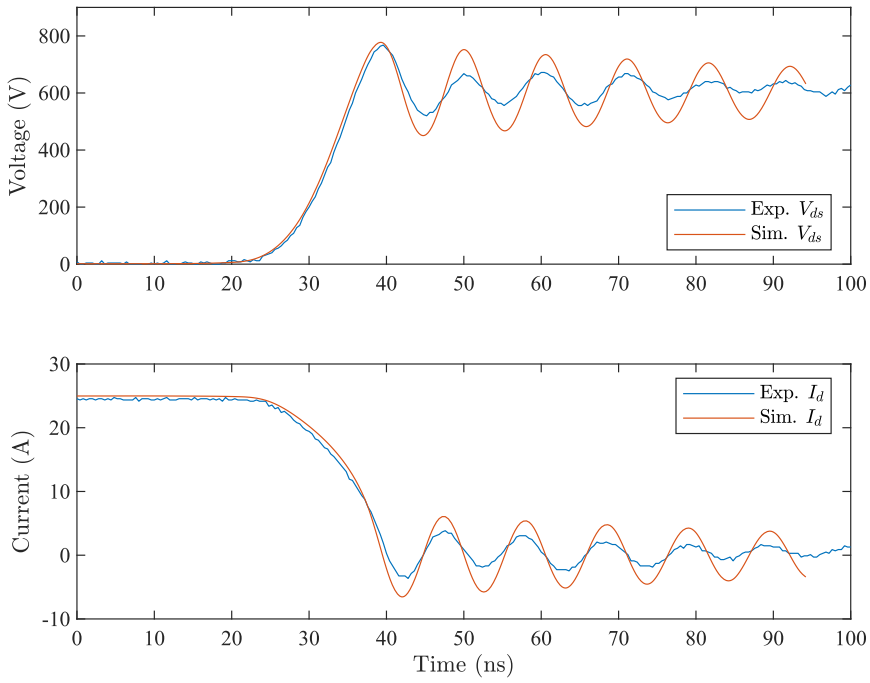


Figure 2.16: Turn-off transient waveform comparison between experimental resutls and SPICE models: $V_d = 600$ V, $I_d = 25$ A, $R_g = 4.7$ Ω.

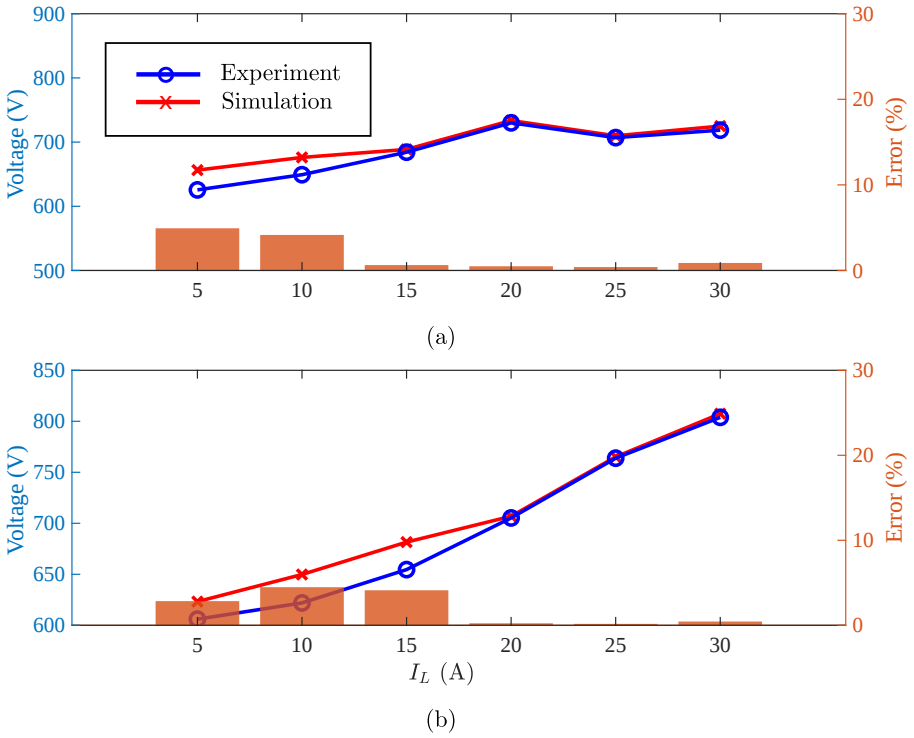


Figure 2.17: Simulated and experimental turn-off maximum voltage stress comparison with: (a) $V_d = 600$ V and $R_g = 0\ \Omega$; (b) $V_d = 600$ V and $R_g = 4.7\ \Omega$.

turn-off transient simulation, the respective source or sink resistance is added to the external gate resistance $R_{g,ext}$. Also note that, although the SiC MOSFET C3M0065090J uses a Kelvin source for the gate driver, a small common source inductance $L_s = 0.8$ nH is added in the simulation.

The turn-off switching transient waveforms comparison between the SPICE model and the experimental results are shown in Fig. 2.16. The switching transient waveforms are very well replicated in the SPICE modeling. The rise and fall edge of the drain-source voltage V_{ds} and drain current I_d match very closely with each other, which suggest the numerical model closely represents the real circuit. The oscillation after the overvoltage peak is more severe in the simulation, likely due to the lack of AC resistance in the SPICE simulation.

The predicted maximum voltage stress from the SPICE model and the experimental values are compared in Fig. 2.17. The DC source voltage $V_d = 600$ V and the gate resistance is 0 Ω or 4.7 Ω. Generally, the numerical model closely matches the experimental results, showing maximum percentage error of less than 5.0%. When the load current I_L is large, the error is nearly minimal. The error is relatively larger when the load current is small. This is probably because of the coarse gate driver model, which play a more important role in light load conditions. The numerical model is able to recreate the nonlinear behavior between switching speed and overvoltage. With I_L being 25 A or 30 A, the overvoltage when $R_g = 0$ Ω is smaller than when $R_g = 4.7$ Ω. Similarly, the nonlinear relationship with load current I_L is also reproduced when the switching speed is fast and $R_g = 0$ Ω. Therefore, the numerical model here further confirms the important role of different oscillation pattern transition for the turn-off transient.

2.5.3 Turn-on comparison

The turn-on switching transient waveforms comparison between the SPICE model and the experimental results are shown in Fig. 2.18. Again, the SPICE model outputs very similar waveforms compared to the experimental data. Like the turn-off transient, the oscillation after the actual switching action is more significant in the SPICE model. Note that because the diode in experiment uses a TO-247 package, its package lead inductance of 9.0 nH is considered in the comparison here. The simulated V_{ka} includes both the "real" diode voltage and the inductive voltage across this 9.0 nH inductance. Again, the waveform comparison confirms the effectiveness of the numerical model.

The overvoltage comparison between the SPICE model and the experimental values is shown in Fig. 2.19. The numerical model is able to recreate and confirm the analysis result that the turn-on overvoltage is largely independent of the load current. When $R_g = 0\ \Omega$, the error between experiment and simulation is similar to the turn-off case as shown in Fig. 2.17, and the error is a lot more significant in the light load condition. However, when $R_g = 4.7\ \Omega$, the error between simulation and experiment is more uniform. This is likely due to the gate driver buffer plays a less important role in the turn-on transient for slower switching speed. The maximum error occurs in the light load condition with $R_g = 0\ \Omega$ and is at around 12.6%. When $R_g = 4.7\ \Omega$, the errors are all at around 7.2%.

2.6 Conclusion and Discussion

The switching transient overvoltage oscillation is discussed in this paper. Circuit analysis focusing on the stage transition and oscillation pattern is first developed, which provides

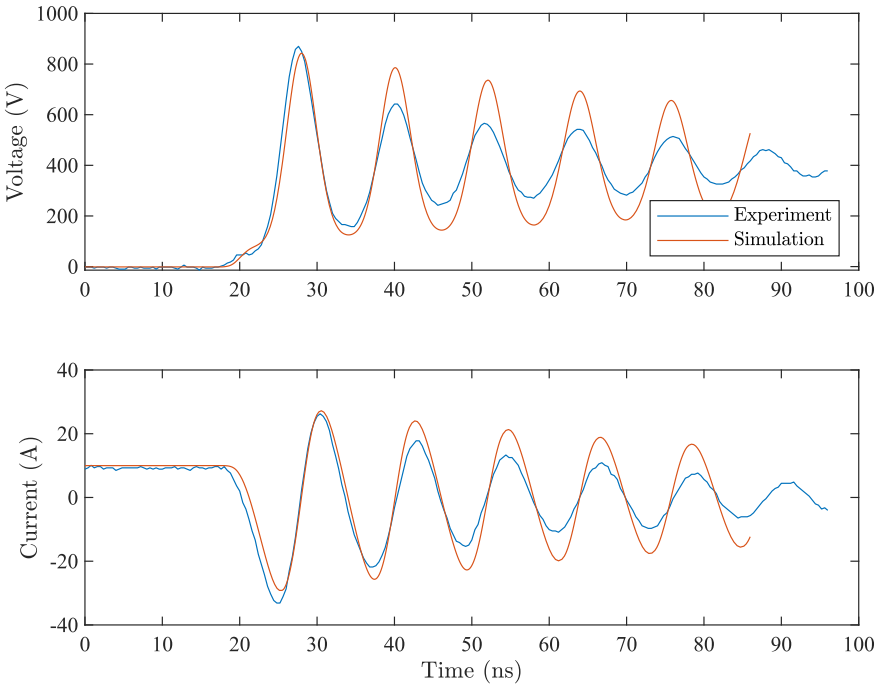


Figure 2.18: Turn-on transient waveform comparison between experimental resutls and SPICE models: $V_d = 600$ V, $I_d = 10$ A, $R_g = 0$ Ω.

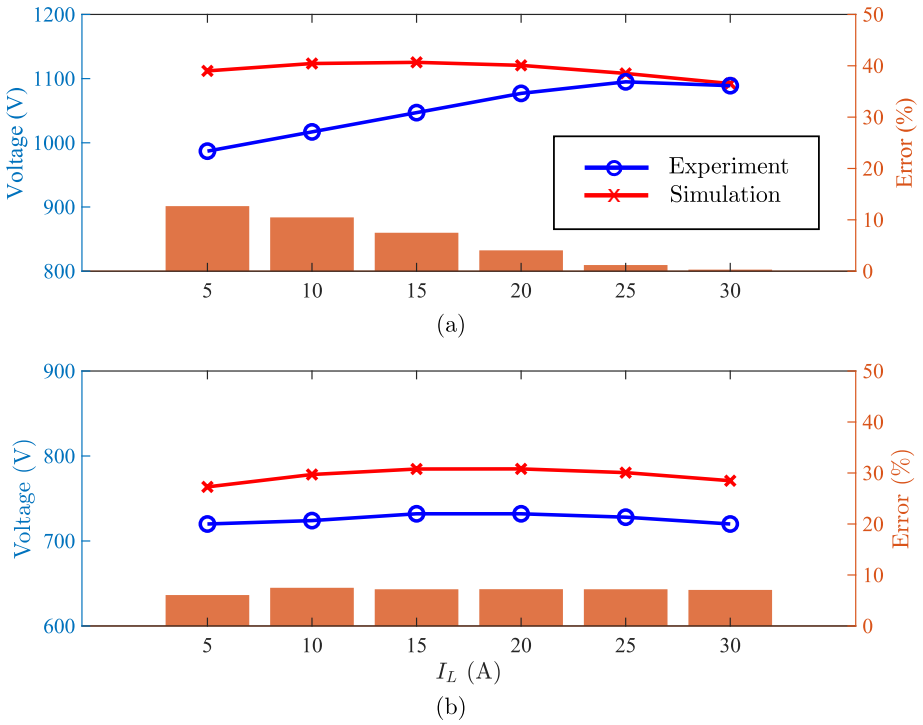


Figure 2.19: Simulated and experimental turn-on maximum voltage stress comparison with: (a) $V_d = 600$ V and $R_g = 0\ \Omega$; (b) $V_d = 600$ V and $R_g = 4.7\ \Omega$.

qualitative understanding of the switching transient. The turn-off overvoltage becomes very nonlinear when the switching speed is fast. Faster switching speed or heavier load current may result in surprisingly lower turn-off overvoltage. The turn-on overvoltage, on the other hand, is much less sensitive to the load current. These special features also provide a general guideline in switching speed and gate driver design. The hypothetical ideal case where the MOSFET can be instantly turned on or off can serve as an outlook for future power semiconductor behaviors. Furthermore, the numerical modeling method with artificial neural network offers a general and easy method to modeling the nonlinear semiconductor behaviors.

For potential future work, the analysis and modeling could be extended to consider the impact of different junction temperatures. The diode here assumes no reverse recovery, and the SiC MOSFET body diode reverse recovery effect could be further included for more general cases.

Chapter 3

Self-Turn-On Phenomena and Large-Signal Switching Transient Stability

3.1 Introduction

The much faster switching speed of wide-bandgap semiconductors helps reduce loss and enables higher switching frequency, but also presents challenges in undesirable ringing during the switching transient. The drain-source voltage V_{ds} overshoot and oscillation in normal switching transients is characterized and analyzed in Chapter 2. Besides the power loop oscillation, excessive amount of gate loop inductance may also result in destructive gate-source overvoltage [17]. In addition to the normal oscillations, abnormal oscillation phenomena have also been reported. An example is the crosstalk phenomenon which happens when the synchronous device is falsely turned on during the active device's turn-on transient

[35], [36]. The root cause is found to be the synchronous device's gate-drain capacitance C_{gd} charging its gate-source votlage V_{gs} above the threshold due to high voltage slew rate in the power loop. Another type of abnormal oscillation phenomenon is reported in [37], [38] where sustained oscillations with SiC JFET and SiC MOSFET are observed in the turn-off transient. The phenomena were partly due to pronounced amount of parasitic elements. Reference [39] reported a simulation phenomenon where a SiC MOSFET channel is temporarily turned on during the turn-off transient when the source inductance is very large. Unstable oscillation is also reported in [40] with parallel MOSFETs in solid-state circuit breaker applications. Gallium nitride (GaN) HFETs abnormal oscillation has also been investigated. In [5], continuous ringing is observed in short circuit condition, and the cause is due to insufficient gate resistance damping. In [41], instability due to the GaN HFET's unique reverse conduction behavior and common source inductance is presented and analyzed.

Although previous works are based on wide-bandgap devices, silicon MOSFETs have been optimized to a stage where the switching transient voltage and current slew rate can be comparable to that of wide-bandgap devices. Thanks to its more complex trench junction structure, the parasitic capacitances of CoolMOS are greatly reduced, especially under strong inversion. When evaluating a CoolMOS's switching behavior, a new abnormal oscillation phenomenon is observed. During the turn-off transient, the oscillation magnitude does not keep decreasing but can spuriously increase. In the worst case, the oscillation is sustainable and keeps going, as shown in Fig. 3.1. This oscillation pattern can be particularly hazardous for power electronics converters as the switching control is completely lost. To understand the phenomena, the same switching behavior was first recreated in SPICE simulation. It is

observed that after the MOSFET channel is pinched off, it is turned on again by its own common source inductance. Therefore, the phenomenon is named "self-turn-on".

Power semiconductor switching transient stability has been analyzed with small-signal models in several previous works. The unstable switching due to gate-drain capacitance C_{gd} feedback has been reported in [26]. Similar phenomena have been discussed with oscillator theory in [38]. Optimizing both the gate-drain capacitance C_{gd} and common source inductance L_s to mitigate the unwanted oscillation is presented in [98]. Reference [41] analyzes the instability by constructing the loop gain function. These methods leverage the small-signal model for analysis which requires careful selection of operating points. A large-signal analysis approach based on the Lyapunov function for electrical networks was proposed in [99] by Brayton and Moser. The large-signal stability can be analyzed by evaluating the properties of a mixed potential function. To further understand the root cause of the self-turn-on phenomenon, it is analyzed with this large-signal approach. It is shown that the mixed potential function can effectively describe the switching transient. The asymptotic stability criterion is also an effective and conservative prediction of the switching transient stability. The root cause of the self-turn-on phenomenon is found to be not only the common source inductance but also the unconventional voltage dependence of its parasitic capacitances.

3.2 Experimental Self-Turn-On Phenomena

The self-turn-on phenomena are observed at room temperature when characterizing a Si MOSFET, which is 4th generation CoolMOS IXKR47N60C5 from IXYS. The simplified experimental setup is shown in Fig. 3.2. The MOSFET has a voltage rating of 600 V and a

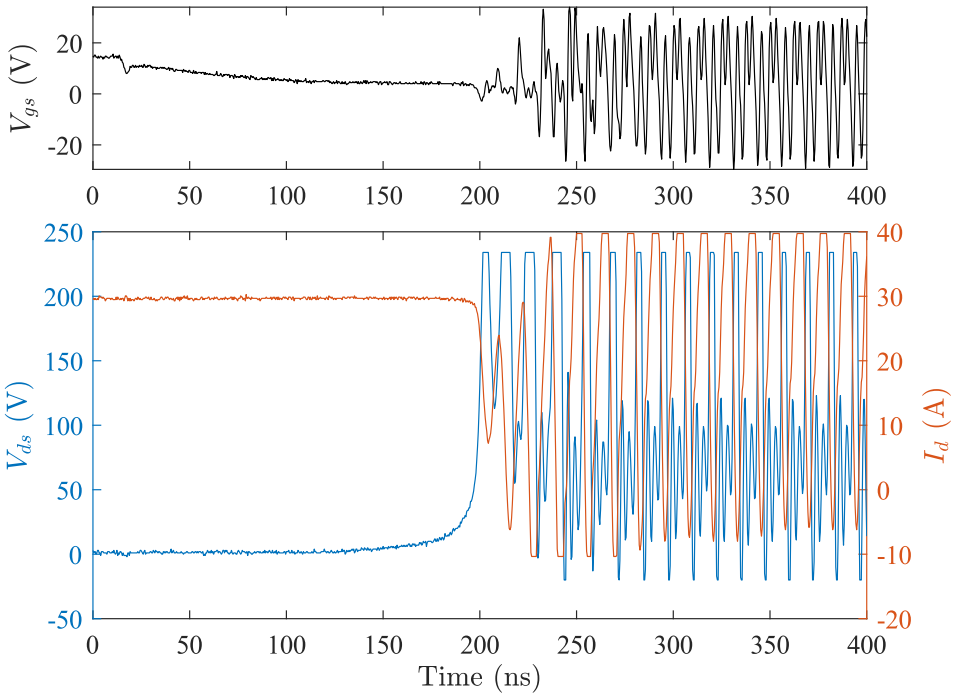


Figure 3.1: Experimental waveforms showing continuous self-turn-on oscillation when testing IXKR47N60C5 in turn-off transient with 200 V DC link, 30 A load current and 4.7 Ω gate resistance.

current rating of 47 A. The free-wheeling diode is a SiC Schottky diode, C4D20120D from Wolfsped. Both devices are in TO-247 package. The gate driver IC is a high-speed gate driver buffer IXDN609 from IXYS. The on-state driving voltage is 15.0 V while the off-state is 0.0 V. The experimental hardware setup is shown in Fig. 3.3.

Fig. 3.4 shows the experimental waveforms under 200 V DC link and 25 A load current, but with different gate resistances. After the plateau region, the gate-source voltage V_{gs} starts to exhibit significant spikes. The drain-source voltage V_{ds} also shows abnormal behavior that the ringing magnitude first increases before decreasing and settling down. The current flowing through the MOSFET I_d also shows significant amount of ringing. Comparing the phenomena with different gate resistances, the one with 2.0 Ω gate resistance shows the worst oscillation.

Fig. 3.5 shows the abnormal ringing in all three measurements getting worse with higher load current. While the ringing frequency remains the same, the magnitude is significantly larger at 25 A load current. In the worst case when $I_L = 30$ A, the oscillation is continuous and does attenuate, as shown in Fig. 3.1. However, the DC link voltage has an opposite effect on the phenomena, as shown in Fig. 3.6. When the DC link voltage is increased from 200 V to 400 V, the self-turn-on phenomena was much less significant.

In summary, the self-turn-on phenomena appear when the switching is relatively fast but the worst case is not necessarily when the gate resistance is the smallest. It only appears when the load current is high enough, and may diminish when the DC link voltage is higher.

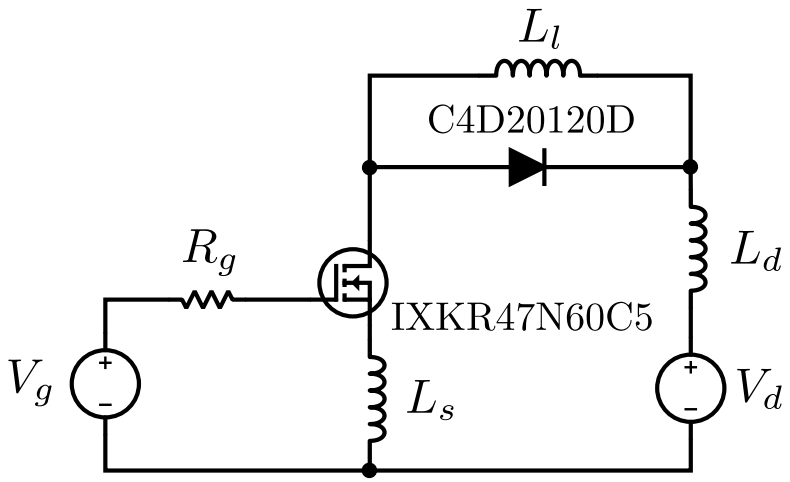


Figure 3.2: Simplified experimental setup circuit schematic for self-turn-on phenomena.

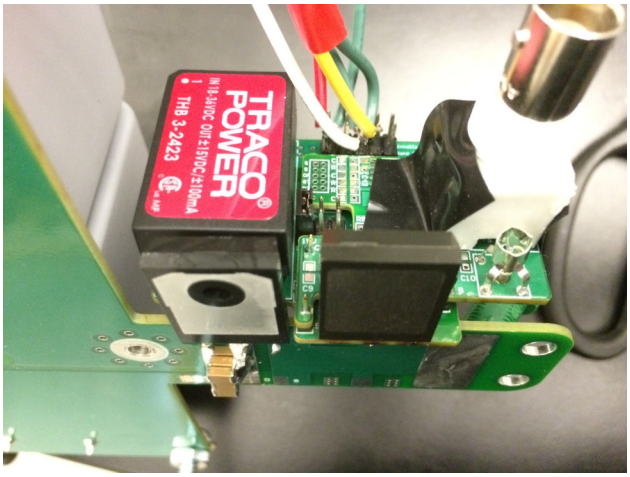


Figure 3.3: Experimental hardware setup for characterizing self-turn-on phenomena.

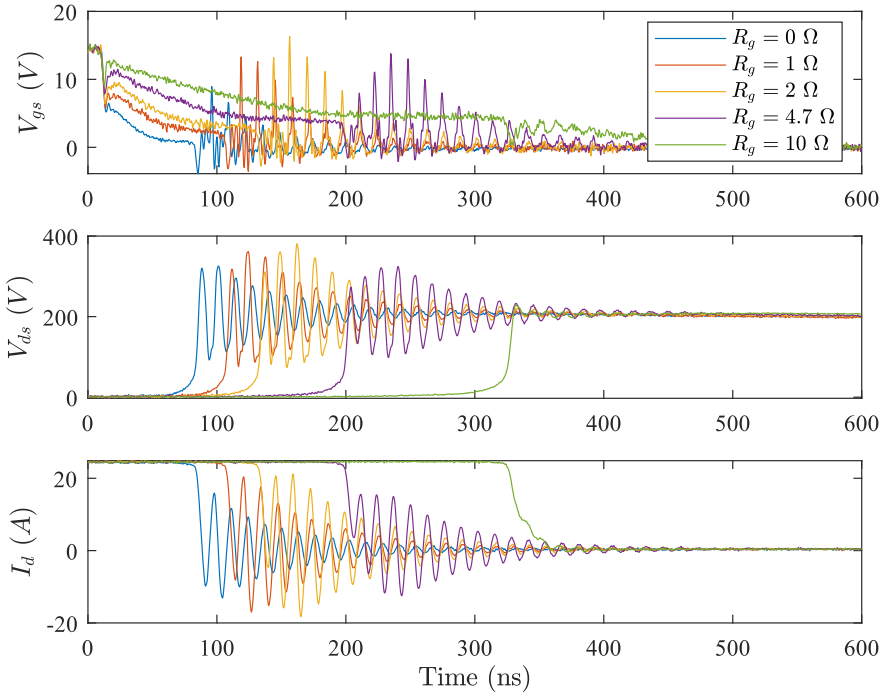


Figure 3.4: Turn-off transients with different gate resistances under 200 V DC link and 25 A load current showing different degrees of self-turn-on phenomena.

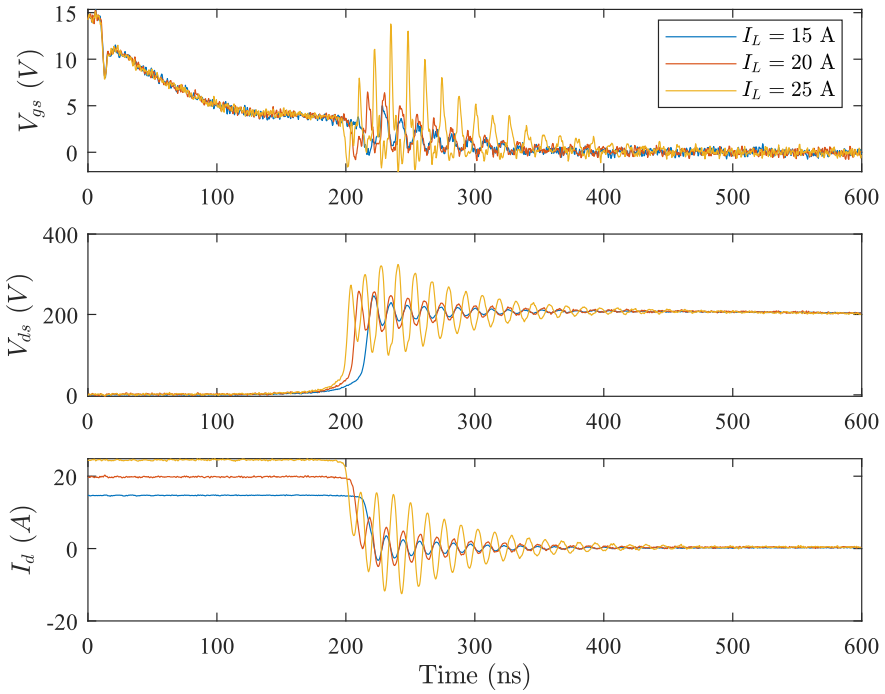


Figure 3.5: Turn-off transients with different load currents under 200 V dc link and 4.7 Ω gate resistance.

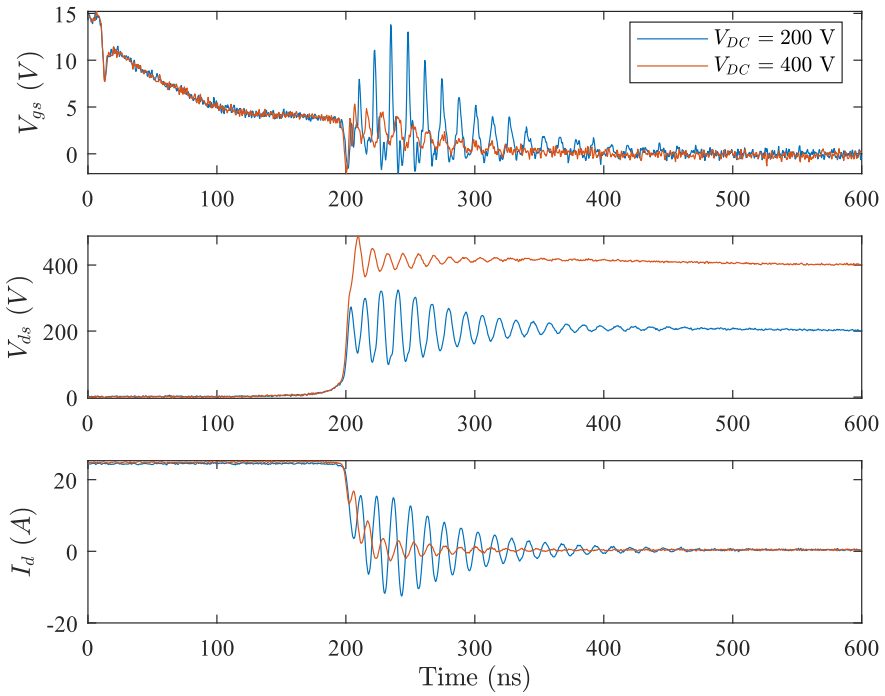


Figure 3.6: Turn-off transients with different DC link voltages under 25 A load current and 4.7 Ω gate resistance.

3.3 SPICE Modeling and Analysis

The unusual spikes in the gate-source voltage V_{gs} measurement and abnormal oscillations in both drain-source voltage V_{ds} and drain current I_d measurements indicate that the MOSFET is turned on spuriously during the turn-off transient. A simulation model is built in SPICE to shed light into this undesirable switching behavior. The simulation model is shown in Fig. 3.7. The transfer characteristics and parasitic capacitances of the MOSFET are modeled as lookup tables with the data from the device datasheet. The internal gate resistance is not provided in the datasheet, and it is assumed to be 1.0 Ω. The free-wheeling diode model is provided by Wolfspeed. Reasonable assumptions are made on the parasitic inductances, with the power loop inductance $L_d = 20.0$ nH, the gate inductance $L_g = 10.0$ nH, and the common source inductance $L_s = 4.0$ nH.

The simulation result of the turn-off transient under 200 V DC link, 25 A load current with 2.0 Ω gate resistance is shown in Fig. 3.8. The simulation model successfully recreated the experimental abnormal oscillations. As the switching transient progresses, the drain-source voltage V_{ds} slew rate is high, and the MOSFET channel current I_x(Channel:D) is very quickly pinched off. Once the channel is turned off, the power loop is then a pure LC resonant network. The voltage across the common source inductance $V(s, ss) = L_s \frac{di_s}{dt}$ acts as a voltage bias back into the gate loop and charges the gate-source voltage V_{gs} up. The gate-source voltage V_{gs} may exceed the threshold voltage V_{th} and the MOSFET channel is turned on again, represented by the huge spikes in the MOSFET channel current I_x(Channel:D) in simulation. Likewise, the gate-drain capacitance C_{gd} under the high voltage slew rate acts as a current source charging through the gate node. However, in both simulation and experiments,

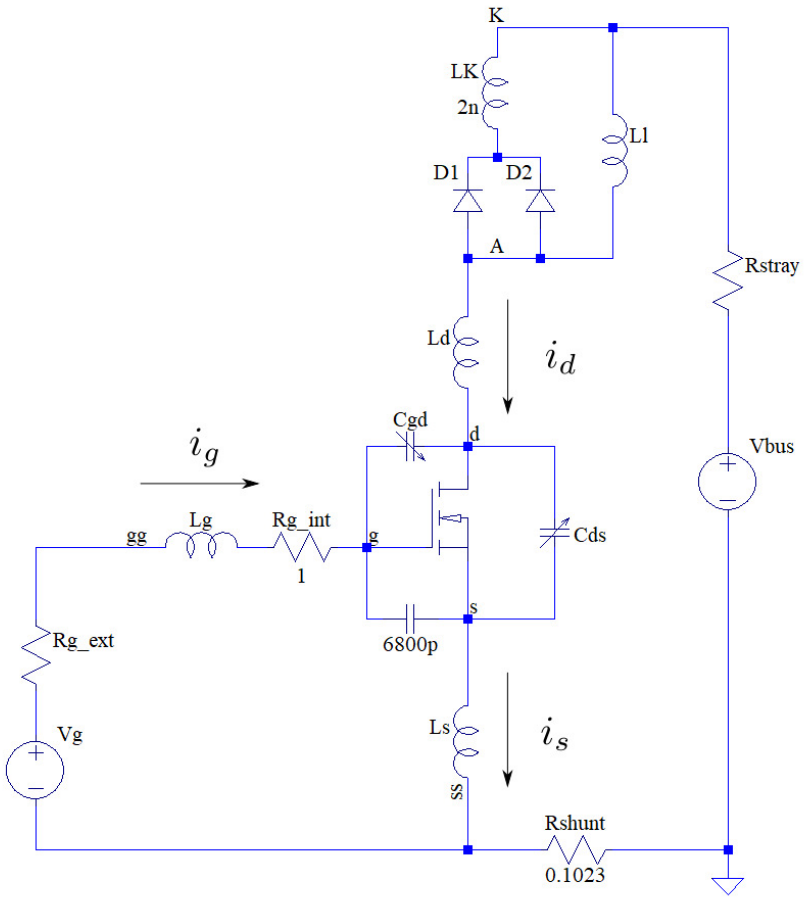


Figure 3.7: SPICE simulation and analysis model for the self-turn-on phenomena.

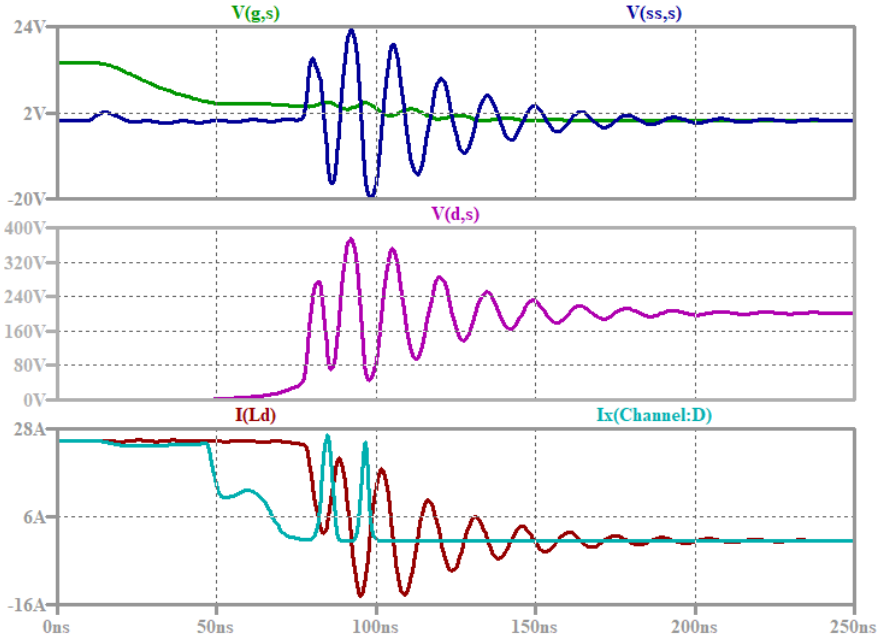


Figure 3.8: SPICE simulation result under 200 V DC link and 25 A load current with 2.0 Ω gate resistance.

it is found that the spurious turn-on events happen after the drain-source voltage V_{ds} exceeds 100 V. The value of gate-drain capacitance C_{gd} is quite small due to its voltage dependence. More importantly, in simulation, the self-turn-on phenomena persists after removing the gate-drain capacitance C_{gd} but disappears after removing the common source inductance L_s.

Therefore, in the time domain, the root cause of the phenomena is the device channel current quickly pinched off because of the parasitic capacitance, and the gate-source voltage V_{gs} charged above the threshold voltage V_{th} due to the common source inductance.

The MOSFET channel being turned off during the voltage rise time can be explained by the MOSFET's parasitic capacitance curve. Reference [26] provides an expression for the drain-source voltage V_{ds} during the turn-off transient, assuming the gate-source voltage V_{gs} remains constant and the parasitic capacitance of the free-wheeling diode can be neglected,

$$\frac{dv_{ds}}{dt} = \frac{I_L + g_{fs}V_{th}}{C_{ds} + (1 + g_{fs}R_g)C_{gd}}, \tag{3.1}$$

where I_L is the load current, g_{fs} is the MOSFET transconductance, and V_{th} is the MOSFET threshold voltage. Therefore, the displacement current flowing through the output capacitance can be written as

$$I_{disp} = (I_L + g_{fs}V_{th}) \cdot \frac{1 + \frac{C_{gd}}{C_{ds}}}{1 + (1 + g_{fs}R_g)\frac{C_{gd}}{C_{ds}}}. \tag{3.2}$$

Note the first term in brackets $(I_L + g_{fs}V_{th})$ depends only on the load current and MOSFET characteristics. And the second fractional term $\frac{1+\frac{C_{gd}}{C_{ds}}}{1+(1+g_{fs}R_g)\frac{C_{gd}}{C_{ds}}}$ depends only on the total gate resistance R_g and MOSFET characteristics. Considering the nonlinearity of parasitic capacitances, the fractional term is plotted in Fig. 3.9b against the drain-source voltage

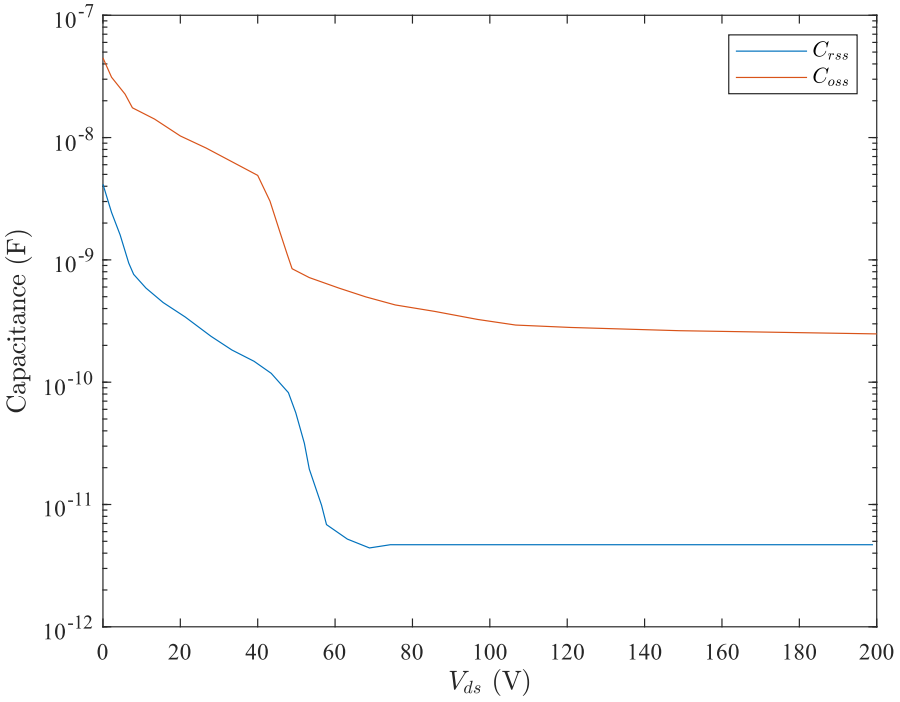
V_{ds}. The fractional term drastically increases at around 50 V due to the unconventional nonlinearity of the MOSFET's parasitic capacitances. When $R_g = 2.0\ \Omega$, the maximum displacement current when the load current $I_L = 25$ A can be approximated

$$I_{disp,max} = (I_L + g_{fs}V_{th}) \cdot 0.48 = 98.4\ \text{A} \gg I_L. \tag{3.3}$$

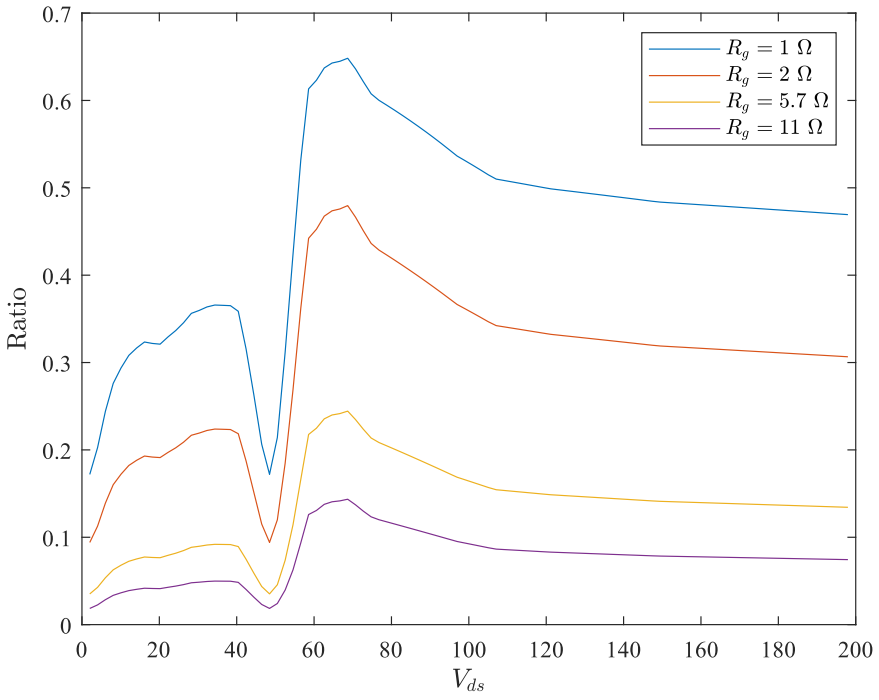
This means the channel is turned off during the voltage rising stage and the power loop current I_d is now only flowing through the parasitic capacitances. In fact, at this point, the assumptions for (3.2) no longer hold true. Nevertheless, this still shows the parasitic capacitances have a significant impact on the voltage slew rate and the displacement current. When the fractional term is large enough, the MOSFET channel may pinch off during the voltage rising stage.

Equation (3.2) also explains why self-turn-on phenomenon does not happen when the gate resistance R_g is large. As shown in Fig. 3.9b, the fractional term is much smaller with larger gate resistances. The switching transient voltage slew rate $\frac{dv_{ds}}{dt}$ is also much slower. Therefore, the channel does not pinch off in the voltage rising stage when the gate resistance R_g is large.

After the MOSFET channel is pinched off if the voltage slew rate $\frac{dv_{ds}}{dt}$ is high, the power loop then becomes a pure LC resonant network. The response from this network is determined by both the DC bias and its initial conditions. For higher load current I_L, the initial condition for the power loop current i_d is larger, which means higher slew rate for the common source inductance current i_s. This explains why the phenomenon does not happen at lower load current. Because the gate driver loses control of the channel current, the current slew rate and



(a)



(b)

Figure 3.9: IXKR47N60C5 parasitic capacitances' impact on voltage slew rate and displacement current: (a) parasitic capacitances versus drain-source voltage; (b) displacement current fractional term against drain-source voltage.

oscillation pattern after the pinch-off will be the same regardless of the gate resistance. This can be verified by comparing the power loop current i_d waveforms where the gate resistance $R_g < 10\ \Omega$ in Fig. 3.4.

If omitting the gate-drain capacitance C_{gd}, the gate loop can be simplified as the common source inductance L_s charging the gate-source capacitance C_{gs},

$$-C_{gs}L_g\frac{d^2v_{gs}}{dt^2} - C_{gs}R_g\frac{dv_{gs}}{dt} + v_{gs} = L_s\frac{di_s}{dt}. \tag{3.4}$$

While solving the equation can provide an analytical solution to the phenomenon, it more straightforward to consider it from a circuit-level perspective. The moment the MOSFET channel is pinched off, the gate-source voltage v_{gs} drops below its threshold voltage V_{th}. Because the current in the power loop i_d is decreasing, the common source inductance appears as a voltage source charging the gate-source capacitance. However, the gate inductor current $i_g = C_{gs}\frac{dv_{gs}}{dt}$ acts as countermeasure against the common source inductance, because its initial condition at the beginning of this oscillation is still negative. When the gate resistance R_g is small, the initial condition i_{g0} is large and the common source inductance L_s may not be able to charge the gate-source capacitance C_{gs} above the threshold voltage V_{th}, and the self-turn-on phenomenon is less severe. In fact, larger gate loop inductance L_g was found to help mitigate the self-turn-on phenomena [47].

In summary, the self-turn-on phenomenon happens in the following sequence: parasitic capacitances take over all the power loop current due to the high voltage slew rate, the power and gate loop become pure LC resonant circuits. The high current slew rate in the power loop makes the common source inductance act as a voltage source charging the gate-source

capacitance C_{gs}, whose voltage V_{gs} may exceed the threshold voltage V_{th}. The MOSFET channel is then falsely turned on. The process may happen a few times before finally settling down, or, in the worst case, continues indefinitely.

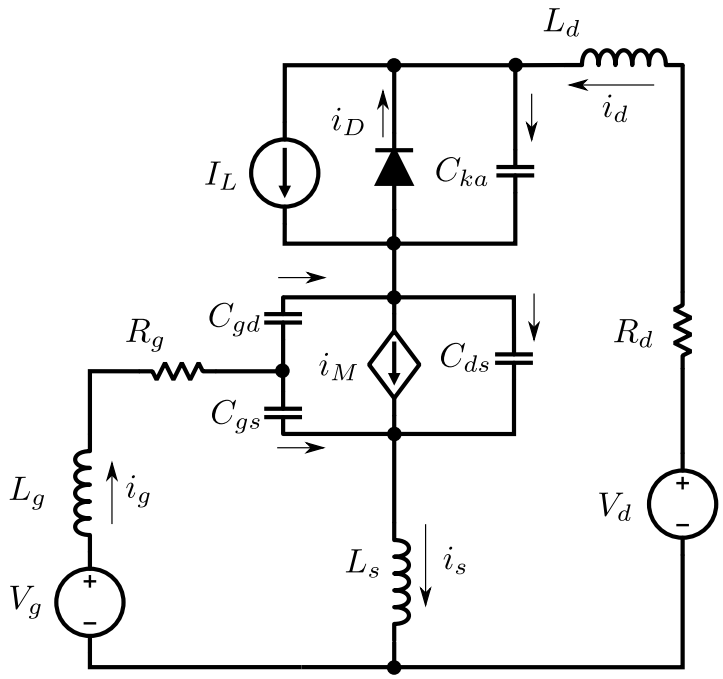
3.4 Large-Signal Switching Transient Stability

Although the previous section recreates the experimental phenomena in simulation and the root cause is explained qualitatively, a clear stability criterion is still missing. Because of the large-signal and nonlinear nature of the switching transients, Lyapynov theorem, or Brayton-Moser's mixed potential function method, is utilized here to further understand the root cause.

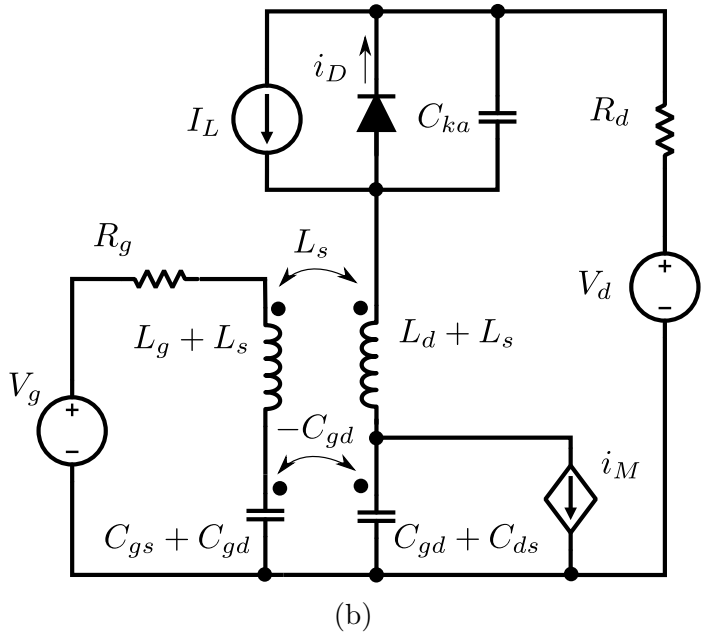
3.4.1 Brayton-Moser's mixed potential function

Lyapunov's direct method provides a framework for analyzing the stability of nonlinear systems, and it relies on constructing a Lyapunov function $P(\boldsymbol{x})$ [100]. Constructing the potential function $P(\boldsymbol{x})$ is generally difficult. Brayton-Moser's mixed potential method is a systematical method to construct such a function for electrical networks [99]. The mixed potential function $P(\boldsymbol{x}) = P(\boldsymbol{i}, \boldsymbol{v})$ has the unit of power and takes the following general form, where $A(\boldsymbol{i})$ is the terms related to the independent current vector $\boldsymbol{i}$, $B(\boldsymbol{v})$ is the terms related to the independent voltage vector $\boldsymbol{v}$, and $N(\boldsymbol{i}, \boldsymbol{v})$ is the terms related to both the current and voltage vectors.

$$P(\boldsymbol{i}, \boldsymbol{v}) = A(\boldsymbol{i}) - B(\boldsymbol{v}) + N(\boldsymbol{i}, \boldsymbol{v}). \tag{3.5}$$



(a)



(b)

Figure 3.10: Switching transient circuit model: (a) phase leg circuit model with parasitic elements; (b) equivalent circuit model with coupling terms.

The equivalent circuit of the switching transient is shown in Fig. 3.10a. During the switching transient, the MOSFET stayed in ohmic region before the gate-source voltage v_{gs} is discharged below the Miller voltage $V_{th} + \frac{I_L}{g_{fs}}$. The drain-source voltage v_{ds} only starts to rise after the MOSFET goes into the saturation region. Therefore, the period in the ohmic region can be neglected. The MOSFET channel current in saturation region and cut-off region can be modeled as a voltage controlled current source,

$$i_M(v_{gs}) = \begin{cases} 0, & \text{if } v_{gs} < V_{th}, \\ g_{fs}(v_{gs} - V_{th}), & \text{otherwise.} \end{cases} \tag{3.6}$$

The diode model here includes a forward voltage $V_f = 0$, a forward resistance of $R_f \neq 0$ and a voltage-dependent parasitic capacitance C_{ka}. The diode current i_D going through its pn junction can be written as,

$$i_D(v_{ka}) = \begin{cases} 0, & \text{if } v_{ka} > 0, \\ -R_f^{-1} v_{ka}, & \text{otherwise.} \end{cases} \tag{3.7}$$

From the circuit in Fig. 3.10a, we can easily see that $i_g + i_d = i_s$ and $v_{gs} = v_{gd} + v_{ds}$. Therefore, the independent variables of the circuit are selected to be $\boldsymbol{x} = [\boldsymbol{i}\ \boldsymbol{v}]^T$, $\boldsymbol{i} = [i_g\ i_d]^T$, and $\boldsymbol{v} = [v_{gs}\ v_{ds}\ v_{ka}]^T$. Because i_s and v_{gd} are dependent variables, the remaining gate-drain capacitance C_{gd} and common-source inductance L_s in Fig. 3.10a are substituted with coupling terms to facilitate the mixed potential function formulation. The equivalent circuit with the coupling elements is shown in Fig. 3.10b.

The first step to formulate the mixed potential function is to construct the current potential for the voltage sources and current-controlled resistors, and voltage potential for the voltage-controlled resistors and current sources [101]. The voltage potential of the MOSFET channel in the saturation region can be represented as a pseudo-resistor [102],

$$\frac{1}{2}G_M v_{ds}^2, \tag{3.8}$$

where $G_M = g_{fs}(v_{gs} - V_{th})/v_{ds}$ when $v_{gs} > V_{th}$, and $G_M = 0$ otherwise.

The voltage potential of the diode current i_D can also be represented as a pseudo-resistor,

$$\frac{1}{2}G_D v_{ka}^2, \tag{3.9}$$

where $G_D = R_f^{-1}$ when $v_{ka} \leq 0$, and $G_D = 0$ otherwise.

The current or voltage potential of the other elements such as the voltage source and capacitors in the circuit Fig. 3.10b can be easily obtained from [99]. Finally, the mixed potential function is given by summing them together,

$$\begin{aligned} P = & - V_g i_g - V_d i_d - I_L v_{ka} \\ & + \frac{1}{2}R_g i_g^2 + \frac{1}{2}R_d i_d^2 \\ & - \frac{1}{2}G_M v_{ds}^2 - \frac{1}{2}G_D v_{ka}^2 \\ & + v_{ds} i_d + v_{gs} i_g + v_{ka} i_d. \end{aligned} \tag{3.10}$$

Rewriting it in the standard form in (3.5),

$$A(\boldsymbol{i}) = -V_g i_g - V_d i_d + \frac{1}{2} R_g i_g^2 + \frac{1}{2} R_d i_d^2, \tag{3.11}$$

$$B(\boldsymbol{v}) = I_L v_{ka} + \frac{1}{2} G_M v_{ds}^2 + \frac{1}{2} G_D v_{ka}^2, \tag{3.12}$$

$$N(\boldsymbol{i}, \boldsymbol{v}) = v_{ds} i_d + v_{gs} i_g + v_{ka} i_d. \tag{3.13}$$

Thus, the mixed potential function or the Lyapunov function for the switching transient circuit is derived. Note the functions G_M and G_D are directly related to the static characteristics of the MOSFET and diode. Although relatively simple equations are used here to describe their characteristics, more complex ones can be easily plugged in to model their behaviors more accurately. If using numerical computations, piece-wise-linear or more complex regression functions can be used [22].

3.4.2 Mixed potential function and system trajectory

Given $\boldsymbol{x} = [\boldsymbol{i}\ \boldsymbol{v}]^T$, $\boldsymbol{i} = [i_g\ i_d]^T$, and $\boldsymbol{v} = [v_{gs}\ v_{ds}\ v_{ka}]^T$, the validity of the mixed potential function in (3.10) can be easily verified because the mixed potential function $P(\boldsymbol{x})$ describes the system trajectory by satisfying the equation below [99],

$$\begin{bmatrix} -L(\boldsymbol{i}) & 0 \\ 0 & C(\boldsymbol{v}) \end{bmatrix} \frac{d\boldsymbol{x}}{dt} = Q(\boldsymbol{x}) \frac{d\boldsymbol{x}}{dt} = \frac{dP}{d\boldsymbol{x}}, \tag{3.14}$$

where the inductance and capacitance matrices are given by

$$L(\boldsymbol{i}) = \begin{bmatrix} L_g + L_s & L_s \\ L_s & L_d + L_s \end{bmatrix}, \tag{3.15}$$

$$C(\boldsymbol{v}) = \begin{bmatrix} C_{gs} + C_{gd} & -C_{gd} & 0 \\ -C_{gd} & C_{gd} + C_{ds} & 0 \\ 0 & 0 & C_{ka} \end{bmatrix}, \tag{3.16}$$

$$Q(\boldsymbol{x}) = \begin{bmatrix} -L(\boldsymbol{i}) & 0 \\ 0 & C(\boldsymbol{v}) \end{bmatrix}. \tag{3.17}$$

Note the capacitances $C_{gs},\ C_{gd},\ C_{ds}$ and C_{ka} are typically nonlinear and voltage-dependent for power semiconductor devices. So the capacitance matrix $C(\boldsymbol{v})$ is voltage dependent. The inductances $L_g,\ L_d$ and L_s are due to the magnetic flux of the PCB trace or semiconductor packaging. They are usually constant and not current-dependent. Therefore, the inductance matrix $L(\boldsymbol{i}) = L$ is considered a constant matrix.

We can immediately see that (3.14) completely describes the switching transient circuit system. The steady-state operating point of the circuit can be trivially found by solving

$\frac{dP}{d\boldsymbol{x}} = 0$, or

$$\frac{dP}{di_g} = -V_g + R_g i_g + v_{gs} = 0, \tag{3.18}$$

$$\frac{dP}{di_d} = -V_d + R_d i_d + v_{ds} + v_{ka} = 0, \tag{3.19}$$

$$\frac{dP}{dv_{gs}} = i_g = 0, \tag{3.20}$$

$$\frac{dP}{dv_{ds}} = -G_M v_{ds} + i_d = 0, \tag{3.21}$$

$$\frac{dP}{dv_{ka}} = -I_L - G_D v_{ka} + i_d = 0. \tag{3.22}$$

It is trivial to see that $i_g = 0,\ i_d = 0,\ v_{gs} = V_g,\ v_{ds} = V_d + I_L R_f,\ v_{ka} = -I_L R_f$ is the steady state operating point of the turn-off transient.

If moving $Q(\boldsymbol{x})$ to the right side of the equation,

$$\frac{d\boldsymbol{x}}{dt} = Q^{-1}(\boldsymbol{x})\frac{dP}{d\boldsymbol{x}}. \tag{3.23}$$

It is obvious that the gradient of every point $\boldsymbol{x}$ on the system trajectory is given by $Q^{-1}\frac{dP}{d\boldsymbol{x}}$, which means the system trajectory is directly related to the product of the gradient of the mixed potential function $P(\boldsymbol{x})$ and the inverse of the passive element matrix $Q(\boldsymbol{x})$.

So far, it is shown that there is a direct relationship between the mixed potential function and the system trajectory. To help illustrate the relationship between the time-domain system trajectory and the mixed potential function Q, time-domain simulation is performed by solving (3.14), and the mixed potential function is plotted against time. The parasitic elements and switching devices in the model are the same as before and listed in Table 3.1.

Table 3.1: Self-turn-on large-signal modeling parameters

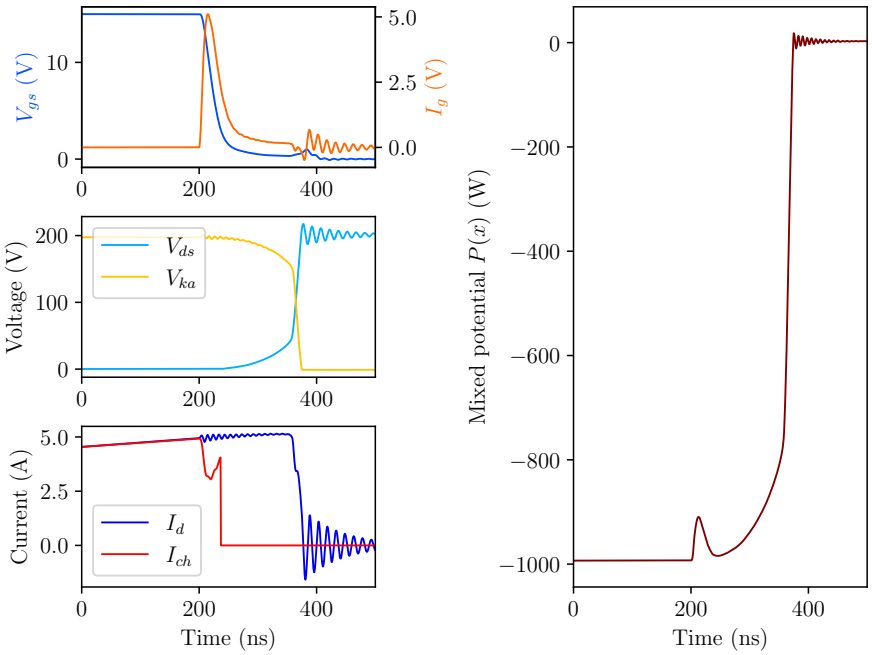
Parameter	Value
MOSFET	IXKR47N60C5
Diode	C4D20120D
L_g	10.0 nH
L_d	20.0 nH
L_s	4.0 nH

Several cases with different load current I_L and DC link voltage V_d are simulated and the switching transient waveforms are plotted along with its mixed potential function $P(\boldsymbol{x})$ in Fig. 3.11. In all four cases, the gate resistance is 2.0 Ω and the DC voltage is kept at 200 V. The load current I_L is varied from 5 A to 30 A. The self-turn-on phenomenon worsens with higher load current, with the switching transient waveforms appear more oscillatory and abnormal. Specifically, the self-turn-on phenomena become much more pronounced when the load current is 30 A, showing the longest oscillation duration. The mixed potential function $P(\boldsymbol{x})$ shows similar trend where it becomes more oscillatory with higher load current. During the turn-off transient, the mixed potential when $I_L = 5$ A drops down to zero with very little oscillation. Note that the oscillatory points of the mixed potential function coincide with the channel current I_{ch} spikes after it first decreases to 0. Therefore, it is shown that the mixed potential function $P(\boldsymbol{x})$ is a direct indication of the switching transient oscillation behavior and stability.

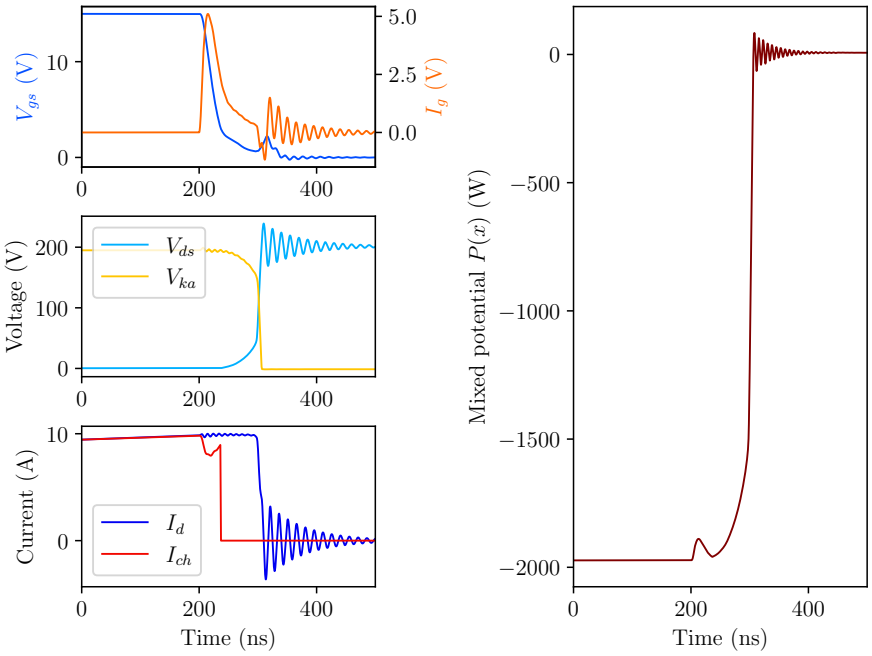
3.4.3 Large-signal asymptotic stability criterion

What is more interesting is whether the large-signal stability criteria can predict the abnormal oscillation and understand its root cause. As shown in (3.14), the system trajectory is completely described by $P(\boldsymbol{x})$ and $Q(\boldsymbol{x})$. This means it is potentially feasible to evaluate a system's stability by only evaluating $P(\boldsymbol{x})$ and $Q(\boldsymbol{x})$, which is the general concept of Lyapunov's direct method.

While [99] provides several theorems to predict the system stability, the theorems require some strict linearity properties of the passive component matrix $Q(\boldsymbol{x})$ or the interconnection

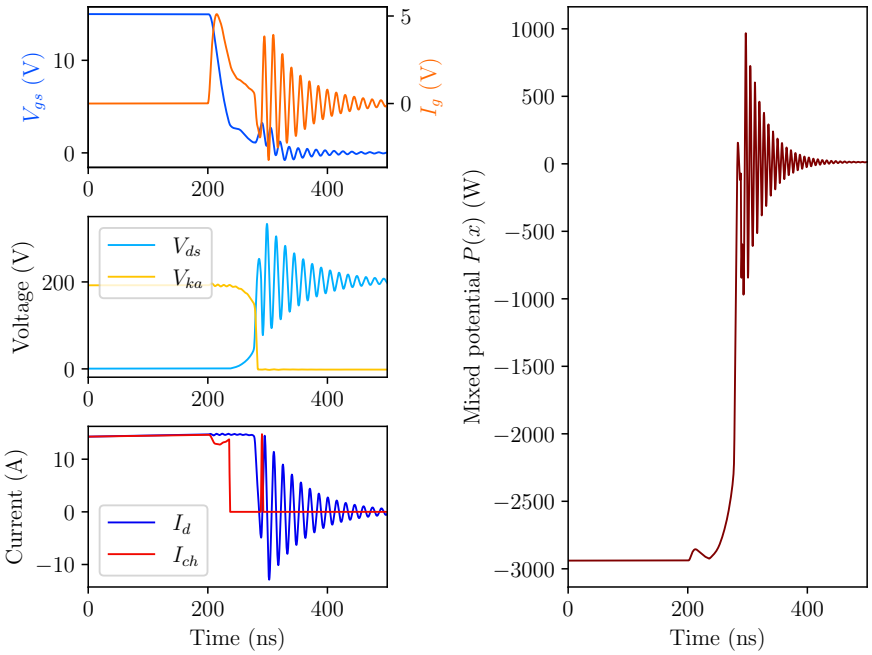


(a)

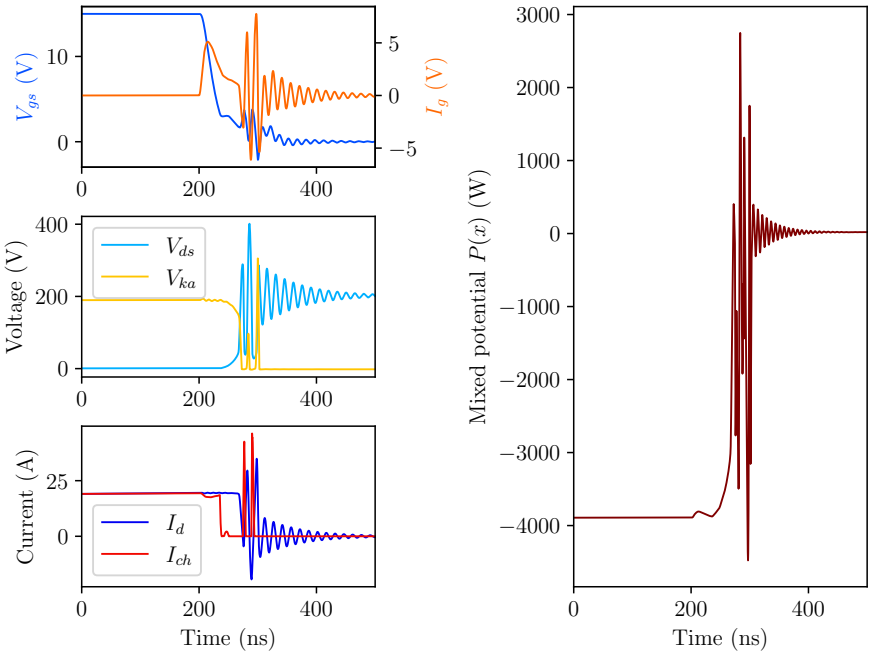


(b)

Figure 3.11: Simulated turn-off switching transient waveforms with self-turn-on phenomena and the corresponding mixed potential function with 200 V DC voltage and 2.0 Ohm gate resistance: (a) 5 A; (b) 10 A.

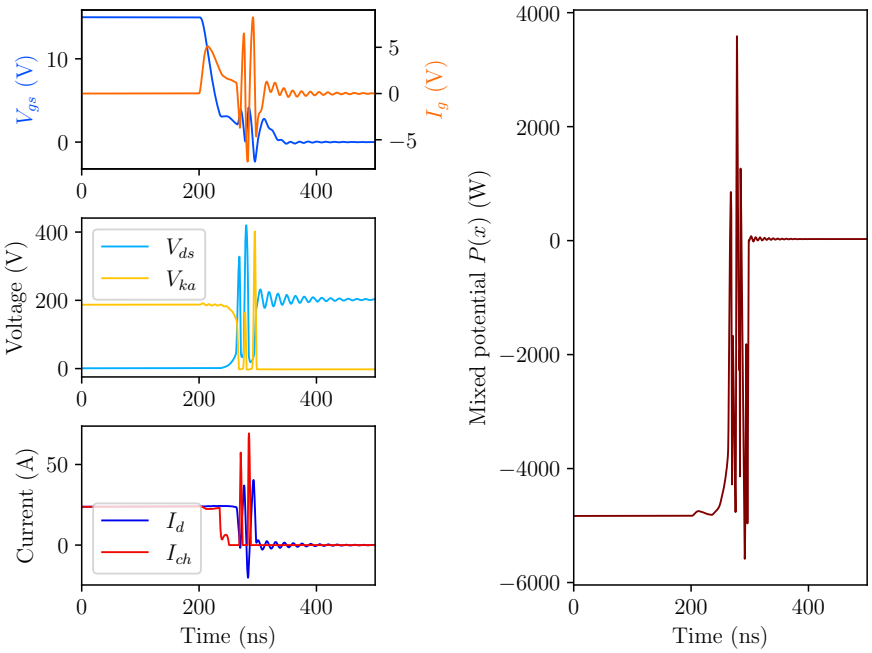


(c)

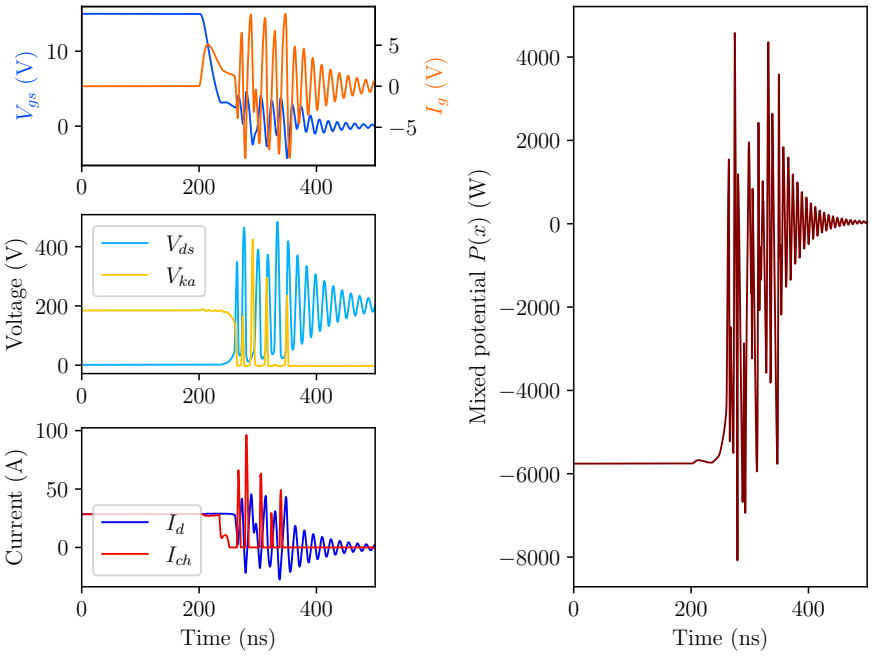


(d)

Figure 3.11: Simulated turn-off switching transient waveforms with self-turn-on phenomena and the corresponding mixed potential function with 200 V DC voltage and 2.0 Ohm gate resistance: (c) 15 A; (d) 20 A (cont.)



(e)



(f)

Figure 3.11: Simulated turn-off switching transient waveforms with self-turn-on phenomena and the corresponding mixed potential function with 200 V DC voltage and 2.0 Ohm gate resistance: (e) 25 A; (d) 30 A (cont.)

function $N(\boldsymbol{x})$. A more general stability theorem is proposed in [101], where the asymptotic stability can be then evaluated by calculating some characteristic value, the sum of infimum of the eigenvalues of some intermediate matrices $\mu_1 + \mu_2$. First let

$$K_1(\boldsymbol{i}, \boldsymbol{v}) = \frac{1}{2} A_{ii}(\boldsymbol{i}) + \frac{1}{2} \left([A_i(\boldsymbol{i}) + \gamma \boldsymbol{v}]^T L^{-1}(\boldsymbol{i}) \right)_i L(\boldsymbol{i}), \tag{3.24}$$

$$K_2(\boldsymbol{i}, \boldsymbol{v}) = \frac{1}{2} B_{vv}(\boldsymbol{v}) + \frac{1}{2} \left([B_v(\boldsymbol{v}) - \gamma^T \boldsymbol{i}]^T C^{-1}(\boldsymbol{v}) \right)_v C(\boldsymbol{v}). \tag{3.25}$$

Note the subscript here means derivative. For example, $A_{ii}(\boldsymbol{i})$ means the second-order derivative of the function $A(\boldsymbol{i})$ against the independent current vector $\boldsymbol{i}$. Let

$$K_j^s(\boldsymbol{x}) = \frac{1}{2} \left(K_j(\boldsymbol{x}) + K_j^T(\boldsymbol{x}) \right), \tag{3.26}$$

where $j = 1, 2$ denote their corresponding symmetric parts. Furthermore, also define

$$\widetilde{K}_1^s(\boldsymbol{i}, \boldsymbol{v}) = L^{-\frac{1}{2}}(\boldsymbol{i}) K_1^s(\boldsymbol{i}, \boldsymbol{v}) L^{-\frac{1}{2}}(\boldsymbol{i}), \tag{3.27}$$

$$\widetilde{K}_2^s(\boldsymbol{i}, \boldsymbol{v}) = C^{-\frac{1}{2}}(\boldsymbol{v}) K_2^s(\boldsymbol{i}, \boldsymbol{v}) C^{-\frac{1}{2}}(\boldsymbol{v}). \tag{3.28}$$

Suppose $\delta_S(x) = \{\delta_1(x), \delta_2(x), \cdots, \delta_m(x)\}$ is the set of eigenvalues for a symmetric set $S(x)$, let $\mu(S)$ denote the infimum of the eigenvalues of $S(x)$ over all x,

$$\mu(S) = \inf\{\delta(x)\}.$$

Finally, denote

$$\mu_1 = \mu(\widetilde{K}_1^s), \tag{3.29}$$

$$\mu_2 = \mu(\widetilde{K}_2^s). \tag{3.30}$$

The sufficient but not necessary condition for asymptotic stability is

$$\mu_1 + \mu_2 \geq \delta,\ \delta > 0, \tag{3.31}$$

and $P^\star(\boldsymbol{x}) \to \infty,\ \text{as}\,|\boldsymbol{x}| \to \infty$.

Note that asymptotic stability is a very "strong" stability requirement where all points around the equilibrium point are drawn toward it and will reach the equilibrium point as time goes infinity. In practice, the theorem may not suffice even though the switching transient appears normal. More discussions will be provided in the case studies below.

3.4.4 Switching transient stability criteria simplification

From previous standard form, the following first order derivatives can be easily obtained.

$$A_i(\boldsymbol{i}) = \begin{bmatrix} -V_g + R_g i_g \\ -V_d + R_d i_d \end{bmatrix}, \tag{3.32}$$

$$B_v(\boldsymbol{v}) = \begin{bmatrix} 0 \\ G_M v_{ds} \\ I_L + G_D v_{ka} \end{bmatrix}. \tag{3.33}$$

The second order derivatives can then be derived.

$$A_{ii}(\boldsymbol{i}) = \begin{bmatrix} R_g & 0 \\ 0 & R_d \end{bmatrix}, \tag{3.34}$$

$$B_{vv}(\boldsymbol{v}) = \begin{bmatrix} 0 & 0 & 0 \\ 0 & G_M & 0 \\ 0 & 0 & G_D \end{bmatrix}. \tag{3.35}$$

The interconnection matrix is given by

$$\gamma = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 1 \end{bmatrix}. \tag{3.36}$$

Furthermore, because in the switching transient $L(\boldsymbol{i}) = L$ is a constant matrix, $K_1(x)$ can be simplified,

$$K_1(\boldsymbol{i}, \boldsymbol{v}) = \frac{1}{2}A_{ii}(\boldsymbol{i}) + \frac{1}{2}([A_i(\boldsymbol{i}) + \gamma \boldsymbol{v}]^T)_i = A_{ii}(\boldsymbol{i}). \tag{3.37}$$

On the other hand, the capacitance matrix $C(\boldsymbol{v})$ is indeed voltage dependent. Therefore, $K_2(\boldsymbol{x})$ is more complex and has to be calculated numerically, which can be readily done in numerical computation software.

However, some interesting conclusions can be drawn if assuming the capacitance matrix $C(\boldsymbol{v})$ is also constant. Under this assumption,

$$K_2(\boldsymbol{i}, \boldsymbol{v}) = \frac{1}{2}B_{vv}(\boldsymbol{v}) + \frac{1}{2}([B_v(\boldsymbol{v}) - \gamma^T \boldsymbol{i}]^T)_v = B_{vv}(\boldsymbol{v}). \tag{3.38}$$

Therefore,

$$\widetilde{K}_1^s(\boldsymbol{i}, \boldsymbol{v}) = L^{-\frac{1}{2}} A_{ii}(\boldsymbol{i}) L^{-\frac{1}{2}}, \tag{3.39}$$

$$\widetilde{K}_2^s(\boldsymbol{i}, \boldsymbol{v}) = C^{-\frac{1}{2}} B_{vv}(\boldsymbol{v}) C^{-\frac{1}{2}}. \tag{3.40}$$

Unfortunately, there is no simple expression for the eigenvalues for the matrices $\widetilde{K}_1^s$ and $\widetilde{K}_2^s$. However, if $C_{gd} = 0$ and $L_s = 0$, we can clearly see that $\widetilde{K}_1^s$ and $\widetilde{K}_2^s$ are diagonal matrices whose elements are all non-negative. Therefore, if there is no feedback terms C_{gd} and L_s in the circuit, the switching transient is always asymptotically stable. This is obviously true as the gate loop and power loop are now decoupled and both loops are unconditionally stable.

3.5 Parametric Large-Signal Stability Study

Because of the complex numerical calculation required in the stability criteria and the numerous circuit elements involved in the circuit, parametric analysis is employed here to understand the effectiveness of the criteria and the root cause of the unstable switching behavior.

3.5.1 Load current and gate resistance

Fixing the common source inductance $L_s = 4.0$ nH and the DC voltage $V_d = 200$ V, the load current I_L is varied from 5 A to 30 A and the gate resistance is varied between 1.0 Ω, 2.0 Ω, 4.7 Ω and 10 Ω. The values of $\mu_1 + \mu_2$ across different cases are shown in Fig. 3.12.

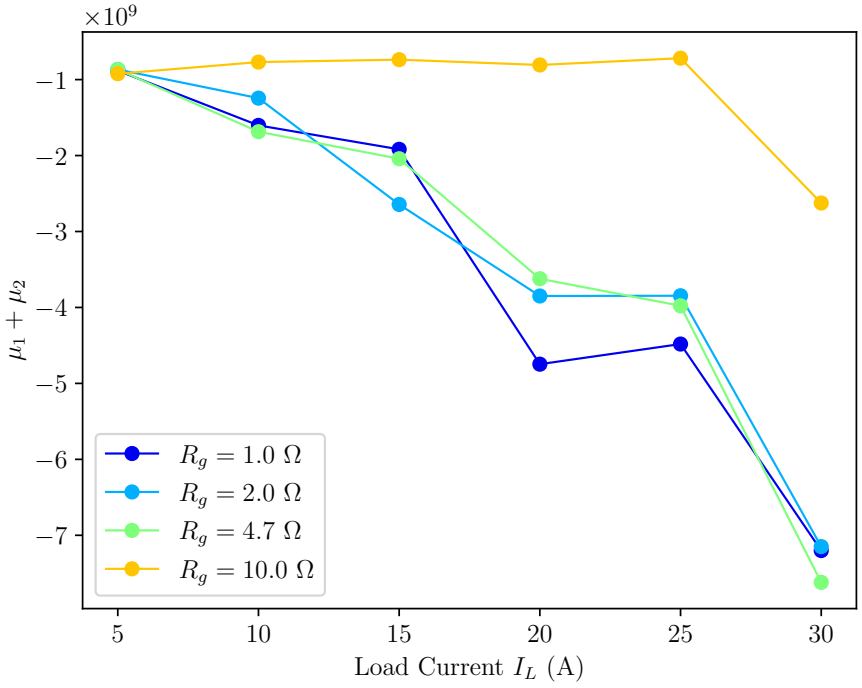


Figure 3.12: Load current I_L and gate resistance R_g impact on characteristic value $\mu_1 + \mu_2$.

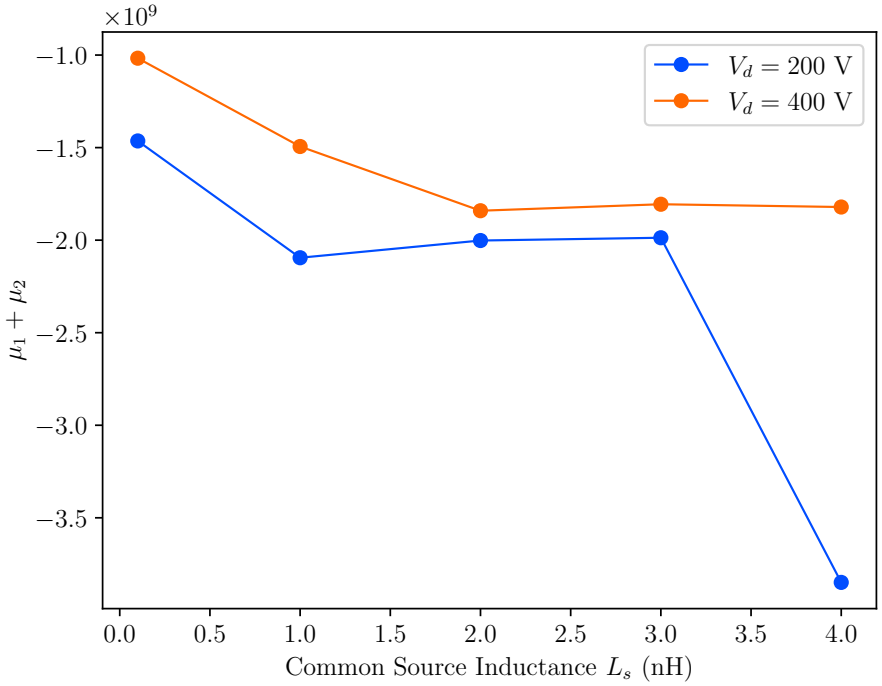


Figure 3.13: Common source inductance L_s and DC voltage V_d impact on characteristic value $\mu_1 + \mu_2$.

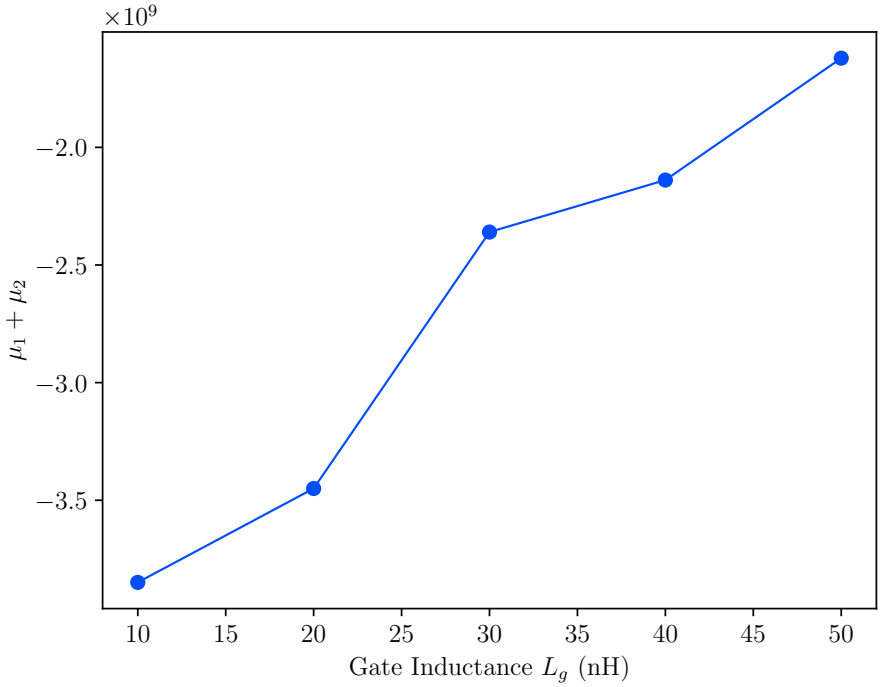


Figure 3.14: Parasitic gate inductance L_g impact on characteristic value

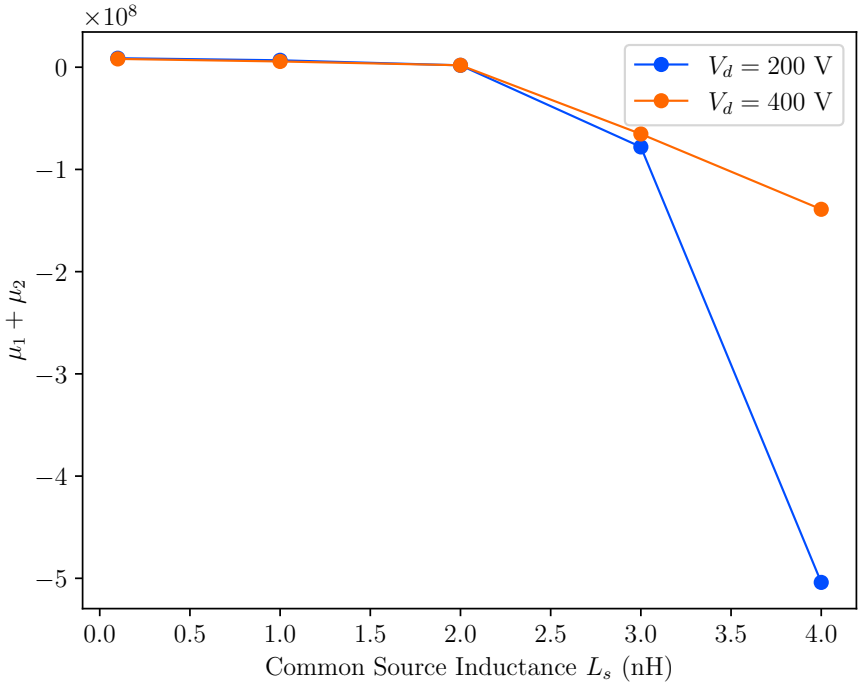


Figure 3.15: Common source inductance L_s and DC voltage V_d impact of characteristic value $\mu_1 + \mu_2$ with hypothetical capacitance from C3M0065090D.

The characteristic value $\mu_1 + \mu_2$ decreases with the increase of load current I_L, coinciding with the experimental phenomenon where the oscillation worsens with higher load current. In terms of gate resistance impact, the difference between 1.0 Ω, 2.0 Ω and 4.7 Ω is seemingly small, with either one of them showing lowest value at different load current condition. This is also in agreement with the experimental observation that the worst oscillation does not necessarily happen with the smallest gate resistance. Note that even with $R_g = 10.0$ Ω, the characteristic value $\mu_1 + \mu_2$ is still negative, although much larger than the values at other gate resistances. This indicates that the asymptotic stability criterion is not satisfied.

3.5.2 Common source inductance and DC voltage

Fixing the load current $I_L = 20$ A and the gate resistance $R_g = 2.0$ Ω, the common source inductance L_s is varied from close to 0.1 nH to 4.0 nH, while the DC voltage is varied between 200 V and 400 V. The values of $\mu_1 + \mu_2$ are again shown in Fig. 3.13.

The characteristic value $\mu_1 + \mu_2$ decreases with the increase of common source inductance L_s. This is within the expectation because previous SPICE simulation has shown the common source inductance is the critical feedback element for the oscillatory phenomenon. The value is also significantly larger at higher DC voltage V_d when the common source inductance L_s is large. This is also in accordance with the experimental results. Note that even when the common source inductance is close to 0, the characteristic value $\mu_1 + \mu_2$ is still negative.

3.5.3 Parasitic gate inductance

So far, the characteristic value is shown to indicate the severity of the self-turn-on phenomena. Therefore, it is also possible to facilitate the gate driver or circuit layout to mitigate the adverse effects. The gate resistance is kept at 2.0 Ω, the DC voltage 200 V and the load current 20 A. The sweep of characteristic value under different gate inductance L_g is shown in Fig. 3.14. As the gate inductance L_g increases, the characteristic value $\mu_1 + \mu_2$ also increases, alluding to less likelihood of instability. This is in agreement with [47] which has shown that the self-turn-on phenomena can be alleviated by increasing the gate loop inductance.

3.5.4 Parasitic capacitance voltage dependence

Note that in all previous cases, the characteristic value $\mu_1 + \mu_2$ remains negative, even when the common source inductance is close to 0. At this point, the self-turn-on phenomenon is nearly nonexistent, but the asymptotic stability criterion is still not met. This suggests that there are other factors involved in the switching transient stability. When calculating $K_2(\boldsymbol{i}, \boldsymbol{v})$, the term $([B_v(\boldsymbol{v}) - \gamma^T \boldsymbol{i}]^T C^{-1}(\boldsymbol{v}))_v$ involves calculating the derivative of $C^{-1}(\boldsymbol{v})$. This means the voltage dependence characteristics of the device parasitic capacitances also impact the large-signal stability.

To verify this observation, the IXKR47N60C5's parasitic capacitances are substituted with the capacitances from C3M0065090D, a 900 V 36 A SiC MOSFET from Wolfspeed. Other parameters including the parasitic inductances and static characteristics remain the same. The parasitic capacitance comparison is shown in Fig. 3.16. Because of the superior

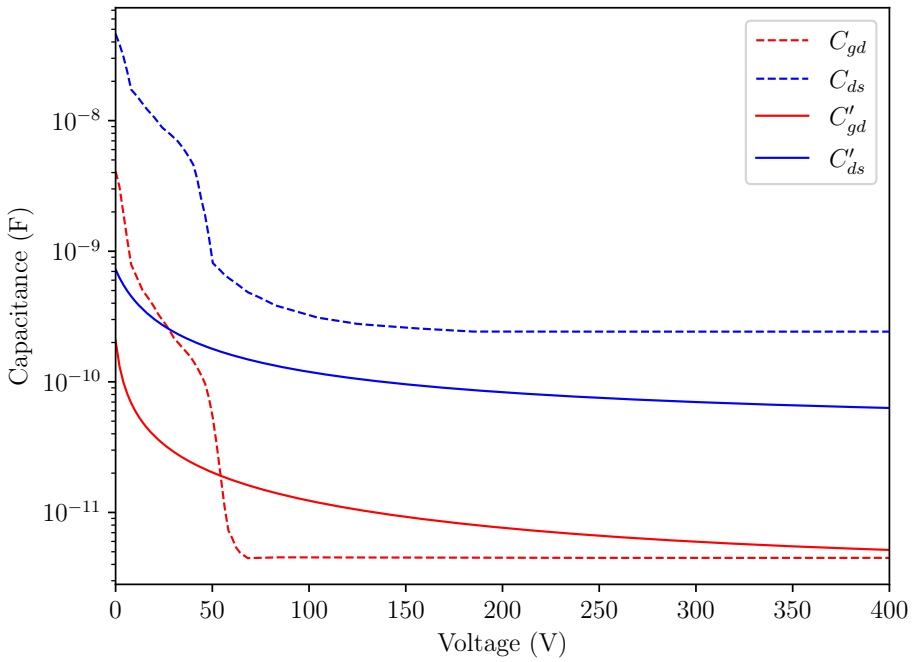


Figure 3.16: Parasitic capacitance voltage dependence comparison between IXKR47N60C5 (C_{gd}, C_{ds}, dashed) and C3M0065090D (C'_{gd}, C'_{ds}, solid).

properties of the SiC material, although the voltage and current rating of these two devices are similar, the SiC device shows even lower parasitic capacitance values.

The lower parasitic capacitance should lead to even faster switching transient voltage and current slew rate. However, as shown in Fig. 3.15, the characteristic value $\mu_1 + \mu_2$ remains positive for smaller common source inductances and only goes negative when $L_s \geq 3.0$ nH. This means the switching transient is asymptotically stable with the hypothetical capacitance from C3M0065090D. Therefore, the parasitic capacitance does indeed affect the characteristic value and the asymptotic stability.

As a summary, the characteristic value $\mu_1 + \mu_2$ can serve as an indication of the severity of abnormal oscillation during the switching transient. When it is positive, it is certain that the switching transient will be stable. However, when it is negative, the switching transient may not be completely oscillatory but the risk of abnormal ringing is high. The root cause of self-turn-on phenomenon is not only the common source inductance but also includes the unconventional voltage dependence of the parasitic capacitances. Considering the circuit model, the capacitance voltage dependence characteristics mean that as the drain-source voltage V_{ds} traverses through the rapid changing region, the channel current is dumped into the parasitic capacitances. This acts as an excitation source to the LC resonance. This is reflected in the characteristic value calculation that it involves the voltage derivative of the parasitic capacitances.

3.6 Conclusion and Discussion

The abnormal turn-off transient oscillation phenomenon, self-turn-on, is observed in experiments. The trench MOSFET channel is spuriously turned on, resulting in severe oscillation the voltage and current waveforms. In the worst case, the oscillation is sustainable and the control over the power semiconductor is completely lost. To understand the behavior and find its root cause, the phenomenon is first recreated in SPICE simulation. The high voltage and current slew rate during the switching transient results in the common source inductance charging up the gate-source capacitance. To better quantitatively predict and understand the phenomenon, large-signal based analysis with Brayton-Moser's mixed potential function is applied. The common source inductance and the unconventional voltage dependence of the device's parasitic capacitances contribute to the phenomenon. The asymptotic stability criterion is also found to be conservative and the characteristic value directly indicates the severity of the self-turn-on phenomenon. The analysis method also provides insightful suggestions on mitigation of the phenomenon.

The work here can be further improved by refining the asymptotic criterion. It is shown that the characteristic value may be negative while there may be negligible self-turn-on phenomena during the switching transient. Although the characteristic value helps understand the root cause, it is a reasonable concern that the criterion may be too stringent and unnecessary. A deeper understanding on the scope and sensitivity of the characteristic value range can provide deeper insight into the unstable switching transient.

Chapter 4

Programmable Gate Driver Platform

4.1 Introduction

Power semiconductor devices make up the heart of power electronics converters. As demonstrated in previous chapters, gate driver is the key component controlling the switching action and regulating the switching transient behavior. However, different devices may have drastically different gate driving requirements. Devices with metal-oxide-semiconductor (MOS) gate, such as silicon (Si) IGBT and MOSFET, are the most common devices today because of their easy voltage-driven characteristics. Since the advent of wide-bandgap semiconductor materials such as silicon carbide (SiC) and gallium nitride (GaN), several MOS-like devices have been reported and commercially available, including SiC junction-field-effect-transistor (JFET) [42] and GaN heterojunction-field-effect-transistor (HFET) [43]. Current driven devices such as SiC bipolar-junction-transistor (BJT) have also been actively investigated [8], [9], [44]. These drastically different devices have very diverse gate/base driving requirements, in terms of on-state or off-state voltage and continuous or transient

gate current magnitude. For example, SiC MOSFETs may require up to +20.0 V for on-state gate voltage while GaN HFETs may require only +6.0 V. Si IGBTs can often tolerate down to −20.0 V turn-off voltage but SiC MOSFETs are susceptible to gate breakdown with such low negative turn-off voltage. In terms of continuous gate current amplitude, MOSFETs and HFETs require little continuous gate current during on-state, but SiC BJTs may require up to a few amperes of continuous gate current to keep the device on.

Numerous works have also been conducted on advanced gate driving strategies. As an extension to the simplest two-level voltage source driving, three or four level driving have been demonstrated and are capable of achieving better transient performance [10], [45]. Instead of simple turn-on or turn-off gate resistors, more complex impedance network with series or parallel RLC networks have also been investigated [10], [46], [47]. Current source or resonant gate drivers are another group of driving schemes which enable the direct control of gate current during switching transients and the recovery of gating energy for high frequency applications [48]–[51]. Unlike the voltage source drivers, the device gate is directly charged or discharged by an inductor current, and the driving voltage is clamped with active switches or diodes. The current source driving concept has also been utilized for SiC BJTs to effectively reduce the base driving loss [8].

Active digital gate drivers have been proposed to fine tune the switching speed online to tackle the switching transient oscillation and EMI issues for either GaN HFET or Si IGBT [76], [77]. The driving impedance of the gate driver is adjusted dynamically by turning on or off the buffer circuits and is precisely controlled over the switching transient. This approach requires dedicated integrated circuit designs and may be difficult to translate into commercial off-the-shelf components.

A programmable driver platform is proposed here and is capable of driving all previous common power semiconductor devices, including Si IGBT, SiC MOSFET, SiC BJT and GaN HFET, with either voltage or current source driving schemes. The platform allows its user to easily adjust the gate driving performance for characterizing the devices dynamic performance. The platform can also be repurposed as a design tool for users to easily drive power semiconductor devices and optimize the gate drive design. The optimized driving schemes can then be translated into commercial components for the final design and mass production.

4.2 Programmable Driver Platform

4.2.1 Gate voltage and transient current requirement

The on-state and off-state driving voltage and the transient gate current of MOSFET and MOSFET-like devices directly determine the buffer voltage and current ratings. Common semiconductor devices, including Si and SiC MOSFET, GaN HFET, from various manufacturers are surveyed and listed in Table 4.1. For a MOSFET or MOSFET-like device, assuming the gate loop can be represented by a simple RLC circuit, the maximum transient gate current during the switching transient is given by

$$i_{g,max} = (V_c - V_e)\sqrt{\frac{C_{iss}}{L_g}} \cdot \frac{1\sqrt{\zeta^2-1}+1}{\left(2\zeta\sqrt{\zeta^2-1}+2\zeta^2-1\right)^{\frac{1}{2}+\frac{\zeta}{2\sqrt{\zeta^2-1}}}}, \tag{4.1}$$

where V_c and V_e are the turn-on and turn-off gate driving voltage, $\zeta = \frac{R_g}{2}\sqrt{\frac{C_{iss}}{L_g}}$ is the damping factor of the gate loop. Therefore, considering both the internal gate resistance $R_{g,int}$ and

the gate loop inductance, the maximum transient gate current for the devices surveyed here can be found to around 8.5 A.

In terms of the on-and off-state driving voltage, the minimum of the devices surveyed is -5 V while the maximum is 20 V. Leaving sufficient margin for both the voltage and current requirements, the switching devices in the programmable gate driver here are selected to be EPC2110 from EPC, which is a common-source-configuration bidirectional switch [103]. The voltage rating of EPC2110 is 120 V, and the continuous current rating at 25°C is 3.4 A, which is more than sufficient to drive the devices listed in Table 4.1. In fact, during the switching transient, the switches can be regarded as ideal as their on-state resistance is small (80 mΩ typical value).

Table 4.1: Power semiconductor device survey for gate driving

Part No.	V_r **(V)**	I_r **(A)**	C_{gs} **(nF)**	V_c **(V)**	V_e **(V)**	L_g **(nH)**	R_g **(Ω)**
E3M0280090D	900	11.5	0.15	15	-4	15.7	26
E3M0120090D	900	23	0.35	15	-4	15.7	16
E3M0065090D	900	35	0.66	15	-4	15.7	4.7
C3M0075120K	1200	30	1.35	15	-4	18	10.5
C3M0120100K	1000	22	0.35	15	-4	23	16
C3M0065100J	1000	35	0.66	15	-4	14	4.7
C3M0120100J	1000	22	0.35	15	-4	14	16
C3M0075120J	1200	30	1.35	15	-4	14	10.5
C3M0030090K	900	63	1.75	15	-4	18	3
C2M0045170P	1700	72	3.67	20	-5	18	1.3
C2M0080170P	1700	40	2.25	20	-5	21	2
C3M0065100K	1000	35	0.66	15	-4	15	4.7
C2M0045170D	1700	72	3.67	20	-5	25	1.3
C2M0025120D	1200	90	2.79	20	-5	25	1.1
C2M0040120D	1200	60	1.89	20	-5	25	1.8
C2M0080120D	1200	36	0.95	20	-5	24	4.6
C2M0160120D	1200	19	0.53	20	-5	24	6.5
C2M0280120D	1200	10	0.26	20	-5	24	11.4
C2M1000170D	1700	5	0.2	20	-5	24	24.8
C3M0065090D	900	36	0.66	15	-4	12	4.7

Table 4.1: continued

Part No.	V_r **(V)**	I_r **(A)**	C_{gs} **(nF)**	V_c **(V)**	V_e **(V)**	L_g **(nH)**	R_g **(Ω)**
C2M1000170J	1700	5.3	0.2	20	-5	14.5	24.8
C3M0120090D	900	23	0.36	15	-4	19	16
C3M0280090D	900	11.5	0.15	15	-4	19	26
C3M0120090J	900	22	0.35	15	-4	14.5	16
C3M0280090J	900	11.5	0.15	15	-4	13.5	26
C3M0065090J	900	11.5	0.66	15	-4	13.4	4.7
SCT10N120	1200	12	0.29	20	-5	6	8
SCT20N120	1200	20	0.65	20	-2	6	7
SCT30N120	1200	45	1.7	20	-2	6	5
SCT50N120	1200	65	1.9	20	-5	6	1.9
SCTH90N65G2V-7	650	90	3.3	18	-5	6	1
SCTW90N65G2V	650	90	3.3	18	-5	6	1
SCTWA50N120	1200	65	1.9	20	-5	6	1.9
SCTW100N65G2AG	650	100	3.6	20	0	6	1.5
SCT3105KL	1200	24	0.574	18	0	10	13
SCT2080KE	1200	40	2.08	18	0	10	6.3
SCT2160KE	1200	22	1.2	18	0	10	13.7
SCT2120AF	650	29	1.2	18	0	10	13.8
SCT2160KE	1200	22	1.2	18	0	10	13.7
SCT2280KE	1200	14	0.67	18	0	10	17

Table 4.1: continued

Part No.	V_r **(V)**	I_r **(A)**	C_{gs} **(nF)**	V_c **(V)**	V_e **(V)**	L_g **(nH)**	R_g **(Ω)**
SCT2450KE	1200	10	0.46	18	0	10	25
SCT2750NY	1700	6	0.28	18	0	10	49
SCT2H12NY	1700	4	0.18	18	0	10	64
SCT2H12NZ	1700	3.7	0.18	18	0	10	64
SCT3017AL	1700	118	2.88	18	0	10	4
SCT3022AL	1700	93	2.21	18	0	10	5
SCT3022KL	1200	95	2.88	18	0	10	4
SCT3030AL	650	70	1.53	18	0	10	7
SCT3030KL	1200	72	2.22	18	0	10	5
SCT3040KL	1200	55	1.34	18	0	10	7
SCT3060AL	650	39	0.85	18	0	10	12
SCT3080AL	650	30	0.57	18	0	10	13
SCT3080KL	1200	31	0.79	18	0	10	12
SCT3120AL	650	21	0.46	18	0	10	18
SCT3160KL	1200	17	0.4	18	0	10	18
LSIC1MO120E0080	1200	25	1.82	20	-5	10	1
LSIC1MO120E0120	1200	18	1.12	20	-5	10	0.85
LSIC1MO120E0160	1200	14	0.87	20	-5	10	0.95
LSIC1MO170E1000	1700	3.5	0.2	20	-5	10	5.8
UJ3C065080K3S	650	31	1.5	12	0	6	4.5

Table 4.1: continued

Part No.	V_r **(V)**	I_r **(A)**	C_{gs} **(nF)**	V_c **(V)**	V_e **(V)**	L_g **(nH)**	R_g **(Ω)**
UJ3C065030K3S	650	85	1.5	12	0	6	4.5
UJ3C065080B3	650	25	1.5	12	0	6	4.5
UJ3C065030B3	650	66	1.5	12	0	6	4.5
UJ3C065080T3S	650	31	1.5	12	0	6	4.5
UJ3C065030T3S	650	85	1.5	12	0	6	4.5
UJC06505K	650	36.5	1.5	12	0	6	4.5
UF3C065030K4S	650	85	1.5	12	0	6	4.5
UF3C065080K4S	650	31	1.5	12	0	6	4.5
UJ3C120080K3S	1200	33	1.5	12	0	6	4.5
UJ3C120040K3S	1200	65	1.5	12	0	6	4.5
UJC1206K	1200	38	2.2	12	0	6	1.1
UJC1210K	1200	21.5	2.2	12	0	6	1.1
UF3C120040K4S	1200	65	1.5	12	0	6	4.5
UF3C120080K4S	1200	33	1.5	12	0	6	4.5
UJ3C120150K3S	1200	18.4	0.74	15	-5	6	4.6
GS66502B	650	7.5	0.065	6	0	0	2.3
GS99504B	650	15	0.13	6	0	0	1.36
GS66506T	650	22.5	0.195	6	0	0	1.1
GS66508B	650	30	0.26	6	0	0	1.13
GS66508P	650	30	0.26	6	0	0	1.13

Table 4.1: continued

Part No.	V_r **(V)**	I_r **(A)**	C_{gs} **(nF)**	V_c **(V)**	V_e **(V)**	L_g **(nH)**	R_g **(Ω)**
GS66508T	650	30	0.26	6	0	0	1.13
GS66516B	650	60	0.52	6	0	0	0.34
GS66516T	650	60	0.52	6	0	0	0.34
GS61004B	100	45	0.295	6	0	0	0.92
GS61008P	100	90	0.59	6	0	0	0.77
GS61008T	100	90	0.59	6	0	0	0.77
EPC2040	15	3.4	0.086	5	0	0	0.5
EPC2023	30	90	2.15	5	0	0	0.3
EPC8004	40	4	0.045	5	0	0	0.34
EPC2014C	40	10	0.22	5	0	0	0.4
EPC2049	40	16	0.67	5	0	0	0.6
EPC2015C	40	53	0.98	5	0	0	0.3
EPC2030	40	48	1.96	5	0	0	0.4
EPC2024	40	90	1.92	5	0	0	0.3
EPC2035	60	1.7	0.095	5	0	0	0.5
EPC2031	60	48	1.64	5	0	0	0.4
EPC2020	60	90	1.78	5	0	0	0.3
EPC8002	65	2	0.02	5	0	0	0.3
EPC8009	65	4	0.045	5	0	0	0.3
EPC2039	80	6.8	0.21	5	0	0	0.5

Table 4.1: continued

Part No.	V_r **(V)**	I_r **(A)**	C_{gs} **(nF)**	V_c **(V)**	V_e **(V)**	L_g **(nH)**	R_g **(Ω)**
EPC2029	80	48	1.41	5	0	0	0.4
EPC2021	80	90	1.65	5	0	0	0.3
EPC2037	100	1.7	0.014	5	0	0	0.5
EPC8010	100	4	0.043	5	0	0	0.3
EPC2036	100	1.7	0.075	5	0	0	0.6
EPC2007C	100	6	0.17	5	0	0	0.4
EPC2016C	100	18	0.36	5	0	0	0.4
EPC2045	100	16	0.57	5	0	0	0.6
EPC2001C	100	36	0.77	5	0	0	0.3
EPC2032C	100	48	1.27	5	0	0	0.4
EPC2022	100	90	1.4	5	0	0	0.3
EPC2033	150	48	1.16	5	0	0	0.5
EPC2012C	200	5	0.1	5	0	0	0.6
EPC2019	200	8.5	0.2	5	0	0	0.4
EPC2046	200	6	0.285	5	0	0	0.4
EPC2010C	200	22	0.38	5	0	0	0.4
EPC2034	200	48	0.95	5	0	0	0.5
EPC2047	200	32	0.875	5	0	0	0.5
EPC2050	350	6.3	0.42	5	0	0	0.4
IPx65R280C6	650	13.8	0.95	13	0	10	12.5

Table 4.1: continued

Part No.	V_r **(V)**	I_r **(A)**	C_{gs} **(nF)**	V_c **(V)**	V_e **(V)**	L_g **(nH)**	R_g **(Ω)**
IPAW60R380CE	600	15	0.7	13	0	10	7.5
IPB60R040C7	600	73	4.37	13	0	10	0.77
IPB65R045C7	650	46	4.34	13	0	10	0.85
IPW60R017C7	600	109	9.89	13	0	10	0.45
IPW60R018CFD7	600	101	9.9	10	0	10	2.7

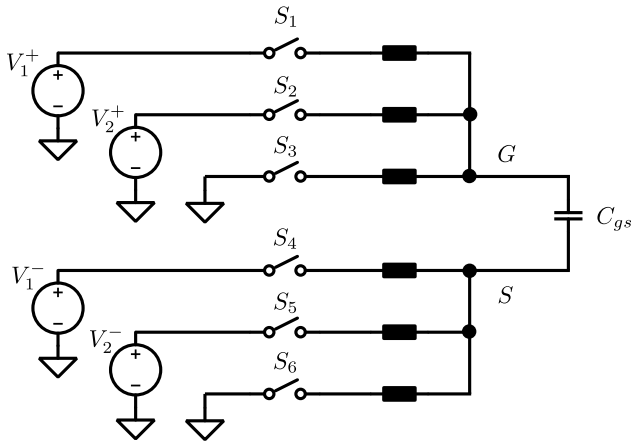
4.2.2 Voltage source driving configuration

The simplified schematic of the programmable driver platform is shown in Fig. 4.1. There are six branches in total, and each branch is made of a voltage source, a bi-directional switch and an impedance network. In particular, the #3 and #6 branches' voltage sources are ground or 0 V. In the voltage source driving configuration shown in Fig. 4.1a, there are three branches connected to the gate and source node, respectively. As an example, if S_2 and S_5 are turned on, the steady-state voltage across the gate-source capacitance C_{gs} will be $(V_2^+ - V_2^-)$. By selecting different switches from S_1, S_2, S_3 or from S_4, S_5, S_6, a total of distinctive $3 \times 3 = 9$ voltages can be achieved. Similarly, if four branches are connected to the gate node, and two remaining branches are connected to the source node, a total of $4 \times 2 = 8$ voltage levels can be achieved.

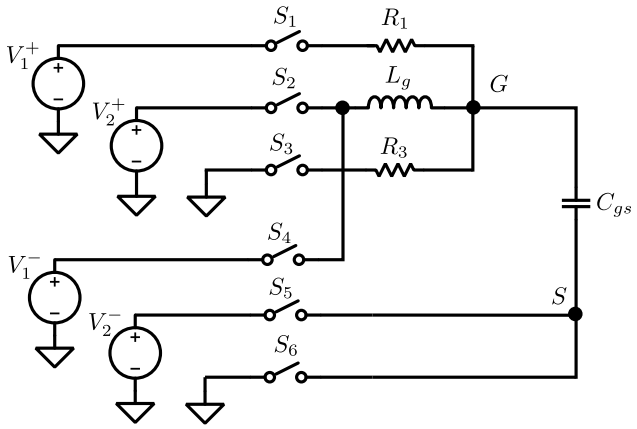
The possibility of many voltage levels and the potential shoot-through of voltage source driving structure means the switching timing of S_1 to S_6 must be well controlled. The voltage sources must be variable in a relatively large range to allow driving different devices. They also should have sufficient continuous current capability for current driven devices such as SiC BJT. More implementation details on the timing and voltage source control will be provided in a later section.

4.2.3 Current source driving configuration

The programmable driver configured as current source driver is shown in Fig. 4.1b. Four branches #1–#4 are used to control the gate inductor L_g and to direct the inductor current to charge and discharge the gate-source capacitance C_{gs}. The resistors R_1 and R_3 help limit



(a)



(b)

Figure 4.1: Simplified schematic of the programmable driver platform: (a) multi-level voltage source driving; (b) current source driving.

the inductor current. By only switching S_1 or S_3, the configuration here also provides simple voltage driving capability if the current driving scheme is not needed for either turn-on or turn-off transient. Finally, the other two branches #5 and #6 are connected directly to the source node without any impedance networks. The turn-off clamping voltage can be zero or negative by turning on S_5 or S_6.

Take the turn-on transient as an example, the typical current driving waveforms are shown in Fig. 4.2. S_3 and S_6 are in on-state prior to the switching action, and the gate-source voltage v_{gs} is clamped at 0 V. The inductor L_g is first charged by turning on S_2, and the voltage source V_2^+ starts charging the inductor current i_g. As i_g reaches desired current level I_{on}, S_3 is turned off and the inductor current is directed to charge the gate-source capacitance C_{gs}. Neglecting R_3, the time duration t_1 of L_g being charged by V_2^+ is,

$$t_1 = \frac{L_g \cdot I_{on}}{V_2^+}. \tag{4.2}$$

The voltage across L_g during t_2 when it is charging the gate-source capacitance is given by $V_2^+ - v_{gs}$. Because the total gate charge Q_g supplied during t_2 may be different for different device operating points, the time duration t_2 is usually difficult to determine without detailed semiconductor device model. As the gate-source voltage v_{gs} reaches desired on-state voltage level, S_1 is turned on and v_{gs} is clamped at V_1^+. In the meantime, S_2 is turned off and S_4 is turned on simultaneously to discharge the inductor current i_g back to 0. The voltage across the inductor is $-(V_1^+ - V_1^-)$. Neglecting R_1, the time duration of t_3 of L_g being discharged is given by,

$$t_3 = \frac{L_g \cdot I'_{on}}{V_1^+ - V_1^-}. \tag{4.3}$$

Finally, as the current in L_g discharges back to 0, S_4 is turned off and the turn-on transient finishes. As for the current source turn-off transient, it is effectively the reverse of the turn-on transient and similar analysis can be applied. Therefore, the programmable driver platform is flexible to emulate current source driving.

4.2.4 Implementation and control interface

The programmable driver platform can emulate both voltage source and current source driving schemes. Replacing the resistors in the voltage source driving configuration, the platform can also emulate various kinds of more complex impedance driving configurations. A high clock speed controller can help enable precise tuning of the switching action of S_1 to S_6 to achieve finer control of the switching transient and avoid potential shoot-through state. In the case of voltage driving in Fig. 4.1a, the variation in the duration of different voltage levels can help investigate the best driving voltage waveform. In the case of current driving in Fig. 4.1b, finer timing scale can optimize the gate current level while avoiding over-charging the inductor current i_g and the gate-source voltage v_{gs}. To enable maximum amount of flexibility in driving voltage, the voltage sources should be also variable.

The overall system implementation architecture is shown in Fig. 4.3. A graphical interface on a PC sends the various commands through UART to the FPGA, including setting the voltage sources and the switching timing for each switch S_1 to S_6. A custom high level data link control (HDLC) protocol is implemented on top of UART to decipher commands from the PC to the FPGA. The switching control implementation with FPGA is shown in Fig. 4.4. For switch S_i where $i \in \{1, 2, 3, 4, 5, 6\}$, the initial condition in the idle state can be set

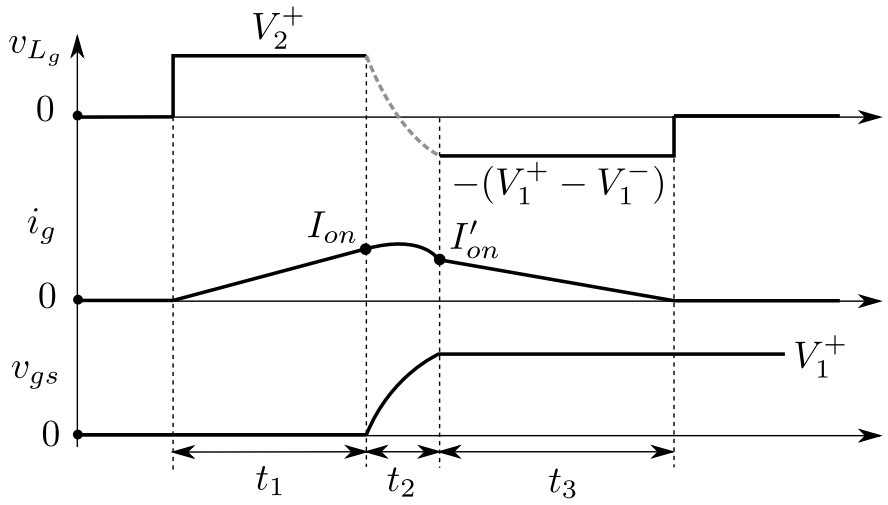


Figure 4.2: Example current source driving waveforms with programmable driver platform.

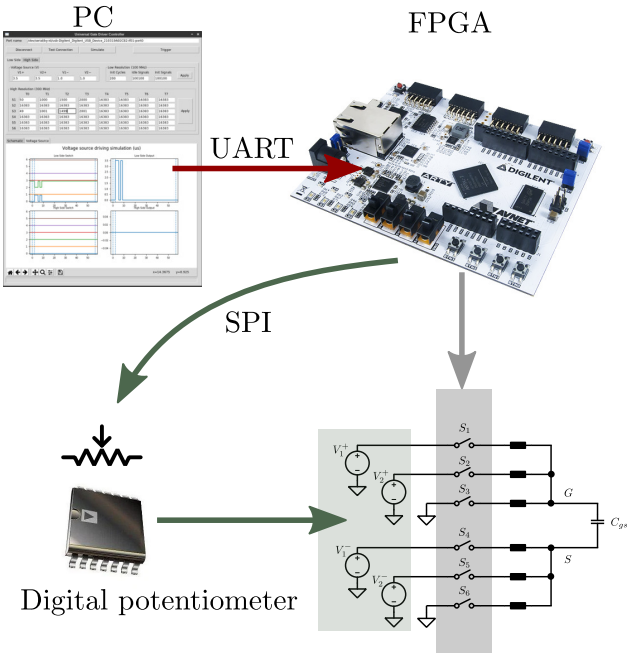


Figure 4.3: Programmable driver platform control architecture.

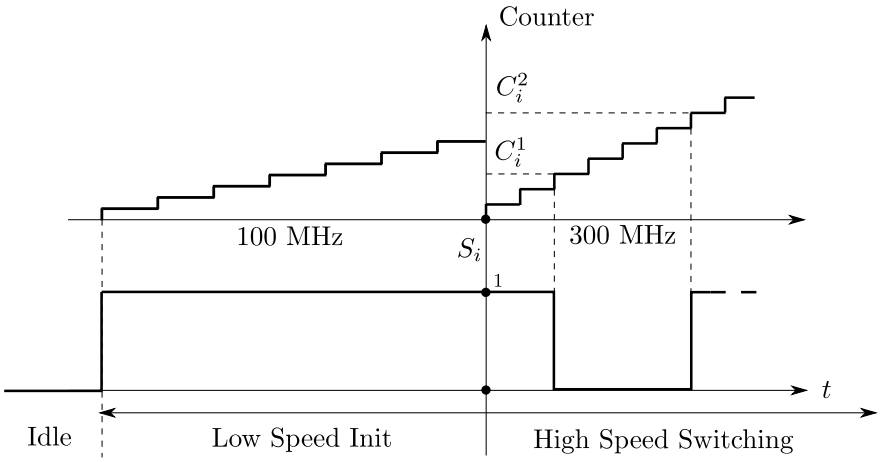


Figure 4.4: Switching timing counter implementation with FPGA.

independently. After the trigger signal from the PC is received, the 100 MHz counter clock starts first. During this "low speed init" stage, the switches can take a predefined position different from the idle condition. This allows setting a very long first pulse for double pulse test. After the 100 MHz clock reaches a designated counter value, the 300 MHz counter and the "high speed switching" starts. During this stage, whenever the high speed counter value equals to a pre-programmed counter value C_i^j, S_i is toggled. As a simple example, if after the low speed init stage, S_3 and S_6 are in on-state and the others are in off-state, the output voltage is 0 V. If S_1 and S_3 have the same predefined counter value $C_1^1 = C_3^1$, they are toggled at the same time, and the output voltage is changed to V_1^+. Typically, at least two cycle is inserted between the switching actions to avoid shoot-through. The implementation here allows up to eight 14 bits counter values which means the maximum number of switching actions is eight and the maximum duration of definable switching actions is $(2^{14} - 1)/300$ MHz $= 54.6$ μs. This provides sufficient timing length and resolution for typical double pulse test.

The voltage source control is achieved with digital potentiometers in the feedback loop of either switch-mode power supplies (Buck-Boost converter) or linear voltage regulators. The FPGA talks to the digital potentiometer through serial peripheral interface (SPI). The digital potentiometers are 10-bit, which enables up to 1024 different voltage levels for the power supplies. Finally, the hardware setup when two programmable drivers are connected to a GaN HFET phase-leg is shown in Fig. 4.5. The connection between the branches and the switching power stage is achieved with catellated vias at the printed circuit board edge, as shown in Fig. 4.6. The direct board-to-board connection helps reduce the overall gate loop inductance.

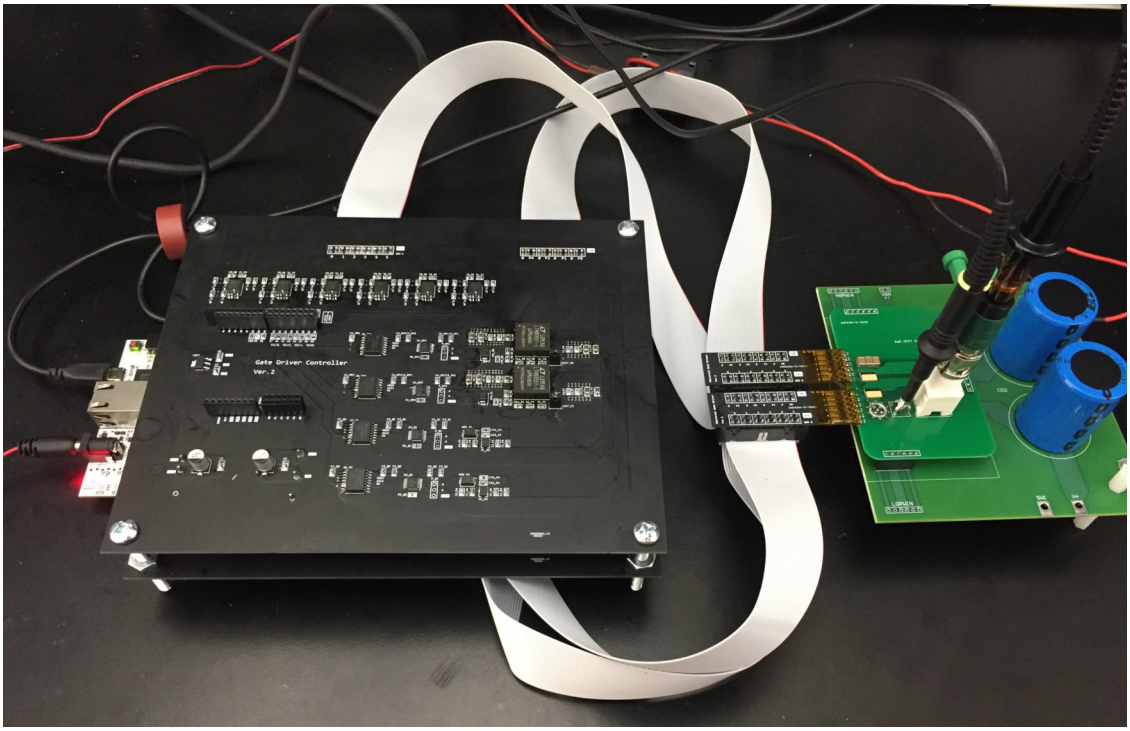


Figure 4.5: Programmable driver platform hardware setup with GaN HFETs.

Figure 4.6: Castellated vias connection between programmable driver and switching power stage.

Also note that the implementation here can be reproduced with cheaper off-the-shelf components once the driving scheme design is finished and the optimal driving strategy is found. The switches can be replaced with common gate driving buffer ICs while the timing can be achieved with FPGA, DSP, or even simple RC delay circuits.

4.3 Experimental Demonstration

As a demonstration of the flexibility offered by the programmable driver platform, several semiconductor devices are showcased here, including Si IGBT, SiC MOSFET, SiC BJT and GaN HFET.

4.3.1 Multi-level voltage driving with Si IGBT

A Si IGBT is driven with the programmable driver platform to demonstrate the basic two levels as well as the multi-level voltage driving capability. The basic timing control is also shown. The device used is the 1700 V 42 A IXBH42N170 from IXYS. The device is connected as in Fig. 4.1a. The voltage source driving waveforms are shown in Fig. 4.7.

In the multi-level voltage driving case, $V_1^+ = 20$ V, $V_1^- = 10$ V, $V_1^- = 8$ V, $V_2^- = 3$ V. The initial conditions for the switches are $\vec{S} = \{0, 0, 1, 0, 0, 1\}$. When S_3 and S_6 are turned on, the voltage across the gate-emitter terminal is 0 V. At $t = 0$, the PC sent the switching trigger signal to the FPGA, and the high resolution counter starts. During the turn-on transient of the IGBT, S_2 and S_3 are first toggled together to apply $V_2^+ = 10$ V at the gate-emitter terminal. After 150 clock cycles or 0.495 μs, S_1 and S_2 are then toggled together to output $V_1^+ = 20$ V. After another 150 clock cycles, S_5 and S_6 are then toggled together and the

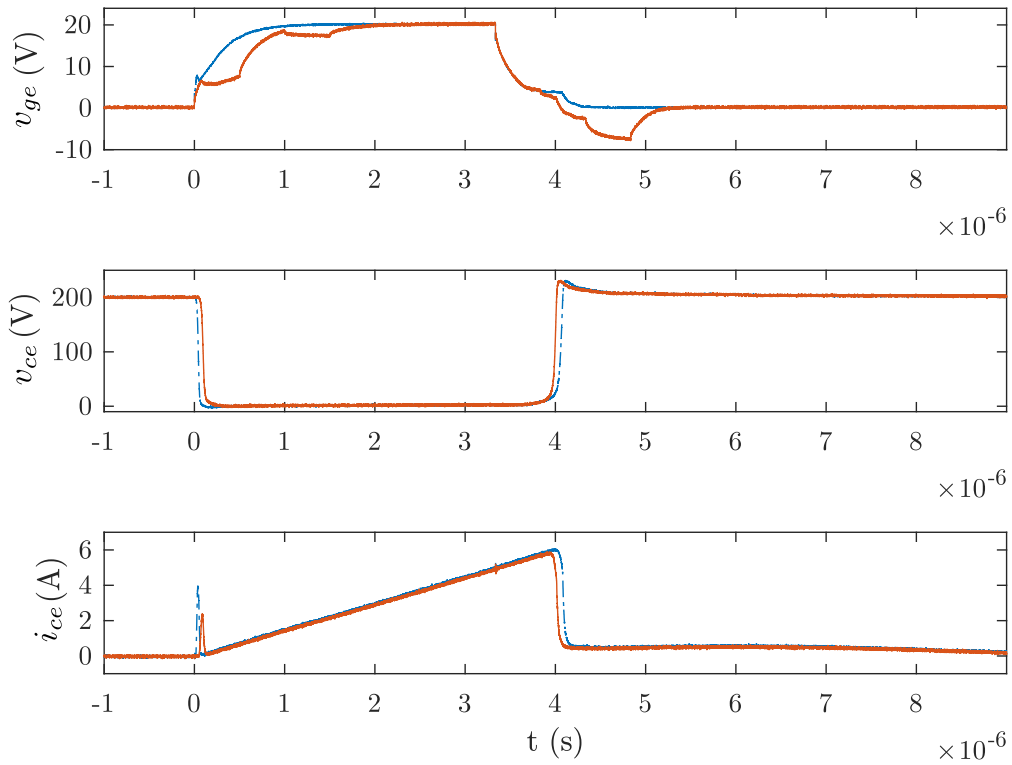


Figure 4.7: IGBT voltage source driving experimental waveforms: two level voltage driving (blue); six level voltage driving (red).

output voltage is $V_1^+ - V_2^+ = 17$ V. Finally, S_5 and S_6 are toggled again, and the output voltage is back to 20 V.

In terms of transient characteristics, by adding an intermediate voltage level of 10 V during the turn-on transient, the switching speed is effectively slowed down and the turn-on current spike is greatly reduced. Similarly in the turn-off transient, as the gate-source voltage traverses through the plateau, the gate voltage bias is reduced to -3.0 V and then to -8.0 V instead a constant 0 V. This results in a faster turn-off transient and faster voltage rise edge.

4.3.2 Variable driving voltage With SiC MOSFET

Typically, the turn-off transient in SiC MOSFETs can be quick enough that the channel is pinched off before the drain-source voltage v_{ds} drops to zero [23]. It is sometimes desirable to speed up the turn-off transient to reduce the turn-off loss. SiC MOSFET's threshold voltage is typically lower than that of Si IGBT which increases the risk of crosstalk [45]. Because of these reasons, negative driving voltage is usually applied for SiC MOSFET. As a demonstration of the programmable driver's capability to clamp the device at different voltages in off-state, the 900 V 35 A SiC MOSFET C3M0065090J from Wolfspeed is characterized here. The devices are connected as in Fig. 4.1a. The experimental comparison between 0 V and -3.5 V off-state bias using the programmable driver platform is shown in Fig. 4.8.

Compared to 0 V off-state bias, the most significant difference by using -3.5 V off-state bias is the much shorter turn-off delay time. The dv/dt and di/dt are also slightly higher in the -3.5 V case.

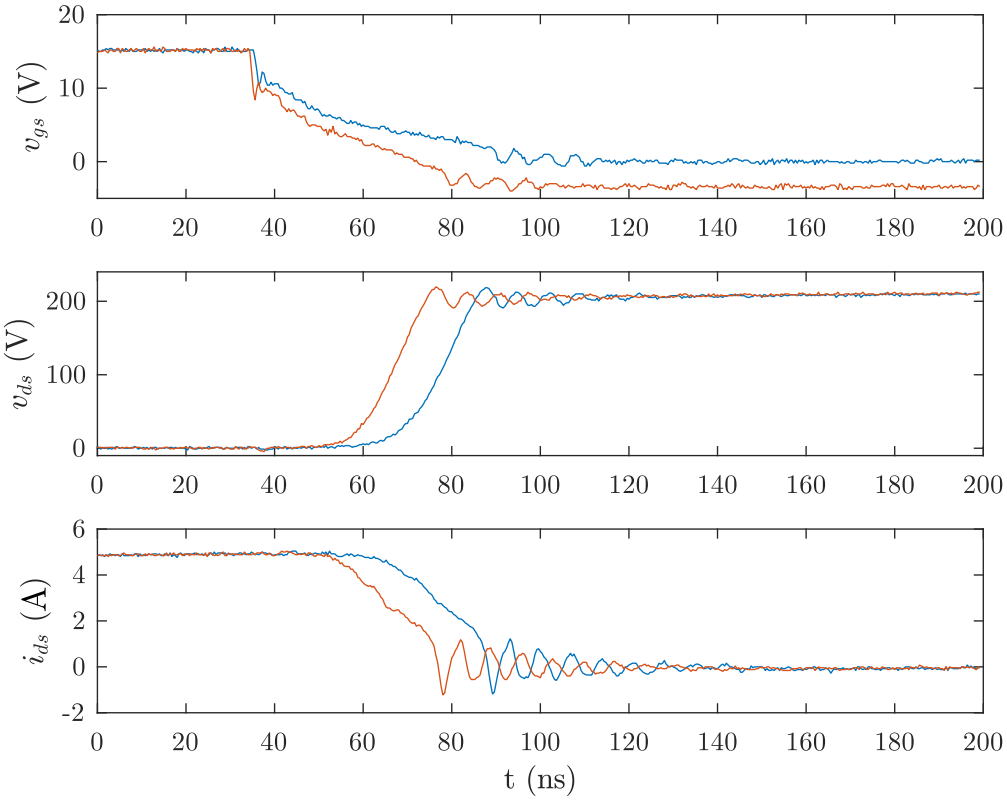


Figure 4.8: SiC MOSFET voltage source driving experimental waveforms: 0 V off-state voltage (blue); -3.5 V off-state voltage (red).

4.3.3 Impedance driving with SiC MOSFET

The SiC MOSFET is also driven with an impedance to demonstrate the impedance source driving capability. The experimental configuration is shown in Fig. 4.9. In the two-level driving case, only the first branch is used and $V_1^+ = 15.0$ V and $R_1 = 4.7\ \Omega$. In the impedance driving case, the second branch is also utilized to create an intermediate voltage level, and $V_2^+ = 19$ V, $R_2 = 2.2\ \Omega$ and $C_2 = 4.7\ \mu$F.

The experimental waveforms are shown in Fig. 4.10 Compared to the simple two-level voltage source driving, the impedance source driving slows the switching transient down and results in a lower dv/dt. However, because of the lower initial current spike, the resulting turn-on energy loss is lower than the faster two-level driving. The turn-on energy loss is reduced from 27.67 μJ to 26.42 μJ.

4.3.4 Current source turn-off with SiC BJT

Unlike the SiC MOSFET, SiC BJT is a minority carrier device which experiences charge sweep-out in the turn-off transient. This results in relatively large turn-off loss compared to a SiC MOSFET whose turn-off loss can be negligible. In this case, it is desirable to speed up the turn-off transient to achieve lower turn-off loss. The device under test here is the 1200 V 45 A SiC BJT GA20SICP12-263 from GeneSiC. The devices are connected as in Fig. 4.1b. The experimental comparison between simple two level voltage source driving and current source driving using the programmable driver platform is shown in Fig. 4.11.

The experimental result verifies the current source driving capability of the programmable driver platform. The current source driving effectively speeds up the turn-off transient by first

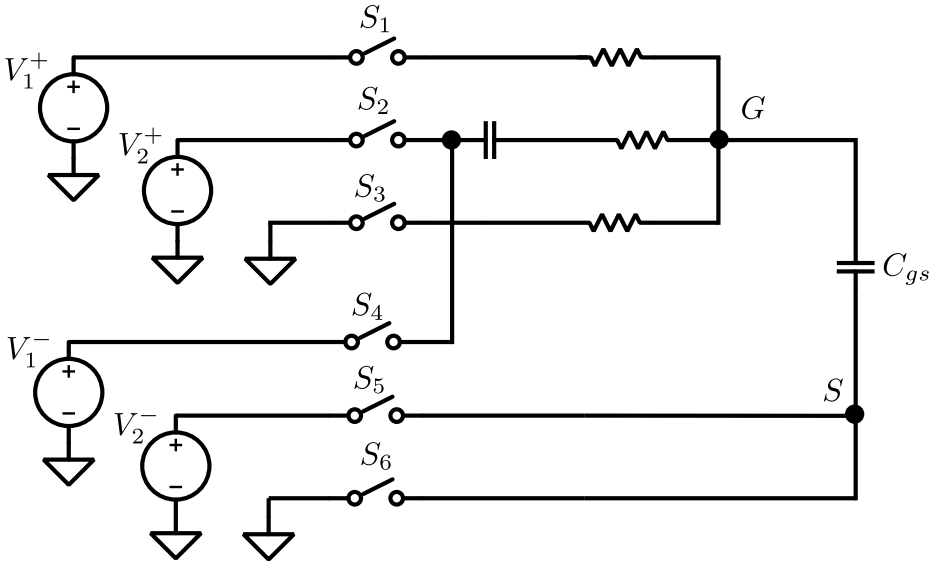


Figure 4.9: SiC MOSFET impedance driving experimental waveforms.

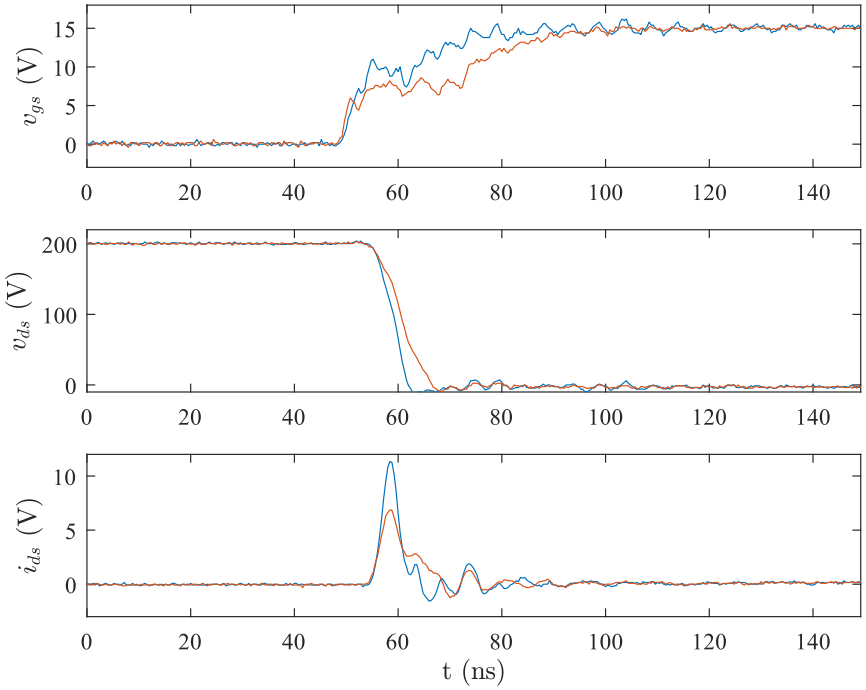


Figure 4.10: SiC MOSFET impedance driving experimental waveforms.

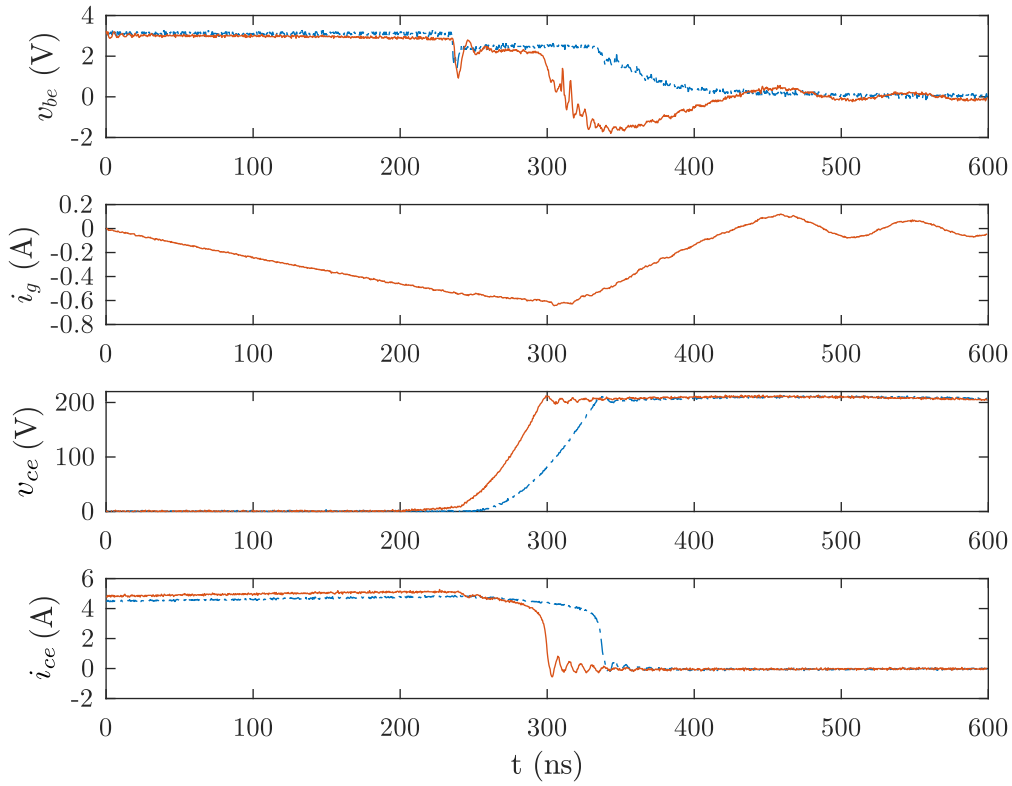


Figure 4.11: SiC BJT turn-off transient comparison: voltage source driving (blue); current source driving (red).

charging the inductor to around -0.5 A. The precharged inductor current greatly shortens the plateau region in the v_{gs} from around 100 ns in the voltage source driving case to around 60 ns in the current source driving case. The overall switching transient is reduced from around 200 ns to around 85 ns. The dv/dt and di/dt is also significantly increased which results in lower switching loss.

4.3.5 Crosstalk mitigation with GaN HFET

For high speed wide-bandgap semiconductors, crosstalk can introduce significant extra power loss during the switching transient [45]. A simple and effective method to mitigate the crosstalk is applying voltage bias when the device is in off state. Unlike MOSFET where there is a parasitic anti-parallel diode, GaN HFETs reverse conduction exhibits much higher voltage drop and on-state resistance. For GaN HFETs, negative voltage bias means very high reverse conduction loss due to its unique reverse conduction behavior.

The reverse conduction loss can be particularly detrimental for high frequency applications such as wireless power transfer. In the case of 6.78 MHz wireless power transfer application, the very high switching frequency means each switching cycle is only 147 ns. In this case, it is desirable to minimize the time duration of the negative gate voltage while avoiding crosstalk. As a demonstration of the fine timing tuning capability of the programmable driver platform, GaN HFETs GS66508T from GaN Systems are tested here. The devices are connected as shown in Fig. 4.1a.

The experimental setup is shown in Fig. 4.5. Only S_1, S_3, S_4 and S_6 are used here. The combination of S_1 and S_6 provides the on-state voltage, while the combination of S_3 and S_6

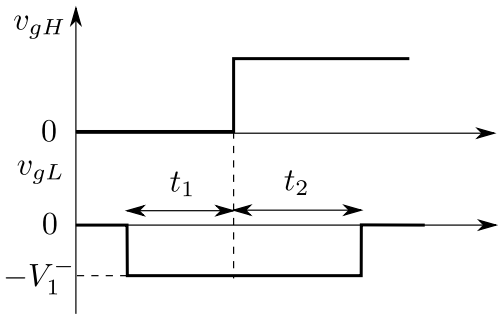
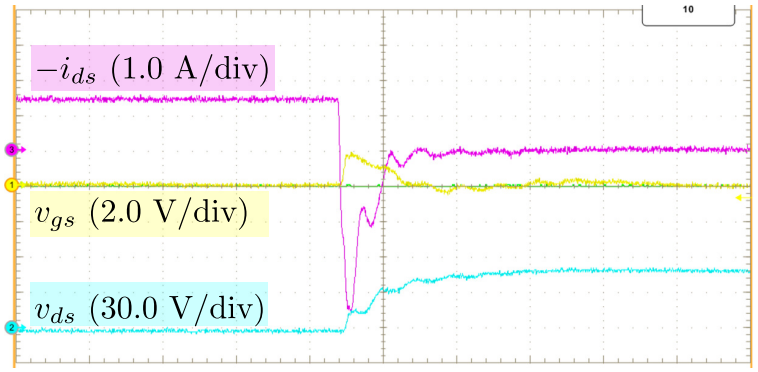
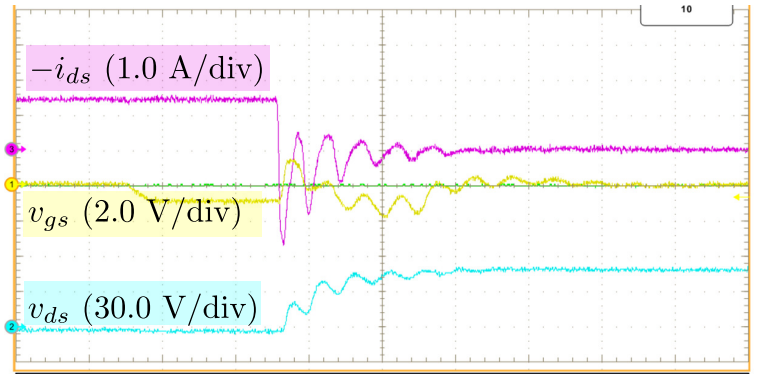


Figure 4.12: Timing diagram with programmable driver platform for GaN HFETs crosstalk mitigation.

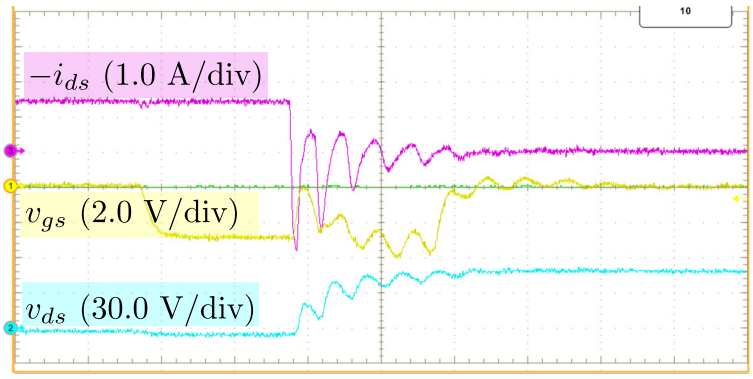


(a)

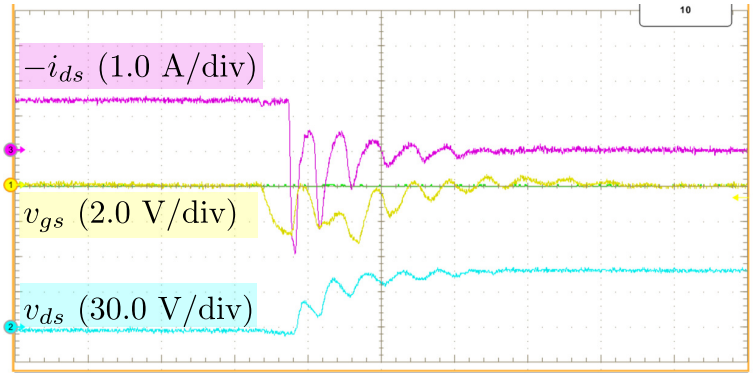


(b)

Figure 4.13: Programmable driver platform GaN HFET crosstalk mitigation: (a) 0 V; (b) -1.0 V, $t_1 = 100$ ns, $t_2 = 100$ ns.

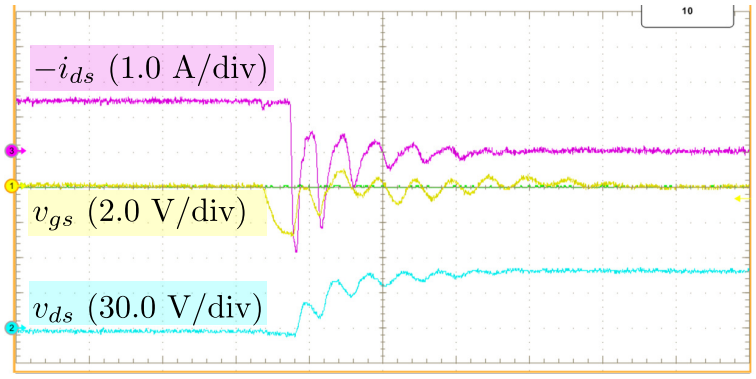


(c)

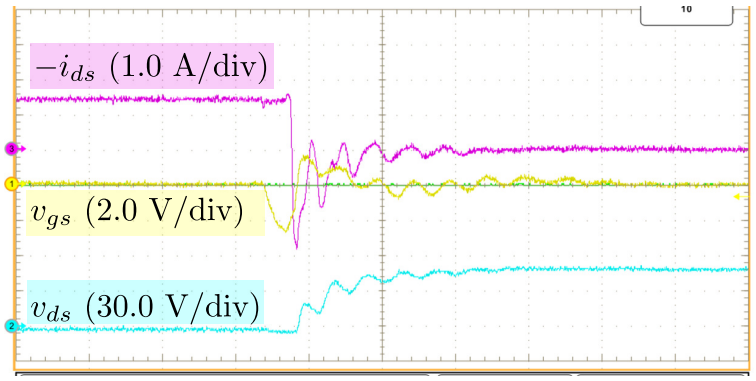


(d)

Figure 4.13: Programmable driver platform GaN HFET crosstalk mitigation: (c) -3.0 V, $t_1 = 50$ ns, $t_2 = 50$ ns; (d) -3.0 V, $t_1 = 16.5$ ns, $t_2 = 50$ ns (cont.).



(e)



(f)

Figure 4.13: Programmable driver platform GaN HFET crosstalk mitigation: (a) 0 V; (b) -1.0 V, $t_1 = 100$ ns, $t_2 = 100$ ns; (c) -3.0 V, $t_1 = 50$ ns, $t_2 = 50$ ns; (d) -3.0 V, $t_1 = 16.5$ ns, $t_2 = 50$ ns; (e) -3.0 V, $t_1 = 16.5$ ns, $t_2 = 10.0$ ns; (f) -3.0 V, $t_1 = 16.5$ ns, $t_2 = 6.6$ ns (cont.).

provides the zero voltage off-state bias. By turning on S_3 and S_4, the voltage source V_1^- is applied across the gate-source terminal which results in a negative voltage bias if $V_1^- > 0$. The voltage source $V_1^+ = 6$ V is the turn-on voltage. The voltage source V_1^- is adjusted to fine tune the off-state bias voltage.

The simplified timing diagram for the high side driving voltage v_{gH} and low side driving voltage v_{gL} is shown in Fig. 4.12. There are three variables that we would like to optimize here: (1) negative gate driving voltage $-V_1^-$, (2) negative pulse leading time t_1, and (3) lagging time t_2. Specifically, the lagging time t_2 is of particular interest because this is when the reverse conduction loss happens.

If the lower device simply uses 0 V gate voltage for turn-off, the crosstalk is quite significant as shown in Fig. 4.13a. The lower device gate-source voltage v_{gs} reaches nearly 2.0 V as the upper device turns on. The current spike is also particularly significant. When applying a -1.0 V negative voltage bias as shown in Fig. 4.13b, the crosstalk phenomena get slightly better but the gate source voltage v_{gs} still crosses over the threshold voltage of 1.1 V. When further applying a -3.0 V negative voltage bias as shown in Fig. 4.13c, the gate source voltage v_{gs} is suppressed below 0 V during upper device turn-on and the current spike is also effectively reduced. The leading and lagging time are then reduced gradually from this point. In Fig. 4.13d, the leading time t_1 is reduced to 16.5 ns without any difference in the switching waveforms. In Fig. 4.13e, the lagging time t_2 is reduced to 10.0 ns, also without inducing any crosstalk, although the gate-source voltage v_{gs} marginally crosses over 0 V. When the lagging time is further reduced to 6.6 ns as shown in Fig. 4.13f, the crosstalk phenomena came back and the gate-source voltage v_{gs} crosses over the threshold voltage and the current waveform i_{ds} exhibits distortion. In conclusion, in this case, the best combination

is $V_1^- = 3.0$ V, $t_1 = 16.5$ ns, and $t_2 = 10.0$ ns.

4.4 Conclusion and Discussion

The programmable driver platform capable of emulating both voltage source and current source driving scheme is described. Multi-level and adjustable voltage driving is demonstrated with Si IGBT and SiC MOSFET. Current source driving is showcased with SiC BJT to reduce the turn-off loss. Fine voltage level and switching timing tuning is demonstrated with GaN HFET crosstalk mitigation. The platform proves to be a useful tool for power electronics designer to quickly drive different switching devices. Given the flexibility of the programmable driver platform offers, many more driving schemes and optimization could be performed and evaluated.

Chapter 5

Switching Transient Current Measurement with Combinational Rogowski Coil

5.1 Introduction

Current measurement and monitoring technique is critical for understanding and modeling switching devices. SiC devices exhibit much faster switching capability and smaller parasitic capacitances than Si counterparts. Furthermore, recent packaging technique improvements have enabled smaller and smaller power loop inductance for SiC MOSFET modules [89], [104]. The switching transient oscillation frequency determined by the parasitic capacitance and inductance is therefore greatly increased. In order to capture the current waveform faithfully, the current sensor or probe must possess sufficiently high measurement bandwidth. Furthermore, the switching transient behavior of SiC MOSFETs is sensitive to the power loop

parasitic inductance [21]. However, threading the power loop current through a current sensor invariably results in a larger power loop area. The resulting extra power loop inductance must be kept as small as possible.

There are several high-bandwidth current measurement techniques [52]. Resistive current shunts can achieve very high bandwidth up to several GHz but are limited to non-continuous pulse operation due to heat dissipation [53], [54]. Current transformers can achieve up to 250 MHz measurement bandwidth but the cross-sectional area is quite large due to the magnetic material saturation limitation [55]. The resulting extra power loop area when routing the power loop conductor around the current transformer is therefore also large. Rogowski coils are another widely used type of current sensor based on the Faraday's induction law [56]. The helix coil directly measures the derivative of the current, which is then reconstructed by a passive or active integrating circuit [57]. The state-of-the-art commercial Rogowski coil has a small circular cross-sectional area with a diameter of 3.5 mm but the measurement bandwidth is limited to 50 MHz [58]. A Rogowski coil with up to 225 MHz bandwidth is demonstrated in [59], but numerical integration with oscilloscope is required and the sensitivity is quite low due to the low number of turns. Reference [60] proposed an integrated Rogowski coil for a GaN power stage, but the measurement bandwidth is not explicitly given.

On the other hand, the lesser-used self-integrating Rogowski coils can exhibit linear instead of differentiating output with respect to the measured current [105]. Instead of a single return turn going through the center of the coil, a layer of copper shielding covers the entire coil from outside, as shown in Fig. 5.1. In this simplified schematic, the circular helix winding is wrapped around with insulating and shielding material. The coil is terminated between one end of the winding and the shielding. The other end of the winding is connected

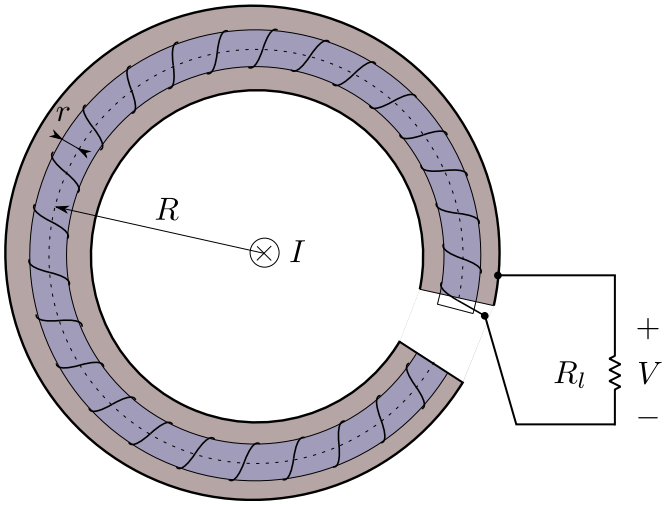


Figure 5.1: Simplified schematic of a shielded Rogowski coil.

to the shielding. The parasitic capacitance between the coil winding and the shielding can achieve passive integration in the high frequency range [57], [106], with higher bandwidth up to hundreds of MHz. However, in the aforementioned literature, the coils are quite large whose diameters are at least in tens of millimeters. Therefore, they are also not suitable for SiC MOSFET measurement.

In this paper, a combinational Rogowski coil concept is proposed, which utilizes both the self-integrating and differentiating characteristics of a shielded Rogowski coil. The measurement bandwidth is greatly increased, while the cross-sectional area is kept small to minimize the extra power loop inductance. The coil is implemented on printed circuit boards (PCB) and can be easily integrated into the switching power stage. The design methodology and practical considerations are also provided, including the parasitic element model and error analysis. Network analyzer measurements verify the measurement bandwidth of experimental prototypes can be up to 300 MHz. SiC MOSFET module double pulse tests with either standalone or integrated combinational Rogowski coil power stage further shows the coil can faithfully capture the switching transient current.

5.2 Combinational Rogowski Coil Concept

5.2.1 Shielded coil characteristics

Assuming the parasitic inductance and capacitance are evenly distributed along the coil, the equivalent distributed element circuit model for a shielded Rogowski coil is shown in Fig. 5.2. The turn-to-turn capacitance and AC winding resistance are neglected to simplify

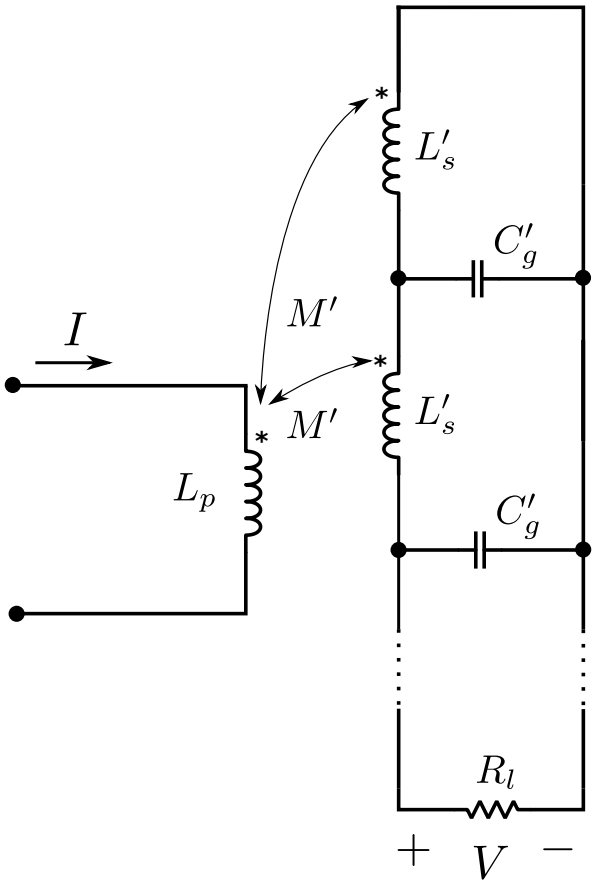


Figure 5.2: Simplified distributed element circuit model of a shielded Rogowski coil assuming all elements are evenly distributed.

the analysis. The inductance L_p represents the primary side conductor carrying the measured current. The coil is terminated with a load resistance of R_l. The coil self inductance is denoted as L_s. The winding to shielding capacitance is denoted as C_g. And the mutual inductance between the primary side conductor and the coil is denoted as M. The superscript prime represents the per-unit-length value in Fig. 5.2. The transfer impedance from the input current I and the output voltage V is given by [105]

$$Z_t = \frac{V}{I} = \frac{M}{L_s} \cdot \frac{1}{R_l^{-1} - jZ_0^{-1} \cot\left(\omega\sqrt{L_s C_g}\right)}, \tag{5.1}$$

where $Z_0 = \sqrt{\frac{L_s}{C_g}}$ is the wave impedance of the coil.

A transfer impedance example over the frequency spectrum is shown in Fig. 5.3. The transfer impedance clearly shows distinctive behaviors in different frequency regions. In the lower frequency spectrum, the coil appears differentiating. The gain increases at a rate of 20 dB/decade and the phase angle is at 90°. Inspecting (5.1), when $Z_0^{-1} \cot\left(\omega\sqrt{L_s C_g}\right) \gg R_l^{-1}$, the coil output behaves as a typical Rogowski coil,

$$Z_t \approx j\omega M. \tag{5.2}$$

From 3 MHz to 400 MHz, Fig. 5.3 shows that the coil output becomes linear. From (5.1), when $Z_0^{-1} \cot\left(\omega\sqrt{L_s C_g}\right) \ll R_l^{-1}$, the output of the coil will be proportional to the primary side current and appears linear or self-integrating,

$$Z_t \approx \frac{R_l M}{L_s}. \tag{5.3}$$

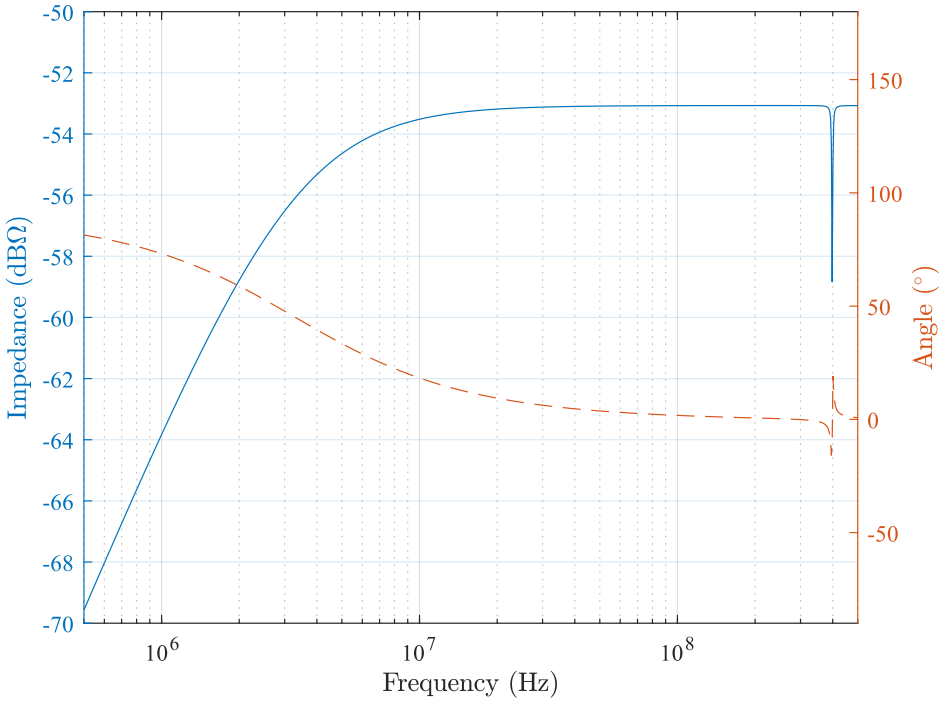


Figure 5.3: Transfer impedance of combinational Rogowski coil #1.

Because of the periodic nature of the cot function, the linear response region appears in many high frequency bands. The first frequency band immediately after the differentiating region can be used for the current sensing purpose. The primary side current signal starts being distorted at the first oscillation point, and the rest of high frequency spectrum response cannot be used to reconstruct the current signal. The lower and higher frequencies of the first self-integrating band can be found by equating the previous frequency band conditions,

$$BW_L = \frac{\arctan \frac{R_l}{Z_0}}{2\pi\sqrt{L_s C_g}}, \tag{5.4}$$

$$BW_H = \frac{\pi - \arctan \frac{R_l}{Z_0}}{2\pi\sqrt{L_s C_g}}. \tag{5.5}$$

In the example shown in Fig. 5.3, $BW_L \approx 3$ MHz and $BW_H \approx 400$ MHz. In fact, typically the coils are designed so that $BW_H \gg BW_L$ and we can leverage the self-integrating region to extend the bandwidth. Therefore, we have $\arctan \frac{R_l}{Z_0} \ll \pi$ and the bandwidth expressions can be further simplified,

$$BW_L \approx \frac{R_l}{2\pi L_s}, \tag{5.6}$$

$$BW_H \approx \frac{1}{2\sqrt{L_s C_g}}. \tag{5.7}$$

5.2.2 Combinational Rogowski coil

The combinational Rogowski coil concept here measures the current signal by utilizing both the differentiating and self-integrating region. The differentiating region below BW_L is integrated by an integrator circuit. And the self-integrating region above BW_L is directly

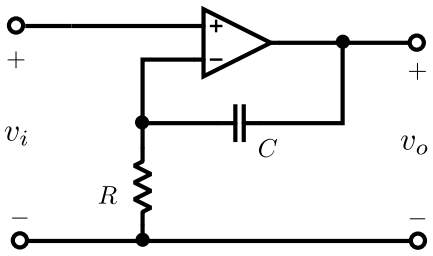


Figure 5.4: Signal processing circuit candidate for the combinational Rogowski coil.

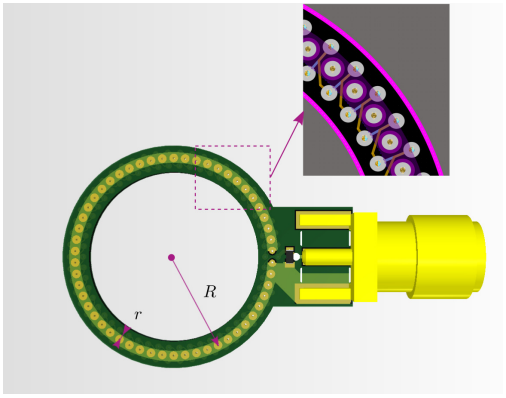
fed to the output. Corresponding to the coil behavior, the analog signal processing circuit must exactly match the transition frequency BW_L, below which it appears integrating and above which it appears linear. A possible analog signal processing circuit candidate is shown in Fig. 5.4. It is trivial to see the transfer function for this simple non-inverting integrator circuit is

$$\frac{v_o}{v_i} = 1 + \frac{1}{sRC}. \tag{5.8}$$

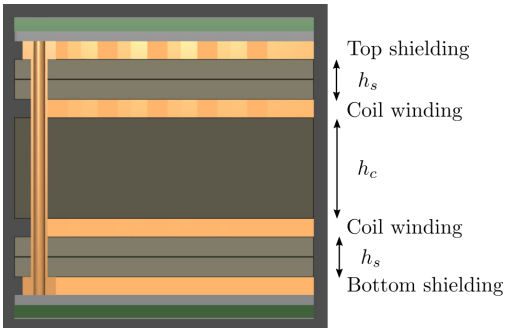
Therefore, to have a flat measured current to output voltage response, we have

$$BW_L = \frac{1}{2\pi RC}. \tag{5.9}$$

Because the integrator circuit has unity gain beyond BW_L, the overall sensor gain is clearly determined by the linear gain in the self-integrating region, as given in (5.3). From (5.3), (5.6) and (5.7), it is trivial to see that the load resistance R_l determines the overall gain and the lower self-integrating frequency. A smaller load resistance R_l means a lower gain and a lower transition frequency BW_L. The higher bandwidth BW_H, however, is only dependent on the natural oscillation frequency of the Rogowski coil. Therefore, it is beneficial to minimize the parasitic elements to achieve the highest possible BW_H. Note though, the performance of the analog signal processing circuit in (5.8) is ultimately limited by the op-amp's bandwidth. This means the overall higher bandwidth is also limited by the choice of op-amp.



(a)



(b)

Figure 5.5: Shielded Rogowski coil design example with 0.4 mm PCB: (a) PCB geometry and winding layout; (b) PCB layer stackup.

5.2.3 Coil hardware implementation

As alluded previously, it is beneficial to create a small coil for higher BW_H. The experimental prototypes are therefore built on printed circuit boards (PCB) with down to 3 mil spacing. The coil implementation approach is shown in Fig. 5.5. The coil is built on a 4-layer PCB. The helix winding is woven in the middle two layers. Blind vias between these two layers are used to connect the traces. The major and minor radius of the winding is denoted as R and r, respectively. The winding height h_c is determined by the distance between the middle layers. The top and bottom layer acts as the shielding layers. Full-stack vias are used to connect the shielding together. The insulation height h_s between the winding and shielding is again determined by the PCB stack up. The load resistance is connected directly to the winding terminal and the shielding. A SMA connector is then connected in parallel to feed the signal to the analog signal processing circuit.

5.3 Coil Models and Practical Considerations

5.3.1 Parasitic element model

Because the shielded Rogowski coil's performance is solely determined by its parasitic elements, analytical models for these elements can greatly facilitate the coil design optimization. Given the Rogowski coil shape in Fig. 5.5, the mutual inductance M_0 between the primary side conductor and the coil is given by

$$M_0 = \frac{\mu_0}{2\pi} N h_c \log \frac{R+r}{R-r}, \tag{5.10}$$

where N is the number of turns, h_c is the winding height and the same as the distance between the PCB inner layers.

The per-unit-length winding-to-shielding capacitance C'_g can be approximated by the asymmetrical stripline capacitance [107],

$$C'_g = \frac{1.10 \times 10^{-10} \epsilon_r}{\ln \frac{2(2h_s+h_c)}{0.268w+0.335t}} (\text{pF/m}), \tag{5.11}$$

where w and t are the width and thickness of the PCB winding copper trace, and ϵ_r is the relative permittivity of the PCB substrate material.

The parasitic inductance L'_s is more convoluted. Reference [105] argues there are two independent contributions of inductance which are the wire-over-ground-plane inductance L'_1 and the helix winding inductance L'_2 for circular shielded Rogowski coils. Similarly, the first part can be calculated by [107],

$$Z_s = \frac{80}{\epsilon_r} \left(1 - \frac{h_s}{4(h_s + h_c)}\right) \cdot \ln \frac{1.9(2h_s + t)}{0.8w + t}, \tag{5.12}$$

$$L'_1 = C'_g Z_s^2. \tag{5.13}$$

The second part can be written as

$$L_2 = \frac{\mu_0}{2\pi} N^2 h_c \ln \frac{R + r}{R - r}. \tag{5.14}$$

Then the self-inductance L'_s can be calculated by $L'_s = L'_1 + L'_2$. However, the assumption that these two inductances are independent and orthogonal may not be true. As the frequency

increases, the magnetic field distribution inside the coil will crowd between the winding and shielding due to the AC proximity effect. Therefore, the calculated self-inductance L_s' may be overestimating, especially in the high frequencies. This means the linear gain, transition frequency BW_L and higher frequency BW_H will all be underestimated.

5.3.2 Mutual inductance error analysis

Given the implementation approach and parasitic element model in the previous section, it is already possible to formulate an optimization problem on the coil design. However, just like conventional differentiating Rogowski coils, the mutual inductance suffer from eccentric and tilting errors because of nonuniform or sparse winding [108].

$$M = \frac{\mu_0 h_c}{2\pi} \ln\left(\frac{R+r}{R-r}\right) \sum_{i=1}^{N} \frac{\cos\theta}{\sqrt{1-\sin^2\theta\sin^2 i\alpha}\cdot\sqrt{\sin^2\theta\cos^2 i\alpha+\cos^2\theta}}. \tag{5.15}$$

$$M = \frac{\mu_0 h_c}{2\pi} \sum_{i=1}^{N} \ln\left(\frac{R^2+\Delta R^2-2R\Delta R\cos i\alpha+Rr-\Delta Rr\cos i\alpha}{R^2+\Delta R^2-2R\Delta R\cos i\alpha-Rr+\Delta Rr\cos i\alpha}\right). \tag{5.16}$$

Ideally, the primary side conductor is placed at the center of the Rogowski coil and goes through it perpendicularly to the coil plane. However, in reality, the primary side conductor can be tilted and at an angle θ against the normal of the coil plane, as shown in Fig. 5.6. The actual mutual inductance M can be found by summing the mutual inductance of each turn, and the expression is given in (5.15), where $\alpha = \frac{2\pi}{N}$ represents the spanning angle of each turn.

Assuming the major radius $R = 7.0$ mm, the minor radius $r = 0.5$ mm, and the coil height $h_c = 0.2$ mm, numerical calculation gives us the variation of mutual inductance M

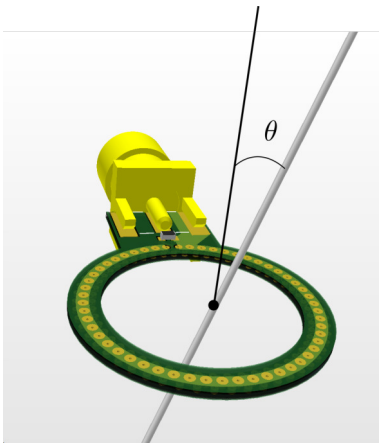


Figure 5.6: Tilted primary side conductor in Rogowski coil.

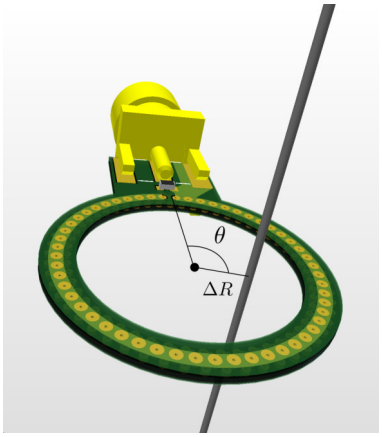


Figure 5.7: Eccentric primary side conductor in Rogowski coil.

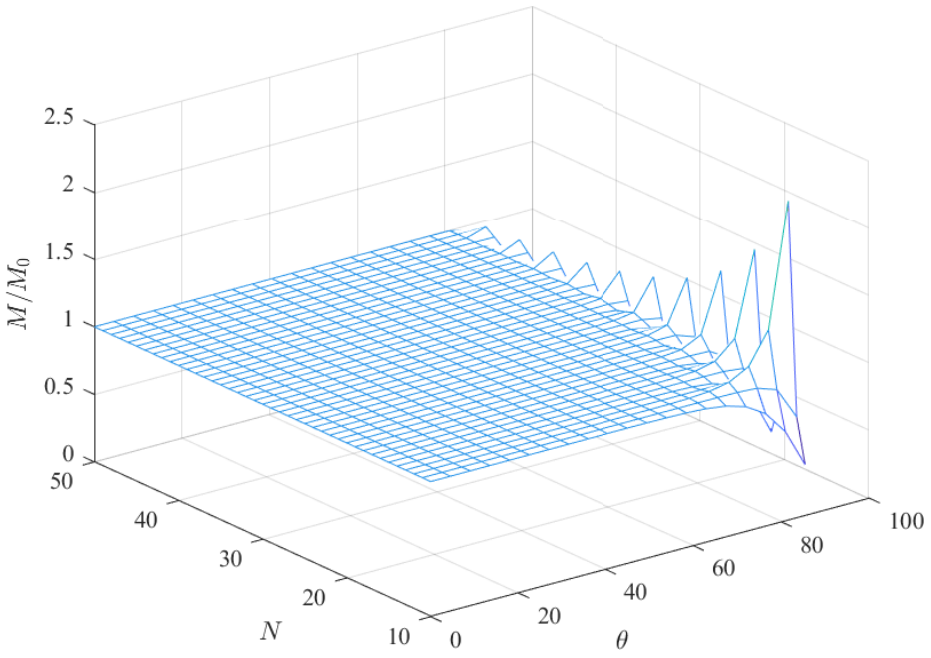


Figure 5.8: Variation of mutual inductance M when primary side conductor is tilted with different number of turns N.

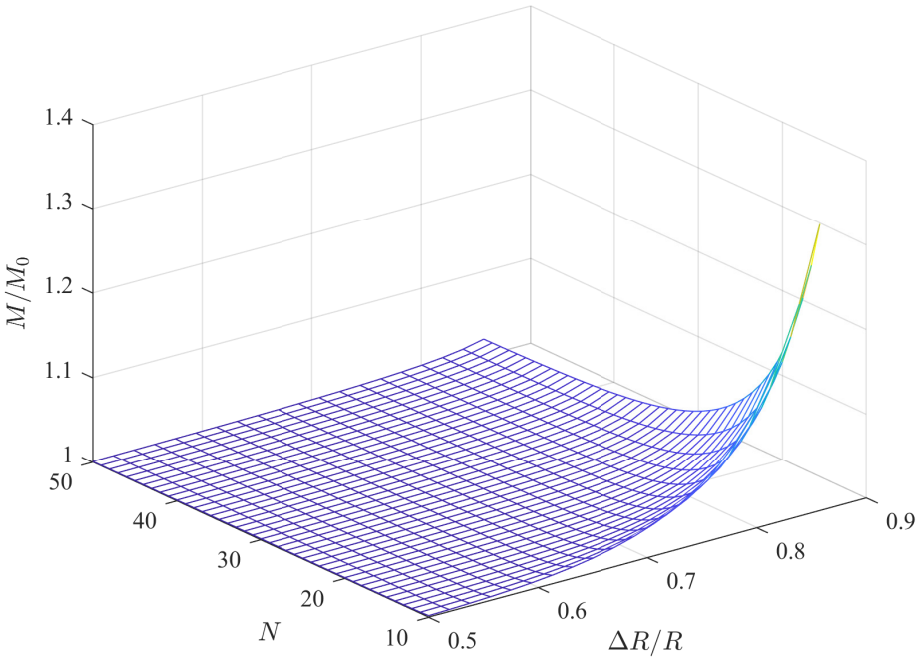


Figure 5.9: Variation of mutual inductance M when primary side conductor is eccentric with different number of turns N.

when the primary side conductor is tilted and sweeping the total number of turns N . The numerical sweeping result is shown in Fig. 5.8. When the tilting angle θ is small, there is little difference between the actual mutual inductance M and the ideal mutual inductance M_0. However, when the primary side conductor is tilted towards 90°, the change in mutual inductance is particularly significant when the number of turns N is small. This means to achieve a consistent measurement for different tilting angle, the winding density should be as dense as possible.

Another non-ideal condition is when the primary side conductor is eccentric and placed at a distance of ΔR to the center of the coil, as shown in Fig. 5.7. Likewise, the actual mutual inductance M is found by summing the mutual inductance of each turn, and the expression is given in (5.16). Similarly, having the winding as dense as possible clearly results in a more consistent measurement.

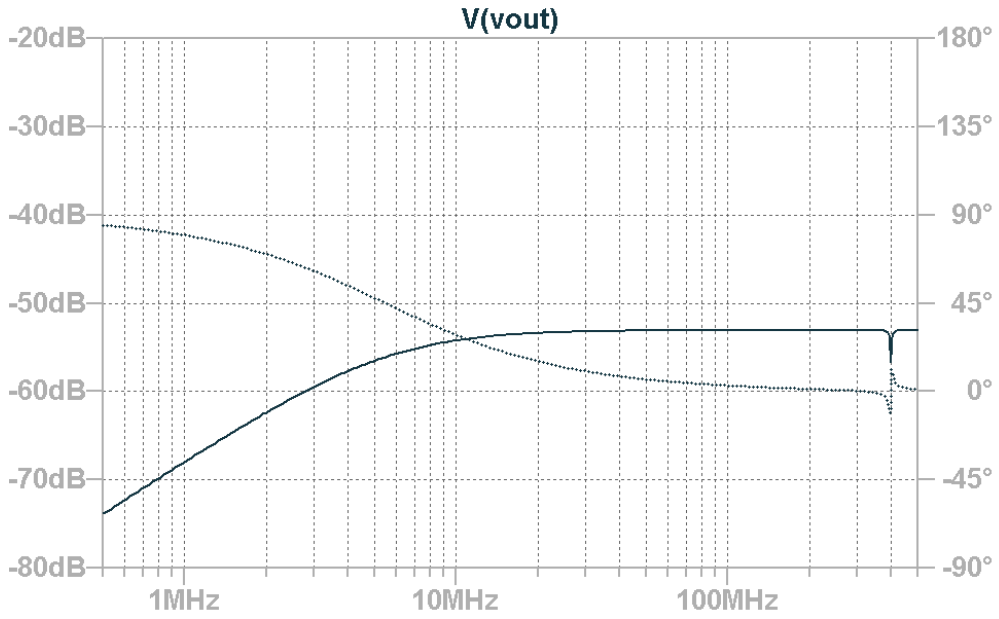
In summary, like a traditional Rogowski coil, the winding density must be sufficiently dense to ensure the mutual inductance is consistent no matter where the primary side conductor is placed. The above analysis provides a design boundary for the number of turns N. In the given example, $N > 45$ to ensure the maximum mutual inductance error is less than 5.0%.

5.3.3 High frequency behavior distortion

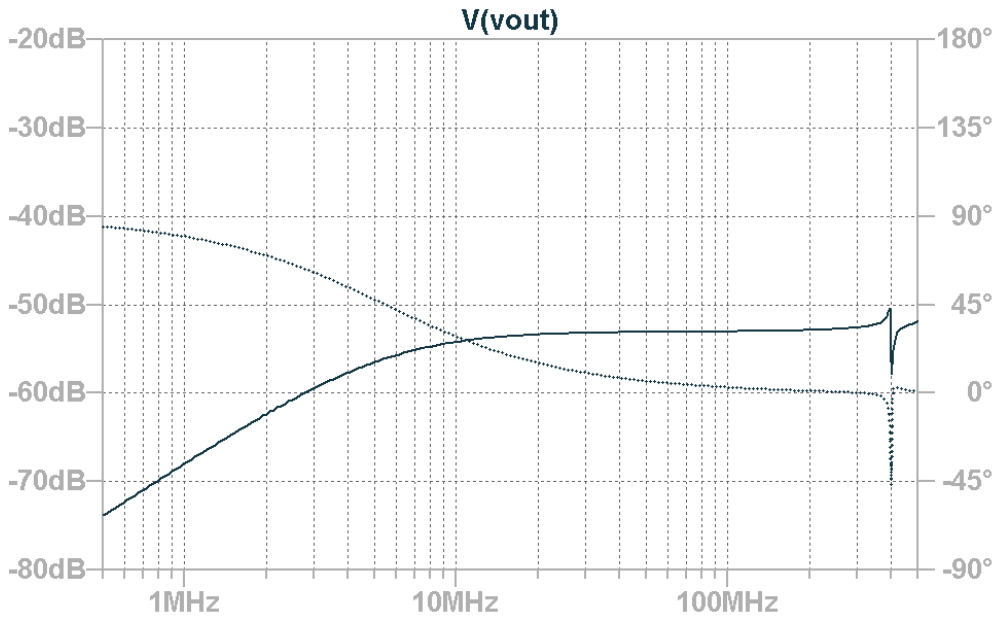
Note that in Fig. 5.2, it is assumed that each segment of the distributed circuit shares the same per-unit-length parameters. While this is true for the self-inductance L'_s and winding-to-shielding capacitance C'_g, the mutual inductance M' distribution becomes uneven when the primary side conductor is not at its ideal location. To illustrate the impact of

Table 5.1: Combinational Rogowski coil #1 parameters

Parameter	Value
No. of Turns N	54
Major Radius R	7.50 mm
Minor Radius r	0.50 mm
Coil Height h_c	0.20 mm
Shielding Height h_s	0.08 mm
Copper thickness	1.0 oz
Trace width	3.0 mil
Load Resistance R_l	0.50 Ω

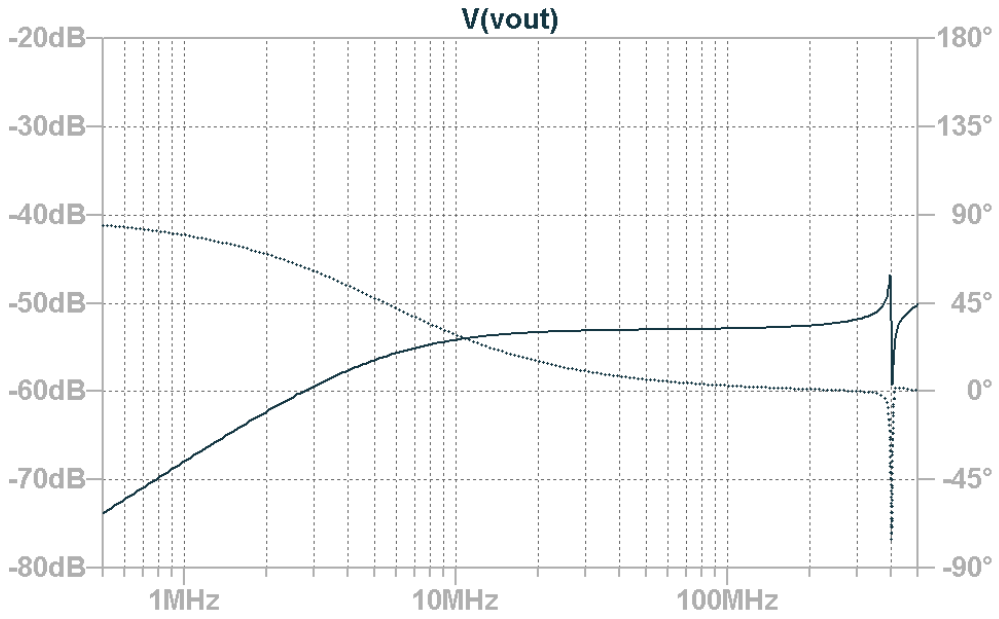


(a)

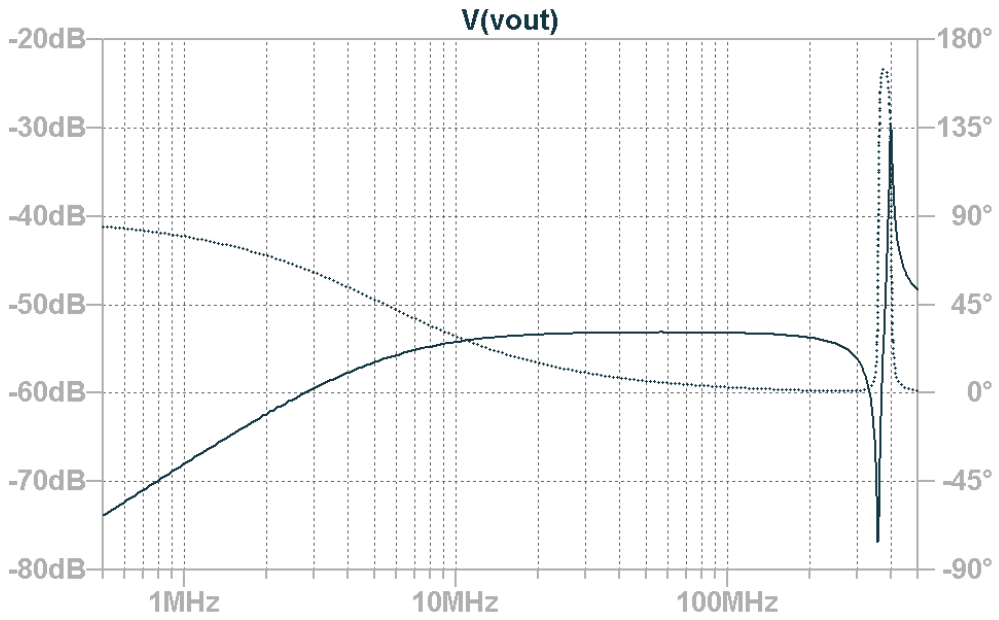


(b)

Figure 5.10: Rogowski coil eccentricity high frequency distortion: (a) $\theta = 0°, \Delta R = 0$; (b) $\theta = 180°, \Delta R = 0.3R$.



(c)



(d)

Figure 5.10: Rogowski coil eccentricity high frequency distortion: (c) $\theta = 180°, \Delta R = 0.8R$; (d) $\theta = 90°, \Delta R = 0.8R$.

uneven mutual inductance distribution, the primary side conductor is assumed eccentric here. The mutual inductance of each turn is first calculated. The distributed circuit model SPICE netlist is then automatically generated with a script, where each turn is modeled as a single segment. The parameters of the coil design used for analysis is shown in Table 5.1.

The variation in transfer impedance with different eccentric angle θ and eccentric distance ΔR is shown in Fig. 5.10. In Fig. 5.10a, the primary side conductor is placed perpendicularly at the center of the coil, the high frequency behavior is exactly the ideal case, as shown in Fig. 5.3, with higher measurement bandwidth at around 400 MHz. However, as the primary side conductor moves away from the center, as shown in Fig. 5.10b and Fig. 5.10c, where $\Delta R = 0.3R$ and $\Delta R = 0.8R$ respectively, the high frequency behavior becomes distorted. The distortion appears most significant when the primary side conductor is placed at $\theta = 90°$ with respect to the terminal of the coil. As shown in Fig. 5.10d, when $\Delta R = 0.8R$, the distortion at the first resonance is a lot more severe and the usable measurement bandwidth ($\pm$3 dB) is reduced to around 300 MHz.

The analysis here clearly shows the high frequency behavior is also subject to variation when the primary side conductor is not at its ideal location. This means the actual usable bandwidth is lower than the designed value, and enough bandwidth margin must be kept to ensure the final bandwidth is sufficient. On the other hand, it also suggests that if applicable, the primary side conductor should be located ideally at the dead center of the coil. It is later shown that it is trivial to do so when embedding the coil in the switching power stage. Finally, this also means the coil winding must be evenly distributed, otherwise the unevenly distributed mutual inductance would distort the high frequency behavior.

5.4 Coil Designs and Performance Verification

5.4.1 Coil high frequency performance measurement

Two experimental prototypes are built and tested. The first prototype coil #1 is shown in Fig. 5.3 and Table 5.1. The sensitivity or gain is around -53.0 dBΩ or 2.2 mΩ, which is more suitable for higher current measurement. The second prototype coil #2 is shown in Fig. 5.11 and Table 5.2. The sensitivity is around -36.3 dBΩ or 15.3 mΩ. Compared to coil #1, #2 is much smaller with a major radius of only 2.0 mm. The upper measurement bandwidth according to the model is also a lot higher, beyond 500 MHz. Therefore, #2 is more suitable to measuring lower current devices.

Both prototypes are show in Fig. 5.12. The coil #2 is very small, with the whole coil smaller than the SMA connector. The measurement setup is also illustrated with the coil #2. An SMA cable is striped near its end and the center conductor is bent to create a small loop and shorted to the external ground shielding. The small loop is wrapped around the coil to act as the primary side conductor. The shorted cable is connected to the port 1 of a network analyzer and the coil output is connected to the port 2. The network analyzer used here is the Keysight E5061B, sweeping from 500 kHz to 500 MHz. The transfer impedance Z_t can be obtained by converting from the S-parameter measurement result,

$$Z_t = \frac{2S_{12}}{(1-S_{11})(1-S_{22}) - S_{12}S_{21}} Z_o, \tag{5.17}$$

where $Z_o = 50\ \Omega$.

The measurement results of both coils are shown in Fig. 5.13. Note that the measurement

Table 5.2: Combinational Rogowski coil #2 parameters

Parameter	Value
No. of Turns N	20
Major Radius R	2.00 mm
Minor Radius r	0.50 mm
Coil Height h_c	0.80 mm
Shielding Height h_s	0.11 mm
Copper thickness	1.0 oz
Trace width	3.0 mil
Load Resistance R_l	0.50 Ω

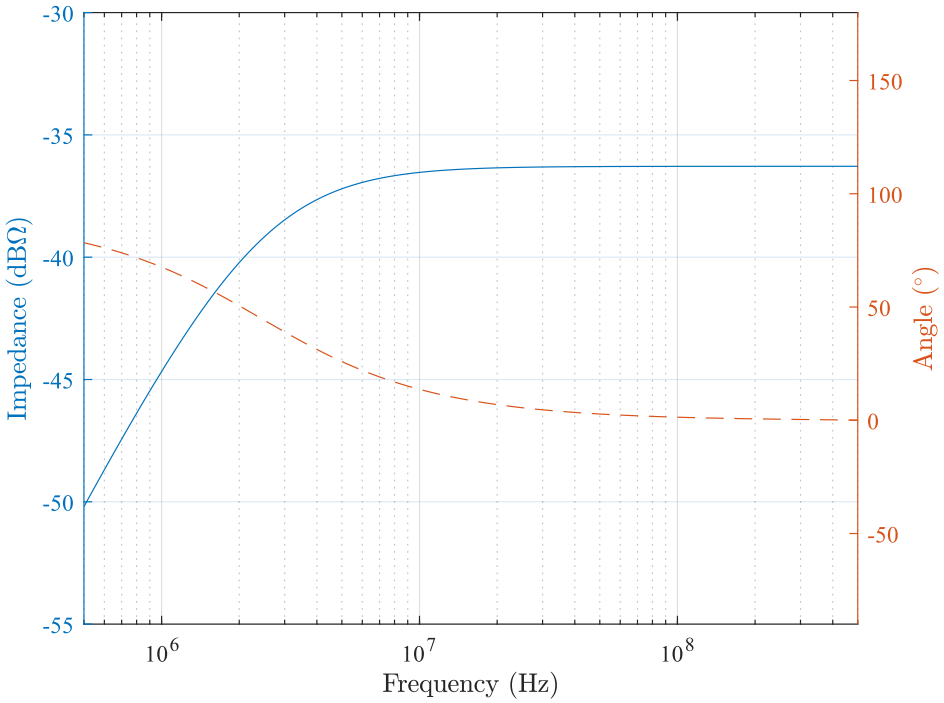
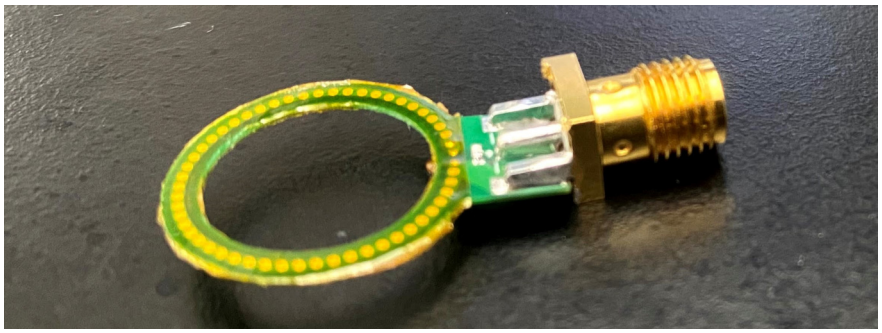
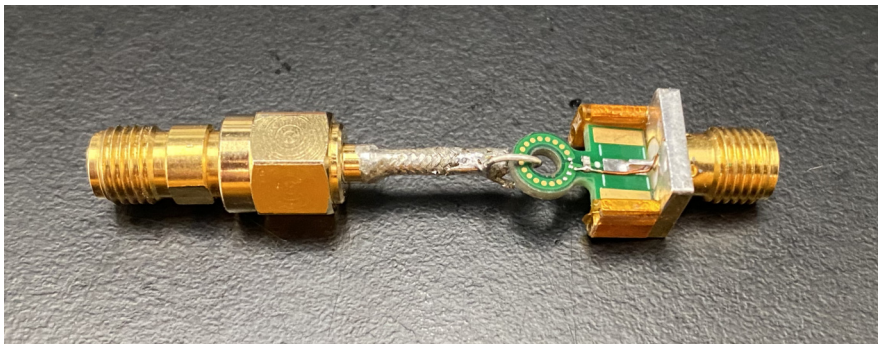


Figure 5.11: Transfer impedance of combinational Rogowski coil #2.

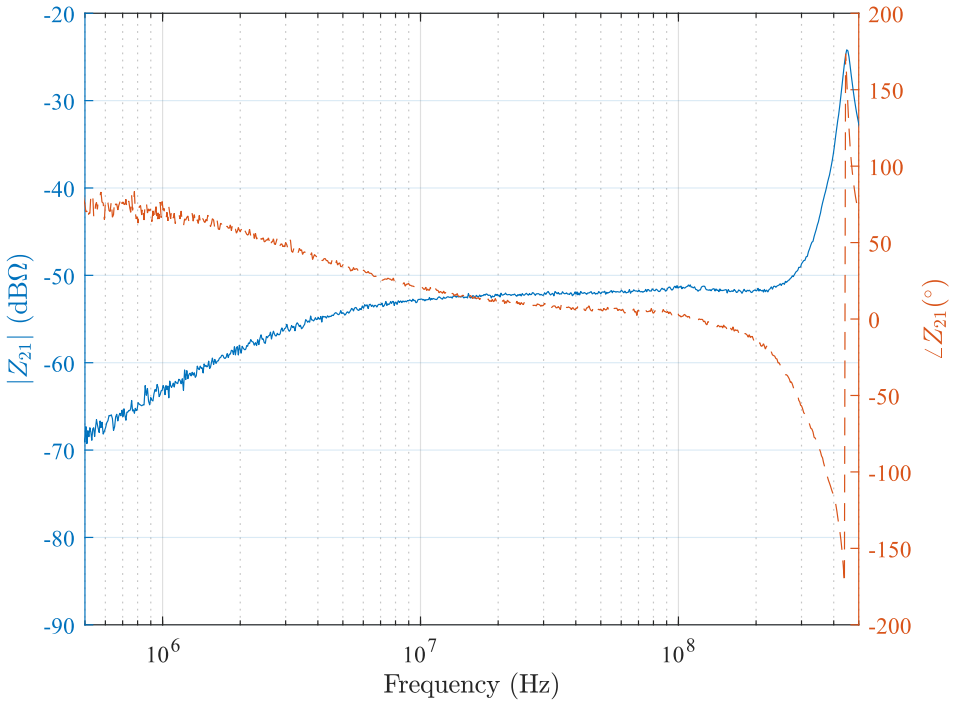


(a)

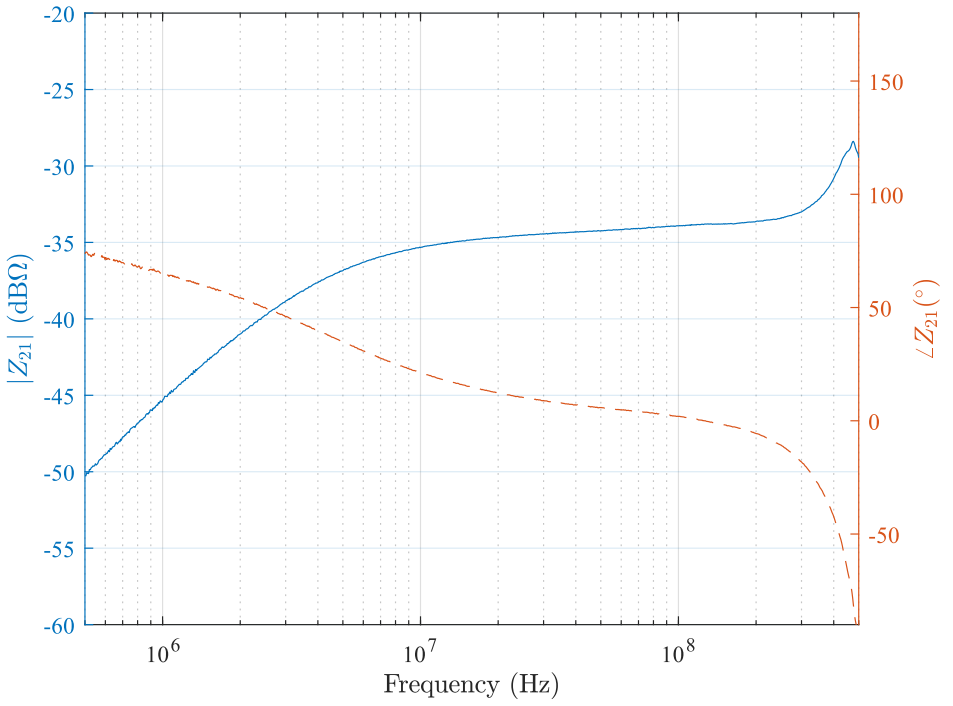


(b)

Figure 5.12: Combinational Rogowski coil prototypes: (a) coil #1 built on 0.40 mm PCB; (b) coil #2 built on 1.20 mm PCB.



(a)



(b)

Figure 5.13: Combinational Rogowski coil prototypes high frequency network analyzer measurement result: (a) coil #1; (b) coil #2.

setup is essentially the worst case for the mutual inductance uneven distribution. The primary side conductor loop has the strongest possible coupling with the turn it immediately encircled. As expected, the high frequency distortion is quite significant in both coils. Nevertheless, the usable measurement bandwidth (±3 dB) for coil #1 is around 300 MHz and for coil #2 is around 382 MHz. The measurement result of coil #1 also appears more noisy. This is because the gain of the coil is much lower than coil #2. The high frequency response is not completely flat for both coils, which is probably because of the high frequency AC resistance impact. Comparing the measurement result to the model prediction in Fig. 5.3 and Fig. 5.11, both the transition frequency BW_L and the gain Z_t are higher than the model. Like previously discussed, this is expected since the self-inductance L'_s calculation tends to overestimate its value.

5.4.2 Overall behavior with analog signal processing circuit

The analog signal processing circuit is implemented with LTC6228, which has a rail-to-rail output. The power supply for the op-amp is ±5.0 V. As an example, the overall performance of coil #2 is shown with the integrator circuit. The high frequency response is measured in the same way as with the coil high frequency response. The primary side conductor made from the SMA cable short loop is connected to port 1. The Rogowski coil is connected with the integrator input terminal, and the integrator output is directly fed to the port 2 of network analyzer. The measurement result is shown in Fig. 5.14. The op-amp circuit further created some high frequency distortion, and its high frequency response is not particularly flat and the overall measurement bandwidth is reduced to around 300 MHz. Also note that at

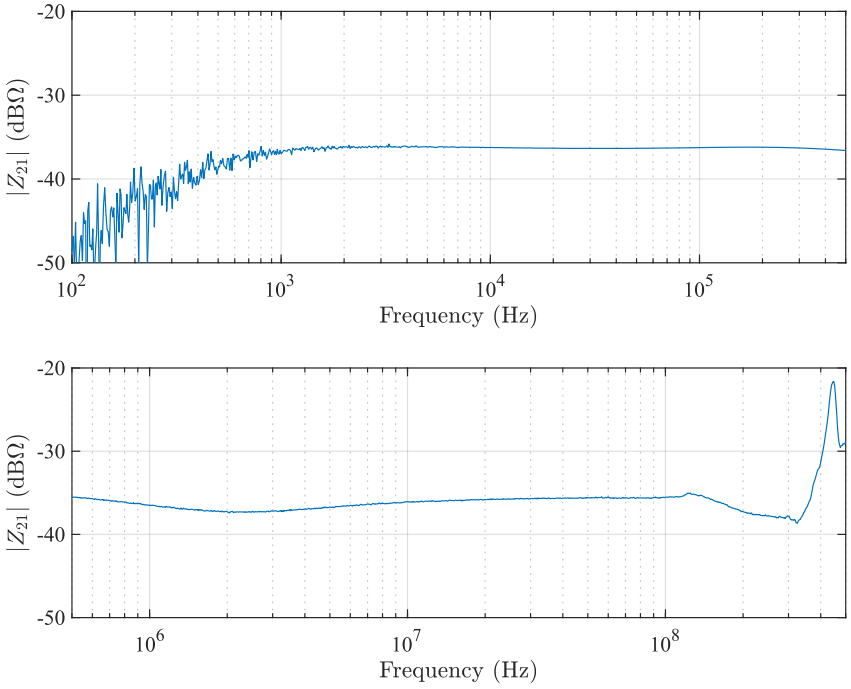


Figure 5.14: Low and high frequency transfer impedance measurement with coil #2 and signal processing circuit.

around the transition frequency of around 4 MHz, the gain is not very flat. This is likely due to the integrator circuit component mismatch. Nevertheless, the concept here is verified and the integrator circuit directly outputs the high frequency components of the Rogowski coil.

The lower frequency response between 100 Hz to 500 kHz is measured with the gain/phase measurement on the Keysight E5061B. The measurement result is also shown in Fig. 5.14. The sensor exhibits a very flat response from around 400 Hz all the way to 500 kHz. Therefore, the analog signal processing circuit works as intended, integrating all the low frequency components. The measurement below 1 kHz is particularly noisy, though, likely because of the op-amp circuit intrinsic noise.

5.4.3 Double pulse test with standalone coil

The coil #1 is tested in a standalone fashion, and the test setup is with SiC MOSFET module CAS325M12HM2 which is rated at 1200 V and 400 A. As a comparison between the commercial current probe TCP0030A (50 A, 120 MHz) and the Rogowski coil, the measurement setup deliberately created a large loop in the switching power loop, as shown in Fig. 5.15. The Rogowski coil is hidden under the current probe.

Because of the large power loop and the limited 50 A maximum current capability of TCP0030A, the double pulse test was performed at relatively low voltage and current. The waveform comparison is shown in Fig. 5.16. Because of the relatively low current and the low sensitivity of coil #1, the measurement noise is relatively significant in the Rogowski coil. The turn-on transient comparison between them shows nearly the same measurement result in the rising edge and the oscillation afterwards. Therefore, it is proved the combinational

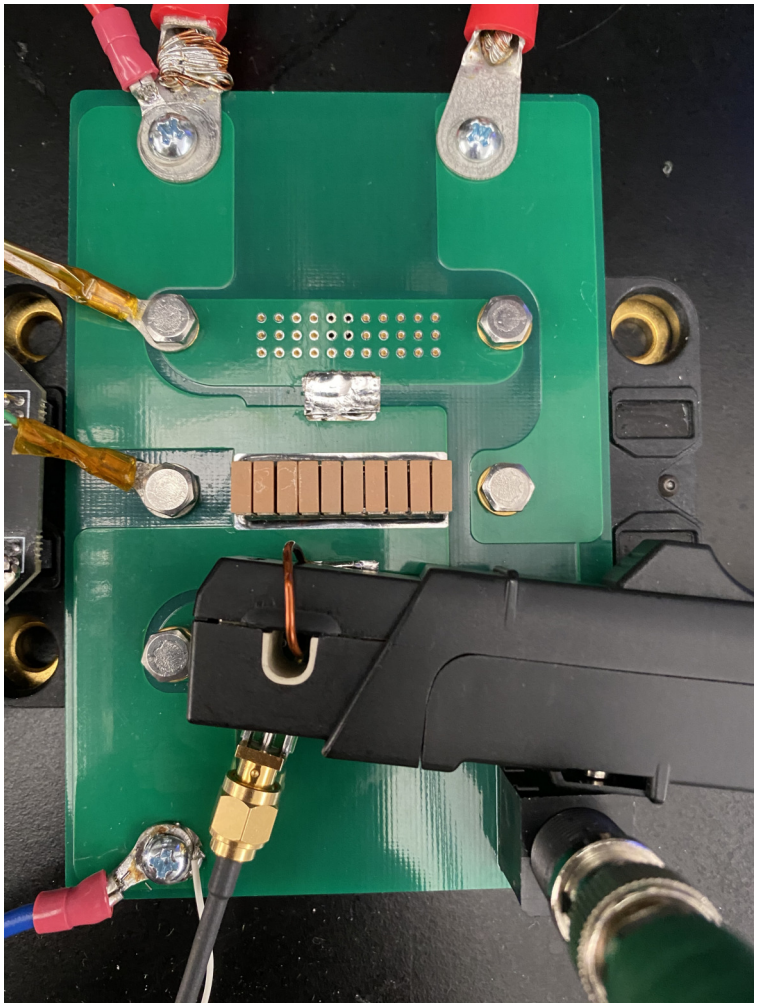


Figure 5.15: Standalone Rogowski coil double pulse test comparison with commercial current probe.

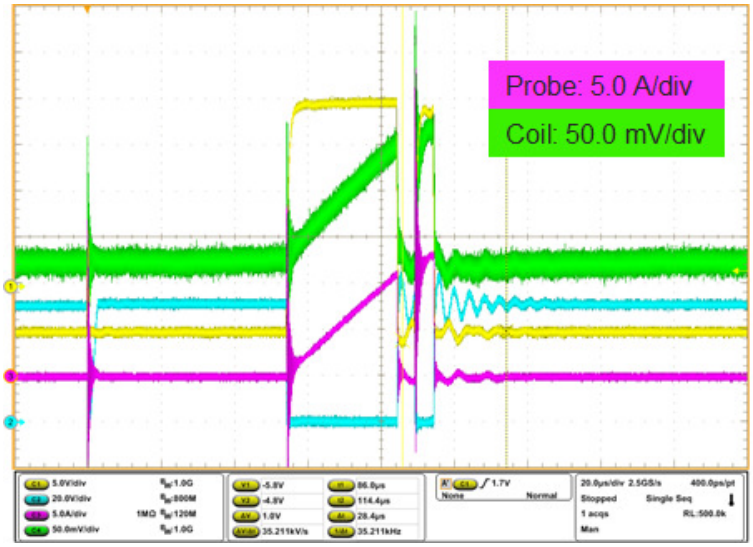
Rogowski coil concept works as intended.

5.4.4 Double pulse test with integrated coil

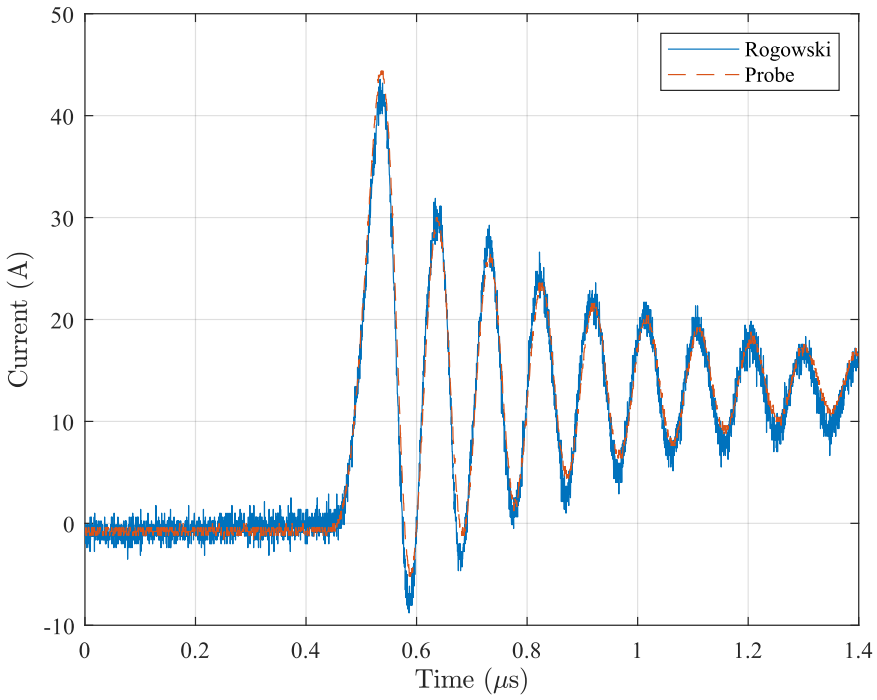
To further demonstrate the capability of integrating the coil into the PCB design, the coil #2 design is embedded into the switching power stage for SiC MOSFET module CCB021M12FM3, which is rated at 1200 V and around 50 A. The PCB layout is shown in Fig. 5.17a. The PCB design uses 6 layers with a total thickness of 2.0 mm. The 3rd to 6th layers share the same stackup as the coil #2 in Table 5.2. The hardware setup is shown in Fig. 5.17b. MMCX connectors are used to feed the integrated coil voltage to the off-board integrator circuit. The turn-on transient voltage and current waveform is shown in Fig. 5.18. The current probe is measuring the load current instead. The switching transient oscillation frequency is around 79 MHz. With the integrated Rogowski coil, the turn-on transient waveforms are captured faithfully with negligible interference into the power loop.

5.5 Conclusion and Discussion

The combinational Rogowski coil concept is proposed here. The self-integrating characteristics of shielded Rogowski coils can be utilized to extend the overall measurement bandwidth. The design methodology and practical considerations are provided. The parasitic element models can facilitate the design, while the error and distortion analysis define the design boundary considerations. Experimental prototypes built with PCB demonstrate a measurement bandwidth of more than 300 MHz. The integrated power stage also shows the concept shows an noninvasive approach for measuring and monitoring the switching transient

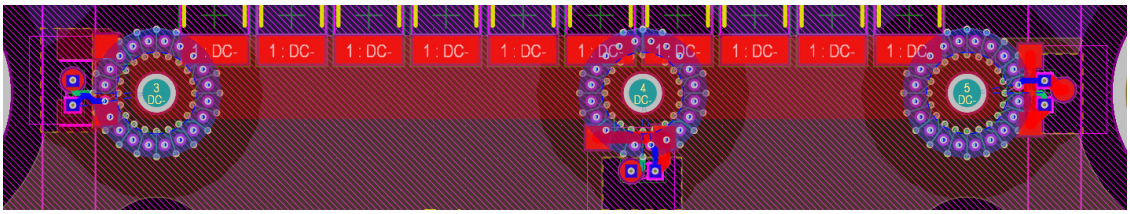


(a)

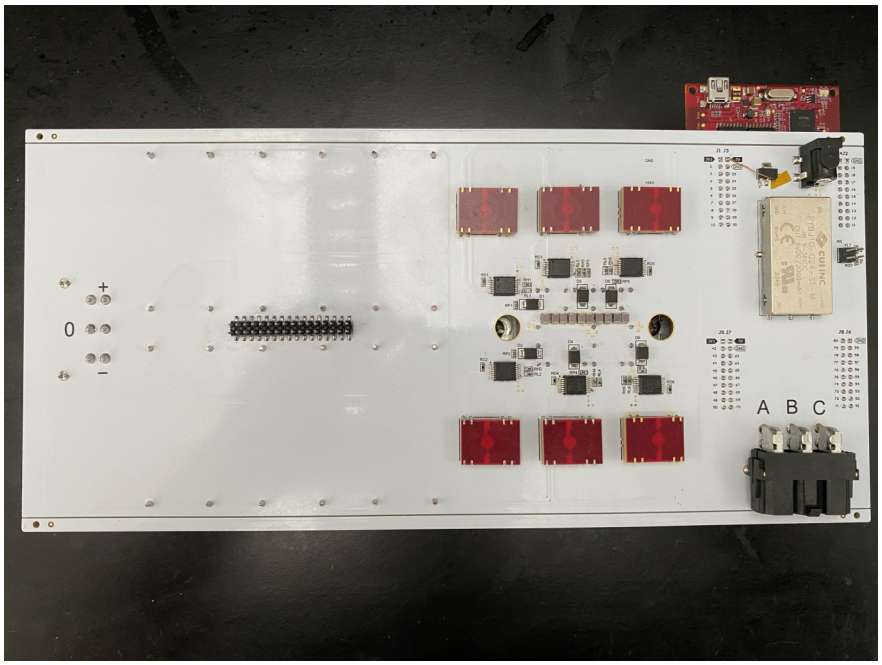


(b)

Figure 5.16: Double pulse test waveform comparison between standalone Rogowski coil and commercial current probe: (a) overall; (b) turn-on transient.



(a)



(b)

Figure 5.17: Integrated Rogowski coil double pulse test setup with SiC MOSFET module CCB021M12FM3: (a) PCB layout; (b) hardware setup.

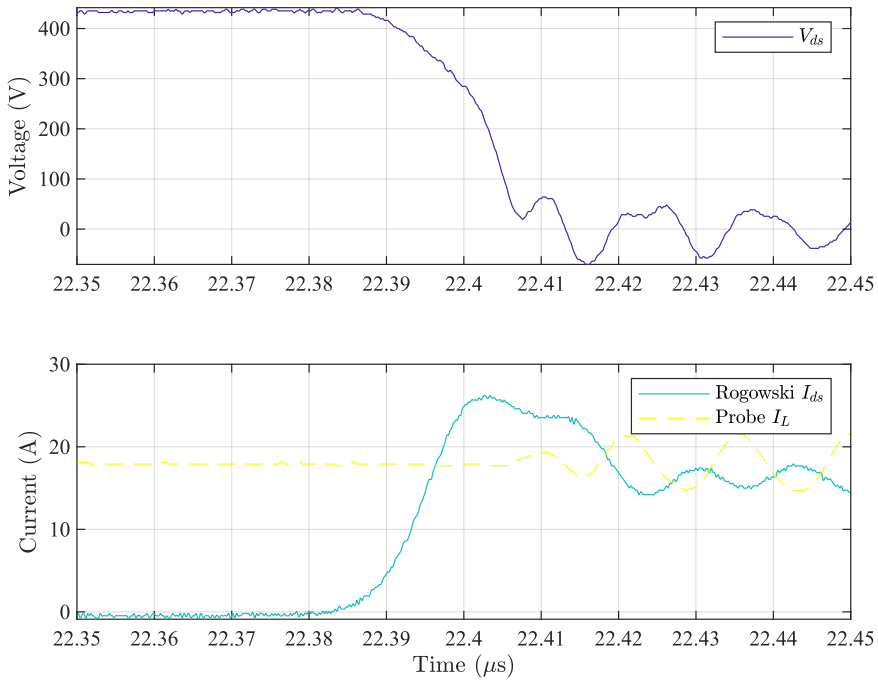


Figure 5.18: Integrated Rogowski coil turn-on transient voltage and current waveform.

current of SiC devices. The combinational Rogowski coil here is also a promising technique to build a standalone current probe for more general-purpose use, given its high bandwidth and small profile. Future work could involve on further improving both the lower and higher bandwidth performance. The gain flatness may also be improved. Given the PCB design here is a closed-loop rigid circle, it may also be interesting to further develop open-ended flexible coils to improve the ease-of-use.

Chapter 6

Output Filters Design and Comparison for SiC-Based Motor Drive

6.1 Introduction

SiC MOSFETs are capable of much higher output voltage slew rate, thanks to its faster switching speed. However, the high voltage slew rate may damage the motor insulation due to the wave reflection [61]. In the worst case, the reflected waves are compounded and the resulting voltage stress may exceed twice the DC link voltage [81]. The sharp voltage edge may also make the voltage distribution inside motor windings uneven, resulting in insulation failure [82]. Furthermore, it has been reported that the fast pulsing capacitive charging and discharging may degrade the insulation in the long term [109], [110]. Therefore, the high output voltage slew rate poses a serious threat to the motor's long term reliability. On the other hand, in deep sea mining or other industrial applications where long cables are needed, the requirement for reliability and efficiency is dominant [111].

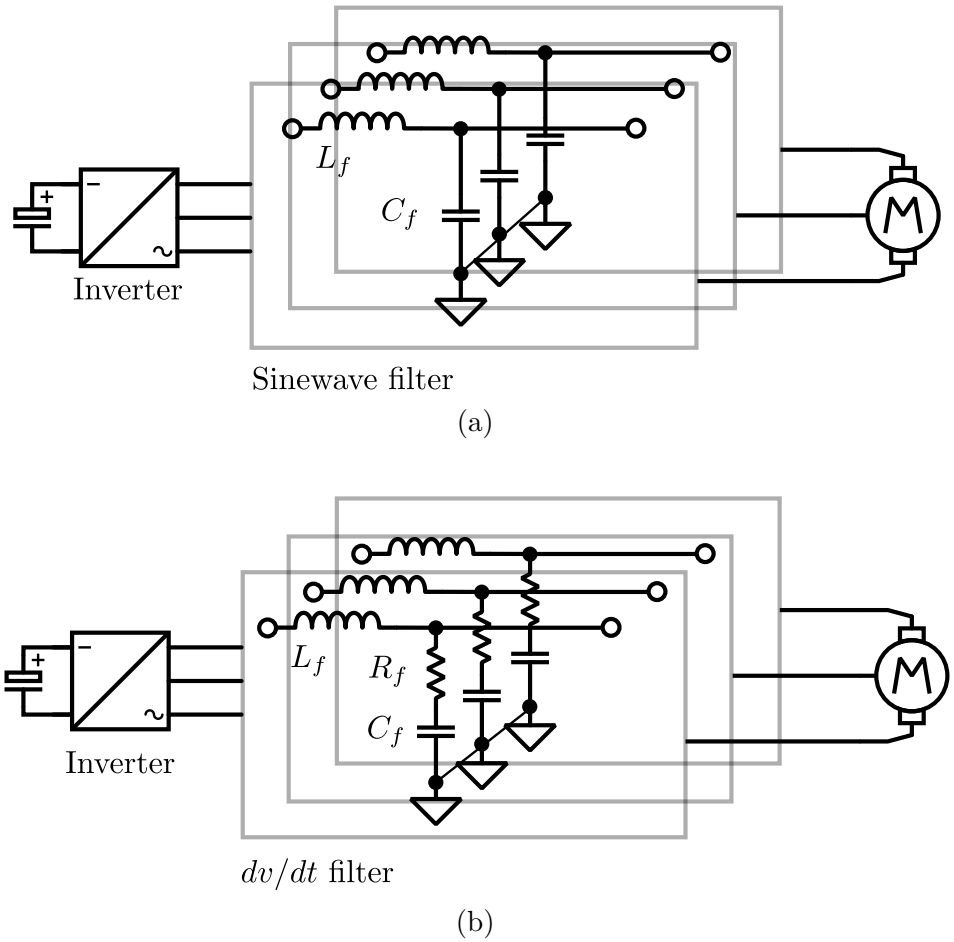


Figure 6.1: Simplified circuit schematic for sinewave and dv/dt filter: (a) sinewave filter; (b) dv/dt filter.

Numerous solutions to these issues have been developed and evaluated over the years. The simplest solution is putting a line termination network consisting of a simple RC filter at the motor terminal to match the cable impedance [62]. While the wave reflection problem is alleviated, the voltage slew rate at the motor terminal is still pretty high and the termination capacitor may result in excessive power loss. An active terminator using diodes to clamp the motor terminal voltage is proposed in [63]. Likewise, although the wave reflection issue is gone, the sharp voltage edge is still present at the motor terminal. A more popular solution, the dv/dt filter, is shown in Fig. 6.1b and has been widely investigated [64]–[71]. Instead of the configuration in Fig. 6.1b, [64] integrates the filter inductor into the converter bus bar and connection cable. Reference [65] put the branch of filter capacitor and resistor in parallel with the filter inductor to reduce the power loss. Reference [66] introduces diode clamping circuit to further limit the voltage overshoot. In addition to diode clamping, [67] put a RC circuit in the diode clamping circuit to help with the EMI. Reference [68] proposes to connect the middle point of the filter capacitors back to the middle point of the DC link to improve EMI. Reference [69] integrates the common mode inductor with the dv/dt filter. Reference [71] combines both the common mode inductor and connects the neutral point back to the middle point of DC link. Reference [70] investigates the effectiveness of using two dv/dt filters in series.

On the other hand, another filter solution, the sinewave filter shown in Fig. 6.1a, has long been considered more expensive, costly and lossy [72]. However, with the high switching frequency capabilities from wide-bandgap devices, they are now being evaluated again. Reference [73] compares the system efficiency of GaN HFET and Si MOSFET motor drive. Reference [74] demonstrates a sinewave filter in GaN HFET motor drive while damping the

sinewave filter with both analog and digital filters.

In addition to the passive filters, active filters involving the switching control of the inverter have also been proposed. In [112], [113], an active dv/dt filter is demonstrated which controls the charging and discharging time of a LC filter to shape the output voltage. However, much more complex gate driving control is required, and the switching frequency is effectively tripled.

Given SiC MOSFETs' faster switching speed capability, the design comparison between sinewave and dv/dt filter is carried out on the system level. The higher switching frequency capability should allow a higher corner frequency for sinewave filter and leads to a better physical size or loss. With the faster switching speed capabilities of SiC MOSFETs, various system level parameters' impact on the comparison are also discussed.

6.2 Filter Design Methodology

6.2.1 System-level requirements

No matter what filter topology is used, to limit the reduction of maximum amount of voltage across the motor, the filter inductance insertion voltage drop should be small. The percentage voltage drop is,

$$\left| \frac{j\omega_0 L_{f,max}}{Z_{lc} + j\omega_0 L_{f,max}} \right| \leq \varepsilon_v, \tag{6.1}$$

where ω_0 is the system fundamental angular frequency, Z_{lc} is the motor impedance in parallel with the filter capacitor branch at nominal condition, and ε_L is the allowed insertion voltage loss and here the requirement is assumed to be $\varepsilon_v = 0.02$. Note that for sinewave filter, Z_{lc} is

essentially the load impedance in parallel with the filter capacitor. For dv/dt filter, typically the filter capacitance is very small and Z_{lc} is dominated by the load impedance and $Z_{lc} \approx Z_l$.

Because the corner frequency of sinewave filters is much lower than the switching frequency, the sinewave filter capacitor may result in significant fundamental frequency capacitive current. Like the filter inductor, another requirement may be brought up for the filter capacitance. However, the capacitive current results in capacitor conduction loss and potentially higher switching device conduction loss. Therefore, by optimizing for a lower overall system loss, the capacitive current or capacitance value will be automatically limited.

For any motor load, the motor current total harmonics distortion (THD) translates into output torque ripple. Sufficiently high PWM switching frequency f_{sw} is usually required to limit the output torque ripple. In other words, there is a lower boundary $f_{sw,min}$ so that

$$\text{THD}_i \leq \varepsilon_{THD}, \tag{6.2}$$

where ε_{THD} is the motor current THD requirement and it is assumed here that $\varepsilon_{THD} = 0.02$.

Finally, the output voltage dv/dt requirement is limited by both the cable length and the motor specification. To avoid the wave reflection along the cable connection, the cable length l must meet the quarter-wavelength requirement

$$l \ll \frac{\lambda}{4}, \tag{6.3}$$

where the wavelength is determined by the frequency components in the voltage rising and falling edges. Given the relationship between rise time and its dominant frequency component

[107], we have

$$\left(\frac{dv}{dt}\right) \ll \frac{c' V_d}{1.4l}, \tag{6.4}$$

where c' is the wave propagation speed in the cable. On the other hand, the motor also typically has a maximum dv/dt specification like in NEMA standard, which can be around 3.0 V/ns to 5.0 V/ns. The overall dv/dt requirement is determined by the more stringent one of the two.

6.2.2 Sinewave filter design

As shown in Fig. 6.1a, the sinewave filter involves two design parameters, the filter inductance L_f and capacitance C_f. Because it is desired to minimize the filter size, the corner frequency for the sinewave filter has to be as high as possible. On the other hand, the converter output voltage is in PWM so there is a risk of LC oscillation for the undamped sinewave filter. Therefore, the corner frequency is placed much lower than the switching frequency,

$$\frac{1}{2\pi L_f C_f} = \frac{1}{10} f_{sw}. \tag{6.5}$$

In addition to the load current THD requirement, the lower boundary of the switching frequency f_{sw} is also bounded by

$$\frac{1}{2\pi L_f C_f} \gg f_0, \tag{6.6}$$

so the impact on fundamental frequency components is minimal. The upper boundary is implicitly included in the overall power loss optimization because higher switching frequency results in higher semiconductor switching loss.

The corner frequency is not enough to define both the filter inductance and capacitance. Therefore, the filter inductance L_f is swept from a small value to $L_{f,max}$. Each combination of f_{sw}, L_f and C_f is simulated in MATLAB/Simulink. The simulation result, namely the converter, filter and load voltage and current, are then used to perform the filter physical design and calculate the system level loss. The filter physical design mainly involves optimizing the filter inductor design, which will be discussed in a later section. The system level power loss includes the device MOSFET switching loss P_{swc}, conduction loss P_{cnd}, capacitor conduction loss P_{cap}, inductor copper loss P_{cop} and magnetic core loss P_{core}. The loss calculation methods will also be discussed later.

6.2.3 Dv/dt filter design

Compared to the sinewave filter, the dv/dt filter's corner frequency is much higher than the switching frequency. Given the dv/dt filter in Fig. 6.1b, assuming the cable and motor load appear as an open circuit during the switching transient, and the source voltage is an ideal step voltage from 0 to V_d, the output voltage V_o of the dv/dt filter is given by

$$\frac{V_o}{V_d} = 1 - e^{-t\frac{R_f}{L_f}} \left(\cosh \frac{t\Delta}{2L_f} - \frac{R_f}{\Delta} \sinh \frac{t\Delta}{2L_f} \right), \tag{6.7}$$

where $\Delta = \sqrt{R_f^2 - \frac{4L_f}{C_f}}$.

The rise time from zero to V_d is given by

$$t_r = \frac{2L_f}{\Delta} \cdot \operatorname{atanh} \frac{\Delta}{R_f}. \tag{6.8}$$

When the filter is critically damped $R_f = 2\sqrt{\frac{L_f}{C_f}}$ and $\Delta = 0$, the rise time can be found with L'Hopital's rule,

$$t_{r,c} = \sqrt{L_f C_f}. \tag{6.9}$$

To simplify the analysis, it is assumed that the dv/dt filter is always in the critically damped condition. Therefore, given a critically damped filter and a motor drive with a output voltage slew rate requirement of dv/dt,

$$\sqrt{L_f C_f} = \frac{V_d}{dv/dt}. \tag{6.10}$$

Similar to the sinewave filter, the dv/dt filter inductance is swept from a small value to the maximum value $L_{f,max}$, and physical design for inductor and loss calculation are performed. Note that, in the dv/dt filter, the filter capacitance C_f is charged and discharged every switching cycle. Instead of capacitor equivalent series resistance loss, the capacitor loss P_{cap} for a dv/dt filter is the loss on the damping resistance R_f. The loss behavior is similar to charging and discharging the gate capacitance, the capacitor loss P_{cap} for dv/dt filters is given by

$$P_{cap} = f_{sw} C_f V_d^2. \tag{6.11}$$

Finally, the overall filter design comparison flowchart is shown in Fig. 6.2. Simulation, loss calculation and inductor physical design are performed for every combination of sinewave and dv/dt filter design. The best case for each filter topology is selected for comparison.

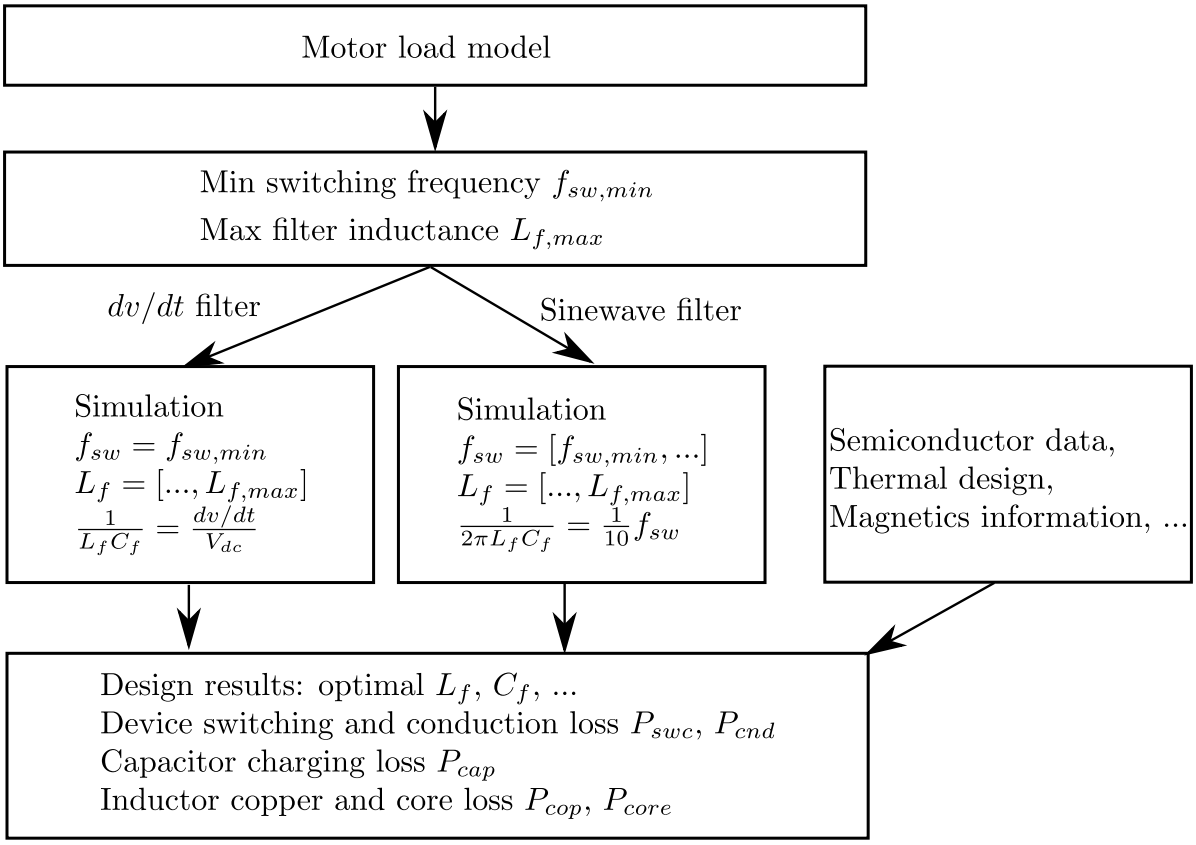


Figure 6.2: High-level simplified sinewave and dv/dt filter design procedure.

6.2.4 Loss calculation method

The switching device switching loss is approximated by linear interpolation,

$$E_{on}(V_d, I_L) = E_{on,0} \cdot \frac{V_d}{V_{d,0}} \cdot \frac{I_L}{I_{L,0}}, \tag{6.12}$$

$$E_{off}(V_d, I_L) = E_{off,0} \cdot \frac{V_d}{V_{d,0}} \cdot \frac{I_L}{I_{L,0}}, \tag{6.13}$$

where $E_{on,0}$ and $E_{off,0}$ are the device datasheet provided turn-on and turn-off energy loss, and $V_{d,0}$ and $I_{L,0}$ is the datasheet DC link voltage and load current testing condition. Note that typically SiC MOSFETs switching loss has little dependence on junction temperature, so it is assumed E_{on} and E_{off} are consistent across different temperatures. The switching loss is then given by

$$P_{swc} = f_0 \left(\sum_{I_{on}} E_{on}(V_d, I_{on}) + \sum_{I_{off}} E_{off}(V_d, I_{off}) \right), \tag{6.14}$$

where I_{on} and I_{off} are the list of turn-on and turn-off instant load current in a fundamental cycle. In practice, I_{on} and I_{off} are obtained through MATLAB/Simulink simulation.

On the other hand, the conduction loss calculation takes the junction temperature T_j into consideration. Given the $R_{ds,on} = R_{ds}(T_j)$ relationship from datasheets, the conduction loss $P_{cnd} = I_{rms}^2 R_{ds}^2(T_j)$ is calculated by iteratively and numerically solving

$$(R_{jc} + R_{ca}) \left(P_{cnd}(T_j) + P_{swc} \right) = T_j - T_a, \tag{6.15}$$

where R_{jc} and R_{ja} are the junction-to-case and junction-to-ambient thermal resistances, T_a

is the ambient temperature is assumed to be 50°C.

The inductor copper loss is simply assumed to the DC resistance condution loss,

$$P_{cop} = R_{winding} I_{ind}^2. \tag{6.16}$$

As for the inductor core loss, it is calculated by separating and major and minor loops as in the IGSE method [114],

$$P_{mag} = V_c f_0 \int_0^{1/f_0} k_i \left| \frac{dB}{dt} \right|^{\alpha} (\Delta B)^{\beta-\alpha} dt, \tag{6.17}$$

where V_c is the volume of the magnetic core.

6.2.5 Toroidal powder core inductor design

The filter inductor typically takes up a major part in the system weight. The inductor copper and core loss also greatly depends on the magnetic core material and geometry. In order to have an apple-to-apple comparison, instead of restricting the cores to commercially available ones, it is assumed here that the core geometrical dimensions are free variables. In other words, we have the freedom to select the optimal core shape and achieve an ideal inductor design. Given a toroidal shape with a rectangular cross section, there are three geometrical variables, namely the inner diameter D_i, outer diameter D_o and height H, as shown in Fig. 6.3. As for the inductor winding, the design choices include the winding wire gauge or cross-sectional area A_w and the number of turns N_t. In some cases, it is preferable to connect multiple inductors in series to achieve higher inductance. So another design variable

is the number cores N_c.

The optimization goal may be to minimize the weight of the inductor, which can be written as

$$m = N_c \left(\frac{\pi}{4} H \left(D_o^2 - D_i^2 \right) \rho_c + (2H + D_o - D_i) N_t A_w \rho_w \right), \tag{6.18}$$

where ρ_c and ρ_w are the density of the core and wire, respectively. If the goal is to minimize the enclosure volume of the inductor, the objective function is

$$V = N_c H \left(\pi \left(0.5 D_o + D_w \right)^2 \right), \tag{6.19}$$

where D_w is the diameter of the winding wire.

As for the design constraints, the winding must fit into the center window of the toroid,

$$\frac{\pi}{4} D_i^2 \geq k_f N_t A_w, \tag{6.20}$$

where k_f is the filling factor. Another constraint is the inductance L must be within design tolerance,

$$L_r = \frac{2\mu_r \mu_0 N_c N_t^2 A_c}{\pi (D_o + D_i)} \in \left[(1 - \varepsilon_l) L_0, (1 + \varepsilon_l) L_0 \right], \tag{6.21}$$

where μ_r is the relative permeability at DC, ε is the design tolerance and here $\varepsilon_l = 0.02$.

Another consideration in inductor design is the core saturation. Given a tolerance of inductance change at maximum current to be ϵ_s, another constraint is

$$\frac{\mu_s}{\mu_r} = \frac{1}{a + b(N_t I_{max})^c} \geq 1 - \varepsilon_s, \tag{6.22}$$

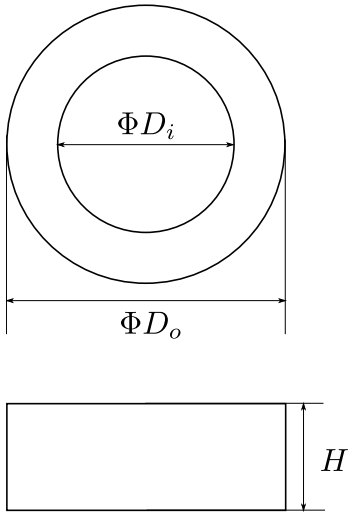


Figure 6.3: Toroidal powder core geometrical shape and relevant design parameters.

where a, b, c are the permeability coefficient when under load and usually provided by manufacturers, I_{max} is the inductor maximum current and is obtained through simulation. The saturation tolerance here $\varepsilon_s = 0.05$.

Finally, the winding wire gauge is limited by the maximum current density [115],

$$\frac{I_{rms}}{A_w} \leq J_m, \tag{6.23}$$

where J_m is the maximum current density and I_{rms} is the root-mean-square (rms) value of the inductor current. For open windings, the maximum current density is assumed to be 6.0 A/mm^2.

The optimization problem here is a mixed-integer nonlinear programming problem and can be attempted with commercial software like MATLAB. As an interesting example, assuming $I_{rms} = 20$ A, $I_{max} = 30$ A, the optimization problem is solved for desired inductance between 10 μH to 600 μH. The core material is assumed to be FluxScan 60μ from Micrometals. The design objective is to minimize the inductor weight. The toroidal powder core inductor design results are shown in Fig. 6.4. Interestingly, the optimal weight increases almost linearly with the desired inductance. It is also shown that it is better to go for two inductors in series for larger inductances $L > 420$ μH.

6.3 Filter Comparison and Switching Frequency Impact

The nominal condition load parameters are listed in Table 6.1. Simple LR loads are used to represent the motor load impedance in rated condition. The load power factor is

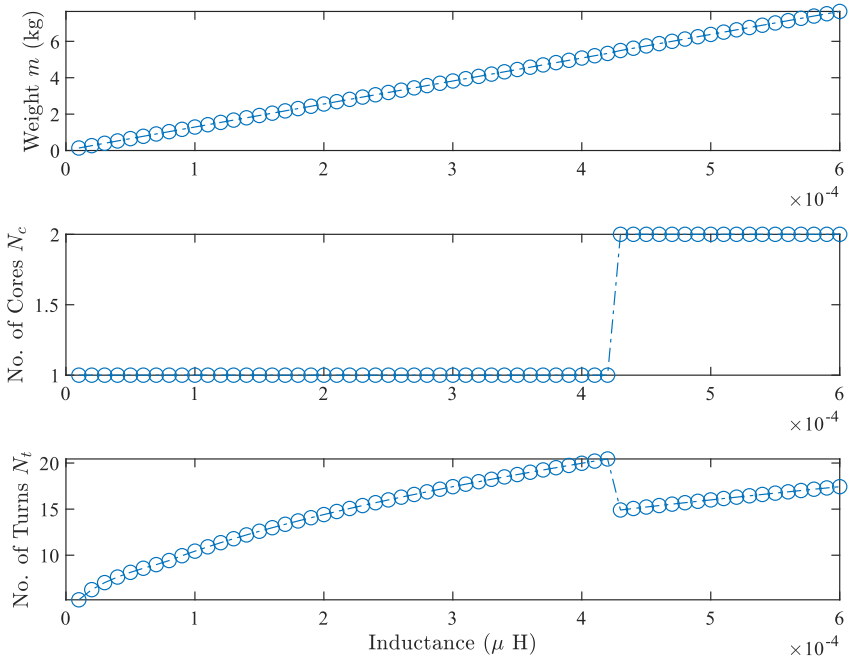


Figure 6.4: Toroidal inductor design optimization example.

assumed to be 0.83, which is typical for induction machines. The DC link voltage is at 650 V and the load RMS current is around 15 A. The ambient temperature T_a is assumed to be 50°C. The SiC MOSFET C2M0080120D from Wolfspeed is used here. Three cases with different fundamental frequency are compared here. Because higher fundamental frequency mandates higher switching frequency given the same current THD requirement, we can study the impact of switching frequency. The motor load dv/dt requirement is assumed to be 2.5 V/ns to leave sufficient margin.

6.3.1 Dv/dt filter design sweep

The dv/dt filter design results for the three different cases are shown in Fig. 6.5. Because the overall system loss is of interest, the per phase loss breakdown for each filter inductance sweep is shown. Looking at each case itself, the MOSFET conduction loss P_{cnd} and switching loss P_{swc} remain nearly constant for all cases. Because the dv/dt filter only target switching transient frequency components, the current flowing through each MOSFET remains unchanged. It is also evident that the inductor copper loss P_{cop} increases with larger inductance value. This is expected because larger inductance means more number of turns and larger magnetic core. The inductor core loss P_{core} stays negligible for all scenarios, as the load current THD or ripple is small and the powder core material is relatively efficient. However, comparing Fig. 6.5a and Fig. 6.5c, the capacitor charging and discharging loss P_{cap} is clearly more pronounced when the fundamental or switching frequency is higher, which is not a surprise because P_{cap} is proportional to the switching frequency f_{sw}. The capacitor loss P_{cap} starts becoming dominant in higher frequency applications, which may require extra heat dissipation. This

Table 6.1: Nominal condition load parameters and system-level requirements

Parameter	Value		
Power factor		0.83	
Nominal voltage (V)		395	
Nominal current (A)		15.2	
Load resistance (Ω)		12.5	
Fundamental frequency (Hz)	100	300	600
Load inductance (mH)	13.2	4.4	2.2
Minimum switching frequency (kHz)	4.6	13.8	27.5
Voltage loss ε_v		0.02	
Load current THD ε_i		0.02	
Motor maximum dv/dt (V/ns)		2.5	

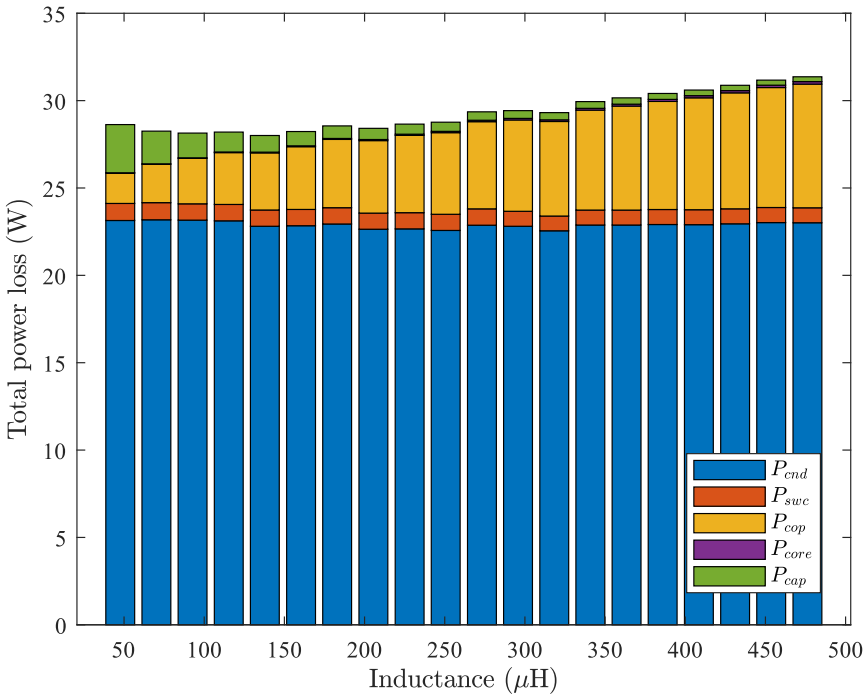
suggests dv/dt filters are suitable for high frequency applications.

It should also be noted that for Fig. 6.5b and Fig. 6.5c, the overall loss exhibits a somewhat "saturated" behavior. In Fig. 6.5c, for example, when the filter inductance increases from 60.6 μH to 79.4 μH, the per-phase power loss only decreases from 40.3 W to 37.6 W. On the other hand, each filter inductor's weight increases from 109 g to 136 g. Therefore, in these cases, it might be beneficial to sacrifice the power loss a little bit and to gain some advantage in filter weight.

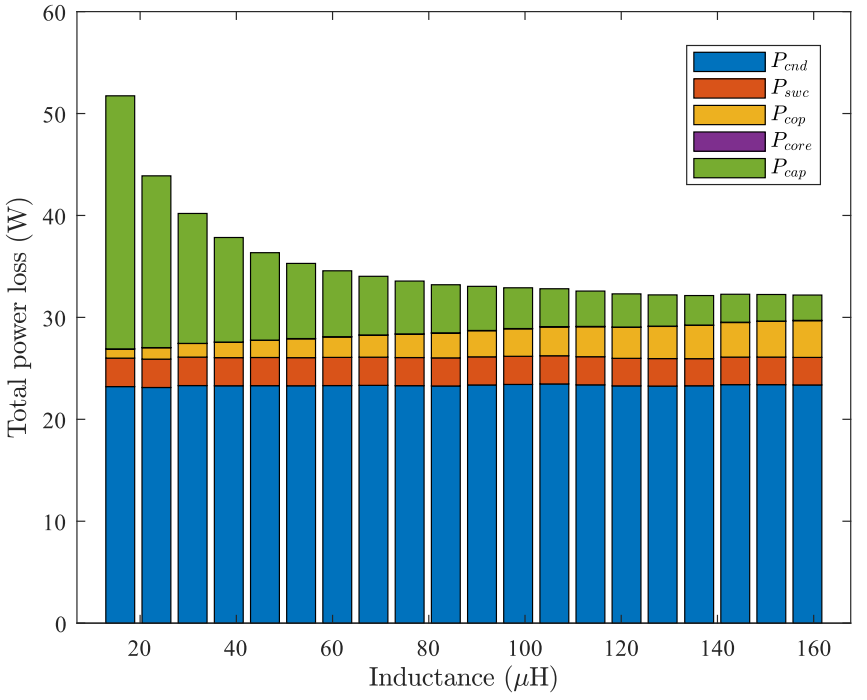
6.3.2 Sinewave filter design sweep

The sinewave filter design results are shown in Fig. 6.6. The larger filter capacitors are usually film capacitors, and it is assumed that the equivalent series resistance (ESR) is 3 mΩ. In some of the results, especially when the filter inductance is small, the loss axis may appear very short and shows up a flat square. This is because the capacitive current draw from the filter capacitor is too large, and the junction temperature of the SiC MOSFET exceed its maximum rating. These results should be neglected. Comparing across the different fundamental and switching frequencies, we can also observe a similar "saturation" behavior. Sometimes further increasing the filter inductance does not change the overall per-phase loss anymore. As the switching frequency increases, smaller filter inductance and capacitance can be utilized, but comes with the sacrifice of higher switching loss. Comparing with the dv/dt filter design result in Fig. 6.5, the filter inductor shows higher core loss, as the filter capacitor current results in much higher current ripple in the filter inductor.

In Fig. 6.6a, we can already see the benefits of the sinewave filter. With $f_{sw} = 31.5$ kHz,

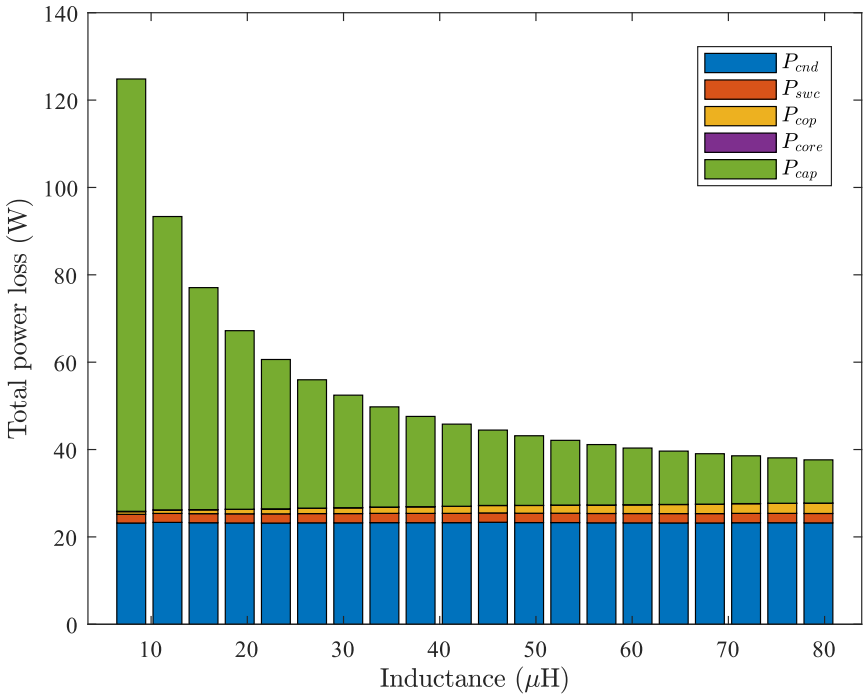


(a)



(b)

Figure 6.5: Filter design per phase loss breakdown for dv/dt filter: (a) $f_0 = 100$ Hz; (b) $f_0 = 300$ Hz; (c) $f_0 = 600$ Hz.



(c)

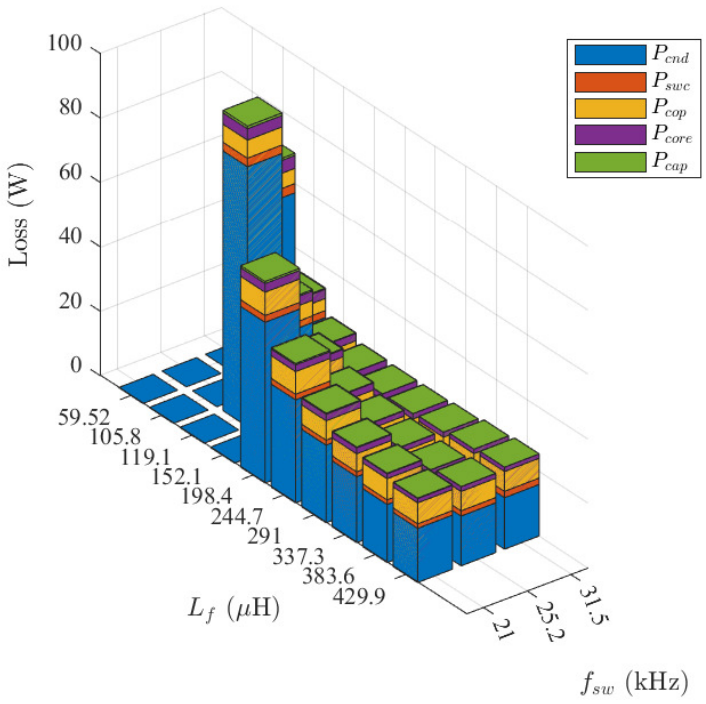
Figure 6.5: Filter design per phase loss breakdown for dv/dt filter: (a) $f_0 = 100$ Hz; (b) $f_0 = 300$ Hz; (c) $f_0 = 600$ Hz.

$L_f = 337.3$ μH and $C_f = 9.34$ μF, the per-phase power loss is only 23.6 W. In Fig. 6.5a, the best case with dv/dt filter at $f_0 = 100$ Hz, where $L_f = 92.7$ μH and $C_f = 0.73$ nF, results in a per-phase power loss of 26.9 W, around 14% higher than the sinewave filter. However, the optimal dv/dt filter design results in a much smaller filter inductance value and lighter inductor. The sinewave inductor weighs 363 g while the dv/dt inductor weighs 167 g. As the fundamental frequency f_0 increases, the sinewave filter starts to become even more advantageous. With $f_0 = 600$ Hz, the optimal sinewave filter is achieved at $f_{sw} = 84$ kHz, $L_f = 42.5$ μH, and $C_f = 10$ μF. The per-phase loss is 27 W. However, with dv/dt filter at $f_0 = 600$ Hz, the optimal case has a filter inductance of 79.4 μH and a filter capacitance of 0.98 nF. The resulting per-phase loss is 37.6 W. The dv/dt filter inductor weighs 136 g while the sinewave filter only weighs 105 g.

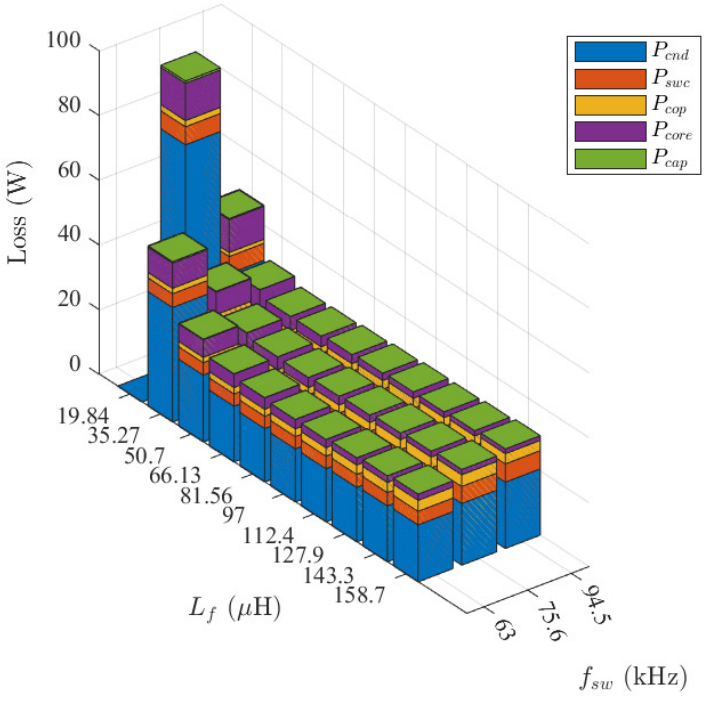
In conclusion, the sinewave filter may be more attractive for SiC MOSFET inverters, especially if the switching frequency is high. Thanks to the lower switching loss of SiC MOSFETs, the switching frequency could be deliberately increased to allow smaller filter inductance and capacitance, while the switching loss takes a minimal impact.

6.4 Experimental Verification

To illustrate and verify the potential benefits of sinewave filters over dv/dt filters, the experimental converter and load setup is established and shown in Fig. 6.7. The experimental load is the same as the 600 Hz case in Table 6.1, where $R_l = 12.5$ Ω and $L_l = 2.2$ mH. The interconnecting cable between the load and the inverter is around 15 ft. The higher fundamental frequency is shown to favor sinewave filter in the previous section. The pulse

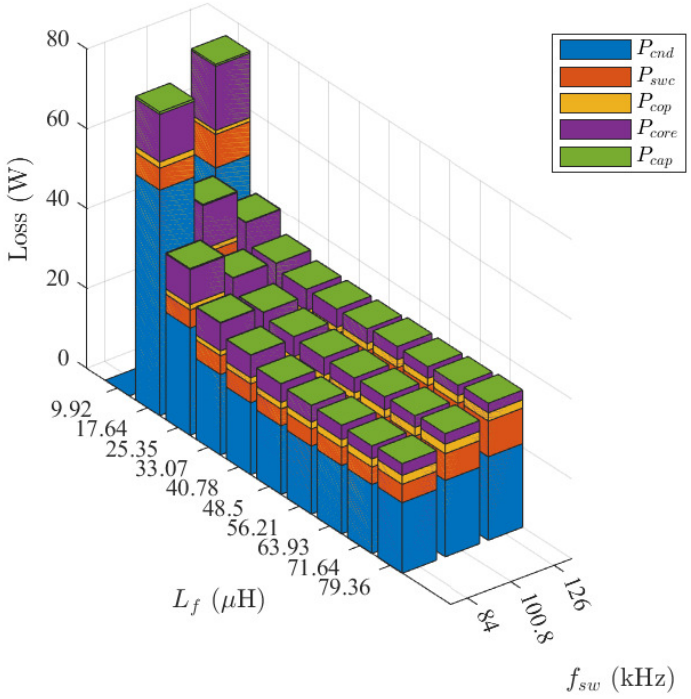


(a)



(b)

Figure 6.6: Filter design per-phase loss breakdown for sinewave filter: (a) $f_0 = 100Hz$; (b) $f_0 = 300Hz$; (c) $f_0 = 600Hz$.



(c)

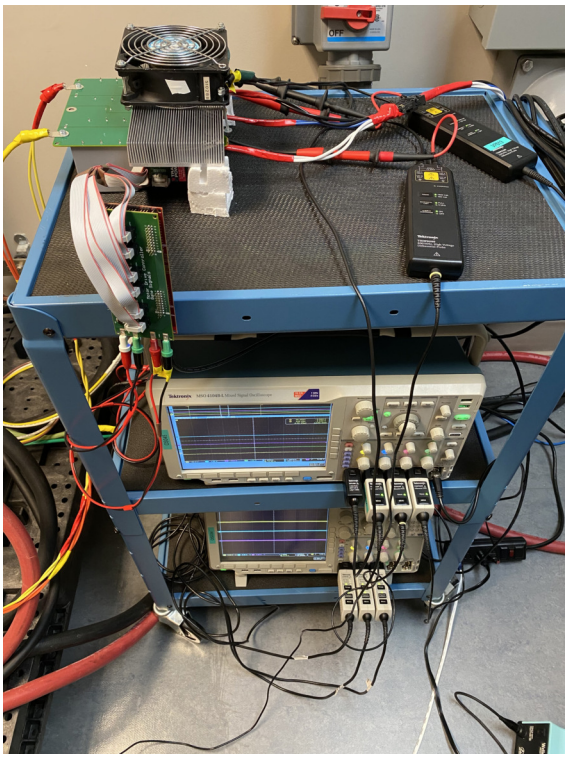
Figure 6.6: Filter design per-phase loss breakdown for sinewave filter: (a) $f_0 = 100Hz$; (b) $f_0 = 300Hz$; (c) $f_0 = 600Hz$.

wave modulation (PWM) strategy here is the simple sinusoidal PWM. The load current is in open-loop and is guaranteed the same through carefully adjusting the modulation index so the load current is the same on the oscilloscope.

The filter choices are listed in Table 6.2, which corresponds to the cases close to the optimal ones in Fig. 6.5c and Fig. 6.6c. The filter inductors are wound on the same powder core FS-300060 from Micrometals, which is the closest available core geometry suitable for the desired inductance. The inductors are shown in Fig. 6.8. The winding is made from two AWG#16 wires in parallel. The dv/dt filter inductor requires more windings. Also note that because it is not practically possible to achieve the optimal inductor design due to the available core geometries, the resulting inductor weight and overall system-level power loss would be different. But still, we can see that the sinewave filter inductor takes less number of turns.

The comparison between the inverter output voltage and the load phase-to-neutral voltage is shown in Fig. 6.9. The inverter output voltage is measured between the phase A output to the inverter ground. The load voltage with or without dv/dt filter is measured between at the A phase input and the load neutral point. The SiC MOSFET's very sharp rise edge is greatly slowed down after the dv/dt filter, around 2.0 V/ns and below 2.5 V/ns. Without the dv/dt filter, the load sees very high voltage overshoot, nearly twice the DC link voltage. Note that the load voltage measurements show significant oscillation, which is likely due to the measurement setup where the load neutral point is very far away from the differential probe. In the filter inductor current waveforms also shown in Fig. 6.9, the current is nearly pure sinusoidal with little harmonics as expected.

As a comparison, the line-to-line voltage waveforms of the inverter output and the load



(a)

(b)

Figure 6.7: Filter loss comparison experimental (a) converter and (b) load setup.

Table 6.2: Filter comparison experimental setup

	Sinewave	Dv/dt
Core	FS-300060	
No. of turns	25	34
Filter inductance (μH)	42.5	78.6
Filter capacitance (nF)	10,000	1.0
Filter resistance (Ω)	-	600
Switching frequency (kHz)	84.0	27.5

Figure 6.8: Sinewave (left) and dv/dt (right) filter inductors comparison.

side are shown in Fig. 6.10. The line-to-line voltage of the inverter has very sharp rise and fall edge, just like the phase voltage. However, after the sinewave filter, the load voltage is nearly completely sinusoidal, which means the load current will also be nearly sinusoidal. In the inverter output current waveforms, on the other hand, there is a lot more harmonics content due to the filter capacitor. Although the RMS value of the phase current is almost the same as in dv/dt filter, the higher harmonics and resulting higher peak current means the SiC MOSFET sees a higher load current during the switching transient, which may negatively impact the switching transient voltage overshoot across the MOSFETs.

The inverter input and output power figures are listed in Table 6.3. Compared to the optimal design results in Fig. 6.5c and Fig. 6.6c, the power loss is a bit higher, which is likely due to the non-optimal inductor design. Still, the dv/dt filter shows nearly 25.8% higher loss than the sinewave filter, proving that sinewave filters are more advantageous for higher frequency applications. The actual per-phase loss is also compared against the previous model. The prediction for the dv/dt filter is very close to the actual loss, with a difference of only 2.2%. The small difference could be due to the difference in the thermal model between experimental setup and the model. For the sinewave filter, the difference is slightly larger at 7.5%. The reason could be the higher harmonics current in the sinewave filter results in AC copper loss, which is not included in the previous loss model.

6.5 Conclusion and Discussion

The high output voltage slew rate of PWM voltage source inverters can be detrimental to the load. The popular choices of dv/dt filter and sinewave filter are compared on the overall

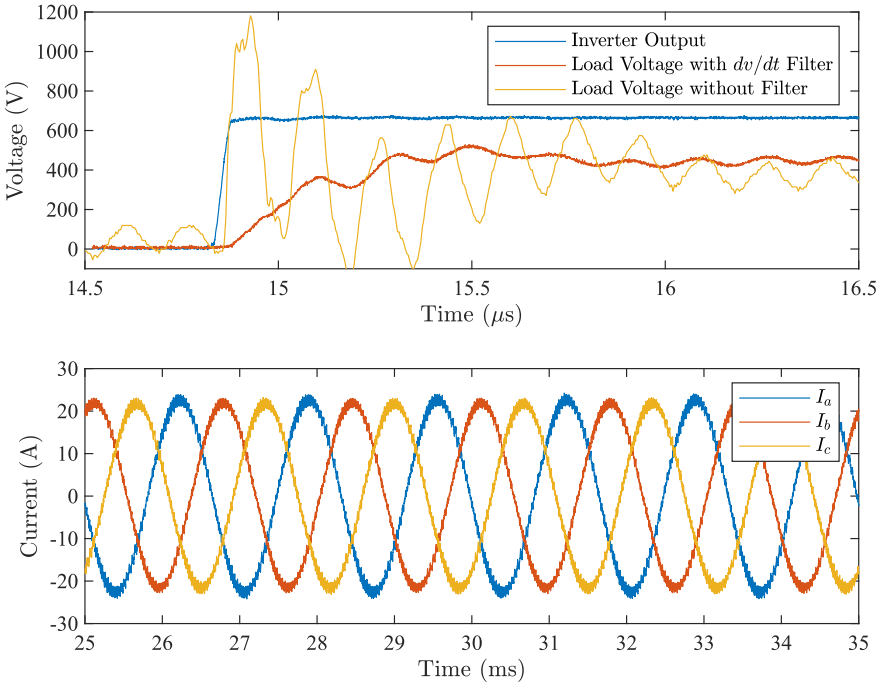


Figure 6.9: Dv/dt filter experimental waveforms.

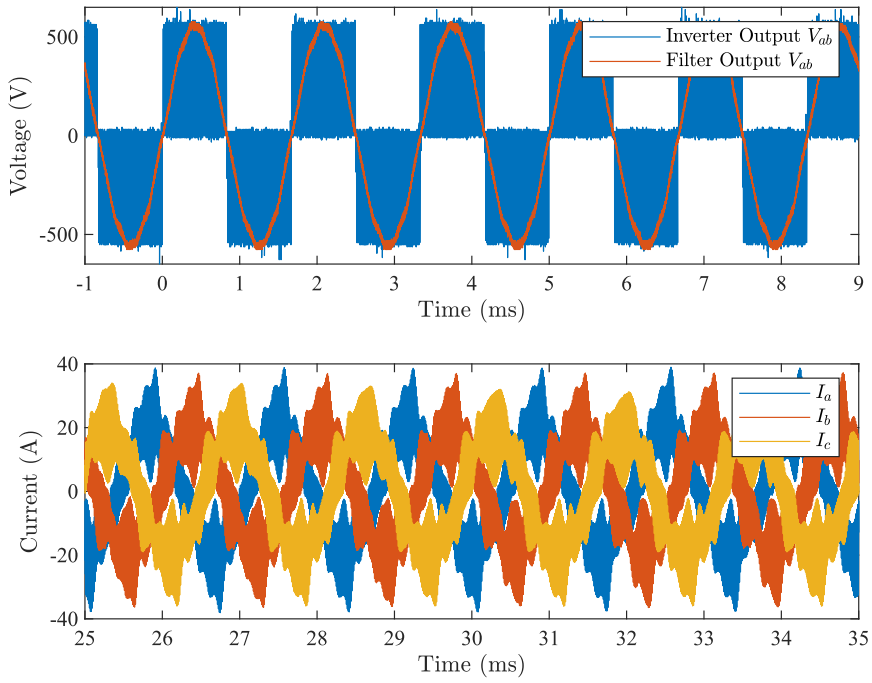


Figure 6.10: Sinewave filter experimental waveforms.

Table 6.3: Filter system level loss comparison

	Sinewave	Dv/dt
Input (kW)	9.94	9.97
Output (kW)	9.82	9.82
Total loss (W)	120.0	150.9
Actual per-phase loss (W)	40.0	50.3
Predicted per-phase loss (W)	37.0	49.2
Efficiency (%)	98.79	98.50

system level loss basis. It is shown that given the higher switching frequency capabilities of SiC MOSFETs, the sinewave filters are especially beneficial for scenarios where the fundamental frequency is high. Not only the overall system level loss is lower, the filter inductor can also be significantly smaller.

This work can be further extended by looking at other system parameters like the load power factor, DC link voltage and load current. Non-nominal conditions like light load or startup process can also be interesting to look into. The higher current ripple in the sinewave filter inductor can also mean higher peak switching transient current. The impact on the noise spectrum and overvoltage stress can also be part of the future work.

Chapter 7

Conclusion and Potential Future Work

7.1 Summary

Various issues related to the fast switching speed of power semiconductors are treated in this dissertation. Key results and contributions in the previous chapters are summarized below.

1. The unique properties of switching transient overvoltages are discussed in **Chapter 2**. The turn-off overvoltage exhibits strong nonlinearity with the faster switching SiC MOSFET, while the turn-on overvoltage shows little dependence of load current condition. Numerical modeling approach with neural net is also presented, and it is shown that the switching transient overvoltage can be accurately predicted to guide the device selection.

2. As the switching speed increases, the parasitic elements' impact become more pronounced. A new abnormal oscillation pattern, "self-turn-on" is reported with a trench

MOSFET. The common source inductance and the unconventional nonlinear parasitic capacitance force the MOSFET channel to turn on again during the turn-off transient, resulting in significant voltage and current spikes and potentially loss of control. The findings could help with the semiconductor device and packaging design. The large-signal models also contribute the understanding of switching transient stability.

3. Gate drivers are the key component regulating the switching transient behavior. With the advent of wide-bandgap semiconductors, a wide range of switching devices have been available. A programmable gate driver platform is proposed to meet the need for fast and easy semiconductor device driving with different schemes. The platform can greatly facilitate the evaluation of devices and optimization of gate driving schemes.

4. The faster switching speed also presents challenges for device switching transient measurement and monitoring. The combinational Rogowski coil concept is proposed to achieve both high-bandwidth and small electrical footprint. Design methodologies and practical considerations are presented. Experimental prototypes proved that the concept can achieve up to 300 MHz bandwidth while introducing little interference to the power loop. The concept here is an enabling technology for switching transient measurement, and can be instrumental for semiconductor protection and monitoring purpose.

5. The high output voltage slew rate may negatively impact the motor load insulation, especially when connected with a long cable. Leveraging the faster switching frequency and lower switching loss capability of SiC MOSFETs, it is shown that sinewave filters can be both more efficient and more compact than dv/dt filters, especially in high

frequency applications. The optimization methodology and filter comparison result here can help guide future output filter design and selection for motor drive application.

7.2 Potential Future Work

While the contributions answer the corresponding issues, several interesting topics and potential future work are pointed out here.

1. The required information and parameters for switching transient modeling purpose can not be obtained solely from the datasheets. The numerical modeling approach can be greatly enhanced with a more streamlined and standardized procedure.

2. The gain flatness of the combinational Rogowski coil is immediately determined by the hand-off region between the integrator and the self-integrating Rogowski coil. A better tuning approach can help achieve better gain flatness. The lower measurement bandwidth is also relatively high. DC current sensors could be potentially integrated into the combinational Rogowski coil to achieve even better functionality and adapt to wider application scenarios.

3. The comparison between the sinewave and dv/dt filters is performed with a LR load due to the motor load availability. The design comparison could further consider non-nominal conditions, such as startup or light load. Besides the fundamental frequency, other system parameters, including power factor, DC link voltage and converter voltage levels, may also impact the comparison result.

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Vita

Wen Zhang received his Bachelor's degree in Electrical Engineering from Huazhong University of Science and Technology, Wuhan, China in 2015 and his Master's degree also in Electrical Engineering from University of Tennessee, Knoxville in 2019. He is now a Ph.D. candidate at the University of Tennessee. His research interests include wide-bandgap semiconductor and their applications, motor drive, and sensing technologies.