

## MINIMUM COMPONENT HIGH FREQUENCY CURRENT MODE RECTIFIER

J. Sampe<sup>1,\*</sup>, M. Fasehuddin<sup>1</sup>, S. Shireen<sup>2</sup> and S. H. M. Ali<sup>3</sup>

<sup>1</sup>Institute of Microengineering and Nanoelectronics (IMEN), University Kebangsaan Malaysia,  
Bangi, Selangor, Malaysia

<sup>2</sup>Indus Institute of Technology and Management, Kanpur, India

<sup>3</sup>Department of Electrical, Electronic and Systems Engineering, University Kebangsaan  
Malaysia, Bangi, Selangor, Malaysia

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### ABSTRACT

In this paper a current mode full wave rectifier circuit is proposed. The current mode rectifier circuit is implemented utilizing a floating current source (FCS) as an active element. The minimum component full wave rectifier utilizes only a single floating current source, two diodes and two grounded resistors. The extremely simple implementation enjoys high frequency operation and provides both inverting and non-inverting rectified outputs simultaneously. The rectifier system can work up to a frequency of 500MHz with acceptable distortion. The circuit exhibits low power consumption at  $\pm 0.75V$  supply voltage. The non-ideal and temperature analysis was also performed to study their impact on its performance. It was also shown that FCS can work as half wave rectifier as well. The performance of the circuit is evaluated using 0.18 $\mu m$  TSMC CMOS parameters using Hspice.

**Keywords:** current-mode circuits; floating current source; high frequency; rectifiers.

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Author Correspondence, e-mail: [jahariah@ukm.edu.my](mailto:jahariah@ukm.edu.my)

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## 1. INTRODUCTION

The rectification process is one of the most important process which find application in piecewise linear function generators, RF demodulators, AC voltmeters, DC converters, watt meters, analogue signal conditioning and processing circuits, communication, instrumentation, measurement and control [1-3]. The threshold voltage of the diode and the diode commutation cause distortion at higher frequencies and this limits the applications of the conventional rectifiers based on diodes to DC power supplies and low frequency and medium accuracy applications. For the applications demanding higher accuracy down to few mV range, precision rectifiers composed of operational amplifiers, diodes and resistors are the choice [3-4]. However, the limited bandwidth and low slew rate of the op-amps render them unsuitable for today's low voltage, high frequency and high precision rectification requirement [1-2]. The current mode technique is found to possess numerous advantageous over its voltage mode counterpart. It provides wide bandwidth, high slew rate, simple implementation and is less affected by reduction in supply voltage [5-7]. Many implementations of current and voltage mode rectifiers based on current mode active elements can be found in the literature [1-4]. The rectifiers based on operational transconductance amplifiers (OTA) and current conveyors (CC) have been proposed recently by many researchers [1-4, 8-20]. These current and voltage mode precision rectifiers are reported to work well but most of them have large component count which increases the area and limits the operating frequency.

In [8] presented a current controlled current conveyor (CCCII) based precision full-wave rectifier circuit. It uses four CCCII, three metal-oxide semiconductor (MOS) transistors and a capacitor. The circuit had an all pass filter to filter out the ripples. The circuit can operate at a maximum frequency of 20 MHz. The circuit proposed by [9] uses four bipolar current mirrors, one second generation current conveyor (CCII) and two resistors. It was shown to work up to 100 kHz but it did not provide low output impedance. Similarly, the rectifier circuit given by [10] employing two CCII, four diodes, and two resistors worked at a frequency of 30 MHz. In [11] used an operational transconductance amplifier (OTA) and four MOS diodes and a resistor to develop a voltage mode rectifier circuit. The circuit operated at high frequency of 300 MHz but with some distortion. The same author [12] proposed an OTA based voltage

mode rectifier utilizing one OTA, four MOS diodes and one resistor. The circuit works up to 200MHz. The circuit uses large number of components leading to increased area and power dissipation. In [13] proposed a voltage mode rectifier using one current controlled current conveyor (CCCII), two MOS transistors and a resistor. The circuit's performance degrades at high frequencies. In [14] proposed a mixed mode full wave rectifier employing current differencing transconductance amplifier (CDTA) and two MOS transistors the circuit performs well above 100MHz. Another CDTA based implementation is presented by [15], employing one CDTA and four diodes and works well up to 5 MHz frequency. The work presented by [16] uses one CDTA and two diodes for current mode rectification. The operating frequency of the circuit is 5MHz. Recently, in [17] presented a rectifier employing dual X current conveyor (DXCCII) and two diodes. The output is available at the high impedance node and the rectifier is shown to work at 120MHz frequency. In [18] recently proposed a high input impedance and low output impedance differential voltage current conveyor based implementation of the full wave rectifier. The rectifier employed two DVCCs, two diodes and two resistors. The circuit performance was discussed at a moderate frequency of 1MHz. In [19] recently proposed a low voltage diode less rectifier based on bulk driven winner take all circuit (BD-WTA) and CMOS inverter. Although the circuit consumes less power, but the rectification frequency is limited at 100 KHz.

The circuit proposed in this study employs a floating current source (FCS) firstly proposed by [20]. The circuit is extremely simple employing only one FCS, one diode and a resistor for half wave rectifier. The full wave rectifier uses one FCS, two diodes and two resistors. The circuit is capable of working at very high frequency of 500MHz and provides both inverting and non-inverting outputs simultaneously leading to flexibility and less chip area. Table 1 provides a detailed comparison between different rectifiers and the proposed rectifier.

**Table 1.** Comparison of rectifiers available in literature

Reference	Operating Frequency	Power Consumption ( $\mu$ W)	Supply Voltage (V)	Number of Active elements	Number of Passive Elements	Type of Operation	Technology Used ( $\mu$ m)
[1]	250 KHz	-	$\pm 1.25$	2 CCII+4 MOS	0	Voltage mode	0.25
[2]	200 MHz	-	$\pm 5$	1OTA+2 MOS	1 Resistor	Voltage mode	0.5
[3]	4.5MHz	-	$\pm 1.5$	1CDBA+2Diodes	0	Voltage mode	0.25
[4]	100 MHz	4900	$\pm 2.5$	1 OTA+ 6 MOS	0	Voltage mode	0.5
[8]	20 MHz	-	$\pm 1.25$	4 CCCII+3 MOS	1 Capacitor	Voltage mode	0.25
[9]	100 KHz	-	$\pm 10$	2 CCII (AD844) + 18 BJT	2 Resistors	Voltage mode	-
[10]	30 MHz	-	-	2 CCII+4 Diodes	2 Resistors	Voltage mode	-
[11]	200 MHz	-	$\pm 5$	1 OTA+4 MOS	0	Voltage mode	0.5
[12]	300 MHz	-	$\pm 5$	1 OTA+4 MOS	0	Voltage mode	0.5
[13]	100 KHz	-	$\pm 2.5$	1 CCCII+2 MOS	1 Resistor	Voltage mode	-
[14]	100 MHz	1120	$\pm 1.5$	1 CDTA+ 2 MOS	1 Resistor	Multi mode	0.18
[15]	5 MHz	6310	$\pm 1.8$	1 CDTA+4 Diodes	2 Resistors	Current mode	0.35

[16]	5 MHz	-	±5	1 CDTA+2 Diodes	1 Resistor	Current mode	-
[17]	120 MHz	-	±2.5	2 DXCCII+2 Diodes	1 Resistor	Current mode	0.35
[18]	200MHz	930	±1.25	2 DVCCII+2 Diodes	2 Resistors	Voltage mode	0.25
[19]	100 KHz	2.14	+0.6	Bulk Drive WTA +Inverter	0	Voltage mode	0.18
[23]	1 MHz		±1.5	1 OTA +2 Diodes	2 Resistors	Current mode	0.25
Proposed	500 MHz	800	±0.75	1 FCS+2 Diodes	2 Resistors	Current mode	0.18

## 2. FLOATING CURRENT SOURCE AND CURRENT MODE RECTIFIER

The Floating current source was first introduced by [20] as an output stage for current mode feedback amplifiers. The FCS is basically a parallel connection of NMOS and PMOS differential pairs fed with their respective tail current sources as depicted in Fig. 1. The block diagram is given in Fig. 2. The circuit is completely current controlled as can be inferred from the Equations (1)-(3). The voltage at the different nodes of the FCS has no importance since they do not affect the operation. The applied input voltage is converted to corresponding currents by the action of the transconductors (MP1-MP2) and (MN1-MN2). Another important advantage of FCS is that the mismatch in the transistors does not affect the output currents. Furthermore, FCS is not affected by crosstalk due to power supply rails as the loop formed by the output currents does not include the power supply rails [20] this leads to high frequency operation.

$$I_1 = I_2 + I_{out+} + I_{out-} \quad (1)$$

$$I_1 = I_2 \quad (2)$$

$$I_{out+} = -I_{out-} \quad (3)$$

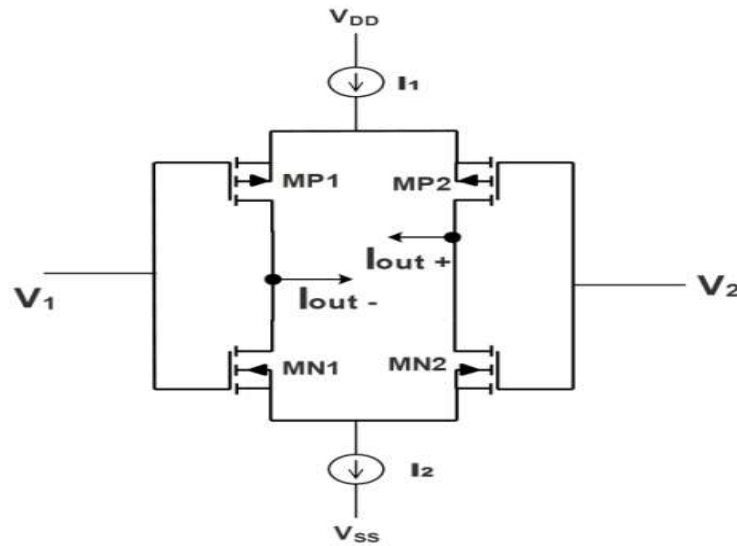


Fig.1. Block diagram of FCS

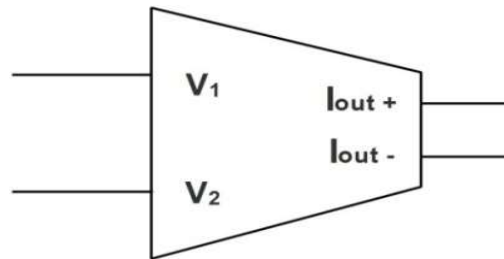


Fig.2. CMOS Implementation of FCS

If the sizes of the NMOS transistors  $MN_1$  and  $MN_2$  are made equal then their transconductance will also be identical ( $g_{mn1} = g_{mn2}$ ) in similar fashion for equal PMOS transistors  $MP_1$  and  $MP_2$  ( $g_{mp1} = g_{mp2}$ ) [21-22]. The small signal transconductance of FCS is given by Equations (4)-(5).

$$g_{meq.} = \frac{g_{mn1}g_{mn2}}{g_{mn1} + g_{mn2}} + \frac{g_{mp} g_{mp2}}{g_{mp1} + g_{mp}} \tag{4}$$

For ( $g_{mn1} = g_{mn}$ ) and ( $g_{mp1} = g_{mp2}$ )

$$g_{meq.} = \frac{(g_{mn1} + g_{mp1})}{2} \tag{5}$$

where  $g_{mi} = \sqrt{2\mu C_{OX} \frac{W}{L} I_i}$  ( $i=1$  to 4)

The block diagram and schematic of the proposed current mode full wave rectifier is presented in Fig. 3 (a)-(b). The rectifier consists of one FCS, two diodes and two grounded resistors. When a current signal to be rectified is applied to the rectifier the following events take place. During the positive half cycle, the diode D1 conducts the current while D2 remains

off. The current  $I_{in}(t)$  from D1 gets converted into the corresponding voltage ( $V_1$ ) by the grounded resistor  $R_1$ . The FCS then converts this voltage ( $V_1$ ) into corresponding output currents at its inverting and non-inverting outputs. During the negative half cycle, D1 is off while D2 conducts current  $-I_{in}(t)$ . The grounded resistor  $R_2$  converts the current into corresponding voltage ( $-V_2$ ) which is converted into rectified output currents. The two outputs of the FCS provide both inverting and non-inverting rectified output simultaneously imparting flexibility to the implementation.

During positive half cycle the output rectified current is given by Equation (6).

$$I_{out+}(t) = |I_{out-}(t)| = -\frac{1}{2}V_1 \left[ \sqrt{K_n} \sqrt{I_{B1} - \left(\frac{K_n V_1^2}{4}\right)} \right] + \sqrt{K_p} \sqrt{I_{B1} - \left(\frac{K_p V_1^2}{4}\right)} \quad (6)$$

During negative half cycle, the output rectified current is given by Equation (7).

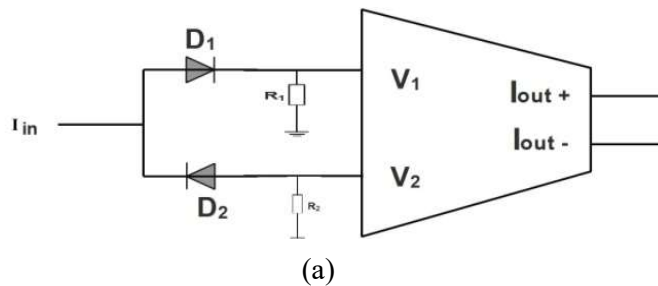
$$\begin{aligned} I_{out+}(t) &= |I_{out-}(t)| \\ &= -\frac{1}{2}(-V_2) \left[ \sqrt{K_n} \sqrt{I_{B1} - \left(\frac{K_n (-V_2)^2}{4}\right)} \right] \\ &+ \sqrt{K_p} \sqrt{I_{B1} - \left(\frac{K_p (-V_2)^2}{4}\right)} \quad (7) \end{aligned}$$

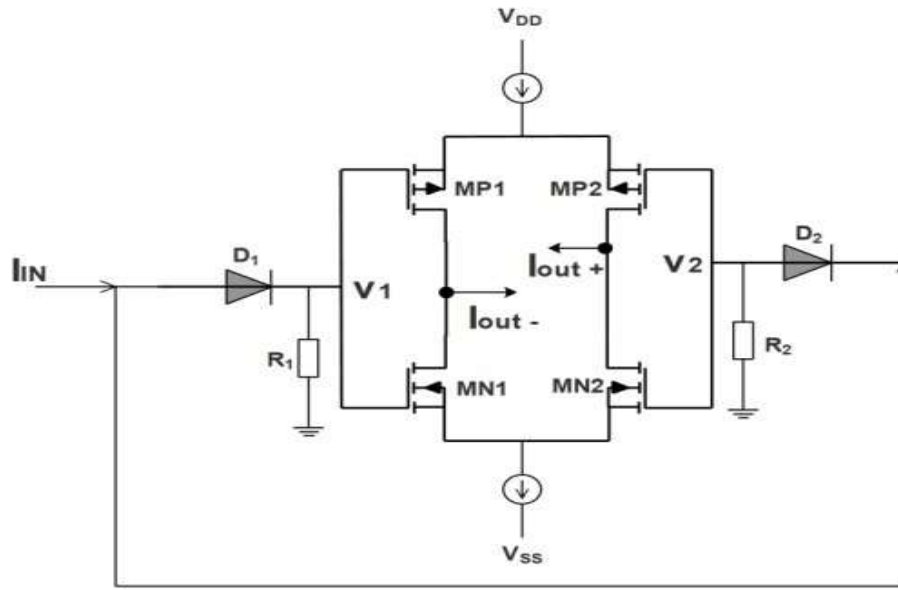
$$V_1 = I_{in}(t)R_1 \quad (8)$$

$$V_2 = -I_{in}(t)R_2 \quad (9)$$

$$K_n = \mu C_{OX} \frac{W_{n1}}{L_{n1}} \quad (10)$$

$$K_p = \mu C_{OX} \frac{W_{p1}}{L_{p1}} \quad (11)$$

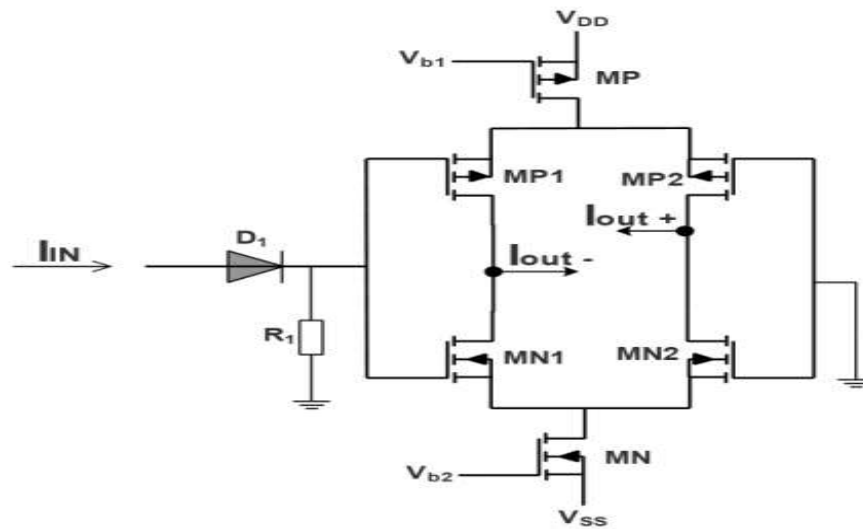




(b)

**Fig.3.** Full wave rectifier: a) Block diagram b) Circuit level implementation

If diode D2 and resistor R<sub>2</sub> are removed and second input node of the FCS is grounded, then the configuration will work as a half wave rectifier as shown in the Fig. 4. The circuit operation principle will remain the same as that of full wave rectifier.



**Fig.4.** Circuit level implementation of half wave rectifier

### 3. RESULTS NAD DISCUSSION

To prove the theoretical results the FCS is implemented in 0.18μm TSMC CMOS technology



and simulated in Hspice. The diodes used are general purpose 1N4148 diodes. The  $W/L$  ratios of the PMOS transistors are  $1.36\mu\text{m}/1.36\mu\text{m}$  and  $1.98\mu\text{m}/0.18\mu\text{m}$  for NMOS transistors. The bias currents are set at  $300\mu\text{A}$ , the supply voltage employed is  $\pm 0.75\text{V}$  and the resistors are fixed at  $2.2\text{k}\Omega$ .

The dc analysis of the rectifier is performed. An input current of  $\pm 100\mu\text{A}$  is applied at the inputs and the output currents are plotted as shown in Fig. 5. It can be deduced from the plot that the circuit exhibits distortion less zero crossings for both inverting and non-inverting outputs. To ascertain the rectifier performance at different frequencies, transient analysis was performed with a sinusoidal signal of  $\pm 100\mu\text{A}$  peak to peak at frequency of 1 MHz for inverting and non inverting outputs Fig. 6. To further validate the high frequency functionality of the rectifier, it was tested at 10 MHz, 100 MHz and 500 MHz the corresponding plots are given in Fig. 7 (a)-(c). It can be inferred from the plot that the rectifier performs well above 100MHz but as the frequency approaches 500MHz the zero crossing distortion increases, but it is still under acceptable range. Hence, the proposed rectifier can operate up to until a very high frequency of 500MHz. To study the rectifier's gain tuning capability, the rectifier was tested for a sinusoidal signal of  $\pm 100\mu\text{A}$  p-p at a frequency of 1MHz for different values of the resistors. It is evident from Fig. 8 that the gain can be varied without introducing distortion. The range of the maximum input current that can be processed by the FCS can be increased by increasing the biasing current at the expense of increased power dissipation.

The DC and transient analysis of the half wave rectifier is also performed at 500MHz as shown in Fig. 9 and 10. The rectifier performance at different values of input currents of  $40\mu\text{A}$ ,  $80\mu\text{A}$  and  $100\mu\text{A}$  is also tested. The results are illustrated in Fig. 11(a)-(b).

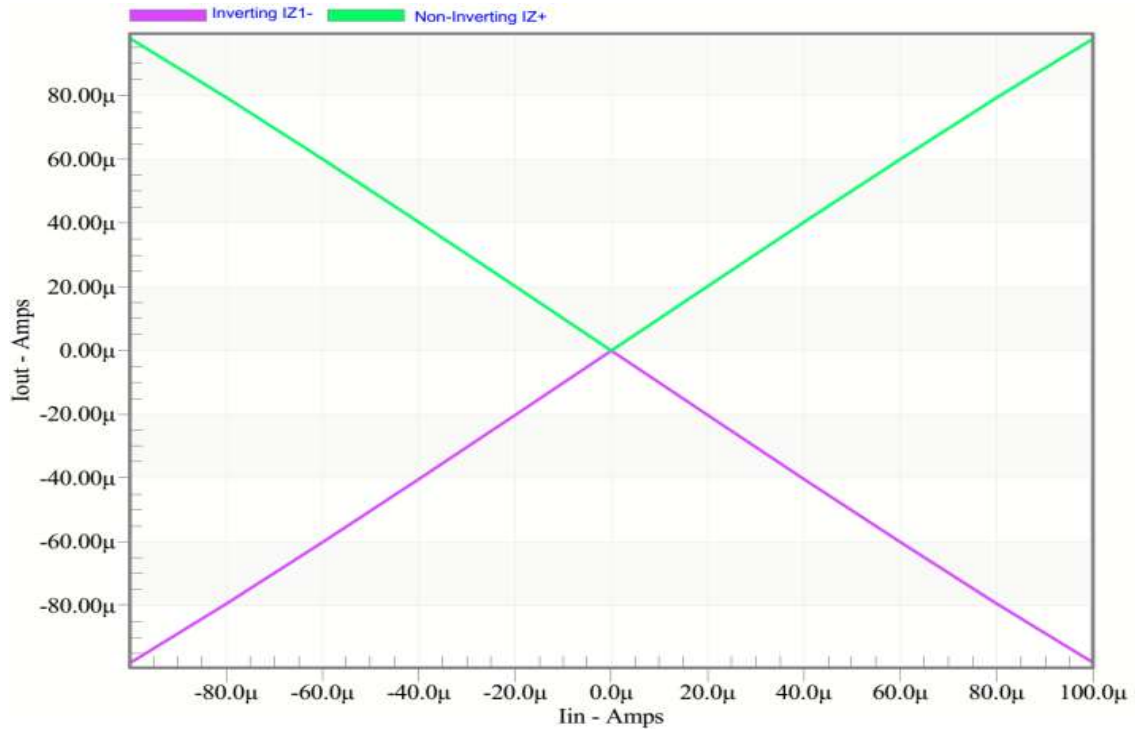
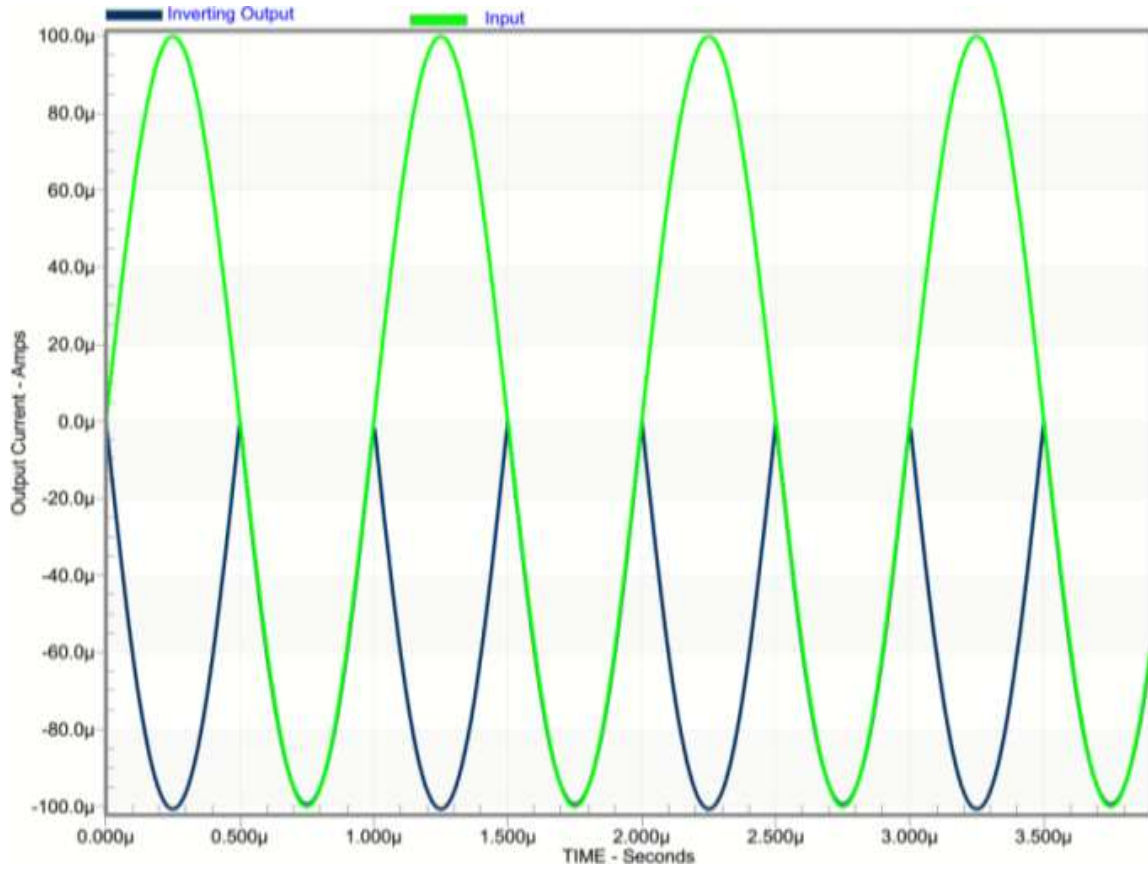
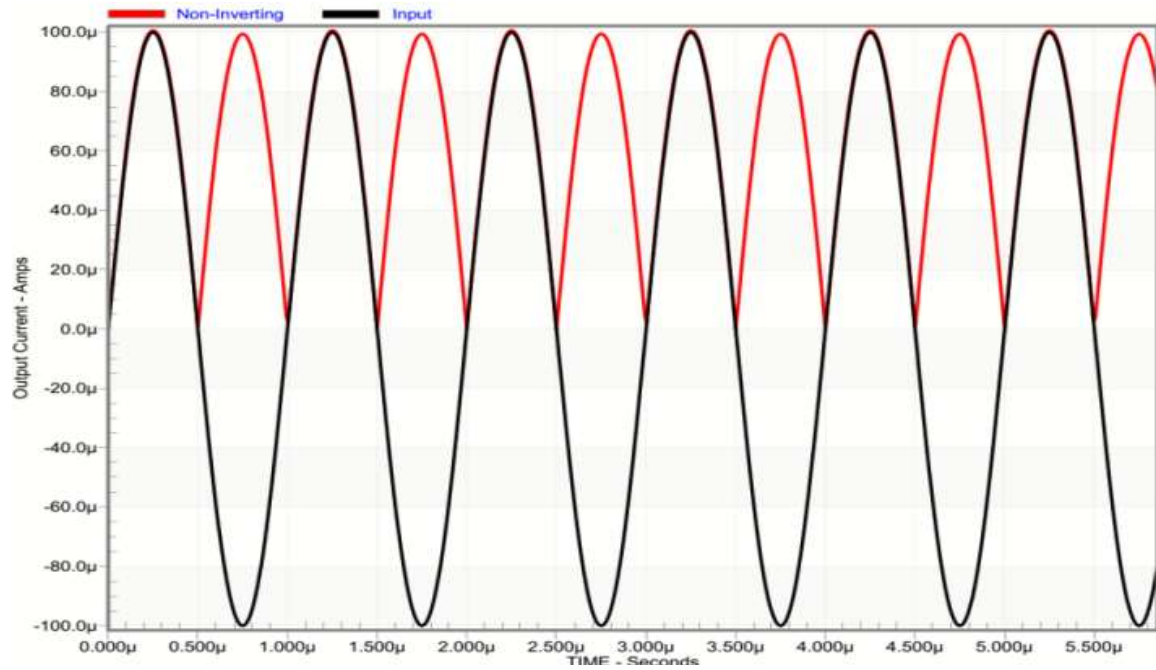


Fig.5. DC analysis of full wave rectifier for inverting and non-inverting output

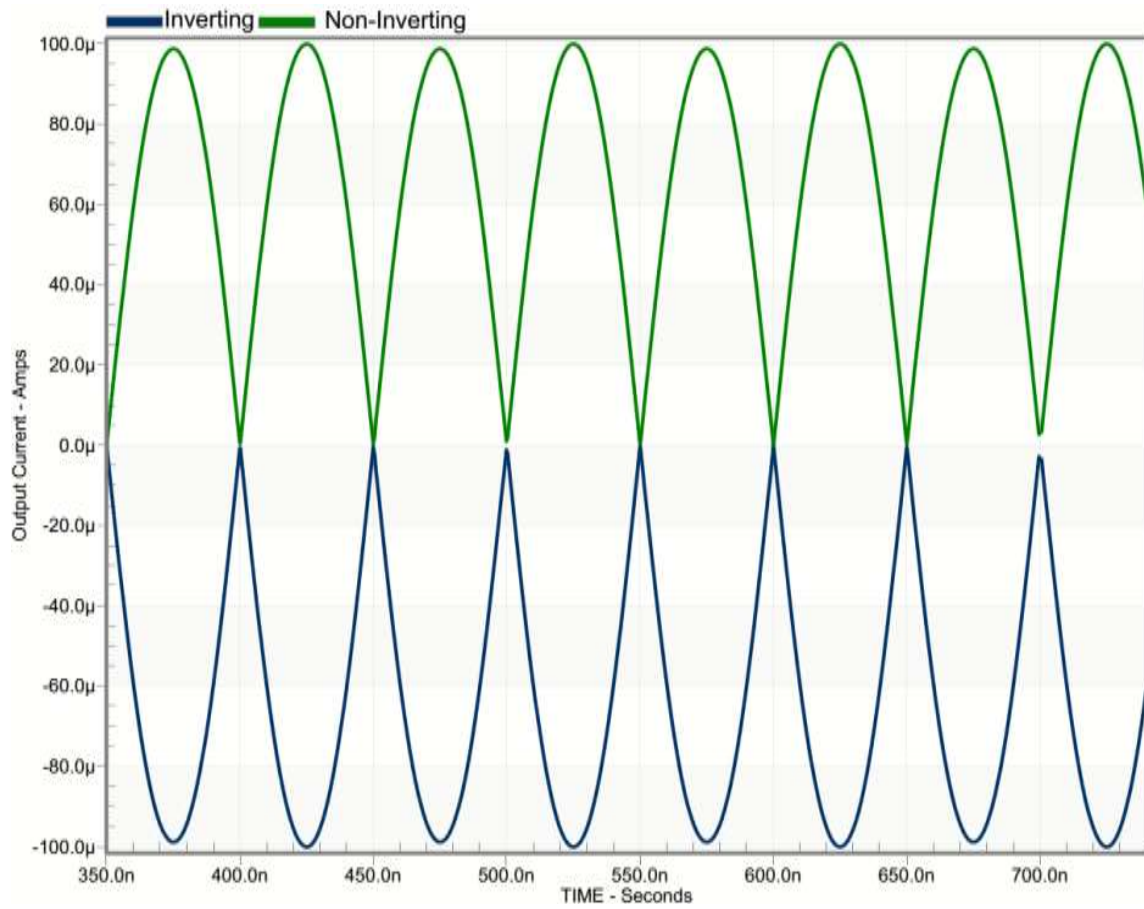


(a)

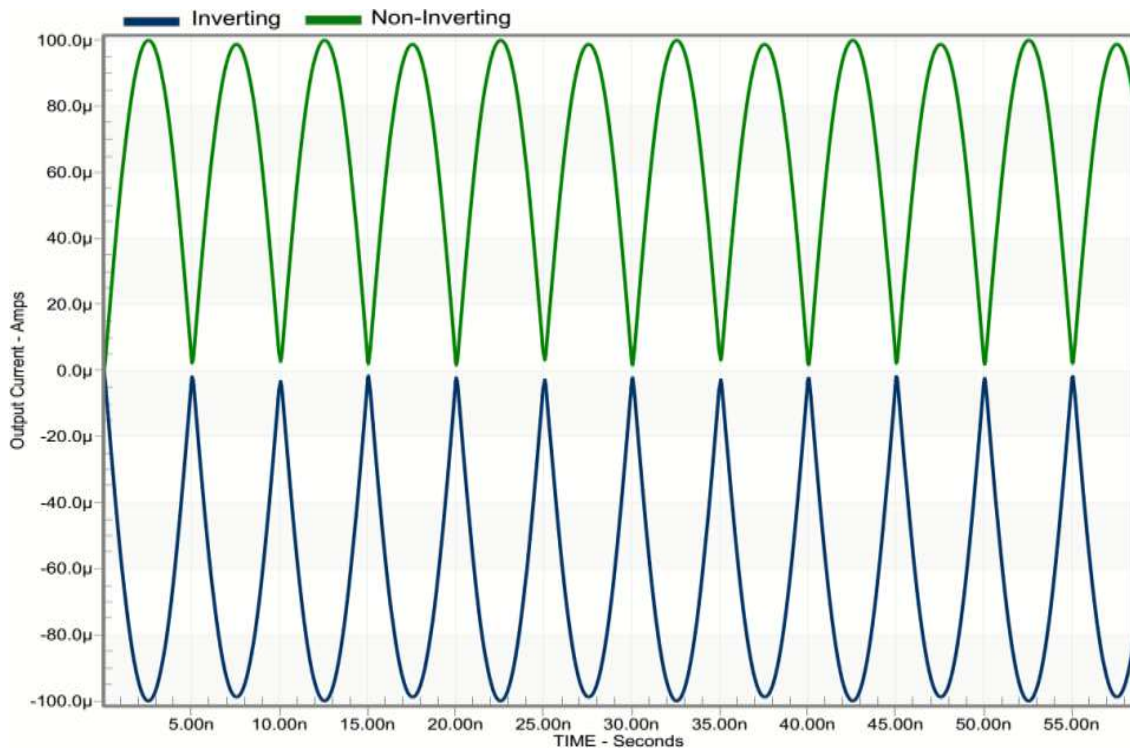


(b)

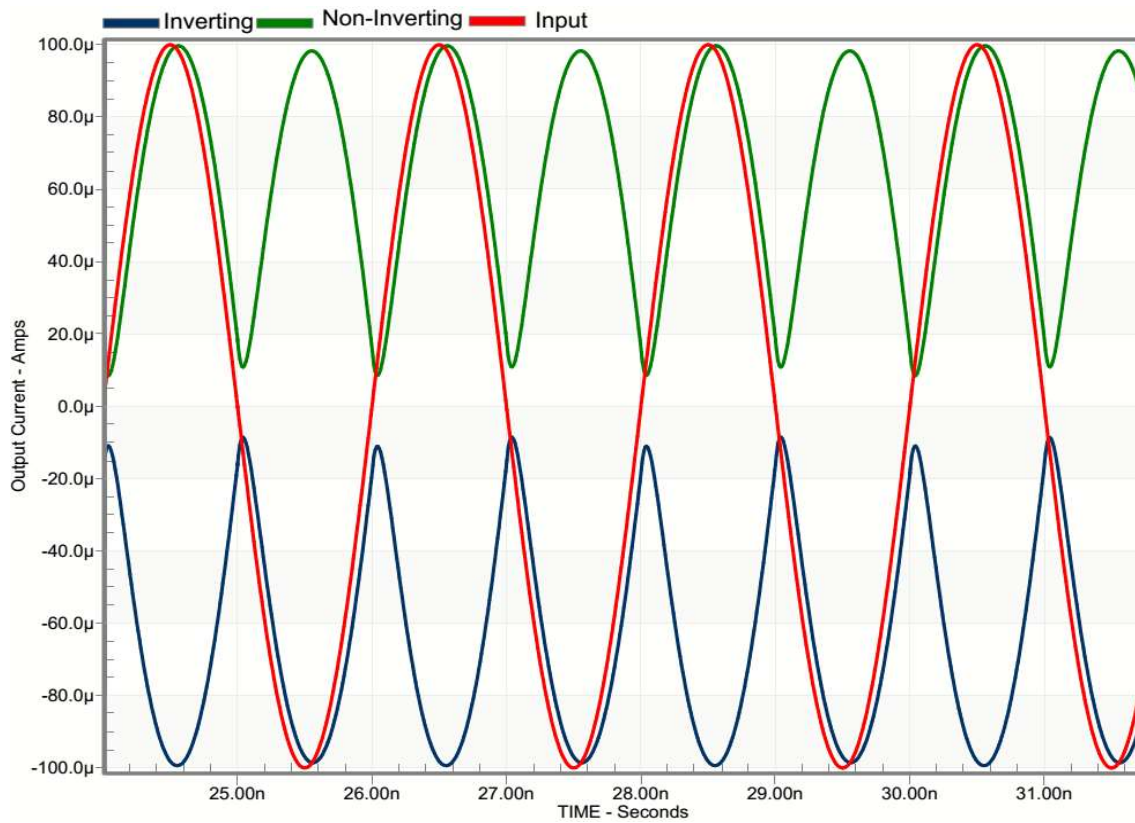
Fig.6. Rectified output current of the rectifier at: 1 MHz a) Inverting b) Non-inverting



(a)



(b)



(c)

Fig.7. Rectified output current of the rectifier for: a) 10 MHz b) 100 MHz c) 500 MHz



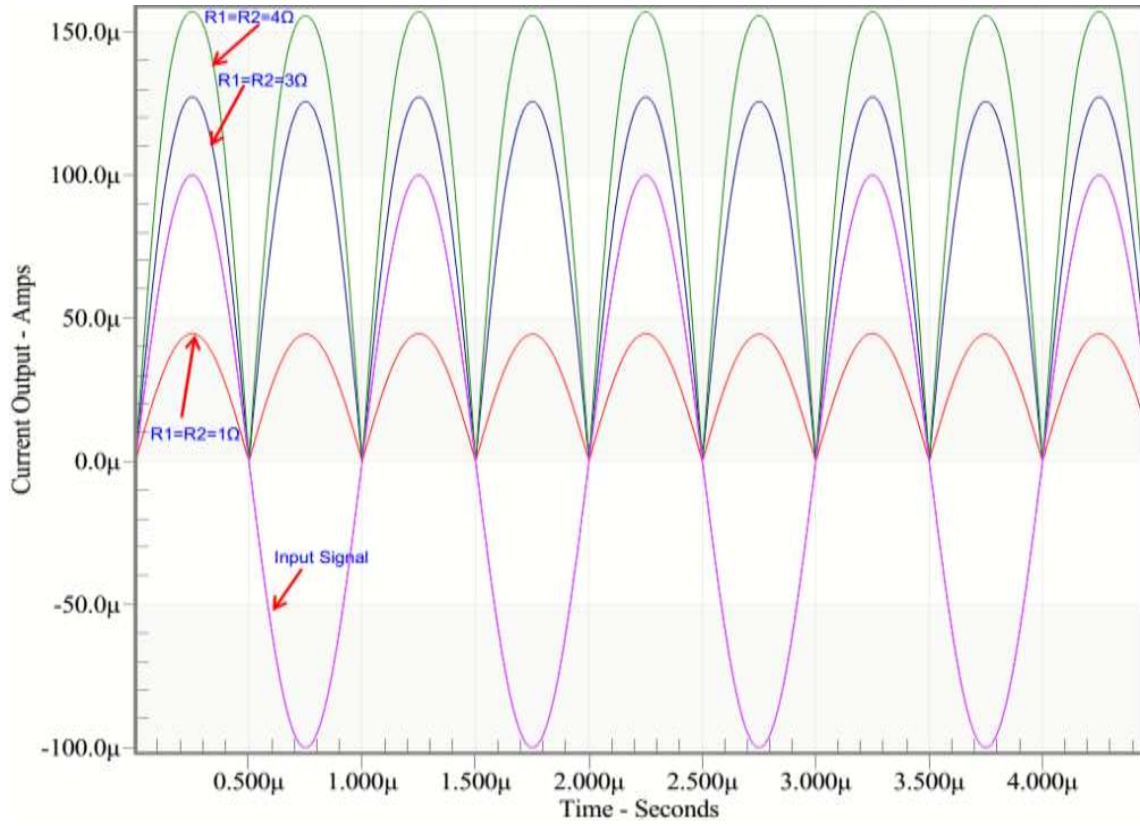


Fig.8. Rectified output for different values of load resistance

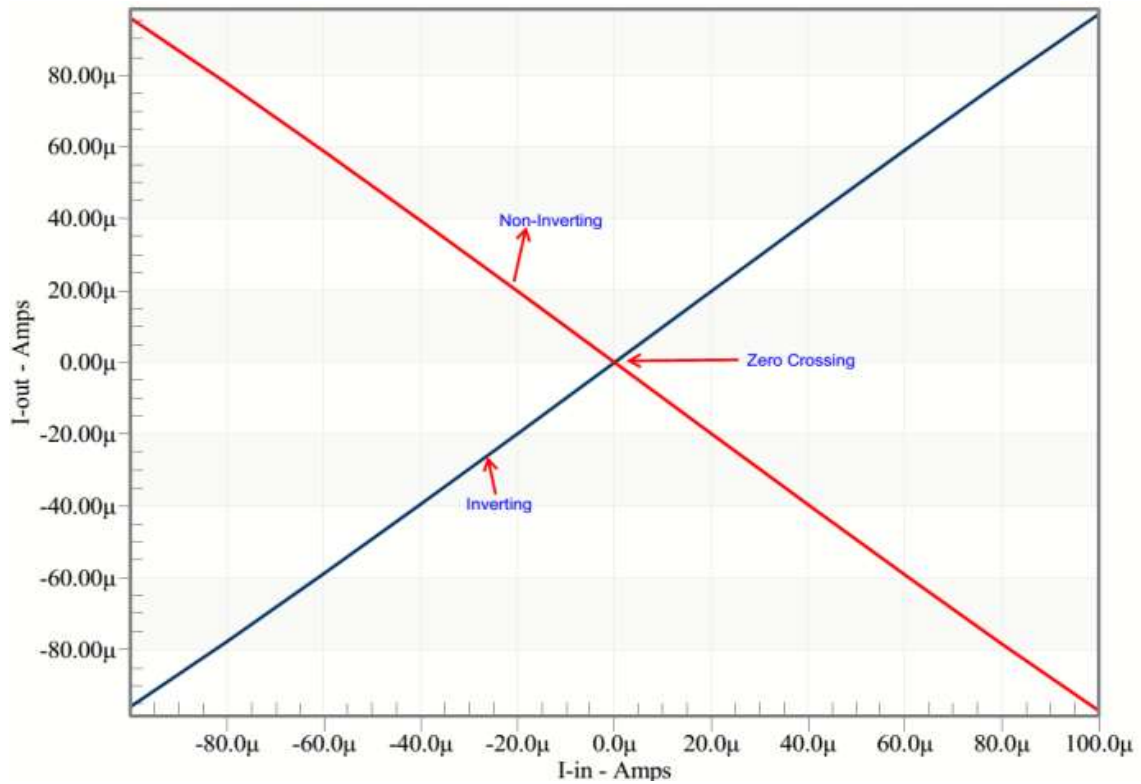


Fig.9. DC analysis of half wave rectifier

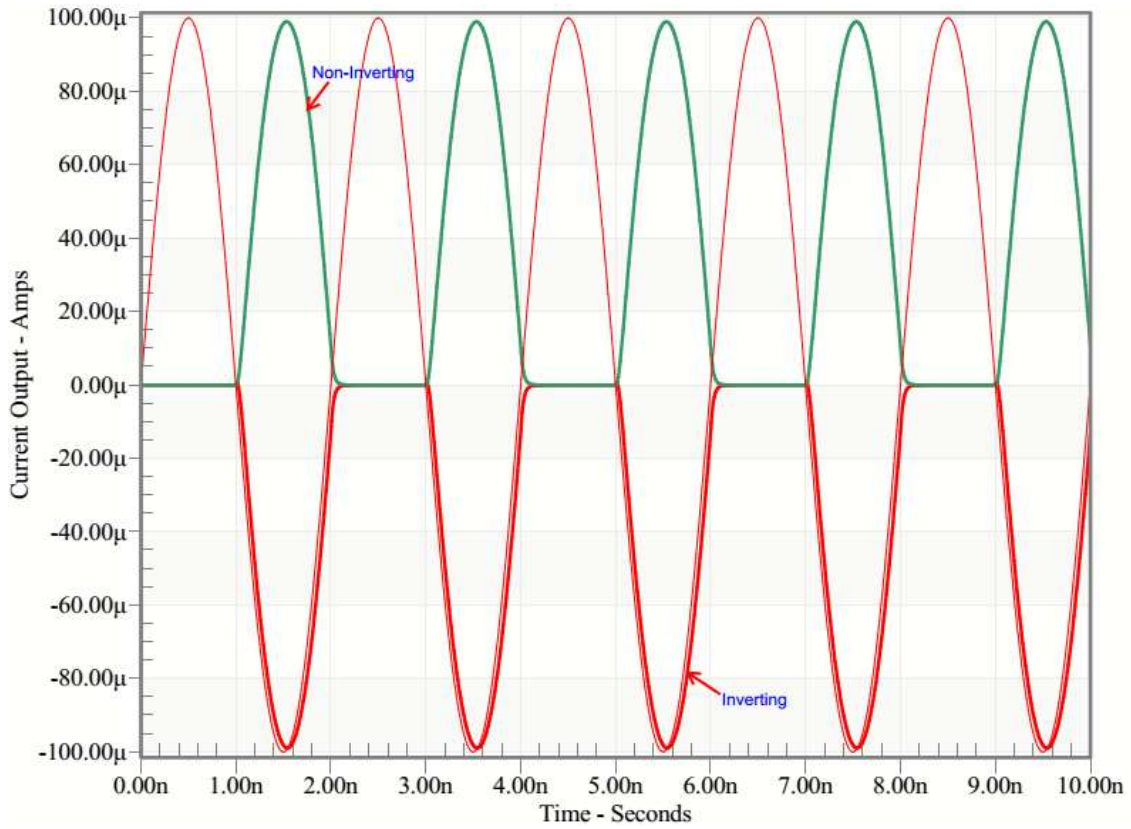
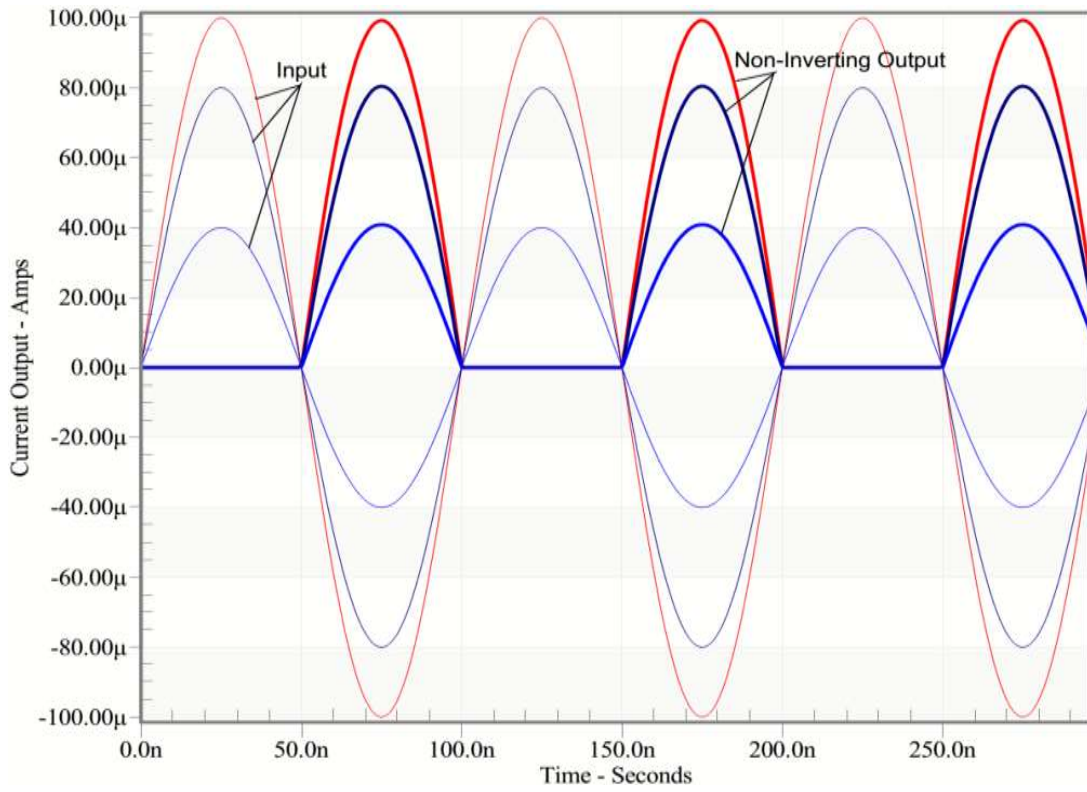
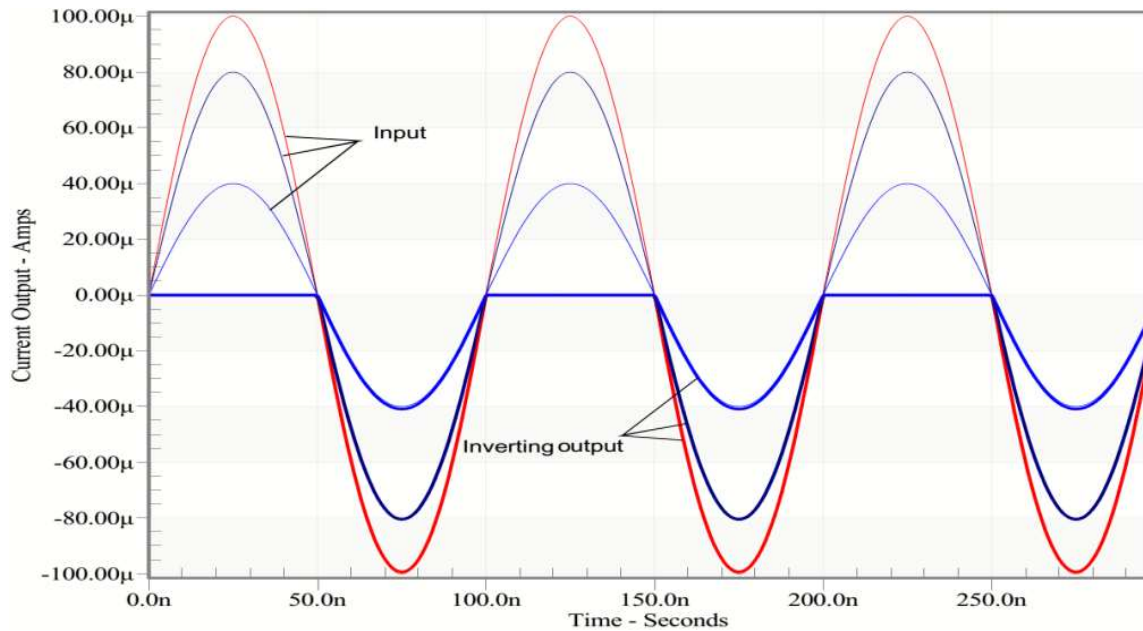


Fig. 10. Rectified output current of the half wave rectifier for 500 MHz



(a)



(b)

**Fig.11.** Rectified output current of the rectifier for different input current amplitudes of  $40\mu\text{A}$ ,  $60\mu\text{A}$  and  $100\mu\text{A}$ : a) Non-Inverting output b) Inverting output

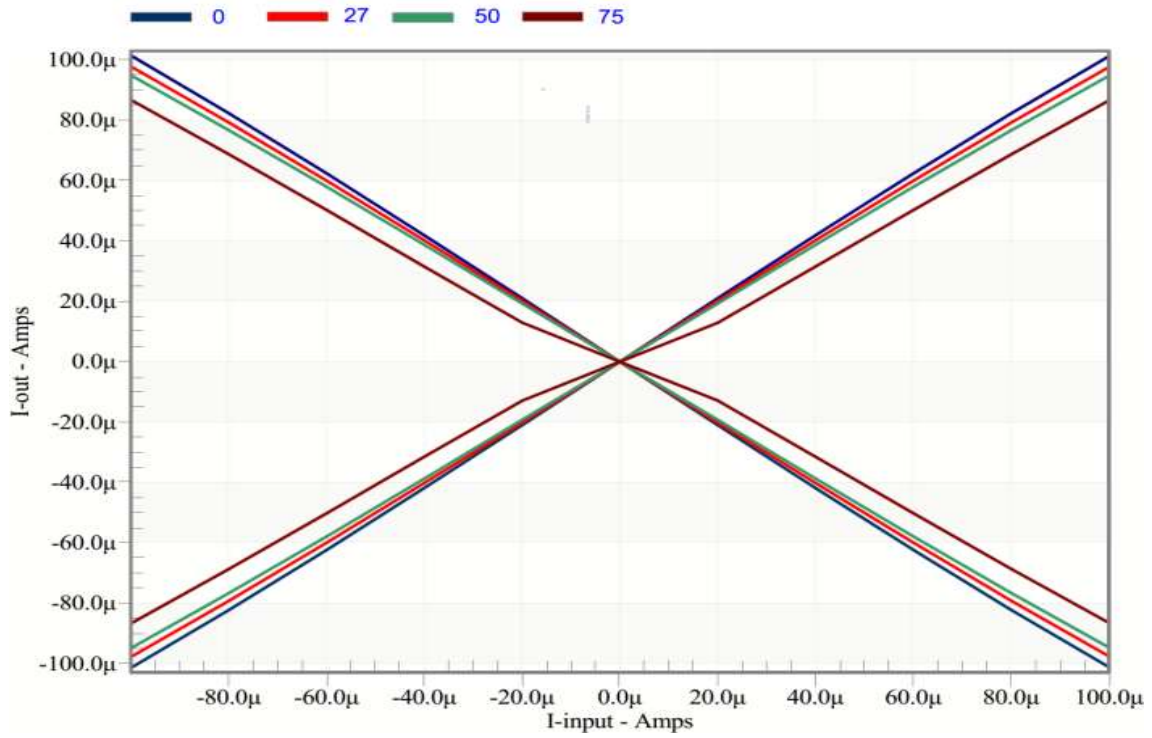
#### 4. EFFECT OF TEMPERATURE

To study the effect of the temperature on the proposed rectifier the simulations were performed for four different temperatures of  $0^\circ\text{C}$ ,  $27^\circ\text{C}$ ,  $50^\circ\text{C}$  and  $75^\circ\text{C}$ . The DC characteristic and the rectified output voltage for the full wave rectifier at 10 MHz are presented in Fig. 12 and 13. It can be inferred as the temperature increases the DC characteristics show a spread and reduced linear range with marginal increase in the zero crossing distortion showcasing its good temperature stability. Moreover, the transient analysis reveals that amplitude of the rectified output decreases with temperature. The FCS is transconductance based active block so the dependence of  $g_m$  on temperature affect the rectifier performance [22]. The expression of the  $g_m$  as given in Equations (12)-(13) reveals that the two temperature dominated parameters are the mobility ( $\mu$ ) and the threshold voltage ( $V_T$ ) of the MOS transistors. The  $V_T$  changes by  $-2.4\text{mV}/^\circ\text{C}$  with increasing temperature while, the mobility decreases with temperature by about 1.5%. Hence, the effect of mobility degradation predominates leading to decrease in the transconductance. This is validated by the simulation results. The threshold voltage of the diode is also sensitive to temperature

contributing to the decrease.

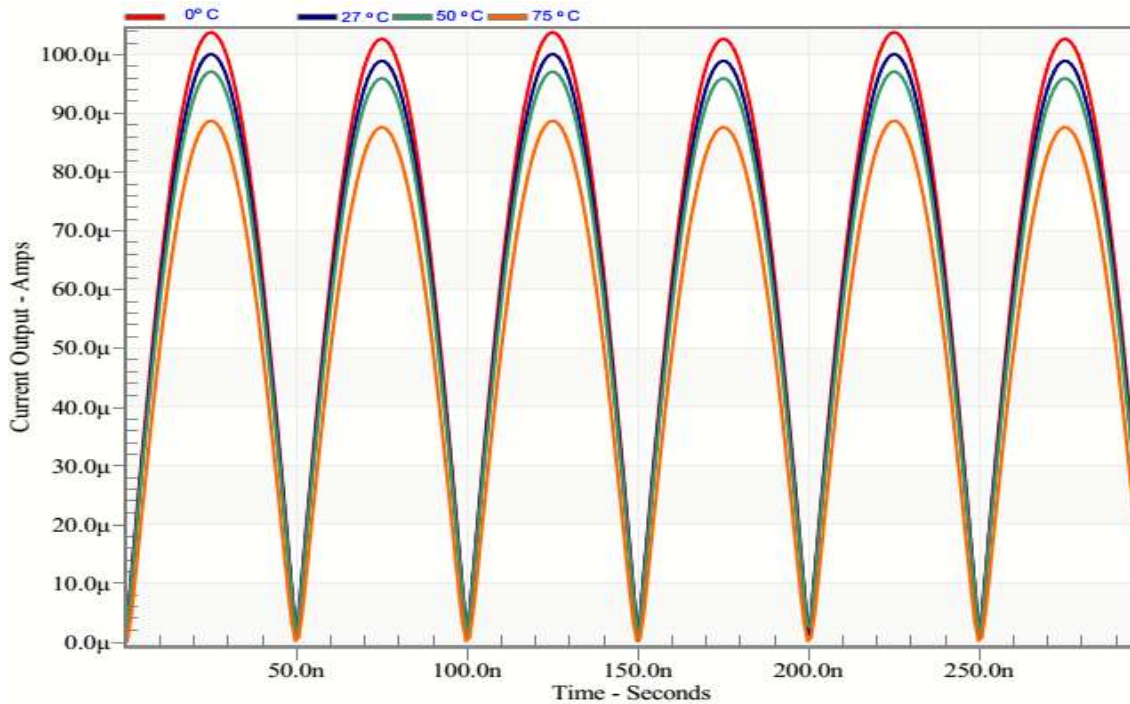
$$g_m = \mu_n \frac{W}{L} C_{OX}(V_{GS} - V_T) \tag{12}$$

$$\mu(T) = \mu(T_o) \left(\frac{T}{T_o}\right)^{-1.5} \tag{13}$$



**Fig.12.** Temperature stability analysis of the DC characteristics of the full wave rectifier





**Fig.13.** Rectified output current of the rectifier for different temperatures

### 5. NON-IDEAL ANALYSIS OF THE RECTIFIER

The distortion in the rectified signal can be attributed to three dominant non-idealities present in the circuit [23]. First, the transconductance transfer error  $g_m = g_o(1 - \varepsilon_{gm})$  of the FCS where  $\varepsilon_{gm}$  is the transconductance tracking error and  $g_o$  the DC transconductance gain. Second, the mismatch between the load resistances ( $\varepsilon_r$ ) and third, the parasitics present in the FCS. The parasitic capacitance limits the frequency performance of the rectifier. The effect of transconductance mismatch is modelled by Equation (14). While, the combined effect of all the non-idealities are modelled by Equations (15)-(19).

$$I(t)_{out} = |I(t)_{out-}| = g_m R_{eq} |I(t)|_{in} = [g_o(1 - \varepsilon_{gm})] R_{eq} [|I(t)|_{in}] \tag{14}$$

$$R_2 = (1 - \varepsilon_r) R_1 = R_{eq} \tag{15}$$

$$Z_1 = R_1 || R_p || 1/sC_p \tag{16}$$

$$Z_2 = (1 - \varepsilon_r) R_1 || R_n || 1/sC_n \tag{17}$$

$$I_{out+} = g_o(1 - \varepsilon_{gm}) [R_1 || R_p || 1/sC_p] |I(t)|_{in} \tag{18}$$

$$I_{out-} = -g_o(1 - \varepsilon_{gm}) [R_1(1 - \varepsilon_r) || R_n || 1/sC_n] |I(t)|_{in} \tag{19}$$

## 6. CONCLUSION

A simple high frequency full wave current mode rectification circuit employing only a single floating current source, two diodes and two grounded passive resistors is proposed. The current mode rectifier works at a low voltage supply of  $\pm 0.75\text{V}$  and exhibits a low power dissipation of  $800\mu\text{W}$ . The circuit is capable of operating satisfactorily up to a frequency of 500 MHz and provides simultaneously the inverting and non-inverting outputs. It is also shown that with a single diode and a grounded resistance the circuit can effectively work as a half wave rectifier. The minimum component rectifier circuit is simulated in  $0.18\mu\text{m}$  TSMC CMOS technology in Hspice to validate the theoretical assumptions. The effect of non-idealities and temperature on the circuit performance is also studied.

## 7. ACKNOWLEDGEMENTS

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