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# A NOVEL METHOD TO DESIGN VARIABLE GAIN AMPLIFIER

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## ABSTRACT

A novel method to design of Variable gain Amplifiers (VGAs) is proposed. A low power VGA with wide range of gain variation and appropriate bandwidth using new technique is presented in this paper. Moreover, the suggested circuit is simulated in whole process corners and different temperatures in the region of -50 to +70 ºC. The circuit has been designed in a typical 0.35µm CMOS process with a power supply of 3.3V, and simulated by HSPICE software using level 49 parameters (BSIM3v3).

**Keywords:** variable gain amplifier; Operational Transconductance Amplifier; wide gain range; low power; unity gain bandwidth.

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## 1. INTRODUCTION

Variable Gain Amplifiers (VGAs) play a significant role as an analog building block in systems like, disk drives, wireless communication links, signal processing chips and data converters [1]. In a disk drive, a VGA helps to stabilize the voltage supplied to the detector and filter section of a read channel or in wireless communication systems, there is a great deal of variation in received signal strength due to channel fading which should be compensated

using VGA. Fundamentally, the VGA is used in an AGC loop and the loop adjusts the gain of the VGA to produce stable output signal amplitude [2]. Meanwhile, the VGA is very useful module in Radio Frequency (RF) applications in where it serves as a universal purpose gain block to adjust the overall gain of a transceiver which may be affected from manufacturing tolerances or other blocks influence in the system. Some of VGAs use a fixed gain amplifier followed by a variable attenuator to control the gain [3]. In other works, the main amplifier parameters are supposed to change. This paper is organized as follows: in section 2; conventional design is presented. Different Operational Transconductance Amplifiers are stated in section 3; Proposed Method to Achieve Variable Transconductance is indicated in section 4; in section 5 the Proposed Variable Gain Amplifier Circuit is presented; Simulation results are conferred in section 6; and finally section 7 concludes the paper.

## 2. CONVENTIONAL DESIGN

Conventionally, different methods are utilized to design variable gain amplifier. One of the popular structures is Programmable Gain Amplifier (PGA). Using capacitor and resistor arrays in the feedback path of an op-amp, PGA creates some digital gain levels.

Generally, gain variations could be achieved through variation in amplifier Transconductance or its output resistance. For a MOS Differential Pair (DP) operating in saturation region having tail current source changed leads to alter in DP Transconductance [4].

Equations (1) and (2) demonstrate the concept.

$$g_{m=}\sqrt{(2\times KP\times (W/L)\times I_{bias}} \quad (1)$$

$$A_v = G_m \times R_{out} \quad (2)$$

Where Av, Rout and $g_m$ are DC gain, output resistance and corresponding Transconductance of the amplifier respectively and $I_{bias}$ represents the tail current source.

As an instance, according to (1) a 30dB change in the gain requires a dramatic change in bias current about 1000 times. The larger current means the more power consumption, especially for high output dynamic ranges.

Moreover, a MOS transistor operating in linear region between the output nodes may be used to have a variable resistance at the output nodes.

On the other hand, the achievable gain range is one of the important parameters of the VGA. Typical values for this parameter may vary from 0 dB to 40dB. Beside a wide gain range, there are some other issues such as, high noise immunity, low 3rd-order (IM3) distortion, and required bandwidth which should be addressed. To achieve high linearity, the first rational choice may be the negative feedback structure. However, the limited speed of CMOS process compared to that of BiCMOS or BJT technologies may obscure this approach. Using open-loop structures may satisfy speed requirements but has several issues to be settled down. First, the gain of the amplifier needs to be stabilized within a certain range (±3dB). Though the gain requirement for the amplifier is not very tight, it should not vary too much over process variations and temperatures, which is usually the case if the gain of the amplifier depends on the Transconductance of the devices. Second, the amplifier needs to be linearized out of MOS transistors' inherently nonlinear characteristics. This is more problematic in modern small-feature size processes that pose more short-channel effects and deviate from the classic square-law equation [5,6].

## 3. DIFFERENT OPERANTIONAL TRANSCONDUCTANCE AMPLIFIERES

Among numerous analog circuits, Operational Transconductance Amplifier (OTA) plays a significant role in different systems. It is an important building block of almost all analog and mixed-mode circuits, such as switched-capacitor filters and data converters. OTA is basically an op-amp without an output buffer which is used to drive large capacitive loads. Some of its main characteristics are Gain, Unity Gain Bandwidth, Phase margin, Output swing, Slew rate, CMRR, and PSRR. Single stage fully differential op-amps are usually used to attain higher unity gain frequency owing to their fewer number of poles compared to that of the multiple stage op-amps. Since in single stage amplifiers wholly expected gain is to be achieved in one stage, cascode structure would be a choice to get higher gain. Telescopic cascode and folded cascode structures are two known instances.

In order to achieve high gain, as discussed, the differential telescopic topology can be used. The telescopic architecture is a candidate for a low power, low noise and high gain OTA [7]. The performance of simple telescopic OTA is limited by its input and output voltage swing.

However, it provides high gain as well as high speed. As a result, this structure is not good idea for systems with low supply voltages. In order to surmount some drawbacks of telescopic operational amplifier, a folded cascode OTA can be used. Although it consumes more power compared to telescopic cascode, it provides higher output swing. Additionally, this structure sustains high gain and bandwidth as well as convenient voltage headroom for systems with low supply voltages [8]. Furthermore, it allows choosing proper overdrive voltage of transistors to achieve desired unity gain frequency, without affecting the output swing. Also, it is easy to frequency compensate a folded cascode op-amp (the load capacitor operates as compensation capacitor too) rather than a two stage op-amp. In this paper PMOS transistors are used at the input stage of the op-amp thanks to lower noise, body effect elimination, by connecting the body to the source terminal in the n-well technology, and covering negative rail (or ground) by single supply [9].

## 4. PROPOSED METHOD TO ACHIEVE VARIABLE TRANSCONDUCTANCE

This section is dedicated to explain the proposed idea. Initially the basic concept of the variable gain amplifier is illustrated briefly. Then on the basis of some figures and equations the suggested idea for VGA is outlined. According to Fig.1 the output branches' current is calculated as [10].

$$\Delta id = \frac{1}{2}\mu_n C_{OX}\frac{W}{L}(\Delta vin)\sqrt{\frac{4I_{SS}}{\mu_n C_{OX}\frac{W}{L}}} \quad (3)$$

$$\Delta id = I_{D_1} - I_{D_2} \quad (4)$$

$$\Delta vin = vin1 - vin2 \quad (5)$$

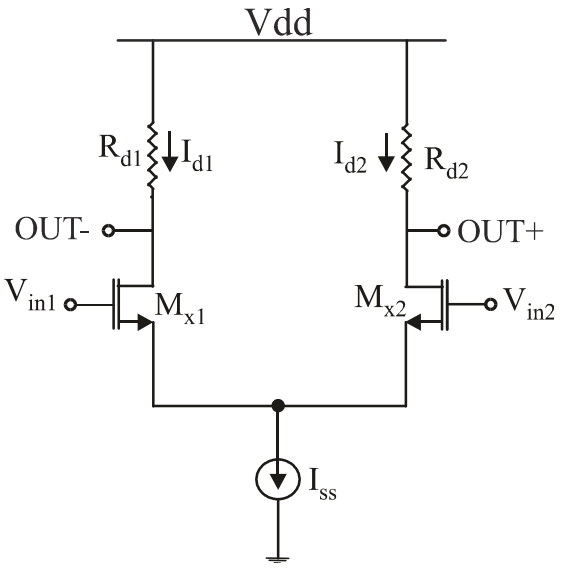


**Fig.1.** A simple differential pair amplifier

Where Δid and Δvin are the differences of the output branches 'current and the input nodes' voltage respectively.

As equation (3) shows Δidis depend on both Δvin andIss. As a result, there are two approaches to attain a variable current at the output nodes. In the common method the output current is changed through altering the bias current. A simple illustration of this method is depicted in Fig.2 where $V_c$ is used to modulate tail current in order to generate variable transconductance.

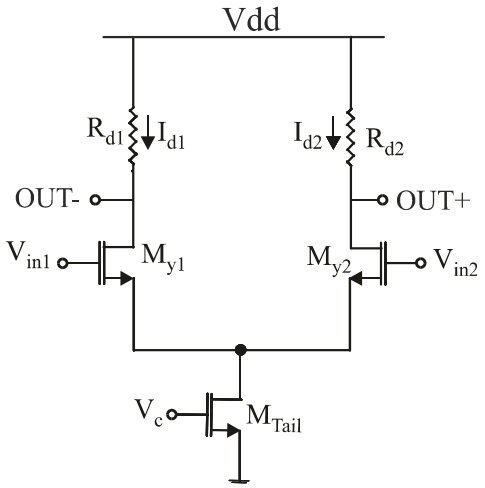


**Fig.2.** A simple differential pair amplifier with variable bias current

As Fig.3 shows that there is initial relationship between the differential output current and

input voltage. Accordingly, modifying $\Delta v$ will cause variation in$\Delta id$. To exploit this advantage in the proposed scheme, input signal is applied in current mode. Therefore, as Fig.4 shows to realize this notion, an ac current source which is to represent the output of Transconductance stage is added in parallel with the tail current source. Furthermore, Fig.5 summarises what has been discussed. To make the notion clear, equation (3) is manipulated by replacing IsswithG$_{m\ vin}$.

$$\Delta \text{vin} = V_c - V_{bias} \tag{6}$$

$$\text{Iss} \longrightarrow \text{Iss} - G_m v_{in} \tag{7}$$

the overall transconductance of the system $G_m$ can be rewritten as (8).

$$G_m = \frac{\partial \Delta I_D}{\partial \Delta V_{in}} = \frac{1}{2}\mu_n C_{OX}\frac{W}{L}\frac{\frac{4(Iss-G_{m\ vin})}{\mu_n C_{OX}\frac{W}{L}} - 2(V_c - V_{bias})^2}{\sqrt{\frac{4(Iss-G_{m\ vin})}{\mu_n C_{OX}\frac{W}{L}} - 2(V_c - V_{bias})^2}} \tag{8}$$

where $V_c$is applied as a control voltage on some devices to achieve a variable gain . Iss is bias current and $G_m v_{in}$ is the output current of the input transconductance stage.

Equation (8) clarifies that $G_m$ is depending on $(V_c - V_{bias})$ and claims a variable transconductance. What has been argued is a general method and it may be applied on different platforms. As an example, in the next section this method is used on a folded cascode op-Amp to create a variable gain amplifier.

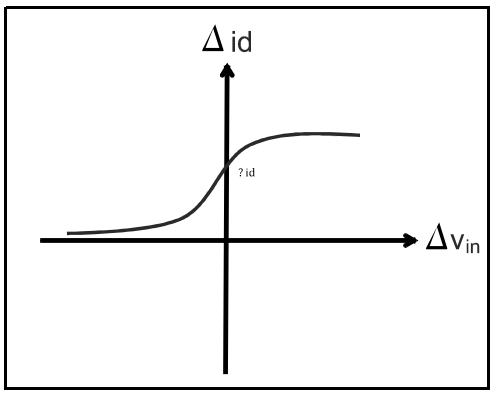


**Fig.3.** Relation of the Δid and Δvin

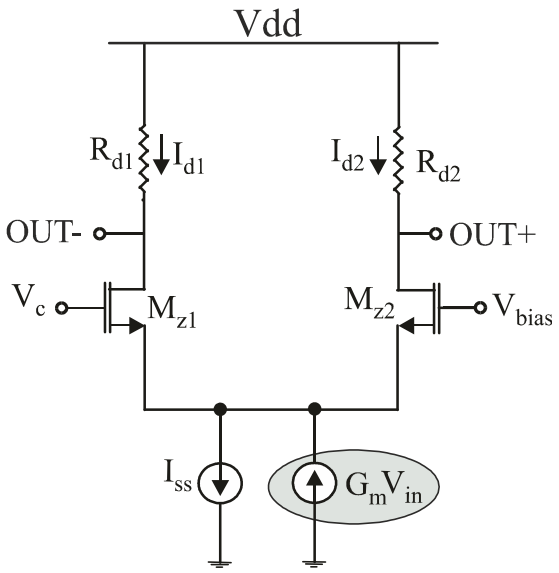


**Fig.4.** A differential pair amplifier which input signal is applied in current mode

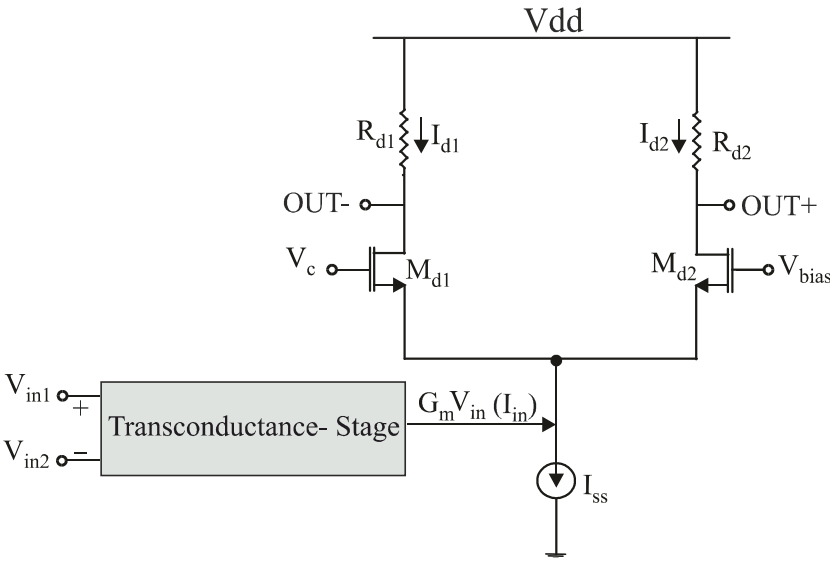


**Fig.5.** The output of the transconductance stage is added in parallel with the tail current source.

## 5. PROPOSED VARIABLE GAIN AMPLIFIER CIRCUIT

The proposed variable gain amplifier circuit is shown in Fig6.

The main purpose of the proposed structure is to transfer a portion of the output current of the transconductance stage to the output nodes. Also, according to the previous section (4) the overall Gm of the amplifier is controlled by external voltage ($V_c$) which is applied to current source transistors M1 and M2. Since in the proposed structure the gain of the amplifier is

controlled by adjusting the newly added differential pair's $\Delta v$ (M1-4), the amplifier's gain is independent of the output signal's magnitude. Furthermore, the suggested structure is so efficient in some parameters such as DC gain, unity gain bandwidth. In the proposed simple circuitry just by altering the control voltage ($V_c$) in M1 and M2 it is possible to obtain wide range of DC gain (0dB-47dB) and fine unity gain bandwidth. Also, with varying the size of the M1 and M2 it is possible to achieve negative gain too. Besides, the resistors R1 and R2 are placed to achieve wide range of control voltage ($V_c$), to maintain M1 and M2 in the saturation region, and to obtain positive gain of the proposed circuit, in case that negative gain is not desired. Meanwhile, it is obvious that by using a positive feedback circuit at the output, gain range would be increased. Consequently, the proposed circuit brings about features like wide gain range with acceptable linearity, suitable bandwidth, and possibility to reach both positive and negative gain all together.

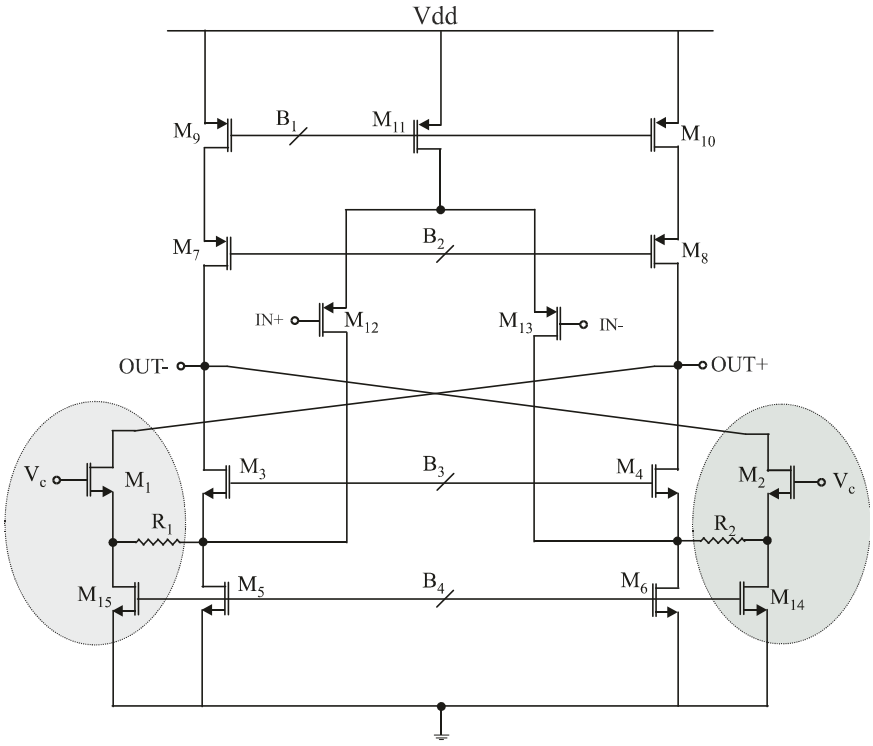


**Fig.6.**The proposed VGA circuit

## 6. SIMULATION RESULTS

In this section, simulation results of the proposed variable gain amplifier are shown. The circuit has been designed in a typical 0.35µm CMOS process with a power supply of 3.3V,

and simulated by HSPICE software using level 49 parameters (BSIM3v3). Fig.7 shows the ac simulation of the proposed VGA for $V_c$ in which it reaches maximum gain. Also unity gain bandwidth of the amplifier is presented in Fig.8; the diagrams of the $A_v$ versus $V_c$ and temperature are sketched using MATLAB in Fig.9 and Fig.10 separately. The DC gain, power consumption, and Unity Gain Bandwidth (UGBW) are given in Table.1 for all corners and within temperatures in the region of -50 to 70 ºCf. In the meantime, to avoid complexity, the temperature is not included in the table and only results of the worst case temperatures are shown. Table.2 performs a comparison between the proposed scheme and previous works.

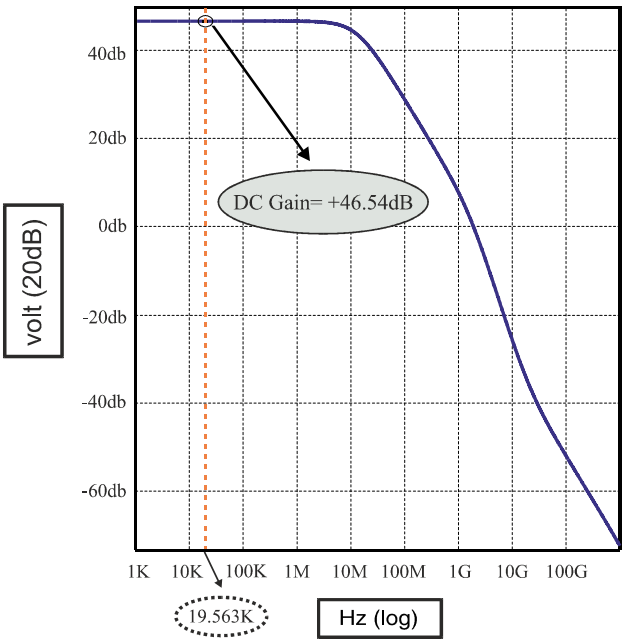


**Fig.7.** Ac simulation for maximum gain

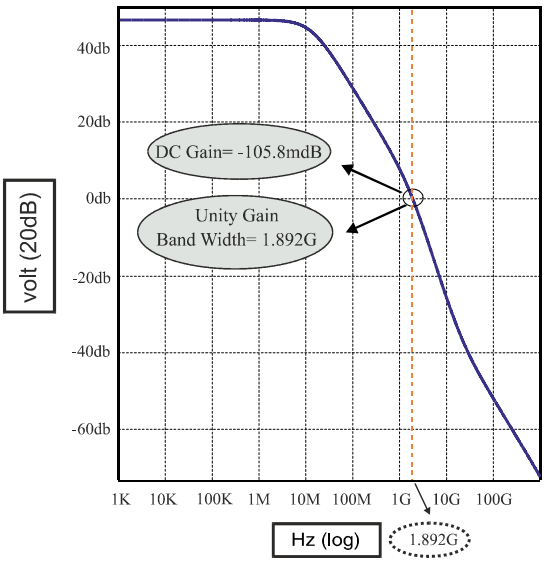


**Fig.8.** Unity gain bandwidth of the amplifier in TT corner.

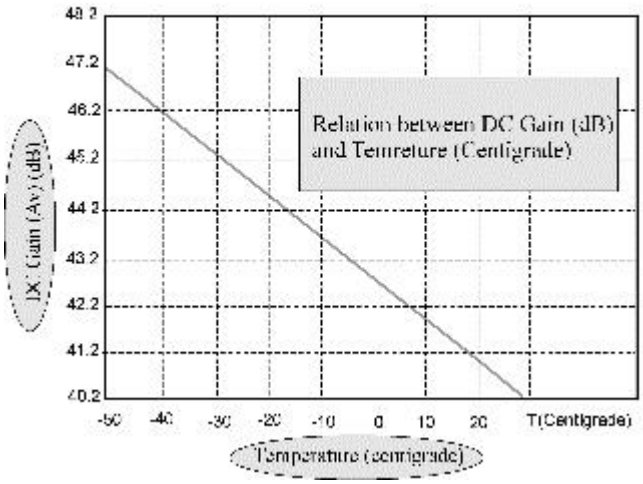


**Fig.9.** $A_v$ vs. T in TT corner

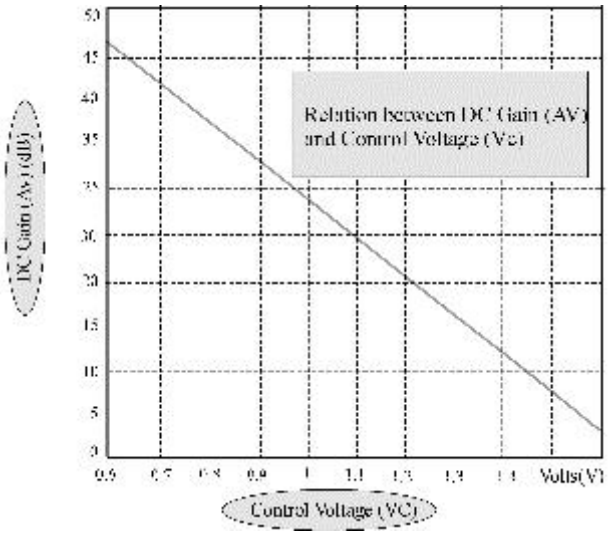


**Fig.10.** $A_v$ vs. $V_c$ in TT corner

**Table 1.** The results of the Dc gain, power consumption and Unity Gain Bandwidth (UGB)

| **Parameters** | **TT** | **SF** | **SS** | **FF** |
|---|---|---|---|---|
| **Vc(v)** | 0.78 | 0.9 | 0.9 | 0.68 |
| **Av (dB)** | 46.54 | 46.26 | 46.3 | 44.36 |
| **UGBW(GHz)** | 1.89 | 1.93 | 1.8 | 2.55 |
| **Power(mw)** | 8.78 | 9 | 8.49 | 11.1 |

**Table 2.** Comparison of VGA performance

| **Ref.** | **Tech.** | **-3dB bandwidth(MHz)** | **power** | **Gain-range(dB) /stage number** |
|---|---|---|---|---|
| [2] | 0.5 µm | 300 | 22mw | 18/1 |
| [6] | 1.2 µm | 25 | 19mw | 20/1 |
| [11][12][13] | 0.35 µm | 125 | 21mw | 19/1 |
| This work | 0.35 µm | 2.5 | 10.5mw | 60/3 |
| | 0.18 µm | 20 | 2.43mw | (-10 to 20)/1 |
| | 0.35 µm | 13 | 8.7mw | (0 to 47)/1 |

## 7. CONCLUSION

A Novel method to achieve variable transconductance is presented. Also this method is implemented on a folded cascode OTA to realize a low power VGA with wide gain variation range and finally spice simulation results have been presented to verify the claims. The proposed algorithm may be used on different platforms to mitigate different requirements of a VGA.

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