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A GENERAL REVIEW AND PERFORMANCE EVALUATION OF MULTI-LEVEL CONVERTERS FOR EFFICIENT POWER GENERATION AND APPLICATIONS

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ABSTRACT
This paper comparatively assessed the performance status of seven different multi-level converters with respect to their output voltages, output currents and corresponding percentage total harmonic distortion under the same RL-load condition. The spectral distributions of these various multi-level converters' waveforms obtained under normal modulation index of 0.8 are presented in this work. The significance of this paper is basically centered on the need to have an improved multi-level converter that has a better flexibility in control, which can ensure continuity in operation and can as well generate a reduced percentage harmonic distortion value under a varied modulation index. This converter will also be able to generate three level or five level output voltages depending on the point of load connection. The analysis and results obtained from this work thus showed that a five-level voltage source inverter formed by a cascade between a three-level flying capacitor and H-bridge produced a given percentage reduction in the value of harmonic distortion under the same loading condition and therefore ensures optimum performance with regard to other power converters of the same rating.

Keywords*: Multi-level Converters, Pulse Width Modulation, Spectral Analysis, percentage total harmonic distortion.*

1. INTRODUCTION
The swift developments in Multi-level inverter technology and the commercial availability of high power switches such as BJT, IGBT, MOSFET, IGCT, and THYRISTORS have resulted in a multifarious inverter topologies and symmetries that enhance its construction for wide electric power application at a low cost. However, for application that involves a medium voltage magnitude, a two level voltage source inverter (VSI) may be a preferred choice. Applications of a higher voltage magnitude such as the speed and torque control of a large horse power induction machine, power lines compensator devices, high voltage direct current electrostatic generators and traction applications, the two-level VSI becomes very inadequate. Higher voltage-levels such as the 3-level, 4-level, 5-level, 7-level and above are used since they ensure the production of an efficient and better output waveforms with a reduced total harmonic distortion at a very appreciable switching frequency above the rated fundamental value [1]-[5].
The multi-level inverter, to all intents and purposes, increases significantly in the cost of its rated power components as the voltage level increases and correspondingly decreases in the percentage value of THD. The background of this study, therefore, centers on the comparative analyses of seven different five-level inverter topologies with special emphasis on a flexibly controlled five-level topology that can generate a three level and five level output voltage magnitudes when connected to two different loading terminals which gives it a unique flexibility in power application. This topology is formed by cascading a three level flying capacitor and H-bridge having a single d.c source quite unlike the existing ones with multiple d.c sources [6].

2. GENERAL OVERVIEW OF MULTI-LEVEL CONVERTERS
Multi-level converter technology began in 1960 with the introduction of the multi-level stepped waveforms having a series connected H-bridge with a separate d.c voltage supply [7]. This topology in 1980's was later christened as the cascaded H-bridge converter [8].
In 1981, Nabae and Akagi invented a diode clamped multi-level converter (DCC) also known as the neutral

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point clamped converter (NPC) [9]. In 1992, Meynard and Foch invented a low power flying capacitor topology called multi-cell flying capacitor converter [10].

These three forms of multi-level converter topologies are presently considered as the classical or the conventional multi-level topologies as depicted in their circuit diagrams. The corresponding circuits and the switching sequences are shown in Figures 1-3 and Tables 1-3.

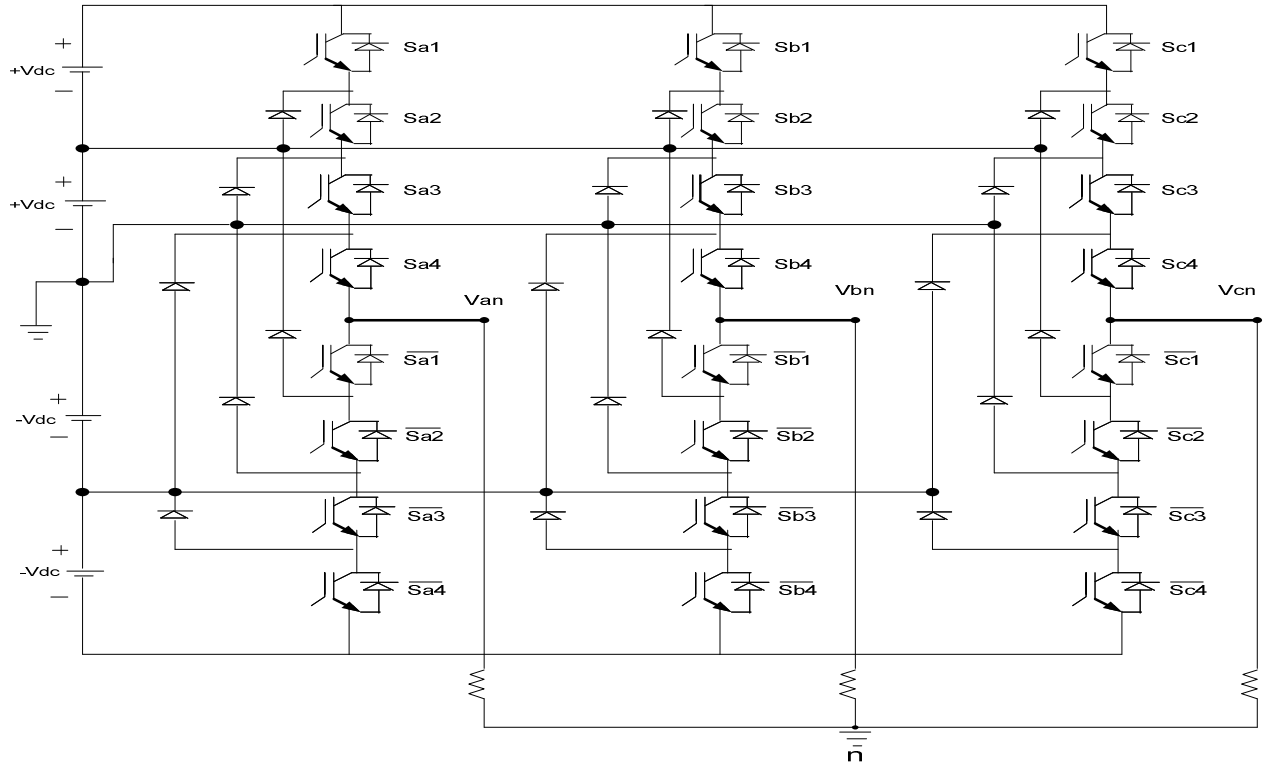

Figure 1: Five-level Diode Clamped Converter (NPC) Topology.

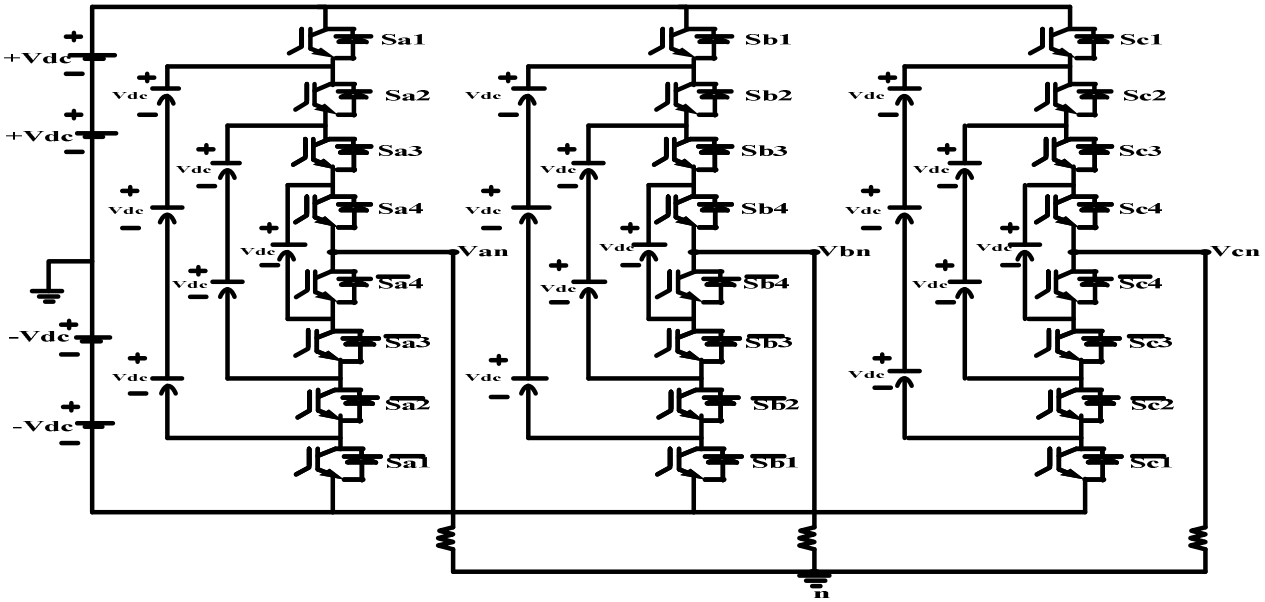

Figure 2: 5level-Flying Capacitor Clamped Converter.

*Table 1: Switching Sequence of Five-level Diode Clamped Converte*r.

s_{a1}	s_{a2}	s_{a3}	s_{a4}	$\overline{S_{a1}}$	$\overline{S_{a2}}$	$\overline{S_{a3}}$	$\overline{S_{a4}}$	V_{an} (Volts)
1	1	1	1	0	0	0	0	2Vdc
0	1	1	1	1	0	0	0	Vdc
0	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	-Vdc
0	0	0	0	1	1	1	1	-2Vdc

Table 2: Switching Sequence of Five Level Flying Capacitor Clamped Converter

s_{a1}	s_{a2}	s_{a3}	s_{a4}	$\overline{S_{a1}}$	$\overline{S_{a2}}$	$\overline{S_{a3}}$	$\overline{S_{a4}}$	V_{an} (Volts)
1	1	1	1	0	0	0	0	$2V_{dc}$
0	1	1	1	1	0	0	0	V_{dc}
1	1	1	0	0	0	0	1	V_{dc}
0	0	1	1	1	1	0	0	0
1	1	0	0	0	0	1	1	0
0	0	0	1	1	1	1	0	$-V_{dc}$
1	0	0	0	0	1	1	1	$-V_{dc}$
0	0	0	0	1	1	1	1	$-2V_{dc}$

Table 3: Switching Sequence of Five-Level Cascaded H-Bridge Inverter Topology.

s_{a1}	s_{a2}	s_{a3}	s_{a4}	$\overline{S_{a1}}$	$\overline{S_{a2}}$	$\overline{S_{a3}}$	$\overline{S_{a4}}$	V_{an} (Volts)
1	0	1	0	0	1	0	1	2Vdc
1	0	1	1	0	1	0	0	Vdc
1	0	0	0	0	1	1	1	Vdc
1	1	1	0	0	0	0	1	Vdc
0	0	1	0	1	1	0	1	Vdc
0	0	0	0	1	1	1	1	0
0	0	1	1	1	1	0	0	0
1	1	0	0	0	0	1	1	0
1	1	1	1	0	0	0	0	0
1	0	0	1	0	1	1	0	0
0	1	1	1	1	0	0	0	-Vdc
0	1	0	0	1	0	1	1	-Vdc
1	1	0	1	0	0	1	0	-Vdc
0	0	0	1	1	1	1	0	-Vdc
0	1	0	1	1	0	1	0	-2Vdc

Analytically, the DCC discussed has its different major drawbacks that are enumerated as follows:

- The diode clamped or neutral point converters have unequal voltage distribution across the series connected capacitors that result in a painstaking connection of the d.c-link capacitor to circumvent undue voltage imbalance.
- Higher number of clamping diodes associated with this topology results in high cost of component as the voltage level increases.
- Complexities in the phase sequencing and switching sequence of the converter for higher level voltages.

The flying capacitor multi-level converters (FCC) utilize flying capacitors as their clamping devices. These topologies have several attractive features in comparison with the diode clamped or neutral point converters. However, FCC requires excess number of storage capacitors for higher voltage steps.

The advantages of FCC include:

- ❖ It aids transformer less operation that promotes portability and elegance in modularity of the inverter structure.
- ❖ Absence of clamping diodes and presence of redundant phase legs which allow the switching stresses to be equally distributed across the semi-conductor switches.

The multi-level cascaded H-bridge inverter with isolated d.c voltage supplies previously mentioned has many advantages when compared to the NPC or DCC and flying capacitor FCC topologies. The cascaded H-bridge (CHB) configuration does not require clamping diodes and the input power is distributed across the different input sources, which makes it more suitable for varieties of applications. Additional advantage of the cascaded hybrid converter (CHB) is that it can easily be combined with either NPC or FCC to generate a higher inverter level and failure of a device in the H-bridges does not preclude the operation of the inverter. It allows for a reduced power level operation; thus enhancing a fault-tolerant inverter configuration. Figure 3 represents the five-level cascaded H-bridge topology while Table 3 depicts its switching sequence.

Many other multi-level converter configuration have been developed based on the above three conventional topologies (NPC, FCC and CHB).

A configuration where three-level DCC/NPC inverter cascaded with multiple H-bridges has been presented in [11]. The circuit diagram of a three-level DCC/NPC cascaded with multiple H-bridges to produce five-level NPC/H-bridge inverter is shown in Figure 4 (5L-NPC/H-bridge) while the switching sequence is presented in Table 4. The problem of voltage imbalance across the dc-link capacitors inherently existing in the diode clamped multi-level converter topology constitutes a defect in this analyzed topology. Also this configuration has a multiple d.c supply which give rise to more cost of implementing it.

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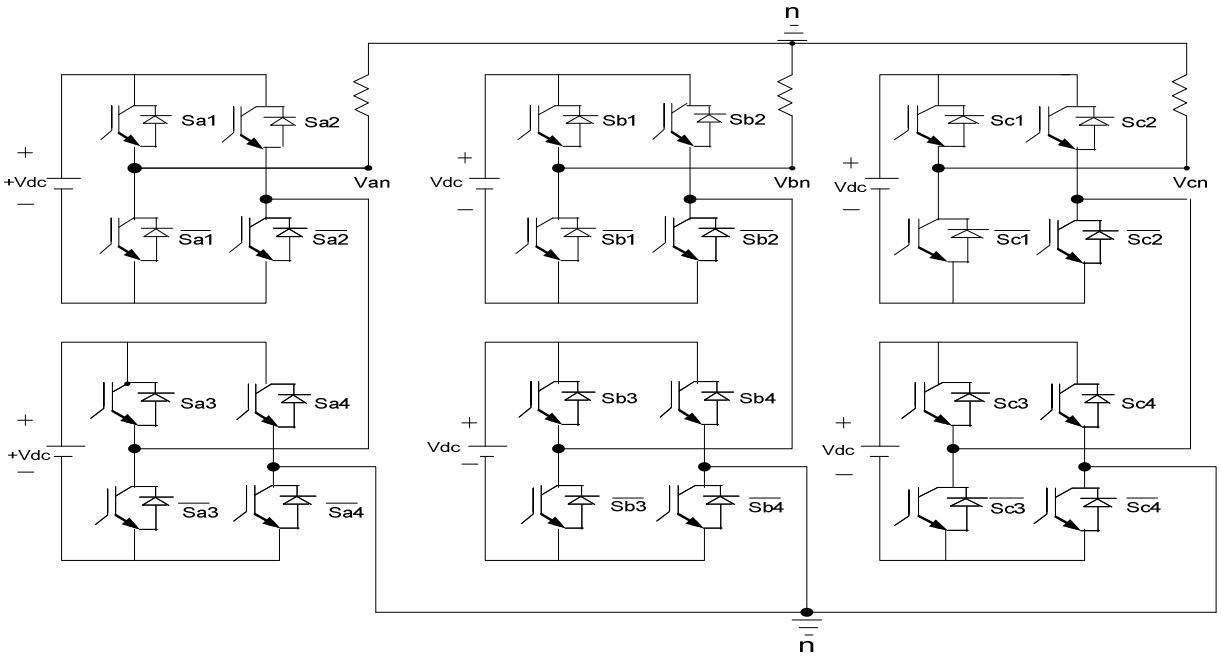

Figure 3: Five-Level Cascaded H-Bridge Inverter Topology.

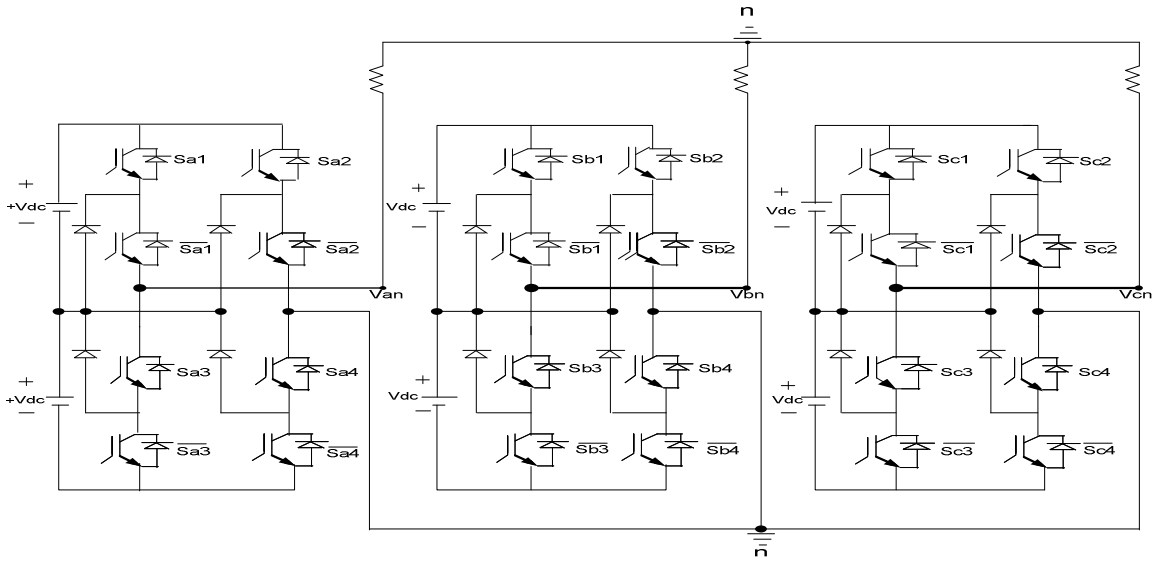

Figure 4: Five-level inverter formed by cascading three-level DCC (NPC) and H-bridge

Table 4: Switching Sequence of 5level inverter formed by cascaded 3level DCC & H-bridge

s_{a1}	s_{a2}	s_{a3}	s_{a4}	$\overline{S_{a1}}$	$\overline{S_{a2}}$	$\overline{S_{a3}}$	$\overline{S_{a4}}$	V_{an} (Volts)
1	1	0	0	0	0	1	1	2E
0	1	0	0	1	0	1	1	E
0	1	0	0	0	0	1	0	0
0	0	1	1	1	0	0	0	-E
0	0	1	1	1	1	0	0	-2E

New multi-level inverter configurations for induction motor drive formed by cascading two multiples of two-level inverter and one three-level DCC is presented in [12]. The circuit diagram for this configuration is shown in Figure 5 while the switching sequence is presented in Table 5. A five-level active neutral point clamped (5L-ANPC) inverter topology is another configuration which is a hybrid of flying capacitor and neutral point clamped topology as presented in [13]-[14]. This topology combines the flexibility of the multi-level floating capacitor converter with the robustness of the industrial neutral point clamped (NPC) converter to generate multi-level voltages.

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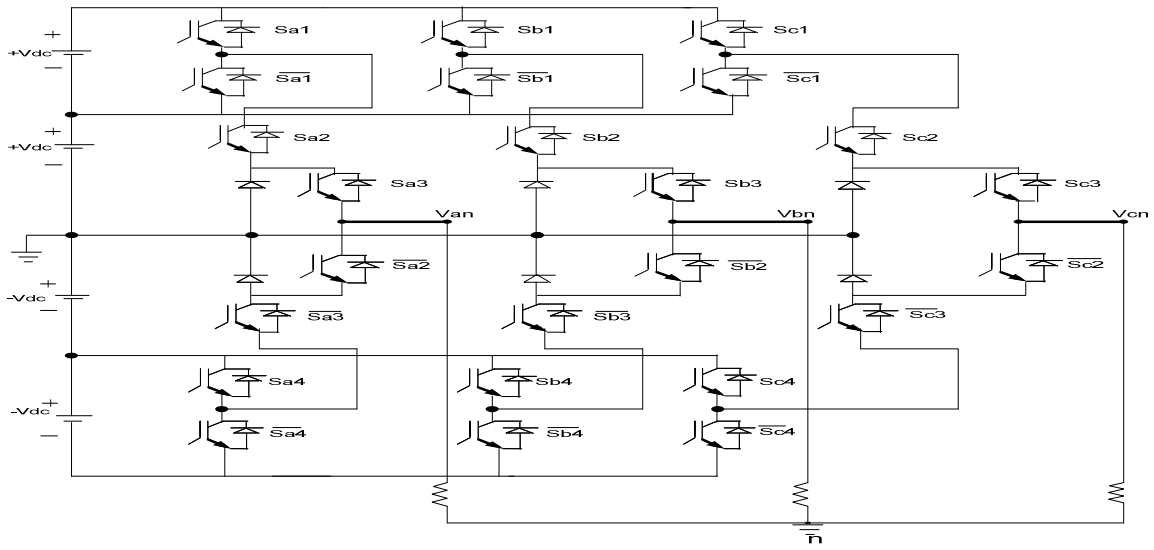

Figure 5: Five-Level Topology Formed By Multiple Two-Levels Cascaded With Three-Level Inverter.

Table 5: Switching Sequence of Figure 5.

s_{a1}	s_{a2}	s_{a3}	s_{a4}	$\overline{S_{a1}}$	$\overline{S_{a2}}$	$\overline{S_{a3}}$	$\overline{S_{a4}}$	V_{an} (Volts)
1	1	1	1	0	0	0	0	2Vdc
0	1	1	1	1	0	0	0	Vdc
0	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	-Vdc
0	0	0	0	1	1	1	1	-2Vdc

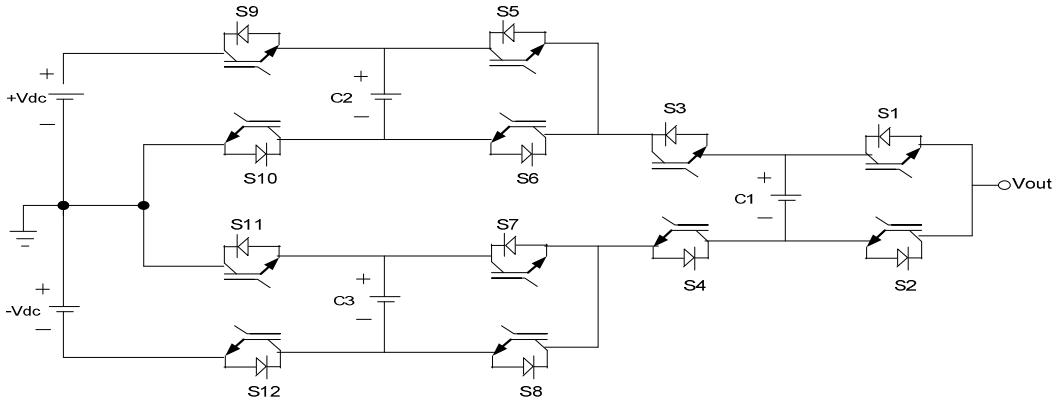

Figure 6a: Circuit Diagram of Five-Level ANPC.

The circuit diagram presented in Figure 6a depicts the single phase five-level active neutral point clamped (5L-ANPC) inverter topology. This converter is an arrangement of two level inverters connected in parallel with the d.c-link capacitors. The first sub-circuit is made up of S_5, S_6, S_9, S_{10}, and C_2, while the second sub-circuit is made up of S_7, S_8, S_{11}, S_{12}, and C_3 and a third sub-circuit S_1, S_2, S_3, S_4, and C_1 that is used to connect the converter to the output phase.

It is worth mentioning that the switches S_5 and S_7 are operated in phase while S_6 and S_8 are also operated in phase. S_5 and S_7 are complementary to S_6 and S_8. A similar sequence is applied to S_9, S_{10}, S_{11} and S_{12}.The three floating capacitors shown in Figure 6a add excessive cost to the overall system and require more space for accommodating the entire volume of the inverter structure. For this reason, it is expedient to reduce the number of floating capacitors. This is achieved by removing C_2 and C_3 from Figure 6a to form a more reduced circuit in Figure 6b which is a simplified diagram for three phase 5Level-ANPC. The possible switching states for the above-discussed 5Level-ANPC is presented in Table 6 with C_1 charged to a voltage level of $\frac{V_{dc}}{2}$.

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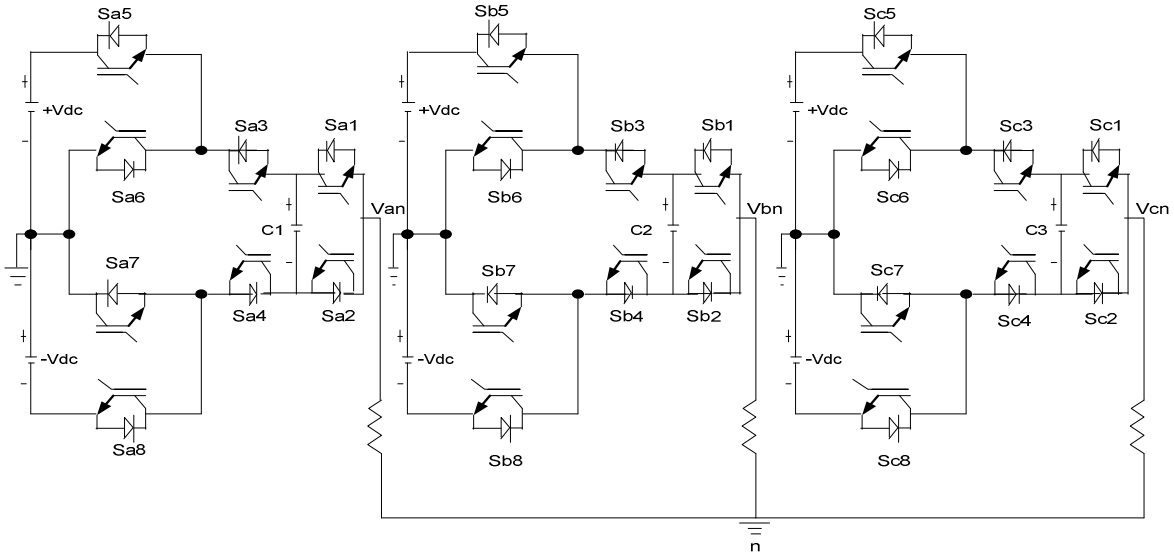

Figure 6b: Modified Circuit Diagram of Five-Level ANPC.

Table 6: Switching Sequence for 5Level-ANPC

S_{a8}	S_{a7}	S_{a6}	S_{a5}	S_{a4}	S_{a3}	S_{a2}	S_{a1}	V_{an} (Volts)
1	0	1	0	1	0	1	0	$-V_{dc}$
1	0	1	0	1	0	0	1	$-V_{dc}/_2$
1	0	1	0	0	1	1	0	$-V_{dc}/_2$
1	0	1	0	0	1	0	1	0
0	1	0	1	1	0	1	0	0
0	1	0	1	1	0	0	1	$V_{dc}/_2$
0	1	0	1	0	1	1	0	$V_{dc}/_2$
0	1	0	1	0	1	0	1	V_{dc}

Derivative of cascaded hybrid (CHB) converter with an embedded auxiliary switches, diodes and separate d.c voltages has been presented by Nasrudin A Rahim in [15]. In this topology, different switching devices such as the insulated gate bipolar transistors (IGBT) and full bridge diodes were applied in a way that the IGBT is modulated with a rectified sinusoidal waveforms and carrier signal to produce the respective five level output voltage. This topology though has an excellent economy of cost reduction in components number; it lacks flexibility in control since a failure of one switch precludes the functional operation of the entire multi-level topology. A similar approach proposed by Won-Siketal [16] applied a five level switched voltage source inverter having twenty four main switches, six main diodes, six balancing capacitors and four separate d.c supplies thus creating more cost in the realization of the proposed topology.

The multi-level topologies discussed above vary comparatively in their switching sequences and in relation to the complexities of their structures cum cost of components in construction process.

The proposed multi-level topology discussed in this paper, employs the features of a cascaded H-bridge and flying capacitor converters at a reduced %THD, simplicity in modulation and ease in practical implementation. As shown in Figure 7a, the proposed topology has a three phase, three-level flying capacitor inverter, a capacitor fed H-bridge cascaded to each phase of the three-level FCC with a common d.c voltage supply. This enhances the control of the d.c voltage supply to the cascaded topology quite unlike the existing topologies which employ isolated or separated d.c voltage supply thereby incurring more cost of construction. An important feature of this topology is the ability to balance the capacitor voltages with ease. A more prominent feature is that when one of the H-bridges fails, the proposed topology can efficiently operate as a three-level inverter by bypassing the H-bridge as shown in Figure 7b. This feature of the inverter improves the reliability of the whole system thus ensuring continuity in operation and fault-tolerant at all load conditions. The modulation scheme is also of paramount importance since it does not need a complex modulation control strategy and thus adaptive to all kinds of load condition with a reduced power loss.

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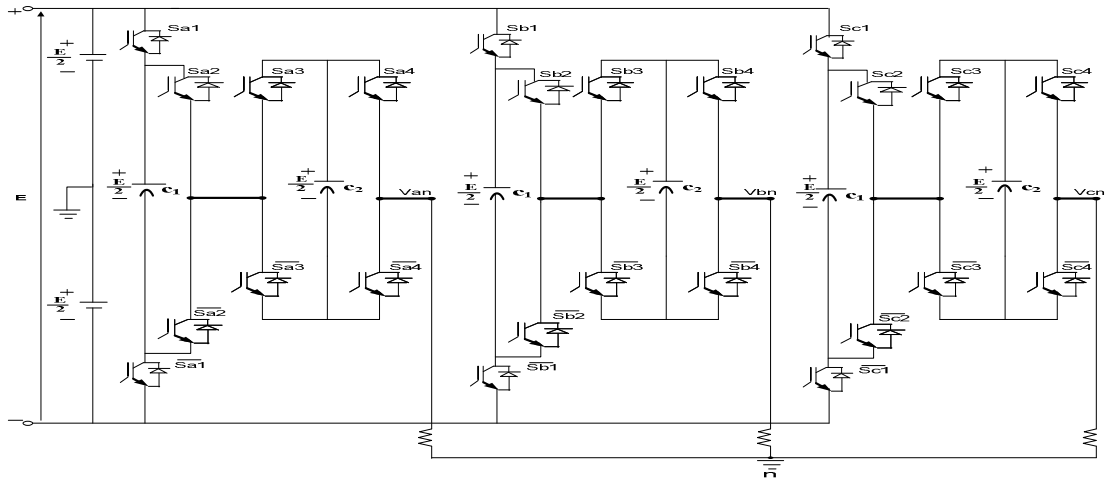

Figure 7a: Circuit Diagram of the Proposed Five-Level Inverter Topology.

Table 7: Switching Sequence and Output Voltages of the Proposed Five-Level Topology.

s_{a1}	s_{a2}	s_{a3}	s_{a4}	$\overline{S_{a1}}$	$\overline{S_{a2}}$	$\overline{S_{a3}}$	$\overline{S_{a4}}$	V_{an}	C_1	C_2	Cycle
1	1	0	1	0	0	1	0	E	No Effect	Charging	Positive half-cycle
1	1	1	1	0	0	0	0	$E/2$	No Effect	No Effect	
1	1	0	0	0	0	1	1	$E/2$	No Effect	No Effect	
1	1	1	0	0	0	0	1	0	No Effect	Discharging	
1	0	1	1	0	1	0	0	0	Discharging	No Effect	
1	0	0	0	0	1	1	1	0	Discharging	No Effect	
0	1	1	1	1	0	0	0	0	Charging	No Effect	
0	1	0	0	1	0	1	1	0	Charging	No Effect	
0	0	0	1	1	1	1	0	0	No Effect	Charging	Negative half-cycle
0	0	1	1	1	1	0	0	$-E/2$	No Effect	No Effect	
0	0	0	0	1	1	1	1	$-E/2$	No Effect	No Effect	
0	0	1	0	1	1	0	1	-E	No Effect	Discharging	

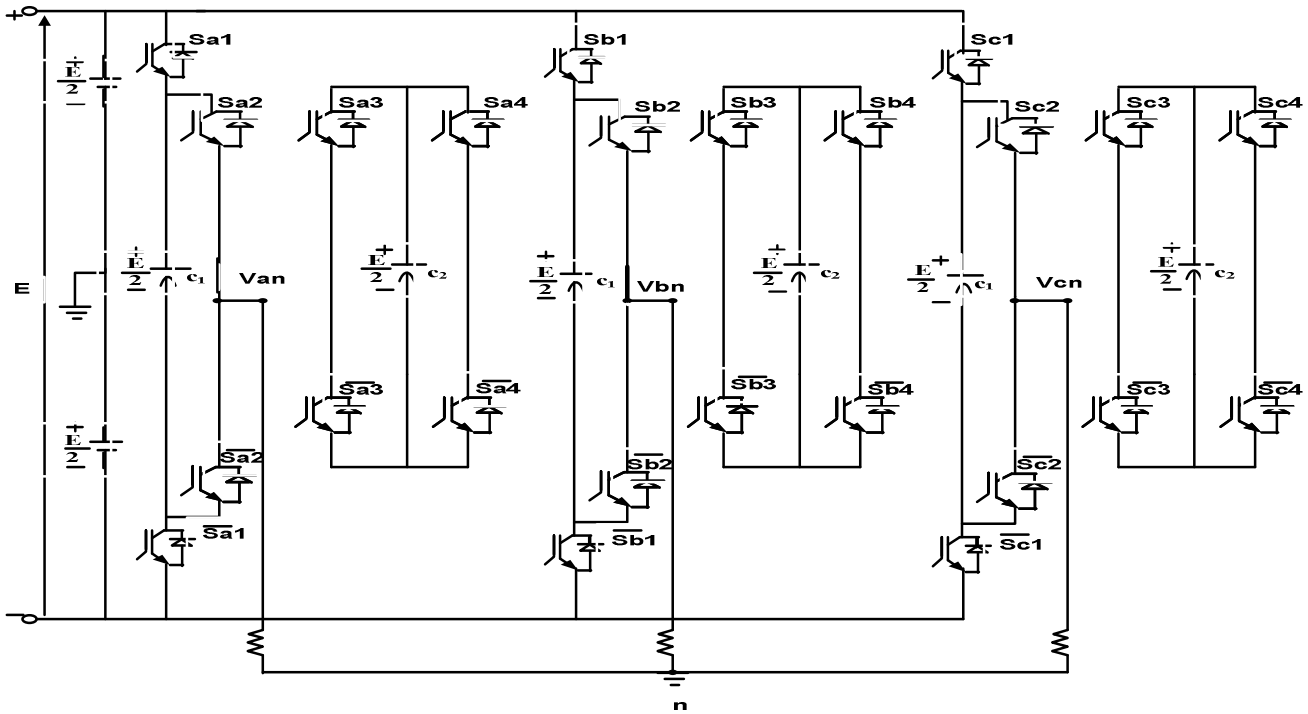

Figure 7b: Circuit Diagram of the Three level obtained from a bypassed H-bridge.

3. MULTI-CARRIER/SINUSOIDAL PULSE-WIDTH MODULATION STRATEGY

Multi-carrier pulse width modulation technique implies the natural sampling of a single modulating wave (reference wave) usually sinusoidal wave or steps of staircase approximated to sine wave through several carrier signals usually triangular waves to produce output pulses with variable widths [17].

Conventionally, an n-level converter always has $n-1$ triangular carrier signals with the same frequency Fc and the same peak-to-peak amplitude Ac which are usually placed in such a way that their frequency bands are close. The reference or the modulating waveform (sinusoidal wave or staircase wave form) has peak to peak amplitude Am and a modulating frequency of Fm which is centered in the middle of the carrier wave. This reference wave is continuously been compared with each of the triangular carrier signals until the following conditions are achieved: If the reference or the modulating waveform is greater than the carrier signal, then the active switching device corresponding to that carrier is turned on. Nevertheless, if the reference waveform is less than the carrier signal, then the active switching device corresponding to that carrier is turned off [17]. The simple algorithm is presented as follows:

if

$V_{mj} > V_c$; $S_i = 1$.

else

$V_{mj} < V_{cj}$; $\bar{S}_i = 0$.

The carrier-based modulation schemes for multi-level inverters are classified into two: Phase Shifted and Level Shifted modulations [18]. Both modulation schemes can be applied to the reviewed topologies.

❖ Phase Shifted Multi Carrier Modulation: In general, a multi-level inverter with m voltage levels requires (m-1) triangular carriers. In the phase shifted multi-carrier modulation, all the triangular carriers have the same frequency and the same peak to peak amplitude but there is a phase shift between two adjacent carrier waves which is given by the relation:

$$\theta_{cr} = \frac{360^0}{(m-1)} \quad (1)$$

Where m represents the voltage level which in this context is five. Therefore, $\theta_{cr} = 90^0$.

The modulating signal is usually a three-phase sinusoidal wave with adjustable amplitude. The gate signals are generated by comparing the modulating wave with the carrier waves [18]. Figure 8 shows the principle of the phase-shifted multi-carrier modulation for a five level topology where four triangular carriers are required with a 90^0 phase displacement between two adjacent carriers. Phase (A) modulating wave V_{MA} was plotted for simplicity. The carriers V_{cr1} and V_{cr2} are used to generate gating signal for the upper switches while the other two carriers V_{cr3} and V_{cr4} which are out of phase with V_{cr1} and V_{cr2} produce the gating signal for the lower switches respectively.

Level-Shifted Multi Carrier Modulation: This scheme also requires (m-1) triangular carriers all having the same frequency and amplitude. The (m-1) triangular carriers are vertically disposed such that the bands they occupy are contiguous. This modulation technique is classified into three viz: In-phase disposition, Alternate phase opposition disposition and Phase opposition disposition technique.

❖ In-phase disposition (IPD): This technique stipulates that all the carriers above and below the reference signal must be in phase across the frequency band as presented in Figure 9.

❖ Alternate Phase Opposition Disposition (APOD): In this modulation technique, every carrier waveform is always out of phase from the adjacent carrier bands by 180^0 as shown in Figure 10.

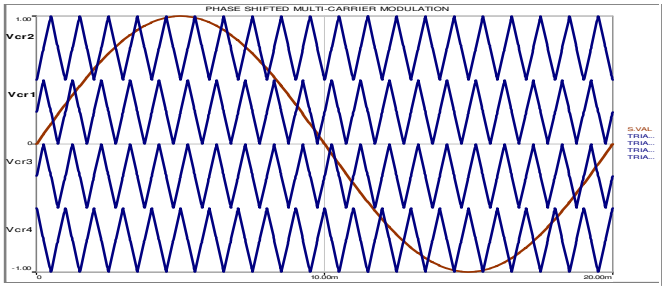

Figure 8: Phase-Shifted Multi-Carrier Modulation for A Five Level Topology.

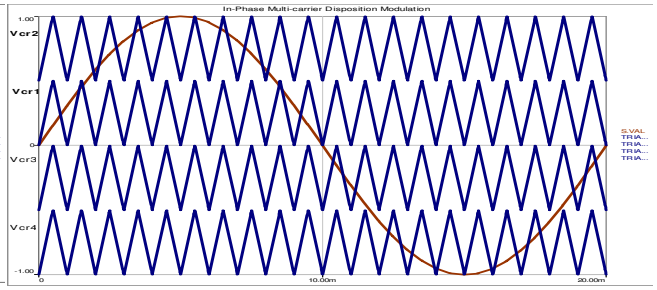

Figure 9: In-Phase Multi-Carrier Modulation for A Five Level Topology.

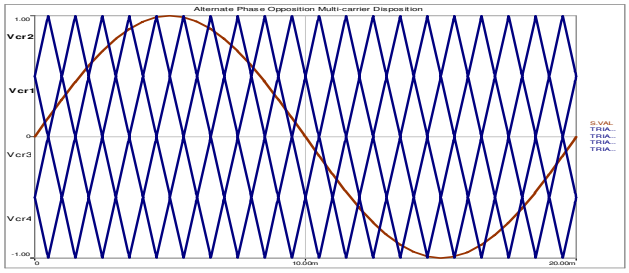

Figure 10: Alternate Phase Opposition Disposition Carrier Modulation

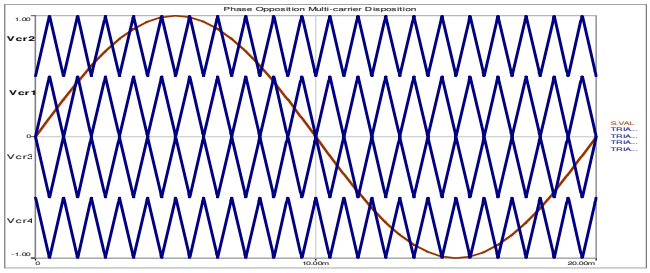

Figure 11: Phase Opposition Disposition Multi-Carrier Modulation for A Five Level Topology.

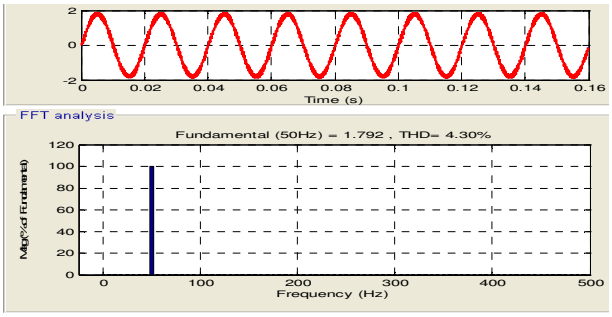

Figure 12: Phase Current of 5-level DCC with Spectral Result.

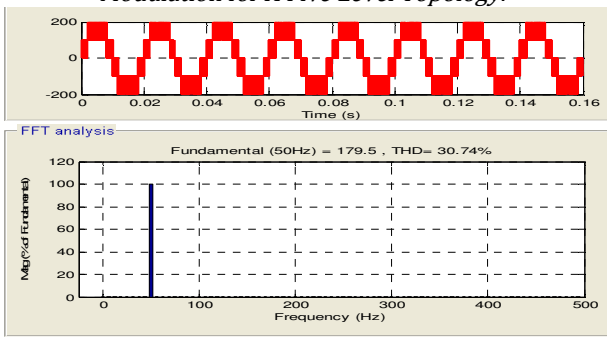

Figure 13:V_{an}& Spectrum of 5-level DCC.

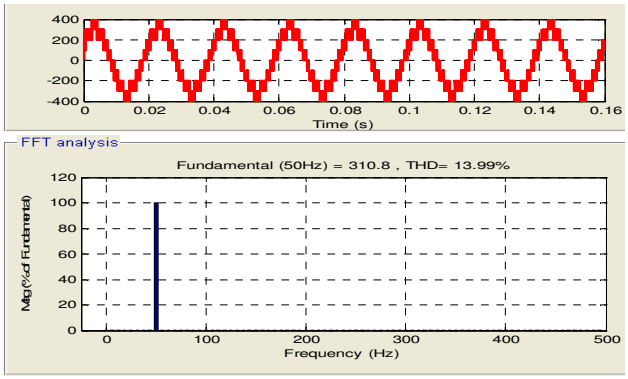

Figure 14:V_{LL}& Spectrum of 5-level DCC.

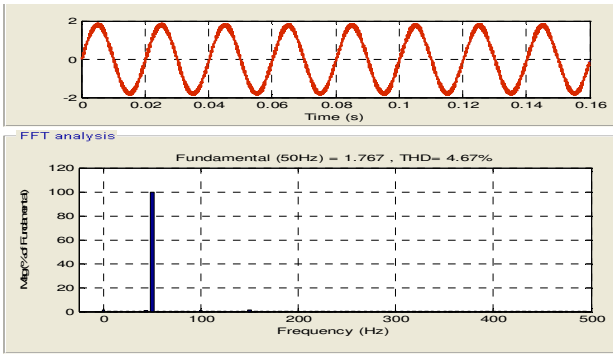

Figure 15: Phase Current of 5-level FCC Converter with Spectral Result.

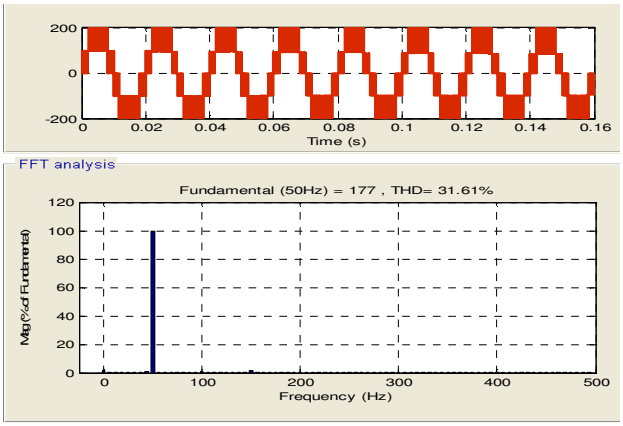

Figure16: V_{an}& Spectrum of 5-level FCC.

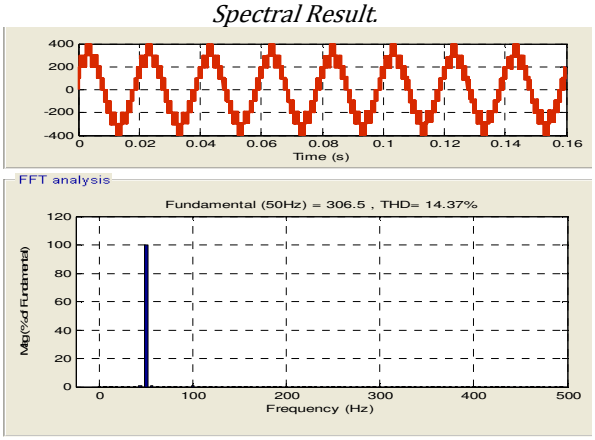

Figure 17:V_{LL}& Spectrum of 5-level FCC.

❖ Phase Opposition Disposition Modulation: In this modulation type, the carrier waveforms above the reference zero axis are out of phase with those below the reference zero axis by 180^0. This is shown in Figure 11.

The report presented in [19] showed that In-phase disposition modulation scheme provides the best harmonic profile out of the entire aforementioned modulation scheme outlined.

3.1 Model Simulation of the Reviewed Multi-level Converter's Topologies.

Simulation was carried out on the above reviewed seven multi-level topologies using the conventional sinusoidal pulse-width modulation (SPWM) method with RL load of 100ohms and 20miliHenry. Results presented below represent the phase currents, phase voltage and line voltages of the various reviewed five-level converter topologies.

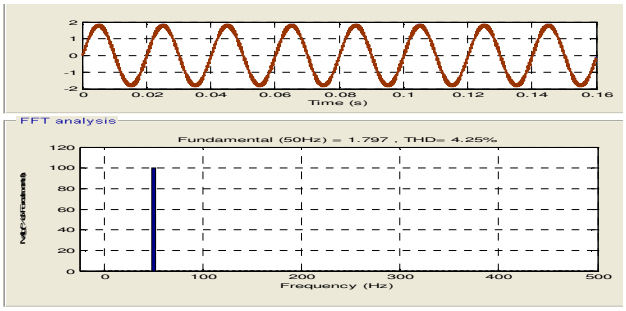

Figure 18: Phase Current of 5-level CHB Converter with Spectral Result.

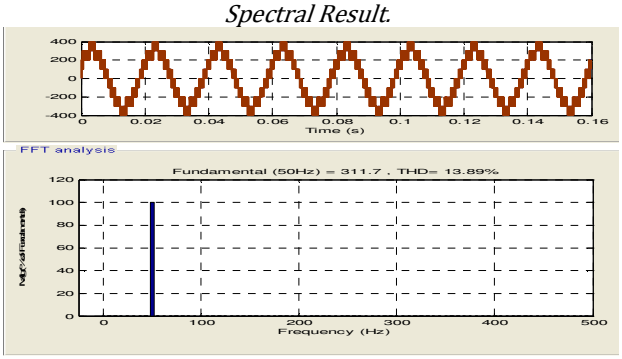

Figure 20: V_{LL}& Spectrum of 5-level CHB.

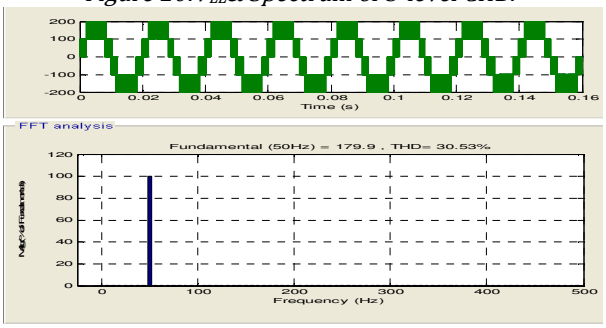

Figure 22: V_{an}& Spectrum of 5-level ANPC.

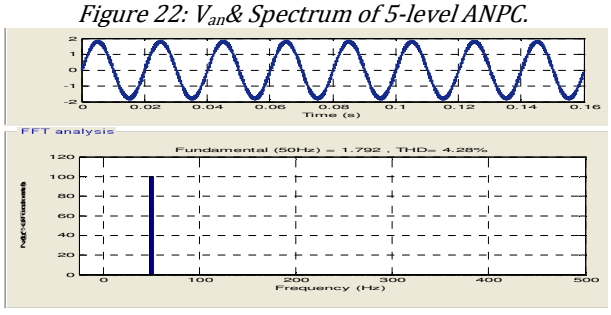

Figure 24: Phase Current of 5-level NPC Cascaded with H.B Converter with Spectral Result.

3.2 Comparative Analysis of the Reviewed Topologies with the Proposed Five-Level.

The comparative analysis of the reviewed topologies was carried out based on the number of components, flexibility of operation and the respective total harmonic distortion produced by the various topologies after simulation. For simplicity in analysis, the reviewed topologies were classified and tabulated as follows:

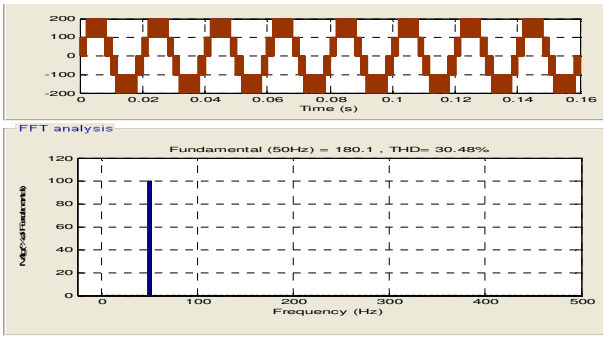

Figure 19: V_{an}& Spectrum of 5-level CHB.

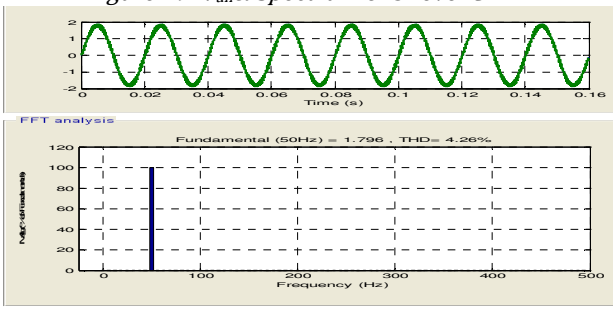

Figure 21: Phase Current of 5-level ANPC Converter with Spectral Result.

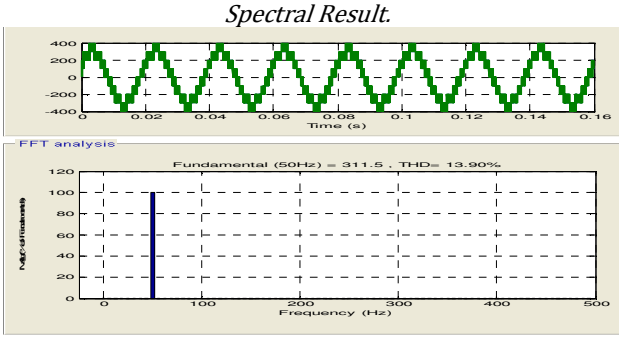

Figure 23: V_{LL}& Spectrum of 5-level ANPC.

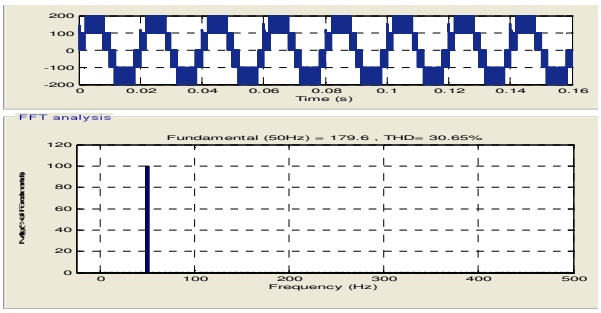

Figure 25: V_{an}& Spectral of 5-level NPC/CHB

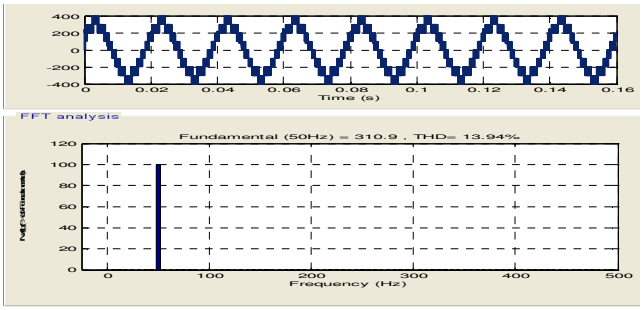

Figure 26: V_{LL} & Spectra of 5-level NPC/CHB.

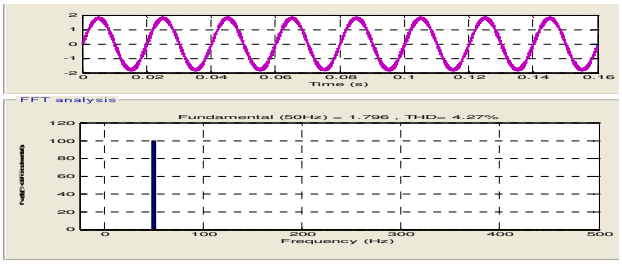

Figure 27: Phase Current of 5-level formed from multiple 2-level and 3-level NPC with Spectral Result.

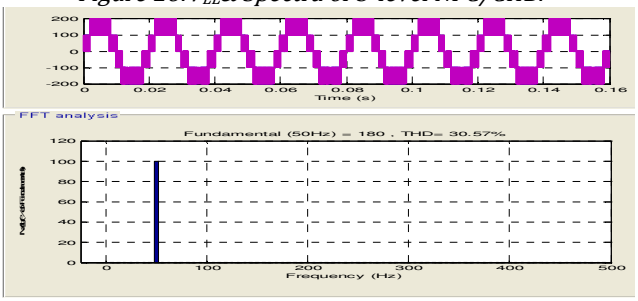

Figure 28: Phase Voltage of 5-level formed from multiple 2-level and 3-level NPC with Spectral Result.

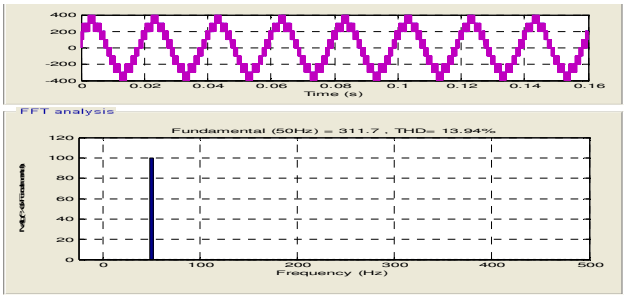

Figure 29: Line Voltage of 5-level formed from multiple 2-level and 3-level NPC with Spectral Result.

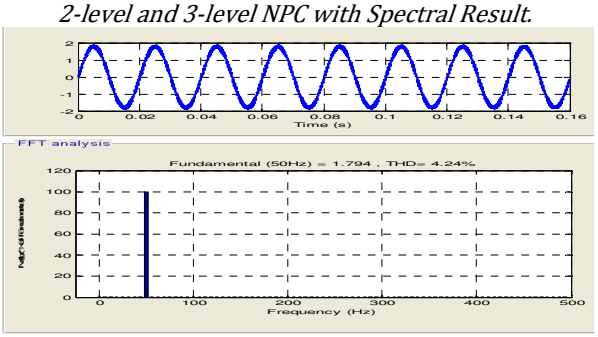

Figure 30: Phase Current of the Proposed Five-level Converter with its Spectral Result.

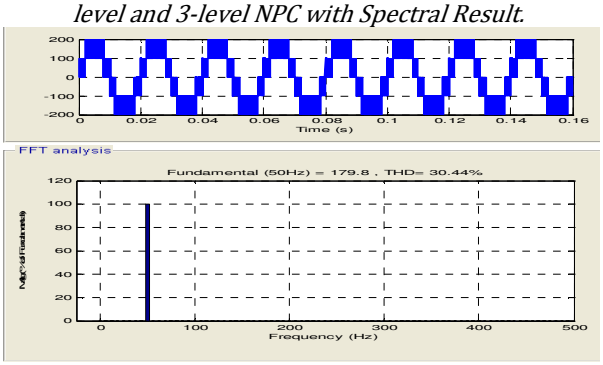

Figure 31: V_{an} &Spectrum of Proposed 5level.

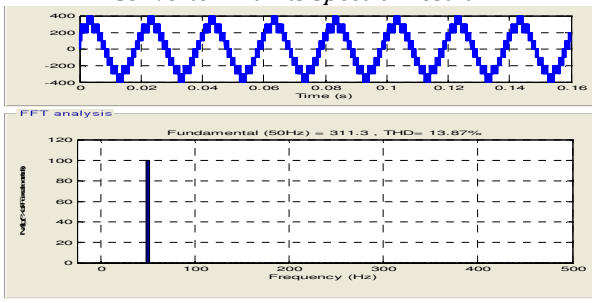

Figure32: V_{LL} & Spectrum of Proposed 5level

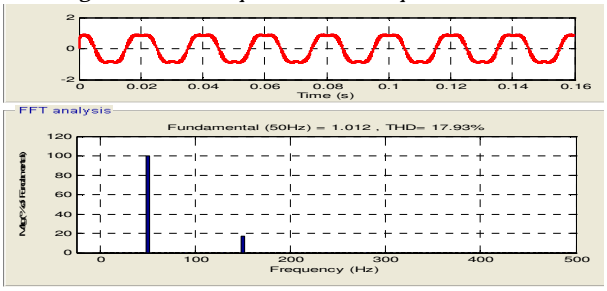

Figure 33: Phase Current of the Proposed Five-level at 0.4 modulation index

Table 8: Comparative Analysis of the Reviewed Topologies.

ITEMS	Class A 3Φ, 5level DCC	Class B 3Φ, 5level FCC	Class C 3Φ, 5level CHB	Class D 3Φ, 5level ANPC	Class E 3Φ, 5level NPC/CHB	Class F 3Φ, 5level formed From 3Level NPC and Multiple 2Level Inverter	Class G Proposed 3Φ, 5level Converter
No of Clamping Diodes	18	0	0	0	12	6	0
Power Supply	1	1	6	3	3	1	1
No of Switches	24	24	24	24	24	24	24
No of Clamping Capacitors	0	18	0	3	0	0	6

Table 9: Comparative Analysis of the Total Harmonic Distortion of the Reviewed Topologies.

Class A	Class B	Class C	Class D	Class E	Class F	Class G
THD of I_{AN} = 4.30%	THD of I_{AN} = 4.67%	THD of I_{AN} = 4.25%	THD of I_{AN} = 4.26%	THD of I_{AN} = 4.28%	THD of I_{AN} = 4.27%	THD of I_{AN} = 4.24%
THD of V_{AN} = 30.74%	THD of V_{AN} = 31.61%	THD of V_{AN} = 30.48%	THD of V_{AN} = 30.53%	THD of V_{AN} = 30.65%	THD of V_{AN} = 30.57%	THD of V_{AN} = 30.44%
THD of V_{LL} = 13.99%	THD of V_{LL} = 14.37%	THD of V_{LL} = 13.89%	THD of V_{LL} = 13.90%	THD of V_{LL} = 13.94%	THD of V_{LL} = 13.94%	THD of V_{LL} = 13.87%

3.3 THD and Spectral Distribution of the Proposed Multi-level Topology at 0.4, 0.6 and 0.8 Modulation Index.

The stepped waveforms presented in Figures 33 – 42 for the line-line and line-neutral voltages as time function can be represented using the following fourier transform equations [20].

$$V_{AB} = \frac{2\sqrt{3} \times V_{dc}}{\pi} \times \left[\sin\left(\omega t + \frac{\pi}{6}\right) + \frac{1}{5}\sin\left(5\omega t + \frac{\pi}{6}\right) + \frac{1}{7}\sin\left(7\omega t + \frac{\pi}{6}\right) + \frac{1}{11}\sin\left(11\omega t + \frac{\pi}{6}\right) + \frac{1}{13}\sin\left(13\omega t + \frac{\pi}{6}\right) + \cdots\right] \quad (2)$$

$$V_{BC} = \frac{2\sqrt{3} \times V_{dc}}{\pi} \times \left[\sin\left(\omega t - \frac{\pi}{2}\right) + \frac{1}{5}\sin\left(5\omega t - \frac{\pi}{2}\right) + \frac{1}{7}\sin\left(7\omega t - \frac{\pi}{2}\right) + \frac{1}{11}\sin\left(11\omega t - \frac{\pi}{2}\right) + \frac{1}{13}\sin\left(13\omega t - \frac{\pi}{2}\right) + \cdots\right] \quad VV \quad (3)$$

$$V_{CA} = \frac{2\sqrt{3} \times V_{dc}}{\pi} \times \left[\sin\left(\omega t - \frac{7\pi}{6}\right) + \frac{1}{5}\sin\left(5\omega t - \frac{7\pi}{6}\right) + \frac{1}{7}\sin\left(7\omega t - \frac{7\pi}{6}\right) + \frac{1}{11}\sin\left(11\omega t - \frac{7\pi}{6}\right) + \frac{1}{13}\sin\left(13\omega t - \frac{7\pi}{6}\right) + \cdots\right] \quad (4)$$

The phase voltages are given by (5) – (7).

$$V_{AN} = \frac{2 \times V_{dc}}{\pi} \times \left[\sin\omega t + \frac{1}{5} \times \sin(5\omega t) + \frac{1}{7} \times \sin(7\omega t) + \frac{1}{11} \times \sin(11\omega t) + \frac{1}{13} \times \sin(13\omega t) + \cdots\right] \quad (5)$$

$$V_{BN} = \frac{2 \times V_{dc}}{\pi} \times \left[\sin\left(\omega t - \frac{2\pi}{3}\right) + \frac{1}{5}\sin\left(5\omega t - \frac{2\pi}{3}\right) + \frac{1}{7}\sin\left(7\omega t - \frac{2\pi}{3}\right) + \frac{1}{11}\sin\left(11\omega t - \frac{2\pi}{3}\right) + \frac{1}{13}\sin\left(13\omega t - \frac{2\pi}{3}\right) + ..\right] \quad (6)$$

$$V_{CN} = \frac{2 \times V_{dc}}{\pi} \times \left[\sin\left(\omega t - \frac{4\pi}{3}\right) + \frac{1}{5}\sin\left(5\omega t - \frac{4\pi}{3}\right) + \frac{1}{7}\sin\left(7\omega t - \frac{4\pi}{3}\right) + \frac{1}{11}\sin\left(11\omega t - \frac{4\pi}{3}\right) + \frac{1}{13}\sin\left(13\omega t - \frac{4\pi}{3}\right) + ..\right] \quad (7)$$

From (5) – (7) V_{BN} and V_{CN} lag V_{AN} by $\frac{2\pi}{3}$ and $\frac{4\pi}{3}$ respectively. It is observed that only odd harmonics of the order $K = 6N \pm 1$ are present, where N is an integer. The different wave forms are due to different phase relationship between the harmonics and the fundamental. The magnitude of the above fourier coefficients for phase A voltage when normalized with respect to $\frac{2 \times V_{dc}}{\pi}$ produces (8).

$$H(\text{Normalized}) = \sum_{N}^{\infty}\left[\sin(\omega t_1) + \frac{1}{5}\sin(5\omega t_2) + \frac{1}{7}\sin(7\omega t_3) + \frac{1}{11} \times \sin(11\omega t_4) + \cdots\right] \quad (8)$$

where ωt_1, ωt_2, ωt_3, ωt_4 and ωt_5 represent the conducting angles along the ωt axis. These angles are chosen such that the voltage total harmonic distortion is reduced to a barest minimum. Normally, the predominant lower harmonic frequencies are cancelled in the choice of these angles. Equation (9) is developed from the above normalized voltage equation in (8).

$$\frac{1}{11}\sin(11\omega t_1) + \frac{1}{11}\sin(11\omega t_2) + \frac{1}{11}\sin(11\omega t_3) + \frac{1}{11}\sin(11\omega t_4) + \frac{1}{11}\sin(11\omega t_5) + \frac{1}{7}\sin(7\omega t_1) + \frac{1}{7}\sin(7\omega t_2) + \frac{1}{7}\sin(7\omega t_3) + \frac{1}{7}\sin(7\omega t_4) + \frac{1}{7}\sin(7\omega t_5) + \frac{1}{5}\sin(5\omega t_1) + \frac{1}{5}\sin(5\omega t_2) + \frac{1}{5}\sin(5\omega t_3) + \frac{1}{5}\sin(5\omega t_4) + \frac{1}{5}\sin(5\omega t_5) + \sin(\omega t_1) + \sin(\omega t_2) + \sin(\omega t_3) + \sin(\omega t_4) + \sin(5\omega t_5) + = \text{Ma} \times \text{s} \quad (9)$$

M_a stands for the modulation index. The variable S is chosen as the maximum voltage level under study which in this context is five. Also M_a value is chosen as 0.8 for this analysis. The MATLAB f-solve programme generated the following results: theta =

1.0562 radian = 60.52^0, 1.3033 radian = 74.67^0, 1.4033 radian = 80.39^0, 1.5708 radian = 90.0^0

This implies that the inverter switching devices and the corresponding output for five level are symmetrically switched on during the positive half cycle of the fundamental voltage to +Vdc at 60.52^0, +2Vdc at 74.67^0 ,+3Vdc at 80.39^0 and +4Vdc at 90^0. Similarly in the negative half cycle it is also switched on to –Vdc at 240.52^0, -2Vdc at 254.67^0 , -3Vdc at 260.39^0 and -4Vdc at 270^0. All other values above the maximum values of angular convergence are eliminated.

Total harmonic distortion: This is defined as the measure of the closeness in shape between a waveform and its fundamental component [20].

Mathematically:

$$THD = \frac{\sqrt{\sum_{N=2,3\ldots}^{\infty}(V_N)^2}}{V_0} \quad (10)$$

where N stands for the harmonic order, V_N= the root mean square value of the nth-harmonic component and V_o = the root mean square value of the output voltage corresponding to the fundamental component.

The results of the Pulse-width modulation carried out on the proposed topology at varying modulation index of 0.4, 0.6, and 0.8 are presented in Figures 33-42 and also in Table 10 with their respective total harmonic distortion values and spectral distributions.

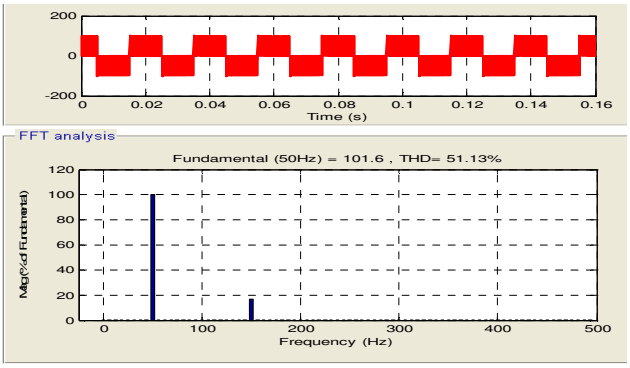

Figure 34:V_{an} of the Proposed 5level at 0.4 MI

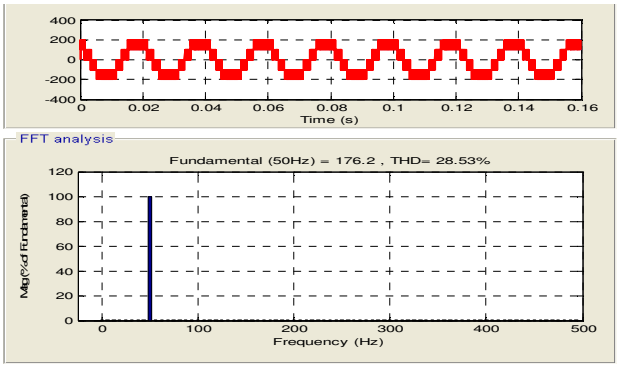

Figure 35:V_{LL} of the Proposed 5level at 0.4 MI

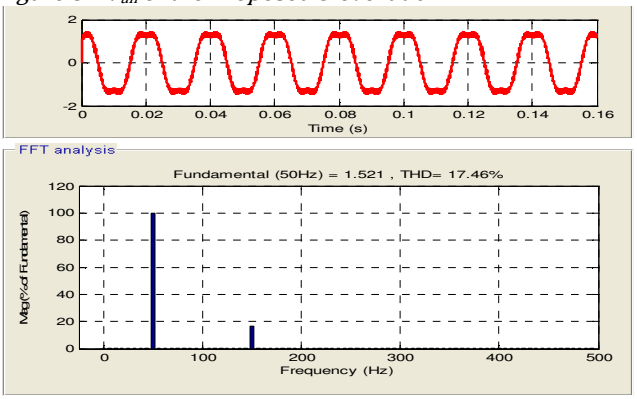

Figure 36: Phase Current of the Proposed 5-level at 0.6 modulation index

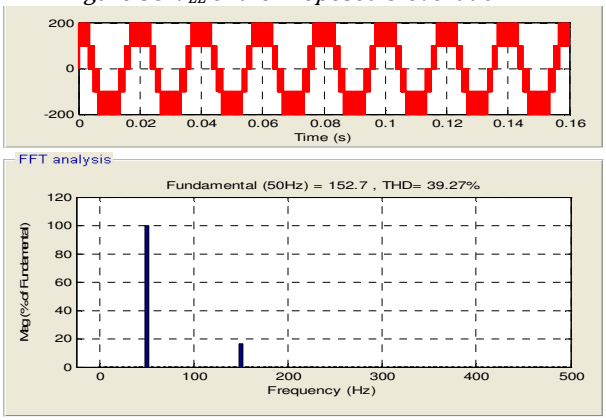

Figure 37: V_{an} of the Proposed 5level at 0.6MI

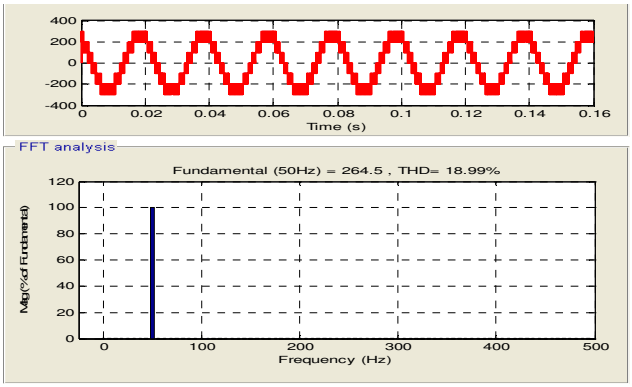

Figure 38: V_{LL} of the Proposed 5level at 0.6MI

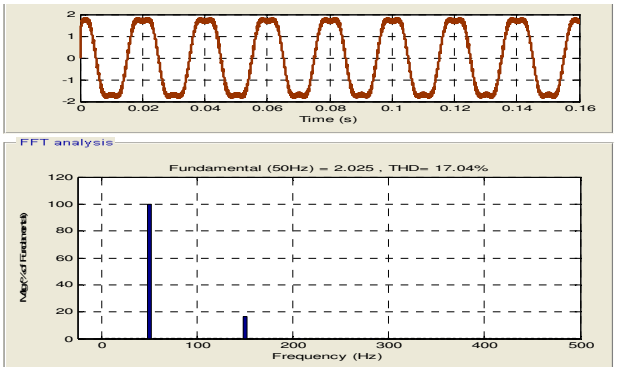

Figure40: Phase Current of the Proposed 5-level at 0.8 modulation index

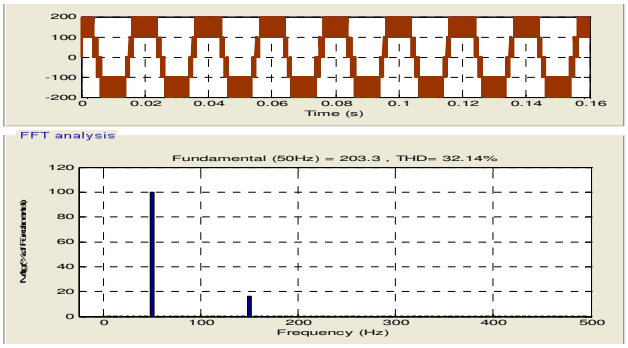

Figure 41: V_{an} of the Proposed 5level at 0.8MI

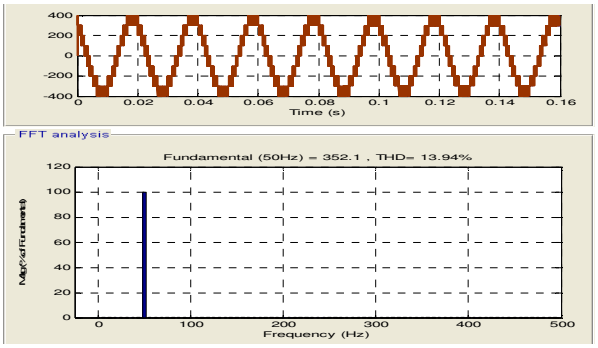

Figure 42: V_{LL} of the Proposed 5Level at 0.8 MI

The simulation analysis of the proposed topology at varying modulation indices indicates a sharp variation in the values of voltage magnitude and the corresponding total harmonic distortion as modulation index increases correspondingly for the proposed five-level topology.

Table 10: Voltage Magnitude and Percentage THD at Varied Modulation Indices.

Modulation index	Phase current (I_{AN}) Magnitude & %THD	Phase Voltage (V_{AN}) Magnitude & %THD	Line Voltage (V_{AB}) Magnitude & %THD
0.4	1.012 and 17.93%	101.6 and 51.13%	176.2 and 28.53%
0.6	1.521 and 17.46%	152.7 and 39.27%	264.5 and 18.99%
0.8	2.025 and 17.04%	203.3 and 32.14%	352.1 and 13.94%

Table 10 showed that as the modulation index increases, the voltage magnitude of the converter also increases with a proportionate decrease in the value of total harmonic distortion which is in conformity with the rule of a multi-level converter and in accordance with reference [20] that supports the validity of the general equation of %THD as presented in (10).

4. SIMULATION RESULTS DISCUSSION.

The spectral results presented in Table 9 and Figures 30-32 showed a clear picture of an improved percentage harmonic reduction using the proposed five-level topology with a phase current THD value of 4.24%, phase voltage THD value of 30.44% and line voltage THD value of 13.87%. These values indicate appreciable improvement in comparison to other discussed multi-level types as classified and presented in Table 9. Table 10 also confirmed the postulation that as the modulation index increases, the voltage magnitude of the converter also increases with a proportionate decrease in the value of total harmonic distortion which is in conformity with the general trend of a multi-level converter and in accordance with the general philosophy of %THD.

Table 8 above indicates that class A which is the 3Φ, 5level DCC has greater number of clamping diodes. This increases the problem of voltage imbalance along the d.c capacitor link that inherently exists in the diode clamped multi-level converter topology. Additionally, the cost of purchasing these eighteen clamping diodes of high power ratings makes this topology economically disadvantaged. Conduction losses emanating from reverse-recovering currents of the diodes during commutation also contribute to the economic infeasibility of this reviewed topology.

In class B, the 3Φ, 5level FCC it is observed that large number of clamping capacitors is required in the implementation of this circuit. This also increases the cost of design and practical implementation of this converter. The intermittent charging and discharging of the clamping capacitors also introduce fluctuations in the voltage level of this topology thereby reducing the reliability level of the steady state voltage magnitude.

In class C, the 3Φ, 5level CHB previous analysis drawn from technical reports showed that higher cost is involved in the generation of the six separate d.c power supply to the inverter input terminals. The input stages which include construction of more boost devices to produce the needed d.c voltage at the inverter supply terminal. This contributes to the cost of purchasing more components at the d.c input stage.

In class D, the 3Φ, 5level ANPC which is similar to class C, requires much cost in the d.c supply stage since three separate d.c power supply is needed to achieve this objective. The three clamping capacitors for the three phases also add to the high cost of achieving the practical implementation at reduced cost.

In class E, the 3Φ, 5level NPC/CHB the problem of greater number of clamping diodes abounds with separate d.c power supply as already discussed above and this therefore makes this topology uneconomical.

In class F, the 3Φ, 5level formed from 3Level NPC and Multiple 2Level inverter**,** contains six clamping diodes in its constituent structure. The positioning of the different two level inverter introduces complexities and a painstaking arrangement in the construction of this topology with the unavoidable d.c capacitor voltage imbalance associated with clamping diodes as earlier discussed as well as its high cost of purchase.

In class G, the proposed 3Φ, 5level Converter which is made up of three-level flying capacitor cascaded with 2level H-bridge and a single d.c supply reduces the complexities and cost associated with the aforementioned topologies. The simplicity of the proposed topology with reduced cost of components as depicted in Table 8 with its ruggedness and flexibility in operational mode of five and three level as shown in Figures 7a and 7b circuit diagrams ensures continuity and reliability to industrial and domestic applications.

5. CONCLUSION

A complete review has been carried out on seven different multi-level converters' topologies. The result analyses obtained have shown that a multi-level converter that can operate in dual states producing three level voltage and five level voltage independently can be achieved in a three level flying capacitor cascaded with H-bridge. The simulation results presented showed that with the proposed topology, some percentage of harmonic is reduced thus enhancing better performance of the proposed topology in high power applications. A better performance is achieved as the modulation index of the converter is increased within the acceptable modulation index range that is less than or equal to one. This is advisable to avoid the inherent emergence of lower harmonics associated with over-modulation which can result to excessive humming and overheating of the insulation level of most power devices applied in electric drives.

6. REFERENCES

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