A MICROPROCESSOR-BASED CONTROL, SCHEME FOR A PWM VOLTAGE-FED INVERTER WITH AN INDUCTION HEATING TANK LOAD

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ABSTRACT

In this paper, the flexibility of programmed control logic is exploited in the close loop control of a PWM thyristor voltage fed inverter supplying an induction heating tank load. The microprocessor used in the control is the MC6809 to which is interfaced the SY6522 versatile interface adapter (VIA). The microprocessor-based scheme performs the dual function of generating the thyristor gating signals as well as estimating and applying control actions to maintain the load power factor at unity and the power delivered to the load at a desired set-point value. The schemed also provides power circuit over-current and over-voltage protection against adverse changes in the inverter input supply and the load. The estimation of the control variables of the control scheme proportional plus integral controllers constitute the main control program while the application of thyristor gating signals and closed loop control actions are carried out in response to interrupts external to the microprocessor unit. Illustrative steady state and transient circuit of an experimental model of the induction heater are given.

1. INTRODUTION

Induction heating of metals is widely used in the industry for melting, casting, forging, annealing and /or hardening work. In majority of the medium power induction heating applications, the static power supply is the load commutated current source inverter (CSI) operating at leading power factor to reduce thyristor turn off losses [1,2.3]. But the CSI has limitation which include the requirement of a pre-stage converter circuit to regulate the inverter dc link current, the need for a relatively large dc link filter inductance, lack of self-starting capability and load dependent nature of the inverter output voltage. On the other hand, the PWM voltage source inverter (VSI) with force or self-commutated thyristor and /or transistors does not suffer from any of the above limitations. In addition, the ability of the PWM force /self –commutated VSI to supply the induction heating load at unity power factor minimizes circuit current and voltage stresses and the transmission (I^2R) losses in the induction heating system. Also, at low frequencies and at the lower region of the medium frequency range where thyristor force-commutation losses have negligible effect on circuit efficiency, the superiority of the PWM force-commutation VSI over the dc link load commutated CSI in supplying power to a parallel capacitor compensated induction heating load is evident.

This paper presents an MC6809 microprocessor based closed loop control of an induction heater comprising of a single pulse per half cycle modulated voltage fed inverter with a parallel capacitor compensated induction load. Three major single pulse modulation strategies are implemented to provide choice to the user depending on application requirements. These are the conventional zero voltage modulation and two other modulation schemes namely the zero current and the hybrid modulation schemes. As the inverter is self or force commutated, the load power factor is maintained at unity by a feedback loop that rapidly adjusts to zero any degree of de-tune between the natural tank load frequency and the inverter operating frequency. Other features of the software control scheme include feedback loops to regulate the heating power and to provide overload protection to the circuit devices and components. Steady state and transient circuit performance waveforms of an experimental model are also presented to demonstrate the viability of the software controlled induction heater.

2. THE CONTROLLED PWM VOLTAGE-FED INVERTER

The PWM voltage source inverter with a tank load is shown in Fig.1. The tank load consists of a small filter inductance L_f in series with a parallel capacitor compensated induction heating load (C_t in parallel with a series combination of L_t and R_t). Thyristors T_1-T_4 with their respective anti-parallel diodes, D_1-D_4, are the inverter main semiconductor switches. Each of the inverter main thyristor has a force commutation circuit consisting of an auxillary thyristor T_{xx} (x=1 to 4), an LC resonant circuit [Lc, Cc, D_{xx}(x=1 to 4)] and a bleeder circuit (R_{st}, R_d, D_d).

Three major PWM strategies of the inverter circuit are implemented to demonstrate the versatility and flexibility of the control scheme and the choice of any of the PWM strategy or a combination of any two of the PWM strategies depend on application requirements. These PWM strategies are the zero voltage modulation, the zero current modulation and the hybrid modulation, the zero current modulation and the hybrid modulation. Table 1 shows the load current conduction pattern of the inverter semiconductor devices for each PWM strategy.

The conventional zero voltage modulation strategy involves the application of full voltage (that is, the positive, $+V_s$, or the negative $-V_s$,) of the inverter dcinput voltage, V_s, across the inverter output for an angular distance δ radians in a half cycle of the inverter operating frequency. This is followed by the application of zero voltage across the same output for the rest of the half cycle.

In the zero current modulation, full voltage is applied across the inverter output for an angular interval δ in a half cycle to allow current flow to the load. This is followed by turning off all conduction main thyristors thus causing the reversal of the inverter output full voltage so as to force the load current to zero in an angular interval ε. The load current essentially remains at zero for the rest of the half cycle. Depending on the inverter output load impedance, there is a maximum value of $\delta=\delta_m$ at which $\delta_m+\varepsilon=\pi$ resulting in the attainment of maximum inverter output voltage for a given inverter input voltage.

In the hybrid modulation technique, full voltage is applied across the inverter output for an angular interval δ in a half cycle. Then zero voltage in next applied across the inverter output to make the load current to decay to zero in an angular interval ε. For values 0f δ where $\delta+\varepsilon \geq \pi$, this modulation technique becomes the same as the zero voltage modulation.

An effective modulation technique is the dual modulation method where by zero voltage is used for steady state operation while zero current modulation is used for overload protection under transient condition during start up, induction load variation and/or change in inverter input supply voltage

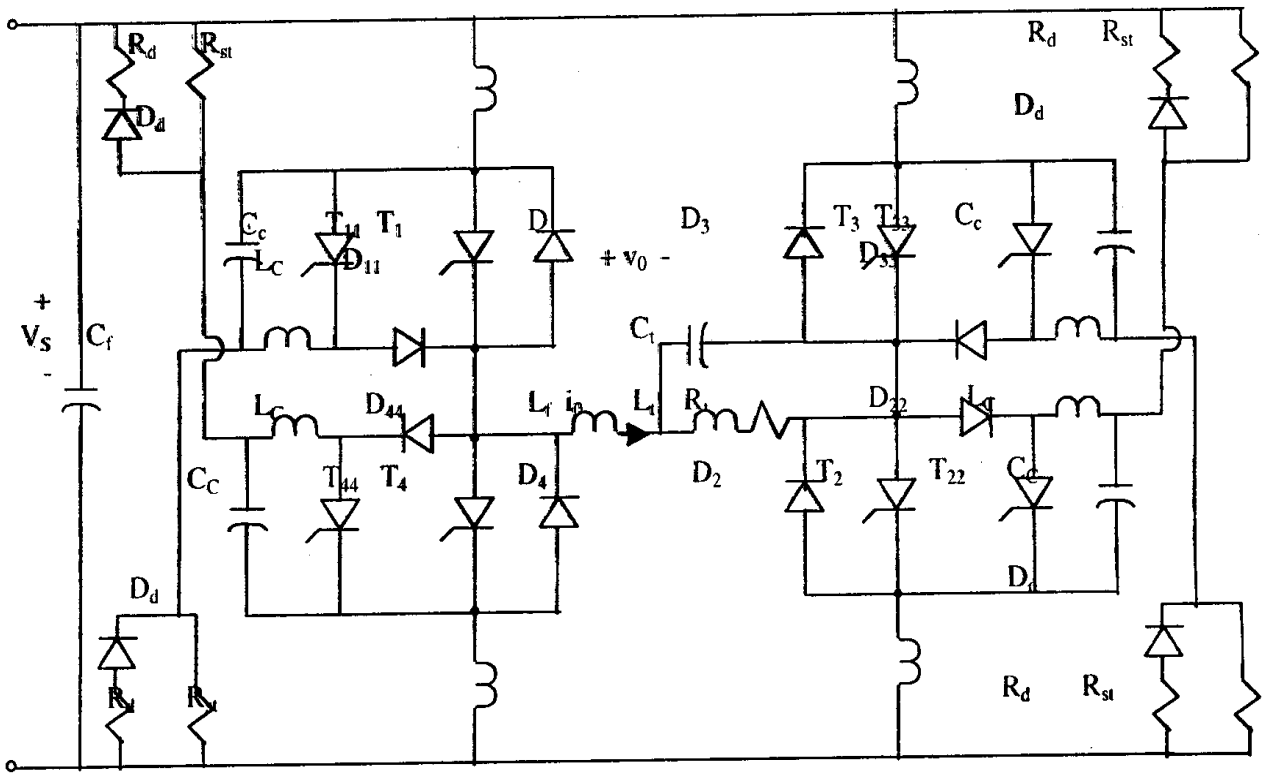


Fig. 1: The PWM Single Phase Voltage Source Inverter with an Induction Heating Tank Load.

Table 1: Inverter Semiconductor Device Load Current Conduction in a Switching Cycle.

PWM Type	Semiconductor Devices Conducting					
Zero Voltage	(D_1, D_2) or (T_1, T_2)		(T_2, D_4) or (D_2, T_4)		(D_3 D_4) or (T_3, T_4)	(D_1, T_3) or (T_1, D_3)
Zero Current	T_1, T_2		D_3 D_4		T_3, T_4	D_1 D_2
Hybrid	T_1, T_2		T_1 D_3		T_3, T_4	D_2 T_4
0		δ	$\delta+\varepsilon$	π	$\pi+\delta$	$\pi+\delta+\varepsilon$ 2π

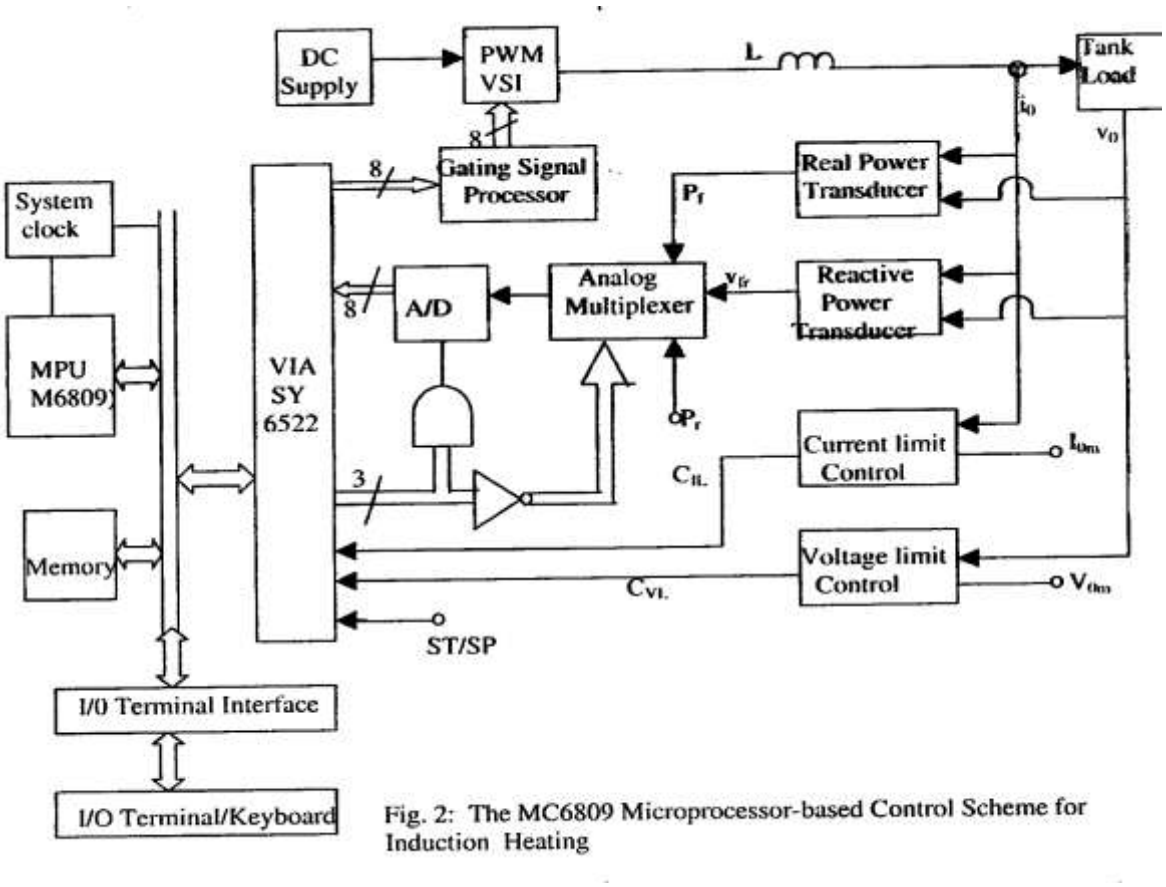


Fig. 2: The MC6809 Microprocessor-based Control Scheme for Induction Heating

3. THE MICROPROCESSOR CONTROL SCHEME

In this section, the microprocessor based control scheme for the induction heating circuit of fig.1 is presented. The presentation covers the description of the hardware setup, thyristor gating signal generation and regulatory feedback arrangements

3.1. HARDWARE DESCRIPTION

Fig.1 shows the functional block diagram of the microprocessor based control scheme. The brain of the control scheme is the M6809 microprocessor unit (MPU). The MPU, the memory and the versatile Interface Adapter (VIA) make up the microcomputer system. These three elements are interconnection by a bus system containing data the address and the control lines. A system clock (of about 1MHz frequency) controls the time the microprocessor takes to execute any one instruction or command signal to the computer is by the use of an 1/0 terminal and a keyboard connected to the system, bus.

The MPU controls, at a rate determined by the system clock, all computer operation initiated by an external command. The software control program as well as the data needed or generated in the progrom execution are stored in the memory. The VIA interfaces the MPU and the memory with the external gating signal transmission and feedback circuit.

One 8-bit VIA register is programmed as an output through which the microcomputer provides gating signals to the eight inverter thyristors. A second 8-bit VIA register is programmed as an input through which digitized information from the inverter and its tank load is transmitted through the A/D converter to the microcomputer. Three other output lines from the VIA are programmed to control the analogue multiplexer and the A/D converter used for reading the feedback and set-point variables at predetermined sampling instants.

3.2 GENERATION OF THE THYRISTOR GATING SIGNALS

The method of generating the thyristor gating signals (i_{GT}^{S}) is illustrated in fig. 3and table 2 with the dual modulation strategy (zero voltage modulation at steady state and zero current modulation under overload or current limiting condition). The gating signal generation is controlled by identifiable sources. These sources are the two programmable. Timers (TX1and TX2) in the VIA and two other sources namely the load current limit pulse (C_{IL}) and the load voltage limit pulse (C_{Vl}) as shown in fig. 3 when interrupted by forcing the Interrupt Request (IRQ)' input low, the microcomputer applies to the inverter thyristor appropriate gating signals as determined by any one of the above source of interrupt. These gating signals are stored in the memory and are accessed using the index addressing mode.

3.2.1 STEADY STATE THYRISTOR GATING

Figure 3(a) shows the basic principle of gating signal generation at steady state. Timer 1(TX1) of the VIA runs at continuous mode and the variation with time of the content ([TX]) of a counter in this timer is as shown. Any time this counter decrements at system clock rate to zero (from a predetermined value U_{TI}), the Timer 1interrupt flag IF_{TI} is set thus interrupting the MPU to apply appropriate gating signal for full voltage (that is $+V_s$ or $-V_s$) across the inverter output. At the same time, this counter of Timer 1is updated or re-triggered with the value U_{TI} so that it starts counting down to zero at which

value IF_{TI} again interrupts the counter to apply reverse full voltage (-V or +V) across the inverter output. Timer 2 (TX2), on the other hand, runs at one shot mode and the variation of its counter content ([TX2]) with time is also shown in fig. 3(a). This counter is re-triggered with a value U_{T2} at the same time as that of Timer 1. At any re-triggered instant, U_{T2} is at least less than U_{T1} by a value determined by the turn of time of the inverter main thyristors. When the counter of Timer 2 decrements at system clock rate to zero, the corresponding interrupt flag IF_{T2} is set thus interrupting the MPU to apply appropriate gating signals for zero load voltage across the inverter output. The Timer 2 counter continues to decrement from zero until it is again re-triggered with the value U_{T2} at the starts of the next full voltage interval. It (counter of TX2) then starts another countdown resulting in repeated operation that generates a series of interrupt commands $IF_{T2}$for zero inverter output voltage.

3.2.2 Gating During Transients for Overload Protection

Figure 3(b) shows gating signal generation during transient period under over-current or over-voltage limiting action. An instantaneous load current limit feedback (shown in fig.2) limits the instantaneous inverter output current i_o to a predetermined maximum value $I_{om,}$ to ensure reliable turn on and turn off of the inverter thyristors. If i_o tries to exceed I_{om}, an amplitude comparator generates a current limit pulse C_{IL} to interrupt the microprocessor by setting the interrupt flag IF_C (fig. 3(b). the interrupt causes the microprocessor to generate appropriate gating signals to commutate all conducting thyristors to limit load current. Gating action for full voltage is re-initiated at the next Timer 1 interrupt. The tank load coil and compensating capacitor are similarly protected against excessive peak voltage by the load voltage limit pulse C_{VL} which sets the interrupt flag IF_V any time the tank load voltage exceeds the load voltage limit value V_{om}

3.2.3 start /stop command

A start/stop input (ST/SP) is also provided in the control scheme of fig. 2. A high logic signal at this input instantly enables all gating signals to the inverter thytristors. On the other hand , a low logic input disables all gating signals to give the thyristors and simultaneously turns off all conducting thyristors.

3.3 the gating waveform buffer

The gating waveform buffer is a designated memory location that contains the per cycle thyristor gating signals for a given modulation strategy. Table 2 gives the waveform buffer for the dual modulation method. The content of each memory location in this buffer is shown in relation to the inverter thyristor being controlled. The buffer, which has 20 memory location each of 1byte length, is divided into four distinct parts representing the four main inverter conducting intervals in one cycle of inverter operation. These main conducting intervals are the full voltage interval (FV+), the two zero voltage intervals (ZV) and the full negative voltage interval (FV). Each of these four distinct parts contains 5 bytes of waveforms.

The way the gating signal interrupt routine uses the waveform buffer of Table 2 can be explained by initially assuming that Timer 1 has interrupted the computer for the application of a positive voltage across the inverter load terminals. The cycle gating sequence will then take the form:

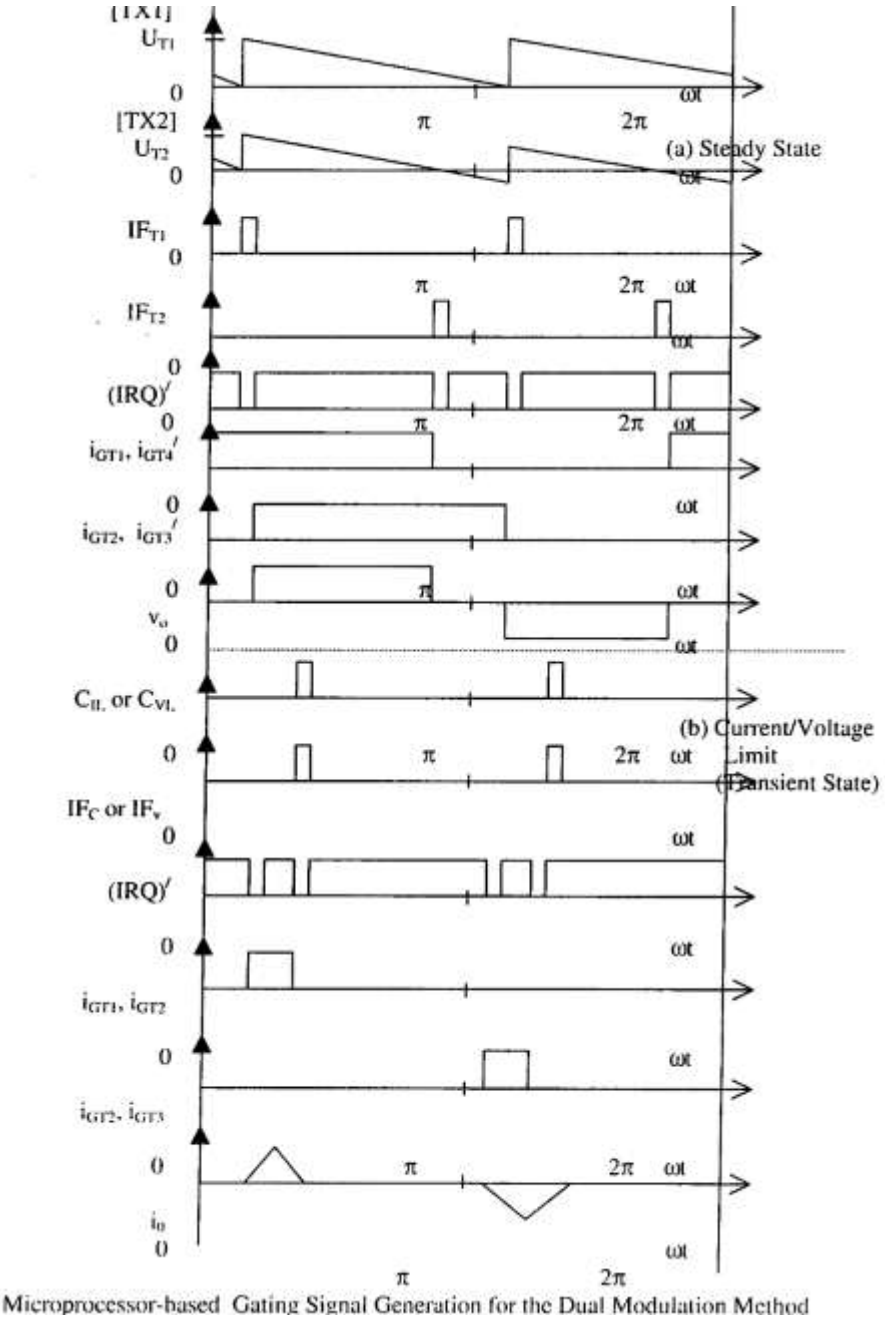
(i) In response to Timer 1 interrupt flag (IF_{TI}), byte 1 is a set of gating waveforms applied to the inverter thyristors for full positive output voltage (T_1 and T_2 conducting)

(ii) If Timer 2 interrupt flag (IF_{T2}) becomes set during this positive full output voltage interval, byte 2 is the gating waveform for the next 20 μsecs followed by byte 4 for the next 100 μsecs after which byte 6 is applied as gating signals to get zero inverter output voltage. In response to IF_{T2} interrupt flag therefore, T_1 is turned off while T_4 is simultaneously turned on.

(iii) If the current limit or the voltage limit command pulse (C_{IL} or C_{VL}) interrupt the processor during the positive full voltage interval, the processor applies byte 3 as the gating waveform for 20μsecs to turn off all conducting thyristors and force the load current to zero for the rest of the half cycle. Gating action is resumed on the next occurrence to Timer d1 interrupt by applying byte 11 to give negative full inverter output voltage.

(iv) If the current limit or voltage limit interrupt flag is received during the commutation of T1 after a full positive voltage interval, byte 5 is applied for 20 μsecs to commutate the remaining thyristor (T_2) and force the load current to zero for the rest of the half cycle. Gating action is again resumed on the next occurrence of Timer 1interrupt by applying byte 11 to negative full inverter output voltage for full negative inverter output voltage.

The above explanation for the positive full voltage interval can easily be extended to the negative full voltage interval to complete a cycle of operation. Gating signal buffers for other modulation methods (as show in table 1) are similarly stored in memory and the inverter operation can easily (through minor change in the software control program) be switched to any of the these modulation methods.



Microprocessor-based Gating Signal Generation for the Dual Modulation Method

3.4 load power factor and load power control

In the control scheme, both the load power factor and the load power are, in accordance with the nature and requirements of the induction heating load, maintained by closed loop control arrangement at desired set-point values for high system performance.

Table 2: The inverter thyristor gating waveform buffer for the dual modulation strategy of Fig. 3.

Memory Location	Byte No.	Content of Memory Location (Binary)								Hex.
		T_{44}	T_{33}	T_{22}	T_{11}	T_4	T_3	T_2	T_1	
		FV+								
0100	1	0	0	0	0	0	0	1	1	03
0101	2	0	0	0	1	0	0	1	0	12
0102	3	0	0	1	1	0	0	0	0	30
0103	4	0	0	0	0	0	0	1	0	02
0104	5	0	0	1	0	0	0	0	0	20
		ZV								
0105	6	0	0	0	0	1	0	1	0	0A
0106	7	0	0	1	0	1	0	0	0	28
0107	8	1	0	1	0	0	0	0	0	A0
0108	9	0	0	0	0	1	0	0	0	08
0109	10	1	0	0	0	0	0	0	0	80
		FV−								
010A	11	0	0	0	0	1	1	0	0	0C
010B	12	1	0	0	0	0	1	0	0	84
010C	13	1	1	0	0	0	0	0	0	C0
010D	14	0	0	0	0	0	1	0	0	04
010E	15	0	1	0	0	0	0	0	0	40
		ZV								
010F	16	0	0	0	0	0	1	0	1	05
0110	17	0	1	0	0	0	0	0	1	41
0111	18	0	1	0	1	0	0	0	0	50
0112	19	0	0	0	0	0	0	0	1	01
0113	20	0	0	0	1	0	0	0	0	10

In load power factor control, a sensed signal of the tank load voltage V_o is integrated and the result multiplied by a sensed signal of the inverter output current i_o. The product is low pass filtered to obtain a dc voltage signal V_{fr} proportional to the load reactive power.

$$V_{fr} = K_o V_{o1} I_{o1} \cos(\phi_{o1} + \pi/2) \quad (1)$$

In equation 1, V_{o1} and I_{o1} are respectively the rms fundamental tank load voltage and inverter output current, ϕ_{o1} is the phase angle of I_{o1} relative to V_{o1} while K_o is the sensor attenuation constant. A digital PI controller algorithm, defined by software, is used to maintain the load power factor at unity under load variation. This PI controller algorithm computes the power factor control signal U_{T1}(mTs) as

$$U_{T1}(mT_s) = U_{T10} - K_{11}T_s \sum_{m=1}^{m}[V'_{fr}(mT_s)] - K_{p1}V_{fr}(mT_s) \quad (2)$$

In equation 2, U_{T1} (mT_s) is the computed re-triggering value for timer 1 counter at the m^{th} sampling time., U_{T10} is the value of U_{TI} at time t = 0, V_{fr},'(mT_s) is the digitized feedback value of the reactive load at the m^{th} sampling time, T_s, is the sampling period, while K_{11} and K_{pl} are respectively the integral and proportional gains of the power factor PI controller. For a leading load power factor V_{fr},' is negative (equation I). As a result, the re-triggering value, $U_{TI}(mT_s)$, is increased at each sampling period thus decreasing the interrupting rate of Timer I. This in turn decreases the inverter operating frequency till V_{fr}, is zero thus indicating operation at unity loadpower factor. In a similar manner, a lagging load power factor decreases U_{TI} (mT_s) thus increasing the inverter operating frequency until the load power factor is unity.

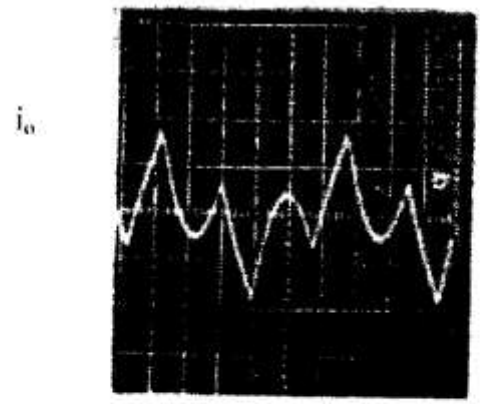
For load power control, both the power feedback signal P_f. and the power reference signal P_r, arc sampled by the processor at the same rate. The power PI controller, defined by software, uses the difference between P_f and P_r to compute the power

$$U_{T2}(mT_s) = U_{T20} - K_{12}T_s \sum_{m=1}^{m}[P'_r(mT_s) - P'_r(mT_s)] - kp^2[P'_r(mT_s) - P'_f(mT_s)] \quad (3)$$

In equation 3, $U_{T2}(mT_s)$ is the re-triggering value for Timer 2 at the m^{th} sampling time, U_{T20} is the triggering value of Timer 2counter at time t=0, P_r'(mT_s)and P_f'(mT_s, are respectively the digitized control signal using the equation:

Values of the load power set-point and load power feedback at the m^{th} sampling time, T_s is

the sampling period while K_{12} and K_{p2} are respectively the integral and proportional gains.



i_o (a) Zero Voltage PWM ($\delta = 65^o$)

(Load Current i_o – 5A/div., 0,5ms/div.)

i_o (a) Zero Voltage PWM ($\delta = 65^o$)

(Load Current i_o – 5A/div., 0,5ms/div.)

i_o (c) Start-up Transient of Dual PWM ($I_{om} = 1.25 i_{op}$)

(Load Current i_o – 10A/div., 2ms/div.)

v_o (Load Voltage v_o – 100V/div., 2ms/div)

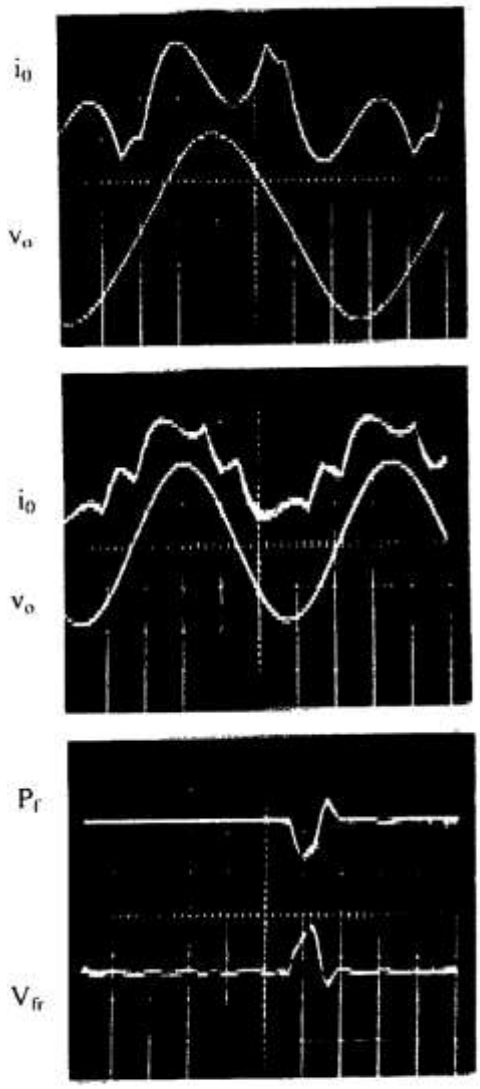
Fig. 4: Experimental Steady State and Start-up Transient waveforms f or the Inverter with a Tank Load (V_s=189V, X_{Lo} = 6.8Ω, Z_{to} = 34 Ω, C_t = 130μF)

4. EXPERIMENTAL WAVEFORMS OF A LABORA TORY MODEL

Figures 4 and 5 illustrate some performance experimental results obtained from a laboratory model of the microprocessor controlled induction heater. Figures 4(a) and 4(b) show the steady state inverter output current waveforms when zero voltage and zero current modulation methods at $\delta = 65°$ are respectively used to control the inverter output voltage. Fig4(c) also shows the start up transient waveforms of the tank load current i_o and voltage Vo under the dual modulation mode of operation and with the load current limit value I_{om} set to 1.25 times the steady state peak load current i_{op}. The load parameters, namely R_{to}, X_{Llo}, and X_{Lfo}. are respectively the impedances of R_t L_t, and L_f (Fig. I) measured at the resonant frequency f_oHz of the tank load.

The hybrid modulation method was also used to demonstrate the effectiveness of the load power factor and load power control action. The result is given in figure 5 which shows the transient response of the load real power p_f and reactive power V_{fr} feedback signals under a step change in heating load impedance (R_{to}+ jX_{Lto}) at constant load power and power factor demand. It is seen that for a

step change in $(R_{to}+ jX_{Lto})\Omega$ from (0.46 +j4.6) Ω, to (0.33 + j3.3) Ω the power control variable δ changed from 160.5^0 to 113^0 to maintain the load power constant (i.e p_f constant) while the power factor control variable f_o changed from 259Hz to 360 Hz maintain the load power factor constant at unity (i .eV_{fr} constant).



(a) Initial Steady State
$R_{to} + jX_{Lto} = (0.46+j4.6)\Omega$, $\delta=160.5^o$
f_o =259Hz
(Load current i_o –5A/div, 0.5ms/div)
(Load voltage v_o –100V/div, 0.5ms/div)

(b) Final Steady State
$R_{to} + jX_{Lto} = (0.33+j3.3)\Omega$, $\delta=113^o$
f_o =360Hz
(Load current i_o –5A/div, 0.5ms/div)
(Load voltage v_o –100V/div, 0.5ms/div)

Load Power Feedback Signal P_f
(2V/div, 0.2secs/div)

Load Reactive Power Feedback Signal V_{fr}
(2V/div, 0.2secs/div)

Fig. 5: Hybrid Modulation: Illustrative Steady State and Transient Waveforms under Step Change in Tank Load Resistance and Inductance {0.46 + j4.6 to 0.33 + j3.3)Ω at constant tank load Power of 480W (X_{Lo}=3.4Ω, V_s=180V, I_{om}=2.7i_{op}), Ct = 130μF)

5. CONCLUSIONS

In this paper, an MC6809 microprocessor-based control of a PWM single phase voltage source inverter supplying an induction heating tank load has been presented. Three single pulse per half cycle modulation methods of the inverter output voltage have been described. These are the zero voltage, the zero current and the hybrid single pulse modulation methods. These basic three modulation techniques have been implemented using the MC6809 microprocessor and appropriate interface accessories. The effectiveness, versatility and flexibility of the control scheme has been demonstrated by using each or the modulation methods (embedded in a common MC6809 assembly language program) to closed loop control the inverter with the induction heating tank load. The control scheme gave high steady state and transient performance under varying load conditions.

The inverter operating frequency rapidly changed automatically under varying tank load

to maintain the load power factor constant at unity. For given load power set-point value, the load power was maintained constant. The scheme also gave accurate and fast overload protection. At medium power and at the medium frequency range of 200Hz-I kHz the reported induction heater scheme is a viable alternative to the current Source inverter and cycloconverter- based schemes.

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