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A REVIEW ON REVERSIBLE LOGIC GATES

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ABSTRACT
In recent years, reversible logic circuits have applications in the emerging field of digital signal processing, optical information processing, quantum computing and nano technology. Reversibility plays an important role when computations with minimal energy dissipation are considered. The main purpose of designing reversible logic is to decrease the number of reversible gates, garbage outputs, constant inputs, quantum cost, area, power, delay and hardware complexity of the reversible circuits. This paper reveals a comparative review on various reversible logic gates. This paper provides some reversible logic gates, which can be used in designing more complex systems having reversible circuits and can execute more complicated operations using quantum computers. Future digital technology will use reversible logic gates in order to reduce the power consumption and propagation delay as it effectively provides negligible loss of information in the circuit.
Keywords: Garbage output, Power dissipation, quantum cost, Reversible Gate, Reversible logic,

INTRODUCTION

In present day technology, Reversible logic has spread its popularity in numerous technologies, due to their ability to reduce the power dissipation which is the main requirement in low power VLSI design (Yelekar & Chiwande, 2011). Applications of the Reversible circuits can be found in the emerging fields of low power CMOS design, optical information processing, DNA computing, quantum computing and nano technology (Markle & Drexler, 1996).

Traditional logic circuits are Irreversible which result in energy dissipation and information loss (Biswas *et al*., 2014). Landaurer's Research has proved that the amount of energy dissipated for every irreversible bit operation is atleast kTLn2 joules, where is k is the Boltzmann's constant and T is the temperature in Kelvin (Landaurer, 1961; Parhami, 2006). In 1973, Bennett showed that in order to avoid kTLn2 joules of energy dissipation in a circuit it must be built from reversible circuits (Bennett, 1973). The amount of energy dissipated in a system bears a direct relationship to the number of bits erased during computation (Mamataj *et al*., 2014). Reversible circuits are those circuits that do not lose information.

Reversible logic gates are required to design reversible circuits (Biswas *etal*., 2014). A reversible logic gate has equal input and output in order to have one to one mapping (Biswas *etal*., 2014). In reversible circuit there should be no fan-out; that is, each output will be used only once and for each input pattern there should be unique output pattern.

In the year 2007 (James et al., 2007) implement a low power circuit using reversible logic that provides single error correction – double error detection (SEC-DED). The design was done using a new 4 x 4 reversible gate called Hamming Code Generating (HCG) for implementing hamming error coding and detection circuits. A parity preserving Hamming Code Generating (PPHCG) that preserves the input parity at the output bits is used for achieving fault tolerance for the hamming error coding and detection circuits.

Rashmi, & Tilak, (2011) invented a reversible gate known as Binary Coded Decimal subtraction correction logic (BSCL). The main purpose of introducing this gate is either to find correction logic for BCD subtraction or to pass same data to the output.

Misra, & Wairya, (2015) demonstrated a reversible BCD adder and carry skip BCD adder circuit based on three new type of reversible gates, namely; Full adder subtraction (FAS), Half adder subtraction (HAS) and Overflow detection (OD) gates, to optimize the adder circuits. The new type of reversible full adder using FAS gate is the best circuit in terms of quantum cost. By utilizing those three new types of gates, reversible n-digit BCD adder and 1-digit carry skip BCD adder are proposed with its algorithm.

Misra, & Sen, (2017) invented two kinds of novel error control circuits such as hamming code, parity generator and checker. To design the HG-PP (HG = Hamming gate, PP = Parity

preserving), NG-PP (NG = New gate) are proposed for optimising the circuits. Based on the proposed gates and few existing gates, the hamming code and parity generator and checker circuits are constructed. The reversible, major metrics such as gate count, quantum cost, unit delay, and garbage outputs, uses best optimisation results compared to counterparts. They can be utilised as a low power error control circuit applied in future communication systems.

Bhoi, K.B, & Misra, N.K. (2017) introduced a new gate named as universal reversible QCA gate (URQG) is proposed. It is a 3×3 gate that realizes 13 standard functions with optimal gate count. 2. The URQG gate is compared with the existing reversible gates using standard Boolean equations. The proposed gate outperforms the existing gates in terms of design cost and testing overhead. An n-bit comparator, was synthesised where proposed URQG and existing Feynman gates are cascaded together.

BASIC DEFINITIONS OF REVERSIBLE LOGIC

1. REVERSIBLE FUNCTION

A function $f \in B_{n.n}$ is called reversible if f is bijective, i.e., if each input pattern is uniquely mapped to a corresponding output pattern and vice versa. Otherwise, it is called irreversible. Clearly, if f is reversible, then its number of inputs is equal to the number of outputs. In other words, each reversible function $f \in B_{n.n}$ is a bijection that performs a permutation of the set of input patterns (Abdessied & Drechler, 2016). An irreversible function can be embedded into a reversible specification by adding extra variables to achieve a bijective function. An embedding is not unique and the choice of embedding can have a very significant effect on the number of the variables of the resulting function (Miller *et al.*, 2009; Soeken *et al.*, 2015).

REVERSIBLE LOGIC GATE

A reversible logic gate is an n-input n-output logic device with one-to-one mapping (Yelekar & Chiwande, 2011), the number of inputs are equal to the number of the outputs of the gates in order to have a one-to-one mapping. This generates a unique set of output vector for each set of input vector (Biswas *et al.*, 2014). This prevents the loss of information which causes power dissipation. In reversible logic, fan-out is not possible and feedback or loops are not allowed. Some features of a reversible logic circuit are: Minimum input constants, Minimum number of reversible gates and Minimum number of garbage outputs.

REVERSIBLE CIRCUIT

A combinational reversible circuit is an acyclic combinational logic circuit in which all gates are reversible, and are interconnected without explicit fan-outs and loops. Boolean functions can be synthesized to a reversible circuit after embedding them to reversible functions. Therefore, in general a reversible circuit contains n inputs with p primary inputs and c constant inputs with p + c = n. At the output side, there are m primary outputs and k garbage outputs with k + m = n. Figure1 depicts the general structure of a reversible circuit (Abdessied & Drechler, 2016). A reversible circuit should be designed using minimum number of reversible logic gates, minimum input constant, minimum number of garbage outputs.

Figure 1: Reversible Circuit Structure

GARBAGE OUTPUT

Unwanted output of reversible gate is called garbage output. The output of reversible gate is not used as a primary output or as input to other gates is called garbage output. Garbage's outputs are needed in circuit to maintain reversibility concept. Figure 2 shows an example of reversible function f=$x_1 x_2\ XOR\ x_3$, the two unused pins are the garbage outputs (Ankush & Bhandari, 2016).

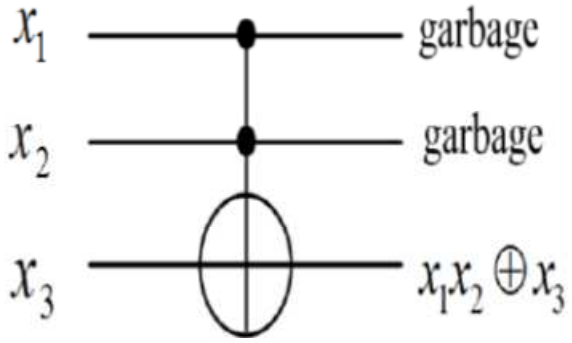

Figure 2: Garbage output

CONSTANT INPUTS

This can be defined as the number of inputs that are to be maintain constant at either 0 or 1 in order to synthesize the given logical function (Thapiyal & Ranganathan, 2010).

QUANTUM COST

Quantum cost may be defined as the cost of the circuit in terms of the cost of a primitive gate. It is calculated by the number of primitive reversible logic gates (1x1 or 2x2) required to realize the circuit. The quantum cost of a circuit is the minimum number of 2x2 unitary gates to represent the circuit keeping the output unchanged. The quantum cost of a 1x1 gate is 0 and that of any 2x2 gate is the same, which is 1(Smoline & David, 1996).

DELAY

The delay of a logic circuit is the maximum number of gates in a path from any input line to any output line. The definition is based on two assumptions: (i) Each gate performs computation in one unit time and (ii) all inputs to the circuit are available before the computation begins. (Mohammadi & Eshghi, 2009).

HARDWARE COMPLEXITY

Hardware Complexity refers to the total number of logic operation in a circuit. Means the total number of AND, OR and EXOR operation in a circuit (Akbar *et al.*, 2011).

REVERSIBLE LOGIC GATES

There are many number of reversible logic gates that exist in present literature. Some of the reversible gates are presented by (Ankush & Bhandari, 2016). In this review we try to show other reversible gates which are not presented by (Ankush & Bhandari, 2016) and may be useful to researchers. The reversible gates are given below;

SG Gate

SG gate is also known as Sayem gate (Sayem& Ueda, 2010) is a 4x4 reversible gate. The input and output vector of this gate are, Iv = (A, B, C, D) and Ov = $\left(A, A'B \oplus AC, A'B \oplus AC \oplus D, AB \oplus A'C \oplus D\right)$. The block diagram of this gate is shown in Figure 3.

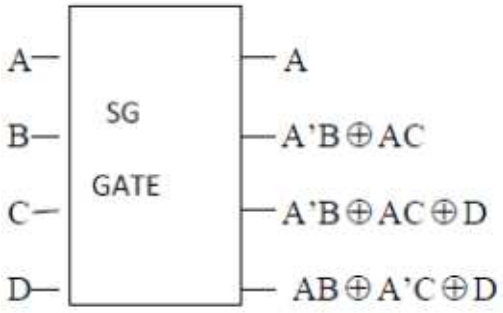

Figure 3: Sayem gate

BME Gate

BME gate is a 4 × 4 reversible gate (Mahfuzzreza *et al.*, 2013). The BME gate can be described as: IV = (A, B, C, D); OV = (A, AB⊕C, AD⊕C, A'B⊕C⊕D), where IV and OV are input and output vectors respectively. Quantum cost of BME gate is five (Garipelly *et al.*, 2013). Figure 4 shows a 4 × 4 BME gate.

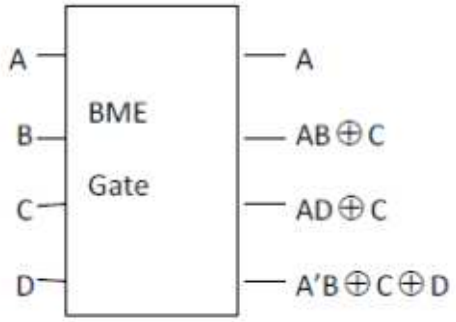

Figure 4: BME Gate

BSCL Gate

Binary Coded Decimal Subtraction Correction logic gate is a 6x6 reversible gate. The purpose of this gate is either to find correction logic for BCD subtraction or to pass same data to the output depending on the control signal (Rashmi *et al.*, 2011). Here F is the control signal as shown in the figure if F is equal to 0, A, B, C, D and E as it is passed to the output P Q R S and T. If F is equal to 1, then output Q R S and T depends on the value of E. If E is equal to 0 then Q R S and T is the nines compliment of the input binary number A B C and D. If E is equal to 1 then binary number 0001 is added to ABCD to get the valid corrected subtraction result.

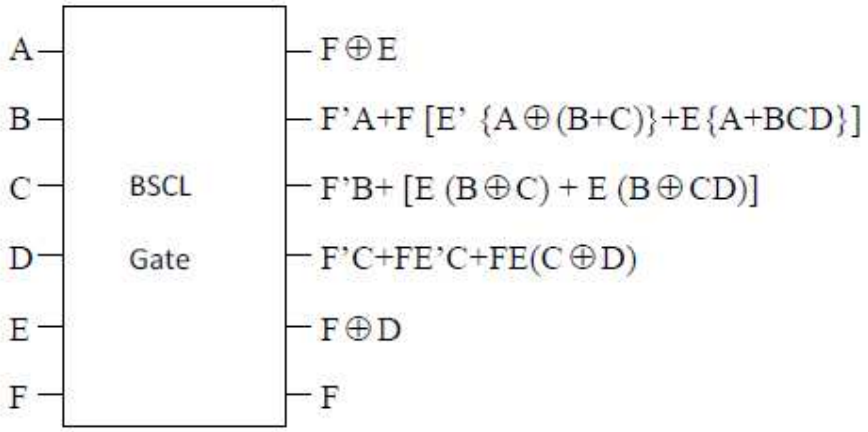

Figure 5: BSCL Gate

PTR Gate

PTR gate is a 4X4 Reversible gate that can work as a reversible full adder

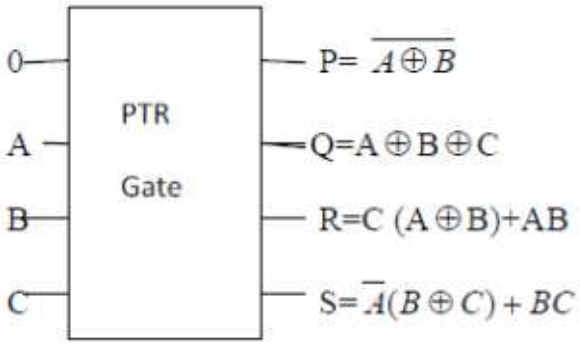

Figure 6: PTR Gate

PAREEK GATE

PAREEK gate is a 4 × 4 reversible gate (Pareek *et al.*, 2014). The PAREEK gate can be described as: IV = (A, B, C, D); OV = (A, A'B⊕AD, A'B⊕AD⊕C, B⊕D), where IV and OV are input and output vectors respectively. Quantum cost of PAREEK gate is seven which is illustrated in (Pareek *et al.*, 2014). Figure 7 shows a 4 × 4 PAREEK gate.

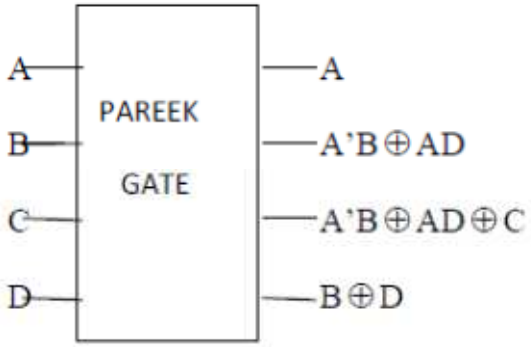

Figure 7: Pareek Gate

RCQCA GATE

Reversible Conservative quantum dot Cellular Automata gate is a 4 × 4 reversible gate (Misra *et al.*, 2018). Quantum cost of 6. This gate is utilised for Sequential circuit synthesis of reversible functions

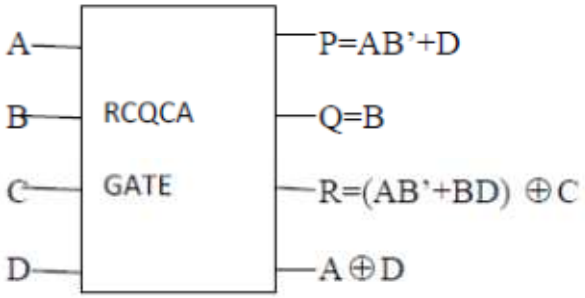

Figure 8: RCQCA Gate

URQG GATE

Universal Reversible Quantum dot Cellular Automata Gate is a 3x3 reversible gate (Bhoi *et al.*, 2017). Based on reversibility given the outputs logic P, Q, R the inputs A, B, C can be computed. The reversible URQG gate is a universal gate and can implements 13 standard functions. By combining two URQG gate N-bit comparator can designed.

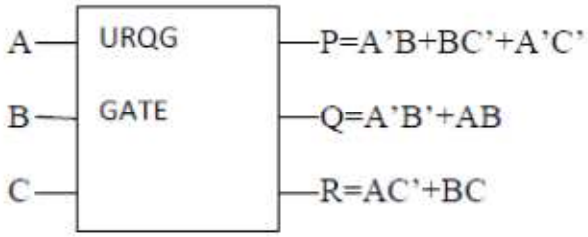

Figure 9: URQG Gate

HCG GATE

A 4x4 reversible gate, Hamming Code Generating gate (James *et al.*, 2007) is depicted in Figure 10. HCG gate is one-through gate which means that one of the input variables is also output. Hamming error coding and detection circuit can be implemented using this gate

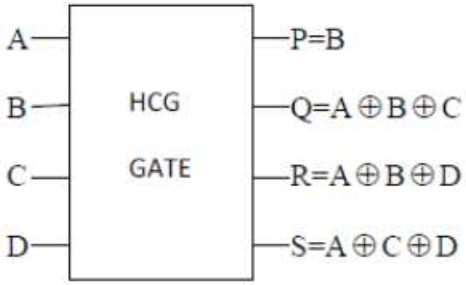

Figure 10: HCG Gate

HAS GATE

Half Adder Subtraction gate is a 3x3 reversible gate which is helpful for the design of reversible BCD adder and carry skip BCD adder circuit. The HAS gate has a quantum cost 5. It consist of four XOR gates, two controlled-V and one controlled-V^+ gate. This gate can implement the operation of haif adder and full subtraction. (Misra *et al.*, 2015).

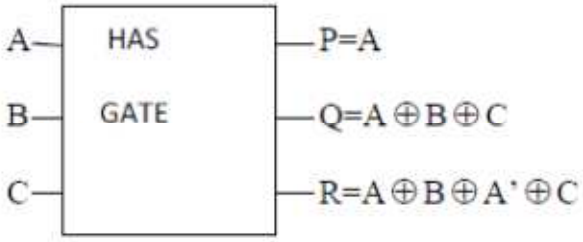

Figure 11: HAS Gate

FAS GATE

Full Adder Subtraction gate is a 4x4 reversible gate. FAS gate can perform the operation of full adder and full subtraction. The gate has a quantum cost of 8. It consist of six XOR gates, two controlled-V and one controlled-V^+. (Misra *et al.*, 2015).

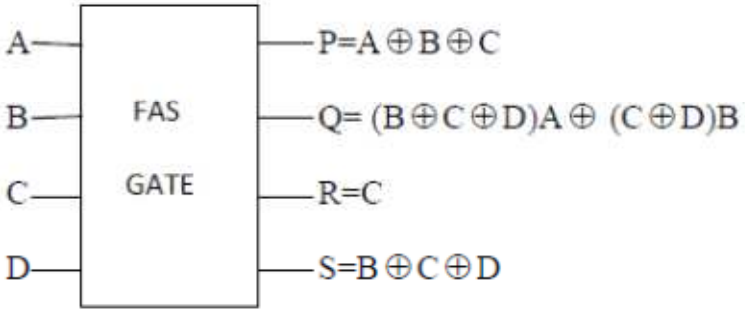

Figure 12: FAS Gate

OD GATE

Over flow Detection gate is a 5x5 reversible gate. The OD gate has a quantum cost of 10. It consist of seven XOR gates, four controlled-V and two controlled-V^+ gate. OD gate is used for overflow detection. (Misra *et al.*, 2015).

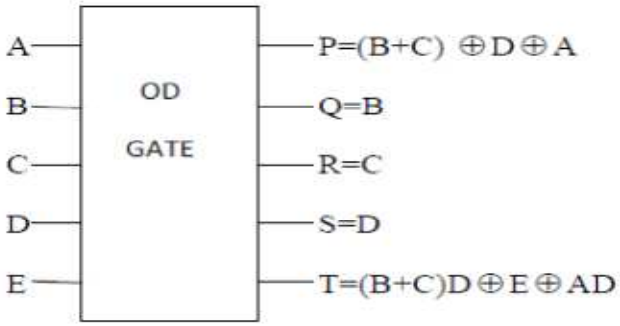

Figure 13: OD Gate

PPHCG GATE

Parity Preserving Hamming Code Generating gate is a 4 x 4 Parity Preserving Reversible gate. The outputs preserve the input parity (James *et al.*, 2007).This gate can be used for achieving fault tolerance for the hamming error coding and detection.

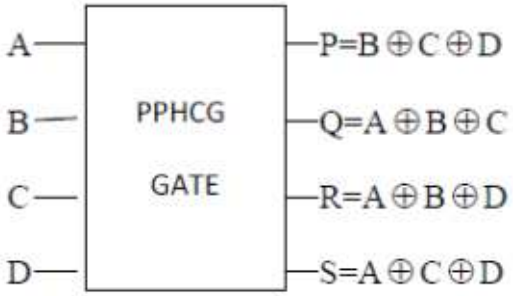

Figure 14: PPHCG Gate.

NG-PP

The NG-PP structure is utilised of 5-input and 5-output. The input parity to output parity is conserved. Hence this gate is a conservative gate. Further, it holds the bijective mapping, it also the reversible gate. The QC of NG-PP gate is 5(Misra *et al.*, 2017). It can singly perform the logic operation of parity generator and checker.

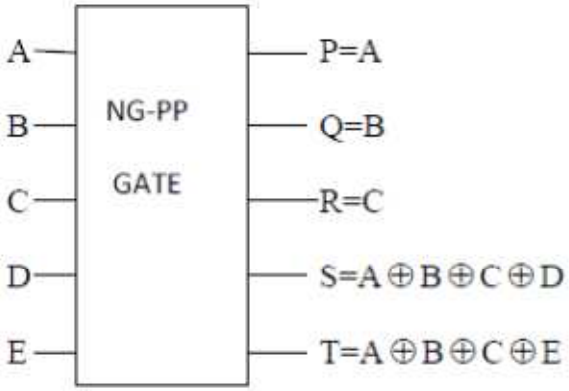

Figure 15: NG-PP Gate

HG-PP GATE

A 5 x 5 conservative reversible logic gate named HG-PP is shown in Figure16.. It depicts the same count of 1's in the output as well as input, further maintain the bijective-mapping property of the reversibility. Hence this gate is reversible as well as conservative. The QC of HG-PP gate is 4(Misra *et al.*, 2017). This gate is helpful for the design of hamming code.

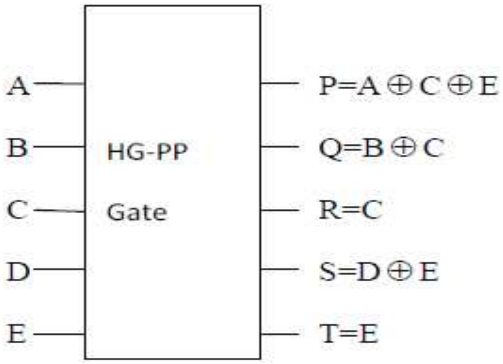

Figure 16: HG-PP Gate

COMPARATIVE STUDY

Various reversible gates and different circuits associated with these gates are discussed here. And also comparisons have been made among the existing circuit in terms of various parameters such as quantum cost, garbage output, constant input, gate count and delay. Comparison between existing reversible gates is shown in Table 1.

Table 1: Comparison between Reversible Logic Gates

Reversible Gates	Quantum cost	Types
SG Gate(Sayem& Ueda, 2010)	Unknown	4x4
BME Gate(Mahfuzzreza *et al*., 2013).	5	4x4
BSCL Gate (Rashmi *et al*., 2011)	Unknown	6x6
PAREEK Gate (Pareek *et al*., 2014)	7	4x4
RCQCA Gate (Misra *et al*., 2018).	6	4x4
URQG Gate (Bhoi *et al*., 2017).	Unknown	3x3
HCG Gate (James *et al*., 2007)	Unknown	4x4
HAS Gate (Misra *et al*., 2015).	5	3x3
FAS Gate (Misra *et al*., 2015).	8	4x4
OD Gate (Misra *et al*., 2015).	10	5x5
PPHCG Gate (James *et al*., 2007)	6	4x4
NG-PP Gate (Misra *et al*., 2017)	5	5x5
HG-PP Gate (Misra *et al*., 2017)	4	5x5

CONCLUSION

In this paper, a survey of various works is carried out in the field of reversible logic with respect to reversible circuits which form the basic building block of quantum computers. This paper presents the reversible gates which are not shown in (Ankush & Bhandari, 2016) and which are gathered from the literature till now. The paper can further be extended towards the digital design development using reversible logic circuits which are helpful in quantum computing, low power CMOS, nanotechnology, cryptography, optical computing, DNA computing, digital signal processing (DSP), quantum dot cellular automata, communication, computer graphics, etc.

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