Bajopas Vol. 2 Number 1 June, 2009

Bayero Journal of Pure and Applied Sciences, 2(1): 6 - 13
Received: November, 2008
Accepted: February, 2009

5KVA POWER INVERTER DESIGN AND SIMULATION BASED ON BOOST CONVERTER AND H-BRIDGE INVERTER TOPOLOGY

***Musa, A. and G.S.M. Galadanci**
Department of Physics, Bayero University, PMB 3011, Kano
*Correspondence author

ABSTRACT
Five (5) kVA power inverter was designed and simulated base on two topologies; Boost converter and Half-bridge inverter topology. A 555 timer IC was used as the control at fixed frequencies of 25 kHz and 50 Hz for the two stages. The results of the simulation were obtained. The graphs for both stages were plotted and the results show a significant increase in the voltage and duty cycle. The wave form of the output gives a square wave form.

Keywords: Power inverter, Simulation, Topology, Converter

INTRODUCTION

The World demand for electrical energy is constantly increasing and conventional energy resources are diminishing and even threatened to be depleted. With the increasing popularity of alternative power sources, such as solar and wind, the need for static inverters to convert dc energy stored in batteries to conventional ac form has increased substantially. This conversion can either be achieved by transistors or by SCRs (silicon controlled rectifiers). For lower and medium power outputs, transistorised inverters are suitable but for high power outputs, SCRs should be used. Transistor inverters are useful in wide variety of applications. They provide power to the complicated electronic systems of orbiting satellites and cool astronaut suits (http;//Guru/PEInverters/introduction/pdf/inv.pdf, 2006).

However, MOSFETs (Metal Oxide Semiconductor Field Effect Transistor) and IGBTs (Insulated Gate Bipolar Transistor) are good candidates for the switches in dc to ac conventional techniques. With the development electronic devices and circuits, newer equipment often have converters that allow the user to change the voltage and frequency applied to the equipment .Power electronics also provides the industries with effective methods to save energy and improve performance (Sen, 2002).

Power electronic devices can be divided in to two categories: Single component and hybrid component. The single component is composed of one solid-state device, and hybrid component is a combination of several single components manufactured as a single block. The single devices are loosely divided into three type :(1) the two layer devices such as diode , (2) the three layer devices such as transistor , and (3) the four layer devices such as the Thyristor . The hybrid components include wider range of devices such as the Insulated Gate Bipolar Transistor (IGBT), Static Insulated Transistor (SIT), and Darlington Transistor (DT). Solid state devices are main building components of any converter. Their function is mainly to mimic the mechanical switches by connecting and disconnecting electrical loads, but at very high speed. When the mechanical switch is open (off), the current through the switch is zero and the voltage across its terminal is equal to the source voltage. When the switch is closed (on), its terminal voltage is zero and its current is determined by load impedance (Mukund, 2006).

Design Stage for fly Boost Converter and Power Inverter

Boost converter design

Based on the dc-dc converter topology; Boost converter circuit design is shown with duty cycle (D), output input gain with pulse width modulation to drive the converter at 25 kHz shown in Figure 1.0

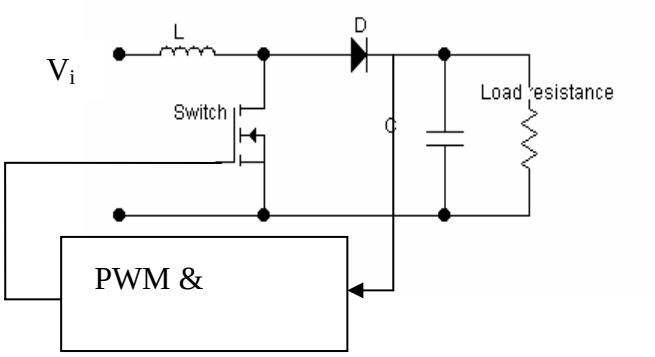


Figure 1.0: Boost converter schematic diagram

The output to the input voltage gain of the inverter is given by (Simon and Oliva, 2005).

$$M(V) = \frac{V_{out}}{V_{in}} = \frac{1}{1-D} \qquad 2.0$$

and $$\frac{I_{out}}{I_{in}} = \frac{1}{1-D} \qquad 2.1$$

where D, is the duty cycle of switching converter that is

$$D = \frac{t_{on}}{T} = \frac{t_{on}}{t_{on}+t_{off}} \qquad 2.2$$

where t_{off} =switched off time for the transistor

t_{on} = switched on time for the transistor and

T = switching period of the transistor which is define by the following relation

$$T = \frac{1}{f_s} = t_{on} + t_{off} = \frac{L\Delta I}{V_{in}} + \frac{L\Delta I}{V_{out}-V_{in}} \qquad 2.3\ a$$

or $$T = \frac{L\Delta V_{out}}{V_{in}(V_{out}-V_{in})} \qquad 2.3\ b$$

However, with 555-timer IC's an inexpensive regulated SMPS is constructed, feedback and pulse width modulation were shown in Figure 2.0. If the desired inverter frequency and the voltage are known, the power consumed by the switching on and off of the converter can be estimated by the following equation (http://supertex.com/pdf/app.note/AN-36.pdf, 2008).

$$P_{out} = f_{out}C_{out}V_{out}^2 \qquad 2.4$$

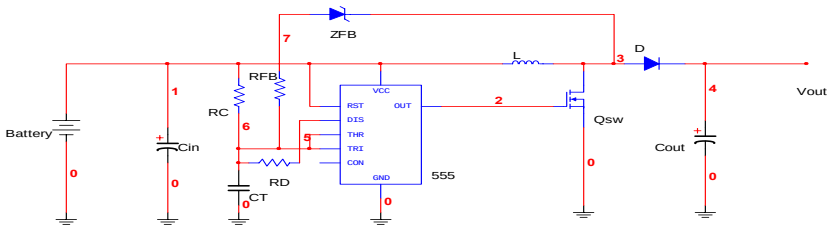


Figure 2.0 DC-DC Boost converter

Determine operating frequency, Duty cycle, and Inductor

Neglecting switch resistance, inductor losses, and other parasitic, the relationship between these parameters can be approximated by the following

$$P_{out} = \frac{(DV_{in})^2}{2f_sL} \qquad 2.5$$

Selection of a converter frequency is very important, since many applications require certain frequencies for EMI reasons. Higher switching frequencies allow the use of smaller inductors but lead to high switching losses. Conversely, lower frequencies can reduce switching losses but require large inductors. Converter in the range of 20 kHz-100 kHz are generally suitable. Duty cycle is calculated as follows.

$$D = \frac{\sqrt{2f_sLP_{out}}}{V_{in}} \qquad 2.6$$

The equation above yield duty cycles greater than 100%. For the inductor rating, peak inductor current can be approximated using the following equation

$$I_{L(pk)} = \sqrt{\frac{2P_{out}}{f_sL}} \qquad 2.7$$

Select Q_{sw} and D

For switching transistor Q_{sw}, the most important parameters are break down voltage, on resistance, peak current, and power dissipation. For the diode, the important parameters are reverse break down voltage, peak repetitive current, and average forward current and reverse recovery time. Since peak inductor current also flows through the switch and the diode, it may be used to rate these components as well.

$$I_{sw(pk)} = I_{D(pk)} = I_{L(pk)} \qquad 2.8$$

Maximum average current will occur at minimum input voltage

$$I_{sw} = \frac{P_{out}}{V_{in}} \qquad 2.9$$

Average power dissipation in the switch can be estimated from the following equation.

$$P_{sw} = \frac{R_{sw}(2P_{out})^{2.5}}{V_{in}\sqrt{f_c L}} \qquad 3.0$$

Where R_{sw} = switch on resistance

Select C_{in} and C_{out}

Input capacitance C_{in} functions as an input bypass capacitor to reduce the effective source impedance and also EMI by restricting high frequency current paths to short loops.. For the best performance C_{in} impedance should be less than 1Ω.

$$C_{in} \geq \frac{1}{2\pi f_c Z_{in}} \qquad 3.1$$

Where $Z_{in} = C_{in}$ impedance

Output capacitance C_{out} stores high voltage energy and also reduces EMI by restricting high frequency current paths to stop short loops. The value of C_{out} must largely dependent on the desired ripple voltage on V_{out}. Generally, ripple (as a fraction of output voltage) of about 10% is adequate.

$$C_{out} \geq \frac{I_{out}}{ripple \cdot f_{inv} V_{out}} \qquad 3.2$$

Where I_{out} = output current to the inverter,

Ripple = $\frac{V_{ripple(p-p)}}{V_{out}}$ and $f_{inv} = $ inverter frequency, both C_{in} and C_{out} should be high frequency types

Select Timing Components R_C, R_D and C_T

Timing components R_c, R_D and C_T determine nominal converter frequency and maximum duty cycle. Selection of these components is an iterative process. The ratio R_C/R_D sets the maximum possible duty cycle, while R_c , R_D and C_T together determine nominal output frequency. Maximum duty cycle can also be calculated using the following equation.

$$D_{(max)} = \frac{1}{1+\frac{0.693}{N_{CD}+2}\ln\left[\frac{2-2N_{CD}}{2-N_{CD}}\right]} \qquad 3.3$$

$$where\ N_{CD} = R_c/R_D$$

The R_c/R_D ratio must be greater than $2/1$ for proper operation of the 555 timer. If less, timing capacitor voltage will be unable to discharge to $1/3\ V_{CC}$ and output of the 555 will remain low. Nominal converter frequency can be calculated using the following equation.

$$f_{c(nom)} = \frac{1}{R_C C_T\left(0.693+\frac{2}{N_{CD}+2}\ln\left[\frac{2-2N_{CD}}{2-N_{CD}}\right]\right)} \qquad 3.4$$

Select Feedback components R_{FB} & Z_{FB}

Output voltage is determine by the zener voltage plus an amount of bias voltage needed to vary duty cycle of the timing

$$V_{out} = V_Z + V_{bias} \qquad 3.5$$

The amount bias will vary depending on load and input voltage. The extreme limits of bias voltage are given in equations 3.6 and 3.7.

$$V_{bias(min)} = \frac{1}{3}V_{in} \qquad 3.6$$

$$V_{bias(max)} = V_{in}\left[\frac{1}{3} - \frac{1}{1+N_{CD}+\frac{2}{N_{FBC}}}\right][1+N_{FZ}(1+N_{CD})] \qquad 3.7$$

$$where:\ N_{FBC} = R_{FB}/R_C \text{ and } N_{CD} = R_c/R_D$$

If R_{FB} is too low, it will prevent timing capacitor voltage from rising to $2/3V_{CC}$ as required for nominal operation of the 555, resulting in switch Q_{SW} staying on and the current rising to destructive levels. To prevent this from occurring, the ratio of R_{FB}/R_C must always be greater than two.

$$\frac{R_{FB}}{R_C} > 2 \qquad 3.8$$

Power Inverter stage design

However, in this part H-bridge inverter topology was adopted. The half bridge inverter in the simplest form is shown is Figure 3.0 H-bridge inverter topology has lower number of switches and simple control.(http://Guru/PEInverter/Half-bridge/pdf/inv.pdf, 2006). The duration of the dead band should be large enough to allow the switch that is turned off to close before the other switch, to start conducting. The advantage of H-bridge inverter topology has lower number of switches and simple control (Emadi and Stoyan, 1992). The differential equation for the current from $t=0$ to $t=T/2$ governing the current and voltage flows of half-bridge inverter may be written as

$$L\frac{di(t)}{dt}+Ri(t)=V_s \qquad 3.9$$

Its general solution is of the form

$$i(t)=\frac{V_s}{R}+Ae^{-t/\tau} \qquad 4.0$$

Where τ , the time constant for R-L load, is $\tau=\frac{L}{R}$, Applying the initial condition, that is

$i(0)=I_{\min}=-I_{\max}$ when $t=0$, we get $A=-\frac{Vs}{R}-I_{\max}$.

Hence, the expression for the current in the circuit during $t=0$ and $t=T/2$ is

$$i(t)=\frac{Vs}{R}\left(1-e^{-t/\tau}\right)-I_{\max}e^{-t/\tau} \qquad 4.1$$

The current attains its maximum value at $t=T/2$ and is obtained from (4.1) as

$$I_{\max}=\frac{V_s}{R}\left(1-e^{-T/2\tau}\right)-I_{\max}e^{-T/2\tau}$$

Rearranging the term we get

$$I_{\max}=\frac{Vs}{R}\left(\frac{1-e^{-T/2\tau}}{1+e^{-T/2\tau}}\right) \qquad 4.2$$

Hence the current in the circuit during $t=0$ and $t=T/2$ is

$$i(t)=\frac{V_s}{R}\left(1-e^{-t/\tau}\right)-\frac{V_s}{R}\left(\frac{1-e^{-T/2\tau}}{1+e^{-T/2\tau}}\right)e^{-t/\tau} \qquad 4.3$$

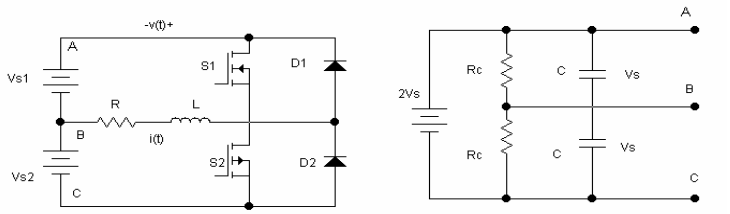


Figure 3.0 (i) Half-bridge inverter with dual supply, and (ii) single supply

MATERIALS AND METHODS

Two methods were employed for the inverter designed and simulation; the computer simulation with NI Multisim 10. Software and the circuit analysis using the above equations. The design topology which was adopted is shown in Fig.4 with two stages; boost converter and half-bridge inverter, and their controls.

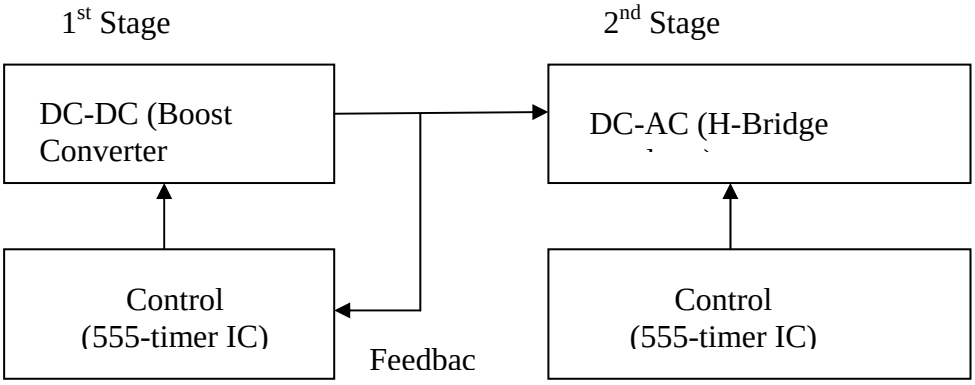


Figure 4.0 DC-AC Inverter circuit design

RESULTS:

Based on the simulation and the equations above the results were plotted using origin 50 with the following graphs:

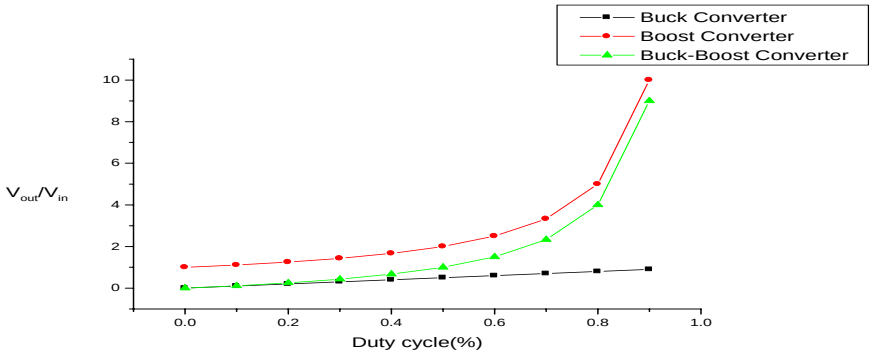


Figure 5.0 Graph of commonly converters compared analytically with equation 2.0 which shows the boost converter has high gain.

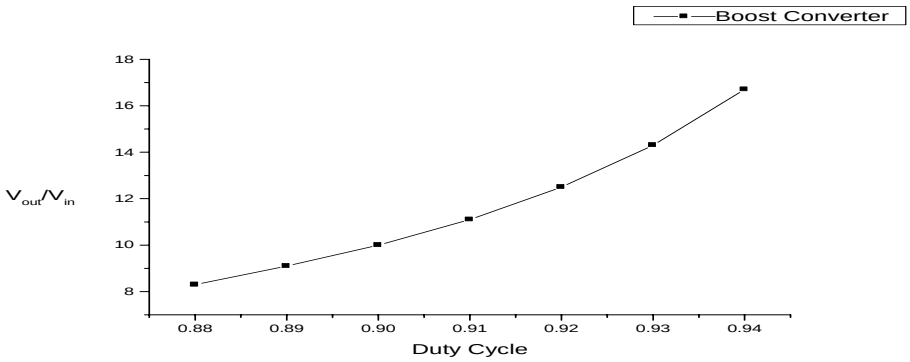


Figure 6.0 Graph of the gain to the duty cycle from the simulation result

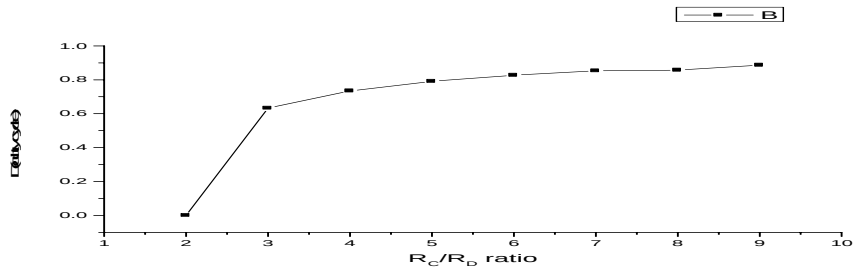


Figure 7.0 Graph of maximum duty cycle with ratio of timing resistors R_C/R_D

However, the nominal converter frequency was chosen to be 25 kHz which gave an inductor of 500µH and inductor peak current $I_{L(pk)}$ using equations (2.6) and (2.7) with design power level of 700mW. Maximum duty is 70% at 6.0volt correspond to R_C/R_D ratio of 3.4 with equation 10; the R_C value was 40.5kΩ which indicated R_D is 11.9kΩ. For maximum regulation, R_{FB} should be greater than 81.0kΩ since R_C was 40.5kΩ then R_{FB} is slightly greater than 81.0kΩ which approximately 90.0kΩ

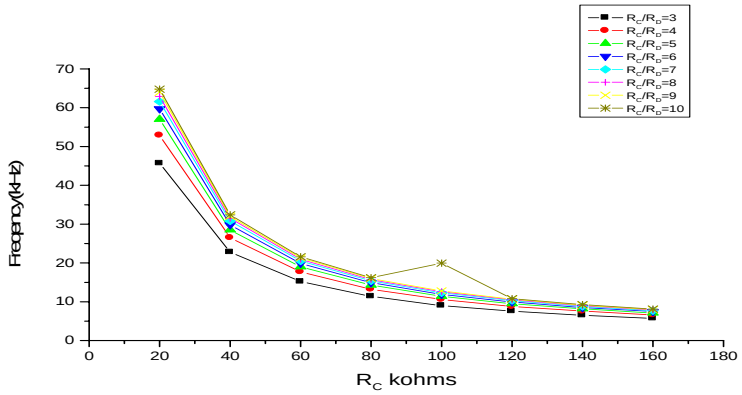


Figure 8.0 Graph of nominal Converter frequency for C_T = 1nF

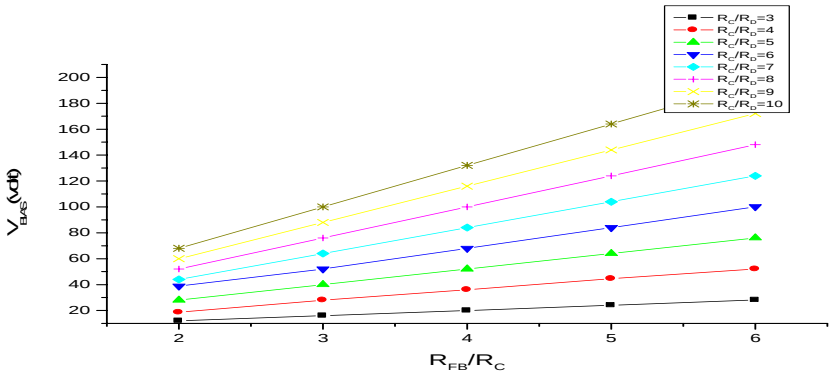


Figure 9.0 Graph of Bias voltages plot from equation (3.7)

However, for maximum regulation R_{FB} are slightly greater than two as equation (3.8). Since R_C is 41.0kΩ than R_{FB} must be greater than 82 kΩ but 90.0 kΩ was selected.

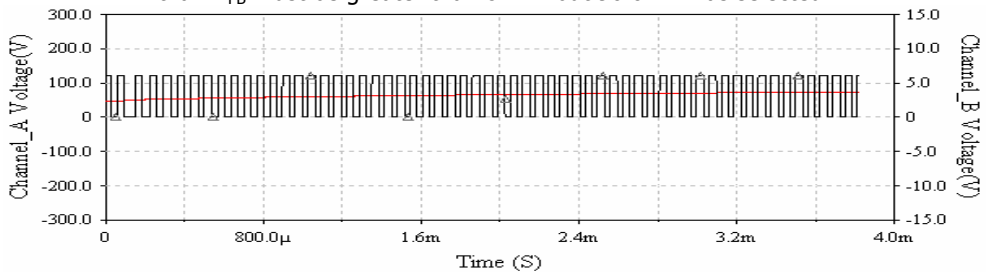


Figure 10.0 Converter output voltage from the simulation

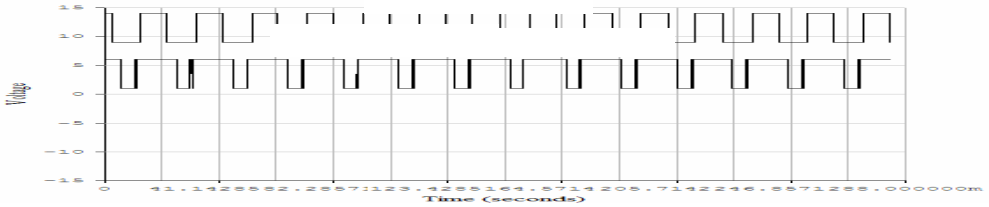


Figure 11.0 Output wave form for the two AND-gate

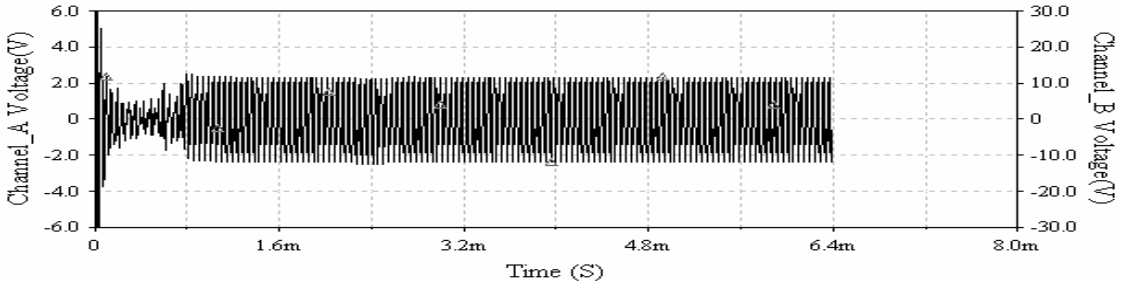


Figure 12.0 Inverter output voltage from the simulation

Table 1.0 Requirement for Comparison

S/no.	Parameter	Required	Achieved
1	V_{out}(converter)	48.0 V	100V
2	V_{out}(inverter)	220V	220V
3	P_{out}(converter)	700mW	0.15W
4	P_{out}(inverter)	5kVA	2.09kVA
5	Converter wave form	Modulated	Modulated
6	Inverter wave form	Modified Sine wave	Square wave with distortion
7	I_{out}(inverter)	22.7 A	9.53A
8	I_{Lpk}	330mA	185.32mA
9	Inverter Freq.	50Hz	48.6Hz
10	Converter Freq.	25kHz	24.6kHz

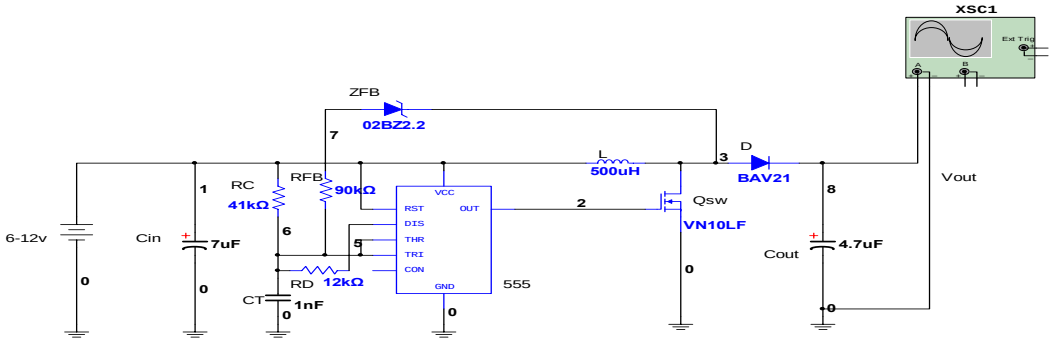
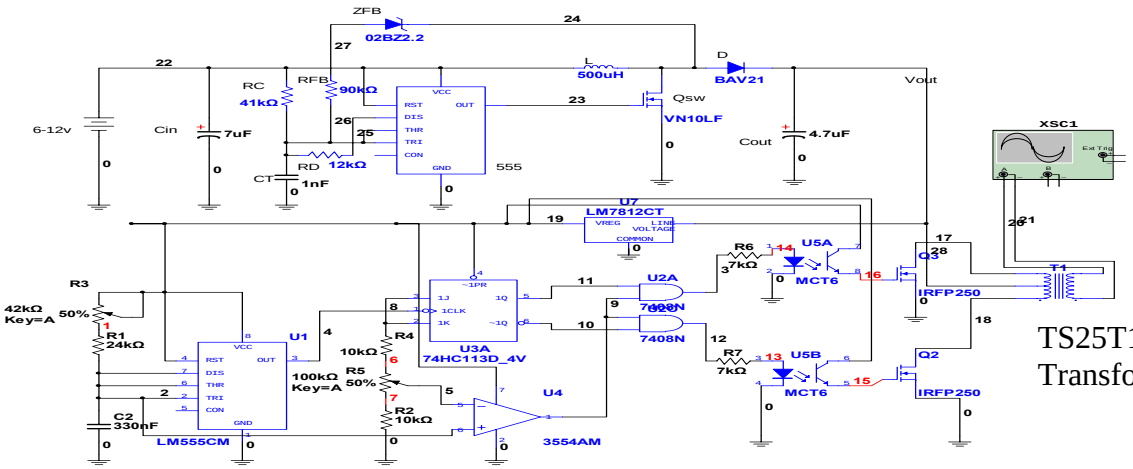


Figure. 13 DC-DC converter stages with the nominal calculated values



TS25T1 power Transformer

Figure 14. DC-DC/DC-AC power Inverter stage

SUMMARY, DISCUSSION AND CONCLUSION

The selection of the above topology simulated and worked with the nominal calculated values. It also shows that from table 1.0 the frequencies for both converter and inverter were close to the required values together with the wave forms.

In conclusion, the circuits when simulated performed much better than the expected result due to calculation assumptions and approximations. It shows that the duty cycle of the converter change completely as seen from the Fig. 6 when compared with general topologies in Fig.5. It is also shown from Fig. 11 output voltage high than expected.

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