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Tunable Lossy and Lossless Grounded Inductors Using Minimum Active and Passive Components

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Abstract

In this contribution, nine new Grounded Inductance Simulators (GISs) using a single Multiple-Output Current Controlled Current Conveyor Transconductance Amplifier (MO-CCCCTA) and one grounded capacitor are proposed. Among them, two are lossless types and seven are lossy types. The use of a single grounded capacitor makes the circuits suitable for fabrication. All the proposed circuits are electronically tunable through the bias currents of MO-CCCCTA. Furthermore, no component matching conditions are needed for realizing them. The designed circuits are verified through PSPICE simulator with ± 0.9 V power supply. The simulation results show that for all the proposed circuits: maximum operating frequencies are about 12 MHz, power dissipation is less than 0.784 mW, Total Harmonic Distortions (THDs) are under 8.09%, and maximum output voltage noise at 1 MHz frequency is 14.094 nV/√Hz. To exhibit the workability of the proposed circuits, they are used to design band-pass, low-pass filter, parallel RLC resonator, and parasitic inductance cancelator.

Keywords: active inductor, multiple-output current controlled current conveyor transconductance amplifier (MO-CCCCTA), electronic controllability, filters, resonant circuit

1. Introduction

Recently, the implementation of inductors using different active building blocks has received much attention as the implementation of passive spiral inductors in an integrated circuit is difficult. The passive inductors consume a large chip area and also suffer from resistive losses and process variabilities. Inductor simulators are used in electronics, instrumentation, measurement, and communication systems. It finds applications in analog active filters and LC oscillators for impedance matching, phase shifters, and parasitic cancellation [1-3].

In the past, several Grounded Inductor Simulators (GISs) were reported using active building blocks, such as Dual X Current Conveyor Differential Input Transconductance Amplifier (DXCCDITA) [1], Modified Differential Voltage Current Conveyor (MDVCC) [2], Voltage Differencing Current Conveyor (VDCC) [3], Dual X Second-Generation Current Conveyor (DXCCII) [4-6], Plus-Type Second Generation Current Conveyor (CCII+) and Inverting Voltage Buffer (IVB) [7], Dual X Current Conveyor Transconductance Amplifier (DXCCTA) [8], Current Differencing Transconductance Amplifier (CDTA) [9], Current Controlled Current Conveyor Transconductance Amplifier (CCCCTA) [10], Current Differencing Buffered Amplifier (CDBA) [11-12], Four Terminal Floating Nullor Transconductance Amplifier (FTFNTA) [13], Voltage Differencing Gain Amplifier (VDGA) [14], Current-Controlled-Current-Feedback Amplifier (CC-CFA) [15], Current Follower Current Controlled Conveyor (CFCCC) [16], Voltage Differencing Transconductance Amplifier (VDTA) [17-19], Z-Copy Current-Controlled Current Inverting Transconductance Amplifier (ZC-CCCITA) [20], Extra X Current Conveyor

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Transconductance Amplifier (EXCCTA) [21], Operational Transresistance Amplifier (OTRA) [22-26], Voltage Differencing Inverting Buffered Amplifier (VDIBA) [27-28], Voltage Differencing Buffered Amplifier (VDBA) [29], etc. Among the inductance simulators, most of the configuration comes with two or more passive components for implementation [1-8, 11-13, 21-26, 29]. Two or more active building blocks are required in [9, 15, 25-26, 28]. The inductors proposed in [4-6, 12, 22-23, 25] require matching conditions between passive components. The work described in [2-29] realize only lossless/lossy/negative inductance simulators. Floating components are required in [1-2, 4-7, 11-12, 22-29]. Additionally, the circuits of [2, 4-7, 11-12, 22-26] cannot be tuned electronically. The vigorous study of this literature gives a scope for realizing inductors for both lossy and lossless inductors that use single active block and single capacitor without component matching conditions, and can offer the electronically tunable facility.

In this research, nine new GISs are proposed. All the proposed inductors are composed of a single active block and single grounded capacitor in each design. Furthermore, the inductors do not require component matching conditions, and the inductors can be tuned electronically. To test the workability of the lossless inductor simulator circuits, the positive inductor is used to design a Band-Pass (BP) filter, the negative inductor is used to cancel parasitic inductance, lossy series RL circuit is used to design a Low-Pass (LP) filter, and lossy parallel RL circuit is used to design parallel resonant circuit.

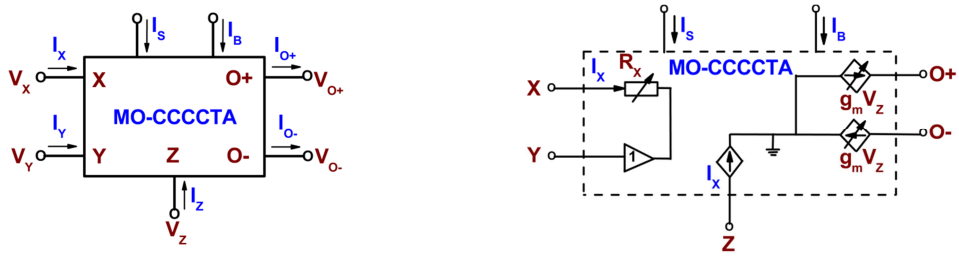
This study has been divided as follows: The introduction is presented in section 1, and Multiple-Output Current Controlled Current Conveyor Transconductance Amplifier (MO-CCCCTA) is introduced in section 2. Section 3 describes the configurations of the proposed GISs. The non-ideal analysis of the proposed configurations is performed in section 4. Section 5 brings simulation results. After that, the applications of the reported inductors are presented in section 6 followed by section 7 where the comparisons of the proposed inductors with the previous publication are discussed. Finally, the study is concluded in section 8.

2. MO-CCCCTA

MO-CCCCTA is a versatile active building block which is effective to simplify the circuit configuration. The most attractive feature of this block is that it requires no resistor in practical applications as it has parasitic resistance. The port relations of MO-CCCCTA block can be characterized as:

$$\begin{bmatrix} V_X \\ I_Y \\ I_Z \\ I_{O\pm} \end{bmatrix} = \begin{bmatrix} R_X & 0 & 1 \\ 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm g_m & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_Z \\ V_Y \end{bmatrix} \tag{1}$$

where R_X is the parasitic resistance at X-port and g_m is the transconductance gain of MO-CCCCTA. The parasitic resistance R_X and transconductance gain g_m are electronically tunable through the input bias currents I_B and I_S, respectively. The circuit symbol and the equivalent circuit of the MO-CCCCTA block are shown in Fig. 1 [30]. The Complementary Metal-Oxide-Semiconductor (CMOS) implementation of MO-CCCCTA is shown in Fig. 2. It consists of two principal blocks: a Current Controlled Second Generation Current Conveyor (CCCII) circuit and an Operational Transconductance Amplifier (OTA) circuit. The circuit implementation consists of mixed translinear loop (M1-M4). The mixed loop is DC biased by using current mirrors (M5-M6 and M9-M11). The output Z-terminal that generates the current from *X* terminal is realized using transistors (M7-M8 and M12-M13). The simple-version transconductance amplifier is realized using transistors (M14-M15, M18-M21, and M23-M24). The inverted output terminals (O-) are realized by using transistors (M16-M17, M22, and M25-M27).



(a) Symbol (b) Equivalent circuit

Fig. 1 MO-CCCCTA [30]

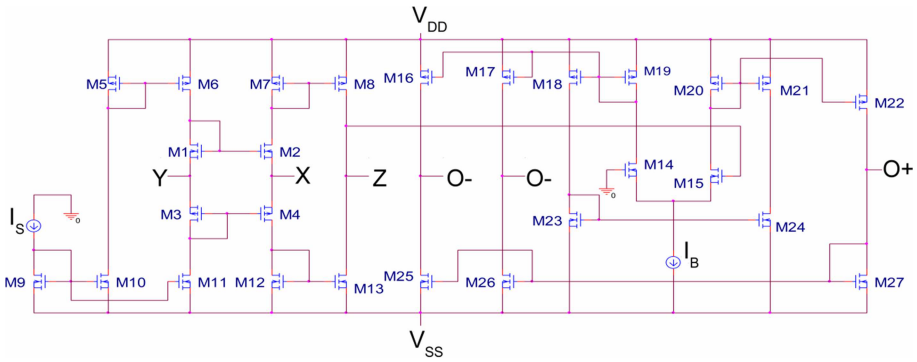


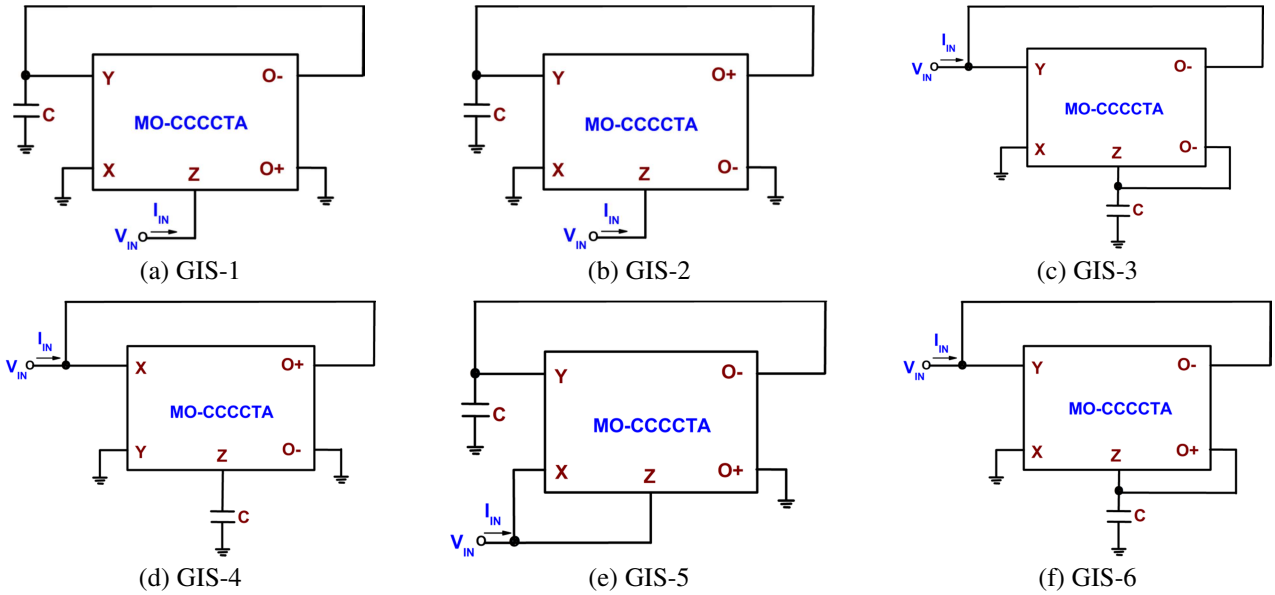
Fig. 2 CMOS implementation of MO-CCCCTA [30]

3. The Proposed GISs

The proposed GISs using a single active block and single capacitor are shown in Fig. 3. The use of a single grounded capacitor for all the configurations makes the circuits suitable for fabrication. Furthermore, it is also beneficial in stopping noise and parasitic effects [1]. Among the nine topologies, the first two circuits provide lossless (positive and negative inductors) and the rest seven circuits can realize lossy inductors. The input impedances along with equivalent inductances and equivalent resistances obtained by routine analysis of these configurations are summarized in Table 1. The sensitivities of the inductors can be expressed as:

$$S_{C,R_X}^{L_{eq}} = -S_{g_m}^{L_{eq}} = 1 \tag{2}$$

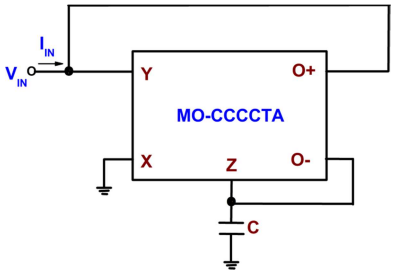
From Eq. (2), it is seen that the sensitivities of the inductors are low and not more than unity.



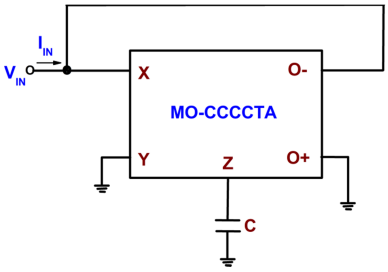
(a) GIS-1 (b) GIS-2 (c) GIS-3

(d) GIS-4 (e) GIS-5 (f) GIS-6

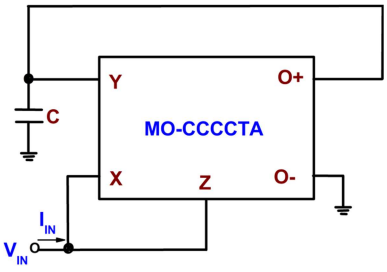
Fig. 3 The proposed lossless and lossy GIS circuits



(g) GIS-7



(h) GIS-8



(i) GIS-9

Fig. 3 The proposed lossless and lossy GIS circuits (continued)

Table 1 The actively realizable inductance constructions

Circuit	Simulator	Type	Impedance realized	L_{eq}	R_{eq}
Fig. 3(a)	GIS-1	Pure L	$\frac{sCR_X}{g_m}$	$\frac{CR_X}{g_m}$	-
Fig. 3(b)	GIS-2	Pure L	$-\frac{sCR_X}{g_m}$	$-\frac{CR_X}{g_m}$	-
Fig. 3(c)	GIS-3	+ L series with + R	$\frac{sCR_X}{g_m}+R_X$	$\frac{CR_X}{g_m}$	R_X
Fig. 3(d)	GIS-4	+ L parallel with + R	$\frac{1}{\frac{g_m}{sCR_X}+\frac{1}{R_X}}$	$\frac{CR_X}{g_m}$	R_X
Fig. 3(e)	GIS-5	+ L parallel with + R	$\frac{1}{\frac{2g_m}{sCR_X}+\frac{2}{R_X}}$	$\frac{CR_X}{2g_m}$	$\frac{R_X}{2}$
Fig. 3(f)	GIS-6	+ L series with – R	$\frac{sCR_X}{g_m}-R_X$	$\frac{CR_X}{g_m}$	$-R_X$
Fig. 3(g)	GIS-7	– L series with – R	$-\frac{sCR_X}{g_m}-R_X$	$-\frac{CR_X}{g_m}$	$-R_X$
Fig. 3(h)	GIS-8	– L parallel with + R	$\frac{1}{-\frac{g_m}{sCR_X}+\frac{1}{R_X}}$	$-\frac{CR_X}{g_m}$	R_X
Fig. 3(i)	GIS-9	– L parallel with + R	$\frac{1}{-\frac{2g_m}{sCR_X}+\frac{2}{R_X}}$	$-\frac{CR_X}{2g_m}$	$\frac{R_X}{2}$

4. Non-Ideal Analysis

For MO-CCCCTA, the non-ideal characteristic equations are expressed as:

$$V_X = \beta V_Y + I_X R_X \tag{3}$$

$$I_Z = \alpha I_X \tag{4}$$

$$I_{O+} = \gamma_P g_m V_Z \tag{5}$$

$$I_{O1-} = -\gamma_N g_m V_Z \tag{6}$$

$$I_{O2-} = -\gamma_{NC} g_m V_Z \tag{7}$$

where β, α, γ_P, γ_N, and γ_{NC} are the transfer ratios and ideally equal to unity.

In addition, like any other active device, a practical MO-CCCCTA shows various terminals parasitic. The parasitic model of MO-CCCCTA is shown in Fig. 4. It shows that a small series resistance R_X appears at X terminal, whereas the parasites in the form of shunt output impedances (R_Y//C_Y), (R_Z//C_Z), (R_{O+}// C_{O+}), and (R_{Oi-}//C_{Oi-}) appear at Y, Z, O+, and O_i– ports (i =1, 2),

respectively. After considering these parasitic impedances and considering the non-ideal gains, on the proposed circuits, the input impedance of the inductors has been reanalyzed and expressed in Table 2. Though it is noted from Table 2 that the impedances are influenced owing to the inclusion of MO-CCCCTA parasitic and non-ideal transfer current gains, it is not excessive as R_Y, R_Z, R_{O+}, and R_{O-} are very high, C_Y, C_Z, C_{O+}, C_{O1-}, and C_{O2-} are very low, and α, β, γ_P, γ_N, and γ_{NC} are very close to unity.

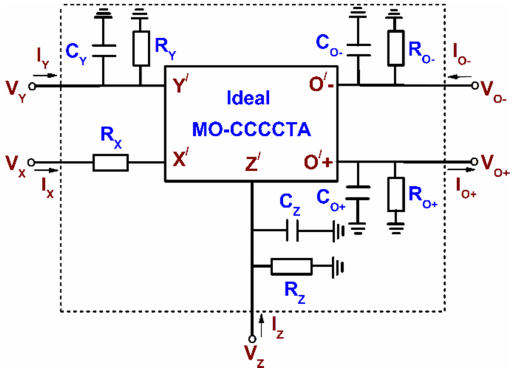


Fig. 4 Non-ideal model of MO-CCCCTA

Table 2 Impedance of the proposed inductors including non-ideal gains and parasitic impedances

Simulator	Impedance realized	Assumed values
GIS-1	$\frac{sC_E+\frac{1}{R_E}}{\frac{\alpha\beta\gamma_N g_m}{R_X}+\left(sC_E+\frac{1}{R_E}\right)\left(sC_Z+\frac{1}{R_Z}\right)}$	$C_E = C+C_Y+C_{O-}$; $R_E = R_Y\|\|R_{O-}$
GIS-2	$\frac{sC_E+\frac{1}{R_E}}{-\frac{\alpha\beta\gamma_P g_m}{R_X}+\left(sC_E+\frac{1}{R_E}\right)\left(sC_Z+\frac{1}{R_Z}\right)}$	$C_E = C+C_Y+C_{O+}$; $R_E = R_Y\|\|R_{O+}$
GIS-3	$\frac{sC_{E2}+\gamma_{NC}g_m+\frac{1}{R_{E2}}}{\frac{\alpha\beta\gamma_N g_m}{R_X}+\left(sC_{E1}+\frac{1}{R_{E1}}\right)\left(sC_{E2}+g_m+\frac{1}{R_{E2}}\right)}$	$C_{E1} = C_Y+C_{O1-}$; $R_{E1} = R_Y\|\|R_{O1-}$ $C_{E2} = C+C_Z+C_{O2-}$; $R_{E2} = R_Z\|\|R_{O2-}$
GIS-4	$\frac{1}{\frac{\alpha\gamma_P g_m}{\left(sC_E+\frac{1}{R_Z}\right)R_X}+\frac{1}{R_X}+\left(sC_{O+}+\frac{1}{R_{O+}}\right)}$	$C_E = C+C_Z$
GIS-5	$\frac{1}{\frac{(1+\alpha)\beta\gamma_N g_m}{\left(sC_E+\frac{1}{R_E}\right)R_X}+\frac{(1+\alpha)}{R_X}+\left(sC_Z+\frac{1}{R_Z}\right)}$	$C_E = C+C_Y+C_{O-}$; $R_E = R_Y\|\|R_{O-}$
GIS-6	$\frac{sC_{E2}-\gamma_P g_m+\frac{1}{R_{E2}}}{\frac{\alpha\beta\gamma_N g_m}{R_X}-\left(sC_{E1}+\frac{1}{R_{E1}}\right)\left(sC_{E2}+\gamma_P g_m+\frac{1}{R_{E2}}\right)}$	$C_{E1} = C_Y+C_{O-}$; $R_{E1} = R_Y\|\|R_{O-}$ $C_{E2} = C+C_Z+C_{O+}$; $R_{E2} = R_Z\|\|R_{O+}$
GIS-7	$\frac{sC_{E2}+\gamma_N g_m+\frac{1}{R_{E2}}}{-\frac{\alpha\beta\gamma_P g_m}{R_X}+\left(sC_{E1}+\frac{1}{R_{E1}}\right)\left(sC_{E2}+\gamma_N g_m+\frac{1}{R_{E2}}\right)}$	$C_{E1} = C_Y+C_{O+}$; $R_{E1} = R_Y\|\|R_{O+}$ $C_{E2} = C+C_Z+C_{O-}$; $R_{E2} = R_Z\|\|R_{O-}$
GIS-8	$\frac{1}{-\frac{\alpha\gamma_N g_m}{\left(sC_E+\frac{1}{R_Z}\right)R_X}+\frac{1}{R_X}+\left(sC_{O-}+\frac{1}{R_{O-}}\right)}$	$C_E = C+C_Z$
GIS-9	$\frac{1}{-\frac{(1+\alpha)\beta\gamma_P g_m}{\left(sC_E+\frac{1}{R_E}\right)R_X}+\frac{(1+\alpha)}{R_X}+\left(sC_Z+\frac{1}{R_Z}\right)}$	$C_E = C+C_Y+C_{O+}$; $R_E = R_Y\|\|R_{O+}$

5. Simulation Results

Simulations have been carried out using the CMOS implementation of MO-CCCCTA as depicted in Fig. 2 through PSPICE simulator with TSMC 0.18 µm process parameters. The aspect ratios of the transistors are given in Table 3. The supply voltages are chosen as $V_{DD} = -V_{SS} = 0.9$ V. The proposed GISs 1-4 are simulated with capacitor value 50 pF. The bias current values are $I_S = 7.113$ µA ($R_x = 5$ kΩ) and $I_B = 24.135$ µA ($g_m = 100$ µS) for all the simulations.

Table 3 The dimensions of the Metal-Oxide-Silicon (MOS) transistors utilized in the MO-CCCCTA architecture [30]

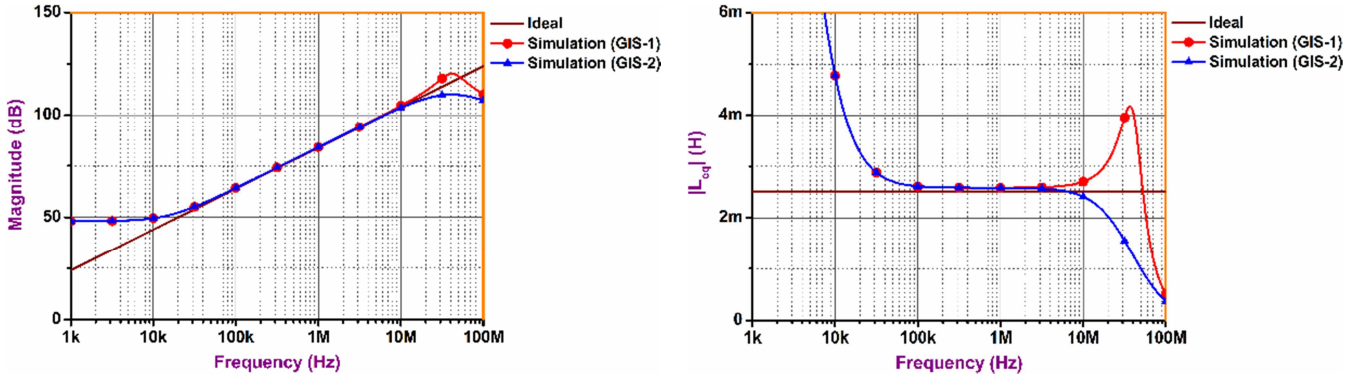
Transistor	W/L (µm/µm)
M1, M2	5/0.18
M3, M4	8/0.18
M5-M8	5/0.18
M9-M13	3/0.18
M14, M15	10/0.5
M16-M22	25/0.8
M23-M27	8/0.8

The ideal and simulated magnitude and corresponding inductance value versus frequency curves of the lossless inductor (GIS-1 and GIS-2) are given in Figs. 5(a)-(b), respectively. It is observed that the simulated and the ideal responses are nearly equal to each other in the frequency range of 20 kHz to 12 MHz. The ideal and simulated phase responses are shown in Fig. 6. The simulated phase values for GIS-1 are 86.85° at 20 kHz and 98.08° at 12 MHz, so the calculated errors are 3.5% and 8.97%, respectively. The same for GIS-2 are 95.52° and 98.95° respectively with corresponding errors of 6.13% and 9.94%. To measure the phase difference between current and voltage for GIS-1 and GIS-2, transient analyses have been done as shown in Fig. 7. The obtained phase differences are 92 degree and 93 degree for GIS-1 and GIS-2, so the calculated error is 2.22% and 3.33%, respectively.

The tunability of the recommended GIS-1 and GIS-2 has been confirmed by varying the bias currents. The resulting magnitude curve for GIS-1 is displayed in Fig. 8, whereas the resulting magnitude curves for GIS-2 are shown in Fig. 9. The corresponding inductor value of GIS-1 and GIS-2 are shown in Figs. 10 and 11, respectively. It is found that between 20 kHz and 12 MHz, changes of impedances are linear, thus simulated inductances are assumed to be constant for this interval. The inductance values at 1 MHz frequency for the GIS-1 and GIS-2 obtained from the theoretical expectation and simulation are given in Table 4. Variation of phase for different bias currents has also been simulated. Fig. 12 shows the phase variation of GIS-1 with different bias currents. Phase variation of GIS-2 is shown in Fig. 13. It is proved that the values of the inductors can be tuned by input bias currents I_B and I_S.

The simulated Total Harmonic Distortion (THD) of GIS-1 and GIS-2 for different input currents are shown in Fig. 14. The results show that the maximum THDs up to 70 µA are 8.09% and 2.69% for the GIS-1 and GIS-2, respectively. Finally, Monte Carlo analysis for 10% deviation in capacitor value is done for 100 runs to study the effect of process variability on the response of the simulator as presented in Fig. 15. It illustrates that the magnitude of inductances vary from 2.4379 mH to 2.68695 mH with a mean value of 2.5658 mH for the GIS-1 and for the GIS-2, it is from 2.41266 mH to 2.65626 mH with the mean value of 2.53878 mH. The noise behavior of the inductance simulator of GIS-1 and GIS-2 with respect to frequency has been shown in Fig. 16. The output voltage noise and equivalent input current noise of GIS-1 at the frequency of 1 MHz are calculated as 12.501 nV/√Hz and 2.306 pA/√Hz, respectively. For GIS-2, the same are 12.467 nV/√Hz and 2.266 pA/√Hz, respectively.

Next, the GIS-3 and GIS-4 are simulated. The theoretical and the simulated magnitude and phase responses for the input impedance of GIS-3 are given in Fig. 17. The electronic tunability of GIS-3 is shown in Fig. 18, whereas the variation of phase with frequency is shown in Fig. 19. The noise behavior of the GIS-3 with respect to frequency is displayed in Fig. 20. The calculated output voltage noise at 1 MHz frequency is 12.059 nV/√Hz and the input referred noise is 2.369 pA/√Hz.



(a) Impedances magnitude (b) Inductance values

Fig. 5 Frequency responses for the proposed lossless inductors

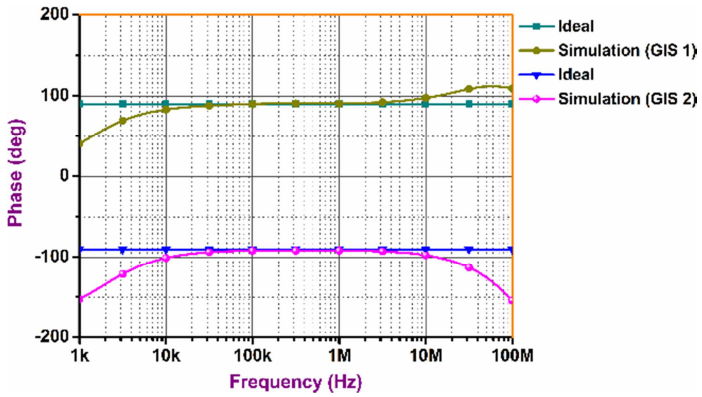
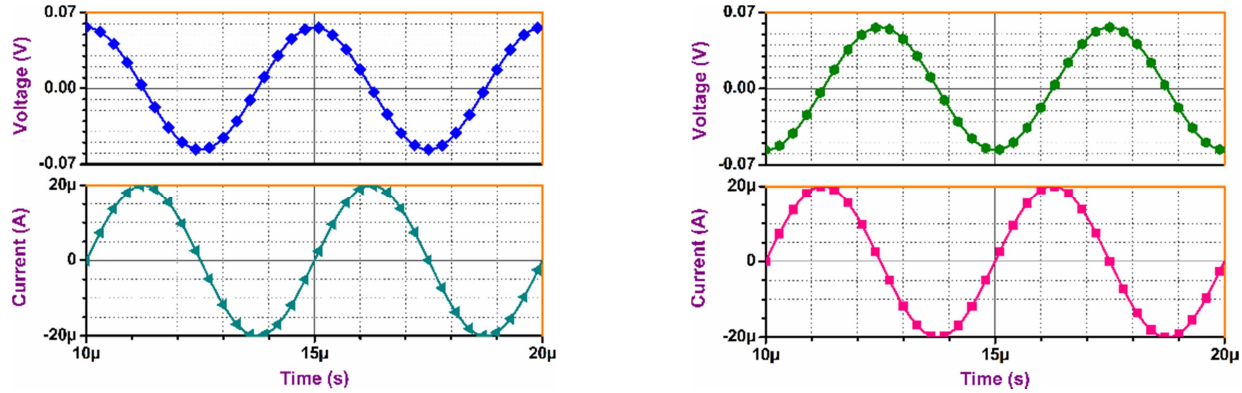
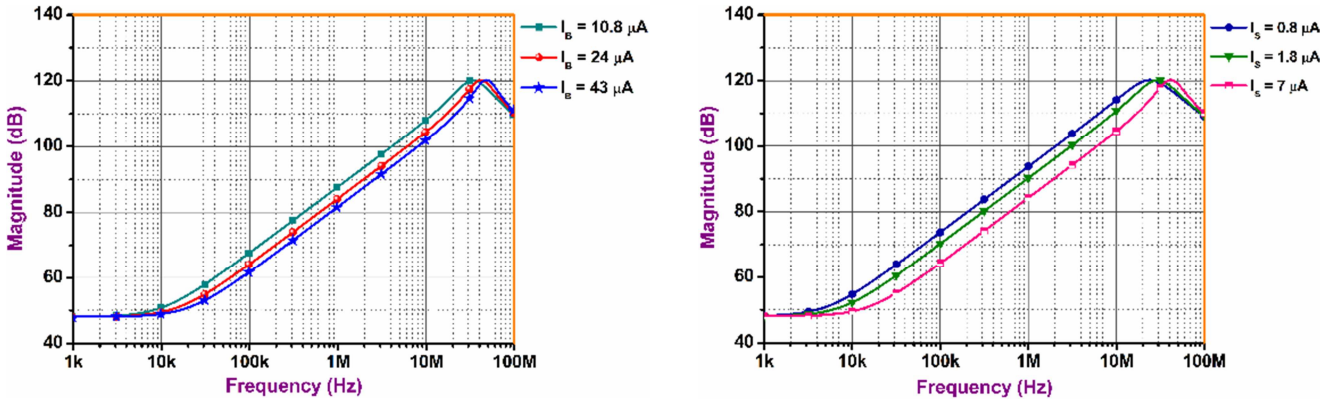


Fig. 6 Frequency responses of the phase for the proposed lossless inductors



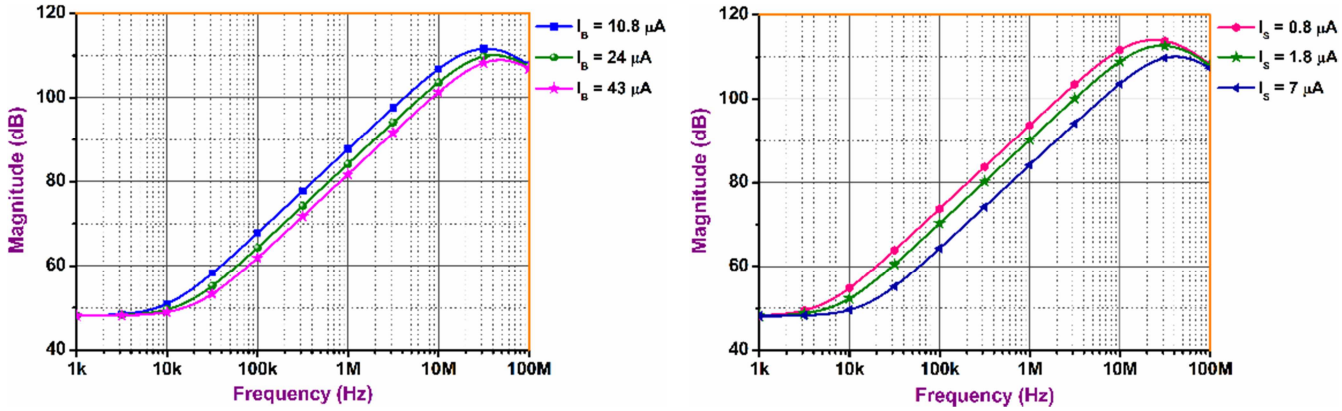
(a) For GIS-1 (b) For GIS-2

Fig. 7 The transient analysis output



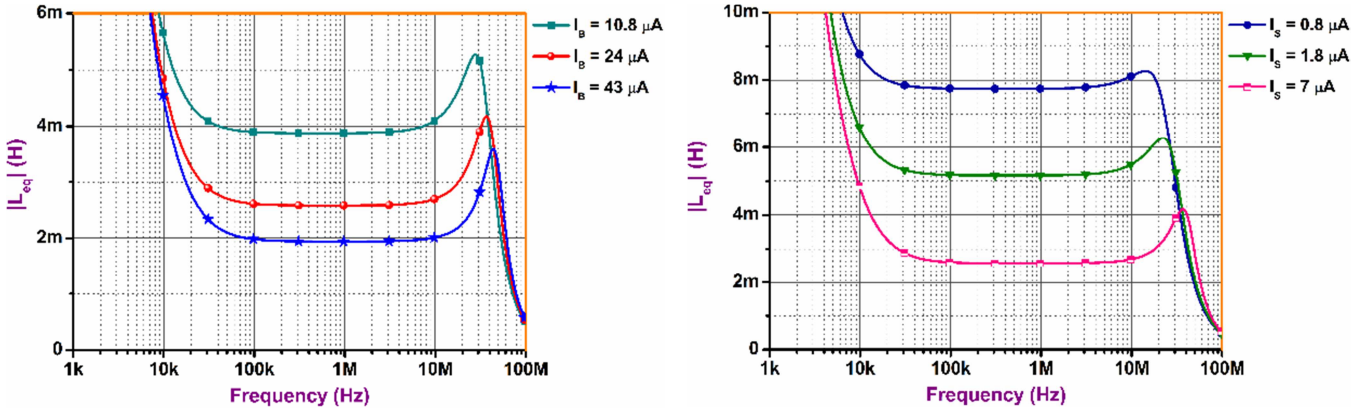
(a) With I_B (b) With I_S

Fig. 8 Variation of impedance magnitude for GIS-1



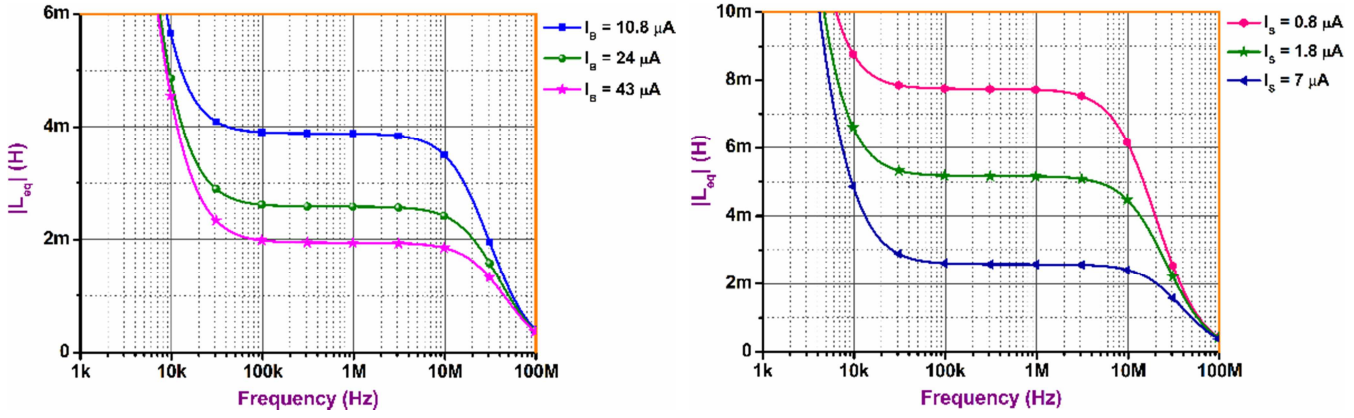
(a) With I_B (b) With I_S

Fig. 9 Variation of impedance magnitude for GIS-2



(a) With I_B (b) With I_S

Fig. 10 Variation of inductance for GIS-1

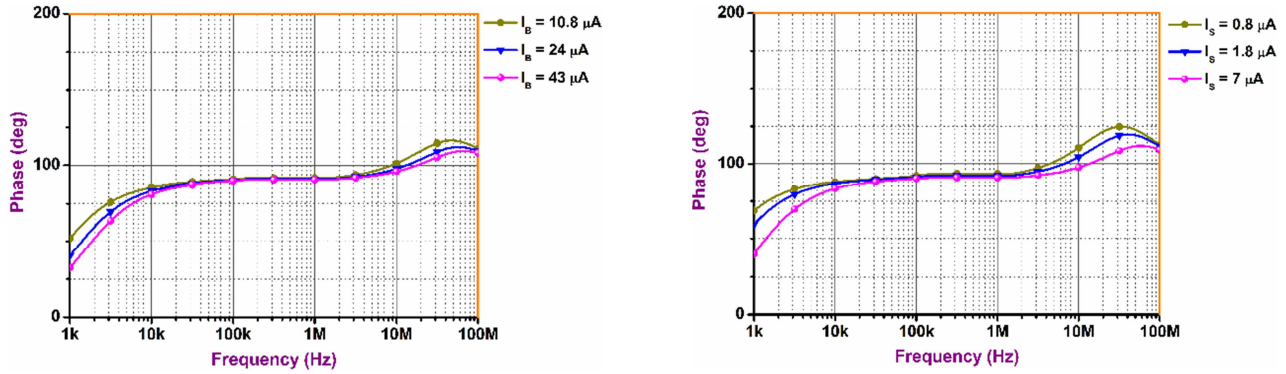


(a) With I_B (b) With I_S

Fig. 11 Variation of inductance for GIS-2

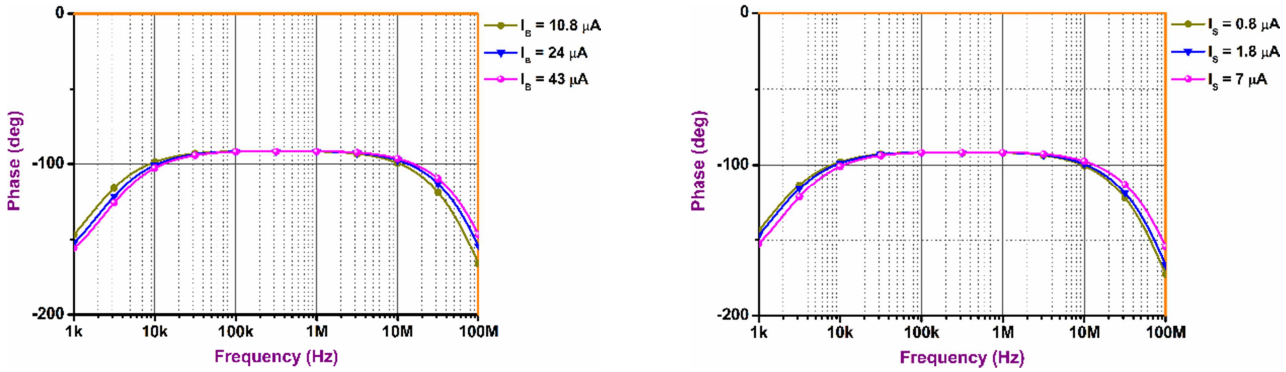
Table 4 Theoretical and simulated inductor values with percentage errors for lossless inductance simulators

Bias current (μA)	Theoretical value (mH)	GIS-1		GIS-2	
		Simulated value (mH)	Error (%)	Simulated value (mH)	Error (%)
I_B = 10.8	3.75	3.88	3.46	3.88	3.46
I_B = 24	2.5	2.58	3.20	2.58	3.20
I_B = 43	1.88	1.94	3.19	1.94	3.19
I_S = 0.8	7.5	7.78	3.73	7.72	2.93
I_S = 1.8	5	5.16	3.20	5.15	3.00
I_S = 7	2.5	2.58	3.20	2.58	3.20



(a) With I_B (b) With I_S

Fig. 12 Variation of phase for GIS-1



(a) With I_B (b) With I_S

Fig. 13 Variation of phase for GIS-2

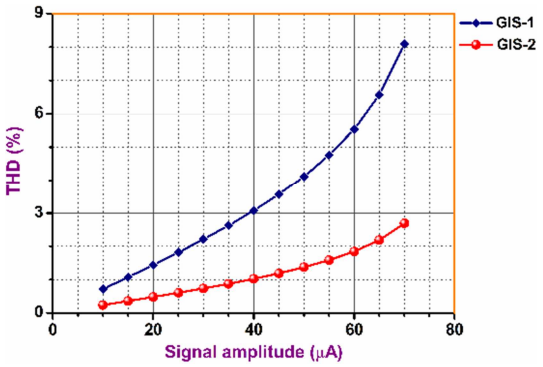
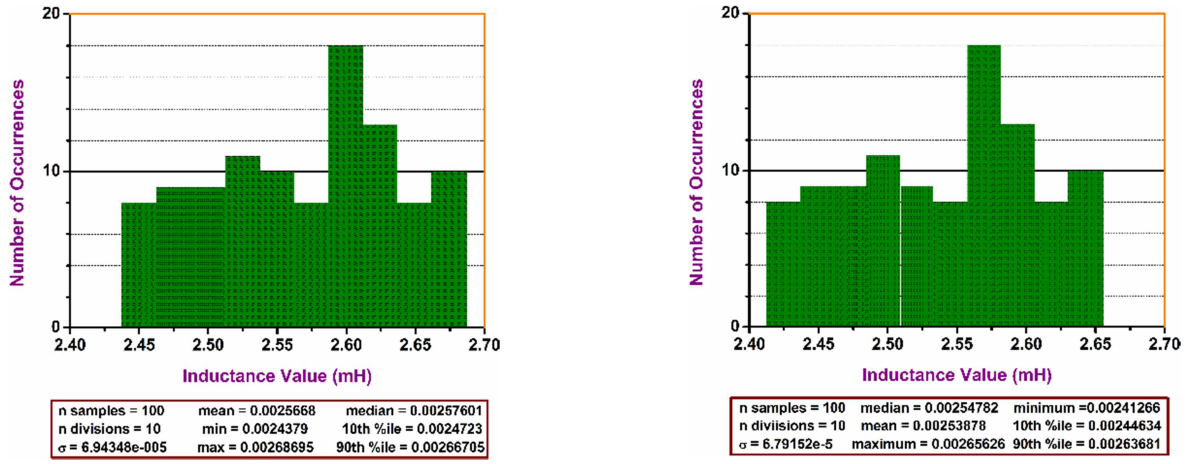
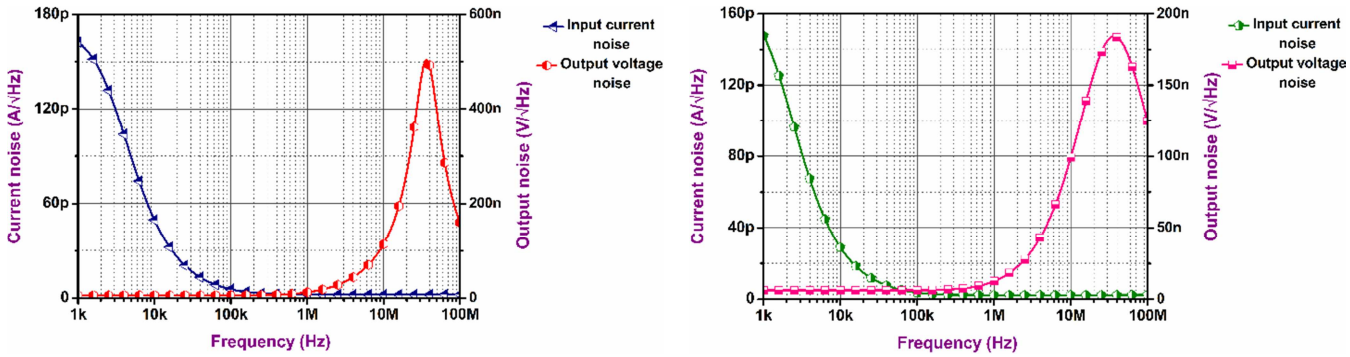


Fig. 14 THD analysis of the lossless inductance simulators' output voltage



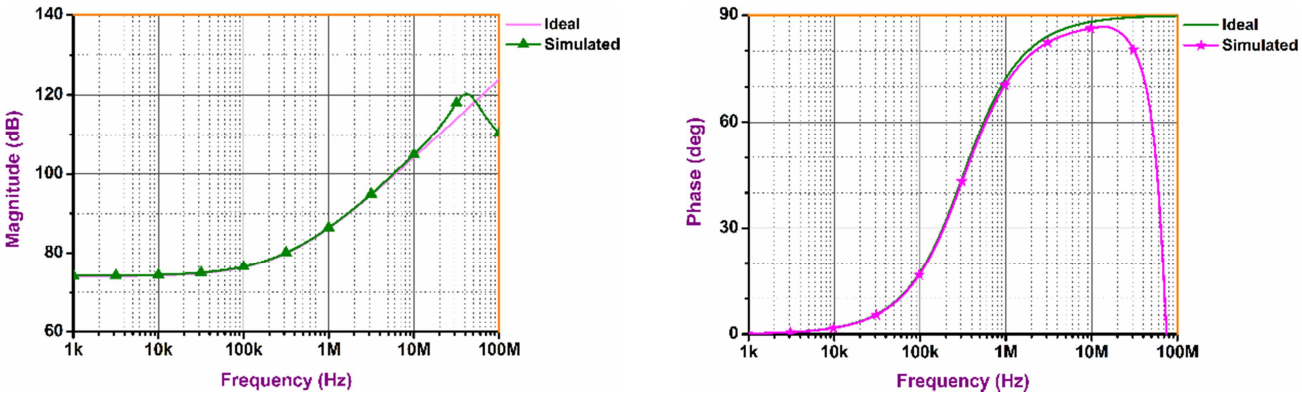
(a) For positive inductor (GIS-1) (b) For negative inductor (GIS-2)

Fig. 15 Monte Carlo simulation results for 10% deviation in the capacitor



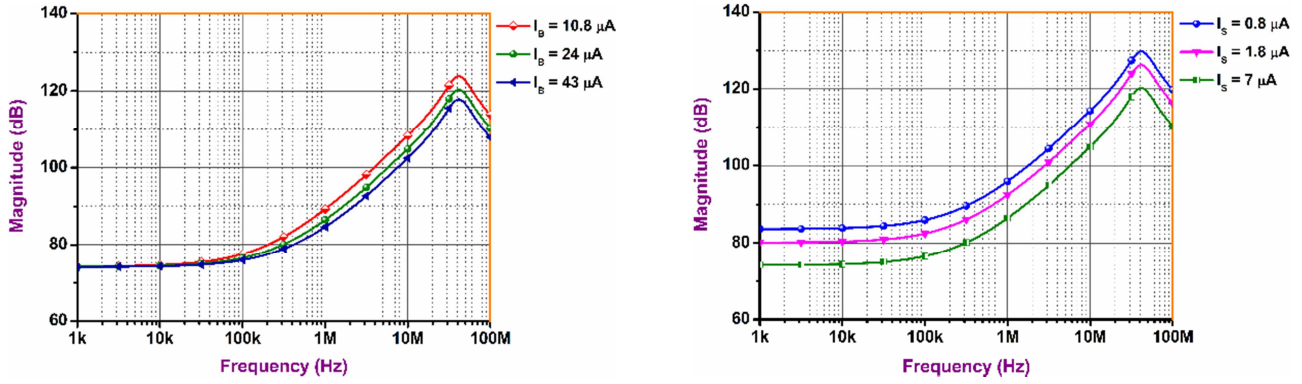
(a) For positive inductor (GIS-1) (b) For negative inductor (GIS-2)

Fig. 16 Output and input referred noise responses of the lossless inductors



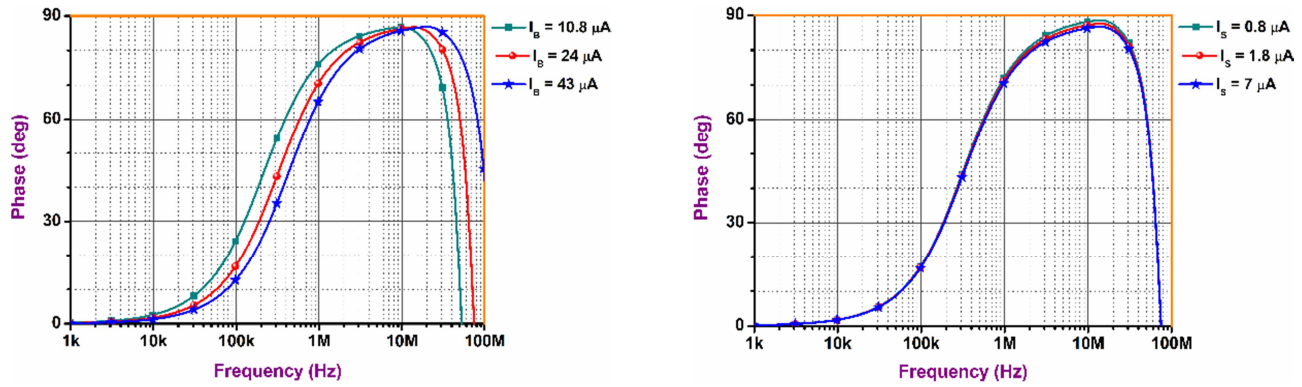
(a) Impedance (b) Phase

Fig. 17 Frequency responses for the proposed GIS-3



(a) For different I_B (b) For different I_S

Fig. 18 Variation of impedance magnitude for GIS-3



(a) For different I_B (b) For different I_S

Fig. 19 Phase-frequency responses of GIS-3

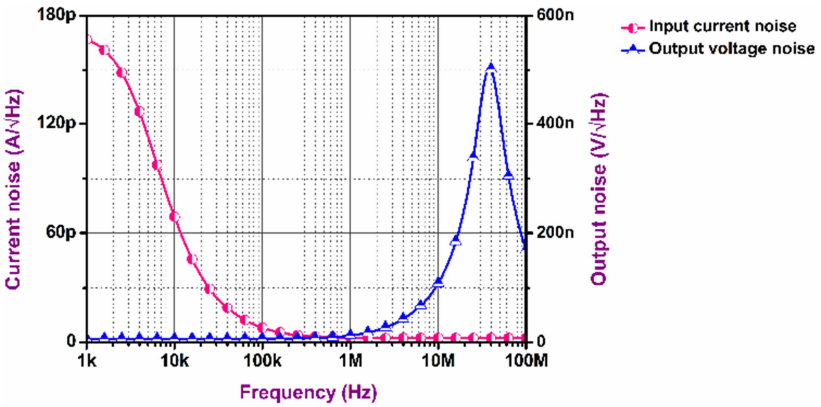
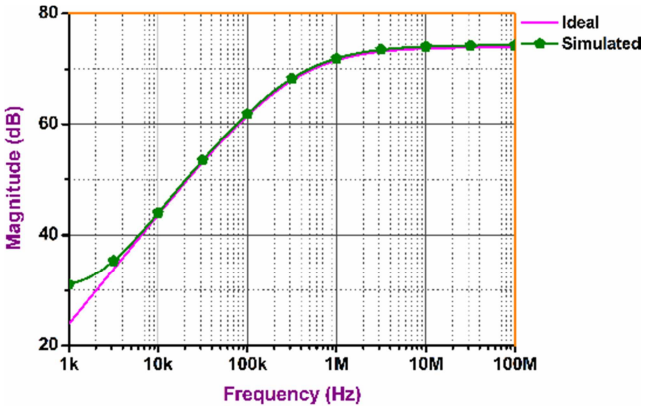


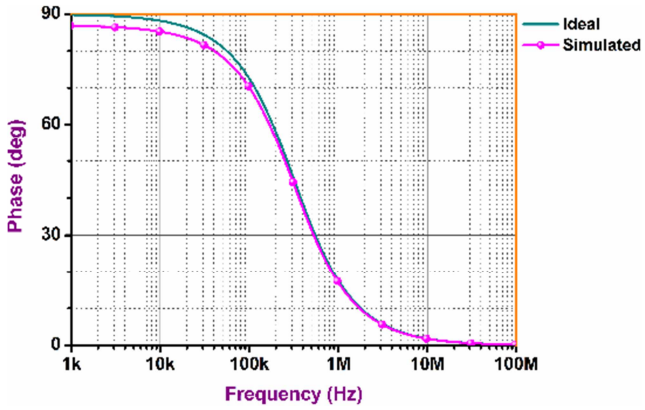
Fig. 20 Output and input referred noise responses of GIS-3

Again, the theoretical and simulated magnitude and phase responses for the input impedance of GIS-4 are given in Fig. 21. From Fig. 21(a), it is concluded that the inductor operates properly between about 20 kHz and about 12 MHz with the relative error within 10%. The electronic tunability of GIS-4 by varying bias currents I_B and I_S is shown in Fig. 22.

Variation of phase for different bias currents has also been performed. Fig. 23 shows the phase variation of GIS-4 for different bias currents. Furthermore, PSPICE noise analysis has been performed on the GIS-4 and the variations in the output voltage and input referred noise is shown in Fig. 24. The output voltage noise at 1 MHz frequency is 14.094 nV/√Hz and the equivalent input current noise is 2.895 pA/√Hz.

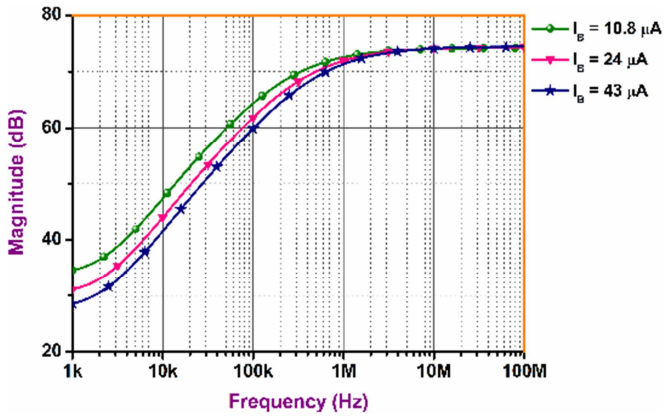


(a) Impedance magnitude

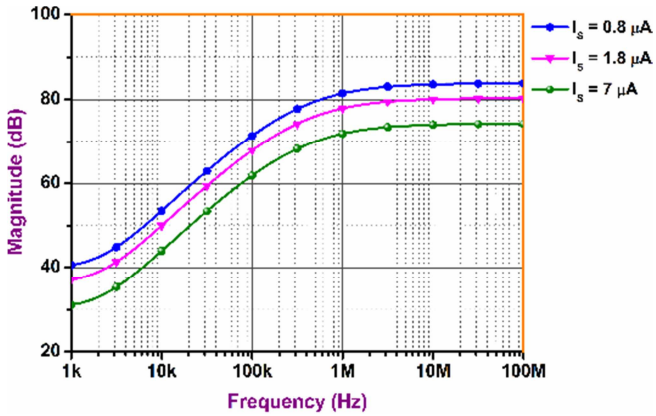


(b) Phase

Fig. 21 Frequency responses for the proposed GIS-4

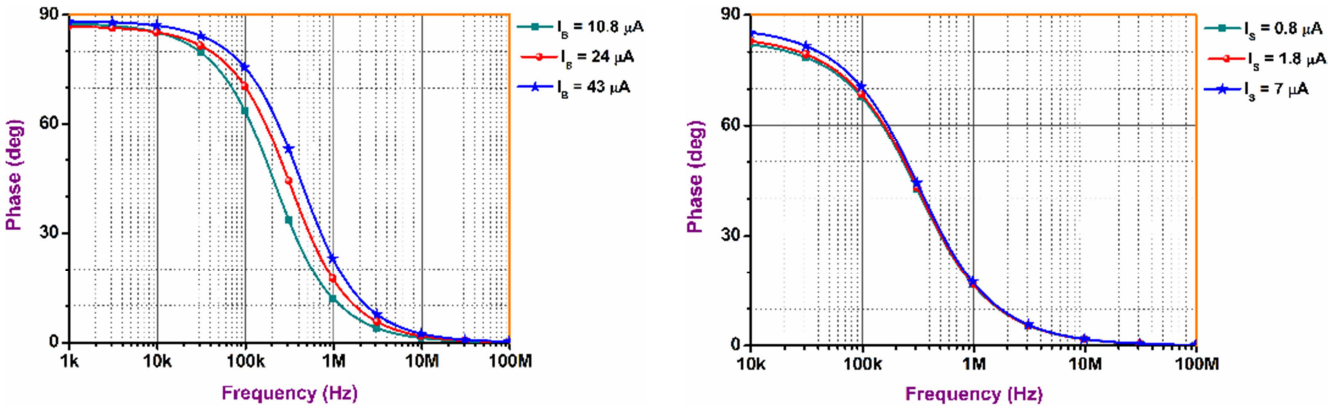


(a) For different I_B



(b) For different I_S

Fig. 22 Variation of impedance magnitude of GIS-4



(a) For different I_B (b) For different I_S

Fig. 23 Variation of phase of GIS-4

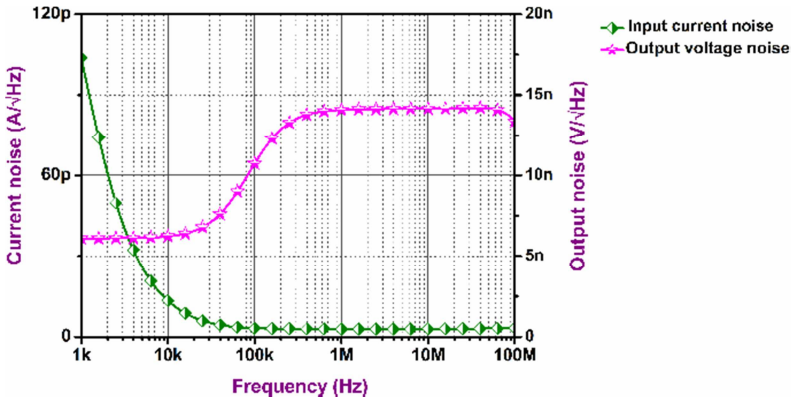


Fig. 24 Output and input referred noise responses of GIS-4

6. Applications

To verify the practical use of the proposed circuits (GISs 1-4), some applications are created using them. The positive inductor is used to design a BP filter, the negative inductor is used to cancel parasitic inductance, the series resistor-inductor circuit is used to design a LP filter, and the parallel resistor-inductor circuit is used to design a parallel resonant circuit.

6.1. Lossless inductors

6.1.1. Positive inductor as voltage-mode BP filter design

The positive GIS (GIS-1) is used to design the BP filter as shown in Fig. 25 [29]. The component values are taken as L = 2.58 mH (I_S = 7.113 µA and I_B = 24.135 µA), R = 4 k, and C =10 pF. Fig. 26 shows the ideal and simulated magnitude responses for the BP filter. The simulation result shows that the pole frequency (f_o) of BP filter is 0.923 MHz. This value is in the error of 3.25% from the theoretical value of 0.954 MHz. The transient analysis of the BP filter is shown in Fig. 27, where a sinusoidal voltage signal with 200 mV peak value at 1 MHz frequency is applied as input. The THD variations in the output voltage for various input signals at 1 MHz frequency are depicted in Fig. 28. It reveals that the THD remains within 2.228% up to 0.5 V input voltage, thus, it confirms the practical utility of the proposed circuit.

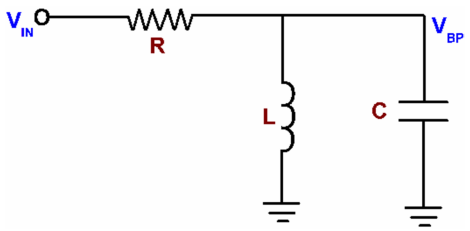


Fig. 25 The structure of the voltage mode BP filter [29]

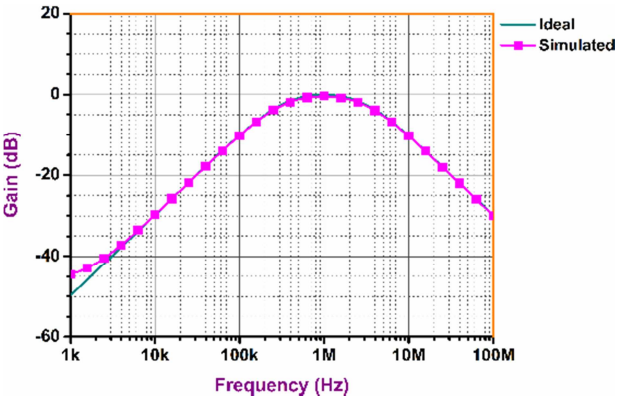


Fig. 26 The gain plot of the response of BP filter

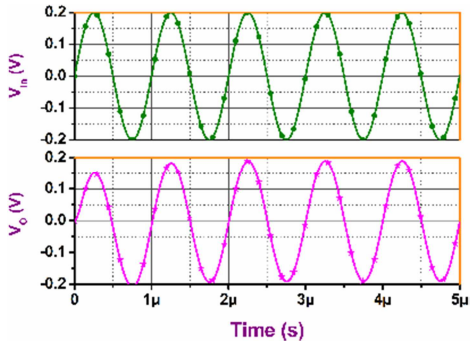


Fig. 27 Transient analysis result of the BP filter

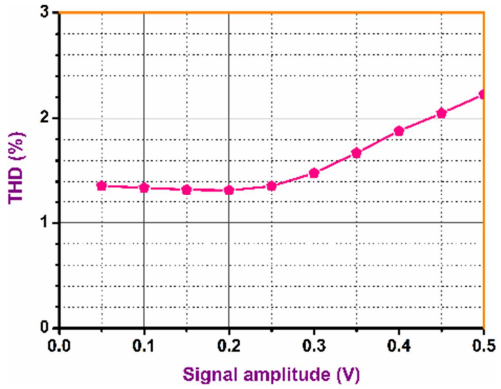


Fig. 28 THD for various input voltage amplitudes for the BP filter application

6.1.2. Negative inductor as an inductance cancellation

To verify the workability of the negative inductor (GIS-2), an inductance cancelation circuit [23] using the proposed negative inductor is demonstrated in Fig. 29. This cancelation circuit plays a major role in the cancellation of any unnecessary inductance presented in an electronic circuit. The values of passive components are selected as R = 1 kΩ and L = 2.58 mH. The simulation result is shown in Fig. 30, where a sinusoidal input signal with the amplitude of 50 mV and the frequency of 500 kHz is applied as input. It is seen that the input voltage (V_{in}) and current (I_{in}) are in phase as the negative inductor cancels the effect of the positive inductor. Hence, the circuit becomes purely resistive.

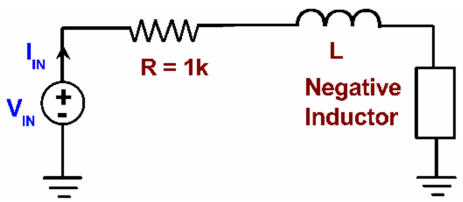


Fig. 29 Inductance cancellation circuit using negative inductor [23]

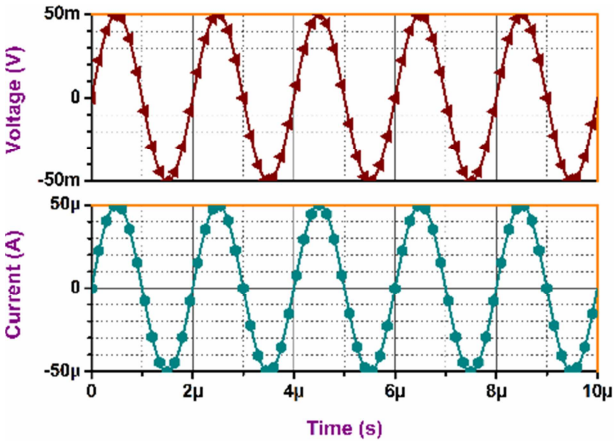


Fig. 30 Transient response of the inductance cancellation circuit

6.2. *Lossy inductors*

6.2.1. *Series R-L as a current-mode LP filter design*

The workability of GIS-4 is examined by reanalyzing a current mode LP filter structure as shown in Fig. 31 [1]. The passive component values are chosen as $I_S = 7.113$ µA, $I_B = 24.135$ µA, and C = 50 pF. The simulation and ideal responses of the LP filter are illustrated in Fig. 32.

To study the effect of mismatches in the component values within GIS-3 on the performance of the LP filter, Monte Carlo simulations have been performed by allocating 5% tolerances to the capacitor value and performing 100 runs. The results for the 5% tolerance are depicted in Fig. 33.

The value of the simulated cut-off frequency is found to be 614.32 kHz, and Monte Carlo analysis indicates that the median value of cut-off frequency is 617.712 kHz, which indicates that the mismatch in the component values within the proposed inductor has a small effect on the realized cut-off frequency.

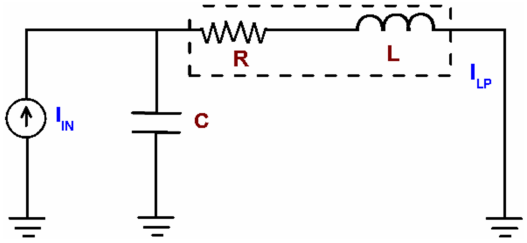


Fig. 31 The structure of the current mode LP filter [1]

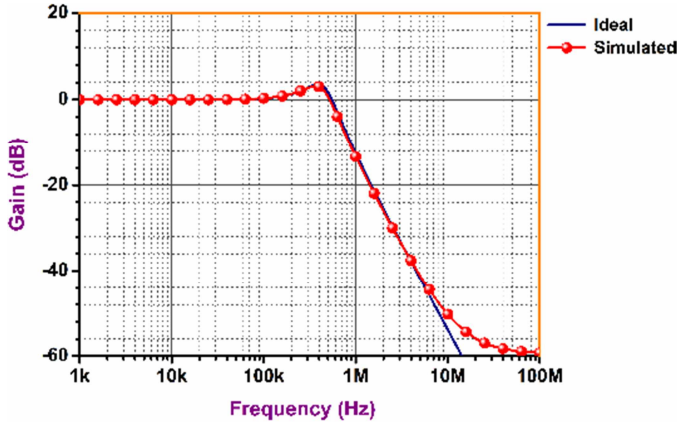


Fig. 32 The gain plot of the LP filter

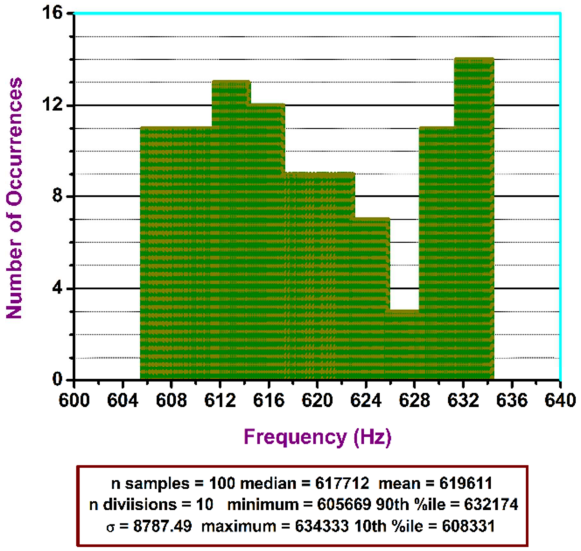


Fig. 33 Simulation results of Monte Carlo analysis for the LP filter

6.2.2. *Parallel R-L as a parallel RLC resonance circuit*

As an application of the reported lossy inductor of parallel R-L type (GIS-4), it can be easily used to design the parallel RLC resonance circuit as shown in Fig. 34 [1]. In simulations, the passive component values are chosen as L_{eq} = 2.58 mH, R = 5 kΩ, and C = 50 pF. The obtained results are depicted in Fig. 35.

To verify the effect of robustness, the Monte-Carlo simulation of RLC resonance circuit has been studied on taking 100 samples and 5% variation in capacitor value. The simulation result is shown in Fig. 36.

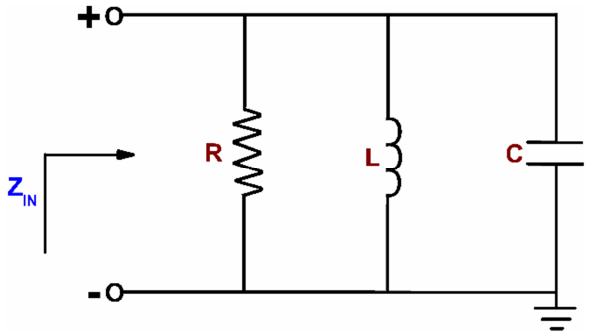


Fig. 34 Parallel RLC resonance circuit [1] realized with the proposed lossy inductor of Fig. 3(d)

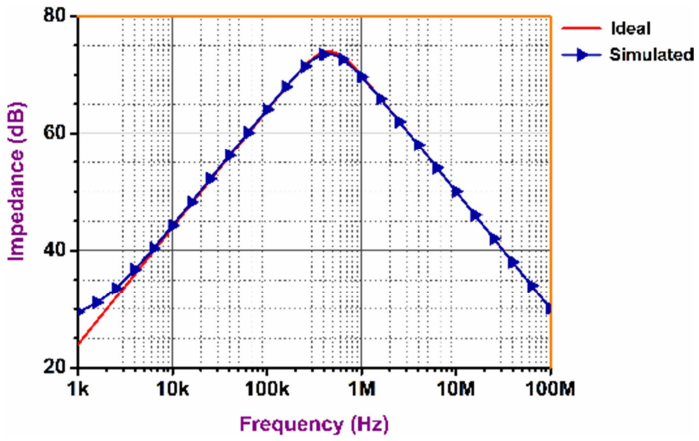


Fig. 35 Impedance-frequency characteristics of the parallel resonance circuit

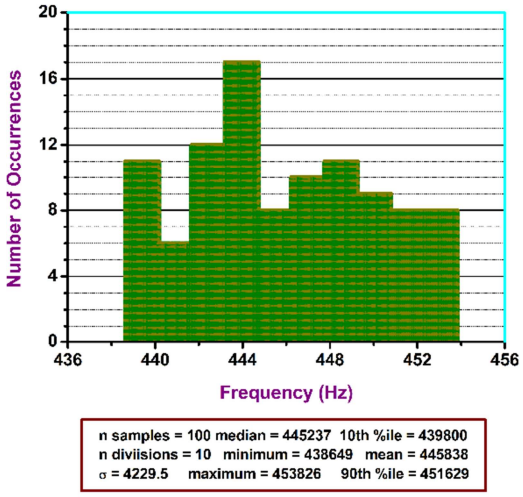


Fig. 36 Simulation results of Monte Carlo analysis for the parallel RLC resonance circuit

7. Comparisons with Previous Publications

Comparison of several performances of the reported inductors with few earlier grounded inductors available in the literature is summarized in Table 5. It is noted that the proposed inductor simulator circuits use a single active block and single grounded capacitor. Also, the circuits do not require any matching conditions.

Although the circuits in [1-8, 11-13, 21-24, 29] use a single active block, the circuits are not resistorless. No resistors are required for the configuration in [9-10, 14-20, 27-28], but all the circuits have one or more drawbacks. The circuit in [9] uses two active blocks and the circuits in [27] use a floating capacitor. On the other hand, a large supply voltage is required in [1, 4-16, 20, 22-25, 29] compared to the proposed circuits. The work in [2-3, 17-19, 21, 26-28] uses the same or less supply voltage compared to the proposed circuits, but the circuits in [2-3, 26-27] consume higher power. The inductor proposed in [17] cannot realize lossless inductors, whereas the work in [18-19] realize only lossless inductor. Series RL circuit cannot be realized in [21]. Also, they require one/two resistor/s. Contrarily, the circuit in [28] uses two active blocks and a floating capacitor. Therefore, the overall performance of the reported inductors is better than any of the inductor circuits cited in Table 5, supporting the design proposal.

Table 5 Comparison between the proposed and previously reported inductor circuits

Ref.	No. and name of active device	Inductor type	G = Grounded, F = Floating		Matching condition	Inbuilt tunability	Technology used	Supply voltage (V)	Frequency range	Power consumption (mW)
			No. of resistors	No. of capacitors						
[1]	1 DXCCDITA	Series RL (Fig. 3(a)) Parallel RL (Fig. 3(b)) Lossless (Figs. 3(c)-(h))	1 (G/F)	1 (G)	Yes No No	Yes	0.35 µm	± 1.5	7 kHz to 10 MHz	Not reported
[2]	1 MDVCC	Lossless	2 (F)	1 (G)	No	No	0.13 µm	± 0.75	100 kHz to 10 MHz	1.61
[3]	1 VDCC	Lossless (Figs. 2 (a)-(b)) Series RL (Fig. 2(c)) + R series – L (Fig. 2(d)) – R series + L (Fig. 2(e)) – R series – L (Fig. 2(f))	1 (G)	1 (G)	No	Yes	0.18 µm	± 0.9	30 kHz to 20 MHz	0.869
[4]	1 DXCCII (Fig. 3(a)) 1 DXCCII (Fig. 3(b))	Lossless	2/3 (G)	1 (F)	Yes	No	0.35 µm	± 1.65	30 kHz to 10 MHz 30 kHz to 30 MHz	Not reported
[5]	1 DXCCII	Lossless (Figs. 2(a), (c)-(f)) Series RL (Figs. 2(b), (f)) Series RL (Figs. 2(c)-(e))	2/3 (1/3G, 1/2F)	1 (G)	Yes	No	0.35 µm	± 2.5	100Hz to 10 MHz	Not reported

Table 5 Comparison between the proposed and previously reported inductor circuits (continued)

Ref.	No. and name of active device	Inductor type	G = Grounded, F = Floating		Matching condition	Inbuilt tunability	Technology used	Supply voltage (V)	Frequency range	Power consumption (mW)
			No. of resistors	No. of capacitors						
[6]	1 DXCCII	Lossless (Fig. 2(a)) Lossless (Fig. 2(b)) + L with parallel – R (Fig. 2(c)) – L with parallel – R (Fig. 2(d)) Parallel RL (Fig. 2(e))	2 (1G, 1F) 2 (1G, 1F) 2 (F) 2 (1G, 1F) 2 (1F)	1 (F)	Yes Yes No Yes Yes	No	0.35 µm	± 1.5	NA	Not reported
[7]	1 CCII+ 2 IVB	Lossless	2 (1G, 1F)	1 (F)	No	No	0.18 µm	± 1.25	200 kHz to 20 MHz (Fig. 3) 200 Hz to 10 MHz (Fig. 5)	Not reported
[8]	1 DXCCTA	Lossless (Fig. 3)	1 (G) (Active)	1 (G) (Active)	No	Yes	0.18 µm	± 1.25	10 Hz to 4 MHz	Not reported
[9]	2 CDTA	Lossless (Fig. 1)	0	1 (G)	No	Yes	0.5 µm	± 2.5	Up to 1 MHz	Not reported
[10]	1 CCCCTA	Lossless	0	1 (G)	No	Yes	PR200N & NR200N	± 1.5	Up to 1 MHZ	Not reported
[11]	1 CDBA	Parallel RL	2 (F)	1 (C)	No	No	AD844	± 12	NA	Not reported
[12]	1 CDBA	Lossless	3 (F)	1 (G)	Yes	No	AD844	± 12	10 kHz to 80 kHz	Not reported
[13]	1 FTFNTA	Lossless (Fig. 6(a))	1 (G)	1 (G)	No	Yes	0.18 µm	± 1.65	1 Hz to 1.5 MHz	1.28
[14]	1 VDGA	Lossless (Fig. 3) Series RL (Fig. 4)	0	1 (G)	No	Yes	0.35 µm	± 1.5	100 Hz to 2 MHz 20 kHz to 2 MHz	0.27
[15]	2 CC-CFA (Figs. 2(a)-(b)) 3 CC-CFA (Fig. 3)	Lossless	0	1 (G)	No	Yes	PR200N, NR200N & 0. 35 µm	± 1.5	Not reported	Not reported
[16]	1 ZC-CFCCC (Fig. 2)	Lossless	0	1 (G)	No	Yes	0.18 µm	± 2.5	Up to 2.99 MHz	2.47
[17]	1 VDTA	Series RL (Figs. 2(a)-(b)) Parallel RL (Fig. 2(c)) +R parallel with – L (Fig. 2(d)) + R parallel with ± L (Fig. 2(e))	0	1 (G)	No	Yes	0.18 µm	± 0.9	Up to 20 MHz	Not reported
[18]	1 VDTA (Fig. 3)	Lossless	0	1 (G)	No	Yes	0.18 µm	± 0.9	600 kHz to 60 MHz	Not reported
[19]	1 VDTA	Lossless	0	1 (G)	No	Yes	0.18 µm	± 0.9	20 kHz to 4 MHz	Not reported
[20]	1 ZC-CCCITA	Lossless	0	1 (G)	No	Yes	0.35 µm	± 1.5	14 kHz to 21 MHz	Not reported
[21]	1 EXCCTA	Lossless (Figs. 1(a)-(b)) Lossless (Fig. 1(c)) + L parallel with ± R (Fig. 1(d)) – L parallel with – R (Fig. 1(e)) + L parallel with + R (Fig. 1(f))	2 (G) 1 (G) 2 (G) 2 (G) 2 (G)	1 (G)	No	Yes	0.18 µm	± 0.9	40 kHz to 10 MHz	Not reported
[22]	1 OTRA	Lossless	4 (F)	1 (F)	Yes	No	0.5 µm	± 1.5	100 Hz to 400 kHz	0.12
[23]	1 OTRA	Lossless	5 (3F, 2G)	2 (F)	Yes	No	AD844	± 5	Up to 100 kHz	Not reported
[24]	1 OTRA (Fig. 2)	Parallel RL	2 (F)	0	No	No	0.5 µm	± 1.5	Not reported	Not reported

Table 5 Comparison between the proposed and previously reported inductor circuits (continued)

Ref.	No. and name of active device	Inductor type	G = Grounded, F = Floating		Matching condition	Inbuilt tunability	Technology used	Supply voltage (V)	Frequency range	Power consumption (mW)
			No. of resistors	No. of capacitors						
[25]	2 OTRA (Figs. 2(a)-(b))	Lossless	5 (F)	1 (F)	Yes	No	0.5µm	± 1.5	1 kHz to 1 MHz	Not reported
[26]	2 OTRA 1 VF	Lossless	1 (F)	1 (F)	No	No	0.18 µm	± 0.9	1 kHz to 9.8 MHz	0.833
[27]	1 VDIBA 1 NMOS	Series RL (Fig. 3(a)) Parallel RL (Fig. 3(b))	0	1 (F)	No	Yes	0.25 µm	± 0.75	1 kHz to 1 MHz	5.72
[28]	2 VDIBA	Lossless	0	1 (F)	No	Yes	0.25 µm	± 0.75	50 KHz to 10 MHz	Not reported
[29]	1 VDBA	Lossless	1 (F)	1 (F)	No	Yes	OPA860	± 5	10 kHz to 10 MHz	Not reported
This work	1 MO-CCCCTA	Lossless (Figs. 3(a)-(b)) Series RL (Fig. 3(c)) Parallel RL (Figs. 3(d)-(e)) + L series with – R (Fig. 3(f)) – L series with – R (Fig. 3(g)) – L parallel with + R (Figs. 3(h)-(i))	0	1 (G)	No	Yes	0.18 µm	± 0.9	20 kHz to 12 MHz	0.784

8. Conclusions

This study comes with an active inductor design for both lossy and lossless inductor simulator configurations which have beneficial properties over former inductor simulator designs. The proposed inductors use only one MO-CCCCTA and one capacitor. The proposed simulators can realize lossless and lossy inductors. All the recommended inductors use only grounded capacitor which is effective for noise cancellation and fabrication. The non-ideal and parasitic analysis of the inductor simulators have also been discussed. To show the beneficial application of the proposed simulators, the proposed positive inductor is used to design a BP filter, whereas the proposed negative inductor is employed to design an inductor cancellation circuit to show the advantageous application of lossless inductor. Series R-L and parallel R-L inductors are used to design the LP and parallel resonance circuit respectively, as an application example. The simulation result using 0.18 µm CMOS process parameter confirms the theoretical analysis.

Acknowledgments

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Conflicts of Interest

The authors declare no conflict of interest.

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