# A Novel Investigation Method for the $S_{21}$ Detection Circuit

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## Abstract

This research proposes a novel method to investigate the performance of the $S_{21}$ detection circuit. Aiming at low frequencies or DC, the method serves as an efficient way of verification and enjoys the benefit of low testing costs. The novel investigation method is demonstrated at 50 MHz and verified by the scattering parameters at 11.05 GHz. Based on the investigation, a model of process variations is constructed. The length of the interface paths is estimated by the model to be 63µm, which is consistent with the corresponding length of 74.6µm in the layout. For the measured phase and magnitude, the model indicates that the process variations in the device under test cause errors of 18.91% and 1.27%, whereas those in the interface paths lead to errors of 1.83% and 1%. Based on the model, practical recommendations are also proposed to further improve the measurement precision in the future.

## 1. Introduction

Scattering parameters (S-parameters) [1-2] are frequently used to characterize the circuit performance in the field of radio frequency (RF). To reduce the costs of testing RF integrated circuits (ICs) with commercial vector network analyzers (VNAs), implementing on-chip S-parameter measurement is one promising research direction [3-10]. Jayaraman [3], Goyal [4], Wu [5], and Howard [6] demonstrated how to exploit the concept of the on-chip measurement to perform self-healing adjustments on RF circuits. Nehring [7] and Niitsu [8] illustrated the possibilities of applying the embedded S-parameter measurement to the field of biomedicine. Philippe [9] and Staszek [10] employed the theory of the six-port reflectometer to execute S-parameter measurement. To implement the on-chip measurement of the transmission coefficient ($S_{21}$) of a two-port device under test (DUT) with a simple circuit, the $S_{21}$ detection circuit was proposed in [11]. The system-level architecture of the $S_{21}$ detection circuit is illustrated in Fig. 1, where the DIV represents the "lumped divider" and the DUT2 represents the exemplary "DUT."
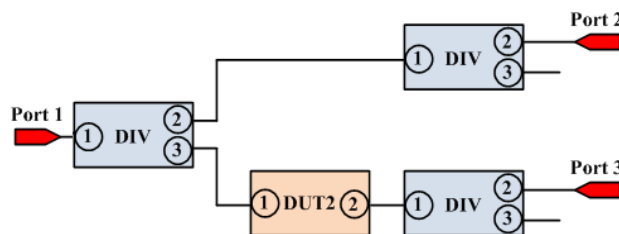


Fig. 1 System-level architecture of the $S_{21}$ detection circuit

When an RF signal is fed into Port 1, the $S_{21}$ of the DUT2 ($S_{21\_DUT2}$) can be derived by dividing the signal reaching Port 3 by the signal reaching Port 2. The derivation is expressed as Eq. (1), where $S_{31\_SYS}$ and $S_{21\_SYS}$ represent the $S_{31}$ and $S_{21}$ of the $S_{21}$ detection circuit, and $S_{21\_DUT2\_DERIVED}$ is defined as the quotient. At around the targeted operational frequency,

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$S_{21\_DUT2\_DERIVED}$ will approach $S_{21\_DUT2}$, signifying that the $S_{21}$ detection circuit functions properly. The closer $S_{21\_DUT2\_DERIVED}$ approaches $S_{21\_DUT2}$, the higher measurement precision the $S_{21}$ detection circuit can achieve. In [11], $S_{31\_SYS}$ and $S_{21\_SYS}$ were measured by a VNA, and $S_{21\_DUT2}$ was obtained through simulation. Although the proximity between $S_{21\_DUT2\_DERIVED}$ and $S_{21\_DUT2}$ was well demonstrated, discrepancies were also found in [11]. To improve the measurement precision of the $S_{21}$ detection circuit, potential causes of the measurement discrepancies require to be studied. However, because the test chips were already fabricated with the DUT2 embedded, the high level of integration and the fixed accessible ports greatly complicate the exploration of process variations.

$$\frac{S_{31\_SYS}}{S_{21\_SYS}} \equiv S_{21\_DUT2\_DERIVED} = S_{21\_DUT2} \tag{1}$$

To address this problem, previous studies provide the valuable reference knowledge in different fields. Since process variations have been an important issue in the fabrication of modern ICs, they have been studied in various aspects [12-16]. For example, Paul [12] studied the effects of process variations on different types of field-effect transistors (FETs). Lu [13] explored the reliability of nanometer-scale ICs. Zahira [14] researched the effects of independent intra-die process variations. Yoon [15] investigated the performance of sub-5-nm node fin FETs (FinFETs) and nanosheet FETs (NSFETs) in the presence of process variations. KONG [16] studied how process variations influence the near-threshold cache memories. In addition, efforts have been made to reduce the gap between circuit design and chip performance [17-19]. Miliozzi [17] explored the challenges of designing RF ICs (RFICs). Putek [18] studied the coupling problems of RFICs. Banerjee [19] researched how the performance of carbon-nanotube FETs is affected by process variations.

Moreover, diverse works [20-24] have demonstrated intelligent strategies to analyze the performance of ICs. In [20], Bandler proposed the concept of network decomposition, which views a large network as mutually uncoupled subnetworks. In [21], Murji constructed the scalable model of the meander-line resistor for RFICs with measured S-parameters and verified it with simulated ones. In [22], Ellouz used internal DC node voltages to estimate RF parameters. In [23], Huang employed machine-training techniques to reduce the excessive costs of specification testing in analog and RF circuits. In [24], Subramani demonstrated the exploration of the activation energy and cross section of the traps by using a more economical method.

The above great works [12-24] inspired this research to propose a novel investigation method for the $S_{21}$ detection circuit. Thanks to the high symmetry between the Port1-to-Port2 and Port1-to-Port3 paths, the method can investigate the performance of the test chips of the $S_{21}$ detection circuit at a low frequency or DC. Requiring no expensive instruments or complicated procedures for high-frequency measurement, the method enjoys low testing costs and is thus suitable for production test.

To present the investigation method, the remainder of this paper is organized as follows. Section 2 presents the novel investigation method and demonstrates it by analyzing the S-parameters measured at 50 MHz. Section 3 verifies the investigation method by analyzing the S-parameters at the targeted operational frequency, 11.05 GHz. By integrating the investigation at the two frequencies and by referring to the layout, post-layout simulation, and other related information, Section 4 constructs a model of process variations. Section 5 discusses various aspects of this research. Subsection 5.1 discusses the comparisons between prior related works and this research. Subsection 5.2 discusses two important assumptions used in this research. Subsection 5.3 discusses the model of process variations and the layout of the test chips. Subsection 5.4 discusses important observations and proposes useful recommendations for improving the measurement precision. Finally, Section 6 summarizes the important achievements of this research.

## 2. Novel Investigation Method

The simulation and measurement results of the $S_{21}$ detection circuit around the targeted operational frequency in [11] are reviewed in Fig. 2. The $S_{21\_DUT2}$ curve, acquired by simulating the DUT2 alone, represents the ideal data of the $S_{21}$ of the DUT2.

Due to the lack of a stand-alone DUT2, $S_{21\_DUT2}$ is used as the substitute for the real $S_{21}$ of the DUT2 after the fabrication. Although possible process variations may make the substitution imprecise, it is the best approximation that is available. The $S_{21\_DUT2\_DERIVED}$ curve, obtained by applying the simulated $S_{21\_SYS}$ and $S_{31\_SYS}$ to Eq. (1), represents the predicted measurement results speculated by the simulation. The $S_{21\_DUT2\_MEASURED}$ curve, derived by applying the measured $S_{21\_SYS}$ and $S_{31\_SYS}$ to Eq. (1), symbolizes the real measurement results. The magnitude and phase of $S_{21\_DUT2\_DERIVED}$ are closest to those of $S_{21\_DUT2}$ at 11.25 GHz, the targeted operational frequency in the design stage. Similarly, $S_{21\_DUT2\_MEASURED}$ approaches $S_{21\_DUT2}$ the most at around 11.05 GHz, the targeted operational frequency in the real implementation. Obviously, both $S_{21\_DUT2\_DERIVED}$ and $S_{21\_DUT2\_MEASURED}$ demonstrate the same trend of approaching $S_{21\_DUT2}$ despite some difference, which is caused by process variations. The X-axis of the shaded area signifies the 3%-error bandwidth of $S_{21\_DUT2\_MEASURED}$ with respect to $S_{21\_DUT2}$ when neglecting the errors in the phase.
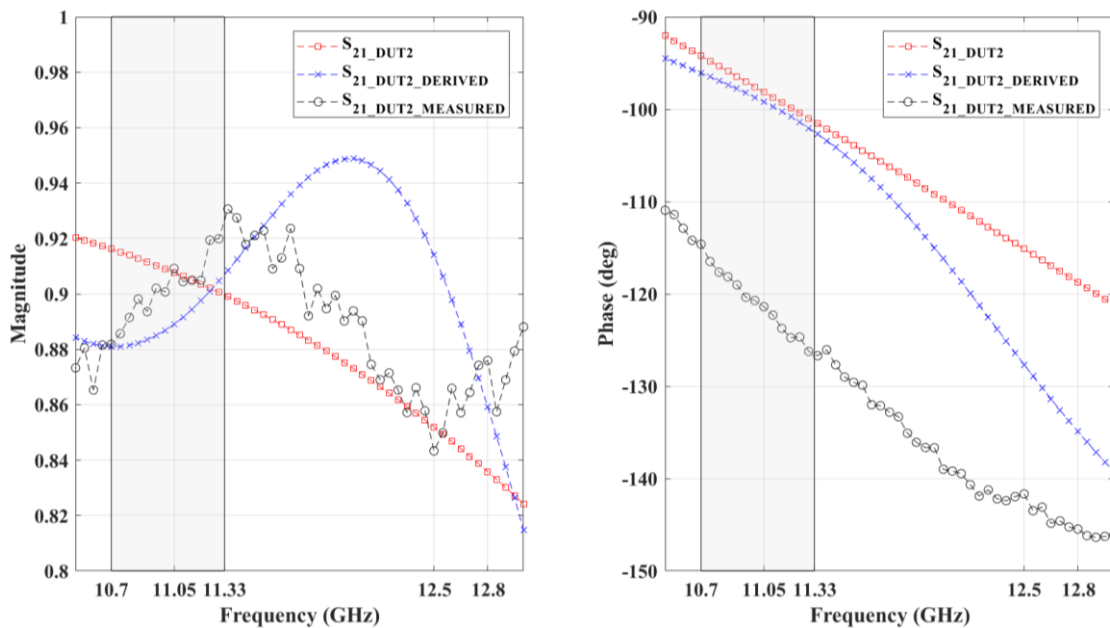


Fig. 2 Simulation and measurement results of the $S_{21}$ detection circuit around the targeted operational frequency

The schematics of the DIV and the DUT2 in Fig. 1 are illustrated in Fig. 3 and Fig. 4. By replacing the DIVs and DUT in Fig. 1 with their schematics, Fig. 1 contains at least twenty four devices, each of which may undergo certain process variations. With many possible combinations, it is difficult to study the potential process variations causing the measurement discrepancies only by using the information in Fig. 2. What is worse, with the DUT2 being embedded, its performance is difficult to ascertain independently.
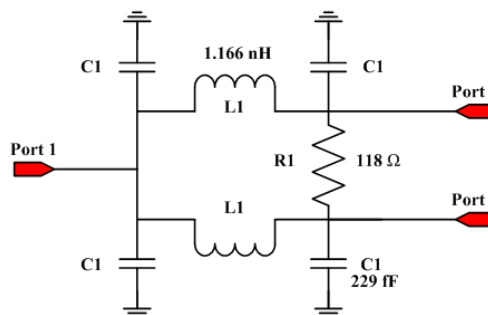


Fig. 3 Schematic of the DIV in the $S_{21}$ detection circuit

To address the above difficulties, this section proposes a novel investigation method that can systematically analyze the performance of the $S_{21}$ detection circuit. The method operates at a low frequency or DC by examining the impedance looking into Port 1 with Ports 2 and 3 terminated, respectively. With the $S_{21}$ detection circuit measured from 50 MHz to 15 GHz, the two-port S-parameters measured at 50 MHz are the best example chosen for the demonstration. At such a low frequency, the

capacitors and inductors within the $S_{21}$ detection circuit can be approximated as open circuits and simple resistors [25]. Such approximation can greatly simplify the $S_{21}$ detection circuit and help identify the most important element of the process variations.
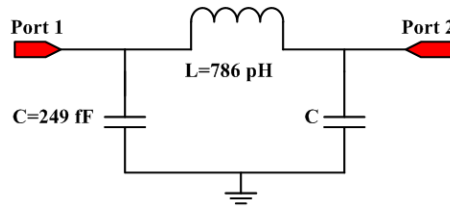


Fig. 4 Schematic of the DUT2 in the $S_{21}$ detection circuit

After applying the above rules of approximation, the $S_{21}$ detection circuit can be simplified as Fig. 5. The resistors $R_{DIV}$ and $R_{118}$ represent the resistance of the inductor L1 and that of the resistor R1 in the DIV, respectively. The resistor $R_{DUT2}$ symbolizes the resistance of the inductor L in the DUT2. Using Fig. 5, the impedance looking into Port 1 should be the $Z_x$ in Fig. 6 when performing the two-port S-parameter measurement at Ports 1 and 2. Similarly, the impedance looking into Port 1 should be the $Z_y$ in Fig. 7 when performing the two-port S-parameter measurement at Ports 1 and 3.
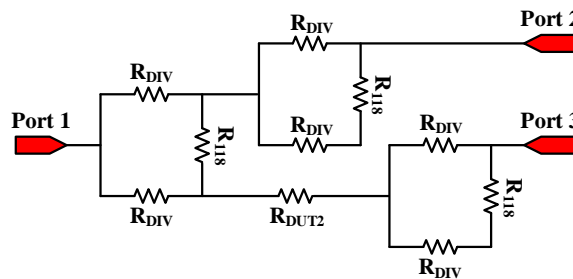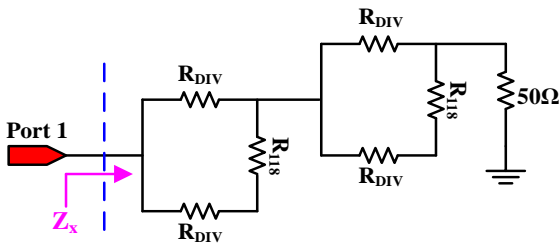


Fig. 5 Simplified $S_{21}$ detection circuit



Fig. 6 Impedance looking into Port 1 when performing the two-port S-parameter measurement at Ports 1 and 2
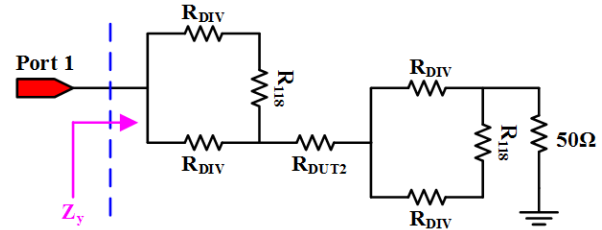
Fig. 7 Impedance looking into Port 1 when performing the two-port S-parameter measurement at Ports 1 and 3

By comparing Fig. 6 and Fig. 7, it can be found that $Z_x$ and $Z_y$ differ only by the resistor $R_{DUT2}$. This is a useful finding and the core of the novel investigation method because the originally unmeasurable $R_{DUT2}$ becomes practically measurable. To obtain the $Z_x$ and $Z_y$, the S-parameters measured by a commercial VNA must be transformed into the corresponding Z-parameters by using Eq. (2) [26-28]. Depending on the ports being measured, the Z in Eq. (2) can represent the $Z_x$ and $Z_y$, respectively. Finally, by subtracting $Z_x$ from $Z_y$, the value of $R_{DUT2}$ can be derived. Likewise, the ideal value of $R_{DUT2}$ can be acquired by applying the above derivation procedures to simulation.

$$S_{11} = \frac{Z - 50}{Z + 50} \tag{2}$$

The S-parameters were measured by using the E8361A of Agilent Technologies. Fig. 8 illustrates the test setup for performing the two-port S-parameter measurement at Ports 1 and 2. According to the measurement results, measuring Ports 1 and 2 derives an $S_{11}$ of 0.121 at 50 MHz with a phase of −16.76 degrees. Besides, measuring Ports 1 and 3 derives an $S_{11}$ of 0.1521 at 50 MHz with a phase of −13.06 degrees. By neglecting the phases and by applying 0.121 and 0.1521 to Eq. (2), the $Z_x$

and $Z_y$ can be derived to be 63.77Ω and 67.94Ω. This means that the $R_{DUT2}$ in the real implementation is 4.17Ω. Compared with the simulated $R_{DUT2}$, 2.21Ω, the measured $R_{DUT2}$ is larger. The increase in $R_{DUT2}$ reveals that an extra resistance of 1.96Ω was formed between Ports 1 and 3 as the test chips were fabricated.
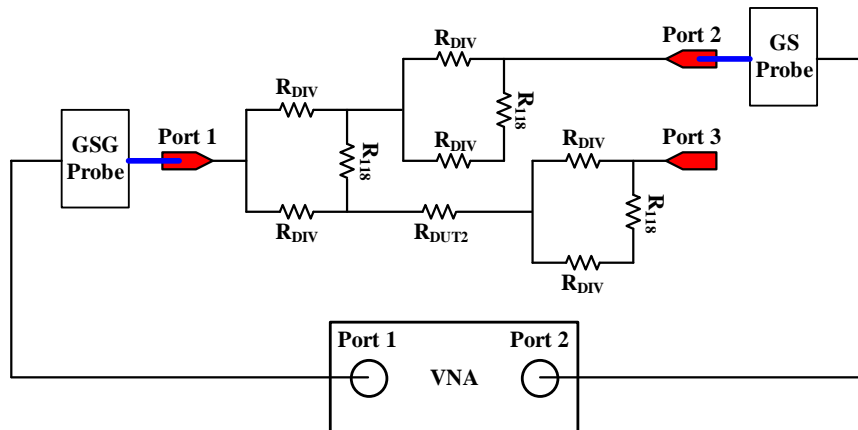


Fig. 8 Test setup for performing the two-port S-parameter measurement at Ports 1 and 2

The above demonstration shows that the novel investigation method can successfully capture the key abnormality of the $S_{21}$ detection circuit that caused the measurement discrepancies. Based on the simplified circuit in Fig. 5, the investigation method can also be performed at DC, which fits the rules of approximation even better. With lower testing costs and higher measurement precision at lower frequencies, the novel investigation method provides an economical and efficient solution to testing the $S_{21}$ detection circuit.

## 3. Verifying the Novel investigation Method at the Targeted Operational Frequency

The novel investigation method in Section 2 discovered an additional resistance of 1.96Ω between Ports 1 and 3 of the $S_{21}$ detection circuit. The resistance is likely to come from the DUT2 and cause the measurement discrepancies in [11]. To verify such a finding, this section attempts to investigate the S-parameters measured at the targeted operational frequency.

For the fabrication of modern ICs, an extra resistance can result from a reduction in the width of a conducting path or an addition to the length of a conducting path [29-31]. However, the former can hardly affect the phase of an RF signal traveling on it, whereas the latter can easily increase phase lags [32-33]. According to Fig. 2, the phase of $S_{21\_DUT2\_MEASURED}$ lags that of $S_{21\_DUT2\_DERIVED}$ by about 20 degrees at 11.05 GHz. This means that the extra resistance should come from a prolonged conducting path. In other words, the measurement discrepancies in [11] are potentially caused by an additional segment of conducting path between Ports 1 and 3 of the $S_{21}$ detection circuit.

To further examine the phase lags, Fig. 9 illustrates the phases of the simulated and measured $S_{21}$ and $S_{31}$ of the $S_{21}$ detection circuit. As can be noted, both of the measured $S_{21}$ and $S_{31}$ lag their simulated counterparts. At 11.05 GHz, the measured $S_{21}$ lags the simulated $S_{21}$ by approximately 81.37 degrees, whereas the measured $S_{31}$ lags the simulated $S_{31}$ by approximately 101.94 degrees. This phenomenon indicates that the Port1-to-Port2 and Port1-to-Port3 paths are both lengthened by the process variations. Moreover, the additional lag of 20.57 degrees in the phase of the measured $S_{31}$ corroborates the extra resistance discovered in $R_{DUT2}$.

However, it should be noted that the additional conducting path between Ports 1 and 3 affects the magnitude and phase of $S_{21\_DUT2\_MEASURED}$ differently. According to Fig. 2, at 11.05 GHz, the magnitude and phase of $S_{21\_DUT2\_MEASURED}$ are 0.9092 and −119.7803 degrees, whereas those of $S_{21\_DUT2\_DERIVED}$ are 0.889 and −99.2084 degrees. This means that the error percentage of the magnitude and phase of $S_{21\_DUT2\_MEASURED}$ with respect to those of $S_{21\_DUT2\_DERIVED}$ are approximately 2.27% and 20.74%, respectively. In other words, the error in the measured magnitude is much less than that in the measured phase, a phenomenon

that can be directly visualized by Fig. 2. It is reasonable that the extra resistance causes a smaller error in the magnitude measurement because the signal attenuation caused by a 1.96Ω resistance in series is small. Indeed, inserting 1.96Ω into a lossless two-port network with 50Ω characteristic impedance only attenuates the magnitude of the $S_{21}$ from unity to 0.981 [26], causing an error of approximately 2%.
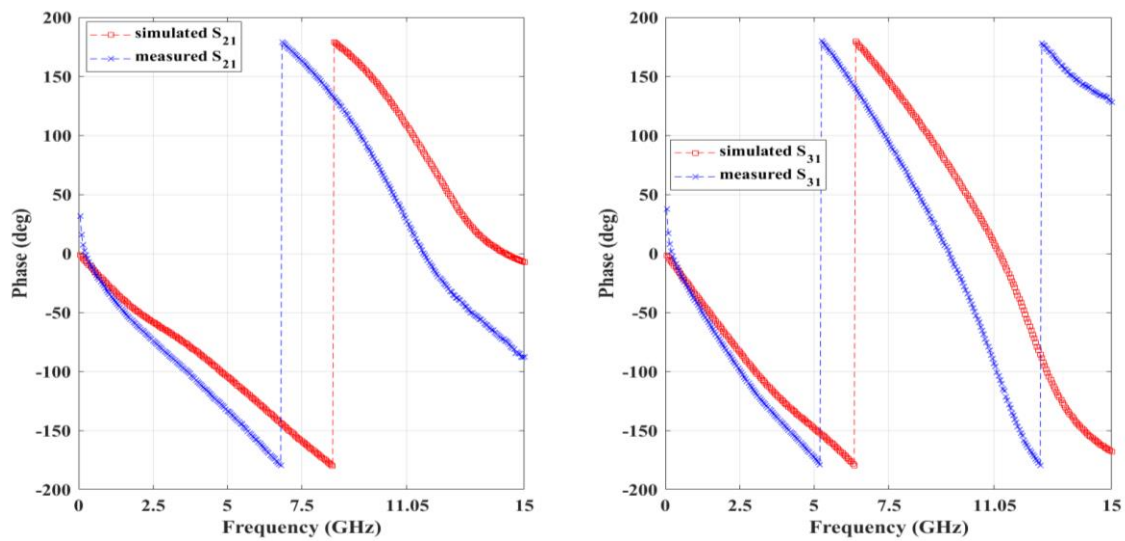


Fig. 9 The phases of the simulated and measured $S_{21}$ and $S_{31}$ of the $S_{21}$ detection circuit

## 4. Model of Process Variations

The previous two sections discovered an extra path of 1.96Ω resistance between Ports 1 and 3 of the $S_{21}$ detection circuit. Furthermore, the novel investigation method in Section 2 derived that the additional resistance was potentially caused by $R_{DUT2}$, the resistance of the inductor L in the DUT2. Hence, the following investigation aims to examine the finding and to modify it if necessary with an ultimate goal of building a complete model of process variations for the discovered additional path.

According to the post-layout simulation, the inductor L of the DUT2 has a resistance of 2.214Ω and causes a phase shift of –37.9909 degrees at 11.05 GHz. For a conducting path, the resistance and the phase lag caused by it are both linearly proportional to the length of that path for the first-order approximation [32-33]. Therefore, it is suitable to assume that the two parameters are linearly proportional to each other for a conducting path made of a certain material. With this assumption, if the extra resistance of 1.96Ω were completely caused by a prolonged path in the inductor L of the DUT2, the extra phase lag would be 33.63 degrees, as interpolated by Eq. (3). However, Fig. 9 illustrates that the additional lag in the phase of the measured $S_{31}$ is only 20.57 degrees at 11.05 GHz. Therefore, the extra path between Ports 1 and 3 cannot be fully attributed to the process variations in the L of the DUT2. Equivalently, the extra resistance of 1.96Ω cannot be solely produced by the process variations in the L of the DUT2.

$$(37.9909) \times \frac{1.96}{2.214} \approx 33.63 \tag{3}$$

Because the measurement discrepancies cannot be solely ascribed to an extra path in the inductor L of the DUT2, another possibility must be investigated. Connected in series with the inductor L, the interface conducting paths are the closest to the L and thus should be the next investigation target. Hence, it will be examined whether the measurement discrepancies can solely result from the process variations in the interface paths, which connect the DUT2 to the core of the $S_{21}$ detection circuit.

According to the layout, the width of the two interface paths linking the DUT2 with the core of the $S_{21}$ detection circuit is 6.48 μm. Of all the metal layers supported by the IBM 7RF technology, these paths were intentionally fabricated with the metal layer—MT, which is good for long-distance connection due to its low sheet resistance, 0.089Ω/square. Based on the

post-layout simulation, an MT-layer path with a width of 6.48μm and a length of 64.8μm can cause a phase shift of −1.86225 degrees at 11.05 GHz. Therefore, if the extra resistance between Ports 1 and 3 were caused by the interface paths alone, the length of the paths would be 696μm, as required by Eq. (4). However, because 696μm is too large a process variation to be possible, the extra resistance cannot originate entirely from the interface paths.

$$(64.8) \times \frac{20}{1.86225} \approx 696 \tag{4}$$

In sum, ascribing the process variations entirely to the L of the DUT2 and to the interface paths cause a surplus and a deficient phase lag between Ports 1 and 3, respectively. Based on this finding, this research proposes a hybrid model for the additional conducting path discovered between Ports 1 and 3. The model assumes that the extra path comprises two components: an additional path in the L of the DUT2 and an extra path in the interface paths linking the DUT2. Using this model, the lengths of the two types of extra paths can be solved by assuming that the resistance of the extra path in the L is $x$ Ω and that in the interface paths is $y$ Ω. Hence, the additional resistance and phase lag between Ports 1 and 3 can be expressed as Eqs. (5) and (6), where 1.96Ω and 20 degrees are replaced by 1.9588Ω and 20.57 degrees to enhance the precision of numerical computation. Since linear algebra [34] requires two independent equations to solve two variables, x and y can be derived by solving the simultaneous Eqs. (5) and (6).

$$x + y = 1.9588 \tag{5}$$

$$(37.9909) \times \frac{x}{2.214} + (1.86225) \times \frac{y}{0.89} = 20.57 \tag{6}$$

By solving Eqs. (5) and (6) together, the x and y are found to be 1.09321 and 0.86559 [35]. That is, the additional path in the L of the DUT2 and that in the interface paths create 55.8% and 44.2% of the extra resistance and cause 91.2% (i.e., 18.76 degrees) and 8.8% (i.e., 1.81 degrees) of the extra phase lag, respectively. According to Eq. (7), to create a phase lag of 1.81 degrees requires the length of the additional path in the interfaces to be 63μm, which is more reasonable in comparison with 696μm.

$$(64.8) \times \frac{1.81}{1.86225} \approx 63 \tag{7}$$

## 5. Discussion

This section discusses various aspects of this research. Subsection 5.1 discusses the comparisons between this research and the previous related studies. Subsection 5.2 discusses two important assumptions used previously. These assumptions prove to be useful in revealing insights into the defects and possible process variations of the test chips when available measured data are limited. Subsection 5.3 discusses the model of process variations and the layout of the test chips corporately. Based on the joint investigation, practical recommendations are proposed in Subsection 5.4 to improve the measurement precision of the $S_{21}$ detection circuit.

### 5.1. Comparisons with past works

The novel investigation method proposed by this research serves as an efficient and low-cost testing method for the $S_{21}$ detection circuit. As introduced in Section 1, related works in various domains [12-24] have provided valuable inspiration and knowledge for the development of the method. Because the investigation method is particularly designed for the $S_{21}$ detection circuit, counterparts highly comparable with the method seem to be absent in the literature. Hence, the following discussions will focus mainly on how related works contribute to the formation of the novel investigation method.

Paul [12] discovered that nanowire and nanotube FETs are less sensitive to many process variations than conventional Metal-Oxide-Semiconductor FETs (MOSFETs) and FinFETs. Lu [13] presented a statistical reliability optimization flow for nanometer-scale IC design by jointly considering the impact of fabrication-induced process variation and run-time aging effects. Zahira [14] developed an efficient gate-sizing methodology for improving circuit speed in the presence of independent intra-die process variations. Yoon [15] revealed that the performance of sub-5-nm NSFETs is less affected by process variations than that of the FinFETs through simulation. KONG [16] proposed a variable-latency L1 data cache architecture to reduce the effects of process variations and improve the yield of near-threshold cache. Unlike the works [12-16] aiming to find an optimal solution in the face of process variations, this research focuses on finding an efficient way to investigate the process variations in the test chips. However, inspired by them, this research does not stop at the demonstration of the novel investigation method. Instead, it exploits the method to infer the model of process variations, based on which recommendations are proposed to reduce the effects of process variations.

To facilitate the design of low-power RFICs, Miliozzi [17] proposed a design system, which explores possible aid from tools, methodologies, models, and layout capabilities. To address on-chip coupling effects in the early design phases of RFICs, Putek [18] proposed the response surface model to quantify the uncertainty of the RFIC interface. To gain a broader understanding of the performance of carbon-nanotube FETs, Banerjee [19] presented a systemic approach to study the impact of process variations. The three works [17-19] endeavored to make the performance of ICs approach the simulation from a higher perspective, such as making a design flow, constructing a statistical model, or running extensive Monte Carlo simulations. On the other hand, this research does not directly aim at such a goal. However, recommendations that can strategically reduce the gap between the simulation and real chip performance will still be proposed at the layout level in Subsection 5.4. These recommendations are the by-product of the model of process variations, which is produced by the novel investigation method, the core of this research.

As for the intelligent analysis methods, the divide-and-conquer strategy proposed by Bandler [20] helped form the model of process variations. Murji's model [21] inspired the idea of acquiring information by comparing the measured and the simulated data, which is a key element of the novel investigation method. In addition, the data-fitted model also inspired the development of the model of process variations. The major difference between Murji's work and this research is that this research particularly concerns the analysis at low frequencies with a simple resistive model. Ellouz's work [22] enlightened the author on the potentiality of investigating circuit performance at low frequencies. Furthermore, the idea of replacing costly RF testing with signature-based verification facilitates the development of the novel investigation method. However, due to the symmetry of the $S_{21}$ detection circuit, the novel investigation method does not require neural networks as a regression model, which is a major difference between Ellouz's work and this research. Huang [23] attempted to replace costly testing with a low-cost substitution implemented by training the combined die-level and wafer-level information. Subramani [24] investigated the activation energy and cross section of the traps in the GaN buffer by low-frequency S-parameter measurement. Indeed, all three works [22-24] stimulated this study to search for an appropriate figure of merit that can efficiently test the performance of the $S_{21}$ detection circuit. Normally, the select figure of merit is required to be obtained at low frequencies and to possess physical meanings. As presented in Section 2, the figure of merit of this research is the difference in the impedances looking into Port 1 with Ports 2 and 3 terminated, respectively. As the core of the novel investigation method, the figure of merit extracted at low frequencies satisfies the two requirements and enables the method to enjoy the advantage of low costs.

Although the investigation method of this research is originally designed for the $S_{21}$ detection circuit, its applications are not limited to the $S_{21}$ detection circuit. As demonstrated in Section 2, any circuit operating differentially enjoys the privilege of exploiting this method. By using this novel investigation method wisely, the testing costs can be reduced and some originally unmeasurable quantities can be acquired.

### 5.2. Important assumptions used in previous sections

Despite the difficulties in analyzing the integrated test chips of the $S_{21}$ detection circuit, the valuable information has been acquired from the previous sections through different techniques. During the analysis processes, some useful assumptions, which also added imprecision, were used to simplify the problems. Hence, although the analysis results are logical and self-consistent, they contain elements of imprecision. Fortunately, the imprecision does not harm the usefulness of the analysis. To better explain the addition of imprecision, two important assumptions are discussed as follows.

The first assumption concerned the circuit simplification performed by the novel investigation method proposed in Section 2. During the simplification, the capacitors and inductors were assumed to be open circuits and simple conducting paths, and the S-parameters were deprived of their phases before being transformed into the corresponding Z-parameters. Because the above operations are absolutely correct only at DC, performing them at 50 MHz unavoidably creates imprecision.

The second assumption lied in the derivation of the model of process variations presented in Section 4. If the model were to be derived in a rigorous way, it would require much information, such as the dimensions of the layout and the detailed fabrication parameters of the IBM 7RF technology. Furthermore, it may even require the electromagnetic software (e.g., HFSS) to provide assistant verification. However, such a rigorous way is time-consuming and much of the required information is unavailable. To circumvent the difficulties, it was assumed that the phase lag caused by a conducting path is proportional to the resistance of that path. Although the assumption may not differentiate subtleties to the extreme, it provides a feasible solution to estimating the potential formation of process variations.

### 5.3. The model of process variations versus the chip layout

In Section 4, the model of process variations was proposed for the additional path between Ports 1 and 3. The core of the model is the novel investigation method that exploits the low-frequency measurement, as demonstrated in Section 2. Despite the adjustment in the sources of the extra resistance, the novel investigation method succeeded in discovering the additional resistance, which laid the foundation for the hybrid model. The greatest advantage of the method is its ability of examining the most important parameter at low frequencies, which requires less costs than the high-frequency measurement. Hence, the novel investigation method serves as a perfect solution to the production testing of the $S_{21}$ detection circuit.

In theory, the discovered additional resistance should reduce the magnitude of $S_{21\_DUT2\_MEASURED}$ by reducing the magnitude of $S_{31\_SYS}$ in Eq. (1) around the targeted operational frequency. However, because $1.96\Omega$ is too small to manifest the reduction in the presence of other influencing factors, the magnitude of $S_{21\_DUT2\_MEASURED}$ is slightly larger than that of $S_{21\_DUT2\_DERIVED}$. In spite of the interference from other factors, the error percentage in the magnitude of $S_{21\_DUT2\_MEASURED}$ (2.27%) is much smaller than that in the phase of $S_{21\_DUT2\_MEASURED}$ (20.74%). This shows that the signal attenuation caused by $1.96\Omega$ is small and that the influence of the process variations in the Port1-to-Port2 and Port1-to-Port3 paths is greatly alleviated by the division in Eq. (1).

The model in Section 4 demonstrated that the process variations in the DUT2 and those in the interface paths cause 55.8% and 44.2% of the extra resistance, respectively. Contributing 55.8% of the extra resistance, the process variations in the DUT2 would be the first target to be reduced. However, because the DUT2 does not concern the fundamental functionalities of the $S_{21}$ detection circuit, the process variations within it are not the focus of attention. On the other hand, the process variations inside the interface paths possess great significance and thus should be carefully discussed. According to the model, the additional length of the interface paths measures about 63μm and lies near Ports 1 and 2 of the DUT2. Fig. 10 illustrates the die micrograph of the $S_{21}$ detection circuit with the dotted red rectangle marking the locations of the interface paths. As can be noted, the length of the two paths measures approximately 74.6μm, which is close to the derived length, 63μm. The high proximity between 74.6μm and 63μm reconfirms the efficacy of the analyses in the previous sections. Furthermore, it reveals

one important fact that except for the DUT2, the lengths of the Port1-to-Port2 and Port1-to-Port3 paths should be made as identical as possible. If the lengths are not identical, a dummy path is recommended to be added to the shorter path to compensate for the difference. Take Fig. 10 for an example, an additional segment of conducting path should be inserted into the Port1-to-Port2 path. Such a dummy path can effectively diminish the difference in path lengths and enhance the overall measurement precision.
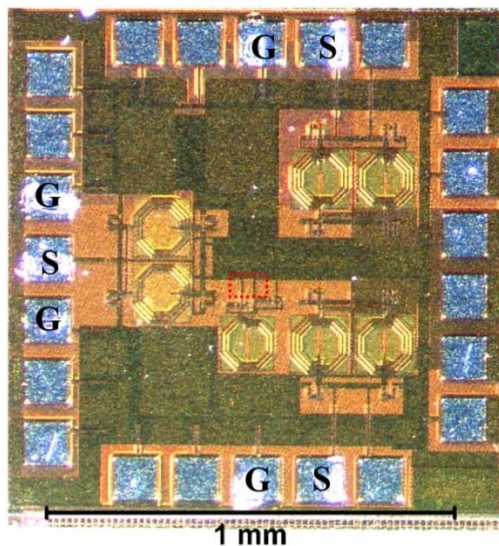


Fig. 10 Die micrograph of the $S_{21}$ detection circuit

At 11.05 GHz, the error percentage of the phase of $S_{21\_DUT2\_MEASURED}$ (20.74%) is much greater than that of the magnitude of $S_{21\_DUT2\_MEASURED}$ (2.27%). The large difference in the error percentages indicates that the phase measurement of the $S_{21}$ detection circuit is more vulnerable to process variations than the magnitude measurement. For the 20.74% error in the phase, 91.2% of it came from the DUT2 and 8.8% originated from the interface paths. Again, the process variations in the DUT2 is not the concern of this research. On the other hand, the effects of the process variations in the interface paths are likely to be counteracted by adding a dummy path. If the effects of the process variations in the interface paths can be fully nullified, the error in the phase of $S_{21\_DUT2\_MEASURED}$ will be optimally reduced by 8.8%, causing a change from 20.74% to 18.91%.

### 5.4. Recommendations for research in the future

Based on the previous discussions, four important observations are made and their corresponding recommendations are proposed to improve the measurement precision of the $S_{21}$ detection circuit in the future. First, the process variations in the test chips deteriorate the phase measurement more significantly than the magnitude measurement. This can be known by comparing the error of 20.74% in the measured phase with that of 2.27% in the measured magnitude. Another aspect of investigation can also be performed by removing the error caused by the DUT2, which is not the focus of this research. Of the 20.74% error in the phase, the process variations in the DUT2 and those in the interface paths contribute 18.91% and 1.83%, respectively. Of the 2.27% error in the magnitude, the process variations in the DUT2 and those in the interface paths contribute 1.27% and 1%, respectively. Hence, the error in the phase is still 1.83 times that in the magnitude when excluding the error caused by the DUT2. In light of the first observation, it is recommended that circuit designers pay more attention to minimize the error in the phase measurement when using the $S_{21}$ detection circuit.

Second, the layout symmetry between the Port1-to-Port2 and Port1-to-Port3 paths helps reduce the effects of process variations through the cancellation between the numerator and denominator in Eq. (1). This can be proved by comparing Fig. 2 with Fig. 9. At 11.05 GHz, Fig. 9 illustrates that the measured $S_{21}$ and $S_{31}$ lag the simulated $S_{21}$ and $S_{31}$ by 81.37 degrees and 101.94 degrees in the face, respectively. The significant phase lag between the simulation and measurement signifies that considerable process variations do exist in the test chips. However, thanks to the high symmetry between the Port1-to-Port2

and Port1-to-Port3 paths, as illustrated in Fig. 10, the phase lag of $S_{21\_DUT2\_MEASURED}$ with respect to $S_{21\_DUT2\_DERIVED}$ is reduced to 20.57 degrees, as illustrated in Fig. 2. The substantial reduction in the error demonstrates that the symmetrical layout between the two paths can greatly mitigate the effects of process variations. The advantage of symmetry can also be proved by comparing the errors caused by the two main sources of process variations. Recall that the process variations in the DUT2 cause a measurement error of 18.91% and 1.27% in the phase and magnitude, respectively. On the other hand, the process variations in the interface paths contribute an error of 1.83% and 1% in the phase and magnitude. With 1.83% and 1% being smaller than 18.91% and 1.27%, it is obvious that the layout symmetry between the two paths can help reduce the measurement errors caused by process variations. To take full advantage of this observation, circuit designers are encouraged to keep the layout of the two paths, except for the DUT2, as identical as possible. The strategy of inserting dummy paths presented before can be useful for attaining this goal.

Third, because the DUT2 exists only on the Port1-to-Port3 path, the effects of process variations in it do not enjoy the benefit of being cancelled through Eq. (1). Hence, the process variations of the DUT2 tend to dominate the error percentage in $S_{21\_DUT2\_MEASURED}$. In light of the unmitigated measurement error caused by the DUT2, it is recommended that a stand-alone DUT2 be fabricated in the future if the die size allows. When the regional difference in process variations is small, the performance of the stand-alone DUT2 should be close to that of the DUT2 embedded in the $S_{21}$ detection circuit. Under such circumstances, the directly measurable DUT2 can provide the useful information about the process variations within itself and help reconfirm other inferences.

Finally, the measurement results in [11] and the investigation results of this research all revealed that process variations did occur during the fabrication of the test chips. Hence, specific calibration procedures for the $S_{21}$ detection circuit will be studied in the future to further enhance the measurement precision. Circuit designers are encouraged to adopt those procedures when they aim to perform a high-precision measurement.

## 6. Conclusions

In this work, the novel investigation method was proposed to examine the performance of the $S_{21}$ detection circuit. The method was demonstrated by analyzing the S-parameters at 50 MHz and corroborated by analyzing the S-parameters at 11.05 GHz. By using the method, the $S_{21}$ detection circuit can be efficiently investigated at a low frequency or DC. Although the method was originally designed for the $S_{21}$ detection circuit, it is applicable to any circuit operating differentially either to reduce the testing costs or to measure some originally unmeasurable quantities. What is better, the accuracy of the novel investigation method will be enhanced when the analysis frequency is reduced. This poses an especially favorable condition for the method because it will become more accurate at lower testing costs.

Furthermore, by integrating the investigation results at the two frequencies, the model of process variations was constructed. Being consistent with the chip layout, the model reconfirmed the novel investigation method and revealed several important findings. Based on these findings, valuable recommendations were proposed to help ameliorate the measurement precision of the $S_{21}$ detection circuit in the future.

## Acknowledgement

## Conflicts of Interest

The author declares no conflict of interest.

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