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# A transformerless three-level three-phase boost PWM inverter for PV applications

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**Abstract**

Multilevel converters have seen rising demands in the past decades, due to their increased power ratings, enhanced power quality, low switching losses and reduced electromagnetic interference. Prominent among them are the three-level (3L) neutral point clamped and the flying capacitor inverter topologies along with their derivatives. Nevertheless, the main drawback of these topologies is the requirement of a front-end boost DC–DC converter to compensate the high dc-link voltage demand, which is usually twice the grid peak voltage. This multi-stage power conversion further pulls down the overall system efficiency. A single-stage dc–ac power converter with boost capability offer an interesting alternative compared to the two stage approach. Considering this aspect, a novel three-level three-phase boost type inverter is introduced in this paper for general-purpose applications (prominently grid-connected renewable energy). The proposed inverter would reduce the DC-link voltage requirement to half using the same or even less number of active and passive components, compared to the conventional three-level neutral point clamped and flying capacitor family. The principle of operation and theoretical analysis are discussed in detail. The design methodology along with simulation and experimental waveforms for a 5 kVA inverter are presented to prove the concept of the proposed inverter topology for practical applications.

## 1 | INTRODUCTION

Since the outset of photovoltaic (PV) systems in the mid 70's, intensive research in terms of technological (power electronics and semiconductors) as well as economical (energy efficient) aspects has witnessed remarkable developments. A tremendous growth in the solar PV capacity installations was recorded in 2019, marking a total global capacity of at least 600 GW [1]. Figure 1, reveals the actual statistics of PV system implementation until 2019 [2].

Concurrent impact was bestowed upon inverter development to accommodate the germinating market. Under this, providing a breakthrough for the conventional converter design was the concept of multilevel inverters (MLI) that evolved in the late 1970's. Multilevel inverters seized the technological attention and has seen increasing demands in the last decades because of their enhanced output waveforms, low switching losses and reduced EMI.

Three level voltage source inverters (VSIs) illustrate certain interesting advantages compared to two-level VSIs especially in terms of higher voltage power conversion, where lower voltage stress on the switches and lower harmonic content exist [3–5]. Two-level VSIs are often used under low switching frequencies where they are comparatively more efficient. Higher switching frequencies are more desirable in order to achieve low rated passive components like inductors, which may result in the reduction of overall weight and cost. Also, multi-level topologies permit replacement of the high voltage switches in two-level inverters by low voltage switches, which are normally small and cheap with high switching frequency handling capability. In addition, the conduction and switching losses (small $dv/dt$) can be reduced due to a low forward-voltage drop.

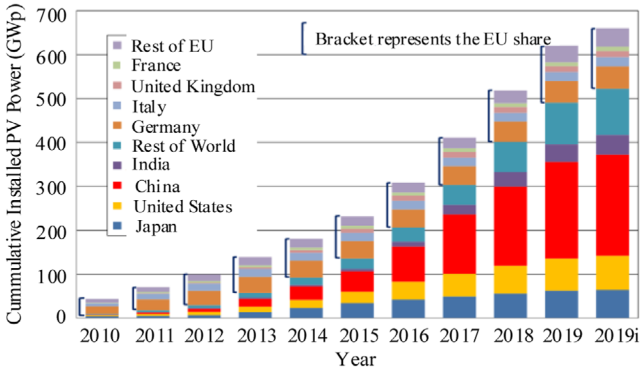


**FIGURE 1** Global cumulative PV installations from 2010–19 [2]

Conventional two-level topologies need to be switched at higher frequency to meet the same output quality of three-level topologies. Thus, a reduced switching frequency can be implemented in MLIs. Numerous three-level inverter topologies have been proclaimed in the literature since 1970's [3] followed by several derivatives [6–9] with distinct features, as shown in Figure 2. With increasing voltage levels a better approximation to a sinusoidal waveform can be achieved with the reduction in passive filter components, also lower total harmonic distortion (THD) and improved power quality.

Besides the reported advantages, a challenging factor in multilevel inverters is their structural complexity and control technique as the number of levels increase. Further, the 3L-Neutral Point Clamped (NPC) inverter topology poses high DC-link voltage requirement (twice the amplitude of grid voltage), which either needs an additional front-end boost DC–DC converter or string of series connected PV modules to raise the DC-link voltage for grid integration.

For instance, in the European grid to switch between the positive and negative waveform for an output of 230 $V_{\mathrm{rms}}$, at least twice the peak output is required at the DC input. This corresponds to an input voltage of 650 $V_{\mathrm{DC}}$ in a VSI, which might be even higher in real-time applications. It reduces the efficiency and reliability, whilst increasing the size and cost of the system. The additional boost stage can be eliminated by series connected PV modules, whereas the losses due to mismatch between the modules and shading relatively reduces the energy gain of the system.

Considering the above aspects in the development of a three-level inverter, a novel three-level three-phase boost type inverter is proposed in this paper (an extension of the single phase prototype proposed in [10]).

The proposed topology offers an interesting alternative to the conventional two-stage power conversion with a single-stage dc–ac power converter accompanied by an in-built boost capability. This reduces the number of active and passive components as well as their voltage stress, control complexity and the required DC-link voltage significantly, impacting in the cutback of the cost and size of the system. Overall, the efficiency and reliability of the system will be improved. Figure 3 illustrates the conventional two-stage converter (DC–DC and dc–ac) system and single-stage (dc–ac) system with the proposed three-level three-phase multilevel topology.

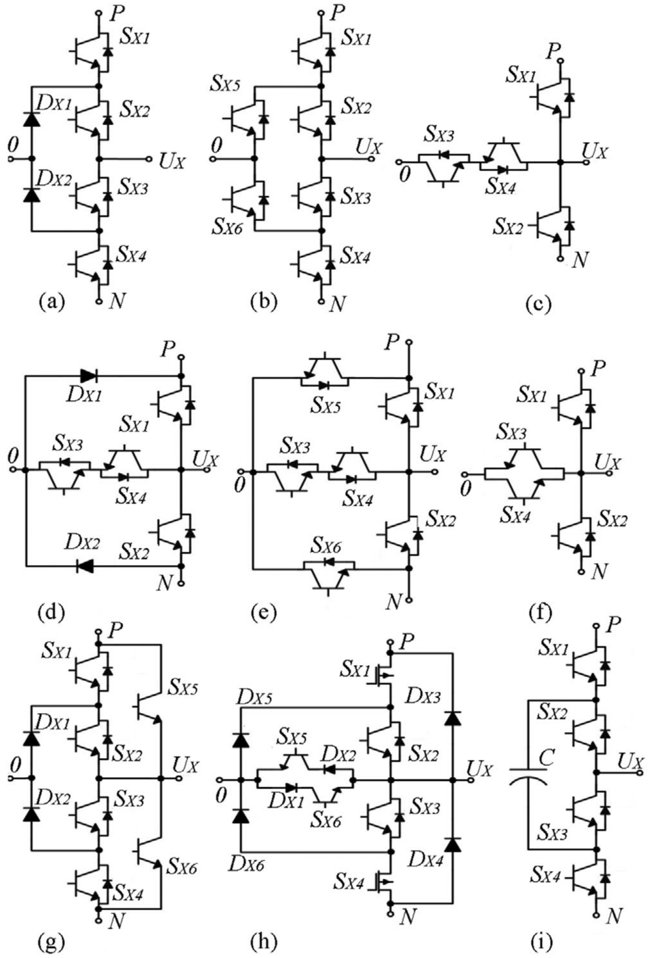

**FIGURE 2** Phase leg of conventional three-level three-phase inverter topologies, a 3L-neutral-point clamped [3], b 3L-active-neutral-point clamped [7], c 3L-conergy neutral-point clamped [5], d 3L-stacked-neutral-point clamped [9], e 3L-stacked-active-neutral-point clamped [9], f 3L-neutral-point clamped T-type [8], g 3L-H-neutral-point clamped [7], h N-3L-stacked-neutral-point clamped [9], i 3L-flying capacitor (FC) [4].

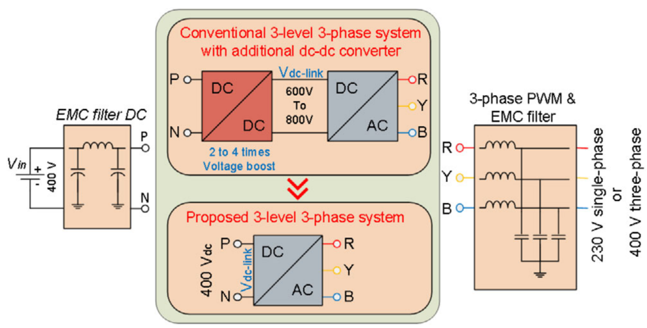


**FIGURE 3** Illustration of the conventional two-stage converter (DC–DC and dc–ac) system and single-stage (dc–ac) system with proposed multilevel topology

## 2 | PROPOSED INVERTER TOPOLOGY

The proposed topology is a common-ground type transformerless inverter based on the principle of flying capacitor, with four active switching elements [10]. The uniqueness of this topology underlies in the fact that the negative voltage bus required

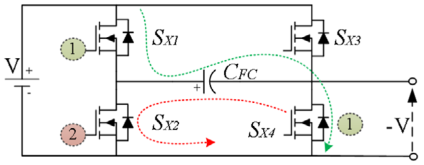


**FIGURE 4** Principle illustrating the charging (green dotted-line) and discharging (red dotted-line) of the capacitor $C_{FC}$ to create the negative voltage bus

during the negative fundamental cycle is fulfilled through a single polarised input supply. This is achieved by the cyclic charging and discharging of the flying capacitor thus creating a virtual negative bus. Since the neutral of the grid is directly connected to the negative pole of the DC-bus, the leakage current is automatically eliminated.

## 2.1 | Principle of operation

When the switches at position-1 (see Figure 4) are in high state, the flying capacitor ($C_{FC}$) gets connected to the input supply and charges upto the input voltage (400 V). Subsequently, as the switch in position-2 turns high, the flying capacitor tends to discharge and hence a negative voltage equal to the magnitude of input voltage is observed at the output. Repeated operation of the above sequence is ensured at high switching frequency to maintain a constant voltage across the load. The phase leg of the proposed three-level three-phase inverter including four power switches and one capacitor, is shown in Figure 4.

While integrating into an inverter circuit (see Figure 6), the contact points across position-1 are replaced by MOSFET-diode series combination (or RB-IGBTs) for switches $S_{X1}$ and $S_{X4}$ considering their bipolar voltage blocking requirement. Likewise, the circuit across position-2 is fulfilled with MOSFETs in place of switches $S_{X2}$ and $S_{X3}$, establishing a unipolar voltage withstanding capability. Switches $S_{X1}$ and $S_{X4}$ charges the flying capacitor, whilst switch $S_{X2}$ discharges it thereby creating the negative cycle. The positive cycle is delivered by switch $S_{X3}$.

## 2.2 | Control and modulation strategy

The inverter modulation is handled using a standard unipolar sinusoidal pulse width modulation (SPWM), as shown in Figure 5. Here, switch $S_{X3}$ is modulated in reference to the positive sinusoidal to generate the positive grid cycle and switch $S_{X2}$ is modulated with negative sinusoidal reference to create the negative half of the grid cycle. Hence, only one switch carries the load current during the positive as well as the negative cycle. The switches $S_{X1}$ and $S_{X4}$ are modulated with a homogeneous gate signal in both the positive and negative half cycle but complementary to the primary sinusoidal reference. The charging of the flying capacitor is achieved through switch $S_{X1}$ as the switch $S_{X4}$ turns ON, thus creating a zero state during both the

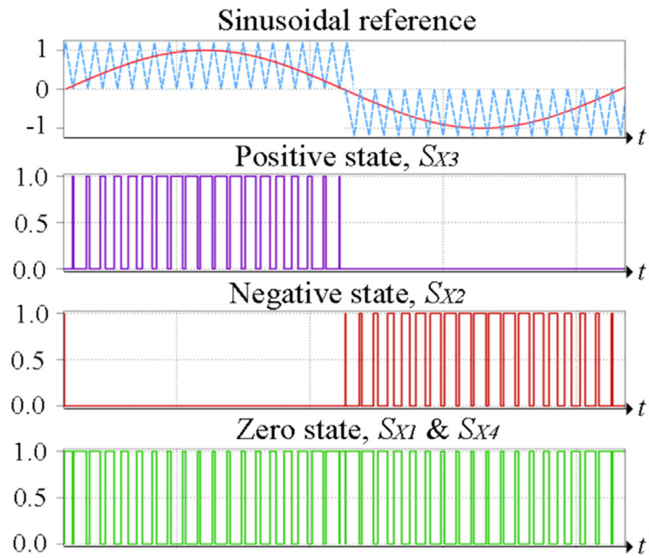


**FIGURE 5** Unipolar SPWM modulation strategy for the switches

positive and negative cycle. These two switches experience high frequency switching during both the positive and negative cycle.

## 2.3 | Modes of operation

To satisfy the power conversion process, three modes of operation have been derived for this topology. The switching sequence for a single phase construction is shown in Table 1.

### 2.3.1 | Positive state

The positive modulating signal is subjected for comparison to a reference triangular waveform in order to generate the required pulse for switch $S_{X3}$. This creates a unipolar positive voltage at the filter. Switches $S_{X1}$ and $S_{X4}$ are OFF during this state, while $S_{X2}$ remains OFF for the complete positive cycle.

### 2.3.2 | Zero state

Following every positive and negative state, the zero state is created by turning ON switch $S_{X4}$ along with switch $S_{X1}$, thus charging the flying capacitor through $S_{X1}$ and $S_{X4}$ (see Figure 7). This ensures the capacitor charging in every switching

**TABLE 1** Switching states of the power switches

| States | $S_{X1}$ | $S_{X2}$ | $S_{X3}$ | $S_{X4}$ |
|---|---|---|---|---|
| Positive state | 0 | 0 | 1 | 0 |
| Zero state | 1 | 0 | 0 | 1 |
| Negative state | 0 | 1 | 0 | 0 |

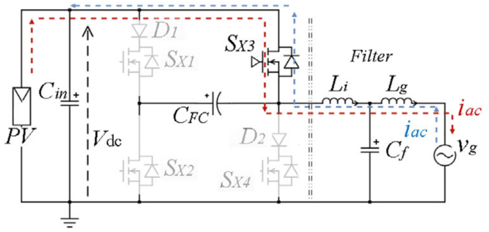

**FIGURE 6** Positive state operation of the proposed topology, red-dotted lines indicate the active current path and the blue dotted lines depict the reactive current path

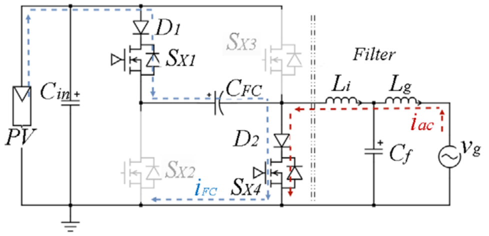

**FIGURE 7** Zero state operation of the proposed topology, blue-dotted lines represents flying capacitor charging current path and the red-dotted lines indicate the active current path

cycle regardless of the power cycle polarity. High frequency switching helps to reduce the size of the capacitor.

### 2.3.3 | Negative state

The negative modulating signal is correlated with the reference triangular waveform to generate the required pulse for switch $S_{X2}$. The charged flying capacitor acts as a negative DC-bus, thus creating unipolar negative voltage at the filter (see Figure 8). Switches $S_{X1}$ and $S_{X4}$ are OFF during this state, while $S_{X3}$ remains OFF for the complete negative cycle.

The sequential repetition of the operating modes during each power cycle creates a unipolar positive and negative voltages at the filter. This unipolar chopped voltage is then filtered out to supply pure sinusoidal voltage and current at the load. The existence of unipolar voltage switching helps to retain its own advantages such as small filter demand, reduced switching losses, low EMI and low ripple current at the output.

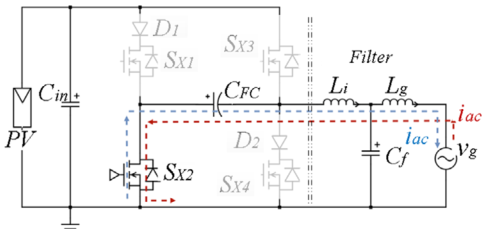

**FIGURE 8** Negative state operation of the proposed topology, red-dotted lines indicate the active current path and the blue dotted lines depict the reactive current path

## 3 | THREE-LEVEL THREE-PHASE BOOST CONVERTER CONFIGURATION

Conventional multilevel converter require two times the peak of AC output voltage, which needs an additional front-end boost DC–DC converter or string of series-connected PV modules to lift the DC-link voltage up to 800 V for active power control to the grid. This means the input DC voltage utilisation factor of the conventional multilevel inverter is ≤50%, compared to the proposed three-level three-phase inverter, where the DC-link voltage utilisation is up to 100%. Figure 9(a) shows the schematic of the proposed three-level three-phase boost converter configuration with four power switches and one capacitor per phase. The converter has similar semiconductor requirement and voltage stress as of conventional T-type NPC topology, as shown in Figure 9(b) [5]. The phase voltage and 3L-line voltage of the inverter clearly demonstrate the improvement of input DC-link voltage utilisation to 100 %.

A comparative summary of the key features of the proposed three-level three-phase converter with the conventional 3L topologies is presented in Table 2. The parameters and number of components are included for a phase leg only. The total semiconductor count includes all diodes (antiparallel and/or series), MOSFET and IGBT in the topology. For example, the total semiconductor count in the proposed topology is 8, which includes 2 RB-IGBT (2 IGBT + 2 body diodes) + 2 MOSFET (2 MOSFET + 2 antiparallel diodes). It is evident from

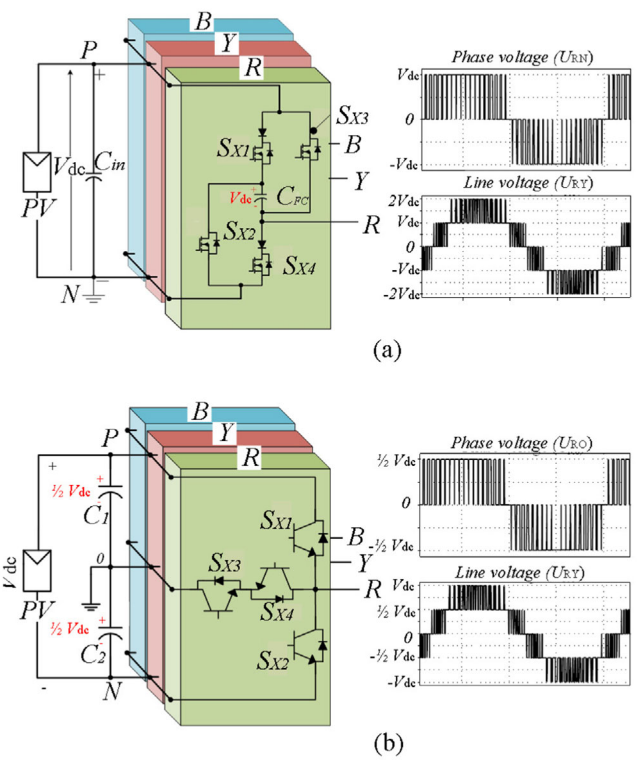

**FIGURE 9** Illustration of input DC-link voltage utilisation in, a proposed 3L-H-bridge-boost inverter, where the DC-bus voltage utilisation is ≤ 100%, b conventional 3L T-type inverter, where the DC-bus voltage utilisation is ≤ 50%

**TABLE 2** Comparative summary of the proposed topology with the conventional three-level topologies (per phase)

| Parameter | Proposed 3L-boost inverter | 3L-NPC [3] | 3L-ANPC [7] | 3L-Conergy NPC [5] | 3L-SNPC [9] | 3L-ASNPC [9] | 3L-NPC T-type [8] | 3L-H-NPC [7] | N-3L-SNPC [9] | 3L-Flying Capacitor (FC) [4] |
|---|---|---|---|---|---|---|---|---|---|---|
| No. of semiconductor | 8 | 10 | 12 | 8 | 10 | 12 | 8 | 12 | 14 | 8 |
| No. of capacitors | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 3 |
| DC-link voltage required for the same output voltage | $V_{DC}$ | 2 $V_{DC}$ | 2 $V_{DC}$ | 2 $V_{DC}$ | 2 $V_{DC}$ | 2 $V_{DC}$ | 2 $V_{DC}$ | 2 $V_{DC}$ | 2 $V_{DC}$ | 2 $V_{DC}$ |
| Maximum voltage stress on the semiconductor | 2 $V_{DC}$ | $V_{DC}$ | $V_{DC}$ | 2 $V_{DC}$ | $V_{DC}$ | 2 $V_{DC}$ | $V_{DC}$ | 2 $V_{DC}$ | 2 $V_{DC}$ | $V_{DC}$ |

the table that the proposed topology requires a minimal number of active and passive components. This effectively reduces the $R_{DS,on}$ and losses in the system. In addition to the reduction in number of semiconductor devices, the reduction in the DC-link voltage requirement by two-fold is the notable contribution compared to the traditional three-level NPC, ANPC and FC inverter family. This will have huge impacts on the system design, cost, efficiency, reliability and power density.

## 4 | CONVERTER DIMENSIONING

The operating parameters for the desired three-level three-phase inverter are listed in Table 3. The design approach focusing on the primary converter elements for a 5 kW grid connected inverter is systematically presented in the following subsections.

**TABLE 3** Inverter operating parameters and component ratings

| Parameter | Variable | Value |
|---|---|---|
| Grid voltage | $U_n$ | 230 $V_{AC}$ |
| Rated power (three-phase) | $P_n$ | 5 kW |
| DC link voltage | $V_{DC}$ | 400 V |
| Grid frequency | $f_n$ | 50 Hz |
| Switching frequency | $f_{sw}$ | 40 kHz |
| DC-link capacitor | $C_{in}$ | 300 $\mu$F, 600 V |
| Flying capacitor (per phase) | $C_{FC1}$ | 360 $\mu$F, 600 V |
| Flying capacitor (per phase) | $C_{FC2}$ | 120 $\mu$F, 600 V |
| Filter inductor | $L_i$ | 400 $\mu$H |
| Filter capacitor | $C_f$ | 5 $\mu$F |
| Grid inductor | $L_g$ | 56 $\mu$H |
| Switches | $S_{X1}, S_{X4}$ | C2M0040120D |
| Switches | $S_{X2}, S_{X3}$ | C2M0080120D |
| Diodes | $D_1, D_2$ | C4D40120D |
| Load | $R_L$ | 32 Ω |

### 4.1 | DC link capacitor ($C_{in}$)

The DC link capacitor is introduced as a decoupling element, to ensure minimal voltage ripple at the input and thus limiting any disturbance generated from the source (PV) to load and vice-versa. This would help to sustain a pure DC voltage in the case of more components being connected to the grid. In addition, it acts as a low-impedance path for the ripple current generated by the power switching circuits. It also plays a major role in mitigating the parasitic inductance of the converter power bridge, which might cause inefficiency due to the voltage spikes generated at high frequency switching. The equivalent input capacitance of the circuit is estimated in Equation (1), considering the permissible voltage ripple across the DC-link ($V_{in}$) and the critical case of the minimum duty cycle.

$$C_{in} = \frac{I_{ac,max} \cdot D_{min}}{\Delta V_{in} \cdot f_{sw}} \tag{1}$$

Here $I_{AC,max}$ is the maximum amplitude of the grid current [11], $D_{min}$ is the minimum duty cycle of the switch in the current path, $\Delta V_{in}$ is the desired permissible voltage ripple and $f_{sw}$ is the PWM frequency. Considering the system parameters, for a voltage ripple of 2 V and minimum duty cycle of 0.8, the DC-link capacitance is rated at 300 μF [12].

### 4.2 | Flying capacitor ($C_{FC}$)

The flying capacitor plays a major role in the operation of this converter topology. It would have a direct impact on the performance of the converter by influencing the current stress on the switches $S_{X1}$ and $S_{X4}$ (in $C_{FC}$ charging path). For determining an intact operating zone of the converter, a new element $\delta$ is introduced as a direct relationship between the size of the flying capacitor and the DC-link capacitor.

$$\delta = \left(\frac{C_{FC}}{C_{in}}\right) \tag{2}$$

Ensuring the current stress on the power switches within limits (5), the range of $\delta$ is determined between 2 and 6 ($2 \le \delta \le 6$). Too less the value of $\delta$ would increase the voltage ripple across the flying capacitor. Estimating the value of $\delta$ as 6, the flying capacitor is rated at 600 $\mu$F per phase. Also, the current rating of the capacitor has to be taken into consideration while selecting, to support the demand from the load.

## 4.3 | Power switches ($S_{X1}$, $S_{X2}$, $S_{X3}$, $S_{X4}$)

From the operating principle it can be inferred that the voltage stress on the switches $S_{X2}$ and $S_{X3}$ would be twice the input voltage (i.e. 800 V). Concurrently, the voltage stresses on the switches $S_{X1}$ and $S_{X4}$ are equal to the input voltage (i.e. 400 V $- V_{DC}$). The switches $S_{X3}$ and $S_{X2}$ completing the positive and negative cycle respectively, experience a current stress equal to that of the peak load current, (i.e. ≈10.16 A). On the other hand, switches $S_{X1}$ and $S_{X4}$ are burdened by both the capacitor charging current as well as the load current. This charging current is dependent on the duty cycle $d(t)$ of the referred switches in the current path, load current $i_{AC}$ and the capacitance ratio $\delta$ of the DC-link and flying capacitor.

$$d(t) = D_{\max} \cdot sin(\omega.t) \tag{3}$$

$$i_{AC}(t) = I_{ac,\max} \cdot sin(\omega.t) \tag{4}$$

Considering the approach presented in [13] the maximum value of the charging current is evaluated using (5), where $D_{\max}$ is the maximum duty cycle of the switch in the current path. It is directly proportional to $D_{\max}$ and inversely proportional to the rating of the flying capacitor. However, small $D_{\max}$ ($\le 0.8$) reduces the DC-link voltage utilisation factor and large $C_{FC}$ ($> 6$) increases the cost and size of the flying capacitor.

$$i_{FC\max,X1} = \frac{0.5 \cdot D_{\max}}{1 - D_{\max}} \cdot \frac{2 + \delta}{1 + \delta} \cdot I_{AC,\max} \tag{5}$$

With an appropriately chosen $D_{\max}$ ($0.8 \le D_{\max} \le 0.95$) and $\delta$ (from 2) the current stress on the relevant switches in the charging current path is estimated between 2 $I_{AC,\max}$ to 5 $I_{AC,\max}$. For the current design, $D_{\max}$ is considered as 0.85.

**TABLE 4** Voltage and current stress distribution on power switches

| Switches | Voltage stress | Current stress |
|---|---|---|
| $S_{X1}$ | $\pm V_{DC}$ | $\approx \frac{0.5 \cdot D_{\max}}{1-D_{\max}} \cdot \frac{2+\delta}{1+\delta} \cdot I_{AC,\max}$ |
| $S_{X2}$ | $+ 2V_{DC}$ | $\approx I_{AC,\max}$ |
| $S_{X3}$ | $+ 2V_{DC}$ | $\approx I_{AC,\max}$ |
| $S_{X4}$ | $\pm V_{DC}$ | $\approx [\frac{0.5 \cdot D_{\max}}{1-D_{\max}} \cdot \frac{2+\delta}{1+\delta} + 1] \cdot I_{AC,\max}$ |

## 4.4 | Output filter ($L_i$, $C_f$, $L_g$)

Among the prevalent filter topologies [14], a LCL filter configuration (see Figure 10) provides a better decoupling between filter and grid impedance with an attenuation of 60 dB/decade. It has a better current ripple attenuation with lower inductance values [15]. Further, its small dependence on the grid parameters is of major importance at high power applications, in order to guarantee a stable power quality level.

The transfer function of the LCL filter is given as [16],

$$\Rightarrow H = \frac{sC_f + 1}{s^3 L_g L_i + s^2 C_f (L_g + L_i) + s(L_g + L_i)} \tag{6}$$

While dimensioning, the filter values are referred as percentage of the base impedance ($Z_b$) and base capacitance ($C_b$) values (7).

$$Z_b = \frac{U_n^2}{P_n} \quad \text{and} \quad C_b = \frac{1}{\omega_n \cdot Z_b} \tag{7}$$

The main inductor ($L_i$) is dimensioned at 50% of duty cycle, when the current ripple of the converter is at the highest [14].

$$L_i = \frac{V_{DC}}{4 \cdot \Delta I_{\max} \cdot f_{sw}} \tag{8}$$

$$\Delta I_{\max} = 0.3 \cdot \left( \frac{P_n \cdot \sqrt{2}}{U_n} \right) \cdot 2 \tag{9}$$

Here $\Delta I_{\max}$ is the maximum peak-to-peak ripple current, which is limited to 30% of the rated current. The filter capacitor ($C_f$) is designed as a factor of the base capacitance considering the power factor variation (max.) to the grid as being 5%.

$$C_f = 0.05 \cdot C_b \tag{10}$$

For dimensioning of the grid inductor ($L_g$), a ripple attenuation factor is inferred. It is given as a ratio between the filter impedance and the difference between resonant and switching frequency [16],

$$\frac{i_g(h_{sw})}{i(h_{sw})} = \frac{1}{|1 + r(1 - (L \cdot C_b \cdot \omega_{SW}^2)\, x)|} \tag{11}$$

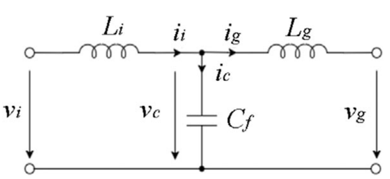


**FIGURE 10** LCL filter electrical circuit—single phase

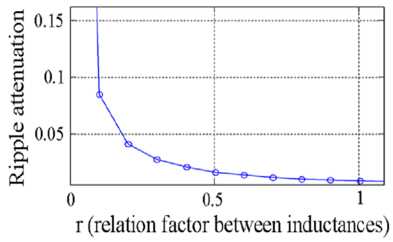


**FIGURE 11** Ripple attenuation as a function of the relation factor between the inductance at the inverter side and grid side

here $r$ is the desired ripple current attenuation, obtained from Figure 11. Choosing a ripple attenuation of 10% on the grid side with respect to the current ripple on the inverter side, the grid inductor is given as

$$L_g = r_i \cdot L_i \tag{12}$$

$$10 \cdot f_n < f_{res}\left(= \frac{1}{2\pi}\sqrt{\frac{L_i + L_g}{L_i \cdot L_g \cdot C_f}}\right) < \frac{f_{sw}}{2} \tag{13}$$

The resonant frequency ($f_{res}$) is ensured to be limited in the order of ten times higher than the grid frequency and half of the switching frequency, allowing the filter with sufficient attenuation under the converter's switching frequency.

### 4.5 | Heatsink

The lifetime of all semiconductor devices is inversely proportional to their operating temperature [17]. For reliable operation and long component life, it is vital to ensure adequate removal of heat from the device. Figure 12 shows the heat transfer path for a semiconductor device.

The junction temperature ($T_j$) [18] as a compound of different temperature zones is estimated as in Equation (14),

$$T_j = \Delta T_{jc} + \Delta T_{ch} + \Delta T_{ha} + T_a \tag{14}$$

where $\Delta T_{jc}$ is the junction and case temperature difference, $\Delta T_{ch}$ is the temperature difference between case and heatsink and $T_a$

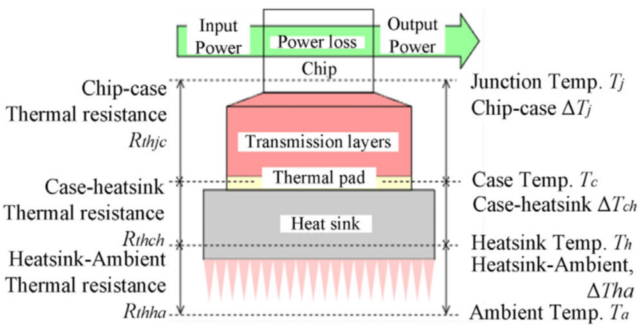


**FIGURE 12** Heatflow model of a power MOSFET on a heat sink

is the ambient temperature. Thermal resistance ($R_{th,ja}$) of the heatsink is evaluated as

$$R_{th,ja} = \frac{T_j - T_a}{P_d} + R_{th,ch} + R_{th,ha} \tag{15}$$

$$T_{jn} = T_a + P_{dt} \cdot R_{ja} \tag{16}$$

The power dissipated by the power switches are estimated in (16), where $R_{ja}$ is the thermal resistance from junction to the ambient and $T_{jn}$ is the estimated temperature of the individual devices [19]. The thermal resistance of the heatsink in the current design is estimated to be 0.9 K/W.

## 5 | SIMULATION AND EXPERIMENTAL RESULTS

To verify the concept of the proposed three-level three-phase inverter and the design approach, PLECS simulations were carried out followed by hardware measurement on a 5 kW prototype. Figure 13 shows the prototype of a three-phase system.

The voltage ripple across DC-link capacitor is comparable to the considered 2 V ripple limit. This shows a clean input DC supply to the converter. The $\delta$ factor ascertained as a trade-off between the capacitor size and current stress on the switches, is yielding a voltage ripple of 46 V.

The continuous current drawn by the inverter in a three-phase setup, substantiates the topology better for PV sources. It is also evident that all proposed three flying capacitors are uniformly charged to a magnitude equal to the input voltage, as shown in Figure 14. It was observed that the flying capacitor voltage ripple is directly proportional to the change in the power of load, with a maximum ripple of 46 V whereas, during power factor variations the voltage ripple stays constant with a minimal ripple of around 3 V. The SiC MOSFETs $S_{X1}$ and $S_{X4}$ (CREE-C2M0040120D) completing the flying capacitor charging path encounters the highest current stress at around 30 and 42 A (see Figure 16), whereas the switches in the positive and negative cycle confronts a current stress (see Figure 15) of 12 A due to the load, as estimated in Section 4.3.

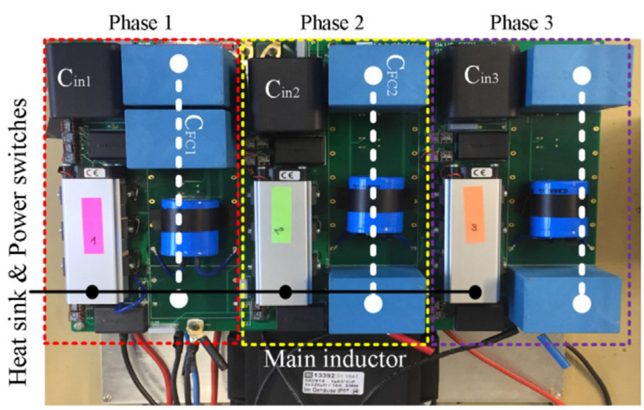


**FIGURE 13** Top view of PCB holding the primary elements

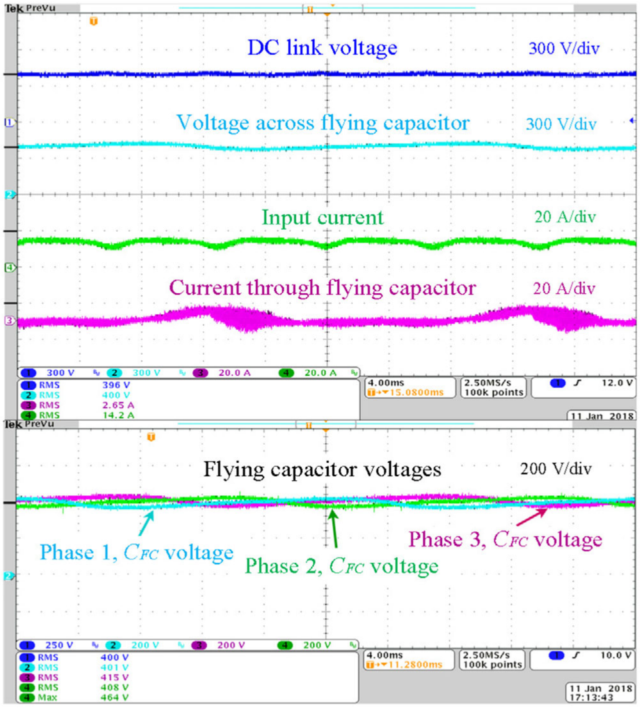


FIGURE 14 Measured waveforms of input voltage and current as well as flying capacitor voltages

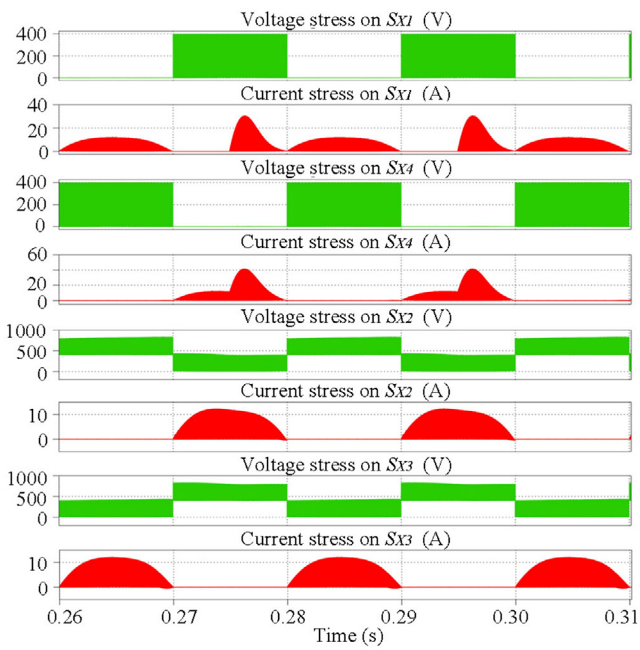


FIGURE 15 Simulated voltage and current stress on the MOSFETs in phase-1

The voltage stress on switches $S_{X1}$ and $S_{X4}$ in the flying capacitor charging path is measured as 400 $V$, while the maximum voltage stress on switches $S_{X2}$ and $S_{X3}$ (CREE-C2M0080120D) was at 800 $V$. A steady state heat dissipation at the semiconductors is observed (see Figure 17) with a maximum temperature of 68 °C, thus ensuring a safe operating zone for the devices. Focusing on semiconductor losses, in simulation it is noticed that the conduction losses ($p_{\text{loss}}(t) = v_{\text{on}}(t) \cdot i_{\text{on}}(t)$) are dominating the switching losses($E = E_{\text{on}}(v_{\text{block}}, i_{\text{on}}, T)$ and $E = E_{\text{off}}(v_{\text{block}}, i_{\text{off}}, T)$), which might have a positive impact on the inverter efficiency. The losses incurred by the individual semiconductor devices are shown in Figure 18.

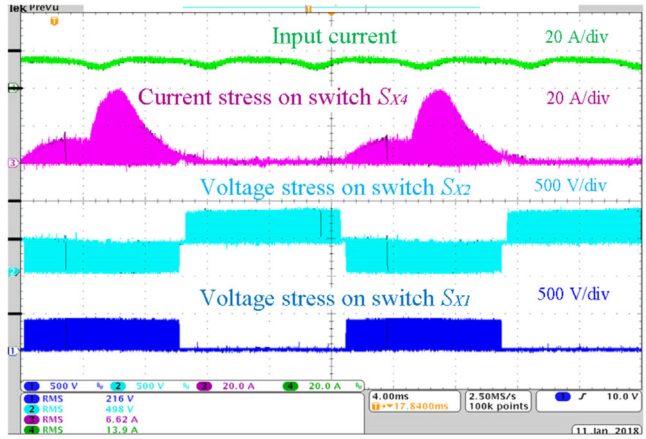


FIGURE 16 Measured voltage and current stress, on the MOSFETs in phase-1

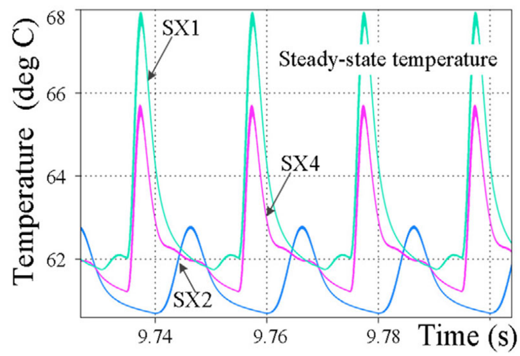


FIGURE 17 Simulated thermal behaviour of the semiconductors

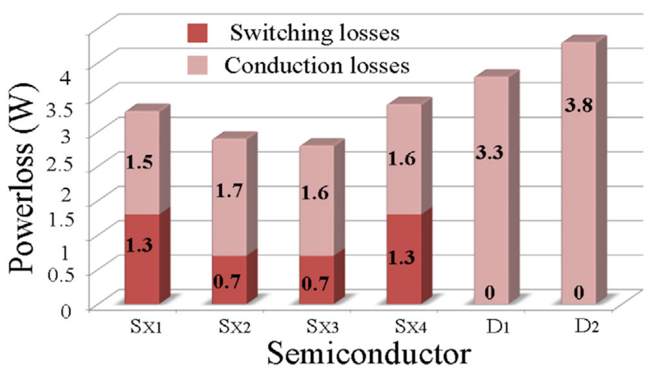


FIGURE 18 Simulated switching and conduction losses of the power switches

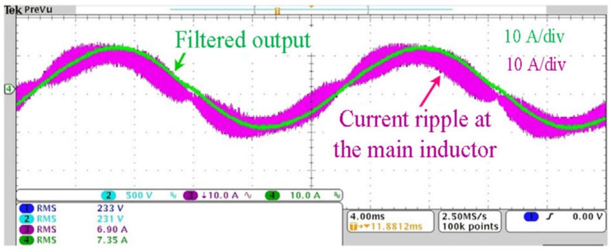


FIGURE 19 Measured converter output current before and after the filter

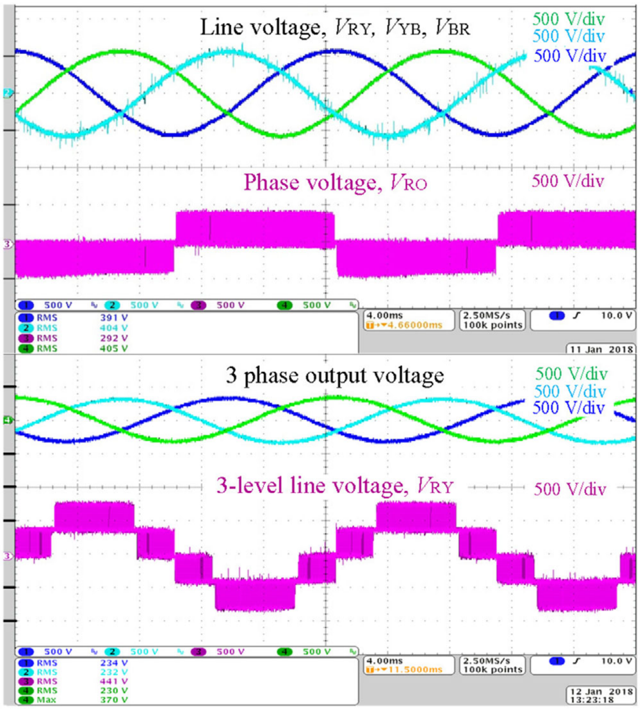


FIGURE 20 Measured three level voltage (unfiltered), filtered output voltage, phase voltage (unfiltered) and line voltage

The LCL filter has provided better ripple attenuation with a maximum peak to peak amplitude at the main inductor of around 6.4 A, while the ripple at the grid inductor is only 84 mA (see Figure 19). Operating at an input voltage of 400 V under a resistive load of 32 Ω for a 40 kHz switching frequency, the desired rms voltage of 230 V (400 $V_{LL}$) is obtained. The measure output waveforms are shown in Figure 20. A clean three level output voltage is observed, thus manifesting the inverter topology and the corresponding modulation technique is applicable for a three-level converter operation. A smooth output at the phase current is noticed with a peak of 10.3 A. The THD of the output current is observed (in simulation) around 2.2%, which is comparable to that of the conventional NPC topology.

A flat efficiency curve is derived based on the measurement results at different power levels (see Figure 21), with a full load (5 kW) efficiency of 97.53%. The thermal analysis on the hardware (see Figure 22) established uniform heat distribution with the device temperatures (max. 68.5 °C).

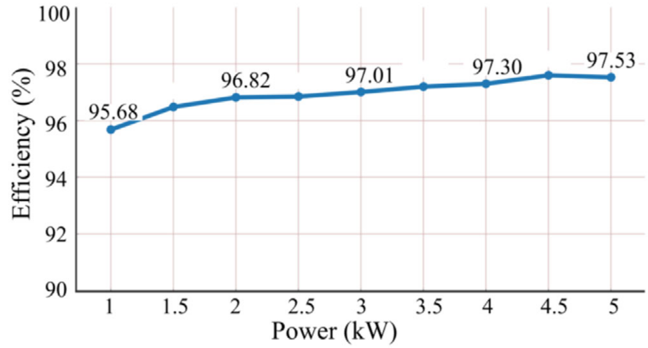


FIGURE 21 Power vs efficiency analysis

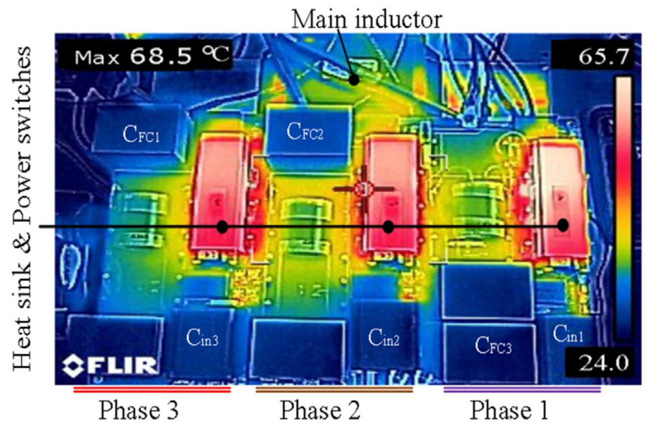


FIGURE 22 Thermal behaviour of the inverter circuit at full load

For evaluating the reactive power capability, a 33 mH inductive load was connected across load and the output voltage and current emphasising a lagging power factor (PF) of 0.93 was detected (see Figure 23). The efficiency under a reactive load at 1.2 kW power level is 97.4%, which is comparatively high to the efficiency of inverter at the same power level operating with a resistive load. The current supplied from the inductive load has reduced the power demand on the input side, thereby having a positive impact on the efficiency. It is apparent that this flying capacitor demonstrates a no harm operating mode, for inductive loads.

Figure 24(a) shows the comparative simulated waveforms of the proposed inverter with a DC-link voltage of 350 V and

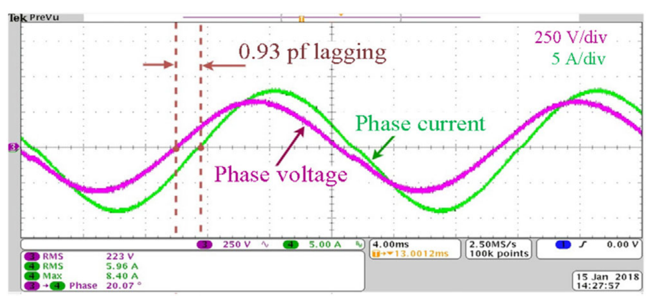


FIGURE 23 Operation of the inverter with reactive load

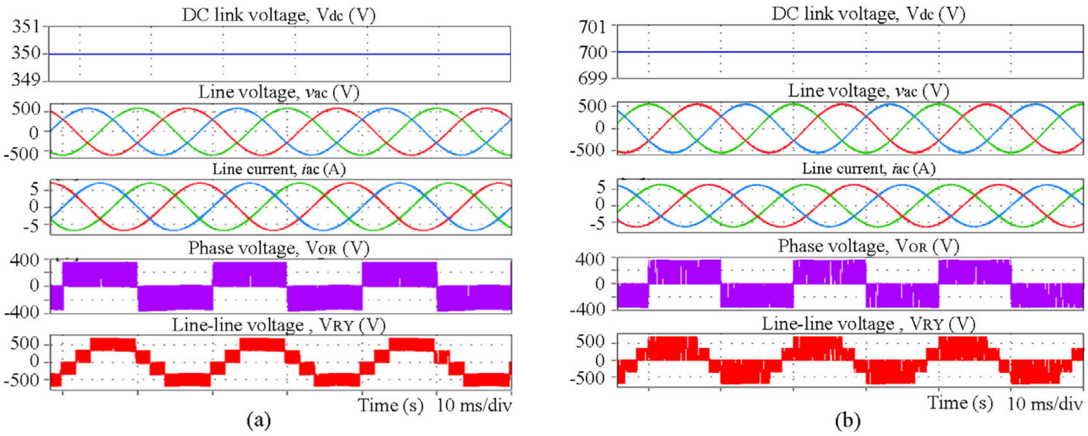


**FIGURE 24** Comparison of the simulated waveforms investigated on a, (a) three-level three-phase inverter flying capacitor boost inverter, (b) three-level three-phase diode clamped NPC inverter

Figure 24(b) shows the simulated waveforms of the conventional NPC inverter with a DC-link voltage of 700 V. Both inverters produce equal RMS voltage of about 400 $V_{LL}$ (230 $V_{ph}$) to a Y-connected load of 50 Ω each phase. The fifth trace in Figure 24(a) shows an unfiltered three-level line voltage, which is filtered out by a small filter (0.5 mH inductor and 2 $\mu$F capacitors in each phase) to get a pure sinusoidal voltage and current at the load. This preliminary simulation result shows a twofold reduction in input DC-link voltage compared to conventional three-level NPC topologies for the same output voltage. This will have a huge impact on the overall efficiency, cost and size of the system design as it eliminates the front-end large boost DC–DC converter. In addition, the proposed three-level topology reduces the number of components (both active and passive), high voltage insulation and spacing requirements and offers better voltage waveforms at the output. The closed-loop operation of the proposed topology was achieved my implementing a state-feedback controller in [21]. The Controller was able to establish the reference tracking with slight deviations in at zero crossing – at positive going: due to influence of dead-time and at negative going: sighting the abrupt change in the source (i.e. switching between input capacitor and the flying capacitor. Apart from the inherent deviations of the topology at zero crossing, a smooth synchronisation was achieved.

## 6 | CONCLUSION

A new three-level three-phase PWM inverter has been developed and investigated analytically as well as experimentally with a comparative study against the conventional 3L topologies. This inverter exhibits an inherent boost capability, offering a single-stage power conversion as an alternative for the conventional two-stage conversion technique. Looking on a comparative perspective for producing 230 $V_{rms}$ at the output, the conventional NPC inverters require 700–800 $V_{DC}$ at the input, whereas the developed inverter requires only 350–400 $V_{DC}$, as shown in Figure 24. Hence, reducing the DC-link voltage requirement by two fold. Therefore, it is apparent that the investigated inverter topology is suitable for various power conversion applications, such as variable speed motor drive systems and grid connected renewable energy systems.

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