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***Abstract* — In this paper, a vertical device structure and its process flow are proposed for fabrication of Gallium Nitride Trench Field Effect Transistors (GaNTT). A TCAD model is developed to capture effect of bulk and interface traps on the electrical performance of fully vertical Gallium Nitride devices on a Silicon Carbide substrate (GaN-on-SiC). The simulation results show a promising specific on-resistance of $R_{sp,on} = 1.4 m\Omega \cdot cm^2$ and a blocking voltage of $BV = 540V$ at V_{GS}=0V for a GaN drift thickness of 4 µm.**

Keywords—GaN, Trench, FETs, TCAD.

I. Introduction

Gallium Nitride (GaN) lateral devices [1-10] have been proliferating the power electronics industry. For power conversion applications, GaN vertical devices with reduced chip area are preferred over lateral GaN HEMT devices since blocking voltage can be scaled independently of the chip area and high value threshold voltages can be achieved. These will lead to a higher power density and more compact sized system. However, growing a few microns of GaN on a foreign substrate and achieving a high quality p-type doping in GaN remain challenging.

To make vertical GaN devices feasible, they need to be grown on a foreign substrate. Silicon (Si) is a cost effective option, but it has a large lattice mismatch with GaN (17%), similar to Sapphire (16%) [11]. Therefore, the resulting GaN-on-Si and GaN-on-Sapphire will feature a high density of Threading Dislocations (TDs), degrading the thermal conductivity of the epi-layers and affecting reliability of such devices [12], [13]. Diamond has been considered an emerging substrate featuring a reduced lattice mismatch of 11% to GaN, yet expensive with a considerable mismatch, enough to encourage high TDs density formation [14]. Silicon Carbide (SiC) has the same Wurtzite-hexagonal crystal structure with GaN, which largely reduces the lattice mismatch (3.4%) between the materials. Thus, GaN-on-SiC structure can be a more promising solution to enhance performance of vertically-structured gallium nitride devices [15].

For commercial success, there needs to be compelling reasons to use GaN on SiC instead of equivalent vertical SiC devices. It is worth considering that currently cost of thick GaN epi is more than the thick SiC epi needed for SiC devices with similar blocking capabilities.

The selection of a foreign substrate for GaN also comes with limitations on the process of activating dopants. The selective area doping in GaN is considered a major processing challenge and a key enabling step for vertical Field Effect Transistors (FETs) [16].

Although GaN begins to decompose at around 840ºC [17], it is relatively easy to accomplish n-type conduction by activating Silicon atoms at a post-annealing temperature lower than 1150ºC by utilizing Si_3N_4 or AlN protective capping layers [18]. On the other hand, the activation of p-type dopants in GaN requires a thermal budget of more than 1300ºC to remove the largely induced damages caused by the Mg ions and to move these impurities to proper lattice sites to substitute for Ga [18]. The utilisation of the Si_3N_4 or AlN protective capping layers during high temperature annealing process has not been successful for p-type doping due to crystallisation making their subsequent removal an issue [19]. Therefore, choosing a proper protective layer is essential [20].

The Multicycle Rapid Thermal Annealing (MRTA) method has been reported in the literature to achieve a high Mg activation ratio of 8%, yet it requires a specially treated system which is not easily scalable [21]. Currently, it is considered difficult to make good ohmic contacts on a p-GaN [22]. Furthermore, the challenge of activating Mg for p-type conductivity is more pronounced in the case of GaN-on-Si where the melting point of Silicon limits the post- annealing temperatures.

The GaN vertical trench Metal-Oxide-Semiconductor FET (MOSFET), combining normally-off operation with a low on-resistance, is an appealing technology for power conversion applications.

In [19], a fully vertical gate-trench GaN-on-Si power MOSFET is reported with 6.6µm thick GaN drift on top of a 6-inch Silicon substrate delivering a blocking voltage of

BV=520V and specific on-resistance ($R_{on,sp}$) of $5m\Omega \cdot cm^2$. A similar device in [10], with the same voltage class demonstrates $R_{on,sp} = 9.5m\Omega \cdot cm^2$, an indication of the questionable GaN-on-Si material quality. A thicker GaN-on-Sapphire epi-layer of 9 µm is utilized in [21] for the fabrication of an in-situ Oxide GaN interlayer-based vertical trench MOSFET (OG-FET) with 990V breakdown voltage and $R_{on,sp} = 2.6m\Omega \cdot cm^2$. For the 600V class, a vertical trench MOSFET based on 8µm thick GaN-on-GaN drift exhibited $R_{on,sp} = 6.4m\Omega \cdot cm^2$ [22]. Similarly, in [23], a freestanding $1.8m\Omega \cdot cm^2$ vertical trench MOSFET based on a 13µm thick drift obtained by homo-epitaxy (GaN-on-GaN) has been demonstrated for 1.2kV class operation.

In this paper, a vertical device structure and its process flow are proposed for fabrication of Gallium Nitride Trench Field Effect Transistors (GaNTT), exploiting the GaN-on-SiC potential. The electrical performance of proposed device is predicted by developing a physical TCAD model employing state-of-the-art material parameters [24], [25] and detailed trap profiles for a gallium nitride epitaxy on silicon carbide substrate. The simulation results predicts a blocking voltage of $BV = 540V$ at the off-state (V_{GS}=0V) with promising on-state characteristics, threshold voltage $V_{th} = 5.5V$ and specific on resistance of $R_{sp,on} = 1.4m\Omega \cdot cm^2$.

II. GaNTT Device Structure And Simulation Model

We target design and specification of vertical GaN trench MOSFETs for 200-600V class applications to grow $Al_xGa_{1-x}N$ layers on top of an n-type SiC substrate by MOCVD. The n-type GaN (n-GaN) is achieved by Silicon (Si) dopants and p-type GaN (p-GaN) is realized using Magnesium (Mg) atoms.

The designed wafer stack comprises 20nm n+GaN ($10^{19}cm^{-3}$), 200nm n-GaN ($5 \times 10^{18}cm^{-3}$), 400nm p-GaN ($2 \times 10^{17}cm^{-3}$), 4µm n-GaN ($2 \times 10^{16}cm^{-3}$), 1µm n+GaN ($10^{19}cm^{-3}$) and 1µm buffer layers grown respectively on a SiC substrate (see Fig.1(a)).

The process flow for fully vertical GaNTTs is illustrated in Fig. 1. The process features 1µm deep vertical gate trenches achieved with deployment of a SiO_2 hard mask (see Fig.1(b)) to realise 90 degrees side walls. The gate oxide is deposited (see Fig.1(c)). The gate metal deposition forms 1µm overlaps on each side of the trench (see Fig.1(d)) to enhance the design credibility against potential misalignments. Although this introduces an additional parasitic capacitance element, its effect is mitigated by the thick (400nm) SiO_2 hard mask layer. The hard mask is selectively removed to allow source metal deposition (see Fig.1(e)). The 2µm source trench (see Fig.1(f)) is formed to realize the p-body diode and source metal is deposited (see Fig.1(g)). Finally, substrate is thinned and drain metal is deposited (see Fig.1(h)).

The GaNTT device process architecture is innovative through the incorporation of a new contact concept forming Ohmic and Schottky contacts simultaneously. This will improve device performance by minimising threshold voltage fluctuations.

Simulations are time- and cost-efficient way of analysing and predicting performance of new device designs. A TCAD model will enable a more accurate prediction of device performance via the Finite Element analysis. Therefore, we developed an advanced TCAD model to simulate a GaNTT

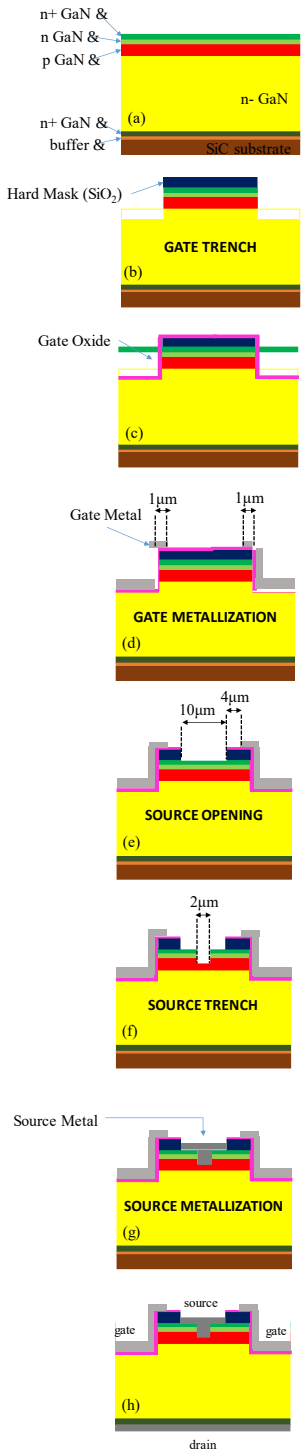

Fig. 1: GaNTT process flow: (a) wafer as grown, (b) gate trench formation, (c) gate oxide deposition, (d) gate metal deposition, (e) source contact opening, (f) p-body diode opening, (g) source metallization, (h) substrate thinning and drain metal deposition.

using drift-diffusion transport model, SRH and Auger recombination models, Fermi-Dirac statistics and material parameter values imported to simulation models from the literature [24], [25]. The self-heating effects have been neglected.

We incorporated defects and interface states in our simulation according to previously reported traps in n-GaN and p-GaN layers and fixed charges existing at the interface of GaN and SiO_2 layers.

In n-GaN bulk layer two electron traps (ET) are considered. One is located at $E_{T1} = E_C - 0.6eV$ with a capture cross-section of $\sigma = 5 \times 10^{-15} cm^2$. Its density D_{ET1} is a function of Silicon doping level [26]. Therefore, we consider $D_{ET1} = 8 \times 10^{14} cm^{-3}$ [27] in the drift region. Another trap level is located at $E_{T2} = E_C - 1eV$ with a capture cross section of $\sigma = 10^{-13} cm^2$ and a density of $D_{ET2} = 2 \times 10^{14} cm^{-3}$ and has been attributed to point defect complexes decorating dislocations [28]. The modelled ET1 and ET2 correspond to very prominent bulk centres in n-GaN and their density has been associated with the density of extensive defects.

The density of the formed TDs in GaN-on-SiC has been determined to be $N_{DD} = 10^{18} cm^{-2}$, the least defective case for GaN grown on a foreign substrate [11], [29]. Utilizing (1), where *c* stands for the GaN lattice constant in *c*-axis, N_{DD} (in cm^{-2}) is translated to volume concentration N_t (in cm^{-3}) [30], [31]. Substituting the $N_{DD} = 10^{18} cm^{-2}$ for the GaN-on-SiC, the resulting N_t value matches the sum of the two modelled electron trap densities in n-GaN ($D_{ET1} + D_{ET2}$) considered in our model.

$$N_t = N_{DD}/c \quad (1)$$

In n-GaN bulk layer, hole traps (HT) are also modelled. One is located at $E_{HT1} = E_V + 0.95eV$ with capture cross section of $\sigma = 2 \times 10^{-13} cm^2$ which has been linked with doubly negatively charged Gallium (Ga) vacancy complexes with Silicon ($V_{Ga} - Si$). Its density D_{HT1} increases with the Silicon doping level. Therefore, we consider $D_{HT1} = 1.6x10^{15} cm^{-3}$ [32] in the drift layer. Another trap level is located at $E_{HT2} = E_V + 1.1eV$ with capture cross section of $\sigma = 5 \times 10^{-12} cm^2$ and density of $D_{HT2} = 4 \times 10^{15} cm^{-3}$ [32]. The HT2 is associated with the $V_{Ga} - O$ defect and considered as a dominant trap in n-GaN demonstrates much higher thermal stability compared to the $V_{Ga} - Si$ complexes, modelled as HT1 in this work.

In p-GaN bulk layer, two hole traps are modelled in this work. One is located at $E_{HT3} = E_V + 0.45eV$ with capture cross section of $\sigma = 2.1 \times 10^{-15} cm^2$. It is a common deep centre in Mg doped GaN grown by MOCVD and has been linked with native Nitrogen (N) vacancies (V_N) [33] . Another trap level is located at $E_{HT4} = E_V + 0.88eV$ with capture cross section of $\sigma = 7.5 \times 10^{-14} cm^2$. It has been ascribed to carbon on nitrogen sites (C_N) [34]. The densities of the HT3 and HT4 have been estimated as 2% and 20% of the GaNTT doping levels correspondingly [35], [36].

Further to the bulk traps, interface states at the GaN/SiO_2 are included in the model [37]. These states demonstrate an acceptor-like or donor-like behavior. The acceptor-like states are considered neutral when they are occupied by a hole, whilst they become negatively charged when ionized by capturing an electron. On the contrary, donor-like states are neutral when occupied by an electron and they become positively charged when ionized by capturing a hole. In particular, for n-channel MOS devices, the acceptor-like states are significant as they are considered responsible for the scattering of free carriers.

The interface states at the GaN/SiO_2 are modelled in this work comprising acceptor-like states with energy intervals close to the conduction band (E_C) and donor-like states with energy intervals close to the valence band (E_V). The modelled distributions of both acceptor- and donor-like states are presented in Table I [38]. These states are spatially located at the interface and modeled with a Gaussian distribution. The listed E_{Mid} and E_{Sig} levels represent the mean and sigma properties of each distribution.

Table I. Modelled Gaussian distributions of donor like and acceptor like states at the interface of GaN and SiO_2 layers.

GaN/SiO_2	Density (cm^{-2})	Energetic Distribution
Acceptor-like states	1×10^{12}	Uniform Band $E_{Mid}^{from\ E_C} = 0.15eV$, $E_{Sig}0.3eV$
	5×10^{11}	Uniform Band $E_{Mid}^{from\ E_C} = 0.35eV$, $E_{Sig}0.1eV$
	1×10^{11}	Uniform Band $E_{Mid}^{from\ E_C} = 0.5eV$, $E_{SigM} = 0.2eV$
Donor-like states	1×10^{12}	Uniform Band $E_{Mid}^{from\ E_V} = 0.1eV$, $E_{SigM} = 0.2eV$
	5×10^{11}	Uniform Band $E_{Mid}^{from\ E_V} = 0.3eV$, $E_{SigM} = 0.2eV$
	2×10^{11}	Uniform Band $E_{Mid}^{from\ E_V} = 0.5eV$, $E_{SigM} = 0.2eV$

The fixed charge (FC) at the interface between the GaN and the SiO_2 could be either positive or negative depending on whether the oxide is grown on the N- or the Ga-polar face. Assuming the SiO_2 is grown on Ga-polar GaN surface, a positive dielectric FCs is also modelled at the GaN/SiO_2 as a design variable with density values ranging $1 \times 10^{12} - 2 \times 10^{12} cm^{-2}$ [39], [40].

On account of the challenging activation of the acceptor dopants in GaN, relatively low Mg doping concentrations are considered for the GaNTT device, namely $1 \times 10^{17} - 2.2 \times 10^{17} cm^{-3}$. In turn, given the fixed thickness of the p-GaN layer, this could contribute to a reduced channel resistance.

Two gate metals were investigated with workfunction values of $WF_1 = 4.53\ eV$ and $WF_2 = 5.15\ eV$, for Molybdenum (Mo) and Nickel (Ni) contacts. Simulation results for Nickel is presented in this paper.

Simulated GaNTT doping profile is illustrated in Fig. 2. To improve the simulation runtime, SiC substrate contribution is incorporated as an additive resistance to the drain electrode.

To capture effect of traps on electrical performance of the GaNTT device, meshing is carefully defined. The mesh is finer around the channel and coarser in other areas, as shown in Fig. 3. Finally, a proper area factor value was determined to emulate the 100μm width of the single cell device.

III. Results and Discussion

The proposed GaNTT design is verified through cell simulations using TCAD toolkit. The developed model is utilized to predict and improve the electrical performance of a fully vertical device including current levels, threshold voltage, blocking voltage capability and specific on-resistance.

Simulations suggest that high p-GaN doping leads to further improvement in reverse characteristics of the p-body diode. However, this could be compromised by the challenging activation of Mg dopants for p-type conductivity in GaN.

Increasing the FCs density value at the GaN/SiO_2 interface degrades the blocking capabilities for a particular p-GaN doping level. A gate metal with larger workfunction mitigates this effect in the expense of a larger V_{th} value.

Simulations reveal that a thinner gate oxide is a more beneficial choice towards reducing the effect from the FCs and the ionized traps at the GaN/SiO_2.

Fig. 4 is IV transfer characteristics of the fully vertical GaNTT device at V_{DS}=0.5V with 4µm drift region showing a normally-off device with threshold voltage of $V_{th} = 5.5V$ at which resistive p-GaN becomes conductive through generation of an inversion layer. The inversion layer forms a continuous path between the source and drain contacts.

Fig. 5 is output IV characteristics of the simulated fully vertical GaNTT with 5.6 µm of gallium nitride epi layers on top of a 1µm buffer at different gate biases with the steps of 2V from V_{GS}=4V to V_{GS}=14V.

The GaNTT design with oxide thickness of $t_{ox} = 60nm$, p-body doping of $N_{Mg} = 2.2 \times 10^{17} cm^{-3}$ and Nickel as gate metal exhibits promising on-state characteristics with a specific on-resistance of $R_{sp,on} = 1.4m\Omega \cdot cm^2$ at $V_G = 10V$.

Fig. 6 is simulated electric field distribution of the proposed GaNTT device at breakdown when a reverse current of $I_r = 10^{-4}\, A/\mu m^2$is reached.

For the forward blocking operation, the proposed GaNTT design exhibited blocking capabilities of $BV = 540V$ at reverse current of $I_r = 10^{-4}\, A/\mu m^2$ for a moderate fixed charge density of $1.5 \times 10^{12} cm^{-2}$. Since the onset of avalanche was not reached at the simulations, the breakdown voltage is considered to be the V_{DS} at which the reverse current of is observed. Simulation with a higher fixed charge density of FC $= 2 \times 10^{12} cm^{-2}$ led to reduced blocking voltage capability at $BV = 420V$.

Fig. 7 is forward blocking performance compared to measurements from two similar fully vertical GaN-on-Si trench MOSFETs. The observed difference in the leakage current could be attributed to the better quality of the GaN-on-SiC material considered in the GaNTT device model.

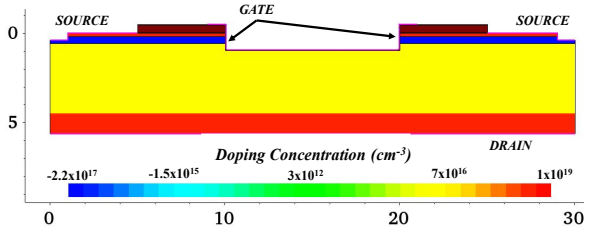

Fig. 2: Doping profile in GaNTT device modelled using TCAD toolkit. SiC substrate contribution during on-state is included as an additive resistance value at the drain electrode.

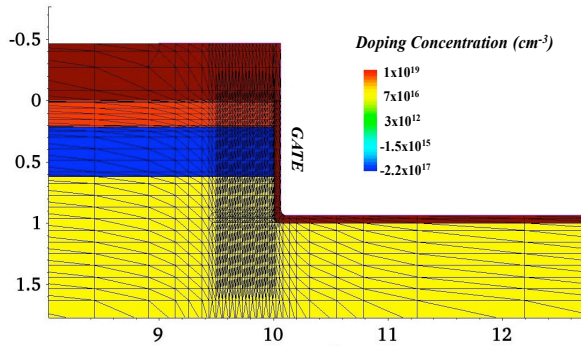

Fig. 3: A fine meshing profile defined to optimise simulation runtime and capture effect of traps incorporated in model.

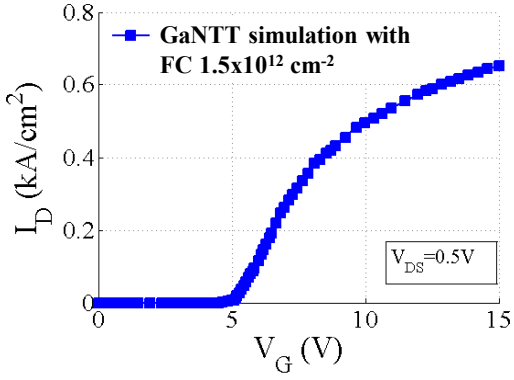

Fig. 4: Predicted transfer characteristics of GaNTT design with oxide thickness of 60nm employing Nickel for gate metal and fixed charge of FC = 1.5 × $10^{12} cm^{-2}$between GaN and SiO_2 interface.

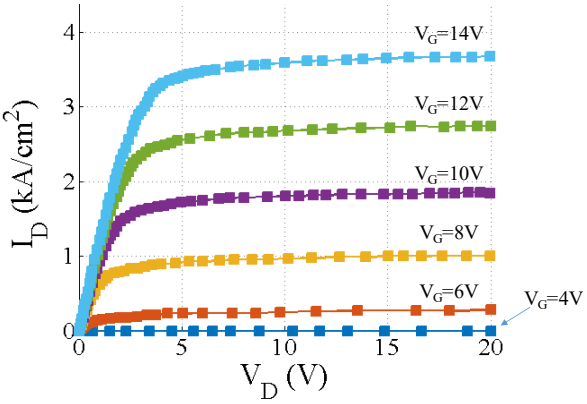

Fig. 5: Predicted family of curves for proposed GaNTT design with oxide thickness of 60nm employing Nickel for gate metal and interface state of FC = 1.5 × $10^{12} cm^{-2}$between GaN and SiO

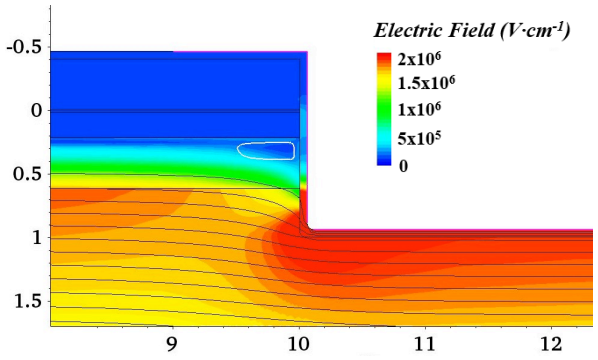

Fig. 6: Electric field distribution of proposed GaNTT design modelled at V_{DS}= 540V and V_{GS}=0V with Nickel as gate metal considering fixed interface charge of FC = 1.5 × $10^{12} cm^{-2}$between GaN and SiO_2. The potential lines are superimposed in black, whilst depletion region is in white.

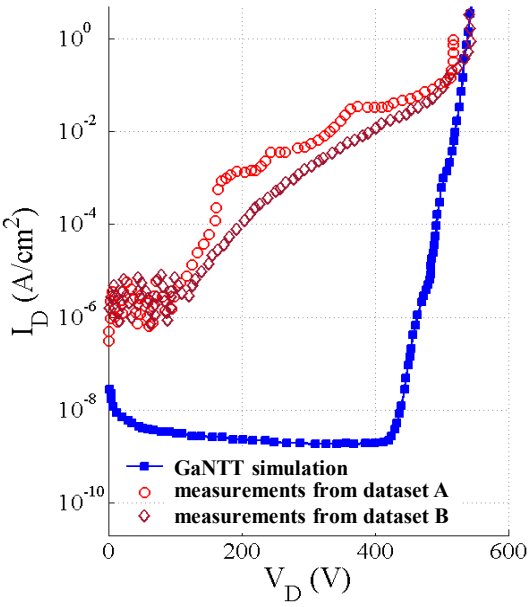

Fig.7: Predicted blocking voltage of proposed GaNTT design with GaN and SiO_2 interface charge of FC = $1.5 \times 10^{12} cm^{2-}$compared to measured datasets A [19] and B [20].

IV. Conclussions

In this paper, we presented a methodology for simulation of vertical gallium nitride field effect transistors and developed an advanced TCAD model to reflect the current state-of-the-art GaN-on-SiC technology. The model was utilized to predict the electrical performance of the proposed trenched device. Although highly p-type doped gallium nitride remains a challenge, simulations predict a promising and scalable device performance for 600V class applications with a practical doping level of $2 \times 10^{17} cm^{-3}$. In addition, blocking voltage found to be dependent on the charge density at the interface of GaN and SiO_2 layers.

Acknowledgment

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